

500mA, Ultralow Noise, Ultrahigh PSRR Negative Linear Regulator for Commercial Space

FEATURES

- ▶ **No Single-Event Latch-Up (SEL) up to $79.9\text{MeV} \times \text{cm}^2/\text{mg}$ at $V_{\text{IN}} \leq 16\text{V}$**
- ▶ **Total Ionizing Dose (TID) Assured up to 30kRad**
- ▶ **Ultralow Root Mean Square (RMS) Noise: $0.8\mu\text{V}_{\text{RMS}}$ (10Hz to 100kHz)**
- ▶ **Ultralow Spot Noise: $2.2\text{nV}/\sqrt{\text{Hz}}$ at 10kHz**
- ▶ **Ultrahigh Power Supply Rejection Ratio (PSRR): 74dB at 1MHz**
- ▶ **Output Current: 500mA**
- ▶ **Wide Input Voltage Range: -2.3V to -20V**
- ▶ **A Single Capacitor Improves Noise and PSRR**
- ▶ **100 μA SET Pin Current: $\pm 1\%$ Initial Accuracy**
- ▶ Single Resistor Programs Output Voltage
- ▶ Programmable Current Limit
- ▶ Low Dropout Voltage: 235mV
- ▶ Output Voltage Range: 0V to -19.5V
- ▶ Programmable Power Good and Fast Start-Up
- ▶ Bipolar Precision Enable/ Undervoltage Lockout (UVLO) Pin
- ▶ Voltage Input-to-Output Control (VIOC) Pin Controls Upstream Regulator to Minimize Power Dissipation and Optimize Power Supply Rejection Ratio (PSRR)
- ▶ Minimum Output Capacitor: 10 μF Ceramic Capacitor
- ▶ 12-Lead MSOP Package

COMMERCIAL SPACE FEATURES

- ▶ Supports Aerospace Applications
- ▶ Wafer Diffusion Lot Traceability
- ▶ Radiation Monitors
 - ▶ Single-Event Latch-Up (SEL)
 - ▶ Total Ionizing Dose (TID)
- ▶ Outgassing Characterization
- ▶ Nickel Palladium Gold (NiPdAu) Terminal Finish

GENERAL DESCRIPTION

The RHP51002 is a high-performance, low-dropout negative linear regulator featuring Analog Devices' ultralow-noise, ultrahigh PSRR architecture for powering noise-sensitive applications. The device can be easily paralleled to further reduce noise, increase output current, and spread heat across a printed circuit board (PCB).

The device supplies 500mA with a typical dropout voltage of 235mV. Operating quiescent current is nominally 2.35mA and drops to 3 μA in shutdown. The device's wide output voltage range (0V to -19.5V) error amplifier operates in unity-gain and provides virtually constant output noise, PSRR, bandwidth, and load regulation independent of the programmed output voltage. Additional features include a bipolar enable pin, programmable current limit, fast-startup capability, and a programmable power good to indicate output-voltage regulation. The regulator incorporates a tracking function that controls the upstream supply to maintain a constant voltage across the RHP51002, minimizing power dissipation and optimizing PSRR.

The device is stable with a minimum of 10 μF ceramic output capacitor. Built-in protection includes an internal current limit with foldback and a thermal limit with hysteresis. The RHP51002 is available in a thermally enhanced 12-lead micro small outline Package (MSOP).

APPLICATIONS

- ▶ Low Earth Orbit (LEO) Satellites
- ▶ Avionics
- ▶ Point-to-Point Communication Systems
- ▶ Very Low Noise Instrumentation
- ▶ High Speed/High Precision Data Converters
- ▶ Post-Regulator for Switching Supplies

TYPICAL APPLICATION

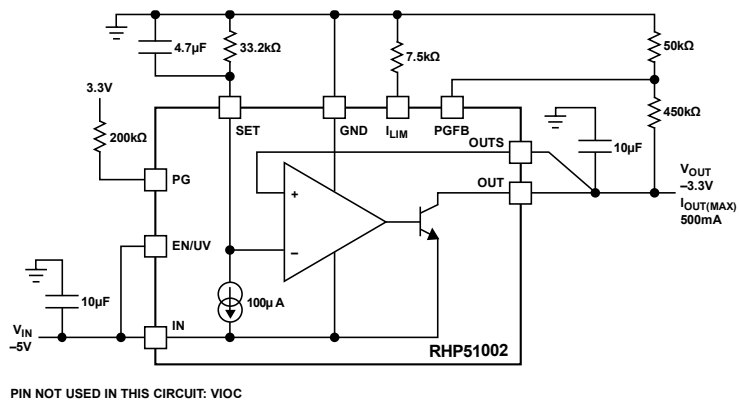


Figure 1. Typical Application Circuit

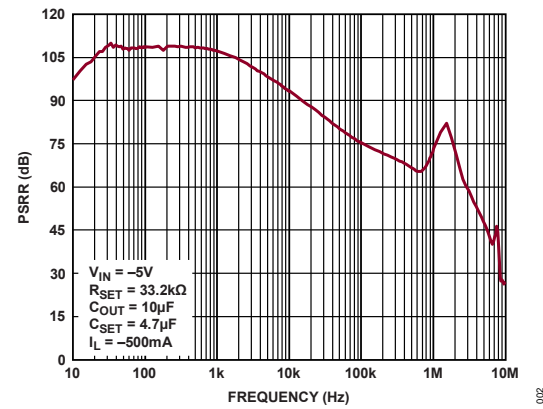


Figure 2. Power Supply Ripple Rejection

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	10/26	Initial Release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(The $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ denotes the specifications that apply over the full operating temperature range; otherwise, specifications are at $T_A = 25^{\circ}\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	$I_{LOAD} = 500\text{mA}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	-20		-2.3	V
Minimum IN Pin Voltage ⁷		$I_{LOAD} = 500\text{mA}$, V_{IN} UVLO Rising	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	-2.3	-1.8		V
		V_{IN} UVLO Hysteresis			130		mV
SET Pin Current	I_{SET}	$V_{IN} = -2.3\text{V}$, $I_{LOAD} = 1\text{mA}$, $V_{OUT} = -1.5\text{V}$		99	100	101	μA
		$-20\text{V} < V_{IN} < -2.3\text{V}$, $-19.5\text{V} < V_{OUT} < 0\text{V}$, $1\text{mA} < I_{LOAD} < 500\text{mA}$ ⁶	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	98	100	102	μA
Fast Start-Up SET Pin Current		$V_{PGFB} = -286\text{mV}$, $V_{IN} = -2.3\text{V}$, $V_{SET} = -1.5\text{V}$			1.8		mA
Output Offset Voltage ($V_{OUT} - V_{SET}$) ⁸	V_{OS}	$V_{IN} = -2.3\text{V}$, $I_{LOAD} = 1\text{mA}$, $V_{OUT} = -1.5\text{V}$		-1		1	mV
		$-20\text{V} < V_{IN} < -2.3\text{V}$, $-19.5\text{V} < V_{OUT} < 0\text{V}$, $1\text{mA} < I_{LOAD} < 500\text{mA}$ ⁶	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	-2		2	mV
Line Regulation	ΔI_{SET}	$V_{IN} = -2.3\text{V}$ to -20V , $I_{LOAD} = 1\text{mA}$, $V_{OUT} = -1.5\text{V}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	-5	0.5	5	nA/V
	ΔV_{OS}	$V_{IN} = -2.3\text{V}$ to -20V , $I_{LOAD} = 1\text{mA}$, $V_{OUT} = -1.5\text{V}$ ⁸	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	-6	0.1	6	$\mu\text{V/V}$
Load Regulation	ΔI_{SET}	$I_{LOAD} = 1\text{mA}$ to 500mA , $V_{IN} = -2.3\text{V}$, $V_{OUT} = -1.5\text{V}$			0.1		nA
	ΔV_{OS}	$I_{LOAD} = 1\text{mA}$ to 500mA , $V_{IN} = -2.3\text{V}$, $V_{OUT} = -1.5\text{V}$ ⁸	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		0.03	0.5	mV
Change in I_{SET} with V_{SET}		$V_{SET} = -1.5\text{V}$ to -19.5V , $V_{IN} = -20\text{V}$, $I_{LOAD} = 1\text{mA}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		100	850	nA
Change in V_{OS} with V_{SET}		$V_{SET} = -1.5\text{V}$ to -19.5V , $V_{IN} = -20\text{V}$, $I_{LOAD} = 1\text{mA}$ ⁸	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		0.02	0.5	mV
Change in I_{SET} with V_{SET}		$V_{SET} = 0\text{V}$ to -1.5V , $V_{IN} = -20\text{V}$, $I_{LOAD} = 1\text{mA}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		150	500	nA

(The $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ denotes the specifications that apply over the full operating temperature range; otherwise, specifications are at $T_A = 25^{\circ}\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Change in V_{OS} with V_{SET}		$V_{SET} = 0\text{V to } -1.5\text{V}$, $V_{IN} = -20\text{V}$, $I_{LOAD} = 1\text{mA}$ ⁸	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		0.15	2	mV
Dropout Voltage ⁹		$I_{LOAD} = 1\text{mA}, 50\text{mA}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		185	225	mV
			$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$			275	mV
		$I_{LOAD} = 100\text{mA}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		185	230	mV
			$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$			280	mV
		$I_{LOAD} = 500\text{mA}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		235	310	mV
			$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$			410	mV
GND Pin Current $V_{IN} = V_{OUT(NOMINAL)}$ ¹⁰		$I_{LOAD} = 10\mu\text{A}$			2.35		mA
		$I_{LOAD} = 1\text{mA}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		2.4	4	mA
		$I_{LOAD} = 50\text{mA}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		3.1	5.5	mA
		$I_{LOAD} = 100\text{mA}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		3.8	6.5	mA
		$I_{LOAD} = 500\text{mA}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		12	23	mA
Output Noise Spectral Density ^{8, 11}		$I_{LOAD} = 500\text{mA}$, Frequency = 10Hz, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 0.47\mu\text{F}$, $V_{OUT} = -3.3\text{V}$			700		nV/ $\sqrt{\text{Hz}}$
		$I_{LOAD} = 500\text{mA}$, Frequency = 10Hz, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 4.7\mu\text{F}$, $-19.5\text{V} \leq V_{OUT} \leq -1.5\text{V}$			70		nV/ $\sqrt{\text{Hz}}$
		$I_{LOAD} = 500\text{mA}$, Frequency = 10kHz, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 0.47\mu\text{F}$, $-19.5\text{V} \leq V_{OUT} \leq -1.5\text{V}$			2.2		nV/ $\sqrt{\text{Hz}}$
		$I_{LOAD} = 500\text{mA}$, Frequency = 10kHz, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 0.47\mu\text{F}$, $-1.5\text{V} \leq V_{OUT} \leq 0\text{V}$			6		nV/ $\sqrt{\text{Hz}}$

(The $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ denotes the specifications that apply over the full operating temperature range; otherwise, specifications are at $T_A = 25^{\circ}\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Output Root Mean Square (RMS) Noise 8, 11		$I_{\text{LOAD}} = 500\text{mA}$, BW = 10Hz to 100kHz, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 0.47\mu\text{F}$, $V_{\text{OUT}} = -3.3\text{V}$			3		μV_{RMS}
		$I_{\text{LOAD}} = 500\text{mA}$, BW = 10Hz to 100kHz, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 4.7\mu\text{F}$, $-19.5\text{V} \leq V_{\text{OUT}} \leq -1.5\text{V}$			0.8		μV_{RMS}
		$I_{\text{LOAD}} = 500\text{mA}$, BW = 10Hz to 100kHz, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 4.7\mu\text{F}$, $-1.5\text{V} \leq V_{\text{OUT}} \leq 0\text{V}$			1.8		μV_{RMS}
Reference Current RMS Output Noise 8, 11		BW = 10Hz to 100kHz			8		nA_{RMS}
Ripple Rejection $-18\text{V} \leq V_{\text{OUT}} \leq -1.5\text{V}$, $V_{\text{IN}} - V_{\text{OUT}} = 2\text{V}$ (Avg) 8, 11		$V_{\text{RIPPLE}} = 500\text{mV}_{\text{P-P}}$, $f_{\text{RIPPLE}} = 120\text{Hz}$, $I_{\text{LOAD}} = 500\text{mA}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 4.7\mu\text{F}$			108		dB
		$V_{\text{RIPPLE}} = 500\text{mV}_{\text{P-P}}$, $f_{\text{RIPPLE}} = 10\text{kHz}$, $I_{\text{LOAD}} = 500\text{mA}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 0.47\mu\text{F}$			94		dB
		$V_{\text{RIPPLE}} = 500\text{mV}_{\text{P-P}}$, $f_{\text{RIPPLE}} = 100\text{kHz}$, $I_{\text{LOAD}} = 500\text{mA}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 0.47\mu\text{F}$			75		dB
		$V_{\text{RIPPLE}} = 500\text{mV}_{\text{P-P}}$, $f_{\text{RIPPLE}} = 1\text{MHz}$, $I_{\text{LOAD}} = 500\text{mA}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 0.47\mu\text{F}$			74		dB
		$V_{\text{RIPPLE}} = 500\text{mV}_{\text{P-P}}$, $f_{\text{RIPPLE}} = 10\text{MHz}$, $I_{\text{LOAD}} = 500\text{mA}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 0.47\mu\text{F}$			28		dB
Ripple Rejection $-1.5\text{V} \leq V_{\text{OUT}} \leq 0\text{V}$, $V_{\text{IN}} - V_{\text{OUT}} = 2\text{V}$ (Avg) 8, 11		$V_{\text{RIPPLE}} = 500\text{mV}_{\text{P-P}}$, $f_{\text{RIPPLE}} = 120\text{Hz}$, $I_{\text{LOAD}} = 500\text{mA}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 4.7\mu\text{F}$			108		dB
		$V_{\text{RIPPLE}} = 500\text{mV}_{\text{P-P}}$, $f_{\text{RIPPLE}} = 10\text{kHz}$, $I_{\text{LOAD}} = 500\text{mA}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 0.47\mu\text{F}$			90		dB

(The $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ denotes the specifications that apply over the full operating temperature range; otherwise, specifications are at $T_A = 25^{\circ}\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Ripple Rejection $-1.5\text{V} \leq V_{\text{OUT}} \leq 0\text{V}$, $V_{\text{IN}} - V_{\text{OUT}} = 2\text{V}$ (Avg) 8, 11		$V_{\text{RIPPLE}} = 500\text{mV}_{\text{p-p}}$, $f_{\text{RIPPLE}} = 100\text{kHz}$, $I_{\text{LOAD}} = 500\text{mA}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 0.47\mu\text{F}$			72		dB
		$V_{\text{RIPPLE}} = 500\text{mV}_{\text{p-p}}$, $f_{\text{RIPPLE}} = 1\text{MHz}$, $I_{\text{LOAD}} = 500\text{mA}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 0.47\mu\text{F}$			78		dB
		$V_{\text{RIPPLE}} = 500\text{mV}_{\text{p-p}}$, $f_{\text{RIPPLE}} = 10\text{MHz}$, $I_{\text{LOAD}} = 500\text{mA}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 0.47\mu\text{F}$			30		dB
EN/UV Pin Threshold		Positive EN/UV Trip Point Rising (Turn-on), $V_{\text{IN}} = -2.3\text{V}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	1.20	1.26	1.35	V
		Negative EN/UV Trip Point Rising (Turn-on), $V_{\text{IN}} = -2.3\text{V}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	-1.33	-1.26	-1.20	V
EN/UV Pin Hysteresis		Positive EN/UV Trip Point Hysteresis, $V_{\text{IN}} = -2.3\text{V}$			200		mV
		Negative EN/UV Trip Point Hysteresis, $V_{\text{IN}} = -2.3\text{V}$			215		mV
EN/UV Pin Current		$V_{\text{EN/UV}} = 0\text{V}$, $V_{\text{IN}} = -20\text{V}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	-1		1	μA
		$V_{\text{EN/UV}} = -1.5\text{V}$, $V_{\text{IN}} = -20\text{V}$			-0.5		μA
		$V_{\text{EN/UV}} = -20\text{V}$, $V_{\text{IN}} = -20\text{V}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	-35	-18.5		μA

(The $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ denotes the specifications that apply over the full operating temperature range; otherwise, specifications are at $T_A = 25^{\circ}\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
		$V_{\text{EN/UV}} = 1.5\text{V}, V_{\text{IN}} = -20\text{V}$			8		μA
		$V_{\text{EN/UV}} = 20\text{V}, V_{\text{IN}} = 0\text{V}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		25	45	μA
Quiescent Current in Shutdown (VEN/UV = 0V)		$V_{\text{IN}} = -6\text{V}, V_{\text{PG}} = \text{Open}$			3	8	μA
			$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$			10	μA
Internal Current Limit ¹³		$V_{\text{IN}} = -2.3\text{V}, V_{\text{OUT}} = 0\text{V}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	550	750		mA
		$V_{\text{IN}} = -12\text{V}, V_{\text{OUT}} = 0\text{V}$			425		mA
		$V_{\text{IN}} = -20\text{V}, V_{\text{OUT}} = 0\text{V}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	40	85	160	mA
Programmable Current Limit		Programming Scale Factor: $-20\text{V} < V_{\text{IN}} < -2.3\text{V}$ ¹²			3.75		A x k Ω
		$V_{\text{IN}} = -2.3\text{V}, V_{\text{OUT}} = 0\text{V}, R_{\text{ILIM}} = 7.5\text{k}\Omega$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	450	500	560	mA
		$V_{\text{IN}} = -2.3\text{V}, V_{\text{OUT}} = 0\text{V}, R_{\text{ILIM}} = 37.5\text{k}\Omega$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	90	105	120	mA
PGFB Trip Point		PGFB Trip Point Rising	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	288	300	312	mV
PGFB Hysteresis		PGFB Trip Point Hysteresis			7		mV
PGFB Pin Current		$V_{\text{IN}} = -2.3\text{V}, V_{\text{PGFB}} = -300\text{mV}$			30	100	nA
PG Output Low Voltage		$I_{\text{PG}} = 100\mu\text{A}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		17	50	mV

(The $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ denotes the specifications that apply over the full operating temperature range; otherwise, specifications are at $T_A = 25^{\circ}\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
PG Leakage Current		$V_{PG} = 20\text{V}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$			1	μA
VIOC Amplifier Gain		$-20\text{V} \leq V_{IN} \leq -2.3\text{V}, V_{OUT} \leq -1.5\text{V}$			1		V/V
VIOC Maximum Output Voltage Swing		$V_{IN} - V_{OUT} = -2\text{V}, V_{OUT} \leq -1.5\text{V}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		-1.35	-1.2	V
VIOC Sink Current		$V_{IN} - V_{OUT} = -2\text{V}, V_{VIOC} = -1\text{V}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	100			μA
VIOC Voltage for Low Output Voltage ¹⁴		$V_{IN} = -2.3\text{V}, V_{OUT} > -1.5\text{V}$			-0.8		V
Minimum Load Current ¹⁵		$V_{OUT} > -1.5\text{V}$	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$			10	μA
Thermal Shutdown		T_J Rising			167		$^{\circ}\text{C}$
		Hysteresis			8		$^{\circ}\text{C}$
Start-Up Time		$R_{SET} = 49.9\text{k}\Omega, V_{OUT(NOM)} = -5\text{V}, I_{LOAD} = 500\text{mA}, C_{SET} = 0.47\mu\text{F}, V_{IN} = -6\text{V}, V_{PGFB} = -6\text{V}$			55		ms
		$R_{SET} = 49.9\text{k}\Omega, V_{OUT(NOM)} = -5\text{V}, I_{LOAD} = 500\text{mA}, C_{SET} = 4.7\mu\text{F}, V_{IN} = -6\text{V}, V_{PGFB} = -6\text{V}$			550		ms
		$R_{SET} = 49.9\text{k}\Omega, V_{OUT(NOM)} = -5\text{V}, I_{LOAD} = 500\text{mA}, C_{SET} = 4.7\mu\text{F}, V_{IN} = -6\text{V}, R_{PG1} = 50\text{k}\Omega, R_{PG2} = 700\text{k}\Omega$ (with fast start-up to 90% of V_{OUT})			10		ms
Thermal Regulation		10ms Pulse			-0.01		%/W

¹ Parasitic diodes exist internally between the EN/UV, I_{LIM} , PG, PGFB, SET, GND, VIOC, OUTS, and OUT pins and the IN pin. Do not drive these pins more than 0.3V below the IN pin during a fault condition. These pins must remain at a voltage more positive than IN during normal operation.

The RHP51002 is tested and specified under pulse-load conditions such that $T_J \cong T_A$. The RHP51002 is 100% tested at $T_A = 25^\circ\text{C}$. The device's performance over the full -40°C to 125°C operating temperature range is assured by design, characterization, and correlation with statistical process controls. High junction temperatures degrade operating lifetimes. Derate operating lifetime at junction temperatures above 125°C .

The SET and OUTS pins are clamped using diodes and two 400Ω series resistors. For transients below 5ms, this clamp circuitry can carry more than the rated current.

Meet the maximum current requirements for the SET and OUTS pins.

The maximum OUT-to-OUTS differential is guaranteed by design.

Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply to all possible combinations of input voltage and output current, especially because of the internal current-limit foldback, which reduces the current limit at $V_{OUT} - V_{IN} > 7\text{V}$. If operating at maximum output current, limit the input voltage range. If operating at maximum input voltage, limit the output current range.

The EN/UV pin threshold must be met to ensure device operation.

OUTS ties directly to OUT.

Dropout voltage is the minimum input-to-output differential voltage required to maintain regulation at a specified output current. The dropout voltage is measured when the output is 1% out of regulation.

This definition results in a higher dropout voltage than hard dropout, which is measured when $V_{IN} = V_{OUT(NOMINAL)}$. For output voltages between 0V and -1.8V , dropout voltage is limited by the minimum input voltage specification.

GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ and a current-source load. Therefore, the device is tested while operating in dropout. This condition represents the worst-case GND pin current. GND pin current decreases at higher input voltages. Note that the GND pin current does not include the SET pin or I_{LIM} pin current, but they are included in the quiescent current.

Adding a capacitor across the SET pin resistor reduces output voltage noise. Adding this capacitor bypasses the SET pin resistor's thermal noise as well as the reference current's noise. The output noise then equals the error amplifier noise. Use of a SET pin bypass capacitor also increases start-up time.

The current limit programming scale factor is specified while the internal backup current limit is not active. Note that the internal current limit has foldback protection for $V_{OUT} - V_{IN}$ differentials greater than 7V.

The internal backup current-limit circuitry incorporates foldback protection that decreases the current limit for $V_{OUT} - V_{IN} > 7\text{V}$. Some level of output current is provided for all $V_{OUT} - V_{IN}$ differential voltages. See the [Typical Performance Characteristics](#) graph for current limit vs. $V_{IN} - V_{OUT}$.

The VIOC amplifier outputs a voltage equal to $V_{IN} - V_{OUT}$ or $V_{IN} + 1.5\text{V}$ (when V_{OUT} is between 0V and -1.5V). See the [Block Diagram](#) and [Applications Information](#) for more information.

For output voltages between 0V and -1.5V , the RHP51002 requires a $10\mu\text{A}$ minimum load current for stability.

Table 2. Radiation Test Limits and Specifications

(All minimum and maximum specifications are at T_J (Junction Temperature) = 25°C. Total ionizing dose (TID) testing is characterized to 30krads.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	$I_{LOAD} = 500mA$	-20		-2.3	V
Minimum IN Pin Voltage ⁷		$I_{LOAD} = 500mA$, V_{IN} UVLO Rising	-2.3	-1.8		V
		V_{IN} UVLO Hysteresis		130		mV
SET Pin Current	I_{SET}	$V_{IN} = -2.3V$, $I_{LOAD} = 1mA$, $V_{OUT} = -1.5V$	93	100	101	μA
		$-20V < V_{IN} < -2.3V$, $-19.5V < V_{OUT} < 0V$, $1mA < I_{LOAD} < 500mA$ ⁶	93	100	102	μA
Fast Start-Up SET Pin Current		$V_{PGFB} = -286mV$, $V_{IN} = -2.3V$, $V_{SET} = -1.5V$		1.8		mA
Output Offset Voltage ($V_{OUT} - V_{SET}$) ⁸	V_{OS}	$V_{IN} = -2.3V$, $I_{LOAD} = 1mA$, $V_{OUT} = -1.5V$	-1		1	mV
		$-20V < V_{IN} < -2.3V$, $-19.5V < V_{OUT} < 0V$, $1mA < I_{LOAD} < 500mA$ ⁶	-2		2	mV
Line Regulation	ΔI_{SET}	$V_{IN} = -2.3V$ to $-20V$, $I_{LOAD} = 1mA$, $V_{OUT} = -1.5V$	-30	0.5	30	nA/V
	ΔV_{OS}	$V_{IN} = -2.3V$ to $-20V$, $I_{LOAD} = 1mA$, $V_{OUT} = -1.5V$ ⁸	-6	0.1	6	$\mu V/V$
Load Regulation	ΔI_{SET}	$I_{LOAD} = 1mA$ to $500mA$, $V_{IN} = -2.3V$, $V_{OUT} = -1.5V$		0.1		nA
	ΔV_{OS}	$I_{LOAD} = 1mA$ to $500mA$, $V_{IN} = -2.3V$, $V_{OUT} = -1.5V$ ⁸		0.03	0.5	mV
Change in I_{SET} with V_{SET}		$V_{SET} = -1.5V$ to $-19.5V$, $V_{IN} = -20V$, $I_{LOAD} = 1mA$		100	850	nA
Change in V_{OS} with V_{SET}		$V_{SET} = -1.5V$ to $-19.5V$, $V_{IN} = -20V$, $I_{LOAD} = 1mA$ ⁸		0.02	0.5	mV
Change in I_{SET} with V_{SET}		$V_{SET} = 0V$ to $-1.5V$, $V_{IN} = -20V$, $I_{LOAD} = 1mA$		150	800	nA
Change in V_{OS} with V_{SET}		$V_{SET} = 0V$ to $-1.5V$, $V_{IN} = -20V$, $I_{LOAD} = 1mA$ ⁸		0.15	2	mV

(All minimum and maximum specifications are at T_J (Junction Temperature) = 25°C. Total ionizing dose (TID) testing is characterized to 30krads.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dropout Voltage ⁹		$I_{LOAD} = 1mA, 50mA$		185	380	mV
		$I_{LOAD} = 100mA$		185	380	mV
		$I_{LOAD} = 500mA$		235	410	mV
GND Pin Current $V_{IN} = V_{OUT(NOMINAL)}$ ¹⁰		$I_{LOAD} = 10\mu A$		2.35		mA
		$I_{LOAD} = 1mA$		2.4	4	mA
		$I_{LOAD} = 50mA$		3.1	5.5	mA
		$I_{LOAD} = 100mA$		3.8	6.5	mA
		$I_{LOAD} = 500mA$		12	23	mA
EN/UV Pin Threshold		Positive EN/UV Trip Point Rising (Turn-on), $V_{IN} = -2.3V$	1.20	1.26	3.00	V
		Negative EN/UV Trip Point Rising (Turn-on), $V_{IN} = -2.3V$	-2.50	-1.26	-1.20	V
EN/UV Pin Hysteresis		Positive EN/UV Trip Point Hysteresis, $V_{IN} = -2.3V$		200		mV
		Negative EN/UV Trip Point Hysteresis, $V_{IN} = -2.3V$		215		mV
EN/UV Pin Current		$V_{EN/UV} = 0V, V_{IN} = -20V$	-1		1	μA
		$V_{EN/UV} = -1.5V, V_{IN} = -20V$		-0.5		μA
		$V_{EN/UV} = -20V, V_{IN} = -20V$	-35	-18.5		μA
		$V_{EN/UV} = 1.5V, V_{IN} = -20V$		8		μA
		$V_{EN/UV} = 20V, V_{IN} = 0V$		25	45	μA
Quiescent Current in Shutdown ($V_{EN/UV} = 0V$)		$V_{IN} = -6V, V_{PG} = \text{Open}$		3	8	μA
					10	μA
Internal Current Limit ¹³		$V_{IN} = -2.3V, V_{OUT} = 0V$	550	750		mA
		$V_{IN} = -12V, V_{OUT} = 0V$		425		mA
		$V_{IN} = -20V, V_{OUT} = 0V$	40	85	160	mA
Programmable Current Limit		Programming Scale Factor: $-20V < V_{IN} < -2.3V$ ¹²		3.75		$A \times k\Omega$
		$V_{IN} = -2.3V, V_{OUT} = 0V, R_{ILIM} = 7.5k\Omega$	450	500	560	mA
		$V_{IN} = -2.3V, V_{OUT} = 0V, R_{ILIM} = 37.5k\Omega$	90	105	120	mA
PGFB Trip Point		PGFB Trip Point Rising	270	300	312	mV
PGFB Hysteresis		PGFB Trip Point Hysteresis		7		mV

(All minimum and maximum specifications are at T_J (Junction Temperature) = 25°C. Total ionizing dose (TID) testing is characterized to 30krads.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGFB Pin Current		$V_{IN} = -2.3V, V_{PGFB} = -300mV$		30	100	nA
PG Output Low Voltage		$I_{PG} = 100\mu A$		17	50	mV
PG Leakage Current		$V_{PG} = 20V$			1	μA
VIOC Amplifier Gain		$-20V \leq V_{IN} \leq -2.3V, V_{OUT} \leq -1.5V$		1		V/V
VIOC Maximum Output Voltage Swing		$V_{IN} - V_{OUT} = -2V, V_{OUT} \leq -1.5V$		-1.35	-1.2	V
VIOC Sink Current		$V_{IN} - V_{OUT} = -2V, V_{VIOC} = -1V$	100			μA
VIOC Voltage for Low Output Voltage ¹⁴		$V_{IN} = -2.3V, V_{OUT} > -1.5V$		-0.8		V
Minimum Load Current ¹⁵		$V_{OUT} > -1.5V$			10	μA
Start-Up Time		$R_{SET} = 49.9k\Omega, V_{OUT(NOM)} = -5V,$ $I_{LOAD} = 500mA, C_{SET} = 0.47\mu F,$ $V_{IN} = -6V, V_{PGFB} = -6V$		55		ms
		$R_{SET} = 49.9k\Omega, V_{OUT(NOM)} = -5V,$ $I_{LOAD} = 500mA, C_{SET} = 4.7\mu F,$ $V_{IN} = -6V, V_{PGFB} = -6V$		550		ms
		$R_{SET} = 49.9k\Omega, V_{OUT(NOM)} = -5V,$ $I_{LOAD} = 500mA, C_{SET} = 4.7\mu F,$ $V_{IN} = -6V, R_{PG1} = 50k\Omega, R_{PG2} = 700k\Omega$ (with fast start-up to 90% of V_{OUT})		10		ms

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise specified.

Table 3. Absolute Maximum Ratings

PARAMETER	RATING
IN Pin Voltage with respect to GND Pin	-22V, 0.3V
EN/UV Pin Voltage with respect to IN Pin ¹	-0.3V, 30V
EN/UV Pin Voltage with respect to GND Pin	$\pm 22\text{V}$
PG Pin Voltage with respect to IN Pin ¹	-0.3V, 30V
PG Pin Voltage with respect to GND Pin	-0.3V, 22V
PGFB Pin Voltage with respect to IN Pin ¹	-0.3V, 30V
PGFB Pin Voltage with respect to GND Pin	$\pm 22\text{V}$
I_{LIM} Pin Voltage with respect to IN Pin ¹	-0.3V, 22V
VIOC Pin Voltage with respect to IN Pin ¹	-0.3V, 22V
VIOC Pin Voltage with respect to GND Pin	-2V, 0.3V
SET Pin Voltage with respect to IN Pin ¹	-0.3V, 22V
SET Pin Voltage with respect to GND Pin	$\pm 22\text{V}$
SET Pin Current ³	$\pm 10\text{mA}$
OUTS Pin Voltage with respect to IN Pin ¹	-0.3V, 22V
OUTS Pin Voltage with respect to GND Pin	$\pm 22\text{V}$
OUTS Pin Current ³	$\pm 10\text{mA}$
SET-to-OUTS Differential ⁴	$\pm 22\text{V}$
OUT Pin Voltage with respect to IN Pin ¹	-0.3V, 22V
OUT Pin Voltage with respect to GND Pin	$\pm 22\text{V}$
OUT-to-OUTS Differential ⁵	$\pm 22\text{V}$
Output Short-Circuit Duration	Indefinite
Operating Junction Temperature Range ¹	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Outgas Testing

The criteria for the acceptance and rejection of materials must be determined by the user based on the specific component and system requirements. Historically, a total mass loss (TML) of 1.00% and collected volatile condensable material (CVCM) of 0.10% have been used as screening levels for rejecting spacecraft materials.

Table 4. Outgas Testing

SPECIFICATIONS (TESTED AS PER ASTM E595-15)	VALUE	UNITS
Total mass loss	0.04	%
Collected volatile condensable material	< 0.01	%
Water vapor recovered	0.02	%

Radiation Features

Table 5. Radiation Features

SPECIFICATIONS	VALUE	UNITS
Maximum total dose available (Dose rate = 50rad(Si)/sec to 300rad(Si)/sec) ¹	30	krad(Si)
No SEL occurs at effective linear energy transfer (LET) ²	79.9	MeV × cm ² /mg

¹Guaranteed by device and process characterization. A radiation report is available on the RHP51002 product web page.

²Limits are characterized at initial qualification and after any design or process changes specified by the customer through the purchase order or contract. If the input voltage exceeds 16V, implement mitigation to prevent SEL. A radiation report is available on the RHP51002 product web page. Contact Analog Devices for further data beyond the report published on the web page.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

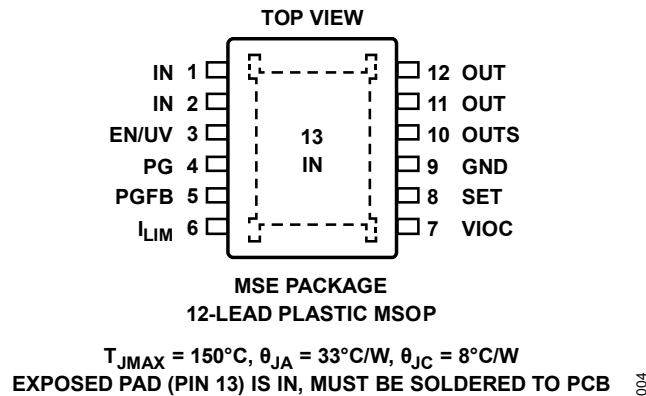


Figure 3. Pin Configuration

Pin Descriptions

Table 6. Pin Descriptions

PIN	NAME	DESCRIPTION
Pin 1, Pin 2, Exposed Pad Pin 13	IN	Input. These pins supply power to the regulator. The RHP51002 requires a bypass capacitor at the IN pin. In general, a battery's output impedance rises with frequency, so include a bypass capacitor in battery-powered applications. While a 10μF input bypass capacitor generally suffices, applications with large load transients may require higher input capacitance to prevent input supply droop. For proper use of the input capacitor and an explanation of its influence on circuit performance, see the Applications Information section.
Pin 3	EN/UV	Enable/UVLO. Pulling the device's EN/UV pin low places the part in shutdown. Quiescent current in shutdown mode drops to 3μA, and the output voltage turns off. Alternatively, the EN/UV pin can set an input supply undervoltage lockout (UVLO) threshold using a resistor divider between IN, EN/UV, and GND. The EN/UV pin is bidirectional and can be switched with either a positive or negative voltage. The device typically turns on when the EN/UV voltage exceeds 1.26V above ground (with a 200mV hysteresis on the falling edge) or 1.26V below ground (with a 215mV hysteresis). If unused, tie EN/UV to IN. Do not float the EN/UV pin.
Pin 4	PG	Power Good. PG is an open-collector flag that indicates output voltage regulation. PG pulls low when PGFB is between 0V and -300mV. If the power good functionality is not needed, float the PG pin. The PG flag status is valid even if the device is in shutdown, with the PG pin being pulled low.

PIN	NAME	DESCRIPTION
Pin 5	PGFB	Power Good Feedback. The PG pin pulls high if PGFB is below -300mV on its rising edge, with 7mV hysteresis on its falling edge. Connecting an external resistor divider between OUT, PGFB, and GND sets the programmable power good threshold with the following transfer function: $-0.3\text{V} \times (1 + R_{\text{PG1}}/R_{\text{PG2}}) - \text{IPGFB} \times \text{RPG1}$. PGFB also activates the fast-start-up circuitry; see the Applications Information section for more details. If power good and fast start-up functionality are not needed, tie PGFB to IN.
Pin 6	ILIM	Current Limit Programming Pin. Connecting a resistor between ILIM and GND programs the current limit. For best accuracy, Kelvin connect this resistor directly to the RHP51002's GND pin. The programming scale factor is nominally $3.75\text{A} \times \text{k}\Omega$. If the programmable current limit functionality is not needed, tie ILIM to GND. Do not float the I_{LIM} pin.
Pin 7	VIOC	Voltage for Input-to-Output Control. The device incorporates a tracking feature to control a circuit that supplies power to the device, maintaining the differential voltage across the device. This function maximizes efficiency and PSRR performance while minimizing power dissipation. See the Applications Information section for more details. If unused, float the VIOC pin.
Pin 8	SET	Set. This pin is the inverting input of the error amplifier and the device's regulation setpoint. The SET pin sinks a precision $100\mu\text{A}$ current that flows through an external resistor connected between SET and GND. The RHP51002's output voltage is determined by $V_{\text{SET}} = I_{\text{SET}} \times R_{\text{SET}}$. The output voltage range is from 0V to -19.5V . Adding a capacitor from SET to GND improves noise, PSRR, and transient response, but increases start-up time unless the fast-start-up capability is used via the PGFB pin. For optimum load regulation, Kelvin connect the ground side of the SET pin directly to the load.
Pin 9	GND	Ground.
Pin 10	OUTS	Output Sense. This pin is the noninverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connect OUTS directly to the output capacitor and the load. Also, tie the GND connections of the output capacitor and the SET pin capacitor directly together. Exercise care when placing input capacitors relative to output capacitors to avoid potential PSRR degradation from magnetic coupling; see the Applications Information section for more information on capacitor placement and board layout. A parasitic substrate diode exists between OUTS and IN pins of the device; do not drive OUTS more than 0.3V below IN during normal operation or a fault condition.

PIN	NAME	DESCRIPTION
Pins 11, 12	OUT	Output. This pin supplies power to the load. For stability, use a minimum of 10 μ F output capacitor with an ESR below 30m Ω and an ESL below 1.5nH. Large-load transients require larger output capacitance to limit peak-voltage transients. See the Applications Information section for more information on output capacitance. A parasitic substrate diode exists between OUT and IN pins of the device; do not drive OUT more than 0.3V below IN during normal operation or during a fault condition.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

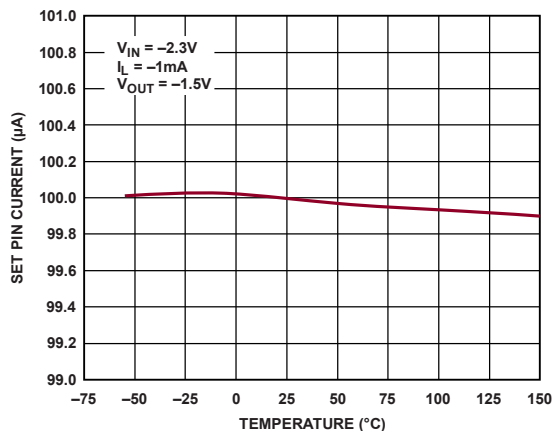


Figure 4. SET Pin Current

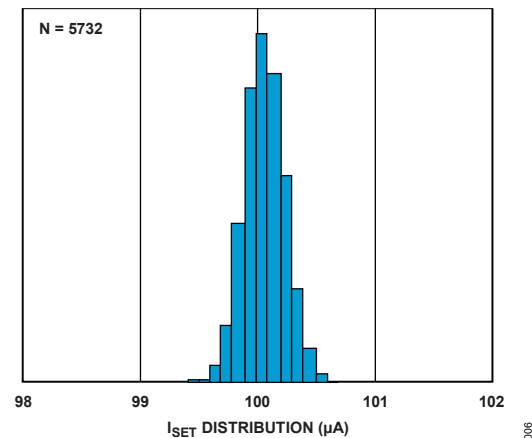


Figure 5. SET Pin Current

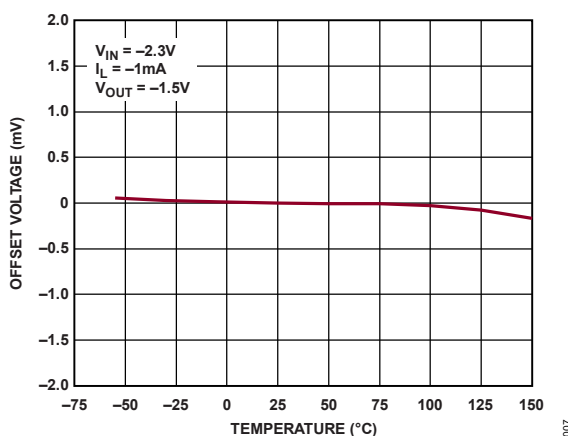


Figure 6. Offset Voltage ($V_{OUT} - V_{SET}$)

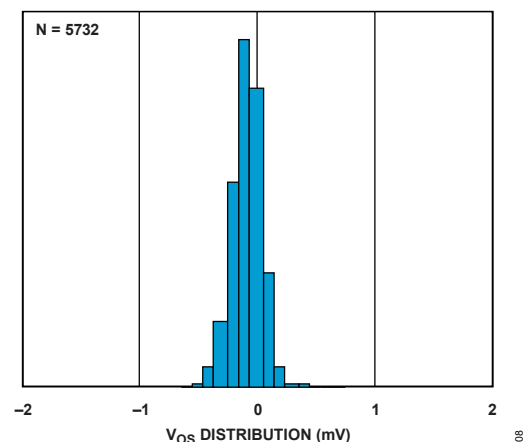


Figure 7. Offset Voltage

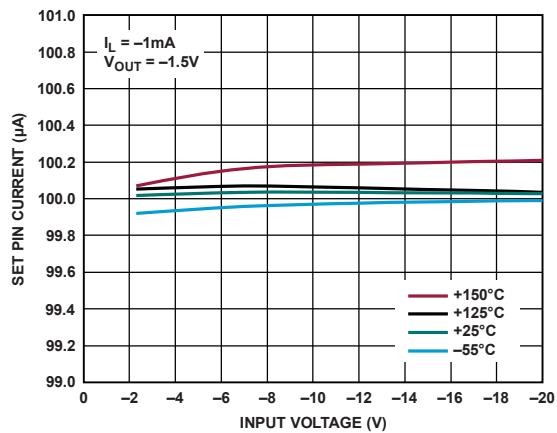


Figure 8. SET Pin Current

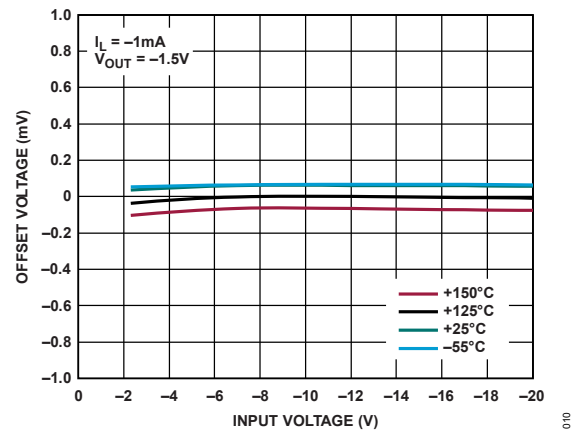
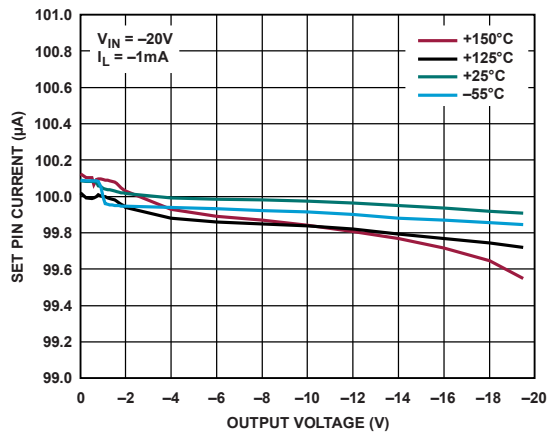
Figure 9. Offset Voltage ($V_{OUT} - V_{SET}$)

Figure 10. SET Pin Current

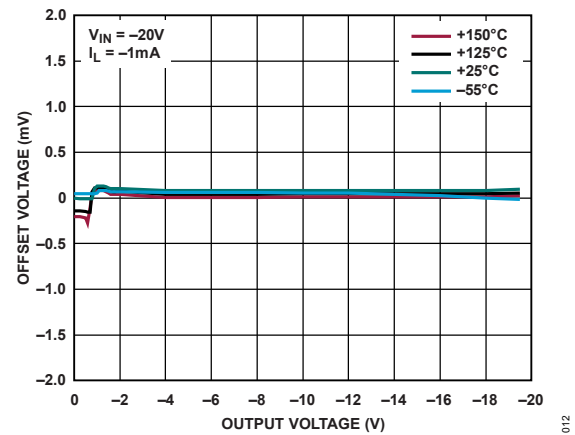
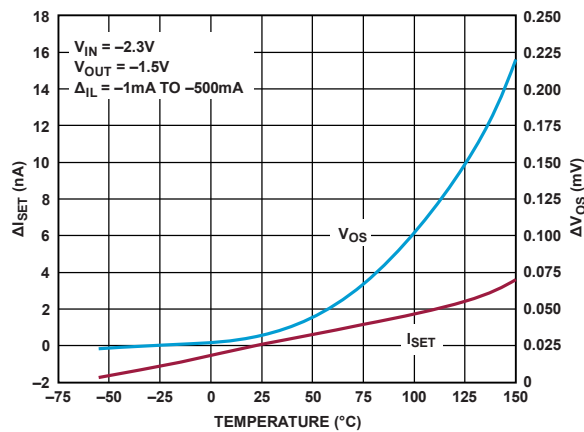
Figure 11. Offset Voltage ($V_{OUT} - V_{SET}$)

Figure 12. Load Regulation

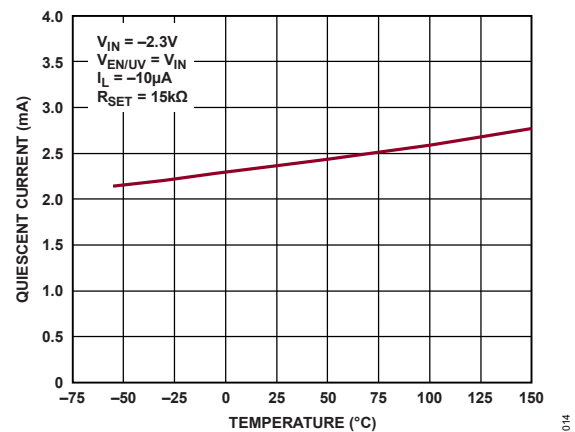


Figure 13. Quiescent Current

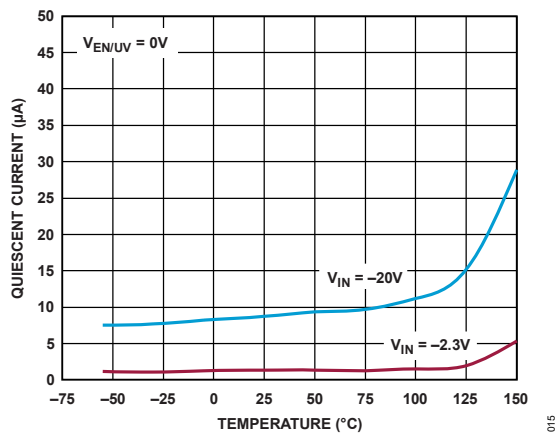


Figure 14. Quiescent Current

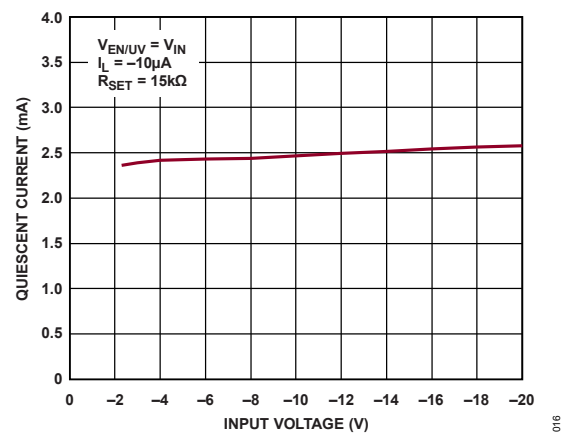


Figure 15. Quiescent Current

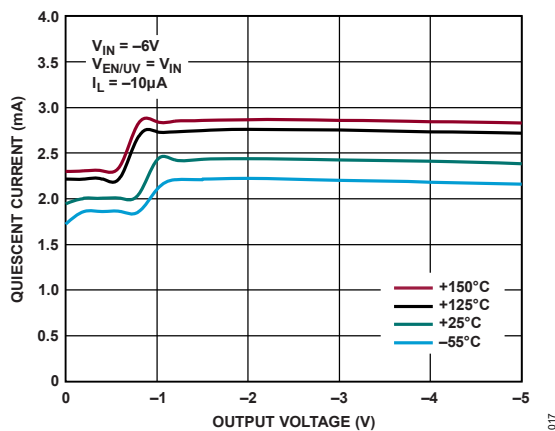


Figure 16. Quiescent Current

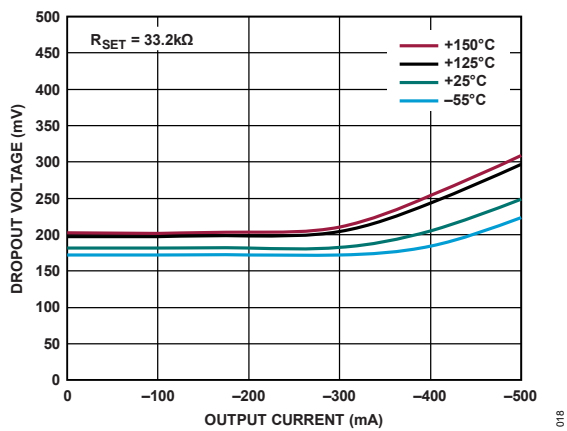


Figure 17. Typical Dropout Voltage

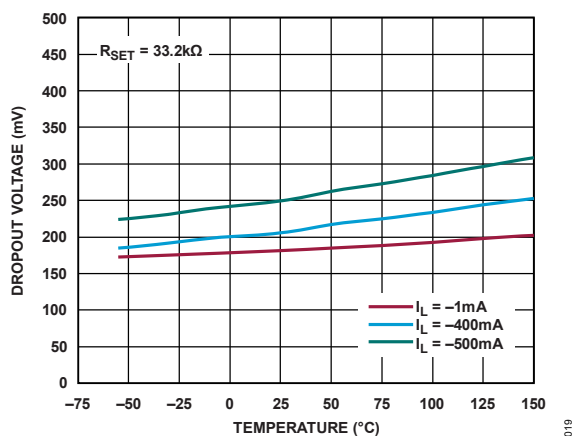


Figure 18. Dropout Voltage

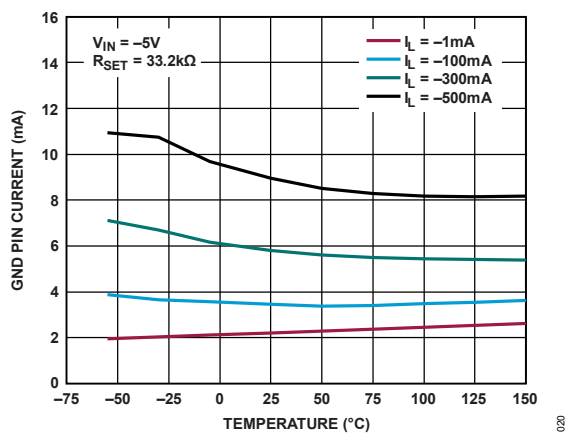


Figure 19. GND Pin Current

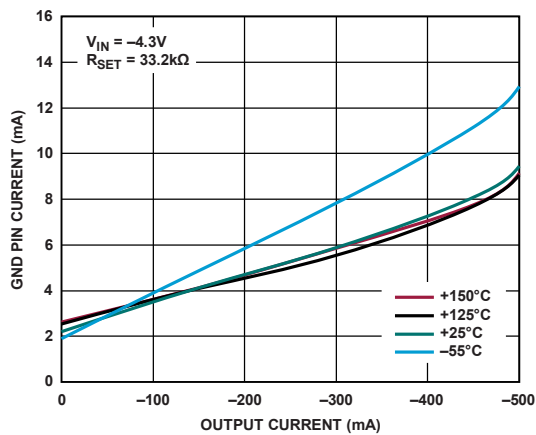


Figure 20. GND Pin Current

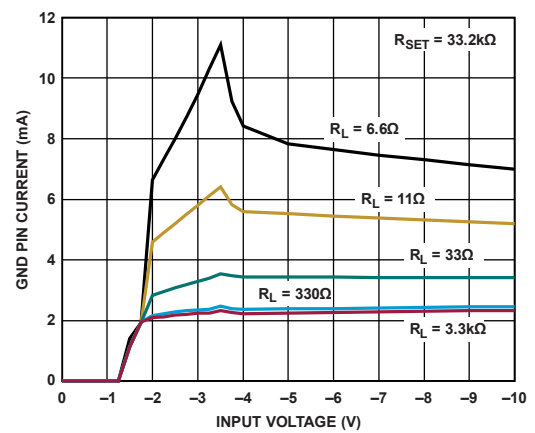


Figure 21. GND Pin Current

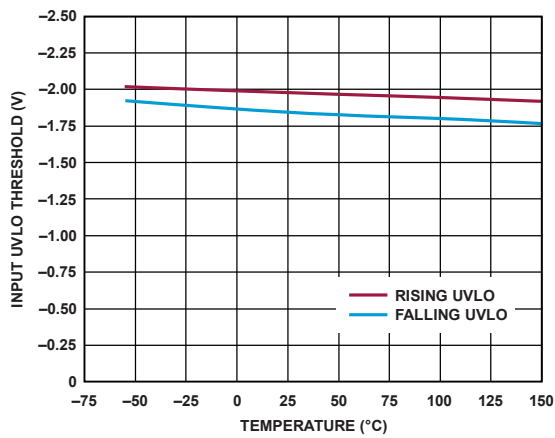


Figure 22. Minimum Input Voltage

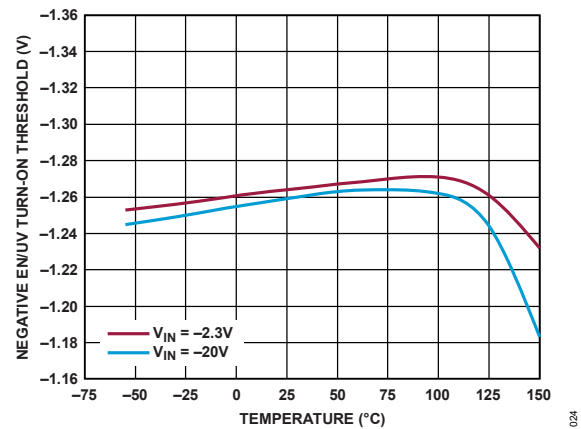


Figure 23. Negative EN/UV Turn-On Threshold

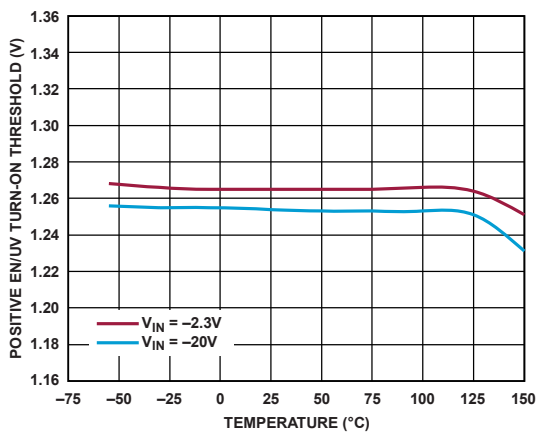


Figure 24. Positive EN/UV Turn-On Threshold

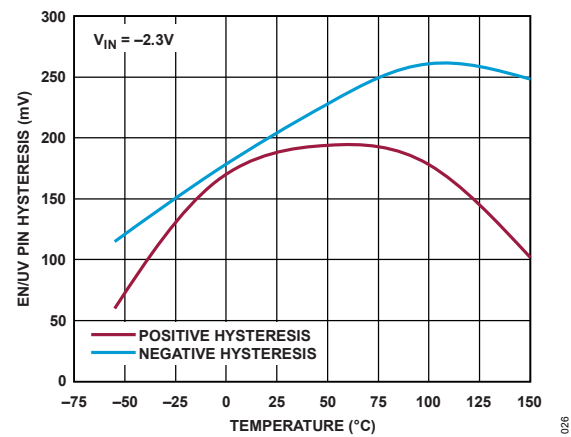


Figure 25. EN/UV Pin Hysteresis

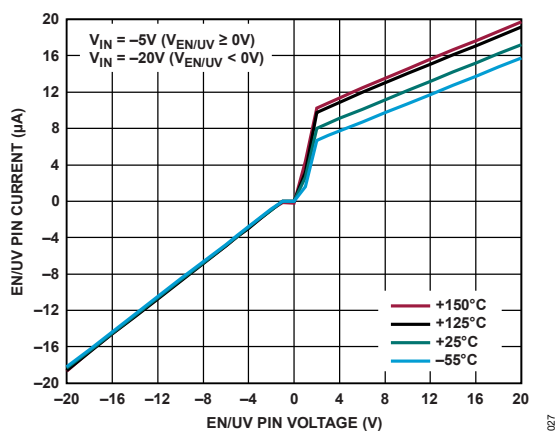


Figure 26. EN/UV Pin Current

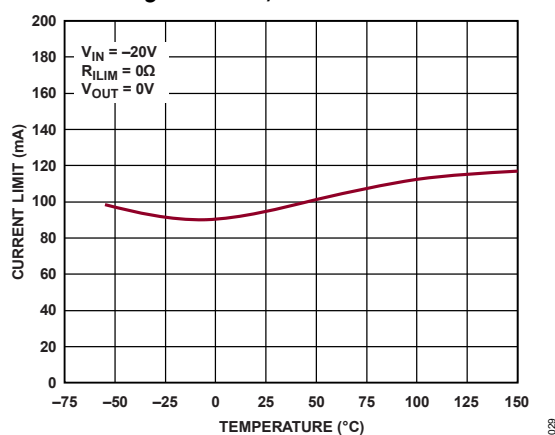


Figure 28. Internal Current Limit

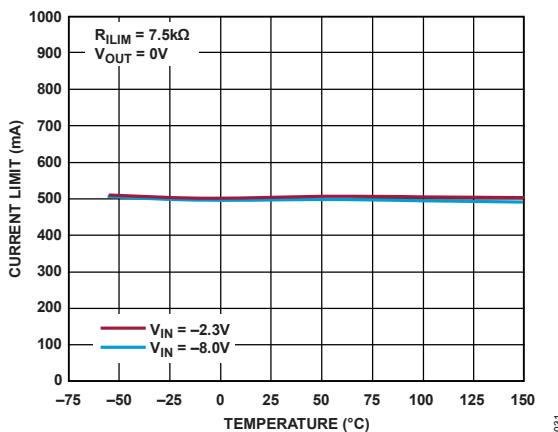


Figure 30. Programmable Current Limit

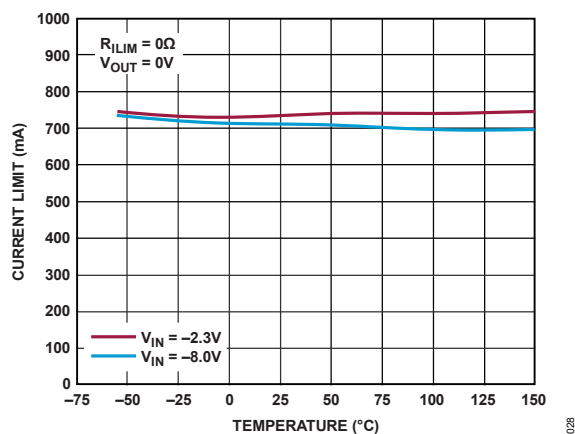


Figure 27. Internal Current Limit

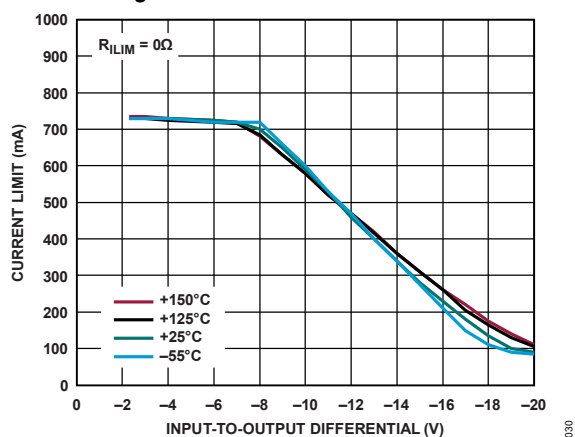


Figure 29. Internal Current Limit

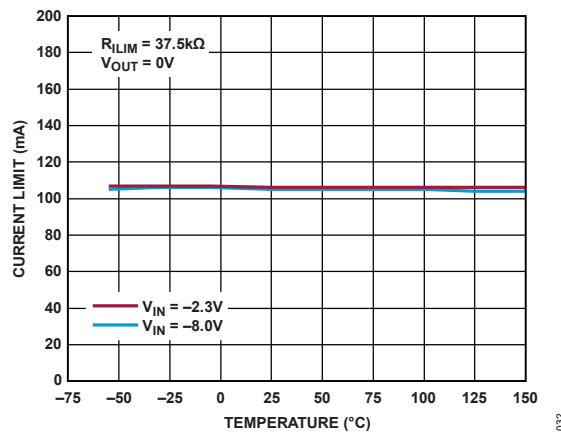


Figure 31. Programmable Current Limit

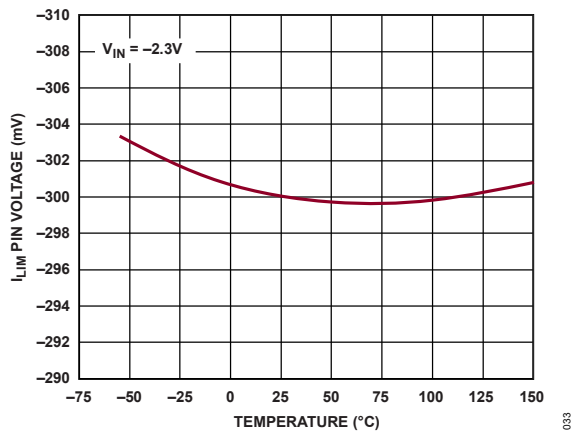
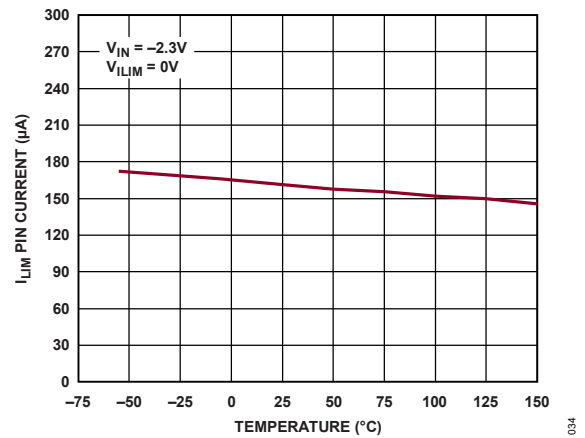
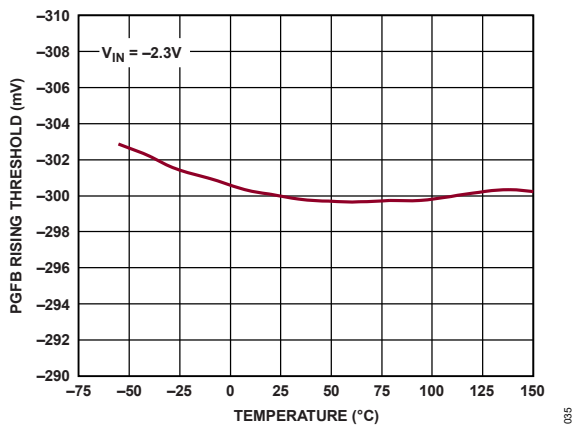
Figure 32. I_{LIM} Pin VoltageFigure 33. I_{LIM} Pin Current

Figure 34. PGFB Rising Threshold

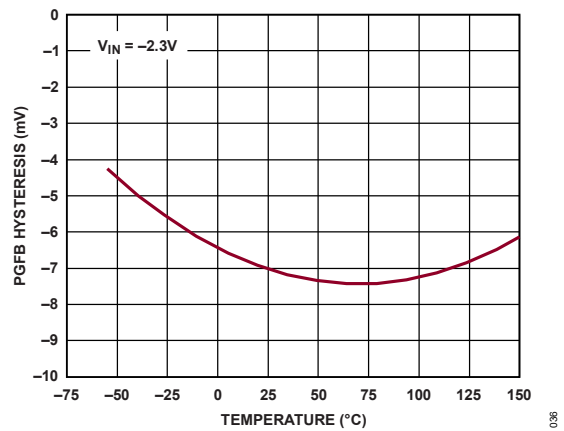


Figure 35. PGFB Hysteresis

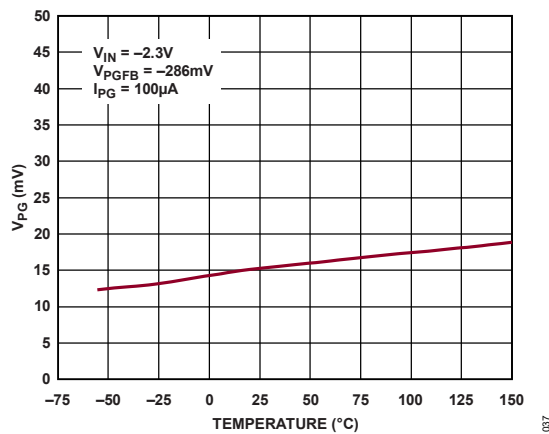


Figure 36. PG Output Low Voltage

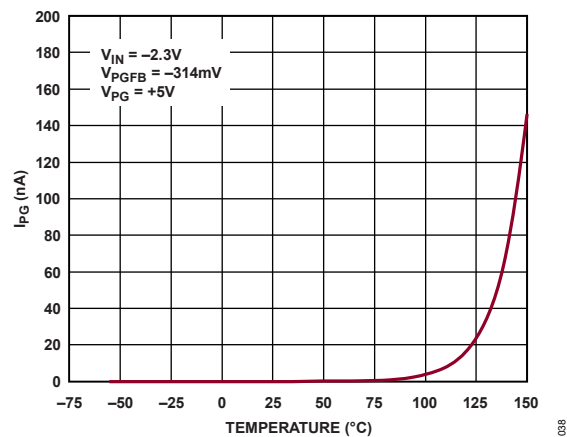


Figure 37. PG Pin Leakage Current

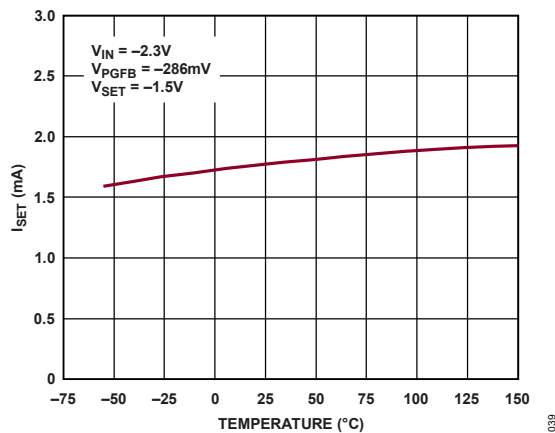
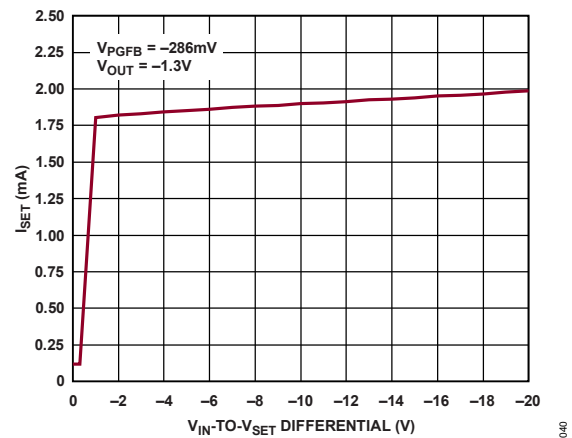
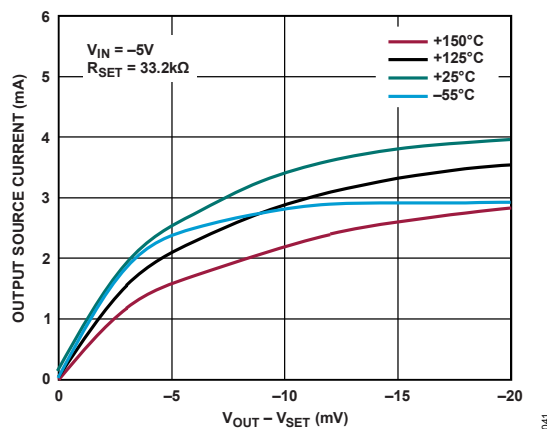
Figure 38. I_{SET} During Start-Up with Fast Start-Up EnabledFigure 39. I_{SET} During Start-Up with Fast Start-Up Enabled

Figure 40. Output Overshoot Recovery Source Current

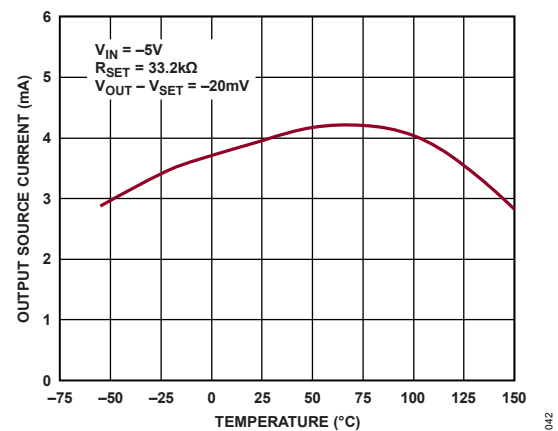
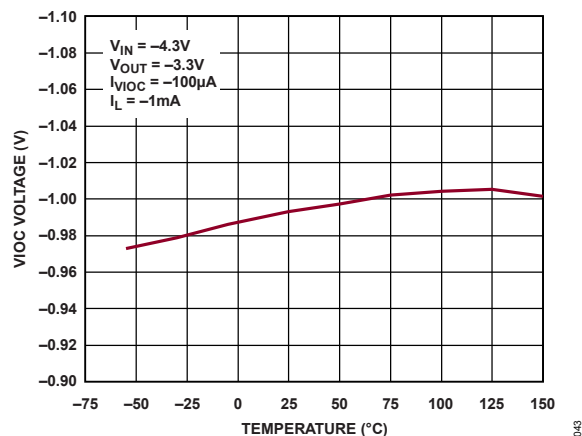
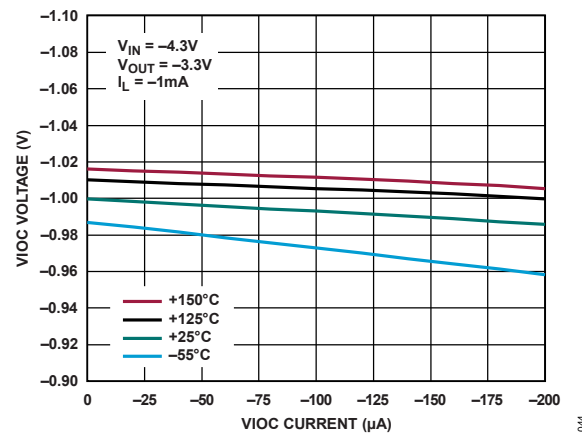


Figure 41. Output Overshoot Recovery Source Current

Figure 42. V_{IOC} VoltageFigure 43. V_{IOC} Voltage

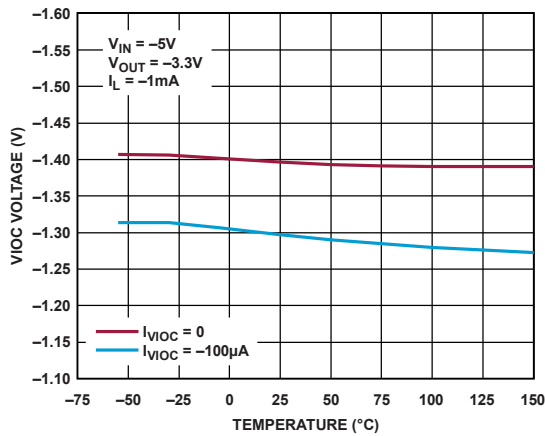


Figure 44. Maximum VIOC Voltage

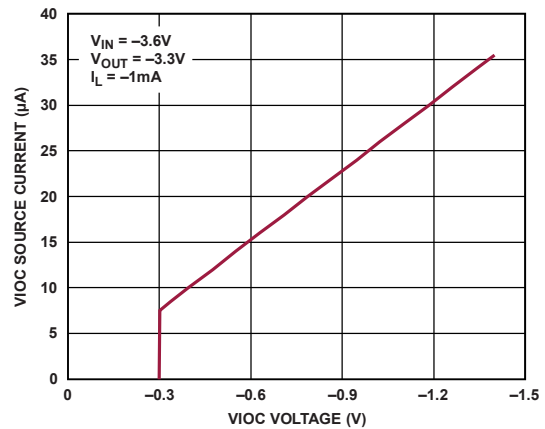


Figure 45. VIOC Source Current

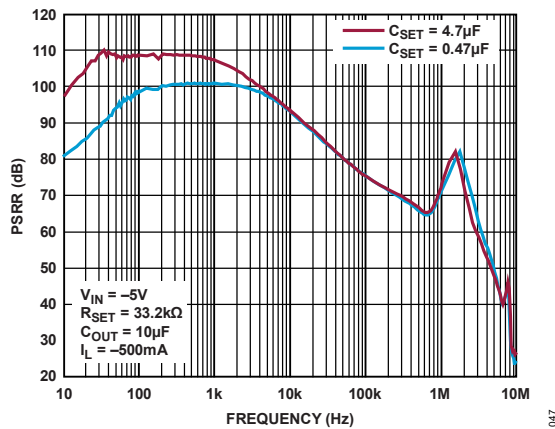


Figure 46. Power Supply Ripple Rejection

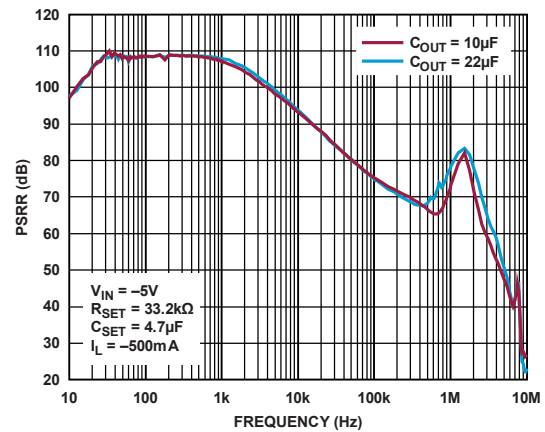


Figure 47. Power Supply Ripple Rejection

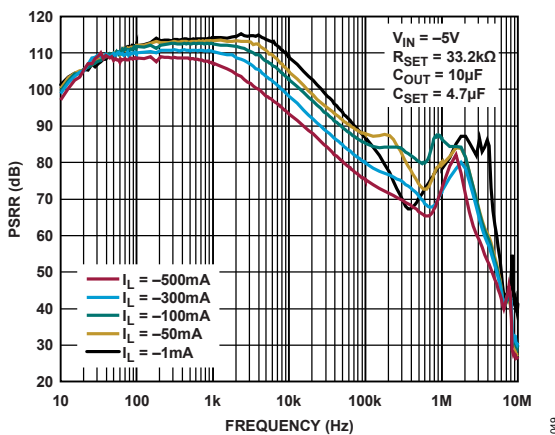


Figure 48. Power Supply Ripple Rejection

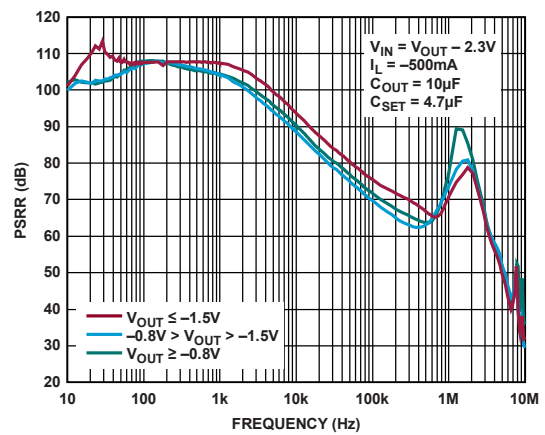


Figure 49. Power Supply Ripple Rejection as a Function of Error Amplifier Input Pair

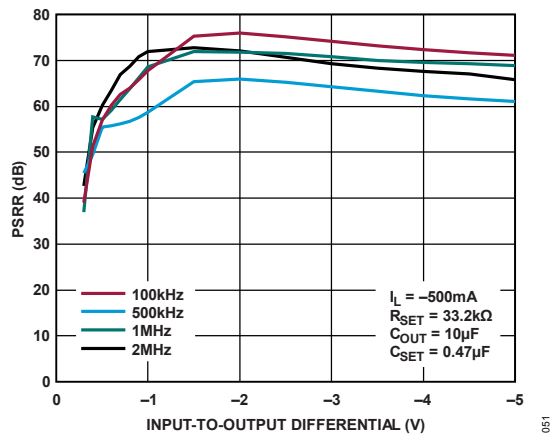


Figure 50. Power Supply Ripple Rejection

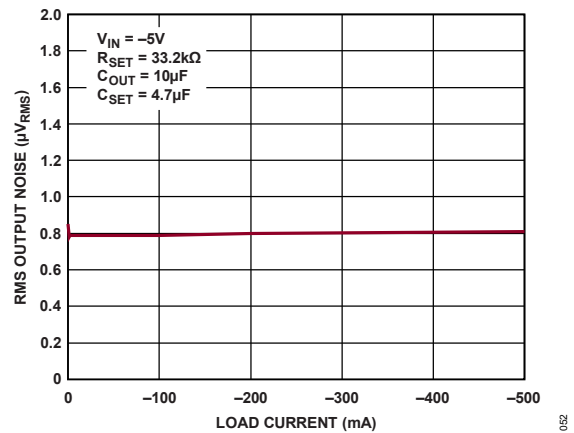


Figure 51. Integrated RMS Output Noise (10Hz to 100kHz)

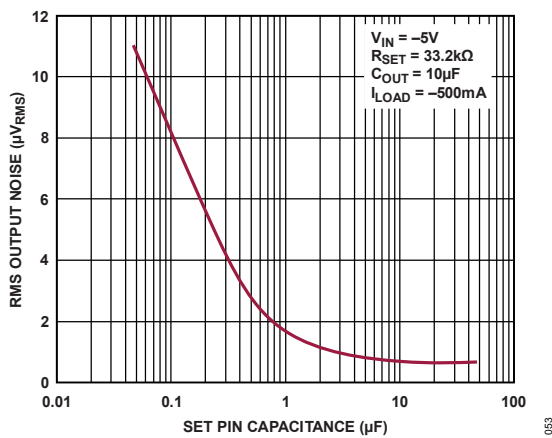


Figure 52. Integrated RMS Output Noise (10Hz to 100kHz)

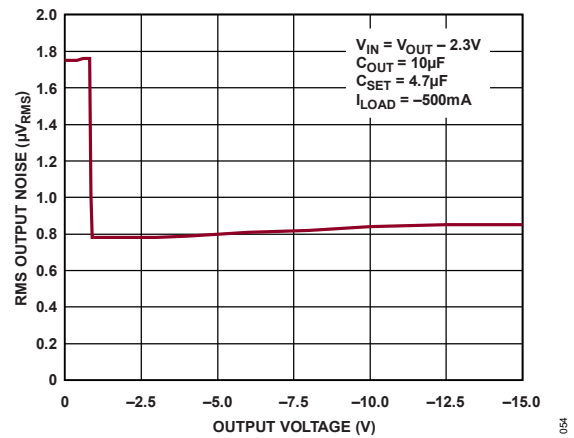


Figure 53. Integrated RMS Output Noise (10Hz to 100kHz)

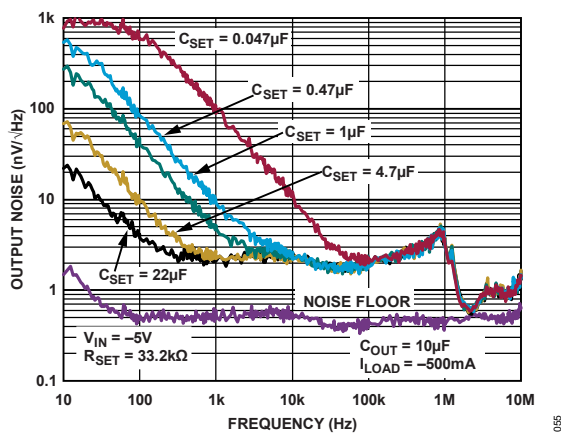


Figure 54. Noise Spectral Density

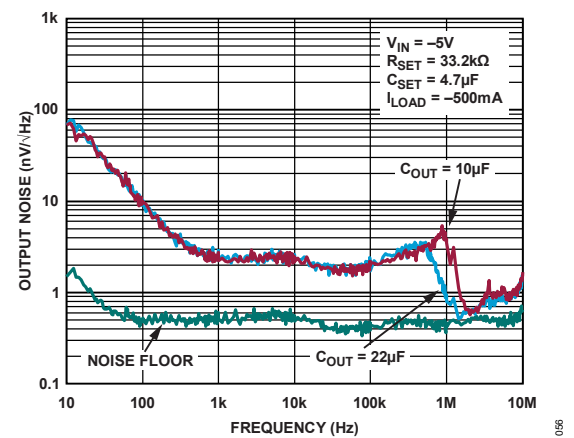


Figure 55. Noise Spectral Density

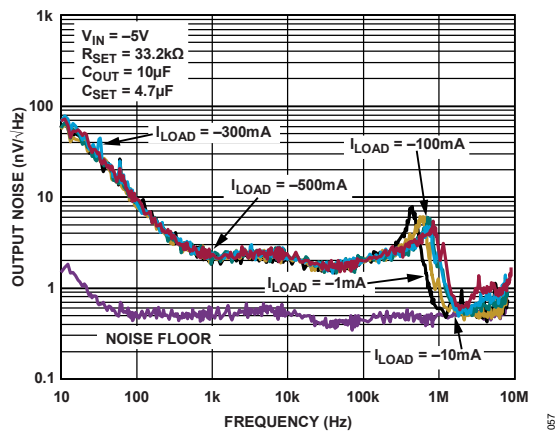


Figure 56. Noise Spectral Density

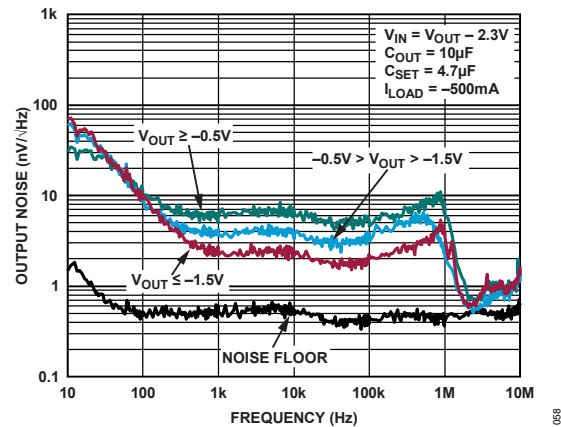


Figure 57. Noise Spectral Density as a Function of Error Amplifier Input Pair

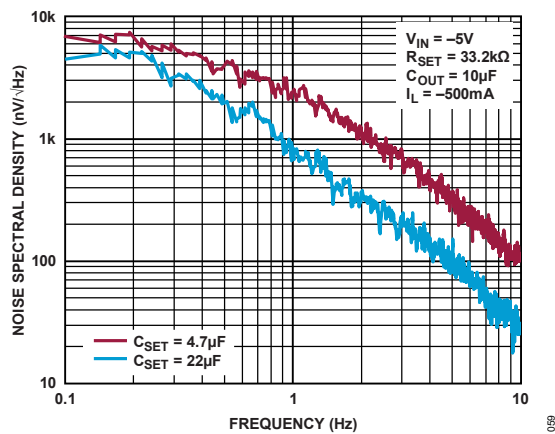


Figure 58. Noise Spectral Density (0.1Hz to 10Hz)

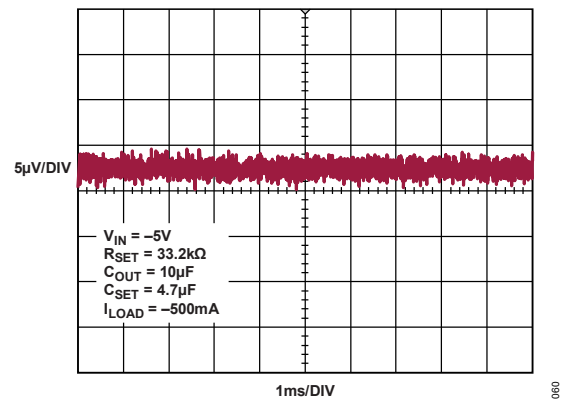


Figure 59. Output Noise (10Hz to 100kHz)

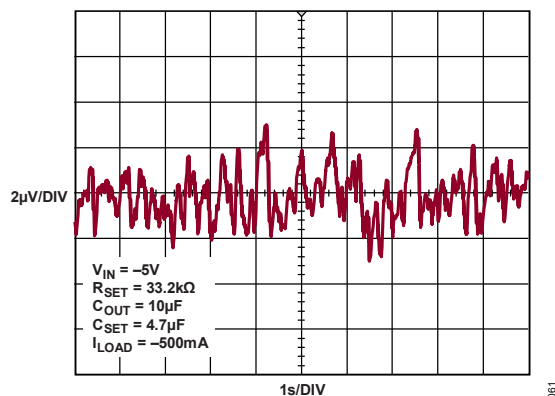


Figure 60. Output Voltage Noise (0.1Hz to 10Hz)

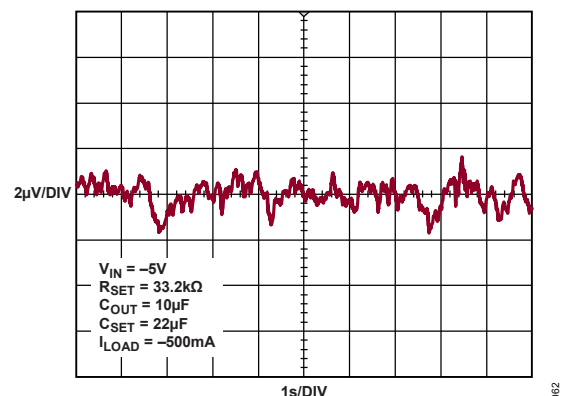


Figure 61. Output Voltage Noise (0.1Hz to 10Hz)

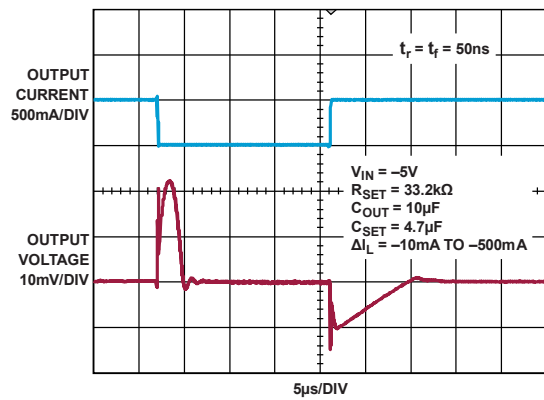


Figure 62. Load Transient Response

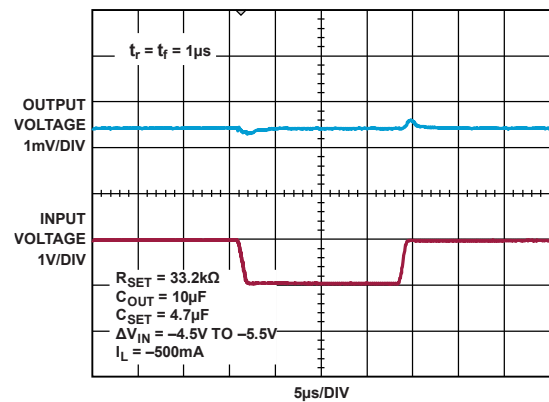


Figure 63. Line Transient Response

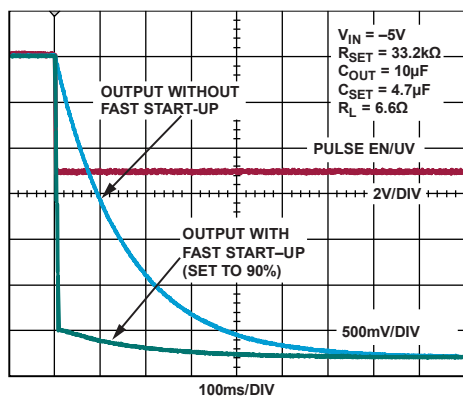
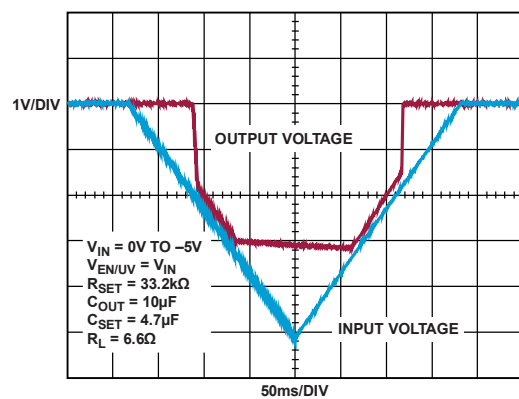
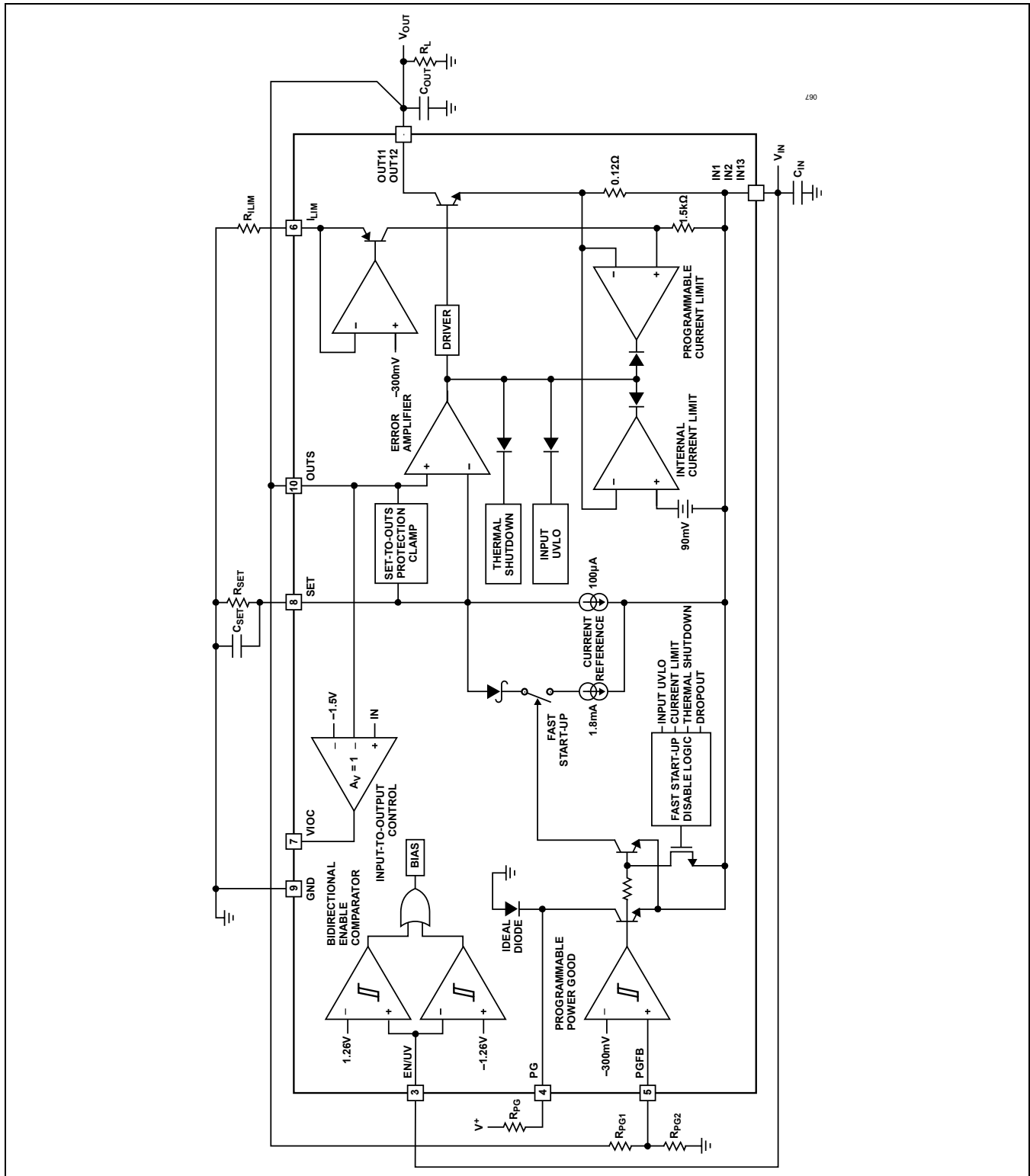
Figure 64. Start-Up Time with and without Fast Start-Up Circuitry for Large C_{SET} 

Figure 65. Input Supply Ramp-Up and Ramp-Down

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The RHP51002 is a high-performance, low-dropout negative linear regulator featuring Analog Devices' ultralow-noise ($2.2\text{nV}/\sqrt{\text{Hz}}$ at 10kHz) and ultrahigh PSRR (74dB at 1MHz) architecture for powering noise-sensitive applications. Designed as a precision current reference followed by a high-performance rail-to-rail voltage buffer, the device can be easily paralleled to further reduce noise, increase output current, and spread heat across the PCB. The device also features a programmable current limit, fast start-up capability, and a programmable power good.

The device is easy to use and incorporates all of the protection features expected in high-performance regulators. Included are short-circuit protection, safe operating area protection, and thermal shutdown with hysteresis.

Output Voltage

The RHP51002 incorporates a precision $100\mu\text{A}$ current reference that flows into the SET pin, and also connects to the error amplifier's inverting input. [Figure 66](#) illustrates that connecting a resistor from SET to ground generates a reference voltage for the error amplifier. This reference voltage is simply the product of the SET pin current and the SET pin resistor. The error amplifier's unity-gain configuration produces a low-impedance version of this voltage at its non-inverting input (the OUTS pin), which is externally tied to the OUT pin. The device's output voltage is determined by $V_{\text{SET}} = I_{\text{SET}} \times R_{\text{SET}}$.

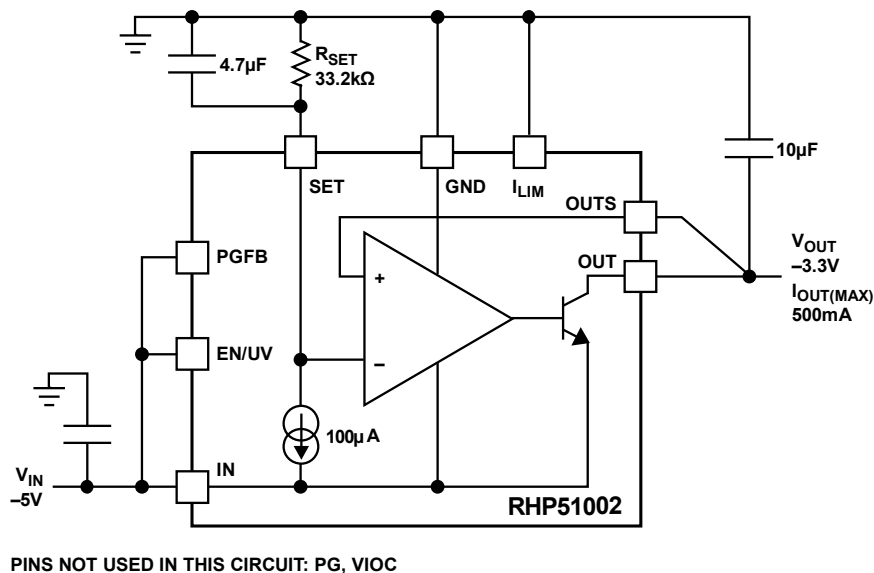


Figure 66. Basic Adjustable Regulator

The RHP51002's rail-to-rail error amplifier and current-reference architecture allow for a wide output-voltage range from 0V (using a 0Ω resistor) to V_{IN} minus dropout. A negative-positive-negative (NPN)-based input pair is active for a 0V to -0.8V output, and a PNP-based input pair is active for output voltages beyond -1.5V , with a smooth transition between the two input pairs from -0.8V to -1.5V output. The PNP-based input pair offers the best overall performance; refer to the Electrical Characteristics table for details on offset voltage, SET pin current, output noise, and PSRR variation depending on the output voltage and the corresponding active input pair(s).

[Table 7](#) lists common output voltages and their corresponding 1% R_{SET} resistors.

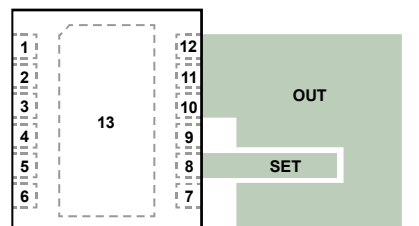
Table 7. 1% Resistor for Common Output Voltages

V_{OUT} (V)	R_{SET} (k Ω)
-2.5	24.9
-3.3	33.2
-5	49.9
-12	121
-15	150

The benefit of using a current reference, rather than a voltage reference as in conventional regulators, is that the regulator always operates in a unity-gain configuration, independent of the programmed output voltage. This allows the RHP51002 to have loop gain, frequency response, and bandwidth that are independent of the output voltage. As a result, noise, PSRR, and transient performance do not change with output voltage. Because the error amplifier gain is not required to amplify the SET pin voltage to a higher output voltage, output load regulation is more tightly specified in the hundreds-of-microvolts range rather than as a fixed percentage of the output voltage.

Because the zero TC current reference is highly accurate, the SET pin resistor can become the limiting factor in achieving high accuracy. Hence, it should be a precision resistor. Additionally, any leakage paths to or from the SET pin create output-voltage errors. If necessary, use high-quality insulation (for example, Teflon, Kel-F); also, cleaning of all insulating surfaces to remove fluxes and other residues may be required. High-humidity environments may require a surface coating at the SET pin to provide a moisture barrier.

Minimize board leakage by encircling the SET pin with a guard ring operated at a similar potential—ideally tied to the OUT pin. Guarding both sides of the circuit board is recommended. Bulk leakage reduction depends on the guard-ring width. A leakage of 100nA into or out of the SET pin creates a 0.1% error in the reference voltage. Leakages of this magnitude, coupled with other leakage sources, can cause significant errors in the output voltage, especially over a wide operating temperature range. [Figure 67](#) illustrates a typical guard ring layout technique.

**Figure 67. Guard Ring Layout**

Because the SET pin is a high-impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This is most noticeable when operating with a minimum output capacitor under heavy load. Bypassing the SET pin with a small capacitor to ground resolves this issue—10nF is sufficient.

For applications requiring higher accuracy or adjustable output voltage, the SET pin may be driven by an external voltage source capable of sourcing 100 μ A. Connecting a precision voltage reference to the SET pin eliminates any errors present in the output voltage due to the reference current and SET pin resistor tolerances.

Output Sensing and Stability

The RHP51002's OUTS pin provides a Kelvin sense connection to the output. The GND side of the SET pin resistor provides a Kelvin-sense connection to the load's GND.

Additionally, for ultrahigh PSRR, the RHP51002 bandwidth is quite high (~1MHz), making it very close to the self-resonance frequency of a typical 10 μ F (1206 case size) ceramic output capacitor (~1.6MHz). Avoid adding extra impedance (equivalent series resistance (ESR) and equivalent series inductance (ESL)) outside the feedback loop. Minimize the effects of PCB trace and solder inductance by connecting the OUTS pin directly to C_{OUT} and the GND side of C_{SET} directly to the GND side of C_{OUT}, as well as keeping the GND sides of C_{IN} and C_{OUT} reasonably close, as shown in [Figure 68](#). For details on a recommended layout that satisfies these requirements, refer to the RHP51002 demo board manual. While the device is robust and will not oscillate if the recommended layout is not followed, depending on the actual layout, phase/gain margin, noise, and PSRR performance may degrade.

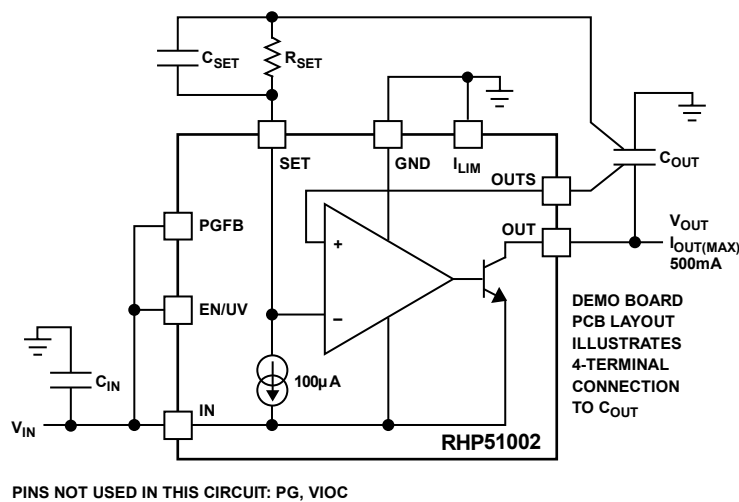


Figure 68. C_{OUT} and C_{SET} Connections for Best Performance

Stability and Output Capacitance

The RHP51002 requires an output capacitor for stability. Because of its high bandwidth, Analog Devices recommends low-ESR and low-ESL ceramic capacitors. For stability, use a minimum of 10 μ F of output capacitance with ESR below 30m Ω and ESL below 1.5nH.

Because a single 10 μ F ceramic output capacitor provides high PSRR and low-noise performance, a larger output capacitor offers only marginal improvement because regulator bandwidth decreases as output capacitance increases; therefore, there is little to gain by using more than the minimum 10 μ F. However, larger output capacitors reduce peak output deviations during load transients.

Note that the bypass capacitors used to decouple individual components powered by the device increase the effective output capacitance.

Carefully consider the type of ceramic capacitors used. They are manufactured with a variety of dielectrics, each exhibiting different behavior with temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R, and X7R. Z5U and Y5V dielectrics provide high capacitance in small packages, but they tend to have stronger voltage and temperature coefficients, as shown in [Figure 69](#) and [Figure 70](#). When used with a 5V regulator, a 16V, 10 μ F Y5V capacitor can exhibit an effective value as low as 1 μ F to 2 μ F for the DC bias voltage across the operating temperature range.

The X5R and X7R dielectrics offer more stable characteristics and are therefore better suited for use with the RHP51002. The X7R dielectric has better temperature stability, while the X5R is less expensive and available in higher values. However, care must still be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify the operating temperature range and the maximum capacitance change over temperature. While the DC bias capacitance change for X5R and X7R is better than that of Y5V and Z5U dielectrics, it can still be significant enough to drop capacitance below acceptable levels. As shown in [Figure 71](#), capacitor DC bias characteristics improve as the component case size increases, **but verification of expected capacitance at the operating voltage is highly recommended**. Due to its good voltage coefficient in small case sizes, Analog Devices recommends using Murata's GJ8 series ceramic capacitor.

High Vibration Environments

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors exhibit a piezoelectric response. A piezoelectric device generates a voltage across its terminals when mechanical stress is applied, similar to how a piezoelectric microphone works. For a ceramic capacitor, mechanical vibrations within the system or thermal transients can induce this stress.

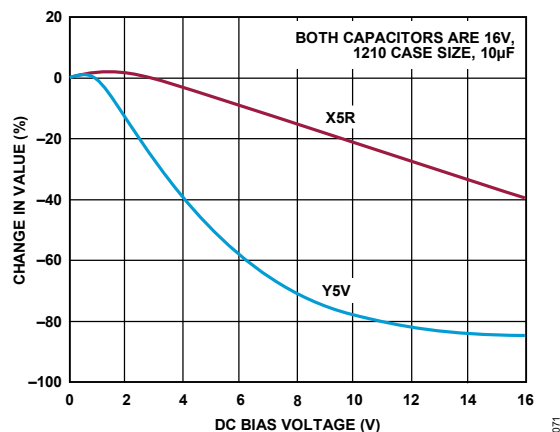


Figure 69. Ceramic Capacitor DC Bias Characteristics

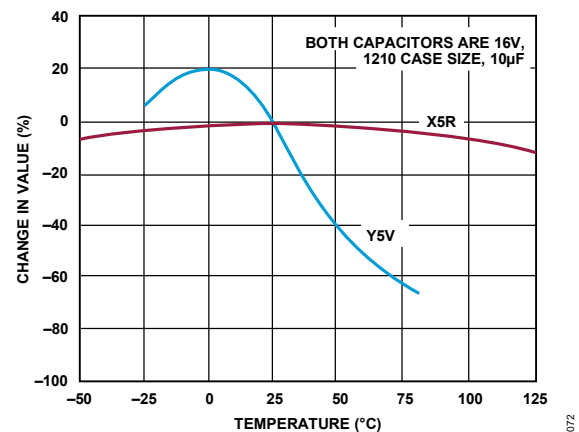


Figure 70. Ceramic Capacitor Temperature Characteristics

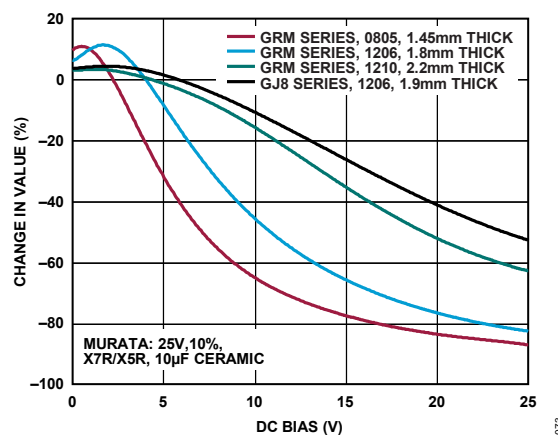


Figure 71. Capacitor Voltage Coefficient for Different Case Sizes

The RHP51002 applications in high-vibration environments feature three distinct piezoelectric noise generators: ceramic output, input, and SET pin capacitors. However, because the RHP51002-CSL has very low output impedance over a wide frequency range, it generates negligible output noise with a ceramic output capacitor. Similarly, because of the device's ultrahigh PSRR, a ceramic input capacitor generates negligible output noise. Given the SET pin's high impedance, any piezoelectric response from a ceramic SET pin capacitor can generate significant output noise; peak-to-peak excursions of hundreds of μV s are possible. However, because of the SET pin capacitor's high ESR and ESL tolerance, any non-piezoelectrically responsive (tantalum, electrolytic, or film) capacitor can be used at the SET pin; do note that electrolytic capacitors tend to have high $1/f$ noise. Surface-mount capacitors are highly recommended.

Stability and Input Capacitance

The RHP51002 is stable with a minimum $10\mu\text{F}$ IN pin capacitor. Analog Devices recommends using low ESR ceramic capacitors. Applications that use long wires to connect the power supply to the device's input and ground terminals, together with low-ESR ceramic input capacitors, are prone to voltage spikes, reliability concerns, and application-specific board oscillations. The wire inductance, combined with the low-ESR ceramic input capacitor, forms a high-Q resonant LC tank circuit. In some instances, this resonant frequency overlaps with the LDO output current bandwidth and interferes with stable operation. The resonant LC tank circuit formed by the wire inductance and the input capacitor causes this, not the device's instability.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. Wire diameter, however, has less influence on self-inductance. For example, the self-inductance of a 2-AWG isolated wire with a diameter of 0.26" is about half the inductance of a 30-AWG wire with a diameter of 0.01". One foot of 30-AWG wire has 465nH of self-inductance.

Several methods exist to reduce a wire's self-inductance. One method divides the current flowing towards the device between two parallel conductors. In this case, placing the wires farther apart reduces inductance, up to a 50% reduction when they are only a few inches apart. Splitting the wires connects two equal inductors in parallel. However, when placed in close proximity to each other, their mutual inductance adds to the overall self-inductance of the wires; therefore, a 50% reduction is not possible in such cases. The second, and more effective, technique to reduce overall inductance is to place the forward and return-current conductors (the input and ground wires) in close proximity. Two 30-AWG wires separated by 0.02" reduce the overall inductance to about one-fifth of a single wire.

If a battery mounted in close proximity powers the device, a $10\mu\text{F}$ input capacitor suffices for stability. If a distantly located supply powers the device, use a larger value input capacitor. Use a rough guideline of $1\mu\text{F}$ (in addition to the $10\mu\text{F}$ minimum) per 6" of wire length. The minimum input capacitance needed to stabilize the application also varies with the output capacitance and the load current. Placing additional capacitance on the device's output helps. However, this requires significantly more capacitance compared to additional input bypassing. Series resistance between the supply and the device input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use a higher ESR tantalum or electrolytic capacitor at the device input in parallel with a $10\mu\text{F}$ ceramic capacitor.

PSRR and Input Capacitance

For applications using the RHP51002 for post-regulating switching converters, placing a capacitor directly at the device input causes AC current (at the switching frequency) to flow near the device. This relatively high-frequency switching current generates magnetic fields that couple to the device output, degrading the effective PSRR. While highly dependent on the PCB layout, the switching preregulator, the input capacitor size, and other factors, PSRR degradation can easily exceed 30dB at 1MHz. This degradation is present even with the RHP51002 desoldered from the board; it is a degradation in the PCB's PSRR. While negligible in conventional low-PSRR LDOs, the device's ultrahigh PSRR requires careful attention to higher-order parasitics to realize the regulator's full performance.

To reduce high-frequency switching current near the device, you can remove the input capacitor entirely as long as the switching converter's output capacitor is more than an inch from the device. Magnetic coupling decreases rapidly with increasing distance. If the switching regulator is placed too far away (conservatively, more than a couple of inches) from the device, the lack of an input capacitor creates high impedance at the device input, and oscillation may occur. It is generally a common (and preferred) practice to bypass regulator inputs with some capacitance, so this option is fairly limited in its scope and not the most palatable solution.

To that end, Analog Devices recommends referencing the RHP51002 demo board layout to achieve the best possible PSRR performance. Two main factors contribute to higher PSRR with a poor layout. Parasitic trace inductance coupled with the low-ESR ceramic input capacitor can lead to higher input ripple in the LDO than at the output of the driving supply. Also, physical loops create magnetic fields that couple from the input to the output. The RHP51002 demo board uses layout techniques to minimize both parasitic inductance in traces and magnetic loop coupling, preventing PSRR degradation while keeping the input capacitor.

Filtering High Frequency Spikes

For applications where the RHP51002 post-regulates a switching converter, its high PSRR effectively suppresses any harmonic content present at the switching frequency (typically 100kHz to 4MHz). However, very high-frequency (hundreds of MHz) spikes associated with the switcher's power-switch transition times are beyond the device's bandwidth and will pass almost directly to the output. While the output capacitor is partly intended to absorb these spikes, its ESL limits its effectiveness at these frequencies. A ferrite bead or even the inductance associated with a short (for example, 0.5") PCB trace coupled with a capacitor with a low impedance at the transition frequency can serve as an LC-filter to suppress these very high-frequency spikes.

Output Noise

The RHP51002 offers many advantages in terms of noise performance. Traditional linear regulators have several sources of noise. The most critical noise sources in a traditional regulator are its voltage reference, error amplifier, noise from the resistor divider network used to set the output voltage, and the noise gain created by this resistor divider. Many low-noise regulators pin out their voltage reference to enable noise reduction by bypassing the reference voltage.

Unlike most linear regulators, the device does not use a voltage reference; instead, it uses a 100μA current reference. The current reference operates at a typical noise current level of $27 \text{ pA}/\sqrt{\text{Hz}}$ ($8 \text{ nA}_{\text{RMS}}$ over the 10Hz to 100kHz bandwidth). The resultant voltage noise equals the current noise multiplied by the resistor values, which is then RMS-summed with the error amplifier's noise and the resistor's Johnson noise of $\sqrt{4kTR}$ (k = Boltzmann's constant, $1.38 \times 10^{-23} \text{ J/K}$, and T is absolute temperature) to give the net output noise.

One problem with conventional linear regulators is that the resistor divider used to set the output voltage increases the reference noise. In contrast, the device's unity-gain follower architecture presents no gain from the SET pin to the output. Therefore, using a capacitor to bypass the SET-pin resistor makes output-voltage noise independent of the programmed output voltage. The resultant output noise is then determined only by the error amplifier's noise,

typically $2\text{nV}/\sqrt{\text{Hz}}$ from 1kHz to 1MHz and $0.8\mu\text{V}_{\text{RMS}}$ in the 10Hz to 100kHz bandwidth when using a $4.7\mu\text{F}$ SET pin capacitor. Paralleling multiple devices further reduces noise by $\sqrt{N}$ for N parallel regulators.

See the [Typical Performance Characteristics](#) section for noise spectral density and root mean square (RMS) integrated noise performance at various load currents and SET pin capacitances.

SET Pin (Bypass) Capacitance: Noise, PSRR, Transient Response and Soft-Start

In addition to reducing output noise, using a SET pin bypass capacitor also improves PSRR and transient performance. Note that any bypass-capacitor leakage deteriorates the RHP51002's DC regulation. Capacitor leakage of as little as 100nA causes a 0.1% DC error. Analog Devices recommends using a high-quality, low-leakage ceramic capacitor. Using a SET pin bypass capacitor also soft-starts the output and limits inrush current. The RC time constant formed by the SET pin resistor and capacitor determines soft-start time. Without the use of fast start-up, the ramp-up rate from 0 to 90% of nominal V_{OUT} is:

$$t_{\text{SS}} \approx 2.3 \times R_{\text{SET}} \times C_{\text{SET}} \text{ (fast start-up disabled)}$$

Fast Start-Up

For ultralow-noise applications requiring low 1/f noise performance at frequencies below 100Hz, a larger SET pin capacitor may be used. SET pin capacitance values up to $22\mu\text{F}$ are supported. While normally this would significantly increase the regulator's start-up time, the RHP51002 incorporates fast-start-up circuitry that increases the SET pin current to about 1.8mA during start-up.

As shown in the [Block Diagram](#), the 1.8mA current source remains engaged while PGFB is less than -300mV unless the regulator is in current limit, dropout, thermal shutdown, or the input voltage is below the minimum V_{IN} .

If fast start-up capability is not used, tie PGFB to IN or to OUT (for output voltages more than -300mV). Note that this action also disables the power-good functionality.

ENABLE/UVLO

The EN/UV pin places the regulator in a micropower shutdown state. The RHP51002 has an accurate -1.26V turn-on threshold on the EN/UV pin with 215mV of hysteresis. This threshold can be used in conjunction with a resistor divider from the input supply to define an accurate undervoltage lockout (UVLO) threshold for the regulator. When calculating the resistor divider network, consider the EN/UV pin current (I_{EN}) at the threshold. See [Table 1](#) (Electrical Characteristics table) and [Typical Performance Characteristics](#) for EN/UV pin characteristics. The EN/UV pin current can be ignored if R_{EN1} is less than $100\text{k}\Omega$. Use the following formula to determine resistor divider values. See [Figure 82](#) (Programming Undervoltage Lockout) in the [Typical Applications](#) section for more details.

$$V_{\text{IN(UVLO)}} = -1.26\text{V} \times (1 + R_{\text{EN2}} / R_{\text{EN1}}) - I_{\text{EN}} \times R_{\text{EN2}}$$

Since the EN/UV pin is bidirectional, it can also be pulled above 1.26V to turn on the device. In bipolar supply applications, the positive EN/UV threshold can be used to sequence device turn-on after the positive regulator turns on. If unused, tie the EN/UV pin to IN.

High Efficiency Linear Regulator—Input-to-Output Voltage Control

The VIOC pin controls an upstream switching converter. It enables a design that maximizes system efficiency while providing good transient response, low noise, and high power supply ripple rejection (PSRR) by maintaining a constant voltage across the RHP51002 regardless of the device's output voltage. This works well in applications where the output voltage varies to meet application requirements. This regulation loop also minimizes total power dissipation under fault conditions; if the output is short-circuited and the device hits its current limit, the VIOC amplifier lowers the switching regulator output voltage, limiting power dissipation in the device.

The VIOC pin is the output of a fast unity-gain amplifier that measures the voltage differential between IN and OUTS or $-1.5V$, whichever is lower. It typically connects to the feedback node or the resistor divider of most Analog Devices switching regulators or power modules, and sinks at least $100\mu A$ of current. Targeting a $-1V$ differential from input to output provides an optimal trade-off between power dissipation and PSRR. If paralleling multiple devices, tie the VIOC pin of one of the devices to the upstream switching converter's feedback pin and float the remaining VIOC pins.

The VIOC amplifier is designed to sink current, and only sources current through its internal impedance to ground. The VIOC pin has a typical impedance to ground of $40k\Omega \pm 15\%$. This is important to consider when using a maximum-input-voltage configuration or when the device is disabled.

As the VIOC buffer operates with high bandwidth, the switching converter's frequency compensation doesn't need to be adjusted while the VIOC buffer is inside the switching converter's feedback loop. Phase delay through the VIOC buffer is typically less than 4° for frequencies as high as $100kHz$; within the switching converter's bandwidth (usually well below $100kHz$), the VIOC buffer is transparent and acts like an ideal wire. For example, with a switching converter operating at a bandwidth below $100kHz$ and a phase margin of 50° , using the VIOC buffer reduces the phase margin by at most 4° . The net phase margin for the switching converter (using the VIOC pin) is at least 46° . With the VIOC buffer inside the switching converter's feedback loop, keep the total capacitance on the VIOC pin below $20pF$.

For $0 \geq V_{OUT} \geq -1.5V$, $V_{IN} = V_{VIOC(NOM)} - 1.5V$. For $V_{OUT} \leq -1.5V$, $V_{IN} = V_{OUT} + V_{VIOC(NOM)}$. The VIOC pin voltage (and the input-to-output differential) is programmable from $-0.41V$ (the regulator's dropout voltage) to $-1.3V$. As shown in [Figure 72](#), the input-to-output differential is easily programmed using the following equation:

$$V_{LDOIN} - V_{LDOOUT} = V_{VIOC(NOM)} = V_{FBSWITCHER} \times \frac{R1 + R2}{R1}$$

If the SET pin has an open-circuit fault condition, the device's input voltage will increase to the switching converter's maximum output voltage. It violates the device's absolute maximum rating for V_{IN} . To prevent this, adding an optional resistor ($R3$) between the VIOC and IN pins of the regulator gives a maximum voltage configuration based on the following equation:

$$V_{LDOIN(MAX)} = V_{FBSWITCHER} \frac{R1 + R2 + R3}{R1} + V_{VIOC(NOM)} \frac{R3}{40k\Omega}$$

Typical VIOC Applications

Figure 73 shows an application using an inverting regulator to power the RHP51002, delivering a -3.3V output. The resistors shown drive the inverting regulator's FBX pin to -0.8V , so that its output is -4.3V (with -1V on the VIOC pin) when the device is operating at -3.3V output, and -5V when the device is disabled.

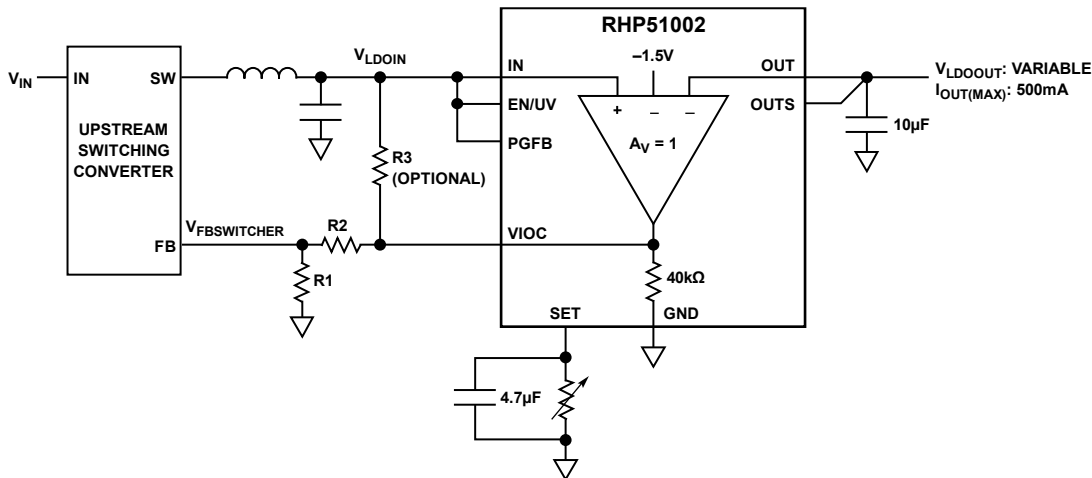


Figure 72. Typical VIOC Application

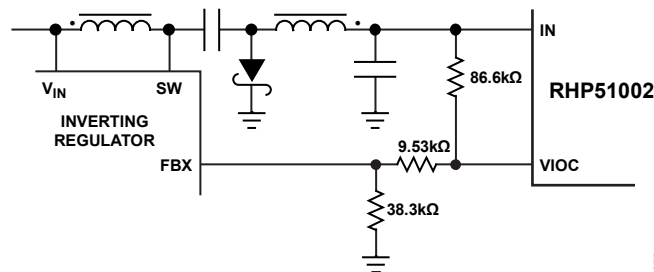


Figure 73. VIOC Connection Using an Inverting Regulator Delivers -4.3V when Operating, -5V when the Device is Disabled

Figure 74 illustrates an alternative inverting regulator configuration. The inverting regulator's FBX pin regulates at 3mV (typical) with $83.3\mu\text{A}$ flowing out of the pin (IFBX). Because of this, only a single resistor is needed between the FBX pin and VIOC (from Figure 72, only R2 is necessary; R1 is not needed). In this case, the resistor is calculated as follows:

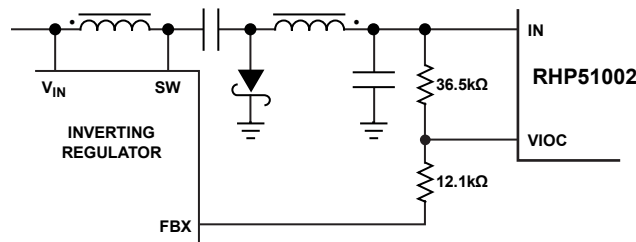


Figure 74. VIOC Connection Using an Inverting Regulator

$$V_{LDOIN} - V_{LDOOUT} = V_{VIOC(NOM)} = V_{FBX} - R2 \times I_{FBX}$$

For the optional maximum voltage configuration, R3 is added, and the maximum input voltage to the device is calculated as follows:

$$V_{LDOIN(MAX)} = V_{VIOC(NOM)} + V_{VIOC(NOM)} \frac{R3}{40k} - R3 \times I_{FBX}$$

Again, the resistors shown are configured to drive the switcher's output to $-4.3V$ when the device is operating at $-3.3V$, and to $-5V$ when disabled. Using the circuit from [Figure 74](#), the LDO's input and output are shown in [Figure 75](#) when pulsing the device's EN/UV pin. As shown, when the LDO is disabled, the LDO input voltage goes to the maximum voltage set by the resistor divider on the VIOC pin. [Figure 76](#) shows the load step response of the LT8580 using the VIOC buffer. [Figure 77](#) shows the LDO's input and output voltage response to stepping the SET pin voltage from $-3V$ to $-4V$. [Figure 78](#) shows the LDO's input and output voltage while ramping the SET pin from $0V$ to $-4.5V$; as shown, the LT8580's output voltage tracks the device's output voltage below $-1.5V$ and limits to the maximum voltage set by the resistor divider on the VIOC pin. Last, [Figure 79](#) shows the noise spectral density at the device's input and output.

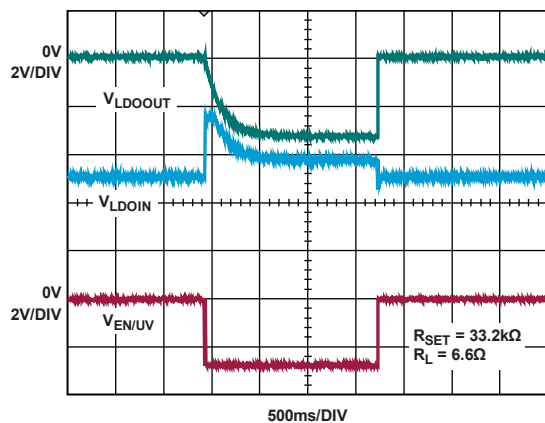


Figure 75. RHP51002-CSL EN/UV Pulse

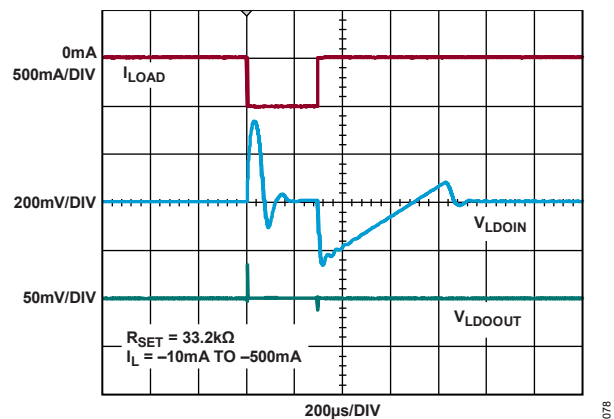


Figure 76. Load-Step Response using the VIOC Buffer

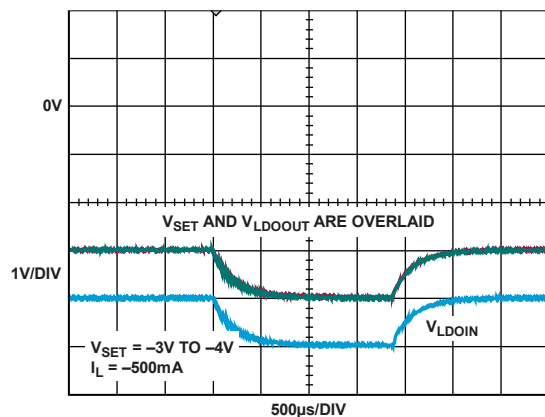


Figure 77. Stepping V_{SET} from $-3V$ to $-4V$ (and back to $-3V$)

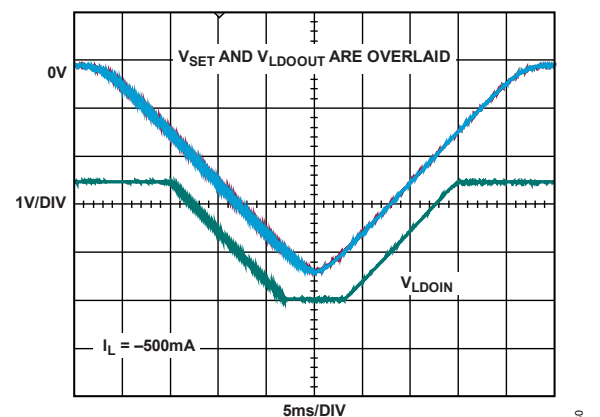


Figure 78. Ramping V_{SET} from $0V$ to $-4.5V$ (and back to $0V$)

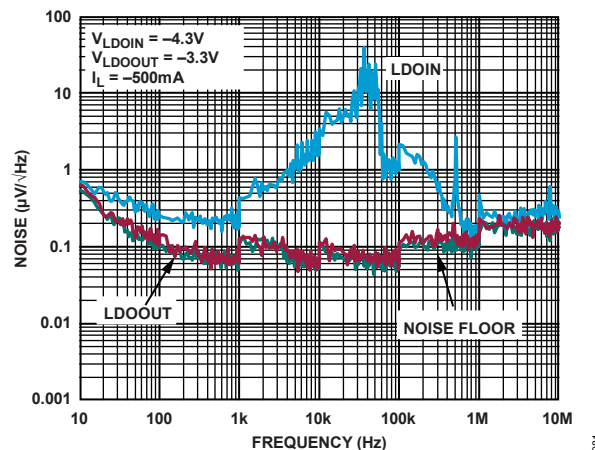


Figure 79. RHP51002's Input and Output Noise Spectral Density

Programmable Power Good

As shown in the [Block Diagram](#), the power good threshold is user-programmable using the ratio of two external resistors, R_{PG1} and R_{PG2} :

$$V_{OUT(PG_THRESH)} = -0.3V(1 + R_{PG1}/R_{PG2}) - I_{PGFB} \times R_{PG1}$$

If the PGFB pin falls below -300mV, the open-collector PG pin deasserts and becomes high-impedance. The power good comparator has 7mV hysteresis and a 5µs of deglitching. The PGFB pin current (I_{PGFB}) can be ignored if R_{PG2} is less than 30kΩ; it must be considered when determining the resistor divider network. If the power good functionality is not used, float the PG pin. Please note that programmable power good and fast-start-up capabilities are disabled for output voltages between 0V and -300mV.

Ensure care when laying out traces for PG and PGFB on a PCB. If the PG and PGFB pins are run close to each other for a distance (typically greater than two inches), stray capacitance from trace-to-trace couples the PG signal into the high-impedance PGFB signal. Since PG is out of phase relative to PGFB, this results in oscillation. To avoid this, minimize the distance the two traces run close together; using lower-value resistors for the PGFB divider also helps by lowering the impedance seen at the PGFB pin.

Externally Programmable Current Limit

The I_{LIM} pin internally regulates to -300mV. Connecting a resistor from ground to I_{LIM} sets the current flowing into the I_{LIM} pin, which in turn programs the RHP51002's current limit. With the 3.75kΩ × A programming scale factor, the current limit can be calculated as follows:

$$\text{Current Limit} = 3.75k\Omega \times A/R_{LIM}$$

For example, a 7.5kΩ resistor programs the current limit to 500mA, and a 15kΩ resistor programs the current limit to 250mA. For better accuracy, Kelvin connect this resistor to the device's GND pin.

When the IN-to-OUT differential exceeds 7V, the RHP51002's foldback circuitry reduces the internal current limit. As a result, the internal current limit may override the externally programmed current limit to keep the device within its safe operating area (SOA). See the graph of internal current limit vs. input-to-output differential in the [Typical Performance Characteristics](#) section. If not used, connect I_{LIM} to GND.

Output Overshoot Recovery

During a load step from heavy load to very light or no load, the output voltage overshoots before the regulator responds and turns off the power transistor. With very light or no load, it takes a long time to discharge the output capacitor.

The RHP51002 incorporates an overshoot-recovery circuit that turns on a current source to discharge the capacitor when OUTS exceeds SET. This current is typically 3.5mA.

If OUTS is externally held above SET, the current source turns on to restore OUTS to its programmed voltage. The current source remains on until the external circuitry releases OUTS.

Direct Paralleling for Higher Current

To get higher output current, parallel multiple RHP51002s. Connect all SET pins together and all IN pins together. Connect the OUT pins together using small pieces of PCB trace (used as a ballast resistor) to equalize currents in the devices. PCB trace resistance in mΩ/inch is shown in [Table 8](#).

Table 8. PC Board Trace Resistance

WEIGHT (oz)	10mil WIDTH	20mil WIDTH
1	54.3	27.1
2	27.1	13.6

Trace resistance is measured in mΩ/in.

The small worst-case offset of 2mV for each paralleled RHP51002 minimizes the required ballast resistor value. [Figure 80](#) illustrates that two RHP51002s, each using a 20mΩ PCB trace ballast resistor, provide better than 20% accurate output current sharing at full load. The two 20mΩ external resistors only add 10mV of output regulation drop with a 1A maximum current. With a –3.3V output, this only adds 0.3% to the regulation accuracy. As has been discussed previously, tie the OUTS pins directly to the output capacitors.

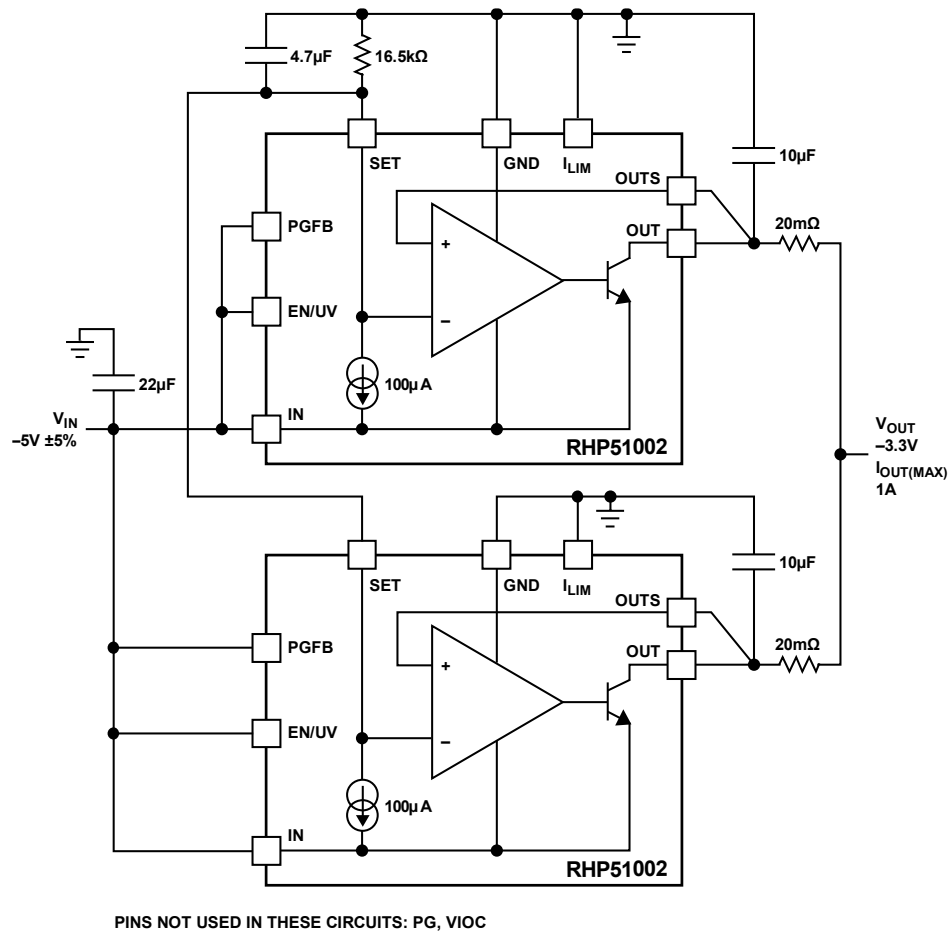


Figure 80. Parallel Devices

More than two RHP51002s can also be paralleled for even higher output current and lower output noise. Paralleling multiple RHP51002s also helps distribute heat on the PCB. For applications with a high input-to-output voltage differential, an input series resistor or a resistor in parallel with the RHP51002 can also be used to spread heat.

PCB Layout Considerations

Given the RHP51002's high bandwidth and ultrahigh PSRR, careful PCB layout must be employed to achieve full device performance. [Figure 81](#) shows a recommended layout that delivers full regulator performance. Refer to the RHP51002's demo board manual for further details.

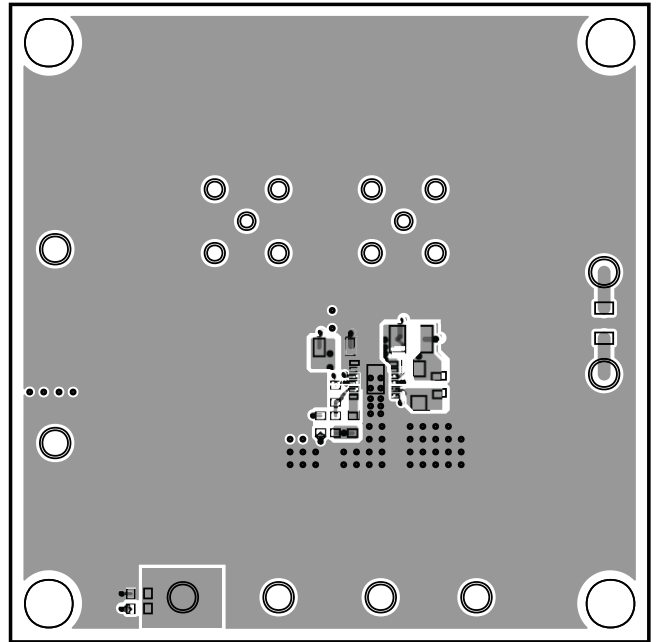


Figure 81. Recommended Layout

Thermal Considerations

The RHP51002 has internal power and thermal limiting circuits that protect the device under overload conditions. The thermal shutdown temperature is nominally 167°C with about 8°C of hysteresis. For continuous normal-load conditions, do not exceed the maximum junction temperature (125°C). It is important to consider all sources of thermal resistance from the junction to the ambient. This includes junction-to-case, case-to-heat sink interface, heat sink resistance, or circuit board-to-ambient as the application dictates. Additionally, consider all heat sources in close proximity to the RHP51002.

The underside of the MSOP package has exposed metal from the lead frame to the die attachment. Both packages allow heat to transfer directly from the die junction to the PCB metal, limiting the maximum operating junction temperature. The dual-in-line pin arrangement allows metal to extend beyond the package ends on the topside (component side) of the PCB.

For surface-mount devices, heat sinking is accomplished using the heat-spreading capabilities of the PCB and its copper traces. Copper board stiffeners and plated-through holes can also spread the heat generated by the regulator.

[Table 9](#) lists thermal resistance as a function of copper area on a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes and 2oz top/bottom planes with a total board thickness of 1.6mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout, and thermal vias affect the resultant thermal resistance. For more information on thermal resistance and high-thermal-conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-7 and JESD51-12. Achieving low thermal resistance necessitates attention to detail and careful PCB layout.

Table 9. Measured Thermal Resistance for MSOP Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE
TOP SIDE*	BOTTOM SIDE		
2500mm ²	2500mm ²	2500mm ²	33°C/W
1000mm ²	2500mm ²	2500mm ²	33°C/W
225mm ²	2500mm ²	2500mm ²	34°C/W
100mm ²	2500mm ²	2500mm ²	35°C/W

Calculating Junction Temperature

Example: Given an output voltage of -3.3V and an input voltage of -5V ±5%, an output current range from 1mA to 500mA, and a maximum ambient temperature of 85°C, what is the maximum junction temperature?

The RHP51002-CSL's power dissipation is:

$$I_{OUT(MAX)} \times (V_{IN(MAX)} - V_{OUT}) + I_{GND} \times V_{IN(MAX)}$$

where:

$$I_{OUT(MAX)} = -500\text{mA}$$

$$V_{IN(MAX)} = -5.25\text{V}$$

$$I_{GND} \text{ (at } I_{OUT} = 500\text{mA and } V_{IN} = -5.25\text{V)} = -9\text{mA}$$

thus:

$$P_{DISS} = -0.5\text{A} \times (-5.25\text{V} + 3.3\text{V}) + 9\text{mA} \times 5.25\text{V} = 1.02\text{W}$$

The thermal resistance ranges from 33°C/W to 35°C/W, depending on the copper area. Therefore, the junction temperature rise above ambient approximately equals:

$$1.02\text{W} \times 34^\circ\text{C/W} = 34.68^\circ\text{C}$$

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient:

$$T_{J(MAX)} = 85^\circ\text{C} + 34.68^\circ\text{C} = 119.68^\circ\text{C}$$

Overload Recovery

Like many IC power regulators, the RHP51002 incorporates safe-operating-area (SOA) protection. The SOA protection activates when the input-to-output differential voltage exceeds 7V. The SOA protection reduces the current limit as the input-to-output differential increases, keeping the power transistor within a safe operating region for all input-to-output voltages up to the device's [Absolute Maximum Ratings](#). The device provides a level of output current for all input-to-output differential voltages. See the Current Limit curves in the [Typical Performance Characteristics](#) section. When power is first applied and the input voltage rises, the output follows the input and keeps the input-to-output differential low, allowing the regulator to supply large output current and start-up into high-current loads.

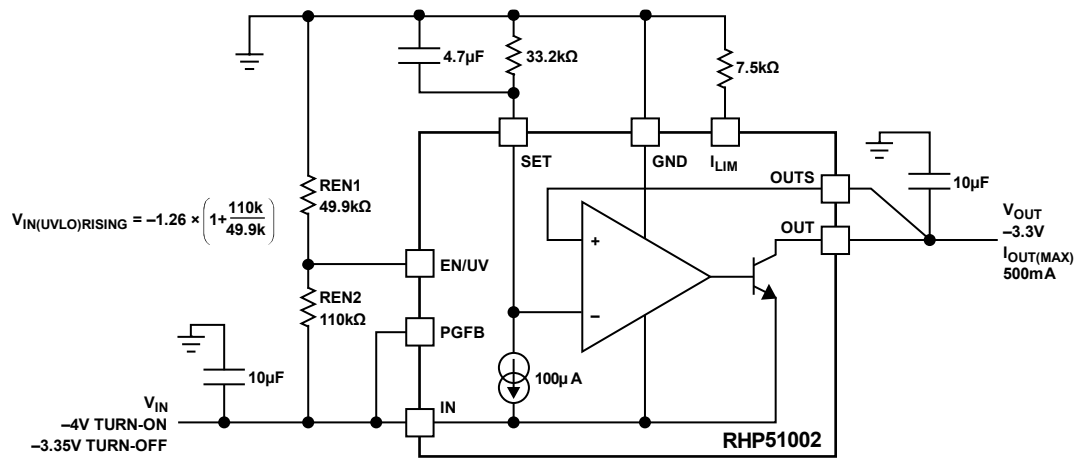
However, due to current-limit foldback, a problem can occur at high input voltages if the output voltage is low and the load current is high. This can happen after removing a short circuit or if the EN/UV pin is pulled high after the input voltage has already turned on. In such cases, the load line intersects the output current profile at two points. The regulator now has two stable operating points. With this double intersection, the input power supply may need to be cycled down to zero and brought back up to recover the output. Other linear regulators with foldback current limit protection also exhibit this phenomenon, so it is not unique to the RHP51002.

Protection Features

The RHP51002 incorporates several protection features for sensitive applications. Precision current limit and thermal overload protection safeguard the device against overload and fault conditions at the device's output. For normal operation, do not allow the junction temperature to exceed 125°C.

Pulling the RHP51002's output above ground induces no damage to the part. If IN is left open circuit or grounded, OUT can be pulled 20V above GND. In this condition, a maximum current of 25mA flows into the OUT pin and out of the GND pin. If IN is powered by a voltage source, OUT sinks the device's (foldback) short circuit current and protects itself by thermal limiting. In this case, however, grounding the EN/UV pin turns off the device and stops OUT from sinking the short-circuit current.

TYPICAL APPLICATIONS



PINS NOT USED IN THIS CIRCUIT: PG, VIOC

Figure 82. Programming Undervoltage Lockout

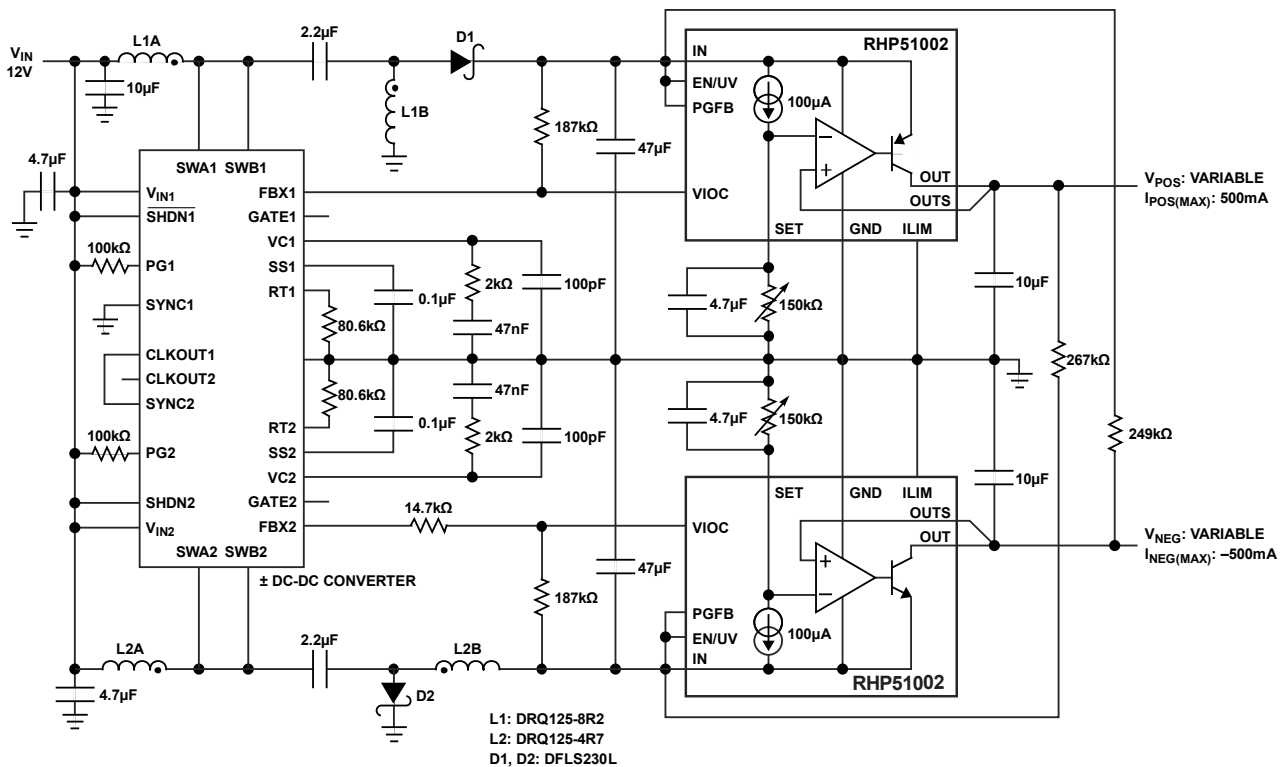


Figure 83. Positive and Negative Variable Supply

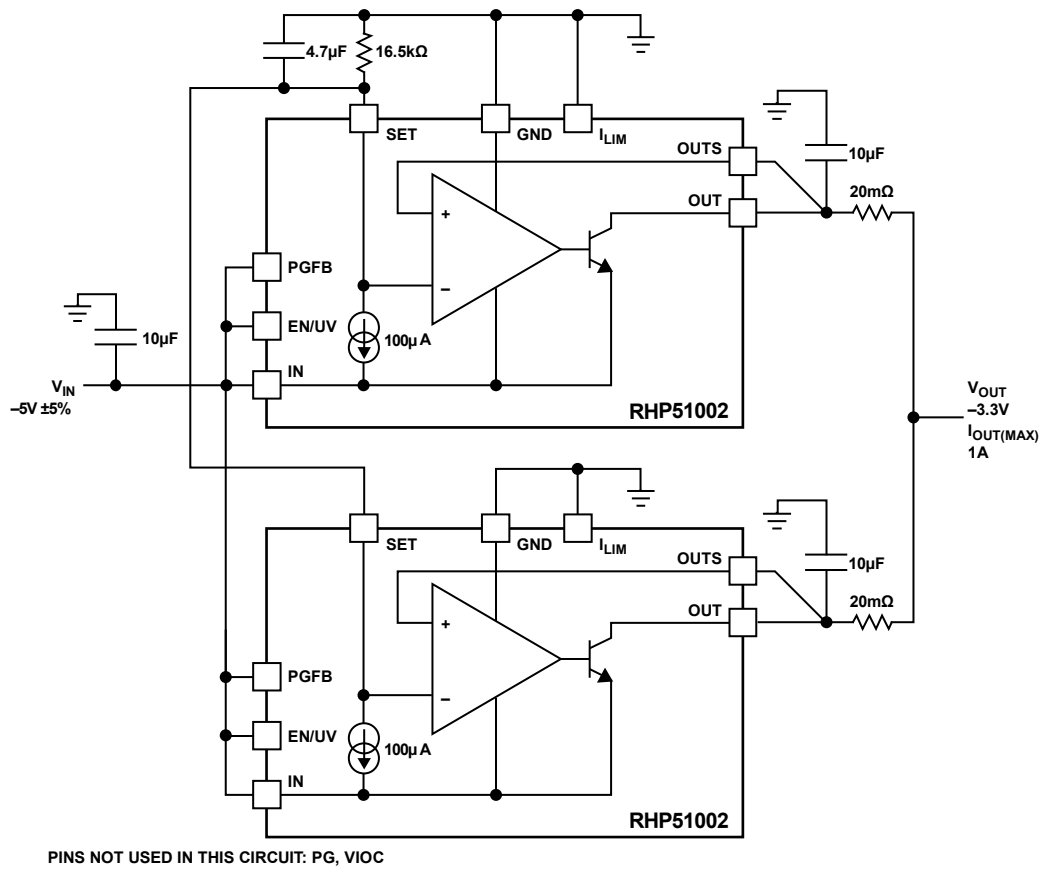
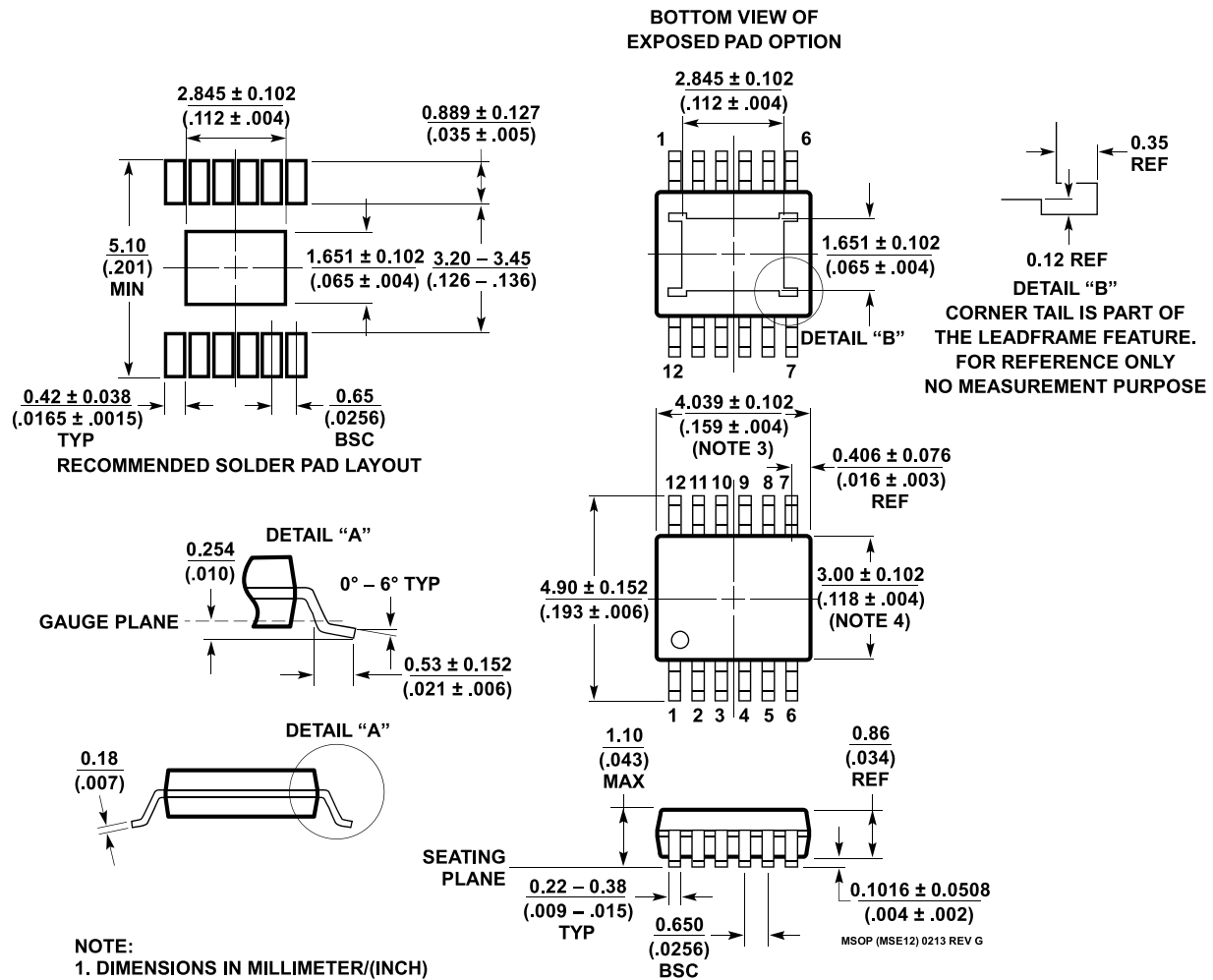


Figure 84. Parallel Devices

086

PACKAGE DESCRIPTION



NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm ($.006''$) PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm ($.006''$) PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm ($.004''$) MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL NOT EXCEED 0.254mm ($.010''$) PER SIDE.

ORDERING GUIDE

MODEL	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE QUANTITY	MARKING CODE
RHP51002IMSE-CSL#PBF	–40°C to 125°C	12-Lead Plastic MSOP	Tube, 1	51002
RHP51002IMSE-CSL#TRPBF	–40°C to 125°C	12-Lead Plastic MSOP	Reel, 2500	51002

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<i>RHP51000</i>	20V, 500mA, Ultralow Noise Ultrahigh PSRR Linear Regulator for Commercial Space	0.8 μ V _{RMS} Noise and 75dB PSRR at 1MHz, V _{IN} = 3V to 20V, 260mV Dropout Voltage, MSOP Package

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