Data Sheet

RHP51000

20V, 500mA, Ultra-Low Noise, Ultra-High PSRR, LDO Regulator for Commercial Space

FEATURES

- No SEL up to ~79.9 MeV·cm2/mg at V_{IN} ≤ 16V
- TID Assured up to 10krad(Si) Post-Accelerated Anneal
- Ultra-Low RMS Noise: 0.8μV_{RMS} (10Hz to 100kHz)
- Ultra-Low Spot Noise: 2nV/√Hz at 10kHz
- Ultra-High PSRR: 76dB at 1MHz
- Output Current: 500mA
- Wide Input-Voltage Range: 2V to 20V
- Single Capacitor Improves Noise and PSRR
- 100μA SET Pin Current: ±1% Initial Accuracy
- VIOC Pin Controls Upstream Regulator to Minimize Power Dissipation
- Programmable Current Limit
- Low Dropout Voltage: 260mV
- Output-Voltage Range: 0 to 15V
- Programmable Power Good
- Fast Start-Up Capability
- Parallelable for Lower Noise and Higher Current
- Internal Current Limit with Foldback
- Minimum Output Capacitor: 10μF Ceramic
- Reverse-Battery and Reverse-Current Protection
- 12-Lead MSOP Package

COMMERCIAL SPACE FEATURES

- Supports Aerospace Applications
- Wafer Diffusion Lot Traceability
- Radiation Monitors
- Single-Event Latch-Up (SEL)
- Total Ionizing Dose (TID)
- Outgassing Characterization

GENERAL DESCRIPTION

The RHP51000-CSL is a high-performance low-dropout linear regulator featuring Analog Devices, Inc., ultra-low noise and ultra-high power supply rejection ratio (PSRR) architecture for powering noise-sensitive applications. Designed as a precision current reference followed by a high-performance voltage buffer, the RHP51000-CSL can be easily paralleled to further reduce noise, increase output current, and spread heat on the printed circuit board (PCB). In addition to the RHP51000-CSL feature set, the RHP51000-CSL incorporates a voltage input-to-output control (VIOC) tracking function to control an upstream switching converter to maintain a constant voltage across the RHP51000-CSL, thereby minimizing power dissipation.

The device supplies 500mA at a typical 260mV dropout voltage. Operating quiescent current is nominally 2.2mA and drops to <1μA in shutdown. The wide output-voltage range (0 to 15V) of the RHP51000-CSL, while maintaining unity-gain operation, provides virtually constant output noise, PSRR, bandwidth, and load regulation, independent of the programmed output voltage. Additionally, the regulator features programmable current limit, fast start-up capability, and programmable power good to indicate output-voltage regulation.

The RHP51000-CSL is stable with a minimum 10μF ceramic output capacitor. Built-in protection includes reverse-battery protection, reverse-current protection, internal current limit with foldback and thermal limit with hysteresis. The RHP51000-CSL is available in a thermally enhanced, 12-lead MSOP package.

APPLICATIONS

- Low Earth Orbit (LEO) Satellites
- Avionics
- Point-to-Point Communication Systems
- Very Low-Noise Instrumentation
- High-Speed/High-Precision Data Converters
- Post-Regulator for Switching Supplies

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TYPICAL APPLICATION

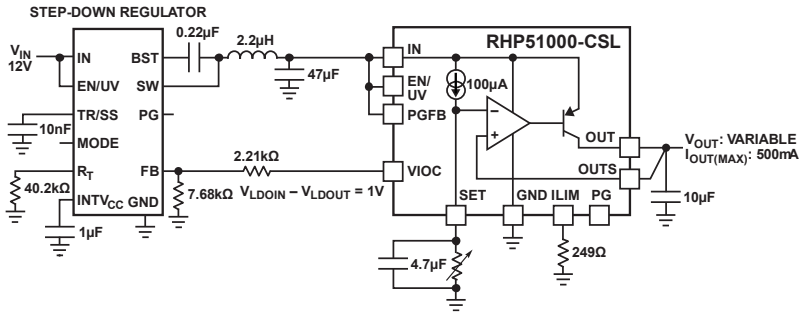


Figure 1. Typical Application Circuit

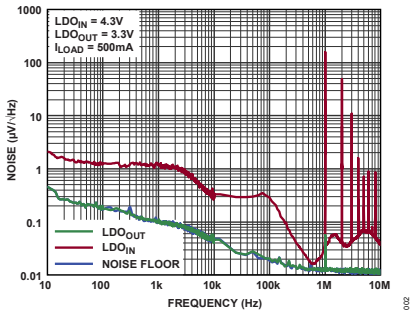


Figure 2. Noise Spectral Density

TABLE OF CONTENTS

SPECIFICATIONS

Table 1. Electrical Characteristics

(The -40°C ≤ T_J ≤ 125°C denotes the specifications that apply over the full operating temperature range; otherwise, specifications are at T_A = 25°C. The same electrical characteristics apply to radiation tests and limits, tested at ambient temperature (T_A) of 25°C. TID testing characterized up to 10krad(Si).)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Input-Voltage Range	V_{IN}		-40°C ≤ T_J ≤ 125°C	2		20	V
Minimum IN Pin Voltage[1]		I_{LOAD} = 500mA, V_{IN} UVLO Rising	-40°C ≤ T_J ≤ 125°C		1.8		V
		V_{IN} UVLO hysteresis			75		mV
Output-Voltage Range	V_{OUT}	V_{IN} > V_{OUT}	-40°C ≤ T_J ≤ 125°C	0		15	V
SET Pin Current	(I_{SET})	V_{IN} = 2V, I_{LOAD} = 1mA, V_{OUT} = 1.3V		99	100	101	µA
		2V < V_{IN} < 20V, 0V < V_{OUT} < 15V, 1mA < I_{LOAD} < 500mA[2]	-40°C ≤ T_J ≤ 125°C	98	100	102	µA
Fast Start-Up Set Pin Current		V_{PGFB} = 289mV, V_{IN} = 2.8V, V_{SET} = 1.3V			2		mA
Output Offset Voltage (V_{OUT} – V_{SET})[3]	V_{OS}	V_{IN} = 2V, I_{LOAD} = 1mA, V_{OUT} = 1.3V		–1		1	mV
		2V < V_{IN} < 20V, 0V < V_{OUT} < 15V, 1mA < I_{LOAD} < 500mA[2]	-40°C ≤ T_J ≤ 125°C	–2		2	mV
Line Regulation	ΔI_{SET}	V_{IN} = 2V to 20V, I_{LOAD} = 1mA, V_{OUT} = 1.3V	-40°C ≤ T_J ≤ 125°C		0.5	±2	nA/V
	ΔV_{OS}	V_{IN} = 2V to 20V, I_{LOAD} = 1mA, V_{OUT} = 1.3V[3]	-40°C ≤ T_J ≤ 125°C		0.5	±3	µV/V
Load Regulation	ΔI_{SET}	I_{LOAD} = 1mA to 500mA, V_{IN} = 2V, V_{OUT} = 1.3V			3		nA
	ΔV_{OS}	I_{LOAD} = 1mA to 500mA, V_{IN} = 2V, V_{OUT} = 1.3V[3]	-40°C ≤ T_J ≤ 125°C		0.1	0.5	mV
Change in I_{SET} with V_{SET}		V_{SET} = 1.3V to 15V, V_{IN} = 20V, I_{LOAD} = 1mA	-40°C ≤ T_J ≤ 125°C		30	400	nA
Change in V_{OS} with V_{SET}		V_{SET} = 1.3V to 15V, V_{IN} = 20V, I_{LOAD} = 1mA[3]	-40°C ≤ T_J ≤ 125°C		0.03	0.6	mV
Change in I_{SET} with V_{SET}		V_{SET} = 0V to 1.3V, V_{IN} = 20V, I_{LOAD} = 1mA	-40°C ≤ T_J ≤ 125°C		150	600	nA

(The -40°C ≤ T_J ≤ 125°C denotes the specifications that apply over the full operating temperature range; otherwise, specifications are at T_A = 25°C. The same electrical characteristics apply to radiation tests and limits, tested at ambient temperature (T_A) of 25°C. TID testing characterized up to 10krad(Si).)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Change in V_{OS} with V_{SET}		V_{SET} = 0V to 1.3V, V_{IN} = 20V, I_{LOAD} = 1mA[3]	-40°C ≤ T_J ≤ 125°C		0.3	2	mV
Dropout Voltage[4]		I_{LOAD} = 1mA, 50mA			220	275	mV
		I_{LOAD} = 1mA, 50mA	-40°C ≤ T_J ≤ 125°C			330	mV
		I_{LOAD} = 300mA			220	280	mV
		I_{LOAD} = 300mA	-40°C ≤ T_J ≤ 125°C			350	mV
		I_{LOAD} = 500mA			260	350	mV
		I_{LOAD} = 500mA	-40°C ≤ T_J ≤ 125°C			450	mV
GND Pin Current V_{IN} = $V_{OUT(NOMINAL)}$[5]		I_{LOAD} = 10µA			2.2		mA
		I_{LOAD} = 1mA	-40°C ≤ T_J ≤ 125°C		2.4	4	mA
		I_{LOAD} = 50mA	-40°C ≤ T_J ≤ 125°C		3.5	5.5	mA
		I_{LOAD} = 100mA	-40°C ≤ T_J ≤ 125°C		4.3	7	mA
		I_{LOAD} = 500mA	-40°C ≤ T_J ≤ 125°C		15	25	mA
Output-Noise Spectral Density[3, 7]		I_{LOAD} = 500mA, frequency = 10Hz, C_{OUT} = 10µF, C_{SET} = 0.47µF, V_{OUT} = 3.3V			500		nV/√Hz
		I_{LOAD} = 500mA, frequency = 10Hz, C_{OUT} = 10µF, C_{SET} = 4.7µF, 1.3V ≤ V_{OUT} ≤ 15V			70		nV/√Hz
		I_{LOAD} = 500mA, frequency = 10kHz, C_{OUT} = 10µF, C_{SET} = 0.47µF, 1.3V ≤ V_{OUT} ≤ 15V			2		nV/√Hz
		I_{LOAD} = 500mA, frequency = 10kHz, C_{OUT} = 10µF, C_{SET} = 0.47µF, 0V ≤ V_{OUT} < 1.3V			5		nV/√Hz
Output RMS Noise[3, 7]		I_{LOAD} = 500mA, BW = 10Hz to 100kHz, C_{OUT} = 10µF, C_{SET} = 0.47µF, V_{OUT} = 3.3V			2.5		$µV_{RMS}$
		I_{LOAD} = 500mA, BW = 10Hz to 100kHz, C_{OUT} = 10µF, C_{SET} = 4.7µF, 1.3V ≤ V_{OUT} ≤ 15V			0.8		$µV_{RMS}$
		I_{LOAD} = 500mA, BW = 10Hz to 100kHz, C_{OUT} = 10µF, C_{SET} = 4.7µF, 0V ≤ V_{OUT} < 1.3V			1.8		$µV_{RMS}$

(The -40°C ≤ T_J ≤ 125°C denotes the specifications that apply over the full operating temperature range; otherwise, specifications are at T_A = 25°C. The same electrical characteristics apply to radiation tests and limits, tested at ambient temperature (T_A) of 25°C. TID testing characterized up to 10krad(Si).)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Reference Current RMS Output Noise[3, 7]		BW = 10Hz to 100kHz			6		nA_{RMS}
Ripple Rejection 1.3V ≤ V_{OUT} ≤ 15V V_{IN} – V_{OUT} = 2V (Avg)[3, 7]		V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 4.7µF			117		dB
		V_{RIPPLE} = 150 mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			90		dB
		V_{RIPPLE} = 150 mV_{P-P}, f_{RIPPLE} = 100kHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			77		dB
		V_{RIPPLE} = 150 mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			76		dB
		V_{RIPPLE} = 80mV_{P-P}, f_{RIPPLE} = 10MHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			53		dB
Ripple Rejection 0V ≤ V_{OUT} < 1.3V V_{IN} – V_{OUT} = 2V (Avg)[3, 7]		V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			104		dB
		V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			85		dB
		V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 100kHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			72		dB
		V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			64		dB
		V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 10MHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			54		dB
EN/UV Pin Threshold		EN/UV trip point rising (turn-on), V_{IN} = 2V	-40°C ≤ T_J ≤ 125°C	1.18	1.24	1.32	V

(The -40°C ≤ T_J ≤ 125°C denotes the specifications that apply over the full operating temperature range; otherwise, specifications are at T_A = 25°C. The same electrical characteristics apply to radiation tests and limits, tested at ambient temperature (T_A) of 25°C. TID testing characterized up to 10krad(Si).)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
EN/UV Pin Hysteresis		EN/UV trip point hysteresis, V_{IN} = 2V			130		mV
EN/UV Pin Current		$V_{EN/UV}$ = 0V, V_{IN} = 20V	-40°C ≤ T_J ≤ 125°C			±1	µA
		$V_{EN/UV}$ = 1.24V, V_{IN} = 20V			0.03		µA
		$V_{EN/UV}$ = 20V, V_{IN} = 0V	-40°C ≤ T_J ≤ 125°C		8	15	µA
Quiescent Current in Shutdown ($V_{EN/UV}$ = 0V)		V_{IN} = 6V			0.3	1	µA
		V_{IN} = 6V	-40°C ≤ T_J ≤ 125°C			10	µA
Internal Current Limit[11]		V_{IN} = 2V, V_{OUT} = 0V	-40°C ≤ T_J ≤ 125°C	570	710	850	mA
		V_{IN} = 12V, V_{OUT} = 0V			700		mA
		V_{IN} = 20V, V_{OUT} = 0V	-40°C ≤ T_J ≤ 125°C	230	330	430	mA
Programmable Current Limit		Programming scale factor: 2V < V_{IN} < 20V[10]			150		mA × kΩ
		V_{IN} = 2V, V_{OUT} = 0V, R_{ILIM} = 300Ω	-40°C ≤ T_J ≤ 125°C	450	500	550	mA
		V_{IN} = 2V, V_{OUT} = 0V, R_{ILIM} = 1.5kΩ	-40°C ≤ T_J ≤ 125°C	90	100	110	mA
PGFB Trip Point		PGFB trip point rising	-40°C ≤ T_J ≤ 125°C	291	300	309	mV
PGFB Hysteresis		PGFB trip point hysteresis			7		mV
PGFB Pin Current		V_{IN} = 2V, V_{PGFB} = 300mV			25		nA
PG Output Low Voltage		I_{PG} = 100µA	-40°C ≤ T_J ≤ 125°C		30	100	mV
PG Leakage Current		V_{PG} = 20V	-40°C ≤ T_J ≤ 125°C			1	µA
Reverse Input Current		V_{IN} = –20V, $V_{EN/UV}$ = 0V, V_{OUT} = 0V, V_{SET} = 0V	-40°C ≤ T_J ≤ 125°C			100	µA
Reverse Output Current		V_{IN} = 0, V_{OUT} = 5V, SET = Open			14	25	µA
Minimum Load Required[12]		V_{OUT} < 1V	-40°C ≤ T_J ≤ 125°C	10			µA
Thermal Shutdown		T_J Rising			165		°C
		Hysteresis			8		°C

(The -40°C ≤ T_J ≤ 125°C denotes the specifications that apply over the full operating temperature range; otherwise, specifications are at T_A = 25°C. The same electrical characteristics apply to radiation tests and limits, tested at ambient temperature (T_A) of 25°C. TID testing characterized up to 10krad(Si).)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Start-Up Time		$V_{OUT(NOM)}$ = 5V, I_{LOAD} = 500mA, C_{SET} = 0.47µF, V_{IN} = 6V, V_{PGFB} = 6V			55		ms
		$V_{OUT(NOM)}$ = 5V, I_{LOAD} = 500mA, C_{SET} = 4.7µF, V_{IN} = 6V, V_{PGFB} = 6V			550		ms
		$V_{OUT(NOM)}$ = 5V, I_{LOAD} = 500mA, C_{SET} = 4.7µF, V_{IN} = 6V, R_{PG1} = 50kΩ, R_{PG2} = 700kΩ (with fast start-up to 90% of V_{OUT})			10		ms
Thermal Regulation		10ms pulse			– 0.01		%/W
Input-to-Output Differential Voltage Control (VIOC)[14]		VIOC amplifier gain			1		V/V
		VIOC pin voltage range: V_{OUT} > V_{VIOC} + 0.5V	-40°C ≤ T_J ≤ 125°C	1		4	V
		VIOC pin voltage: V_{OUT} ≤ 1.5V, V_{IN} = 2.5V			1		V
		VIOC pin source current	-40°C ≤ T_J ≤ 125°C	200			µA
		VIOC pin sink current: V_{IN} ≥ 2.5V	-40°C ≤ T_J ≤ 125°C			15	µA

1 The EN/UV pin threshold must be met to ensure device operation.

2 The maximum T_J limits operating conditions. The regulated output-voltage specification does not apply for all possible combinations of input voltage and output current, especially due to the internal current-limit foldback, which starts to decrease current limit at V_{IN} – V_{OUT} > 12V. If operating at maximum output current, limit the input-voltage range. If operating at the maximum input voltage, limit the output-current range.

3 OUTS ties directly to OUT.

4 Dropout voltage is the minimum input-to-output differential voltage needed to maintain regulation at a specified output current. The dropout voltage is measured when output is 1% out of regulation. This definition results in a higher dropout voltage compared to hard dropout, which is measured when V_{IN} = $V_{OUT(NOMINAL)}$. For lower output voltages less than 1.5V, the dropout voltage is limited by the minimum input-voltage specification. See *Figure 16* for the dropout voltage as a function of the output current and for temperature, see *Figure 17*, which was measured in a typical application circuit.

5 The GND pin current is tested with V_{IN} = $V_{OUT(NOMINAL)}$ and a current source load. Therefore, the device is tested while operating in dropout, which is the worst-case GND pin current. The GND pin current decreases at higher input voltages. Note that the GND pin current does not include SET pin or the ILIM pin current; however, quiescent current does include the SET and ILIM pins.

6 The SET and OUTS pins are clamped using diodes and two 25Ω series resistors. For less than 5ms transients, this clamp circuitry can carry more than the rated current. See the *Applications Information* for more information.

7 Adding a capacitor across the SET pin resistor decreases output voltage noise. Adding this capacitor bypasses the thermal noise of the resistor on the SET pin as well as the noise of the reference current. The output noise then equals the error-amplifier noise. Use of a SET pin bypass capacitor also increases the start-up time.

8 The RHP51000-CSL is tested and specified under pulsed load conditions such that $T_J \approx T_A$. The RHP51000-CSL is 100% tested at 25°C. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization, and correlation with statistical process controls. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

9 Parasitic diodes exist internally between the VIOC, ILIM, PG, PGFB, SET, OUTS, and OUT pins and the GND pin. Do not drive these pins more than 0.3V less than the GND pin during a fault condition. These pins must remain at a voltage more positive than GND during normal operation.

10 The current-limit programming scale factor is specified while the internal backup current limit is not active. Note that the internal current limit has foldback protection for $V_{IN} – V_{OUT}$ differentials greater than 12V.

11 The internal back-up current-limit circuitry incorporates foldback protection that decreases current limit for $V_{IN} – V_{OUT} > 12V$. Some level of output current is provided at all $V_{IN} – V_{OUT}$ differential voltages. See the *Typical Performance Characteristics* section for current limit vs. $V_{IN} – V_{OUT}$.

12 For output voltages less than 1V, the RHP51000-CSL requires a 10µA minimum load current for stability.

13 Maximum OUT-to-OUTS differential is guaranteed by design.

14 The VIOC buffer outputs a voltage equal to $V_{IN} – V_{OUT}$ or $V_{IN} – 1.5V$ for $V_{OUT} \leq 1.5V$. See *Block Diagram* and the *High-Efficiency Linear Regulator: Voltage Input-to-Output Control (VIOC)* section for further information. Set the source current of the VIOC pin between 10µA and 200µA.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
IN Pin Voltage	±22V
VIOC Pin Voltage[9]	–0.3V, 4V
EN/UV Pin Voltage	±22V
IN-to-EN/UV Differential	±22V
PG Pin Voltage[9]	–0.3V, 22V
ILIM Pin Voltage[9]	–0.3V, 1V
PGFB Pin Voltage[9]	–0.3V, 22V
SET Pin Voltage[9]	–0.3V, 16V
SET Pin Current[6]	±20mA
OUTS Pin Voltage[9]	–0.3V, 16V
OUTS Pin Current[6]	±20mA
OUT Pin Voltage[9]	–0.3V, 16V
OUT-to-OUTS Differential[13]	±1.2V
IN-to-OUT Differential	±22V
IN-to-OUTS Differential	±22V
Output Short-Circuit Duration	Indefinite
Operating Junction Temperature Range[8]	–40°C to 125°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10sec) MSE Package	300°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Outgas Testing

The criteria for the acceptance and rejection of materials must be determined by the user based on the specific component and system requirements. Historically, a total mass loss (TML) of 1.00% and collected volatile condensable material (CVCM) of 0.10% have been used as screening levels for rejecting spacecraft materials.

Table 3. Outgas Testing

SPECIFICATIONS (TESTED AS PER ASTM E595-15)	VALUE	UNIT
Total mass loss	0.04	%
Collected volatile condensable material	< 0.01	%
Water vapor recovered	0.02	%

Radiation Features

Table 4. Radiation Features

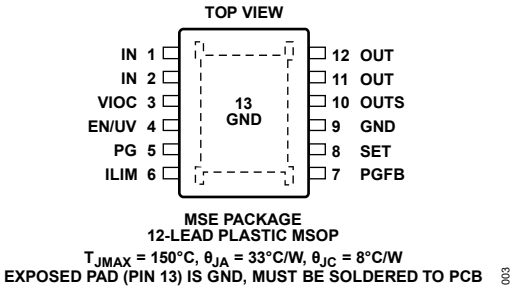
SPECIFICATIONS	VALUE	UNIT
Maximum total dose available (Dose rate = 50rad(Si)/sec to 300rad(Si)/sec)[1]	50	krad(Si)
Maximum total dose available (Dose rate = 10mrad(Si)/sec to 100mrad(Si)/sec)[1, 2]	10	krad(Si)
No SEL occurs at effective linear energy transfer (LET)[3]	79.9	MeV·cm2/mg

[1] Guaranteed by device and process characterization. A radiation report is available on the RHP51000-CSL product web page.

[2] Parametric shift at EN hysteresis post-irradiation. Post-irradiation testing and 24-hr anneal failures recovered through accelerated annealing at 100°C ±5°C, 168hrs.

[3] Limits are characterized at initial qualification and after any design or process changes specified by the customer through the purchase order or contract. If applying an input voltage > 16V, mitigation must be used to avoid SEL. A radiation report is available on the RHP51000-CSL product web page. Contact Analog Devices for further data beyond the report published on the web page.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Pin Descriptions

Table 5. Pin Descriptions

PIN	NAME	DESCRIPTION
1, 2	IN	Input. The IN pins supply power to the regulator. The RHP51000-CSL requires a bypass capacitor at the IN pin. In general, the output impedance of a battery rises with frequency; therefore, it is best practice to include a bypass capacitor in battery-powered applications. While a 4.7µF input bypass capacitor generally suffices, applications with large load transients can require higher input capacitance to prevent input supply droop. See the *Stability and Input Capacitance* and *PSRR and Input Capacitance* Applications Informationsections on the proper use of an input capacitor and its effect on circuit performance, in particularly PSRR. The RHP51000-CSL withstands reverse voltages on IN with respect to GND, OUTS, and OUT. In the case of a reversed input, which occurs if a battery is plugged-in backwards, the RHP51000-CSL acts as if a diode is in series with its input. Therefore, no reverse-current flows into the RHP51000-CSL, and no negative voltage appears at the load. The device protects itself and the load.
3	VIOC	Voltage for Input-to-Output Control. The RHP51000-CSL incorporates a tracking function to control the switching preregulator powering the RHP51000-CSL. The VIOC pin is the output of this tracking function that drives the feedback (FB) pin preregulator to maintain the input voltage of the RHP51000-CSL at V_{OUT} + V_{VIOC}. This function minimizes power dissipation while maintaining PSRR performance. See *High-Efficiency Linear Regulator: Voltage Input-to-Output Control (VIOC)* section for further details.
4	EN/UV	Enable/UVLO. Pulling the EN/UV pin low moves the RHP51000-CSL in shutdown mode. Quiescent current in shutdown mode drops to less than 1µA and the output voltage turns off. Alternatively, the EN/UV pin can set an input supply undervoltage lockout (UVLO) threshold by using a resistor divider between IN, EN/UV, and GND. The RHP51000-CSL typically turns on when the EN/UV voltage exceeds 1.24V on its rising edge, with a 130mV hysteresis on its falling edge. The EN/UV pin can be driven above the input voltage and maintain proper functionality. If unused, connect EN/UV to IN. Do not float the EN/UV pin.
5	PG	Power Good. PG is an open-collector flag that indicates output-voltage regulation. PG pulls low if PGFB is less than 300mV. If the power-good functionality is not needed, float the PG pin. A parasitic substrate diode exists between the PG and GND pins of the RHP51000-CSL; therefore, do not drive PG more than 0.3V less than GND during normal operation or during a fault condition.

PIN	NAME	DESCRIPTION
6	ILIM	Current-Limit Programming Pin. Connecting a resistor between ILIM and GND programs the current limit. For best accuracy, Kelvin connect this resistor directly to the GND pin of the RHP51000-CSL. The programming-scale factor is nominally 150mA × kΩ. The ILIM pin sources current proportional (1:500) to the output current. Therefore, ILIM also serves as a current-monitoring pin with a 0V to 300mV range. If the programmable current-limit functionality is not needed, connect ILIM to GND. A parasitic substrate diode exists between the ILIM and GND pins of the RHP51000-CSL; therefore, do not drive ILIM more than 0.3V less than GND during normal operation or during a fault condition.
7	PGFB	Power-Good Feedback. The PG pin pulls high if PGFB increases beyond 300mV on its rising edge, with 7mV hysteresis on its falling edge. Connecting an external resistor-divider between OUT, PGFB, and GND sets the programmable power-good threshold with the following transfer function: $0.3V \times (1 + R_{PG2}/R_{PG1})$. As discussed further in the *Fast Start-Up* section, PGFB also activates the fast start-up circuitry. Connect PGFB to IN if the power-good and fast start-up functions are not needed. In addition, if reverse-input protection is additionally required, connect the anode of a 1N4148 diode to IN and its cathode to PGFB. See *Figure 90* for further details. A parasitic-substrate diode exists between the PGFB and GND pins of the RHP51000-CSL; therefore, do not drive PGFB more than 0.3V less than GND during normal operation or during a fault condition.
8	SET	SET. The inverting input of the error amplifier and the regulation set-point for the RHP51000-CSL. SET sources a precision 100µA current that flows through an external resistor connected between SET and GND. The output voltage of the RHP51000-CSL is determined by $V_{SET} = I_{SET} \times R_{SET}$. The output voltage range is from 0V to 15V. Adding a capacitor from SET to GND improves noise, PSRR and transient response at the expense of an increased start-up time. For optimum load regulation, Kelvin connect the ground side of the SET pin resistor directly to the load. A parasitic-substrate diode exists between the SET and GND pins of the RHP51000-CSL; therefore, do not drive SET more than 0.3V less than GND during normal operation or during a fault condition.
9, Exposed Pad 13	GND	Ground. The exposed backside is an electrical connection to GND. To ensure proper electrical and thermal performance, solder the exposed backside to the PCB ground and connect it directly to the GND pin.
10	OUTS	Output Sense. The OUTS pin is the noninverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connect OUTS directly to the output capacitor and the load. In addition, connect the GND connections of the output capacitor and the SET pin capacitor directly together. A parasitic substrate diode exists between the OUTS and GND pins of the RHP51000-CSL; therefore, do not drive OUTS more than 0.3V less than GND during normal operation or during a fault condition.
11, 12	OUT	Output. These pins supply power to the load. For stability, use a minimum 10µF output capacitor with an ESR less than 20mΩ and an effective series inductance (ESL) of less than 2nH. Large load transients require larger output capacitance to limit peak voltage transients. See the *Stability and Output Capacitance* section for more information on output capacitance. A parasitic-substrate diode exists between the OUT and GND pins of the RHP51000-CSL; therefore, do not drive OUT more than 0.3V less than GND during normal operation or during a fault condition.

TYPICAL PERFORMANCE CHARACTERISTICS

(T_J = 25°C, unless otherwise noted.)

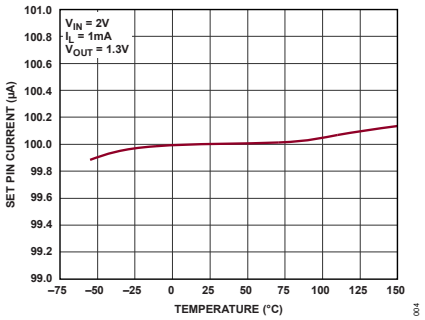


Figure 3. SET Pin Current vs. Temperature

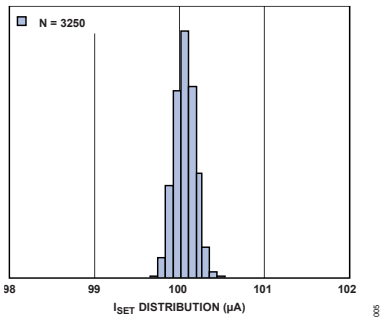


Figure 4. I_{SET} Distribution

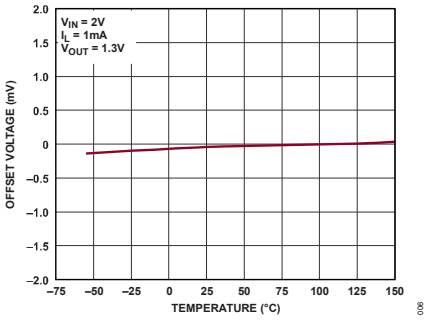


Figure 5. Offset Voltage (V_{OUT} – V_{SET}) vs. Temperature

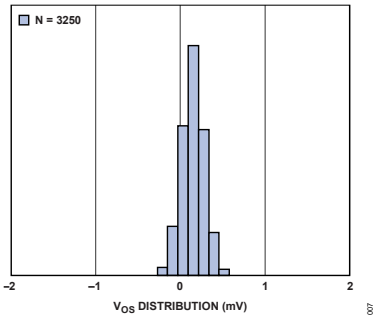


Figure 6. Offset Voltage (V_{OS}) Distribution

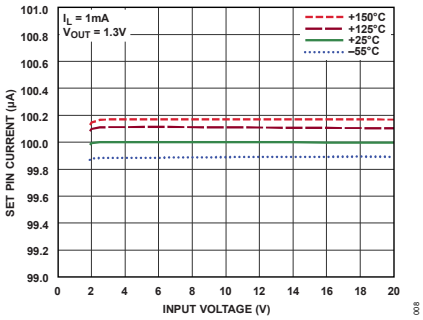


Figure 7. SET Pin Current vs. Input Voltage

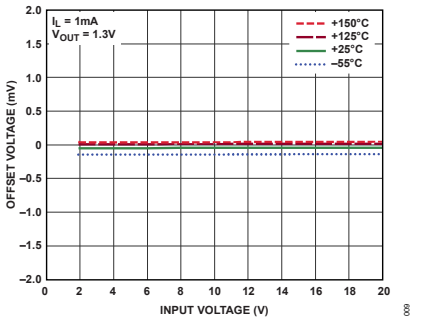


Figure 8. Offset Voltage (V_{OUT} – V_{SET}) vs. Input Voltage

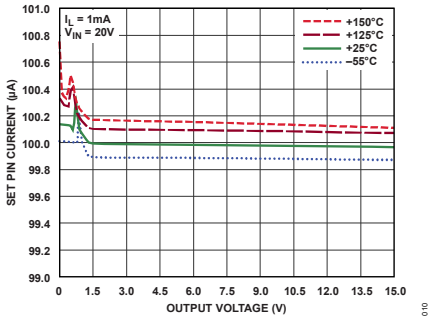


Figure 9. SET Pin Current vs. Output Voltage

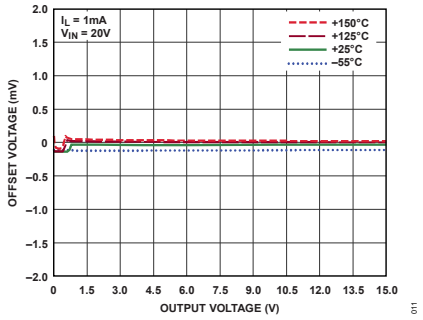


Figure 10. Offset Voltage (V_{OUT} – V_{SET}) vs. Output Voltage

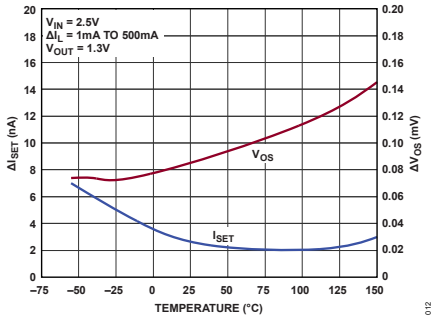


Figure 11. ΔI_{SET} and ΔV_{OS} Load Regulation vs. Temperature

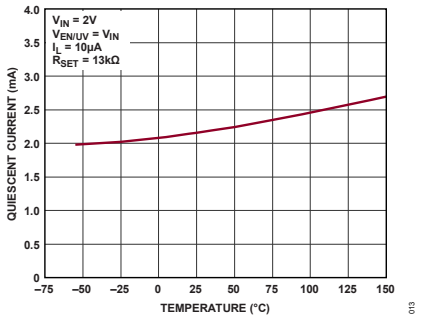


Figure 12. Quiescent Current vs. Temperature

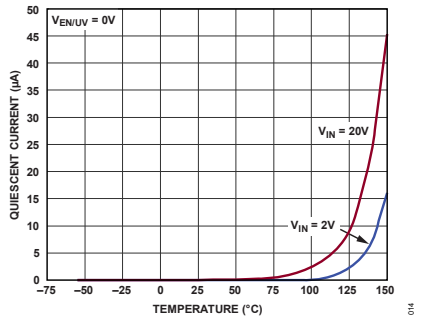


Figure 13. Quiescent Current vs. Temperature

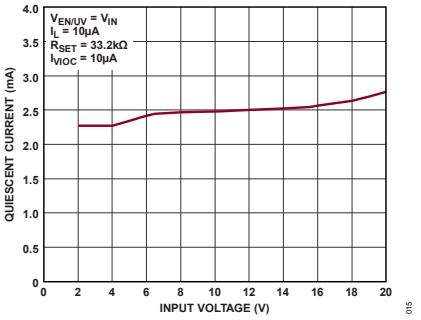


Figure 14. Quiescent Current vs. Input Voltage

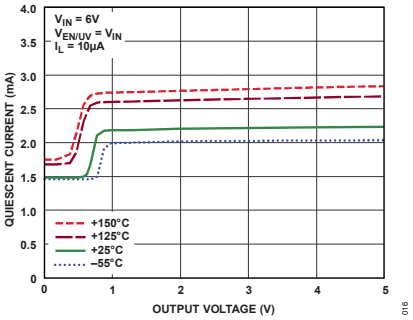


Figure 15. Quiescent Current vs. Output Current

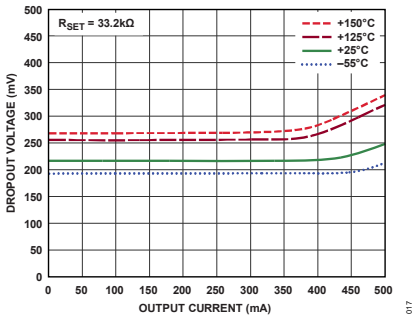


Figure 16. Dropout Voltage vs. Output Current

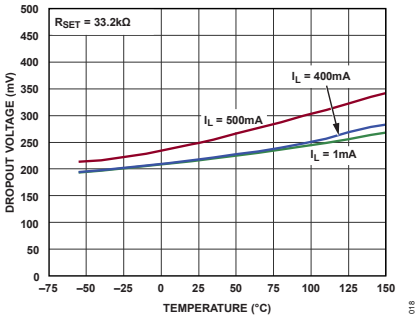


Figure 17. Dropout Voltage vs. Temperature

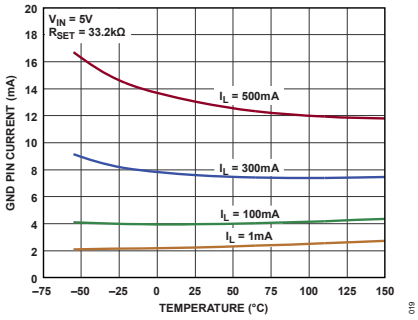


Figure 18. GND Pin Current vs. Temperature

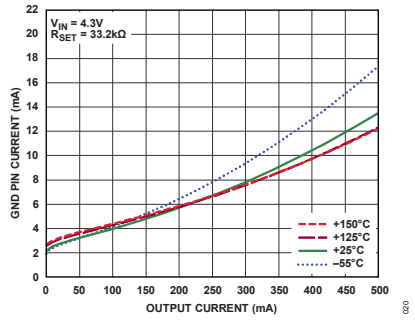


Figure 19. GND Pin Current vs. Output Current

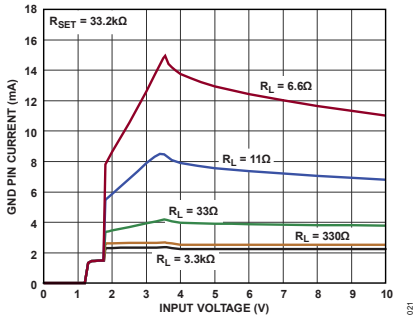


Figure 20. GND Pin Current vs. Input Voltage

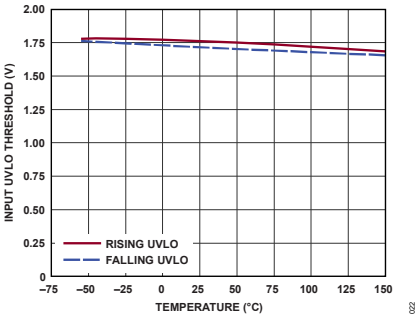


Figure 21. Input UVLO Threshold vs. Temperature

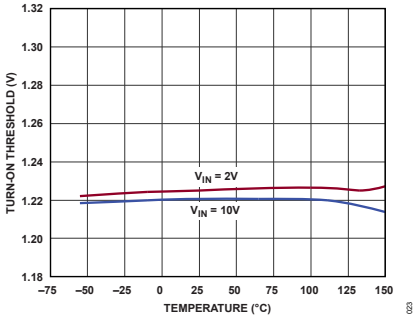


Figure 22. Turn-On Threshold vs. Temperature

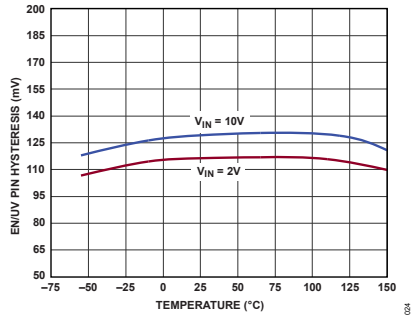


Figure 23. EN/UV Pin Hysteresis vs. Temperature

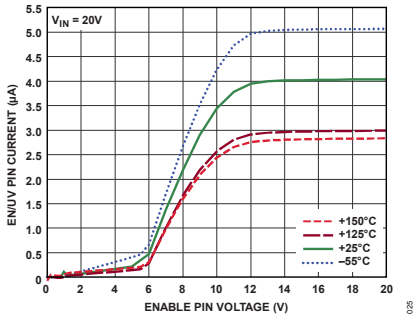


Figure 24. EN/UV Pin Current vs. Enable Pin Voltage

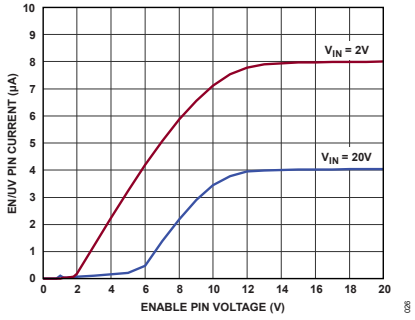


Figure 25. EN/UV Pin Current vs. Enable Pin Voltage

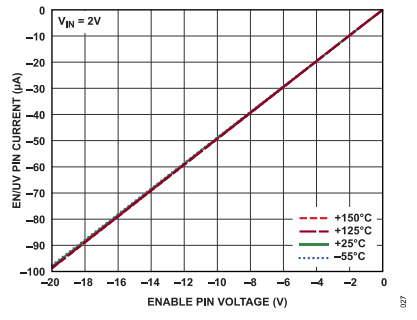


Figure 26. EN/UV Pin Current vs. Enable Pin Voltage

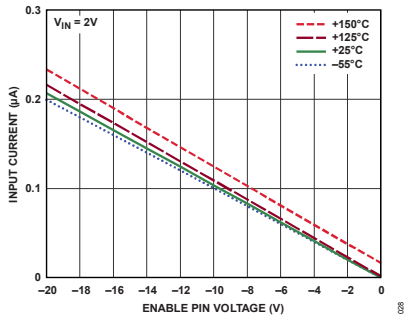


Figure 27. Input Pin Current vs. Enable Pin Voltage

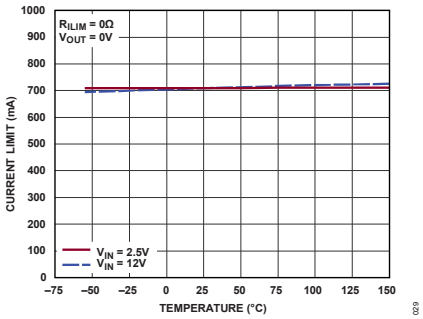


Figure 28. Current Limit vs. Temperature

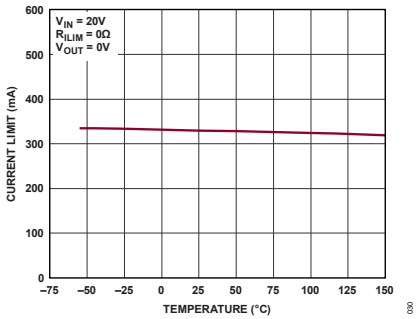


Figure 29. Current Limit vs. Temperature

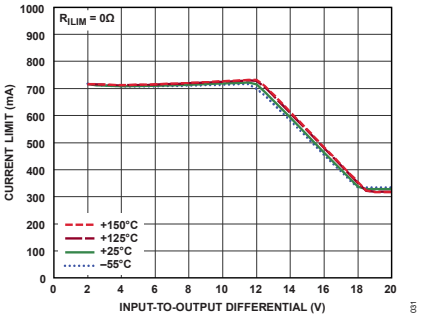


Figure 30. Current Limit vs. Input-to-Output Differential

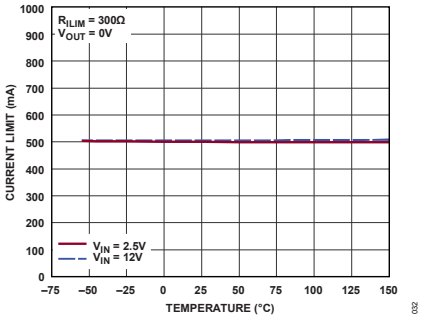


Figure 31. Current Limit vs. Temperature

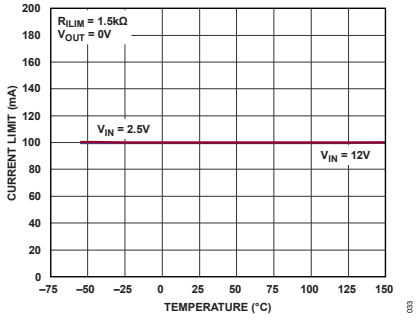


Figure 32. Current Limit vs. Temperature

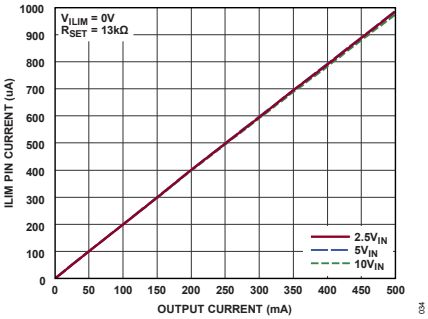


Figure 33. ILIM Pin Current vs. Output Current

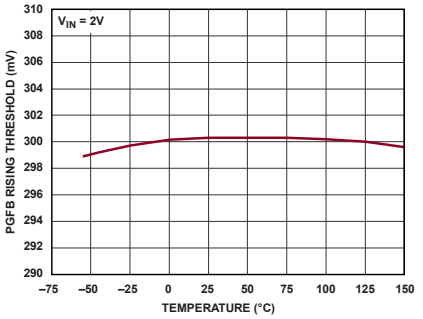


Figure 34. PGFB Rising Threshold vs. Temperature

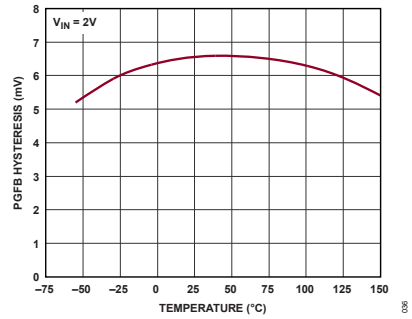


Figure 35. PGFB Hysteresis vs. Temperature

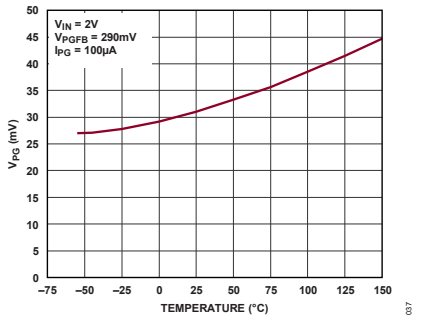


Figure 36. PG Output Low Voltage

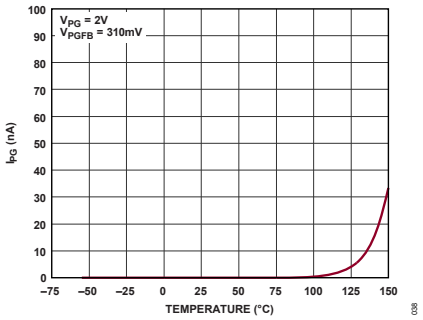


Figure 37. PG Pin Leakage Current

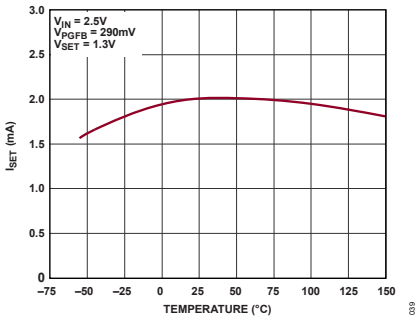


Figure 38. I_{SET} During Start-Up with Fast Start-Up Enabled vs. Temperature

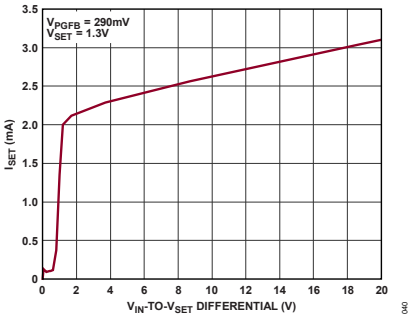


Figure 39. I_{SET} During Start-Up with Fast Start-Up Enabled

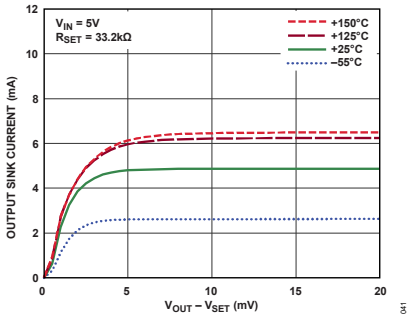


Figure 40. Output Overshoot Recovery Current Sink

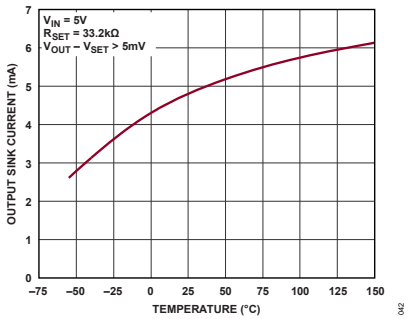


Figure 41. Output Overshoot Recovery Current Sink

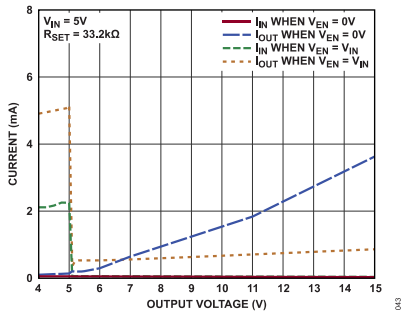


Figure 42. V_{OUT} Forced Above $V_{OUT(NOMINAL)}$

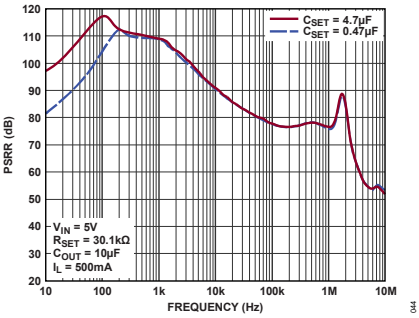


Figure 43. Power Supply Ripple Rejection

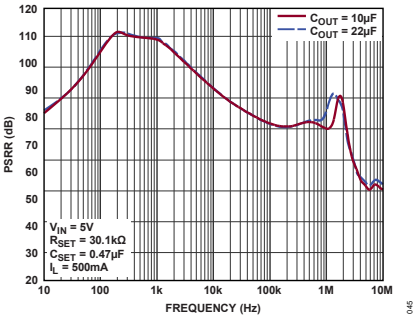


Figure 44. Power Supply Ripple Rejection

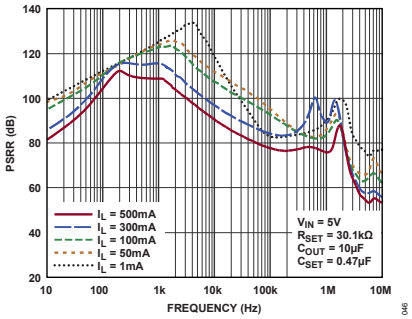


Figure 45. Power Supply Ripple Rejection

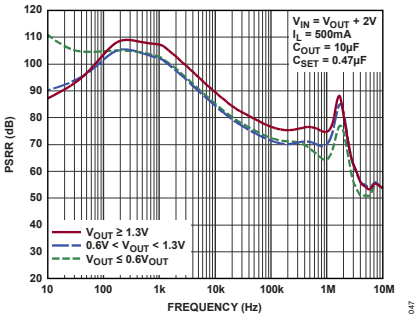


Figure 46. Power Supply Ripple Rejection as a Function of Error Amplifier Input Pair

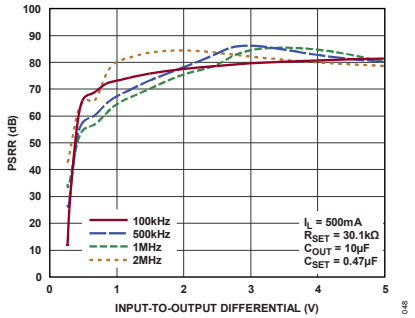


Figure 47. Power Supply Ripple Rejection

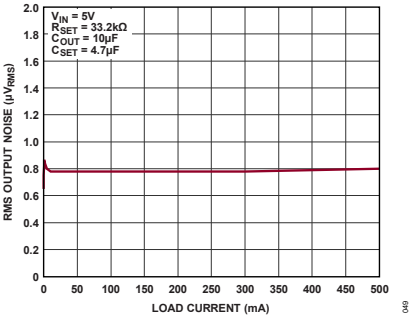


Figure 48. Integrated RMS Output Noise (10Hz to 100kHz) vs. Load Current

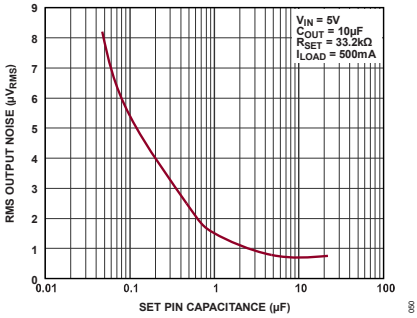


Figure 49. Integrated RMS Output Noise (10Hz to 100kHz) vs. SET Pin Capacitance

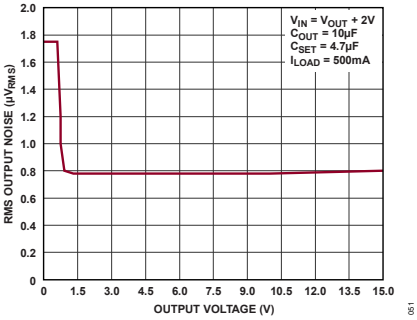


Figure 50. Integrated RMS Output Noise (10Hz to 100kHz) vs. Output Voltage

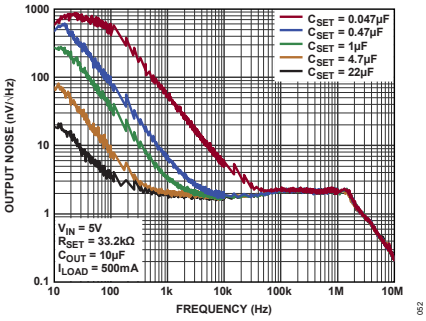


Figure 51. Output Noise vs. Frequency (C_{SET} Steps)

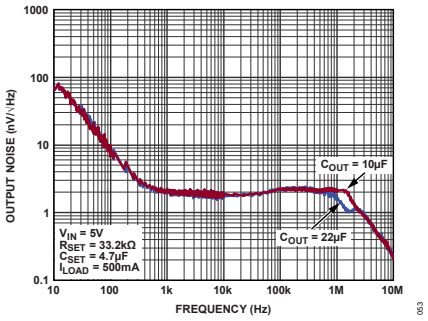


Figure 52. Output Noise vs. Frequency (C_{OUT} Steps)

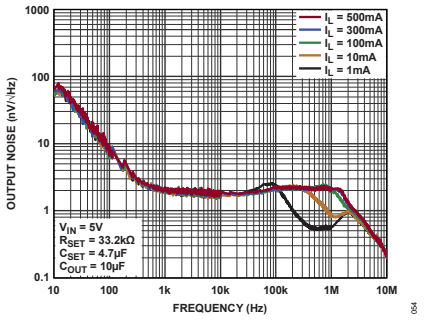


Figure 53. Output Noise vs. Frequency (I_L Steps)

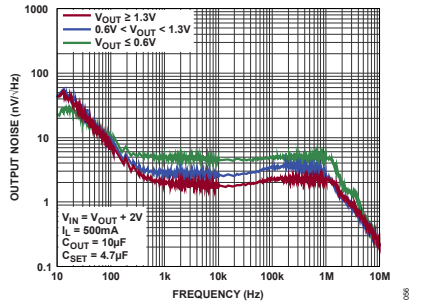


Figure 54. Noise Spectral Density as a Function of Error Amplifier Input Pair

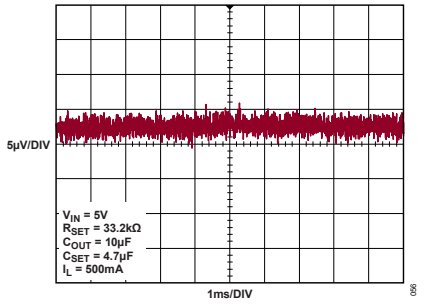


Figure 55. Output Noise: 10Hz to 100kHz

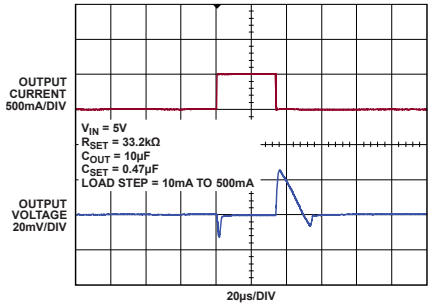


Figure 56. Load-Transient Response

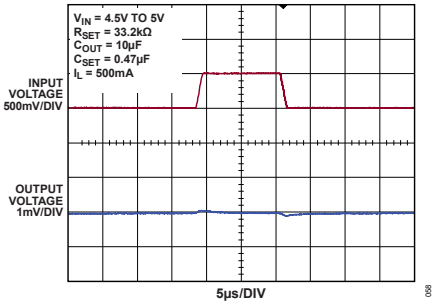


Figure 57. Line Transient Response

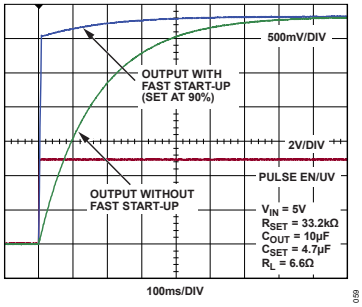


Figure 58. Start-Up Time with and without Fast Start-Up Circuitry for Large CSET

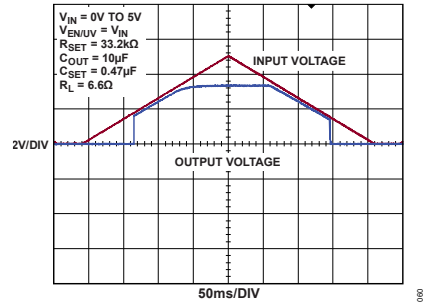


Figure 59. Input Supply Ramp-Up and Ramp-Down

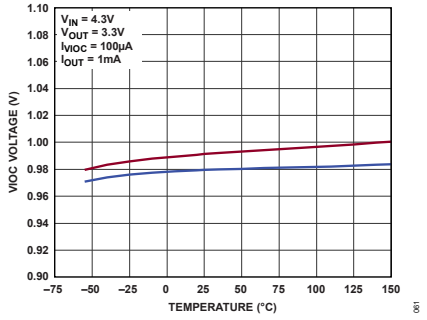


Figure 60. VIOC Voltage vs. Temperature

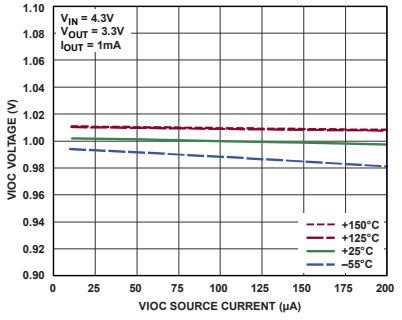


Figure 61. VIOC Voltage vs. VIOC Source Current

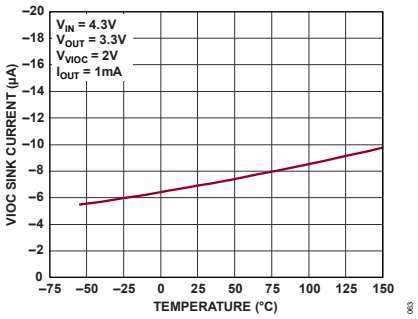


Figure 62. VIOC Sink Current vs. Temperature

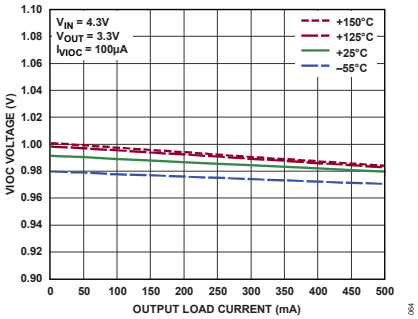
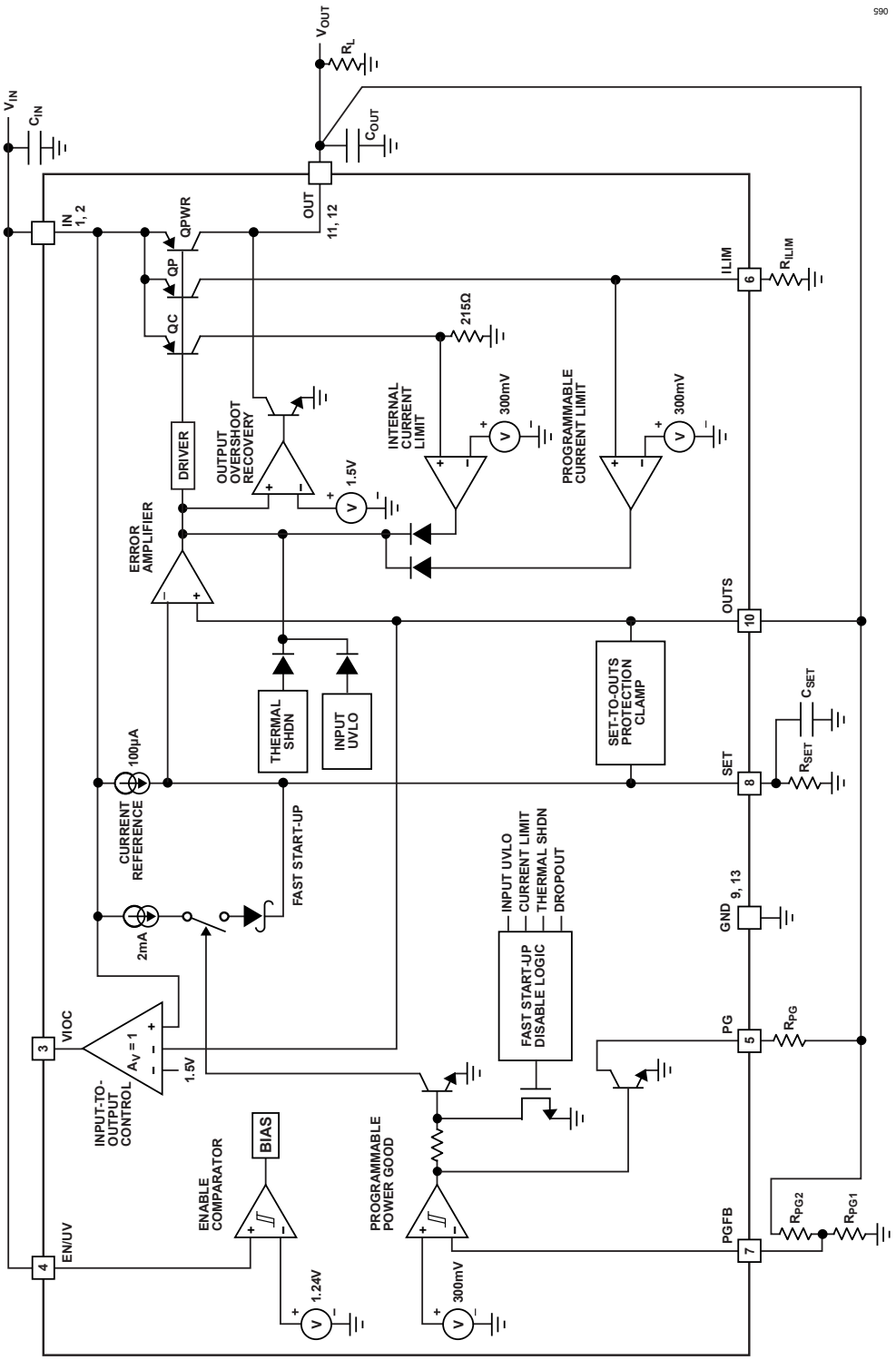


Figure 63. VIOC Voltage vs. Output Load Current (mA)

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The RHP51000-CSL is a high-performance, low-dropout, linear regulator featuring Analog Devices' ultra-low noise (2nV/√Hz at 10kHz) and ultra-high PSRR (76dB at 1MHz) architecture for powering noise-sensitive applications. Designed as a precision current source followed by a high-performance rail-to-rail voltage buffer, the RHP51000-CSL can be easily paralleled to further reduce noise, increase output current, and spread heat on the PCB. The device additionally features programmable current limit, fast start-up capability, and programmable power good.

The RHP51000-CSL is simple to use and incorporates all of the protection features expected in high-performance regulators. Included are short-circuit protection, safe-operating area protection, reverse-battery protection, reverse-current protection, and thermal shutdown with hysteresis.

The RHP51000-CSL incorporates a VIOC tracking function to control an upstream switching converter to maintain a constant voltage across the RHP51000-CSL, and therefore, to minimize power dissipation.

Output Voltage

The RHP51000-CSL incorporates a precision 100µA current source flowing out of the SET pin, which also connects to the inverting input of the error amplifier. *Figure 64* illustrates that connecting a resistor from SET to ground generates a reference voltage for the error amplifier. This reference voltage is the product of the SET pin current and the SET pin resistor. The unity-gain configuration of the error amplifier produces a low-impedance version of this voltage on its noninverting input, that is, the OUTS pin, which is externally connected to the OUT pin.

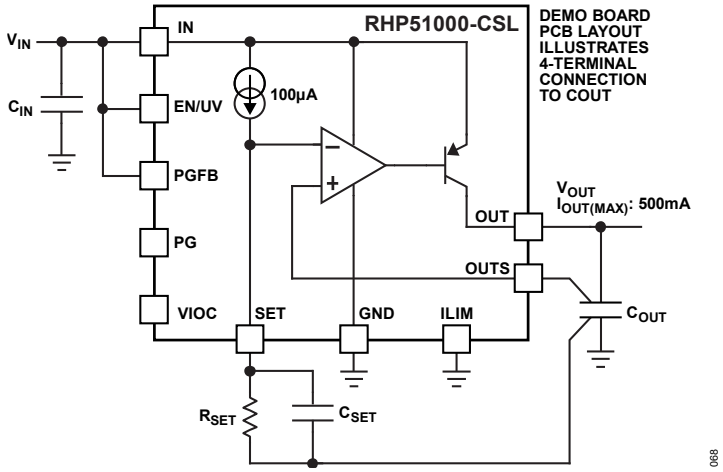


Figure 64. Basic Adjustable Regulator

The rail-to-rail error amplifier and current reference of the RHP51000-CSL allows for a wide output-voltage range from 0V (using a 0Ω resistor) to V_{IN} minus dropout, up to 15V. A PNP-based input pair is active for 0V to 0.6V output and an NPN-based input pair is active for output voltages greater than 1.3V, with a smooth transition between the two input pairs from 0.6V to 1.3V output. While the NPN-based input pair is designed to offer the best overall performance, see the *Electrical Characteristics* table for details on the offset voltage, SET pin current, output noise, and PSRR variation with the error-amplifier input pair. *Table 6* lists many common output voltages and their corresponding 1% R_{SET} resistors.

Table 6. 1% Resistor for Common Output Voltages

V_{OUT} (V)	R_{SET} (kΩ)
2.5	24.9
3.3	33.2
5	49.9
12	121
15	150

The benefit of using a current reference compared to the voltage reference used in conventional regulators is that the regulator always operates in a unity-gain configuration, independent of the programmed output voltage. This configuration allows the RHP51000-CSL to have loop gain, frequency response, and bandwidth independent of the output voltage. As a result, noise, PSRR, and transient performance do not change with output voltage. Moreover, because none of the error-amplifier gain is needed to amplify the SET pin voltage to a higher output voltage, output load regulation is more tightly specified in the hundreds of microvolts range and not as a fixed percentage of the output voltage.

Because the zero temperature-coefficient current source is highly accurate, the SET pin resistor can become a limiting factor in achieving high accuracy. Therefore, the SET pin resistor must be a precision resistor. Additionally, any leakage paths to or from the SET pin create errors in the output voltage. If necessary, use high-quality insulation (for example, Teflon™ or KEL-F®). Moreover, cleaning of all insulating surfaces to remove fluxes and other residues can be required. High humidity environments can require a surface coating at the SET pin to provide a moisture barrier.

Minimize board leakage by encircling the SET pin with a guard ring that operates at a potential close to itself, ideally connected to the OUT pins. Guarding both sides of the circuit board is recommended. Bulk leakage reduction depends on the guard-ring width. Leakages of 100nA into or out of the SET pin creates a 0.1% error in the reference voltage. Leakages of this magnitude, coupled with other sources of leakage, can cause significant errors in the output voltage, especially over a wide operating temperature range. *Figure 65* illustrates a typical guard-ring layout technique.

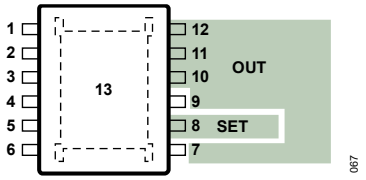


Figure 65. Guard-Ring Layout

Because the SET pin is a high-impedance node, unwanted signals can couple into the SET pin and cause erratic behavior, which is most noticeable when operating with a minimum output capacitor at heavy load currents. Bypassing the SET pin with a small capacitance to ground resolves this issue, 10nF is sufficient. For applications requiring higher accuracy or an adjustable output voltage, the SET pin can be actively driven by an external voltage source capable of sinking 100µA. Connecting a precision-voltage reference to the SET pin eliminates any errors present in the output voltage due to the reference current and SET pin resistor tolerances.

Output Sensing and Stability

The OUTS pin of the RHP51000-CSL provides a Kelvin-sense connection to the output. The GND side of the SET pin resistor provides a Kelvin-sense connection to the GND side of the load.

Additionally, for ultra-high PSRR, the RHP51000-CSL bandwidth is made quite high (~1MHz), making it close to the self-resonance frequency (~1.6MHz) of a typical 10µF (1206 case size), ceramic, output capacitor. Therefore, it is important to avoid adding extra impedance (ESR and ESL) outside the feedback loop. To that end, as shown in *Figure 66*, minimize the effects of PCB trace and solder inductance by connecting the OUTS pin directly to C_{OUT} and the GND side of C_{SET} directly to the GND side of C_{OUT}. Also keep the GND sides of C_{IN} and C_{OUT} reasonably close. Refer to the RHP51000-CSL demo board manual for more information on the recommended layout that meets these requirements. While the RHP51000-CSL is robust enough not to oscillate if the recommended layout is not followed, depending on the actual layout, phase and gain margin, noise, and PSRR performance can degrade.

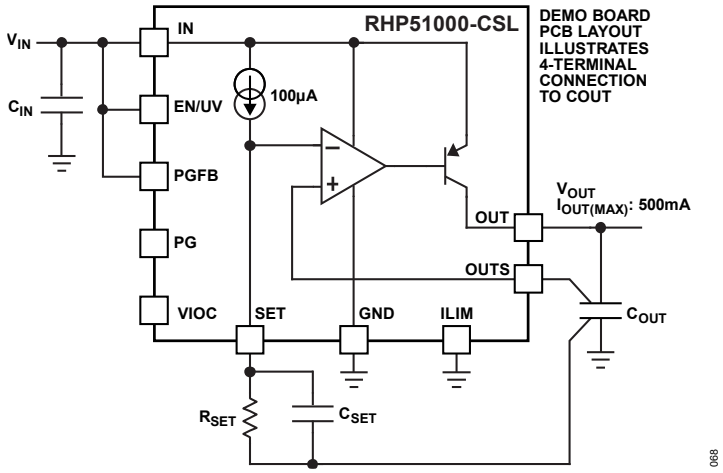


Figure 66. C_{OUT} and C_{SET} Connections for Best Performance

Stability and Output Capacitance

The RHP51000-CSL requires an output capacitor for stability. Given its high bandwidth, Analog Devices recommends low ESR and ESL ceramic capacitors. A minimum of 10µF output capacitance with an ESR of less than 20mΩ and an ESL of less than 2nH is required for stability.

Given the high PSRR and low-noise performance attained using a single 10µF ceramic-output capacitor, larger values of output capacitor only marginally improves the performance because the regulator bandwidth decreases with increasing output capacitance. Therefore, there is little to be gained by using larger than the minimum 10µF output capacitor. Moreover, larger values of output capacitance decreases peak-output deviations during a load transient. Note that bypass capacitors used to decouple individual components powered by the RHP51000-CSL increase the effective-output capacitance.

Consider the type of ceramic capacitors used. The capacitors are manufactured with a variety of dielectrics, each with different behaviors across temperature and applied voltage. The most common dielectrics used are specified with Electronic Industries Alliance (EIA) temperature characteristic codes of Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are good for providing high capacitance in small packages, but these dielectrics tend to have stronger voltage and temperature coefficients as shown in *Figure 67* and *Figure 68*. When used with a 5V regulator, a 16V, 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied over the operating temperature range.

X5R and X7R dielectrics result in more stable characteristics and are thus more suitable for the RHP51000-CSL. The X7R dielectric has better stability across temperature, while the X5R is less expensive and is available in higher values. Nonetheless, care must still be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and the maximum capacitance change over temperature. While capacitance

changes due to DC bias for X5R and X7R is better than Y5V and Z5U dielectrics, it can still be significant enough to drop capacitance below sufficient levels. As shown in *Figure 69*, capacitor DC bias characteristics tend to improve as component case size increases. However, verification of expected capacitance at the operating voltage is highly recommended. Due to its good voltage coefficient in small case sizes, Analog Devices recommends using the Murata GJ8 series ceramic capacitors.

High Vibration Environments

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to how a piezoelectric microphone works. For a ceramic capacitor, this stress can be induced by mechanical vibrations within the system or due to thermal transients.

RHP51000-CSL applications in high-vibration environments have three distinct, piezoelectric noise generators: ceramic output, input, and SET pin capacitors. However, due to the low output impedance over a wide frequency range of the RHP51000-CSL, negligible output noise is generated using a ceramic-output capacitor.

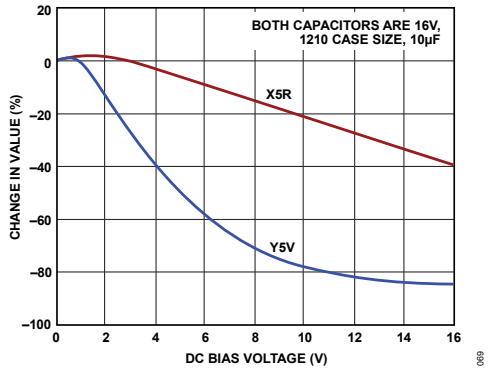


Figure 67. Ceramic Capacitor DC Bias Characteristics

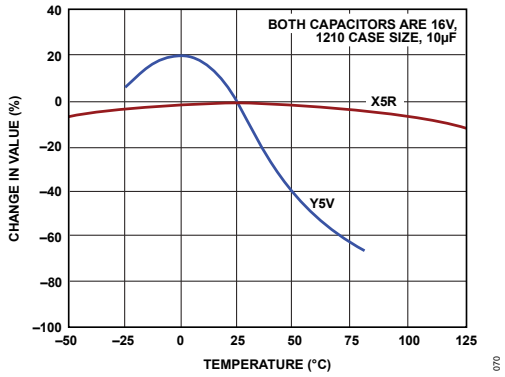


Figure 68. Ceramic Capacitor Temperature Characteristics

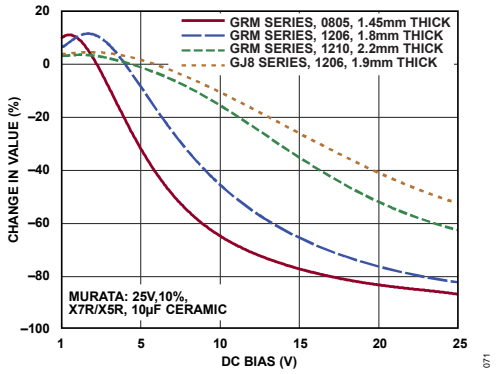


Figure 69. Capacitor Voltage Coefficient for Different Case Sizes

Similarly, due to the ultra-high PSRR of the RHP51000-CSL, negligible output noise is generated using a ceramic-input capacitor. Nonetheless, given the high SET pin impedance, any piezoelectric response from a ceramic SET pin capacitor generates significant output noise, peak-to-peak excursions of hundreds of µVs. However, due to the high ESR and ESL tolerance of the SET pin capacitor, any nonpiezoelectrically responsive (tantalum, electrolytic, or film) capacitor can be used at the SET pin, although electrolytic capacitors tend to have high 1/f noise. In any case, use of a surface-mount capacitor is highly recommended.

Stability and Input Capacitance

The RHP51000-CSL is stable with a minimum 4.7µF IN pin capacitor. Analog Devices recommends using low ESR ceramic capacitors. In cases where long wires connect the power supply to the input and ground terminals of the RHP51000-CSL, the use of low-value input capacitors combined with a large load current can result in instability. The resonant LC tank circuit formed by the wire inductance and the input capacitor is the cause of this instability and not the RHP51000-CSL.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. The wire diameter, however, has less influence on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire with a diameter of 0.26in is about half the inductance of a 30-AWG wire with a diameter of 0.01in. One foot of 30-AWG wire has 465nH of self-inductance.

Several methods exist to reduce the self-inductance of a wire. One method divides the current flowing toward the RHP51000-CSL between two parallel conductors. In this case, placing the wires further apart reduces the inductance; up to a 50% reduction when placed only a few inches apart. Splitting the wires connects two equal inductors in parallel. However, when placed in close proximity to each other, their mutual inductance adds to the overall self-inductance of the wires; therefore, a 50% reduction is not possible in such cases. The second and more effective technique to reduce the overall inductance is to place the forward and return current conductors (the input and ground wires) close. Two 30-AWG wires separated by 0.02in reduce the overall inductance to about one-fifth of a single wire.

If a battery mounted close powers the RHP51000-CSL, a 4.7µF input capacitor suffices for stability. However, if a distantly located supply powers the RHP51000-CSL, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 4.7µF minimum) per 6in of wire length. The minimum input capacitance required to stabilize the application also varies with the output capacitance as well as the load current. Place additional capacitance on the output of the RHP51000-CSL to help this issue. However, this method requires significantly more output capacitance compared to additional input bypassing. Series resistance between the supply and the input of the RHP51000-CSL also helps stabilize the application. As little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at

the expense of dropout voltage. A better alternative is to use a higher ESR tantalum or electrolytic capacitor at the input of the RHP51000-CSL in parallel with a 4.7µF ceramic capacitor.

PSRR and Input Capacitance

For applications using the RHP51000-CSL for post-regulating switching converters, placing a capacitor directly at the input of the RHP51000-CSL results in AC current (at the switching frequency) to flow near the RHP51000-CSL. This relatively high-frequency switching current generates a magnetic field that couples to the output of the RHP51000-CSL, degrading its effective PSRR. While highly dependent on the PCB, the switching preregulator, and the input capacitance, amongst other factors, the PSRR degradation can be easily more than 30dB at 1MHz. This degradation is present even if the RHP51000-CSL is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional, low PSRR, LDO regulators, the ultra-high PSRR of the RHP51000-CSL requires careful attention to higher order parasitics to extract the full performance offered by the regulator.

To mitigate the flow of the high-frequency switching current near the RHP51000-CSL, as long as the output capacitor of the switching converter is located more than an inch away from the LT3046, remove the input capacitor of the RHP51000-CSL. Magnetic coupling rapidly decreases with increasing distance. Nonetheless, if the switching preregulator is placed too far away (conservatively more than a couple inches) from the RHP51000-CSL, with no input capacitor present, as with any regulator, the input of the RHP51000-CSL oscillates at the parasitic LC resonance frequency. In addition, it is generally a common (and a preferred) practice to bypass regulator input with some capacitance. Therefore, this option is fairly limited in its scope and not the optimal solution.

To that end, Analog Devices recommends using the RHP51000-CSL demo board layout for achieving the best possible PSRR performance. The RHP51000-CSL demo board layout uses magnetic-field cancellation techniques to prevent PSRR degradation caused by this high-frequency current flow, while using the input capacitor.

Filtering High-Frequency Spikes

For applications where the RHP51000-CSL is used to post regulate a switching converter, its high PSRR effectively suppresses any noise present at the switching frequency of the switching converter, typically 100kHz to 4MHz. However, the high-frequency (hundreds of MHz) spikes, beyond the bandwidth of the RHP51000-CSL, associated with the power-switch transition times of the switching converter almost directly pass through the RHP51000-CSL. While the output capacitor is intended partly to absorb these spikes, its ESL limits its ability at these frequencies. A ferrite bead or even the inductance associated with a short (for example, 0.5in) PCB trace between the output of the switching converter and the input of the RHP51000-CSL can serve as an LC filter to suppress these high-frequency spikes.

Output Noise

The RHP51000-CSL offers many advantages with respect to noise performance. Traditional linear regulators have several sources of noise. The most critical noise sources for a traditional regulator are its voltage reference, error amplifier, noise from the resistor-divider network used for setting the output voltage, and the noise gain created by this resistor-divider. Many low-noise regulators pin out their voltage reference to allow for noise reduction by bypassing the reference voltage.

Unlike most linear regulators, the RHP51000-CSL does not use a voltage reference. Instead, the RHP51000-CSL uses a 100µA current reference. The current reference operates with a typical noise-current level of 20pA/√Hz (6nA$_{RMS}$ over a 10Hz to 100kHz bandwidth). The resultant voltage noise equals the current noise multiplied by the resistor value, which, in turn, is RMS summed with the noise of the error amplifier and the own noise of resistor, √4kTR, whereby k = Boltzmann constant (1.38×10^{-23}J/K), and T is the absolute temperature.

One problem that conventional linear regulators face is that the resistor-divider setting the output voltage gains up the reference noise. In contrast, the unity-gain follower architecture of the RHP51000-CSL presents no gain from the SET pin to the output. Therefore, if a capacitor bypasses the SET pin resistor, the output noise is independent of the programmed output voltage. The resultant output noise is then set only by the noise of the error amplifier, typically 2nV/√Hz from a 10kHz to 1MHz bandwidth and 0.8μV_{RMS} from a 10Hz to 100kHz bandwidth using a 4.7μF SET pin capacitor. Paralleling multiple RHP51000-CSL devices further reduces noise by √N, for N parallel regulators.

See *Figure 48*, *Figure 49*, *Figure 50*, *Figure 51*, *Figure 52*, *Figure 53*, and *Figure 54* for the noise spectral density and RMS integrated noise over various load currents and SET pin capacitance information.

Set Pin (Bypass) Capacitance: Noise, PSRR, Transient Response, and Soft-Start

In addition to reducing output noise, using a SET pin bypass capacitor also improves PSRR and transient performance. Note that any bypass-capacitor leakage deteriorates the DC regulation of the RHP51000-CSL. Capacitor leakage of even 100nA is a 0.1% DC error. Therefore, Analog Devices recommends the use of a good quality, low-leakage ceramic capacitor.

Using a SET pin bypass capacitor also soft starts the output and limits inrush current. The RC time constant, formed by the SET pin resistor and capacitor, controls soft-start time. The ramp-up rate from 0% to 90% of nominal V_{OUT} is the following:

$$t_{SS} \approx 2.3 \times R_{SET} \times C_{SET} \text{ (Fast Start-up Disabled)}$$

Fast Start-Up

For ultra-low noise applications that require low 1/f noise (that is, at frequencies below 100Hz), a larger value, SET pin capacitor of up to 22μF is required. Typically, this larger value significantly increases the start-up time of the regulator. However, the RHP51000-CSL incorporates fast start-up circuitry that increases the SET pin current to approximately 2mA during start-up.

As shown in the *Block Diagram*, the 2mA current source remains engaged while PGFB is less than 300mV, unless the regulator is in current limit, dropout, thermal shutdown, or the input voltage is less than the minimum V_{IN}.

If the fast start-up capability is not used, connect PGFB to IN or to OUT for output voltages more than 300mV and note that this also disables the power-good functionality.

ENABLE/UVLO

The EN/UV pin is used to put the regulator into a micropower shutdown state. The RHP51000-CSL has an accurate 1.24V turn-on threshold on the EN/UV pin with 130mV of hysteresis. This threshold can be used with a resistor-divider from the input supply to define an accurate UVLO threshold for the regulator. The EN/UV pin current (I_{EN}) at the threshold from the *Electrical Characteristics* table must be considered when calculating the resistor-divider network as follows:

$$V_{IN(UVLO)} = 1.24V \times \left(1 + \frac{R_{EN2}}{R_{EN1}}\right) + I_{EN} \times R_{EN2}$$

The EN/UV pin current (I_{EN}) can be ignored if R_{EN1} is less than 100k. If unused, connect the EN/UV pin to IN.

Programmable Power Good

As illustrated in the *Block Diagram*, power-good threshold is user programmable using the ratio of two external resistors, R_{PG2} and R_{PG1}:

$$V_{OUT(PG\_THRESHOLD)} = 0.3V \times \left(1 + \frac{R_{PG2}}{R_{PG1}}\right) + I_{PGFB} \times R_{PG2}$$

If the PGFB pin increases to more than 300mV, the open-collector PG pin deasserts and becomes high impedance. The power-good comparator has 7mV hysteresis and 5µs of deglitching. The PGFB pin current (I_{PGFB}) from the *Electrical Characteristics* table must be considered when determining the resistor-divider network. The PGFB pin current can be ignored if R_{PG1} is less than 30kΩ. If the power-good functionality is not used, float the PG pin. Note that programmable power good and fast start-up capabilities are disabled for output voltages less than 300mV.

Externally Programmable Current Limit

The current-limit threshold of the ILIM pin is 300mV. Connecting a resistor from ILIM to GND sets the maximum current flowing out of the ILIM pin, which, in turn, programs the current limit of the RHP51000-CSL. With a 150mA × kΩ programming scale factor, calculate the current limit as follows:

$$\text{Current Limit} = \frac{150mA \times k\Omega}{R_{ILIM}}$$

For example, a 1kΩ resistor programs the current limit to 150mA and a 2kΩ resistor programs the current limit to 75mA. For accuracy, Kelvin connect this resistor to the GND pin of the RHP51000-CSL.

When the IN-to-OUT differential is greater than 12V, the foldback circuitry of the RHP51000-CSL decreases the internal current limit. As a result, the internal current limit can override the externally programmed current-limit level to keep the RHP51000-CSL within its safe-operating area (SOA). See *Figure 30* .

As shown in the *Block Diagram*, the ILIM pin sources current proportional (1:500) to the output current; therefore, it also serves as a current-monitoring pin with a 0V to 300mV range. If external current limit or current monitoring is not used, connect ILIM to GND.

Output Overshoot Recovery

During a load-step change from full load to no load (or light load), the output voltage overshoots before the regulator responds to turn the power transistor off. Given that there is no load (or a light load) present at the output, it takes a long time to discharge the output capacitor.

As illustrated in the *Block Diagram*, the RHP51000-CSL incorporates overshoot recovery circuitry that turns on a current sink to discharge the output capacitor in the event OUTS is higher than SET. This current is typically approximately 4mA. No load recovery is disabled for input voltages less than 2.5V or output voltages less than 1.5V.

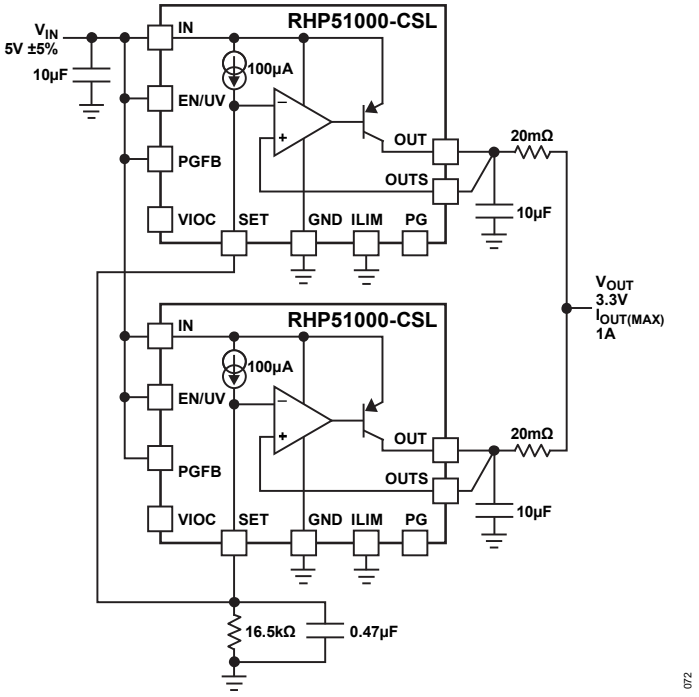


Figure 70. Parallel Devices

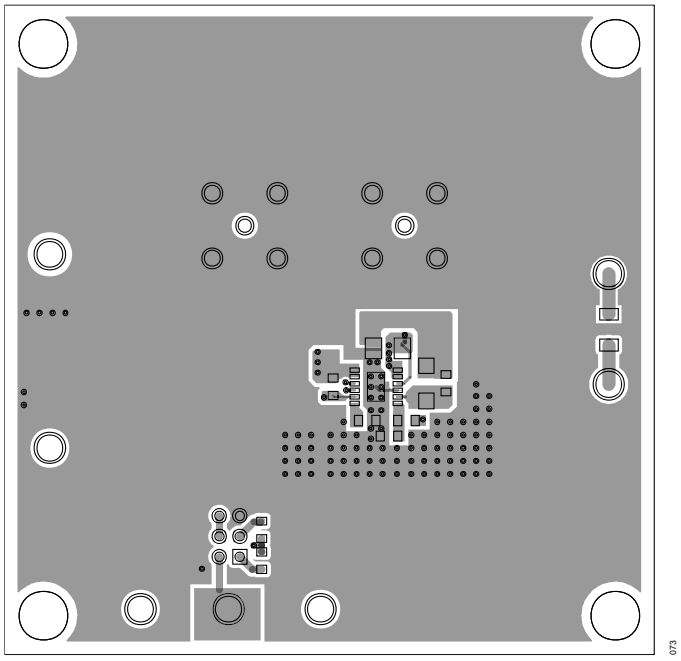


Figure 71. Recommended Layout

If OUTS is externally held more than SET, the current sink turns on in an attempt to restore OUTS to its programmed voltage. The current sink remains on until the external circuitry releases OUTS.

Direct Paralleling for Higher Current

Higher output current is obtained by paralleling multiple RHP51000-CSL devices. Connect all SET pins together and all IN pins together. Connect the OUT pins together using small pieces of PCB trace (used as a ballast resistor) to equalize currents in the RHP51000-CSL devices. PCB trace resistance in milliohms per inch is shown in *Table 7*.

Table 7. PC Board Trace Resistance (Measured in mΩ per inch)

WEIGHT (oz)	10mil WIDTH	20mil WIDTH
1	54.3	27.1
2	27.1	13.6

The small worst-case offset of 2mV for each paralleled RHP51000-CSL minimizes the required ballast resistor value. *Figure 70* illustrates that two RHP51000-CSL devices, each using a 20mΩ PCB trace ballast resistor, providing better than 20% accurate output current sharing at full load. The two 20mΩ external resistors only add 10mV of output regulation drop with a 1A maximum current. With a 3.3V output, this voltage drop only adds 0.3% to the regulation accuracy. Connect the OUTS pin directly to the output capacitor.

In addition, more than two RHP51000-CSL devices can be paralleled for even higher output current and lower output noise. Paralleling multiple RHP51000-CSL devices is also useful for distributing heat on the PCB. For applications with high input-to-output voltage differential, an input series resistor or resistor in parallel with the RHP51000-CSL can also be used to spread heat.

PCB Layout Considerations

Given the high bandwidth and ultra-high PSRR of the RHP51000-CSL, careful PCB layout must be employed to achieve full device performance. *Figure 71* shows a recommended layout that delivers full performance of the regulator. Refer to the RHP51000-CSL demo board manual for further details.

High-Efficiency Linear Regulator: Voltage Input-to-Output Control (VIOC)

The VIOC pin controls an upstream switching converter (for example, buck, boost, or buck-boost) to maintain a constant voltage across the RHP51000-CSL, regardless of the output voltage of the LDO regulator. This constant voltage maximizes efficiency while maintaining PSRR performance. The VIOC pin is the output of a fast unity-gain amplifier that measures the difference between IN and OUT or 1.5V, whichever is higher. As shown in *Figure 72*, the VIOC feature is simple to use. Connect the VIOC pin to the feedback (FB) pin of the upstream switching converter, which regulates the input-to-output differential of the RHP51000-CSL to the feedback voltage of the switching converter. When paralleling multiple RHP51000-CSL devices, connect the VIOC pin of one of the RHP51000-CSL devices to the feedback pin of the upstream switching converter and float the remaining VIOC pins.

While the VIOC buffer is inside the feedback loop of the switching converter, given the high bandwidth of the VIOC buffer, the frequency compensation of the switching converter does not require adjustment. Phase delay through the VIOC buffer is typically less than 2° at frequencies up to 100kHz; therefore, within the bandwidth (usually much less than 100kHz) of the switching converter, the VIOC buffer remains transparent and acts like an ideal wire.

For example, for a switching converter with less than 100kHz bandwidth and a phase margin of 50°, using the VIOC buffer causes the phase margin to degrade by at most 2°. Therefore, the phase margin for the switching converter (using the VIOC pin) is at least 48°. Given that the VIOC buffer is inside the feedback loop of the switching converter, the total capacitance on the VIOC pin must be less than 20pF.

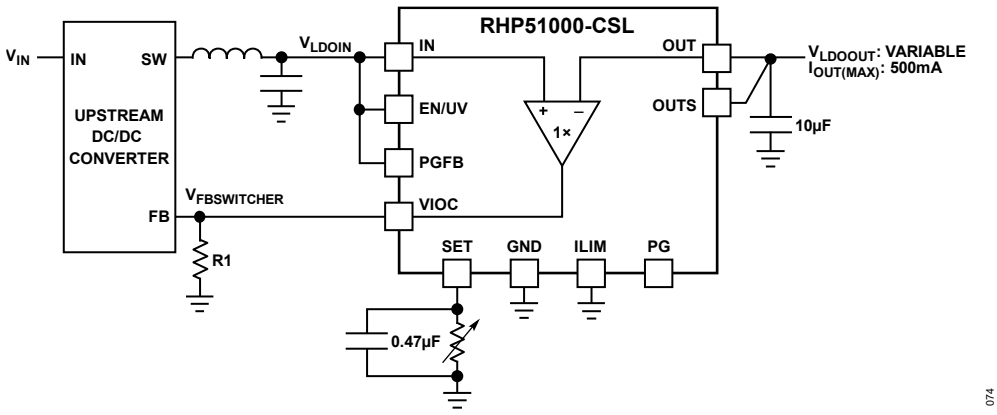


Figure 72. VIOC Basic Operation

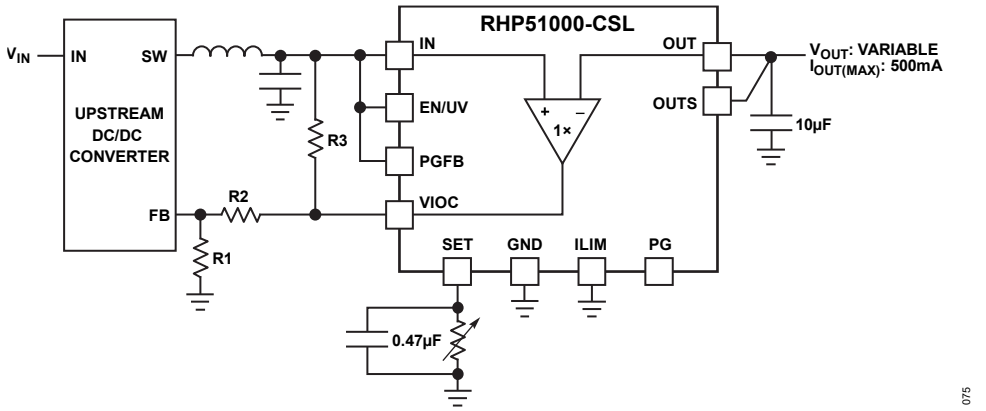


Figure 73. Programming Input-to-Output Differential

As shown in *Figure 73*, the input-to-output differential voltage is easily programmable to support different application needs (PSRR vs. power dissipation) by using the following equation:

$$V_{LDOIN} - V_{LDOOUT} = V_{VIOC} = V_{FBSWITCHER} \times \frac{R1 + R2}{R1}$$

where:

R1 is the resistance from the switching converter FB pin to ground.
R2 is the resistance from the switching converter FB pin to the VIOC pin.

Furthermore, in the event that the RHP51000-CSL SET pin opens up, the RHP51000-CSL input voltage can rise up to the input voltage of the switching converter, and thus, potentially violate the *Absolute Maximum Ratings* of the RHP51000-CSL. To prevent this violation, set the maximum RHP51000-CSL input voltage by using a resistor (R3) between the VIOC and IN pins of the regulator such that:

$$V_{(MAX)LDOIN} = V_{FBSWITCHER} \times \frac{R1 + R2 + R3}{R1} + I_{SINK} \times R3$$

where I_{SINK} is the sink current.

Moreover, the VIOC pin is capable of sourcing 200µA and sinking 15µA of current. To mitigate the effect of the sink current on the maximum LDO input voltage, choose R1 such that the resistor-divider typically runs at least 100µA.

For V_{OUT} > 1.5V, V_{IN} = V_{OUT} + V_{VIOC}. The VIOC pin voltage (and therefore, the input-to-output differential) can be programmed anywhere between a minimum of 1V and a maximum of 4V or V_{OUT} – 0.5V (for V_{OUT} > 1.5V), or whichever is lower. For applications where the feedback pin of the switching regulator is less than 1V, use the R1 and R2 resistors to make sure that the VIOC pin is within the previously mentioned range. Note that the VIOC pin voltage cannot be programmed to less than the feedback pin of the upstream switching converter. For V_{OUT} ≤ 1.5V, the VIOC programming range is 1V ±5%. If VIOC is set outside of this range, the input voltage of the RHP51000-CSL rises to the maximum value set using R3. If VIOC functionality is not used, float the VIOC pin.

Because the maximum VIOC programming voltage is dependent on V_{OUT}, care must be taken in setting the VIOC voltage. For instance, if VIOC is set to 1V, the IN-to-OUT differential of the LDO regulates to 1V for V_{OUT} > 1.5V. Similarly, if VIOC is set to 2V, the IN-to-OUT differential of the regulator regulates to 2V for V_{OUT} > 2.5V (that is, V_{VIOC} + 0.5V). However, if the output voltage is less than 2.5V, for this example, the LDO regulator is not able to drive its VIOC pin to the right level of 2V. As a result, the output of the upstream preregulator rises, causing the input voltage of the RHP51000-CSL to rise to the maximum voltage set using R3. Therefore, for protection under various fault conditions, the use of R3 to set the maximum V_{IN} voltage (less than 20V) is required.

Typical VIOC Application

Figure 74 shows a typical VIOC application used to post regulate the output of the step-down regulator. The VIOC voltage is set at 1V with the maximum LDO input voltage set to 16.5V. *Figure 75* shows the input and output voltage of the LDO regulator when pulsing the EN/UV pin of the RHP51000-CSL, and as can be seen, when the LDO regulator is disabled, the LDO input voltage goes to the maximum input voltage set by the resistor-divider on the VIOC pin. *Figure 76* shows the load-step response of the step-down regulator using the VIOC buffer. *Figure 77* shows the input and output-voltage response of the LDO regulator to stepping the SET pin from 3V to 4V. *Figure 78* shows the output and input voltage of the LDO regulator while ramping the SET pin from 0V to 10V, and as can be seen, the output voltage of the step-down regulator tracks the output voltage of the RHP51000-CSL when it is greater than 1.5V. Lastly, *Figure 79* shows the noise spectral density at the input and output of the RHP51000-CSL.

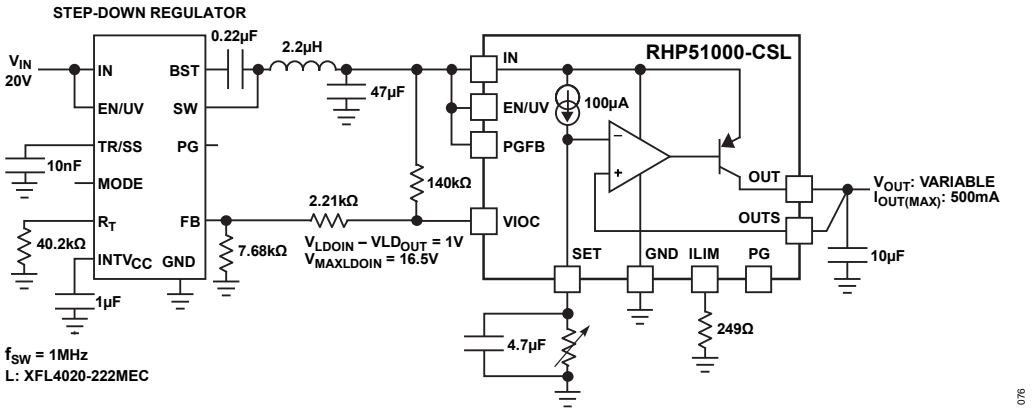


Figure 74. Typical RHP51000-CSL Post-Regulating Application

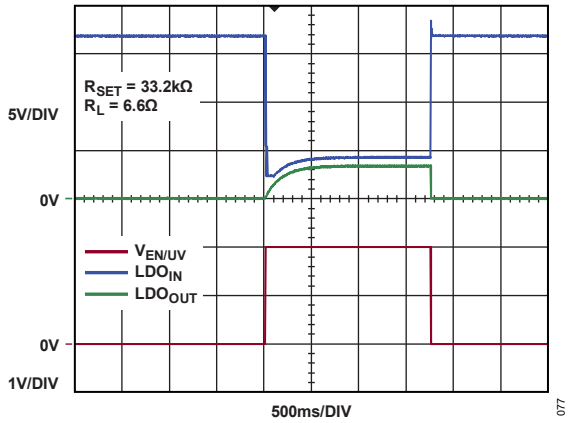


Figure 75. RHP51000-CSL EN/UV Pulse

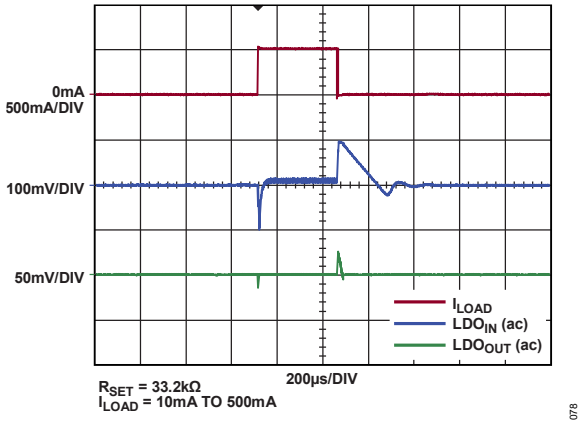


Figure 76. Load-Step Response Using the VIOC Buffer

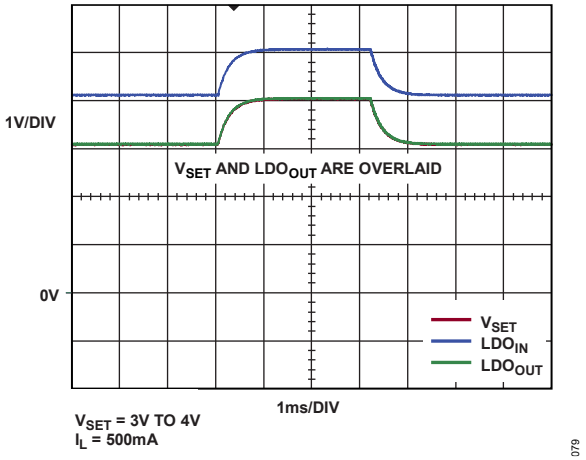


Figure 77. Stepping V_{SET} from 3V to 4V (and Back to 3V)

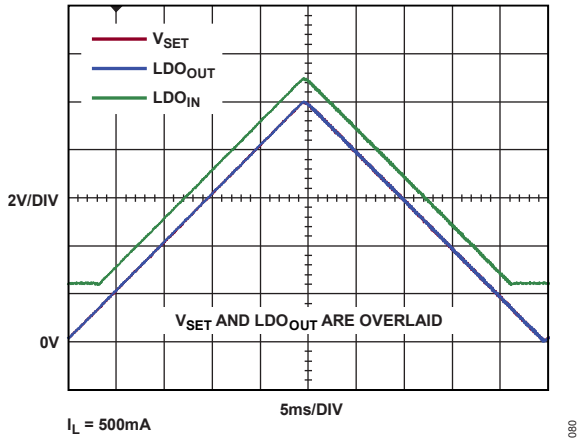


Figure 78. Ramping V_{SET} from 0V to 10V (and Back to 0V)

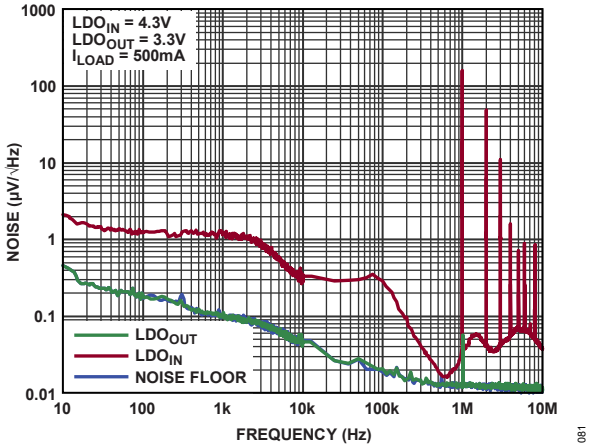


Figure 79. Input and Output Noise Spectral Density of the RHP51000-CSL

Thermal Considerations

The RHP51000-CSL has internal power and thermal limiting circuits that protect the device under overload conditions. The thermal shutdown temperature is nominally 165°C with about 8°C of hysteresis. For continuous normal load conditions, do not exceed the maximum junction temperature, 125°C. It is important to consider all sources of thermal resistance from junction to ambient, which includes junction to case, case to heatsink interface, heatsink resistance, or circuit board to ambient as the application dictates. Additionally, consider all heat sources close to the RHP51000-CSL.

The underside of the device package has exposed metal from the lead frame to the die attachment. This package allows heat to directly transfer from the die junction to the PCB metal to limit maximum operating junction temperature. The dual, inline pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of the PCB.

For surface-mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PCB and its copper traces. Copper board stiffeners and plated throughholes can also be used to spread the heat generated by the regulator.

Table 8 lists the thermal resistance as a function of the copper area on a fixed board size. All measurements were taken in still air on a 4-layer FR4 board with 1oz solid internal planes and 2oz top and bottom planes with a total board thickness of 1.6mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout, and thermal vias affect the resultant thermal resistance. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD51, JESD51-7, and JESD51-12. Achieving low thermal resistance necessitates careful PCB layout.

Table 8. Measured Thermal Resistance for MSOP Package

COPPER AREA		BOARD AREA (mm^2)	THERMAL RESISTANCE
TOP SIDE[1] (mm^2)	BOTTOM SIDE (mm^2)		
2500	2500	2500	33°C/W
1000	2500	2500	33°C/W
225	2500	2500	34°C/W
100	2500	2500	35°C/W

[1] Device is mounted on the top side.

Calculating Junction Temperature

For example, given an output voltage of 3.3V, an input voltage of 5V ± 5%, an output current range from 1mA to 500mA, and a maximum ambient temperature of 85°C, what is the maximum junction temperature?

The power dissipation of the RHP51000-CSL is the following:

$$I_{OUT(MAX)} \times (V_{IN(MAX)} - V_{OUT}) + I_{GND} \times V_{IN(MAX)}$$

where:
$I_{OUT(MAX)} = 500mA$
$V_{IN(MAX)} = 5.25V$
I_{GND} (at $I_{OUT} = 500mA$ and $V_{IN} = 5.25V$) = 12.5mA

Therefore,

$$P_{DISS} = 0.5A \times (5.25V - 3.3V) + 12.5mA \times 5.25V = 1W$$

The thermal resistance is 33°C/W. Therefore, the junction temperature rise above ambient approximately equals 1W × 33°C/W = 33°C.

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient, which calculates as follows:

$$T_{JMAX} = 85°C + 33°C = 118°C$$

Overload Recovery

Like many IC power regulators, the RHP51000-CSL incorporates safe-operating-area (SOA) protection. The SOA protection activates at input-to-output differential voltages greater than 12V. The SOA protection decreases the current limit because the input-to-output differential increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltages up to the *Absolute Maximum Ratings* of the RHP51000-CSL. The RHP51000-CSL provides some level of output current for all values of input-to-output differentials. See *Figure 30*. When power is first applied and input voltage rises, the output follows the input and keeps the input-to-output differential low to allow the regulator to supply the large output current and start-up into high-current loads.

Due to current-limit foldback, however, at high-input voltages, a problem can occur if the output voltage is low, and the load current is high. Such situations occur after the removal of a short-circuit or if the EN/UV pin is pulled high after the input voltage is already turned on. The load-line in such cases intersects the output-current profile at two points. The regulator now has two stable operating points. With this double intersection, the input-power supply may need to be cycled down to zero and brought back up again to result in the output recover. Other linear regulators with foldback current-limit protection also exhibit this phenomenon; therefore, it is not unique to the RHP51000-CSL.

Protection Features

The RHP51000-CSL incorporates several protection features for battery-powered applications. Precision current-limit and thermal-overload protection protect the RHP51000-CSL against overload and fault conditions at the output fo the device. For normal operation, do not allow the junction temperature to exceed 125°C.

To protect the low-noise error amplifier of the RHP51000-CSL, the SET-to-OUTS protection clamp limits the maximum voltage between SET and OUTS with a maximum DC current of 20mA through the clamp. Therefore, for applications where SET is actively driven by a voltage source, the voltage source must be current limited to 20mA or less. Moreover, to limit the transient current flowing through these clamps during a transient fault condition, limit the maximum value of the SET pin capacitor (C_{SET}) to 22µF.

The RHP51000-CSL also incorporates reverse-input protection whereby the IN pin withstands reverse voltages of up to –20V without causing any input-current flow and without developing negative voltages at the OUT pin. The regulator protects both itself and the load against batteries that are plugged in backwards.

In circuits where a backup battery is required, several different input and output conditions can occur. The output voltage can be held up while the input is either pulled to GND, pulled to some intermediate voltage, or left open-circuit. In all cases, the reverse-current protection circuitry prevents current flow from output to the input. Nonetheless, due to the OUTS-to-SET clamp, unless the SET pin is floating, current can flow to GND through the SET pin resistor as well as up to 15mA to GND through the output overshoot recovery circuitry. This current flow through the output overshoot recovery circuitry can be significantly reduced by placing a Schottky diode between the OUTS and SET pins, with its anode at the OUTS pin.

TYPICAL APPLICATIONS

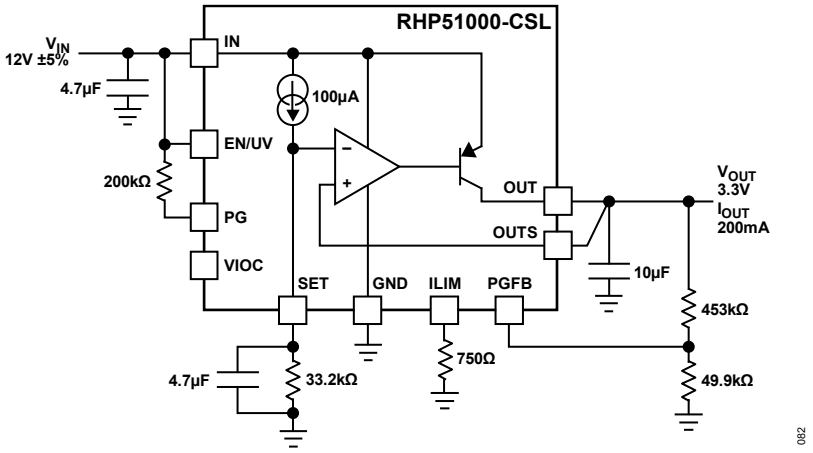


Figure 80. 12V_{IN} to 3.3V_{OUT} with 0.8µV_{RMS} Integrated Noise

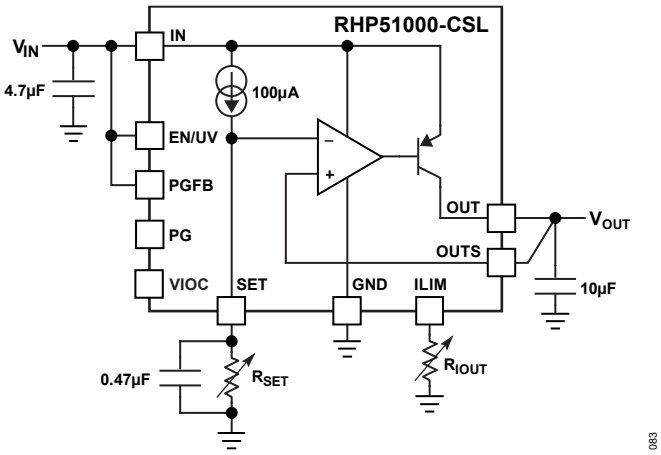


Figure 81. Low Noise CC/CV Lab Power Supply

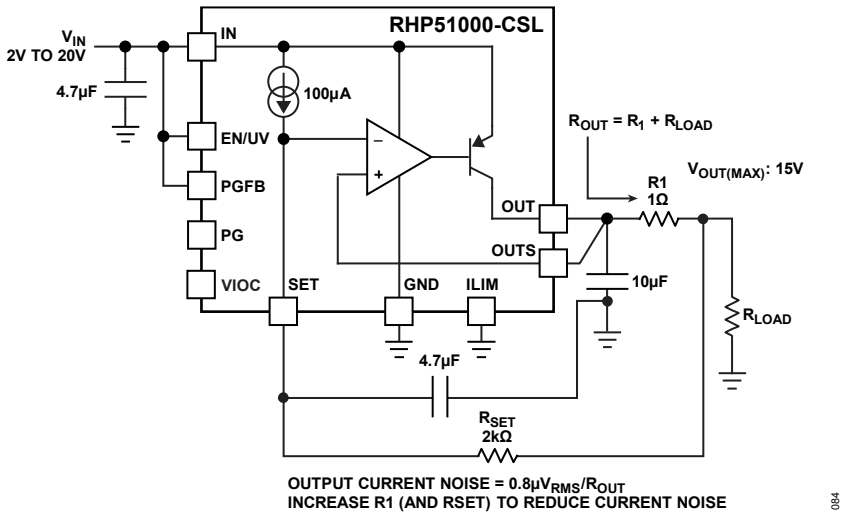


Figure 82. Ultra-Low Noise Current Source for RF Biasing Applications

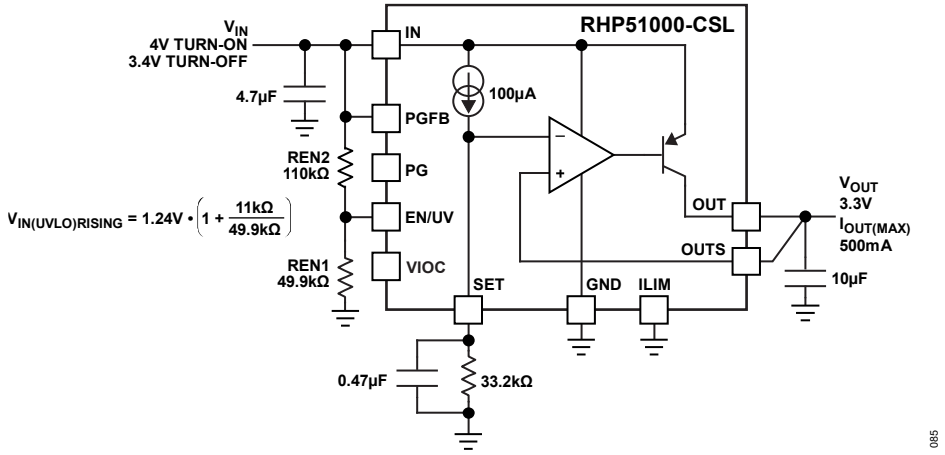


Figure 83. Programming Undervoltage Lockout

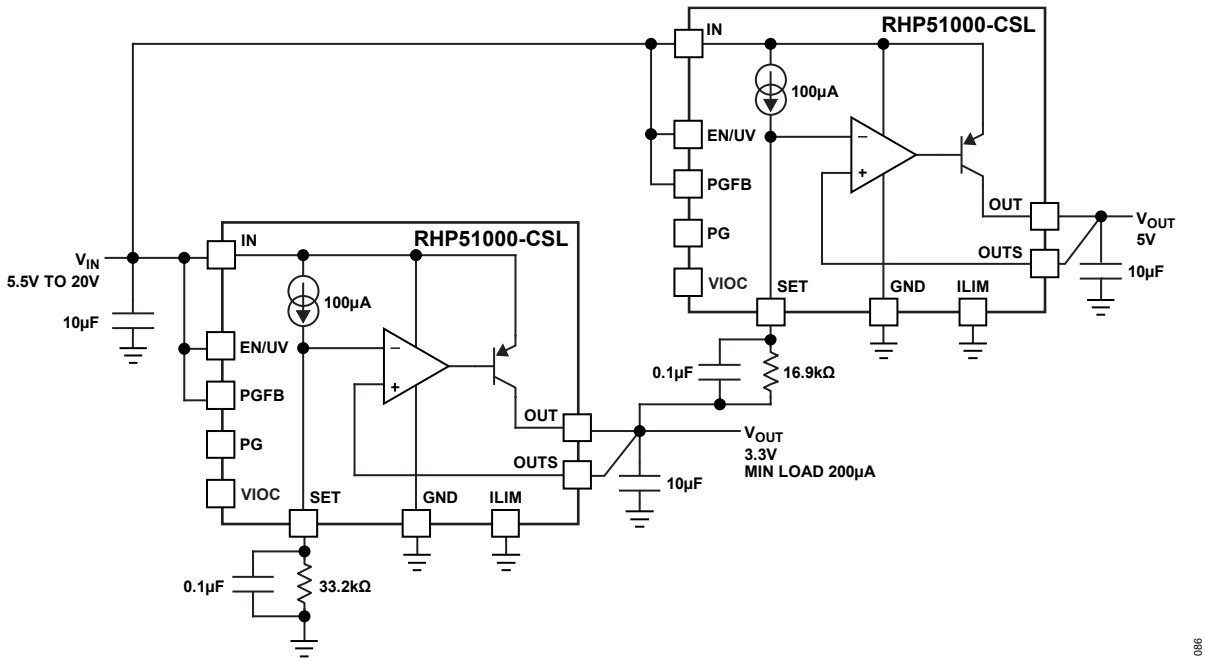


Figure 84. Ratiometric Tracking

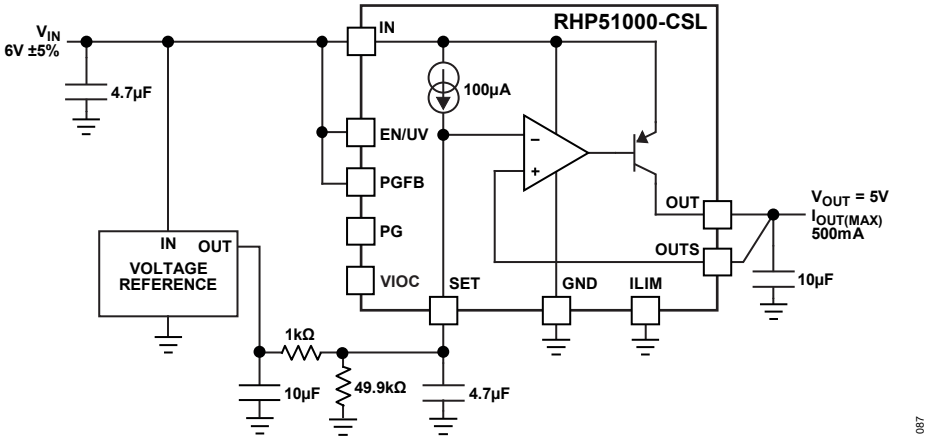


Figure 85. Ultralow 1/f Noise Reference Buffer

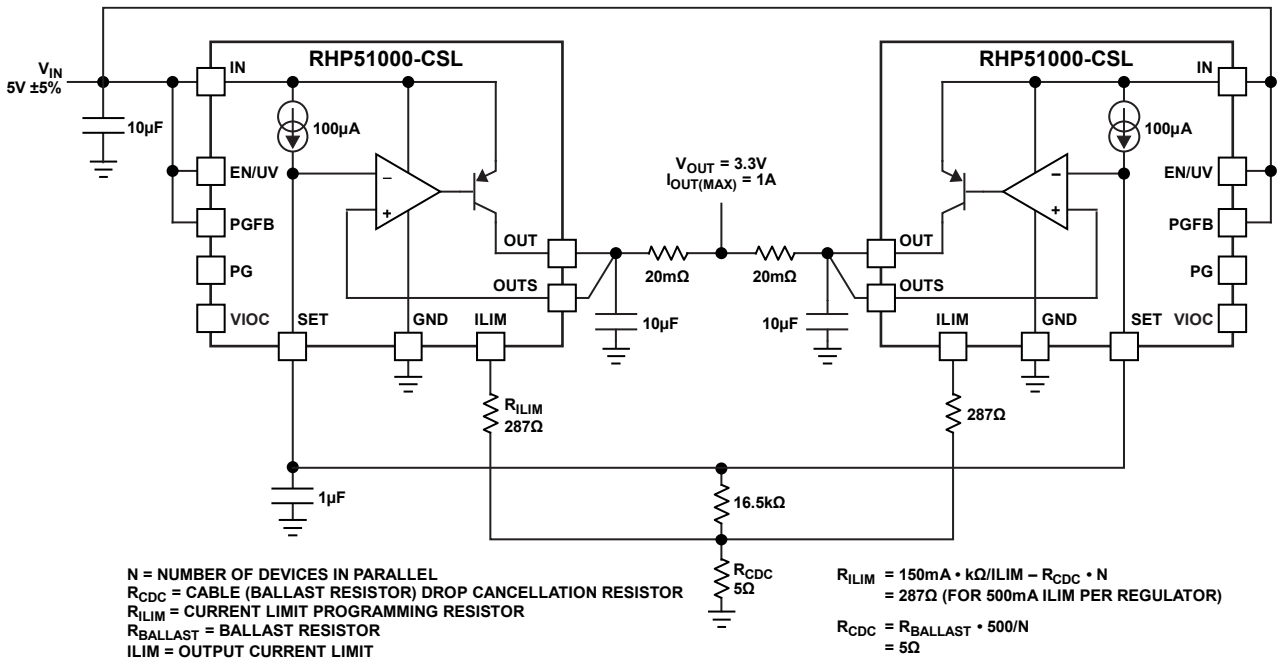


Figure 86. Paralleling Multiple Devices Using ILIM (Current Monitor) to Cancel Ballast Resistor Drop

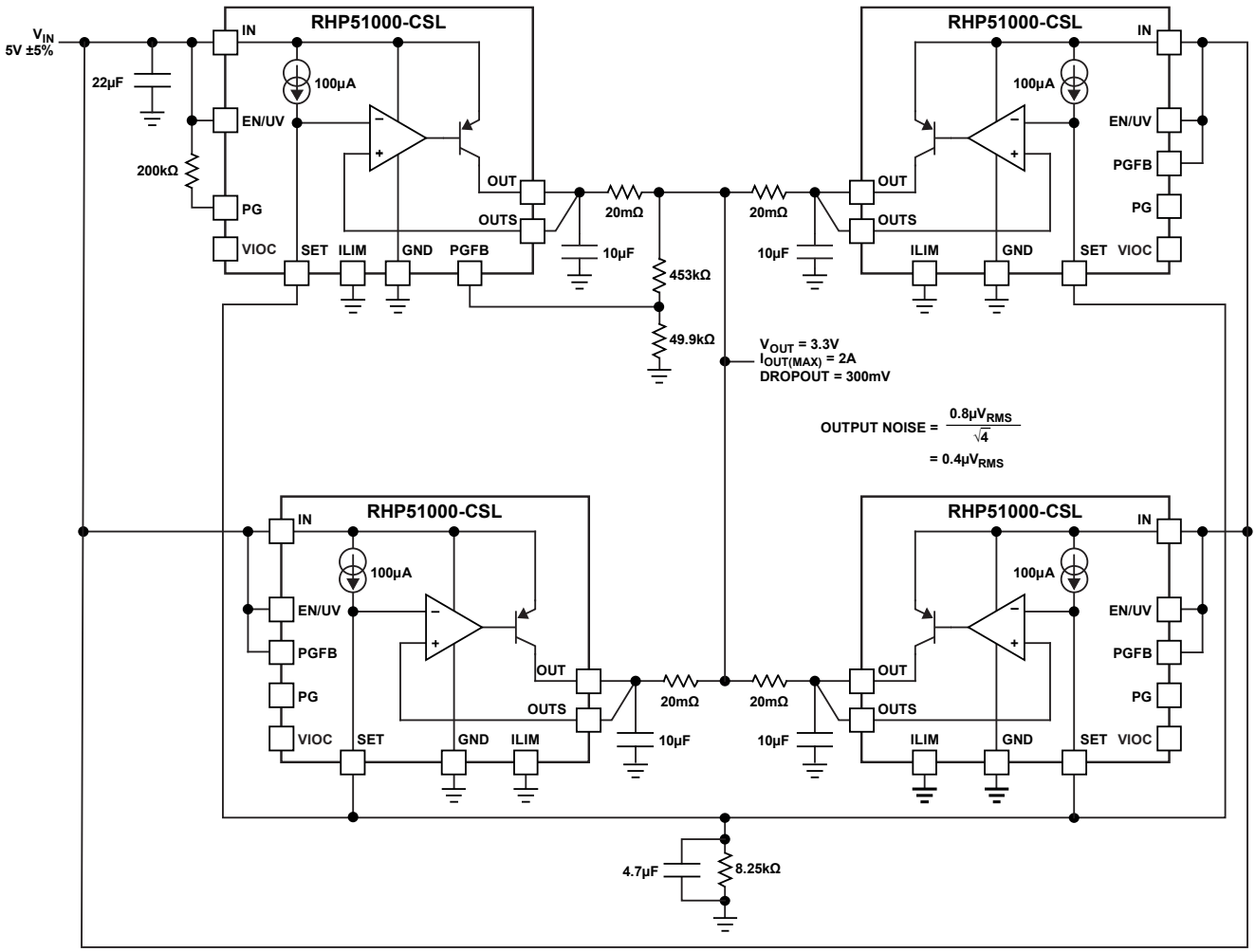


Figure 87. Paralleling Multiple RHP51000-CSLs for 2A Output Current

NOISE: 0.8µV$_{RMS}$ (10Hz TO 100kHz)

RESISTOR TOLERANCE	BRIDGE PSRR	NOISE AT VBRIDGE
PERFECT MATCHING	INFINITE	–
1%	40dB	8nV$_{RMS}$
5%	26dB	42.5nV$_{RMS}$

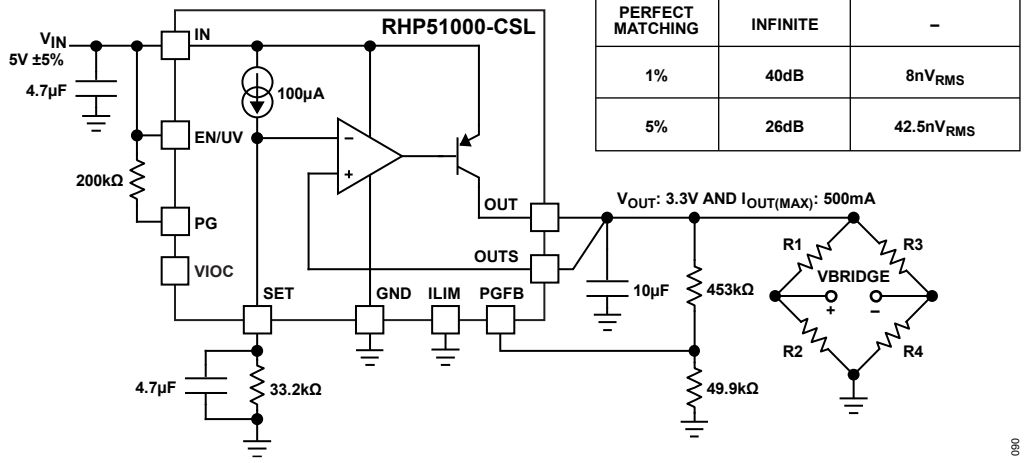


Figure 88. Low Noise Wheatstone Bridge Power Supply

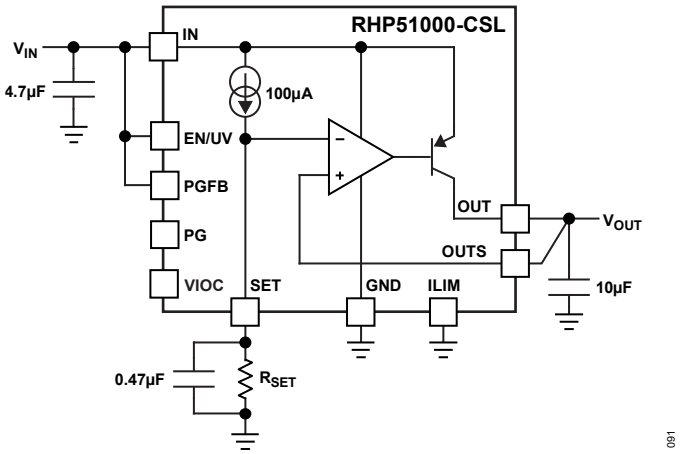


Figure 89. PGFB Disabled without Reverse Input Protection

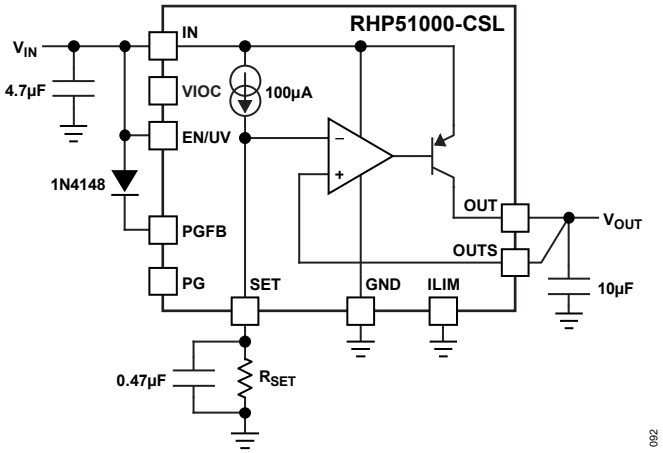


Figure 90. PGFB Disabled with Reverse Input Protection

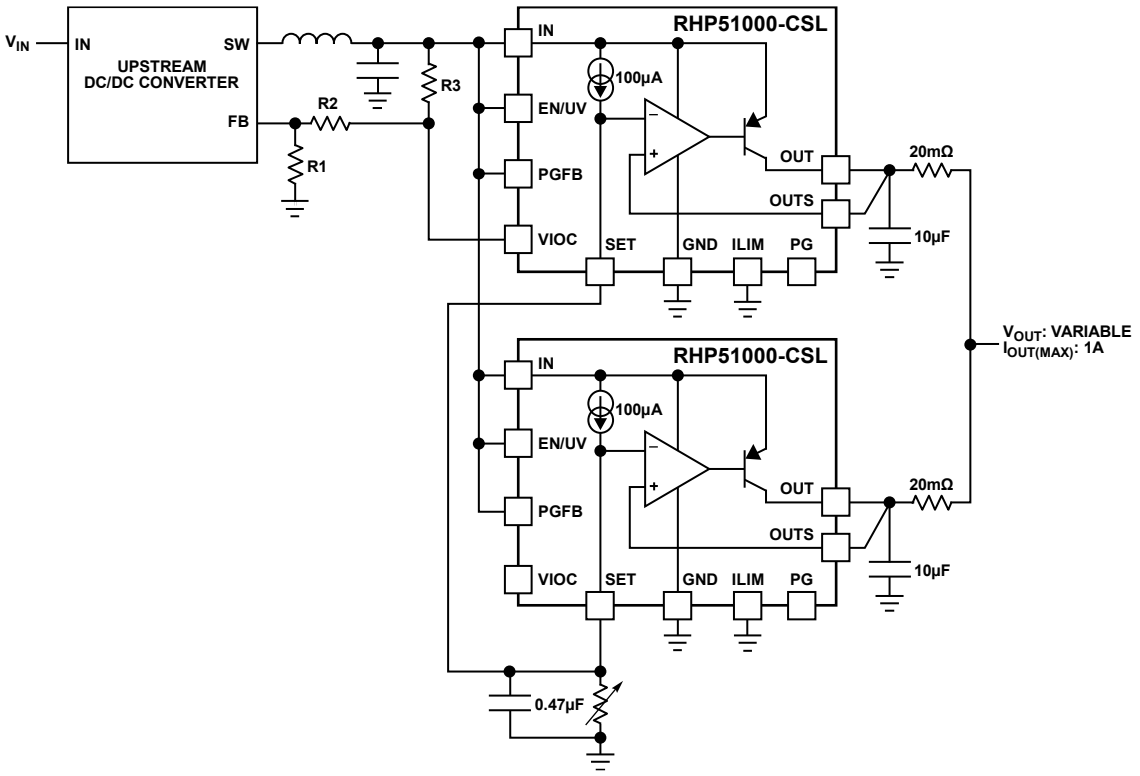
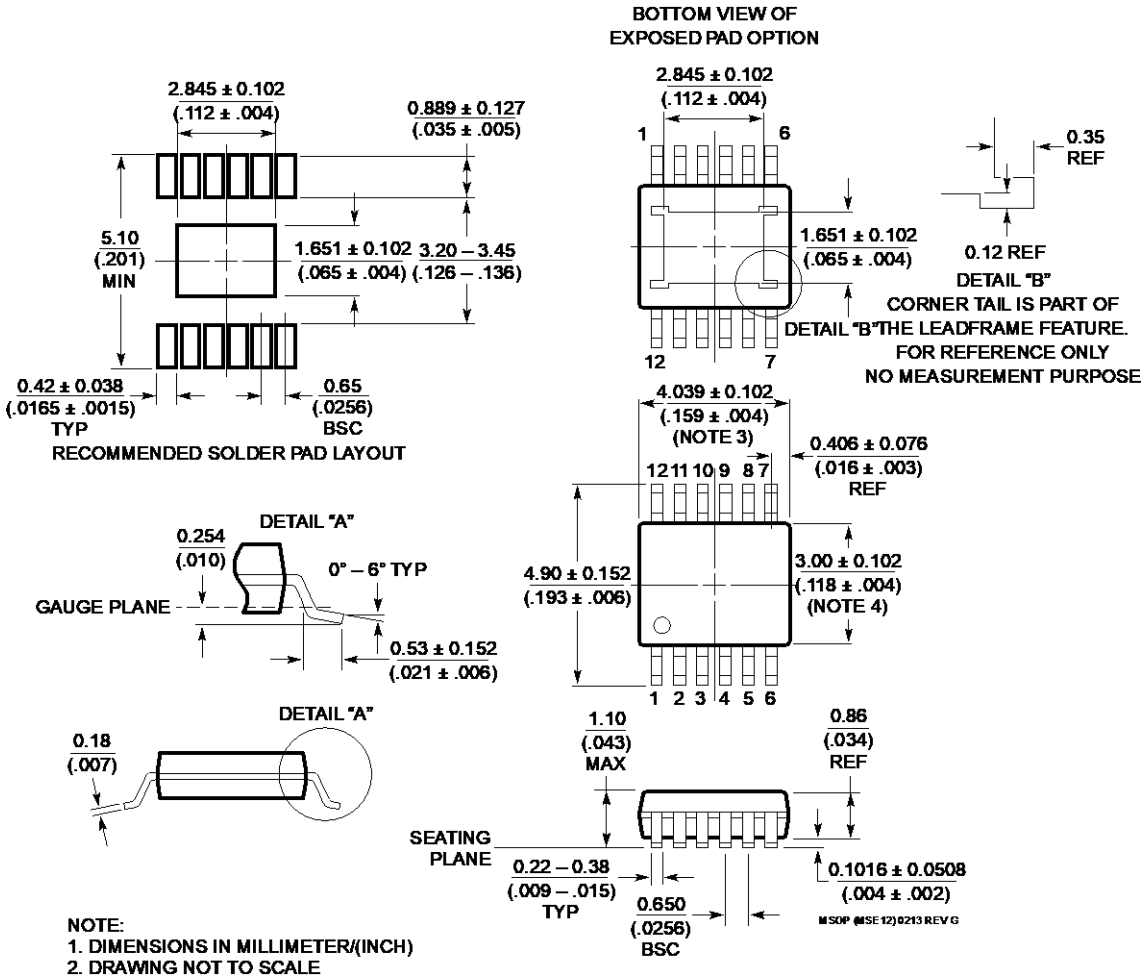


Figure 91. Parallel Devices

PACKAGE DESCRIPTION



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

Figure 92. MSE Package 12-Lead Plastic MSOP, Exposed Die Pad (Reference LTC DWG # 05-08-1666 Rev G)

ORDERING GUIDE

MODEL	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE QUANTITY	MARKING CODE
RHP51000IMSE-CSL#PBF	–40°C to 125°C	12-Lead Plastic MSOP	Tube, 1	51000
RHP51000IMSE-CSL#TRPBF	–40°C to 125°C	12-Lead Plastic MSOP	Reel, 2500	51000

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/26	Initial Release	—
1	8/26	Updated Header Updated Package Quantity Column in the Ordering Guide	1–47 45