

Precision, High Speed
Operational Amplifier

DESCRIPTION

The RH[®]118 is a precision, high speed operational amplifier which offers wide bandwidth and high slew rate. Unlike many wideband amplifiers, the RH118 is unity-gain stable and has a slew rate of 50V/μs.

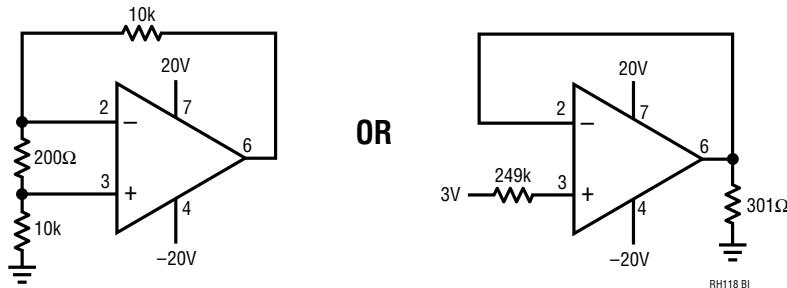
The wafer lots are processed to Analog Devices' in-house Class S flow to yield circuits usable in stringent military applications.

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ABSOLUTE MAXIMUM RATINGS

| | |
|---|----------------|
| Supply Voltage..... | ±20V |
| Differential Input Current (Note 1)..... | ±10mA |
| Input Voltage (Note 2) | ±20V |
| Output Short-Circuit Duration | Indefinite |
| Operating Temperature Range | -55°C to 125°C |
| Storage Temperature Range | -65°C to 150°C |
| Lead Temperature (Soldering, 10 sec)..... | 300°C |

BURN-IN CIRCUIT (Each Amplifier)



PACKAGE/ORDER INFORMATION

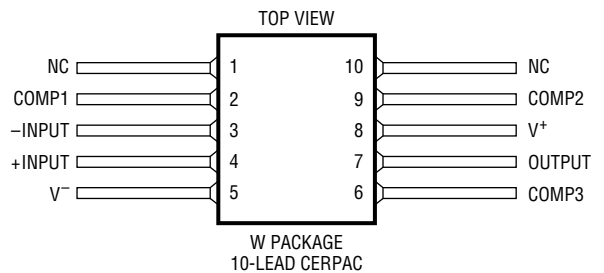
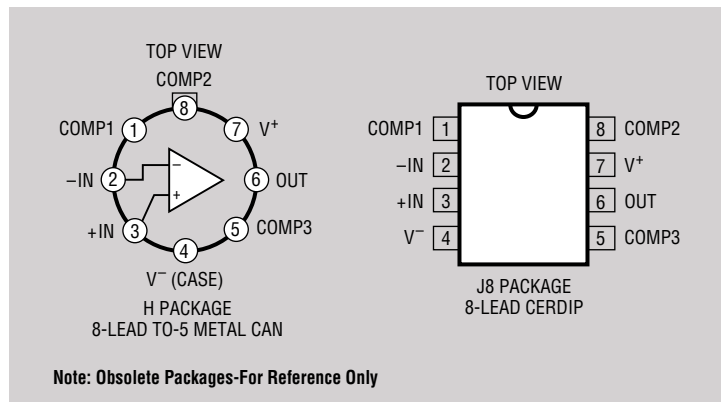


TABLE 1: ELECTRICAL CHARACTERISTICS (Preirradiation) (Note 3)

Device is characterized at the TID levels below. Device is production tested at 100kRad(Si).

| SYMBOL | PARAMETER | CONDITIONS | NOTES | T _A = 25°C | | | SUB-GROUP | -55°C ≤ T _A ≤ 125°C | | | SUB-GROUP | UNITS |
|-----------------|------------------------------|---|-------|-----------------------|-----|-----|-----------|--------------------------------|-----|-----|-----------|-------|
| | | | | MIN | TYP | MAX | | MIN | TYP | MAX | | |
| V _{OS} | Input Offset Voltage | | | | | 4 | 1 | | | 6 | 2,3 | mV |
| I _{OS} | Input Offset Current | | | | | 50 | 1 | | | 100 | 2,3 | nA |
| I _B | Input Bias Current | | | | | 250 | 1 | | | 500 | 2,3 | nA |
| R _{IN} | Input resistance | | 4 | 1 | | | | | | | | MΩ |
| A _V | Large-Signal Voltage Gain | V _S = ±15V, V _{OUT} = ±10V R _L ≥ 2k | | 50 | | | 1 | 25 | | | 2,3 | V/mV |
| SR | Slew Rate | V _S = ±15V, A _V = 1 | 5 | 50 | | | | | | | | V/μs |
| GBW | Gain Bandwidth Product | V _S = ±15V | | 15 | | | | | | | | MHz |
| | Output Voltage Swing | V _S = ±15V, R _L = 2k | | ±12 | | | 4 | ±12 | | | 5,6 | V |
| | Input Voltage Range | V _S = ±20V | | ±16.5 | | | 1 | ±16.5 | | | 2,3 | V |
| I _S | Supply Current | | | | | 8 | 1 | | | | | mA |
| | | T _A = 125°C | | | | | | | | 7 | 2 | mA |
| CMRR | Common Mode Rejection Ratio | | | 80 | | | 1 | 80 | | | 2,3 | dB |
| PSRR | Power Supply Rejection Ratio | | | 70 | | | 1 | 70 | | | 2,3 | dB |

TABLE 1A: ELECTRICAL CHARACTERISTICS (Postirradiation) (Note 6)

Device is characterized at the TID levels below. Device is production tested at 100kRad(Si).

| SYMBOL | PARAMETER | CONDITIONS | NOTES | 10kRad(Si) | | 20kRad(Si) | | 50kRad(Si) | | 100kRad(Si) | | 200kRad(Si) | | UNITS |
|-----------------|------------------------------|---|-------|------------|-------|------------|-------|------------|-------|-------------|-----|-------------|-----|-------|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{OS} | Input Offset Voltage | | | 4 | | 4 | | 4 | | 4 | | 10 | | mV |
| I _{OS} | Input Offset Current | | | 50 | | 50 | | 50 | | 50 | | 100 | | nA |
| I _B | Input Bias Current | | | 250 | | 250 | | 250 | | 300 | | 400 | | nA |
| R _{IN} | Input Resistance | | 4 | 1 | | 1 | | 1 | | 0.5 | | 0.5 | | MΩ |
| A _V | Large-Signal Voltage Gain | V _S = ±15V, V _{OUT} = ±10V R _L ≥ 2k | | 50 | | 50 | | 50 | | 50 | | 25 | | V/mV |
| SR | Slew Rate | V _S = ±15V, A _V = 1 | 5 | 50 | | 50 | | 50 | | 50 | | 50 | | V/μs |
| GBW | Gain Bandwidth Product | V _S = ±15V | | 15 | 15 | 15 | 15 | 15 | 15 | 15 | MHz | | | |
| | | | | (Typ) | (Typ) | (Typ) | (Typ) | (Typ) | (Typ) | (Typ) | | | | |
| | Output Voltage Swing | V _S = ±15V, R _L = 2k | | ±12 | | ±12 | | ±12 | | ±12 | | ±12 | | V |
| | Input Voltage Range | | | ±16.5 | | ±16.5 | | ±16.5 | | ±15 | | ±12 | | V |
| I _S | Supply Current | | | 8 | | 8 | | 8 | | 8 | | 8 | | mA |
| CMRR | Common Mode Rejection Ratio | | | 80 | | 80 | | 80 | | 80 | | 70 | | dB |
| PSRR | Power Supply Rejection Ratio | | | 70 | | 70 | | 70 | | 70 | | 60 | | dB |

ELECTRICAL CHARACTERISTICS (Continued)

Note 1: The inputs are shunted with back-to-back Zeners for overvoltage protection. Excessive current will flow if a differential voltage greater than 5V is applied to the inputs.

Note 2: For supply voltages less than $\pm 15\text{V}$, the maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5\text{V} \leq V_S \leq \pm 20\text{V}$. The power supplies must be bypassed with a $0.1\mu\text{F}$ or greater disc capacitor within four inches of the device.

Note 4: Guaranteed by design, characterization or correlation to other tested parameters.

Note 5: Slew rate is 100% tested at wafer probe testing. It is QA sample tested in finished package form.

Note 6: $T_A = 25^\circ\text{C}$, $V_S = \pm 20\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise specified. Supply bypassed per Note 3.

TOTAL DOSE BIAS CIRCUIT

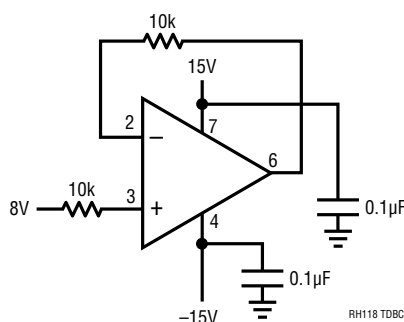


TABLE 2: ELECTRICAL TEST REQUIREMENTS

| MIL-PRF-38535 TEST REQUIREMENTS | SUBGROUP |
|---|-------------------|
| Final Electrical Test Requirements | 1*, 2, 3, 4, 5, 6 |
| Group A Test Requirements | 1, 2, 3, 4, 5, 6 |
| Group C End Point Electrical Parameters | 1, 2, 3 |
| Group D End Point Electrical Parameters | 1, 2, 3 |
| Group E End Point Electrical Parameters | 1 |

*PDA Applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures (including Delta parameters) of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

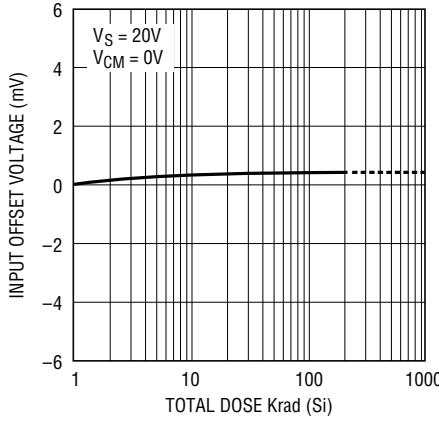
Analog Devices reserves the right to test to tighter limits than those given.

REVISION HISTORY

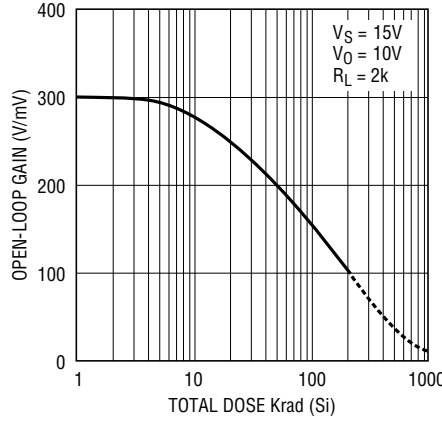
| REV | DATE | DESCRIPTION | PAGE NUMBER |
|-----|-------|---|-------------|
| C | 04/19 | Obsolete H + J Package and updating to ADI format | 1-4 |
| D | 07/23 | Updated art title in the Electrical Characteristics section | 2 |
| E | 06/24 | Changed Electrical Test Requirements, Table 2 | 3 |

TYPICAL PERFORMANCE CHARACTERISTICS

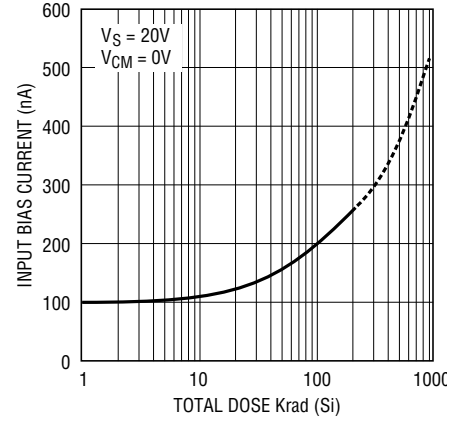
Input Offset Voltage



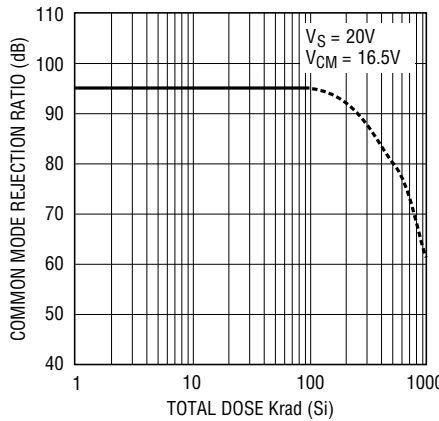
Input Bias Current



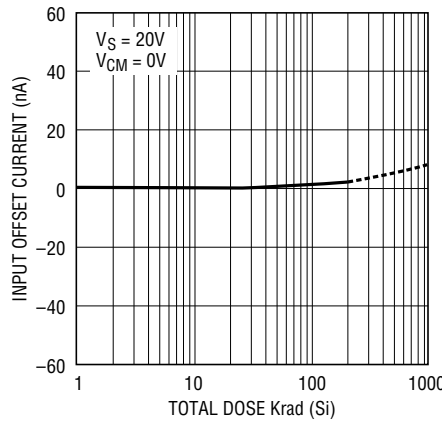
Input Offset Current



Open-Loop Gain



Common Mode Rejection Ratio



Power Supply Rejection Ratio

