PSM Family
ERRATA SHEET

PSM PMBus Silicon Errata

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Analog Devices may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Analog Devices has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

This errata sheet only applies to the LTC3880, LTC3882, LTC3883, LTC3884, LTC3886, LTC3887, LTC3888, LTC3889, LTC7132, LTC7880, and LTC7883 (all versions of these parts).

1) **THE DEVICE MAY INCORRECTLY NACK ITS ADDRESS IF THE DELAY BETWEEN COMMANDS IS TOO GREAT**

Conditions:
The following conditions, when present simultaneously, may expose this problem:

- The PMBus is idle or communicating at a very slow update rate.
- A command is sent to the device by the host.

Impact:
The part may time out incorrectly and not process the command sent by the host. The device address will be NACKed so the host is aware of the error.

Root Cause:
The PMBus data packet timeout is based on the time delay between START commands, not the delay between START and STOP commands (as defined in the data sheet). Every subsequent START command restarts the PMBus timer, and the STOP command does not disable the timer. The timer starts at the first START command on the bus. It runs continuously and is reset to 0 every time a START command occurs. The time delay between resets is nominally 30ms. If bit 3 of MFR_CONFIG_ALL is set to 1, the time delay is increased to 254ms. If a START command is sent to the part when the internal PMBus timeout timer is in reset, the command will be missed, and the part will NACK its address. The part is in reset for two internal clocks (nominally 62.5ns), then it is available to receive commands. Thus, the window of vulnerability is approximately 60ns out of either 30ms or 254ms depending on the setting of MFR_CONFIG_ALL bit 3.

Workarounds:
Three workarounds are possible, depending on the system configuration and requirements. Additional workarounds may be possible. Contact Factory Applications for additional assistance, if required.

Workaround 1:
Ensure that the bus is never idle for more than 30ms or 254ms if MFR_CONFIG_ALL bit 3 is set to 1.

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Workaround 2:

If the part NACKs its address, send the command again within the reset time interval. The time interval can be increased to nominally 254ms by setting bit 3 of MFR_CONFIG_ALL to 1 to allow more time for the host to resend the command.

Workaround 3:

Send any command with a valid START/STOP on the bus to any address before sending the command to the part. Then send the desired command to the part within the reset time interval. The time interval can be increased to nominally 254ms by setting bit 3 of MFR_CONFIG_ALL to 1 to allow more time for the host to resend the command. For example, if a bus mux is used in the system, send the Enable Bus Mux command twice before sending the desired command to the part. Send the command to the part within the reset time interval to assure valid processing of the command.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/25	Initial release	—