FEATURES
Excellent Sonic Characteristics
Low Noise: 6 nV/√Hz
Low Distortion: 0.0006%
High Slew Rate: 22 V/µs
Wide Bandwidth: 9 MHz
Low Supply Current: 5 mA
Low Offset Voltage: 1 mV
Low Offset Current: 2 nA
Unity Gain Stable
SOIC-8 Package
PDIP-8 Package

APPLICATIONS
High Performance Audio
Active Filters
Fast Amplifiers
Integrators

GENERAL DESCRIPTION
The OP275 is the first amplifier to feature the Butler Amplifier front end. This new front end design combines both bipolar and JFET transistors to attain amplifiers with the accuracy and low noise performance of bipolar transistors, and the speed and sound quality of JFETs. Total Harmonic Distortion plus Noise equals that of previous audio amplifiers, but at much lower supply currents.

A very low l/f corner of below 6 Hz maintains a flat noise density response. Whether noise is measured at either 30 Hz or 1 kHz, it is only 6 nV/√Hz. The JFET portion of the input stage gives the OP275 its high slew rates to keep distortion low, even when large output swings are required, and the 22 V/µs slew rate of the OP275 is the fastest of any standard audio amplifier. Best of all, this low noise and high speed are accomplished using less than 5 mA of supply current, lower than any standard audio amplifier.

Improved dc performance is also provided with bias and offset currents greatly reduced over purely bipolar designs. Input offset voltage is guaranteed at 1 mV and is typically less than 200 µV. This allows the OP275 to be used in many dc-coupled or summing applications without the need for special selections or the added noise of additional offset adjustment circuitry.

The output is capable of driving 600 Ω loads to 10 V rms while maintaining low distortion. THD + Noise at 3 V rms is a low 0.0006%.

The OP275 is specified over the extended industrial (–40°C to +85°C) temperature range. OP275s are available in both plastic DIP and SOIC-8 packages. SOIC-8 packages are available in 2500-piece reels. Many audio amplifiers are not offered in SOIC-8 surface-mount packages for a variety of reasons; however, the OP275 was designed so that it would offer full performance in surface-mount packaging.
## ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15.0$ V, $T_A = 25^\circ$C, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td><strong>AUDIO PERFORMANCE</strong></td>
<td></td>
<td></td>
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<tr>
<td>THD + Noise</td>
<td></td>
<td>$V_{IN} = 3$ V rms, $R_L = 2$ k\Omega, $f = 1$ kHz</td>
<td>0.006</td>
<td>%</td>
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<tr>
<td>Voltage Noise Density</td>
<td>$e_n$</td>
<td>$f = 30$ Hz</td>
<td>7</td>
<td>nV/Hz</td>
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<td>Current Noise Density</td>
<td>$i_n$</td>
<td>$f = 1$ kHz</td>
<td>6</td>
<td>nV/Hz</td>
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<tr>
<td>Headroom</td>
<td></td>
<td>$THD + Noise \leq 0.01%$, $R_L = 2$ k\Omega, $V_S = \pm 18$ V</td>
<td>&gt;12.9</td>
<td>dBu</td>
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<tr>
<td><strong>INPUT CHARACTERISTICS</strong></td>
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<td></td>
</tr>
<tr>
<td>Offset Voltage</td>
<td>$V_{OS}$</td>
<td>$-40^\circ$ C $\leq T_A \leq +85^\circ$C</td>
<td>1</td>
<td>mV</td>
<td></td>
<td></td>
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<tr>
<td>Input Bias Current</td>
<td>$I_B$</td>
<td>$V_{CM} = 0$ V</td>
<td>100</td>
<td>nA</td>
<td>350</td>
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<tr>
<td>Input Offset Current</td>
<td>$I_{OS}$</td>
<td>$V_{CM} = 0$ V, $-40^\circ$ C $\leq T_A \leq +85^\circ$C</td>
<td>2</td>
<td>nA</td>
<td>50</td>
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<td>Input Voltage Range</td>
<td>$V_{CM}$</td>
<td>$V_{CM} = 0$ V</td>
<td>106</td>
<td>dB</td>
<td>200</td>
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<tr>
<td>Common-Mode Rejection Ratio</td>
<td>CMRR</td>
<td>$V_{CM} = \pm 10.5$ V, $-40^\circ$ C $\leq T_A \leq +85^\circ$C</td>
<td>80</td>
<td>dB</td>
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<td>Large Signal Voltage Gain</td>
<td>$A_{VO}$</td>
<td>$R_L = 2$ k\Omega, $-40^\circ$ C $\leq T_A \leq +85^\circ$C</td>
<td>175</td>
<td>V/mV</td>
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<td>Offset Voltage Drift</td>
<td>$\Delta V_{OS}/\Delta T$</td>
<td>$R_L = 600$ $\Omega$, $V_S = \pm 18$ V</td>
<td>2</td>
<td>$\mu$V/°C</td>
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<td></td>
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<td><strong>OUTPUT CHARACTERISTICS</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Output Voltage Swing</td>
<td>$V_O$</td>
<td>$R_L = 2$ k\Omega</td>
<td>-13.5</td>
<td>V</td>
<td>+13.5</td>
<td>V</td>
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<tr>
<td></td>
<td></td>
<td>$R_L = 2$ k\Omega, $-40^\circ$ C $\leq T_A \leq +85^\circ$C</td>
<td>-13</td>
<td>V</td>
<td>+13</td>
<td>V</td>
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<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>$V_S = \pm 4.5$ V to $\pm 18$ V</td>
<td>85</td>
<td>dB</td>
<td>111</td>
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<tr>
<td>Supply Current</td>
<td>$I_{SV}$</td>
<td>$V_S = \pm 4.5$ V to $\pm 18$ V, $V_{O} = 0$ V, $R_L = \infty$, $-40^\circ$ C $\leq T_A \leq +85^\circ$C</td>
<td>4</td>
<td>mA</td>
<td>5</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>$V_S = \pm 22$ V, $V_{O} = 0$ V, $R_L = \infty$, $-40^\circ$ C $\leq T_A \leq +85^\circ$C</td>
<td>5.5</td>
<td>mA</td>
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<td><strong>DYNAMIC PERFORMANCE</strong></td>
<td></td>
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<tr>
<td>Slew Rate</td>
<td>SR</td>
<td>$R_L = 2$ k\Omega</td>
<td>15</td>
<td>V/\mu s</td>
<td>22</td>
<td>kHz</td>
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<td>Full-Power Bandwidth</td>
<td>BW_P</td>
<td>$R_L = 2$ k\Omega</td>
<td></td>
<td>kHz</td>
<td></td>
<td></td>
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<tr>
<td>Gain Bandwidth Product</td>
<td>GBP</td>
<td>$R_L = 2$ k\Omega</td>
<td>9</td>
<td>MHz</td>
<td></td>
<td></td>
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<tr>
<td>Phase Margin</td>
<td>$\phi_m$</td>
<td>$R_L = 2$ k\Omega</td>
<td>62</td>
<td>Degrees</td>
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<tr>
<td>Overshoot Factor</td>
<td></td>
<td>$V_{IN} = 100$ mV, $A_V = +1$, $R_L = 600$ $\Omega$, $C_L = 100$ $\mu$F</td>
<td>10</td>
<td>%</td>
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</tbody>
</table>

Specifications subject to change without notice.
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ............................................. ±22 V
Input Voltage ............................................. ±22 V
Differential Input Voltage ................................ ±7.5 V
Output Short-Circuit Duration to GND ..................... Indefinite

Storage Temperature Range
  P, S Packages ........................................... –65°C to +150°C

Operating Temperature Range
  OP275G ................................................... –40°C to +85°C

Junction Temperature Range
  P, S Packages ........................................... –65°C to +150°C

Lead Temperature Range (Soldering, 60 sec) ...................... 300°C

<table>
<thead>
<tr>
<th>Package Type</th>
<th>$\theta_J$</th>
<th>$\theta_J$</th>
<th>Unit</th>
</tr>
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<tbody>
<tr>
<td>8-Lead Plastic DIP (P)</td>
<td>103</td>
<td>43</td>
<td>°C/W</td>
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<tr>
<td>8-Lead SOIC (S)</td>
<td>158</td>
<td>43</td>
<td>°C/W</td>
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</tbody>
</table>

NOTES

1 Absolute maximum ratings apply to packaged parts, unless otherwise noted.
2 For supply voltages greater than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
3 Shorts to either supply may destroy the device. See data sheet for full details.
4 $\theta_J$ is specified for the worst-case conditions, i.e., $\theta_J$ is specified for device in socket for PDIP packages; $\theta_J$ is specified for device soldered in circuit board for SOIC packages.

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
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<tr>
<td>OP275GP</td>
<td>–40°C to +85°C</td>
<td>8-Lead PDIP</td>
<td>N-8</td>
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<tr>
<td>OP275GS</td>
<td>–40°C to +85°C</td>
<td>8-Lead SOIC</td>
<td>R-8</td>
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<tr>
<td>OP275GS-REEL</td>
<td>–40°C to +85°C</td>
<td>8-Lead SOIC</td>
<td>R-8</td>
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<tr>
<td>OP275GS-REEL7</td>
<td>–40°C to +85°C</td>
<td>8-Lead SOIC</td>
<td>R-8</td>
</tr>
<tr>
<td>OP275GSZ*</td>
<td>–40°C to +85°C</td>
<td>8-Lead SOIC</td>
<td>R-8</td>
</tr>
<tr>
<td>OP275GSZ-REEL*</td>
<td>–40°C to +85°C</td>
<td>8-Lead SOIC</td>
<td>R-8</td>
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<tr>
<td>OP275GSZ-REEL7*</td>
<td>–40°C to +85°C</td>
<td>8-Lead SOIC</td>
<td>R-8</td>
</tr>
</tbody>
</table>

*Z = Pb-free part.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP275 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
TPC 1. Output Voltage Swing vs. Supply Voltage

TPC 2. Open-Loop Gain vs. Temperature

TPC 3. Closed-Loop Gain and Phase, $A_V = +1$

TPC 4. Open-Loop Gain, Phase vs. Frequency

TPC 5. Closed-Loop Gain vs. Frequency

TPC 6. Closed-Loop Output Impedance vs. Frequency

TPC 7. Common-Mode Rejection vs. Frequency

TPC 8. Power Supply Rejection vs. Frequency

TPC 9. Open-Loop Gain, Phase vs. Frequency
OP275 – Typical Performance Characteristics

**TEMPERATURE – °C**
- Gain Bandwidth Product – MHz
- Phase Margin – Degrees
- Overshoot – %
- Overload Voltage – V
- Outputs: VOM

**FREQUENCY – Hz**
- Maximum Output Swing – V
- Supply Current – mA
- Absolute Output Current – mA

**SUPPLY VOLTAGE – V**
- Supply Current – mA
- Absolute Output Current – mA

**LOAD CAPACITANCE – pF**
- Maximum Output Swing – V

**LOAD RESISTANCE – Ω**
- Supply Current – mA
- Absolute Output Current – mA

**TCVOS – V/°C**
- TCVOS Distribution

**INPUT BIAS CURRENT – nA**
- Current Noise Density – pA/√Hz

**SUPPLY CURRENT – mA**
- Absolute Output Current – mA

**MAXIMUM OUTPUT SWING – V**
- Maximum Output Swing – V

**CURRENT NOISE DENSITY – pA/√Hz**
- Current Noise Density – pA/√Hz

**UNITS**
- TCVOS = µV/°C

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TPC 10. Gain Bandwidth Product, Phase Margin vs. Temperature
TPC 11. Small Signal Overshoot vs. Load Capacitance
TPC 12. Maximum Output Voltage vs. Load Resistance
TPC 13. Maximum Output Swing vs. Frequency
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TPC 15. Short-Circuit Current vs. Temperature
TPC 16. Input Bias Current vs. Temperature
TPC 17. Current Noise Density vs. Frequency
TPC 18. TCVOS Distribution
TPC 19. Input Offset ($V_{OS}$) Distribution

TPC 20. Step Size vs. Settling Time

TPC 21. Slew Rate vs. Capacitive Load

TPC 22. Slew Rate vs. Differential Input Voltage

TPC 23. Slew Rate vs. Temperature

TPC 24. Negative Slew Rate

TPC 25. Positive Slew Rate

TPC 26. Small Signal Response

TPC 27. Voltage Noise Density vs. Frequency $V_S = \pm 15$ V

TPC 28. 

TPC 29. 

TPC 30. 

CH A: 8.0 µV FS
MKR: 6.23 nV/Hz
BW: 15.0 MHz

0 Hz
MKR: 1.000 Hz

2.5 kHz

10.0 µV/DIV

50mV

100ns

500ns

REV. C
APPLICATIONS
Circuit Protection
OP275 has been designed with inherent short-circuit protection to ground. An internal 30 Ω resistor, in series with the output, limits the output current at room temperature to $I_{SC}^+ = 40$ mA and $I_{SC}^- = -90$ mA, typically, with ±15 V supplies.

However, shorts to either supply may destroy the device when excessive voltages or currents are applied. If it is possible for a user to short an output to a supply for safe operation, the output current of the OP275 should be design-limited to ±30 mA, as shown in Figure 1.

Total Harmonic Distortion
Total Harmonic Distortion + Noise (THD + N) of the OP275 is well below 0.001% with any load down to 600 Ω. However, this is dependent upon the peak output swing. In Figure 2, the THD + Noise with 3 V rms output is below 0.001%. In Figure 3, THD + Noise is below 0.001% for the 10 kΩ and 2 kΩ loads but increases to above 0.1% for the 600 Ω load condition. This is a result of the output swing capability of the OP275. Notice the results in Figure 4, showing THD versus $V_{IN}$ (V rms). This figure shows that the THD + Noise remains very low until the output reaches 9.5 V rms. This performance is similar to competitive products.

![Figure 1. Recommended Output Short-Circuit Protection](image1)

![Figure 2. THD + Noise vs. Frequency vs. $R_{LOAD}$](image2)

![Figure 3. THD + Noise vs. $R_{LOAD}; V_{IN} = 10$ V rms](image3)

The output of the OP275 is designed to maintain low harmonic distortion while driving 600 Ω loads. However, driving 600 Ω loads with very high output swings results in higher distortion if clipping occurs. A common example of this is in attempting to drive 10 V rms into any load with ±15 V supplies. Clipping will occur and distortion will be very high. To attain low harmonic distortion with large output swings, supply voltages may be increased. Figure 5 shows the performance of the OP275 driving 600 Ω loads with supply voltages varying from ±18 V to ±20 V. Notice that with ±18 V supplies the distortion is fairly high, while with ±20 V supplies it is a very low 0.0007%.

![Figure 4. Headroom, THD + Noise vs. Output Amplitude (V rms); $R_{LOAD} = 600$ Ω, $V_{SUP} = ±18$ V](image4)

![Figure 5. THD + Noise vs. Supply Voltage](image5)

Noise
The voltage noise density of the OP275 is below 7 nV/√Hz from 30 Hz. This enables low noise designs to have good performance throughout the full audio range. Figure 6 shows a typical OP275 with a 1/f corner at 2.24 Hz.

![Figure 6. 1/f Noise Corner, $V_S = ±15$ V, $A_V = 1000$](image6)
Noise Testing
For audio applications, the noise density is usually the most important noise parameter. For characterization, the OP275 is tested using an Audio Precision, System One. The input signal to the Audio Precision must be amplified enough to measure it accurately. For the OP275, the noise is gained by approximately 1020 using the circuit shown in Figure 7. Any readings on the Audio Precision must then be divided by the gain. In implementing this test fixture, good supply bypassing is essential.

Input Overcurrent Protection
The maximum input differential voltage that can be applied to the OP275 is determined by a pair of internal Zener diodes connected across its inputs. They limit the maximum differential input voltage to ±7.5 V. This is to prevent emitter-base junction breakdown from occurring in the input stage of the OP275 when very large differential voltages are applied. However, to preserve the OP275’s low input noise voltage, internal resistances in series with the inputs were not used to limit the current in the clamp diodes. In small signal applications, this is not an issue; however, in applications where large differential voltages can be inadvertently applied to the device, large transient currents can flow through these diodes. Although these diodes have been designed to carry a current of ±5 mA, external resistors as shown in Figure 8 should be used in the event that the OP275’s differential voltage were to exceed ±7.5 V.

Output Voltage Phase Reversal
Since the OP275’s input stage combines bipolar transistors for low noise and p-channel JFETs for high speed performance, the output voltage of the OP275 may exhibit phase reversal if either of its inputs exceeds its negative common-mode input voltage. This might occur in very severe industrial applications where a sensor or system fault might apply very large voltages on the inputs of the OP275. Even though the input voltage range of the OP275 unis the negative common-mode input voltage can be exceeded in small signal, but not in large signal applications, the input voltage will be limited to ±7.5 V by the internal clamp diodes. In inverting amplifier con

Overload or Overdrive Recovery
Overload or overdrive recovery time of an operational amplifier is the time required for the output voltage to recover to a rated output voltage from a saturated condition. This recovery time is important in applications where the amplifier must recover quickly after a large abnormal transient event. The circuit shown in Figure 10 was used to evaluate the OP275’s overload recovery time. The OP275 takes approximately 1.2 ms to recover to \( V_{OUT} = +10 \text{ V} \) and approximately 1.5 µs to recover to \( V_{OUT} = -10 \text{ V} \).

Measuring Settling Time
The design of OP275 combines a high slew rate and a wide gain bandwidth product to produce a fast settling \( (t_s < 1 \mu\text{s}) \) amplifier for 8- and 12-bit applications. The test circuit designed to measure the settling time of the OP275 is shown in Figure 11. This test method has advantages over false-sum node techniques in that the actual output of the amplifier is measured, instead of an error voltage at the sum node. Common-mode settling effects are exercised in this circuit in addition to the slew rate and bandwidth effects measured by the false-sum node method. Of course, a reasonably flat-top pulse is required as the stimulus.

High Speed Operation
As with most high speed amplifiers, care should be taken with supply decoupling, lead dress, and component placement. Recommended circuit configurations for inverting and non-inverting applications are shown in Figures 12 and 13.
In inverting and noninverting applications, the feedback resistance forms a pole with the source resistance and capacitance ($R_S$ and $C_S$) and the OP275’s input capacitance ($C_{IN}$), as shown in Figure 14. With $R_S$ and $R_F$ in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor, $C_{FB}$, in parallel and $R_{FB}$ eliminates this problem. By setting $R_S (C_S + C_{IN}) = R_{FB}C_{FB}$, the effect of the feedback pole is completely removed.

**Figure 15. Balanced Input Impedance to Minimize Distortion in Noninverting Amplifier Circuits**

Figure 15 shows some guidelines for maximizing the distortion performance of the OP275 in noninverting applications. The best way to prevent unwanted distortion is to ensure that the parallel combination of the feedback and gain setting resistors ($R_F$ and $R_C$) is less than 2 kΩ. Keeping the values of these resistors small has the added benefits of reducing the thermal noise of the circuit.
and dc offset errors. If the parallel combination of $R_F$ and $R_G$ is larger than 2 kΩ, then an additional resistor, $R_S$, should be used in series with the noninverting input. The value of $R_S$ is determined by the parallel combination of $R_F$ and $R_G$ to maintain the low distortion performance of the OP275.

**Driving Capacitive Loads**

The OP275 was designed to drive both resistive loads to 600 Ω and capacitive loads of over 1000 pF and maintain stability. While there is a degradation in bandwidth when driving capacitive loads, the designer need not worry about device stability. The graph in Figure 16 shows the 0 dB bandwidth of the OP275 with capacitive loads from 10 pF to 1000 pF.

**High Speed, Low Noise Differential Line Driver**

The circuit in Figure 17 is a unique line driver widely used in industrial applications. With ±18 V supplies, the line driver can deliver a differential signal of 30 V p-p into a 2.5 kΩ load. The high slew rate and wide bandwidth of the OP275 combine to yield a full power bandwidth of 130 kHz while the low noise front end produces a referred-to-input noise voltage spectral density of 10 nV/√Hz.

**A 3-Pole, 40 kHz Low-Pass Filter**

The closely matched and uniform ac characteristics of the OP275 make it ideal for use in GIC (Generalized Impedance Converter) and FDNR (Frequency-Dependent Negative Resistor) filter applications. The circuit in Figure 18 illustrates a linear-phase, 3-pole, 40 kHz low-pass filter using an OP275 as an inductance simulator (gyrator). The circuit uses one OP275 (A2 and A3) for the FDNR and one OP275 (A1 and A4) as an input buffer and bias current source for A3. Amplifier A4 is configured in a gain of 2 to set the pass band magnitude response to 0 dB. The benefits of this filter topology over classical approaches are that the op amp used in the FDNR is not in the signal path and that the filter’s performance is relatively insensitive to component variations. Also, the configuration is such that large signal levels can be handled without overloading any of the filter’s internal nodes. As shown in Figure 19, the OP275’s symmetric slew rate and low distortion produce a clean, well behaved transient response.
OP275 SPICE Model

* Node assignments
  * noninverting input
  * inverting input
  * positive supply
  * negative supply
  * output
**

.SUBCKT OP275 1 2 99 50 34

* INPUT STAGE & POLE AT 100 MHz
*
R3 5 51 2.188
R4 6 51 2.188
CIN 1 2 3.7E-12
CM1 1 98 7.5E-12
CM2 2 98 7.5E-12
C2 5 6 364E-12
I1 97 4 100E-3
IOS 1 2 1E-9
EOS 9 3 POLY(1) 26 28 0.5E-3 1
Q1 5 2 7 QX
Q2 6 9 8 QX
R5 7 4 1.672
R6 8 4 1.672
d1 2 36 D2
D2 1 36 D2
EN 3 1 10 0 1
GN1 0 2 13 0 1E-3
GN2 0 1 16 0 1E-3
*
EREF 98 0 28 0 1
EP 97 0 99 0 1
EM 51 0 50 0 1
*
* VOLTAGE NOISE SOURCE
*
DN1 35 10 DEN
DN2 10 11 DEN
VN1 35 0 DC 2
VN2 0 11 DC 2
*
* CURRENT NOISE SOURCE
*
DN3 12 13 DIN
DN4 13 14 DIN
VN3 12 0 DC 2
VN4 0 14 DC 2
*
* CURRENT NOISE SOURCE
*
DN5 15 16 DIN
DN6 16 17 DIN
VN5 15 0 DC 2
VN6 0 17 DC 2
*
* GAIN STAGE & DOMINANT POLE AT 32 Hz
*
R7 18 99 1.09E6
C3 18 98 4.55E-9
G1 98 18 5 6 4.57E-1
V2 97 19 1.35
V3 20 51 1.35
D3 18 19 DX
D4 20 18 DX
*
* POLE/ZERO PAIR AT 1.5 MHz/2.7 MHz
*
R8 21 98 1E-3
R9 21 22 1.25E-3
C4 22 98 47.2E-12
G2 98 21 18 28 1E-3
*
* POLE AT 100 MHz
*
R10 23 98 1
C5 23 98 1.59E-9
G3 98 23 21 28 1
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT 1 kHz
*
R11 24 98 1
C6 24 98 1.59E-9
G4 98 24 23 28 1
*
* OUTPUT STAGE
*
R15 28 99 100E3
R16 28 50 100E3
C9 28 50 1E-6
ISY 99 50 1.85E-3
R17 29 99 100
R18 29 50 100
L2 29 34 1E-9
G6 32 50 27 29 10E-3
G7 33 50 29 27 10E-3
G8 29 99 27 27 10E-3
G9 50 29 27 50 1E-3
V4 30 29 1.3
V5 29 31 3.8
F1 29 0 V4 1
F2 0 29 V5 1
D5 27 30 DX
D6 31 27 DX
D7 99 32 DX
D8 99 33 DX
D9 50 32 DY
D10 50 33 DY
*
* MODELS USED
*
.MODEL QX PNP(BF=5E5)
.MODEL DX D(IS=1E-12)
.MODEL DY D(IS=1E-15 BV=50)
.MODEL DZ D(IS=1E-15 BV=7.0)
.MODEL DEN D(IS=1E-12 RS=4.35K KF=1.95E-15 AF=1)
.MODEL DIN D(IS=1E-12 RS=268 KF=1.08E-15 AF=1)
.ENDS
OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package [SOIC] (S Suffix) (R-8)
Dimensions shown in millimeters and (inches)

Dimensions shown in inches and (millimeters)

Revision History

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2/04—Data Sheet changed from REV. B to REV. C. 3
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Updated OUTLINE DIMENSIONS 12
1/03—Data Sheet changed from REV. A to REV. B.
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