

**SCOPE: CMOS, 10-BIT MONOLITHIC, MULTIPLYING D/A CONVERTER**

<u>Device Type</u>	<u>Generic Number</u>
01	MX7533S(x)/883B
02	MX7533T(x)/883B
03	MX7533U(x)/883B

**Case Outline(s).** The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
Q	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
E	CQCC1-N20	20 LCC	L20

**Absolute Maximum Ratings:**

$V_{DD}$ to GND .....	-0.3V, + 17V
$V_{RFB}$ to GND .....	$\pm 25V$
$V_{REF}$ to GND .....	$\pm 25V$
Digital Input Voltage Range .....	-0.3V to $V_{DD}$
$V_{OUT1}$ , $V_{OUT2}$ , to GND .....	-0.3V to $V_{DD}$
Lead Temperature (soldering, 10 seconds) .....	+300°C
Storage Temperature .....	-65°C to +150°C
Continuous Power Dissipation .....	$T_A=+70^\circ C$
16 pin CERDIP(derate 10mW/°C above +70°C) .....	800mW
20 pin LCC(derate 9.1mW/°C above +70°C) .....	727mW
Junction Temperature $T_J$ .....	+150°C
Thermal Resistance, Junction to Case, $\theta_{JC}$	
16 pin CERDIP.....	50°C/W
20 pin LCC .....	20°C/W
Thermal Resistance, Junction to Ambient, $\theta_{JA}$ :	
16 pin CERDIP.....	100°C/W
20 pin LCC .....	110°C/W

**Recommended Operating Conditions**

Ambient Operating Range ( $T_A$ ) .....	-55°C to +125°C
Supply Voltage Range .....	+15V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TABLE 1. ELECTRICAL TESTS:**

TEST	Symbol	CONDITIONS	Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T <sub>A</sub> ≤ +125 °C 1/ Unless otherwise specified					
<b>ACCURACY</b>							
Resolution NOTE 2	RES			All	10		Bits
Relative Accuracy	RA		1,2,3	01 02 03		±2.0 ±1.0 ±0.5	LSB
Gain Error NOTE 3	AE		1 2,3	All		±14 ±15	LSB
Gain Tempco NOTE 2	TC <sub>AE</sub>			All	-10	10	ppm/°C
Power Supply Rejection (ΔGain/ΔV <sub>DD</sub> )	PSRR	Digital inputs at V <sub>IH</sub> , V <sub>DD</sub> =14V to 17V	1 2,3	All		±0.005 ±0.008	%/%
Output Leakage Current	I <sub>OUT1</sub>	Digital inputs at V <sub>IL</sub> , VREF=+10V	1 2,3	All		±50 ±200	nA
Output Leakage Current	I <sub>OUT2</sub>	Digital inputs at V <sub>IH</sub> , VREF=+10V	1 2,3	All		±50 ±200	nA
Output Current Settling Time NOTE 2		T <sub>O</sub> ±0.5LSB. OUT 1 load is 100Ω    13pF, digital inputs =V <sub>IH</sub> to V <sub>IL</sub> or V <sub>IL</sub> to V <sub>IH</sub>	4	All		0.8	μs
Feedthrough Error NOTE 2, NOTE 4	FTE	VREF=20Vp-p at 100kHz sine wave. Digital inputs at V <sub>IL</sub> .	4	All		15	mVp-p
Input Resistance	R <sub>IN</sub>		1,2,3	All	5	20	kΩ
Digital Input High Voltage	V <sub>IH</sub>		1,2,3	All	2.4		V
Digital Input Low Voltage	V <sub>IL</sub>		1,2,3	All		0.8	V
Digital Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> =0V or V <sub>DD</sub>	1,2,3	All		±1.0	μA
Supply Current	I <sub>DD</sub>	All digital inputs V <sub>IL</sub> or V <sub>IH</sub>	1,2,3	All		2.0	mA
Digital Input Capacitance NOTE 2	C <sub>IN</sub>		4	All		5	pF
Output Capacitance	C <sub>OUT1</sub>	Digital inputs at V <sub>IH</sub> Digital inputs at V <sub>IL</sub>	4	All		100 35	pF
	C <sub>OUT2</sub>	Digital inputs at V <sub>IH</sub> Digital inputs at V <sub>IL</sub>				35 100	

NOTE 1: V<sub>DD</sub>=+15V, V<sub>OUT1</sub>=V<sub>OUT2</sub>=0V; VREF=+10V, unless otherwise specified.

NOTE 2: Characteristics supplied for use as a typical design limit, but not production tested.

NOTE 3: Measured using internal feedback resistor and includes effect of leakage current and gain TC.

NOTE 4: Feedthrough error can be reduced by connecting the metal lid on the package to ground.

**ORDERING INFORMATION:**

	Package	Pkg. Code	
01	16 pin CERDIP	J16	MX7533SQ/883B
01	20 pin LCC	L20	MX7533SE/883B
02	16 pin CERDIP	J16	MX7533TQ/883B
02	20 pin LCC	L20	MX7533TE/883B
03	16 pin CERDIP	J16	MX7533UQ/883B
03	20 pin LCC	L20	MX7533UE/883B

**TERMINAL CONNECTIONS:**

	J16	L20
Pin		
1	OUT1	NC
2	OUT2	OUT2
3	GND	OUT1
4	D1(MSB)	GND
5	D2	D1(MSB)
6	D3	NC
7	D4	D2
8	D5	D3
9	D6	D4
10	D7	D5
11	D8	NC
12	D9	D6
13	D10(LSB)	D7
14	V <sub>DD</sub>	D8
15	VREF	D9
16	R <sub>FB</sub>	NC
17		D10(LSB)
18		V <sub>DD</sub>
19		VREF
20		R <sub>FB</sub>

## QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
  1. Test condition A, B, C, D.
  2. TA = +125°C, minimum.
  3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

**TABLE 2. ELECTRICAL TEST REQUIREMENTS**

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3
Group A Test Requirements Method 5005	1, 2, 3, 4**
Group C and D End-Point Electrical Parameters Method 5005	1

\* PDA applies to Subgroup 1 only.

\*\* Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 116 units.