

**SCOPE: CMOS QUAD SERIAL INTERFACE, 8-BIT D/A CONVERTER**

<u>Device Type</u>	<u>Generic Number</u>
01	MAX500B(x)/883B

**Case Outline(s).** The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
MAXIM SMD			
JE E	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
LP 2	CQCCI-N20	20 LEADLESS CHIP CARRIER	L20

**Absolute Maximum Ratings**

$V_{DD}$ to AGND .....	-0.3V, +17V
$V_{DD}$ to DGND .....	-0.3V, +17V
$V_{SS}$ to DGND.....	-7V, $V_{DD} + 0.3V$
$V_{DD}$ to $V_{SS}$ .....	-0.3V, +24V
Digital Input Voltage to DGND .....	-0.3V, ( $V_{DD} + 0.3V$ )
$V_{REF}$ to AGND .....	-0.3V, ( $V_{DD} + 0.3V$ )
$V_{OUT}$ to AGND <u>1/</u> .....	-0.3V, ( $V_{DD} + 0.3V$ )

Lead Temperature (soldering, 10 seconds) .....	+300°C
Storage Temperature .....	-65°C to +150°C

Continuous Power Dissipation .....	$T_A = +70^\circ C$
16 pin CERDIP(derate 10mW/°C above +70°C) .....	800mW
20 pin LCC(derate 9.1mW/°C above +70°C) .....	727mW
Junction Temperature $T_J$ .....	+150°C
Thermal Resistance, Junction to Case, $\theta_{JC}$	
16 pin CERDIP.....	40°C/W
20 pin LCC .....	50°C/W
Thermal Resistance, Junction to Ambient, $\theta_{JA}$ :	
16 pin CERDIP.....	20°C/W
20 pin LCC .....	110°C/W

**Recommended Operating Conditions**

Ambient Operating Range ( $T_A$ ) .....	-55°C to +125°C
Positive Supply Voltage ( $V_{DD}$ ) Single Supply .....	+14.25V to +15.75V
Positive Supply Voltage, ( $V_{DD}$ ) Dual Supply .....	+11.4V to +16.5V

1/ The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typical short circuit current to AGND is 25mA.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TABLE 1. ELECTRICAL TESTS:**

TEST	Symbol	CONDITIONS	Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T <sub>A</sub> ≤ +125 °C 2/ Unless otherwise specified					
<b>STATIC PERFORMANCE</b>		<b>DUAL SUPPLY SPECIFICATION</b>					
Resolution	N		1,2,3	All	8		Bits
Total unadjusted error	BT	V <sub>DD</sub> =15V±5%, V <sub>REF</sub> =10V	1,2,3	All		±2.0	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic	1,2,3	All		±1.0	LSB
Zero Code Error	BPOE		1 2,3	All		±20 ±30	mV
<b>REFERENCE INPUT</b>							
Reference Input Range	V <sub>REF</sub>		1,2,3	All	2	V <sub>DD</sub> -4	V
Reference Input Resistance	R <sub>IN</sub>	Pins V <sub>REF</sub> C and V <sub>REF</sub> D  Pins V <sub>REF</sub> A/B	1,2,3	All	11  5.5		kΩ
Reference Input Capacitance	C <sub>REFIN</sub>	Code dependent NOTE 3	4	All		100	pF
Channel-to-Channel Isolation		NOTE 3, 4	4	All	-60		dB
AC Feedthrough		NOTE 3, 4	4	All	-70		dB
<b>DIGITAL INPUTS</b>							
Input High Level Voltage	V <sub>IH</sub>		1,2,3	All	2.4		V
Input Low Level Voltage	V <sub>IL</sub>		1,2,3	All		0.8	V
Output High Level Voltage	V <sub>OH</sub>	I <sub>OUT</sub> =-1mA, SRO only	1,2,3	All	V <sub>DD</sub> -1		V
Output Low Level Voltage	V <sub>OL</sub>	I <sub>OUT</sub> =+1mA, SRO only	1,2,3	All	0.4		V
Input Leakage Current	I <sub>IL</sub>	Excluding $\overline{\text{LOAD}}$ , NOTE 5  $\overline{\text{LOAD}}$ =0V, NOTE 5	1,2,3	All		±1.0  30	μA
Digital Input Capacitance	C <sub>DIGIN</sub>	NOTE 5	1,2,3	All		8	pF
<b>DYNAMIC PERFORMANCE</b>							
Voltage Output Slew Rate		NOTE 3, NOTE 6	4	All	3		V/μs
V <sub>OUT</sub> Settling Time	t <sub>S</sub>	To 0.5 LSB, V <sub>REF</sub> =10V, V <sub>DD</sub> =+15V, 2kΩ in parallel with 100pF load. NOTE 3	9	All		4.0	μs
Output Load Resistance		V <sub>OUT</sub> =10V	1,2,3	All	2		kΩ
<b>POWER SUPPLIES</b>		<b>Dual Supply Specifications</b>					
Positive Supply Voltage	V <sub>DD</sub>	For specification performance	1,2,3	All	11.4	16.5	V
Positive Supply Current	I <sub>DD</sub>	Outputs unloaded	1 2,3	All		10 12	mA
Negative Supply Current	I <sub>SS</sub>	Outputs unloaded	1 2,3	All		-9 -10	mA
<b>SWITCHING CHARACTERISTICS</b>		<b>Three-Wire Mode</b> NOTE 6					
SDA valid to SCL setup	t <sub>S1</sub>	See Figure 5	9	All	150		ns
SDA valid to SCL hold	t <sub>H</sub>	See Figure 5	9	All	0		ns
SCL high time	t <sub>1</sub>		9	All	350		ns
SCL low time	t <sub>2</sub>		9	All	350		ns
$\overline{\text{LOAD}}$ pulse width	t <sub>LDW</sub>		9	All	150		ns

TEST	Symbol	CONDITIONS		Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C <=T <sub>A</sub> <= +125°C 2/ Unless otherwise specified						
LOAD delay from SCL	t <sub>LDS</sub>			9	All	150		ns
LDAC pulse width	t <sub>LDAC</sub>			9	All	150		ns
SRO output delay	t <sub>D1</sub>	C <sub>LOAD</sub> =50pF		9	All		150	ns
<b>Switching Characteristics</b>		<b>Two-Wire Mode</b> NOTE 6 Figure 6						
SDA valid to SCL setup	t <sub>S2</sub>	Start condition		9	All	100		ns
SCL valid to SDA setup	t <sub>S1</sub>	Start condition		9	All	150		ns
SDA valid to SCL hold	t <sub>H</sub>			9	All	0		ns
SCL high time	t <sub>1</sub>			9	All	350		ns
SCL low time	t <sub>2</sub>			9	All	350		ns
SDA valid to rising SCL	t <sub>S3</sub>			9	All	125		ns
LOAD pulse width	t <sub>LDW</sub>			9	All	150		ns
LDAC pulse width	t <sub>LDAC</sub>			9	All	150		ns
SRO output delay	t <sub>D1</sub>	C <sub>LOAD</sub> =50pF		9	All		150	ns
<b>STATIC PERFORMANCE</b> 7/		<b>SINGLE SUPPLY SPECIFICATION</b>						
Resolution	N			1,2,3	All	8		Bits
Total unadjusted error	BT	V <sub>DD</sub> =15V±5%, V <sub>REF</sub> =10V		1,2,3	All		±2.0	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic		1,2,3	All		±1.0	LSB
Zero Code Error	BPOE			1 2,3	All		±20 ±30	mV
<b>Power Supplies</b> 7/		<b>Single Supply Specifications</b>						
Positive Supply Voltage	V <sub>DD</sub>	For specification performance		1,2,3	All	14.25	15.75	V
Positive Supply Current	I <sub>DD</sub>	Outputs unloaded		1 2,3	All		10 12	mA

NOTE 2: V<sub>DD</sub>=+11.4V to 16.5V, V<sub>SS</sub>=-5V±10%, AGND=DGND=0V, and V<sub>REF</sub>=+2V to (V<sub>DD</sub>-4V).

NOTE 3: Guaranteed by design. Not production tested.

NOTE 4: V<sub>REF</sub>=10kHz, 10V peak-to-peak sine wave.

NOTE 5: LOAD has a weak internal pull-up resistor to V<sub>DD</sub>.

NOTE 6: Sample tested at +25°C to ensure compliance.

NOTE 7: V<sub>DD</sub>=+15V±5%, V<sub>SS</sub>=AGND=DGND=0V and V<sub>REF</sub>=10V.

Figures 5 and 6: See Commercial Datasheet.

	Package	ORDERING INFORMATION:	SMD Number
01	16 pin CERDIP	MAX500BMJE/883B	5962-9452702MEA
01	20 pin LCC	MAX500BMLP/883B	5962-9452702M2C

**TERMINAL CONNECTIONS**

	J16	20 LCC		J16	20 LCC
1	V <sub>OUTB</sub>	NC	11	SRO	SDA
2	V <sub>OUTA</sub>	V <sub>OUTB</sub>	12	V <sub>REFD</sub>	LOAD
3	V <sub>SS</sub>	V <sub>OUTA</sub>	13	V <sub>REFC</sub>	SCL
4	V <sub>REF A/B</sub>	V <sub>SS</sub>	14	V <sub>DD</sub>	NC
5	AGND	V <sub>REF A/B</sub>	15	V <sub>OUTD</sub>	SRO
6	DGND	AGND	16	V <sub>OUTC</sub>	V <sub>REFD</sub>
7	LDAC	NC	17		V <sub>REFC</sub>
8	SDA	NC	18		V <sub>DD</sub>
9	LOAD	DGND	19		V <sub>OUTD</sub>
10	SCL	LDAC	20		V <sub>OUTC</sub>

**QUALITY ASSURANCE**

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
  1. Test condition A, B, C, D.
  2. TA = +125°C, minimum.
  3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

**TABLE 2. ELECTRICAL TEST REQUIREMENTS**

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 4**, 5, 6, 9
Group A Test Requirements Method 5005	1, 2, 3, 4**, 5, 6, 9
Group C and D End-Point Electrical Parameters Method 5005	1

\* PDA applies to Subgroup 1 only.

\*\* Subgroup 4, Capacitance tests are performed initially and after any design changes.