SCOPE: CMOS VIDEO MULTIPLEXER/AMPLIFIER

Device Type	Generic Number
01	MAX453M(x)/883B
02	MAX455M(x)/883B
03	MAX452M(x)/883B
04	MAX454M(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JA	GDIP1-T8 or CDIP2-T8	8 LEAD CERDIP	J8
JD	GDIP1-T14 or CDIP2-T14	14 LEAD CERDIP	J14
LP	CQCC1-N20	20 Leadless Chip Carrier	L20

Absolute Maximum Ratings

Total Supply Voltage (V+ to V-) 12V
Positive Supply Voltage, V+ (rel. GND) ..... +12V
Negative Supply Voltage, V- (rel. GND) ..... -12V
Analog Input Voltages: .....(V+) +0.3V to (V-) -0.3V
Digital Input Voltages: ..... -0.3V to (V+) +0.3V
Duration of Output Short-Circuit to ground ..... Indefinite
Input Current, power on or off:
Digital Inputs ..... ±20mA
All other pins ..... ±50mA
Short-Circuit Duration, T_{OUT}..... Continuous
Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +160°C

Continuous Power Dissipation ..... T_A=+70°C
8 pin CERDIP(derate 8.0mW/°C above +70°C) 640mW
14 pin CERDIP(derate 9.1mW/°C above +70°C) 727mW
20 pin CERDIP(derate 11.1mW/°C above +70°C) 889mW
20 pin LCC(derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
8 pin CERDIP..... 55°C/W
14 pin CERDIP..... 55°C/W
20 pin CERDIP..... 40°C/W
20 pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
8 pin CERDIP..... 125°C/W
14 pin CERDIP..... 110°C/W
20 pin CERDIP..... 90°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Input Voltage Range ..... -2V to +2V
Operating Supply Voltage ..... ±4.5Vdc to ±5.5V dc

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
VIDEO AMPLIFIER							
Input Voltage Range	V_{IN}		1,2,3	All	-2.0	2.0	V
Input Offset Voltage	V_{OS}		1 2,3	All		5.0 10.0	mV
Input Bias Current	IB	NOTE 2	1 2,3	All		10 500	nA
Open-Loop Voltage Gain	A_{VOL}	R_L=1000Ω R_L=150Ω R_L=75Ω	1	All	180 45 25		V/V
Common-Mode Rejection Ratio	CMRR	-2V≤V_{IN}≤+2V	1	All	60		dB
Power Supply Rejection Ratio	PSRR	±4.5V to ±5.5V	1 2,3	All	54 48		dB
Slew Rate	SR	NOTE 3	1	All	150		V/µs
VIDEO AMPLIFIER							
-3dB Bandwidth	GBW1 GBW2	AV=0dB, RL=75Ω, NOTE 3 AV=6dB, RL=150Ω, NOTE 3	1	All	30 25		MHz
Full-Scale Output Current	I_{OUT}		1	All	±14		mA
Output Voltage Swing	V_{OUT}		1	All	±2.1		V
Input noise, dc to 40 MHz	Vn	NOTE 3	1	All		0.5	mVrms
Operating Supply Voltage	V+, V-		1,2,3	All	±4.5	±5.5	V
Supply Current	I_{CC}	V_{IN}=0V	1 2,3	All	20 17	30 32	mA
MULTIPLEXER							
Input Voltage Range	V_{IN}		1,2,3	02,03,04	-2.0	2.0	V
OFF Input Leakage Current	I_{OFF}	NOTE 4	1 2,3	02,03,04		10 500	nA
Logic Low Threshold	V_{IL}		1,2,3	02,03,04		0.8	V
Logic High Threshold	V_{IH}		1,2,3	02,03,04	2.4		V
Input Pullup/down Current	I_{IL}/I_{IH}		1	02,03,04		20	µA
Turn-On Time	t_{ON}	NOTE 3	9	02,03,04		120	ns
Turn-Off Time	t_{OFF}	NOTE 3	9	02,03,04		60	ns
Break-Before-Make Delay	t_D	NOTE 3	9	02,03,04	10		ns
Channel "On" Capacitance	C_{ON}	NOTE 3	9	02,03,04		15	pF
Channel "Off" Capacitance	C_{OFF}	NOTE 3	9	02,03,04		12	pF
Channel "Off" Isolation Delay	OIRR	fIN=4MHz, RS=75Ω, NOTE 3, Channel 2 to Channel 3 All other channels	9	02,03,04	 45 60		dB

NOTE 1: V+=+5V, V-=-5V, -2V≤V_{IN}≤+2V, Output Load Resistor=150Ω.
NOTE 2: Input bias includes the multiplexer's On-state leakage current.
NOTE 3: Guaranteed by design.
NOTE 4: Guaranteed over the voltage range, V-≤V_{IN}≤V+

TERMINAL CONNECTIONS FOR 01, 02, 03, 04

	MAX452	MAX453	MAX454	MAX455
1	NC	A0	A1	A2
2	NC	GND	A0	A1
3	V-	V-	GND	A0
4	NC	IN0	V-	GND
5	+IN	+IN	NC	IN0
6	V+	V+	NC	V-
7	-IN	-IN	IN0	IN1
8	V_{OUT}	V_{OUT}	IN1	NC
9			NC	IN2
10			IN2	IN3
11			IN3	IN4
12			V+	NC
13			-IN	IN5
14			V_{OUT}	NC
15				IN6
16				NC
17				IN7
18				V+
19				-IN
20				V_{OUT}

	Package	**ORDERING INFORMATION:**	**SMD Number**
01	8 pin CERDIP	MAX453MJA/883B	5962-9451201MPA
01	20 pin LCC	MAX453MLP/883B	5962-9451201M2C
02	20 pin CERDIP	MAX455MJP/883B	5962-9451202MRA
02	20 pin LCC	MAX455MLP/883B	5962-9451202M2C
03	8 pin CERDIP	MAX452MJA/883B	5962-9451203MPA
03	20 pin LCC	MAX452MLP/883B	5962-9451203M2C
04	14 pin CERDIP	MAX454MJD/883B	5962-9451204MCA
04	20 pin LCC	MAX454MLP/883B	5962-9451204M2C

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9**
Group A Test Requirements Method 5005	1, 2, 3, 9**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Guaranteed by design.