SCOPE: Serial-Output, 250 ksps 12-Bit ADC with Track/Hold and Reference

Device Type	Generic Number
01	MAX176AM(x)/883B
02	MAX176BM(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JA	GDIP1-T8 or CDIP2-T8	8 LEAD CERDIP	J08
LP	CQCC1-N20	20-Pin LCC	L20

Absolute Maximum Ratings

V_{DD} to GND ..... -0.3V to +7V
V_{SS} to GND ..... +0.3V to -17V
AIN to GND ..... ±15V
Digital Input Voltage to GND ..... -0.3V to (V_{DD} +0.3V)
Digital Output Voltage to GND ..... -0.3V to (V_{DD} +0.3V)

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +160°C

Continuous Power Dissipation ..... T_A=+70°C
8 pin CERDIP(derate 8.0mW/°C above +70°C) 640mW
20 pin LCC(derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
8 pin CERDIP..... 55°C/W
20 pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
8 pin CERDIP..... 125°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Supply Voltage (V_{CC})..... +4.75V to +5.25V
Supply Voltage (V_{EE})..... -11.4V to -15.75V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V±5%, V_{SS}=-11.4V to -15.75V, f_{CLK}=3MHz Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
ACCURACY							
Resolution	RES	Guaranteed Monotonic over temp	1,2,3	All	12		Bits
Differential Nonlinearity	DNL	NOTE 1	1,2,3	01 02		±0.75 ±1.0	LSB
Integral Nonlinearity	INL	NOTE 1	1 2,3	01		±0.5 ±0.75	LSB
Integral Nonlinearity	INL	NOTE 1	1,2,3	02		±1.0	LSB
Offset Error	V_{OS}	NOTE 1, NOTE 2 For JA pkg. NOTE 1, NOTE 2 For LP pkg.	1,2,3	All		±3.0 ±5.0	LSB
Full-Scale Error	AE	NOTE 3	1	All		±8.0	LSB
ANALOG INPUTS							
Input Voltage Range			1,2,3	All	-5	+5	V
Input Current			1,2,3	All		2.5	mA
Input Capacitance		Note 4	4	All		10	pF
INTERNAL REFERENCE							
V_{REF} Output Voltage			1,2,3	All	-4.98	-5.02	V
V_{REF} Output Tempco		NOTE 5	1,2,3	All		±40	ppm/°C
Load Regulation		NOTE 6 0mA<I_L<5mA	1,2,3	All		5	mW
POWER SUPPLY REJECTION							
Positive Supply Rejection	V_{DD}	FS change, V_{SS}=-15V or -12V, V_{DD}=5V±5%	1,2,3	All		±0.5	LSB
Negative Supply Rejection	V_{SS}	FS change, V_{SS}=-15V or -12V V_{DD}=5V | V_{SS}=-15V or -12V	1,2,3	All		±0.5 ±0.5	LSB
LOGIC INPUTS		**(CLK, CONVST)**					
Logic High Voltage	V_{IH}		1,2,3	All	+2.4		V
Logic Low Voltage	V_{IL}		1,2,3	All		+0.8	V
Input Current	I_{IN}	V_{IN}=0V or V_{DD}	1,2,3	All		±5	µA
Input Capacitance	C_{IN}	NOTE 4	4	All		10	pF
LOGIC OUTPUTS							
Output High Voltage	V_{OH}	Data I_{SOURCE}=200µA	1,2,3	All	4.0		V
Output Low Voltage	V_{OL}	Data I_{SINK}=1.6mA	1,2,3	All		0.4	V
POWER REQUIREMENTS							
Positive Supply Current	I_{DD}	CONVST=V_{DD}, AIN=0V	1,2,3	All		8	mA
Negative Supply Current	I_{SS}	CONVST=V_{DD}, AIN=0V	1,2,3	All		-11	mA
TIMING NOTE 7							
Clock Pulse Width	t_{CH} t_{CL}	Clock High Clock Low	9,10,11	All	50 100		ns
CONVST Pulse Width	t_{SH} t_{SL}	Clock High Clock Low	9,10,11	All	50 150		ns
CONVST to Clock Skew	t_{SC0} t_{SC1}	Leading clock Leading clock +1	9,10,11	All	 160	30 	ns
Clock to Data Delay	t_{PD}	NOTE 8	9,10,11	All	20	170	ns
Acquisition Time	t_{AQ}	FS change at AIN NOTE 4	9,10,11	All		400	ns
CONVST Rise Time		NOTE 4	9,10,11	All		100	ns
Output Float Delay		NOTE 9	9,10,11	All		120	ns

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V±5%, V_{SS}=-11.4V to -15.75V, f_{CLK}=3MHz Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
DYNAMIC TESTS		(AIN=10Vp-p, f_{AIN}=50.17kHz, $f_{SAMPLING}$=200ksps					
Signal -to-Noise Plus Distortion	S/(N+D)		9,10,11	All	70		dB
Total Harmonic Distortion	THD		9,10,11	All		-80	dB
Peak Harmonic or Spurious Noise	SFDR		9,10,11	All		-80	dB
Input Slew Rate			9,10,11	All	1.5		V/µs
Conversion Time	t_{CONV}	14 clock cycles	9,10,11	All		4.7	µs
Acquisition Time	t_{AQ}	NOTE 4	9,10,11	All		400	ns
Clock Frequency	f_{CLK}		9,10,11	All	0.1	3.0	MHz

NOTE 1: These tests are performed at V_{DD}=+5V, V_{SS}=-15V. Operation over supply is guaranteed by supply rejection tests.

NOTE 2: Offset measured at 0...00 to 0...01 digital output code.

NOTE 3: FS=+5.000V. Ideal last code transition = FS-3/2 LSB. Adjusted for offset error.

NOTE 4: Guaranteed by design. Not subject to test.

NOTE 5: V_{REF} Tempco=$\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from 25°C to +125°C or -55°C.

NOTE 6: Output current should not change during conversion.

NOTE 7: Timing Specifications are 100% tested. All input control signals are specified with tR=tF=5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. Output delays are measured to 0.8V if going low and 2.4V if going high.

NOTE 8: DATA pin is loaded with 50pF to GND.

NOTE 9: DATA pin is loaded with 10pF‖3kΩ. Defined as the time required for data lines to change 0.5V.

TERMINAL CONNECTIONS:

	20 PIN LCC	
1	V_{DD}	Positive Supply, +5V
2	V_{DD}	Positive Supply, +5V
3	NC	No Connect
4	NC	No Connect
5	A_{IN}	Analog Input, 0V to +5V Unipolar
6	V_{REF}	Reference Voltage Output, -5.0V
7	NC	No Connect
8	NC	No Connect
9	GND	Ground
10	GND	Ground
11	GND	Ground
12	DATA	Serial Data Output
13	NC	No Connect
14	NC	No Connect
15	NC	No Connect
16	CLOCK	Clock Input, TTL/+5V CMOS compatible.
17	CONVST	Conversion start input for three wire mode. End-of-conversion output for two wire mode.
18	NC	No Connect
19	NC	No Connect
20	V_{SS}	Negative Supply, -12V or -15V.

TERMINAL CONNECTIONS:

	8 PIN CERDIP	
1	V_{DD}	Positive Supply, +5V
2	A_{IN}	Analog Input, 0V to +5V Unipolar
3	V_{REF}	Reference Voltage Output, -5.0V
4	GND	Ground
5	DATA	Serial Data Output
6	CLOCK	Clock Input, TTL/+5V CMOS compatible.
7	CONVST	Conversion start input for three wire mode. End-of-conversion output for two wire mode.
8	V_{SS}	Negative Supply, -12V or -15V.

Package	**ORDERING INFORMATION:**	
8 pin CERDIP	MAX176AMJA/883B	MAX176BMJA/883B
20 pin LCC	MAX176AMLP/883B	MAX176BMLP/883B

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 4*, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 4*, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Guaranteed by design.