SCOPE: CMOS, 8-BIT, 8-CHANNEL DATA ACQUISITION SYSTEM

Device Type	Generic Number
01	MAX170DM(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JA	GDIP1-T8 or CDIP2-T8	8 LEAD CERDIP	J08

Absolute Maximum Ratings

V_{DD} to AGND ..... -0.3V to +7V
V_{SS} to DGND..... +0.3V to -17V
AIN to AGND ..... ±15V
Clock Input Voltage to DGND ..... -0.3V to V_{DD}
Digital Input Voltage to GND ..... -0.3V to (V_{DD} +0.3V)
Digital Output Voltage to GND ..... -0.3V to (V_{DD} +0.3V)

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +160°C

Continuous Power Dissipation ..... T_A=+70°C
8 pin CERDIP(derate 8.0mW/°C above +70°C) 640mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
8 pin CERDIP..... 55°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
8 pin CERDIP..... 125°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Supply Voltage (V_{DD})..... +4.75V to +5.25V
Supply Voltage (V_{SS})..... -11.4V to -15.75V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V±5%, V_{SS}=-11.4V to -15.75V, f_{CLK}=2.5MHz Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
ACCURACY							
Resolution	RES			All	12		Bits
Integral Nonlinearity	INL		1,2,3	All		±1.0	LSB
Differential Nonlinearity	DNL	Guaranteed Monotonic over Temperature	1,2,3	All		±1.0	LSB
Offset Error	V_{OS}	NOTE 1	1,2,3	All		±5.0	LSB
Full-Scale Error	AE	NOTE 2	1	All		±5.0	LSB
Full-Scale Tempco		NOTES 3,4	1,2,3	All		±45	ppm/°C
Conversion Time	t_{CONV}	14 Clock cycles	9,10,11	All		5.6	µs
ANALOG INPUTS	RM						
Input Voltage Range			1,2,3	All	0	+5	V
Input Current		AIN=0V to +5V	1,2,3	All		3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage			1	All	-5.2	-5.3	V
Output Current Sink Capability		NOTE 5	1,2,3	All		5.0	mA
LOGIC INPUTS							
Logic High Threshold	V_{IH}		1,2,3	All	+2.4		V
Logic Low Threshold	V_{IL}		1,2,3	All		+0.8	V
Input Current	I_{IN}	AIN=0V to $V_{DD,}$ Clock AIN=0V to $V_{DD,}$ $\overline{CONVST/EOC}$	1,2,3	All	 ±200	±10 ±500	µA
Input Capacitance	C_{IN}	NOTE 6	4	All		10	pF
LOGIC OUTPUTS							
Output High Voltage	V_{OH}	Data I_{SOURCE}=200µA	1,2,3	All	4.0		V
Output Low Voltage	V_{OL}	Data I_{SINK}=1.6mA Data I_{SINK}=6.0mA	1,2,3	All		0.4 1.5	V
POWER REQUIREMENTS							
Positive Supply Current	I_{DD}	$\overline{CONVST/EOC}$=V_{DD}, AIN=0V	1,2,3	All		8	mA
Negative Supply Current	I_{SS}	$\overline{CONVST/EOC}$=V_{DD}, AIN=0V	1,2,3	All		-11	mA
TIMING							
Clock Pulse Width	t_{CH} t_{CL}	Clock High Clock Low	9	All	40 60		ns
$\overline{CONVST/EOC}$ Pulse Width	t_{SH} t_{SL}	$\overline{CONVST/EOC}$ High $\overline{CONVST/EOC}$ Low	9	All	40 60		ns
$\overline{CONVST/EOC}$ to Clock Skew	t_{SC0} t_{SC1}	Leading clock Leading clock +1	9	All	 275	50	ns
Clock to Data Delay	t_{PD}		9	All	25	155	ns

NOTE 1: Typical change over temperature is ±1LSB.
NOTE 2: FS=+5.000V. Ideal last code transition = FS-3/2 LSB. Adjusted for offset error.
NOTE 3: Full scale Tempco=ΔFS/ΔT, where ΔFS is full scale change from 25°C to +125°C or -55°C.
NOTE 4: Includes internal reference drift.
NOTE 5: Output current should not change during conversion.
NOTE 6: Guaranteed by design, not subject to test.
NOTE 7: Timing Specifications are sample tested at 25°C to ensure compliance. Guaranteed but not tested over temperature. All input control signals are specified with tR=tF=5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Package	**ORDERING INFORMATION:**
8 pin CERDIP	MAX170DMJA/883B

TERMINAL CONNECTIONS:

	8 PIN CERDIP	
1	V_{DD}	Positive Supply, +5V
2	A_{IN}	Analog Input, 0V to +5V Unipolar
3	V_{REF}	Reference Voltage Output, -5.25V
4	GND	Ground
5	DATA	Serial Data Output
6	CLOCK	Clock Input, TTL/+5V CMOS compatible.
7	$\overline{\text{CONVST}}$/EOC	Conversion start input for three wire mode. End-of-conversion output for two wire mode.
8	V_{SS}	Negative Supply, -12V or -15V.

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10**, 11**
Group A Test Requirements Method 5005	1, 2, 3, 9, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Guaranteed but not tested.