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14-Bit GMSL Serializer with High-Immunity/ Bandwidth Mode and Coax/STP Cable Drive

MAX96701A

General Description

The MAX96701A is a compact serializer in a 4mm x 4mm TQFN package especially suited for automotive camera applications. In high-bandwidth mode, the parallel-clock maximum is 116MHz for 12-bit linear or combined HDR data types.

The embedded control channel operates at 9.6kbps to 1Mbps in I²C mode, allowing programming of serializer, deserializer (SerDes), and camera registers independent of video timing.

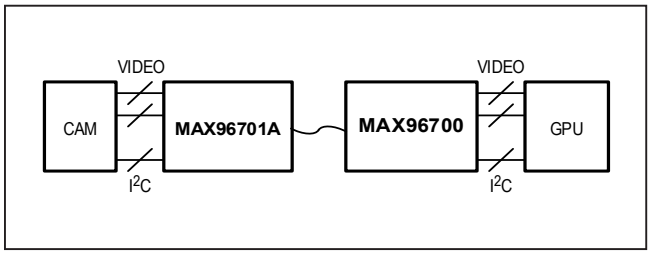
For driving longer cables, the IC has programmable pre/deemphasis. Programmable spread spectrum is available on the serial output. The serial output meets ISO 10605 and IEC 61000-4-2 ESD standards. The supply range is 1.7V to 1.9V.

The MAX96701A is available in a 24-pin TQFN package with 0.5mm lead pitch, and operates over the -40°C to +115°C temperature range.

Applications

- Automotive Camera Applications

Simplified Block Diagram



***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Ideal for Safety Camera Applications
  - Works with Low-Cost 50Ω Coax (100Ω STP) Cables
  - Error Detection of Video/Control Data
  - High-Immunity Mode for Robust Control-Channel EMC Tolerance
  - Retransmission of Control Data Upon Error Detection
  - Best-in-Class Supply Current: 88mA (max)
  - Pre/Deemphasis Allows 15m Cable at Full Speed
  - 24-Pin (4mm x 4mm) TQFN Package with 0.5mm Lead Pitch
- High-Speed Data Serialization for Megapixel Cameras
  - Up to 1.74Gbps Serial-Bit Rate
  - 12.5MHz to 116MHz x 12-Bit + H/V Data
- Multiple Modes for System Flexibility
  - 9.6kbps to 1Mbps Control Channel in I²C Mode (with Clock Stretch)
  - Crosspoint Switch Accepts Any Input Bitmap
  - Modes for Encoded VSYNC and HSYNC
- Reduces EMI and Shielding Requirements
  - Programmable Output Spread Spectrum
  - Tracks Spread Spectrum Applied at the Parallel Input
  - 1.7V to 1.9V I/O Supply
- Peripheral Features for Camera Power-Up and Verification
  - Built-In PRBS Generator for BER Testing
  - Dedicated GPO for Camera Frame-Sync Trigger and Other Uses
  - Remote/Local Wake-Up from Sleep Mode
- Meets AEC-Q100 Automotive Specification
  - -40°C to +115°C Operating Temperature
  - ±8kV Contact and ±15kV Air IEC 61000-4-2 and ISO 10605 ESD Protection

19-101025; Rev 1; 7/26

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Absolute Maximum Ratings

AVDD to GND* .....-0.5V to +1.9V
DVDD to GND*.....-0.5V to +1.9V
OUT+, OUT- to GND*.....-0.5V to +1.9V
All Other Pins to GND*.....-0.5V to (DVDD + 0.5V)
OUT+, OUT- Short Circuit to Ground or Supply.....Continuous

Continuous Power Dissipation, T_A = +70°C
TQFN (derate 27.8 mW/°C above +70°C) 2222.2mW
Operating Temperature Range.....-40°C to +115°C
Junction Temperature.....+150°C
Storage Temperature Range..... -40°C to +150°C
Soldering Temperature (reflow).....+260°C

**EP externally connected to GND.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

24-Pin TQFN-EP

Package Code	**T2444+4**
Outline Number	**21-0139**
Land Pattern Number	**90-0022**
Single-Layer Board:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	48
Junction-to-Case Thermal Resistance (θ_{JC})	3
Four-Layer Board:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	36
Junction-to-Case Thermal Resistance (θ_{JC})	3

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, R_L = 100Ω ±1% (differential), T_A = -40°C to +115°C, EP connected to GND, typical values are at V_{DVDD} = V_{AVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (DIN_, PCLKIN, HS, VS, HIM, MS)						
High-Level Input Voltage	V_{IH}		0.65 x V_{DVDD}			V
Low-Level Input Voltage	V_{IL}				0.35 x V_{DVDD}	V
Input Current	I_{IN}	V_{IN} = 0 to V_{DVDD}	-20		+20	µA
SINGLE-ENDED OUTPUT (GPO)						
High-Level Output Voltage	V_{OH}	I_{OH} = -2mA	V_{DVDD} - 0.2			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 2mA			0.2	V
Output Short-Circuit Current	I_{OS}	V_O = 0V	3	12	21	mA
I^2C and GENERAL-PURPOSE I/Os (SDA, SCL, GPIO_) with OPEN-DRAIN OUTPUTS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DVDD}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input Current	I_{IN}	V_{IN} = 0 to V_{DVDD} (Note 2), SDA, SCL	-110		+5	µA
		V_{IN} = 0 to V_{DVDD} (Note 2), GPIO_	-80		+5	
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Input Capacitance	C_{IN}	Each pin (Note 3)			10	pF

DC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, R_L = 100Ω ±1% (differential), T_A = -40°C to +115°C, EP connected to GND, typical values are at V_{DVDD} = V_{AVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL OUTPUTS (OUT+, OUT-)						
Differential Output Voltage	V_{OD}	Preemphasis off, high drive (Figure 1)	300	400	500	mV
		3.3dB preemphasis, high drive (Figure 2)	350		610	
		3.3dB deemphasis, high drive (Figure 2)	240		425	
Change in V_{OD} Between Complementary Output States	ΔV_{OD}				25	mV
Output Offset Voltage (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off	1.1	1.4	1.56	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}				25	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V	-60			mA
		V_{OUT+} or V_{OUT-} = 1.9V			25	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V			25	mA
Output-Termination Resistance (Internal)	R_O	From OUT+ or OUT- to AVDD	45	54	63	Ω
REVERSE CONTROL-CHANNEL RECEIVER OUTPUTS (OUT+, OUT-)						
High-Switching Threshold	V_{CHR}	Legacy			27	mV
		High immunity			40	
Low-Switching Threshold	V_{CLR}	Legacy	-27			mV
		High immunity	-40			
SINGLE-ENDED SERIAL OUTPUTS (OUT+ or OUT-)						
Single-Ended Output Voltage	V_O	Preemphasis off, high drive (Figure 3)	375	500	625	mV
		3.3dB preemphasis, high drive (Figure 2)	435		765	
		3.3dB deemphasis, high drive (Figure 2)	300		535	
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V	-69			mA
		V_{OUT+} or V_{OUT-} = 1.9V			32	
Output-Termination Resistance (Internal)	R_O	From OUT+ or OUT- to AVDD	45	54	63	Ω

DC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, R_L = 100Ω ±1% (differential), T_A = -40°C to +115°C, EP connected to GND, typical values are at V_{DVDD} = V_{AVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Current, Worst-Case Pattern (Figure 4)	I_{WCS}	f_{PCLKIN} = 116MHz, HIBW = 0, BWS = 0, default register values, AVDD + DVDD (1.9V)		66	88	mA
		f_{PCLKIN} = 116MHz, HIBW = 1, BWS = 0, default register values, AVDD + DVDD (1.9V)		63	83	
		f_{PCLKIN} = 87MHz, BWS = 1, default register values, AVDD + DVDD (1.9V)		62	83	
Sleep-Mode Supply Current	I_{CCS}	Wake-up receiver enabled		40	100	µA
ESD PROTECTION						
OUT+, OUT- (Note 4)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF, Contact Discharge		±8		
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF, Air Discharge		±15		
		ISO 10605, R_D = 2kΩ, C_S = 330pF, Contact Discharge		±8		
		ISO 10605, R_D = 2kΩ, C_S = 330pF, Air Discharge		±15		
All Other Pins (Note 5)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±4		kV

AC Electrical Characteristics

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, R_L = 100Ω ±1% (differential), T_A = -40°C to +115°C, EP connected to GND, typical values are at V_{DVDD} = V_{AVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PARALLEL CLOCK INPUT (PCLKIN)						
Clock Frequency	f_{PCLKIN}	BWS = 0, HIBW = 0, single input	16.66		58	MHz
		BWS = 0, HIBW = 1, single input	36.66		58	
		BWS = 1, single input	12.5		43.5	
		BWS = 0, HIBW = 0, double input	33.32		116	
		BWS = 0, HIBW = 1, double input	73.33		116	
		BWS = 1, double input	25		87	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Note 3, Figure 5)	35	50	65	%
Clock Transition Time	t_R, t_F	(Note 3, Figure 5)			4	ns
Clock Jitter	t_J	1.74Gbps bit rate, 300kHz sinusoidal jitter (Note 3)			800	ps
I²C PORT TIMING						
I²C Bit Rate			9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to DVDD	20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to DVDD	20		150	ns
I²C TIMING (Figure 6)						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2CMSTBT = 010, I2CSLVSH = 10)	9.6		100	kHz
		Mid f_{SCL} range: (I2CMSTBT 101, I2CSLVSH = 01)	> 100		400	
		High f_{SCL} range: (I2CMSTBT = 111, I2CSLVSH = 00)	> 400		1000	
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, Low	4			µs
		f_{SCL} range, Mid	0.6			
		f_{SCL} range, High	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, Low	4.7			µs
		f_{SCL} range, Mid	1.3			
		f_{SCL} range, High	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, Low	4			µs
		f_{SCL} range, Mid	0.6			
		f_{SCL} range, High	0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, Low	4.7			µs
		f_{SCL} range, Mid	0.6			
		f_{SCL} range, High	0.26			

AC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, R_L = 100Ω ±1% (differential), T_A = -40°C to +115°C, EP connected to GND, typical values are at V_{DVDD} = V_{AVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, Low	0			ns
		f_{SCL} range, Mid	0			
		f_{SCL} range, High	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, Low	250			ns
		f_{SCL} range, Mid	100			
		f_{SCL} range, High	50			
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range, Low	4			µs
		f_{SCL} range, Mid	0.6			
		f_{SCL} range, High	0.26			
Bus-Free Time	t_{BUF}	f_{SCL} range, Low	4.7			µs
		f_{SCL} range, Mid	1.3			
		f_{SCL} range, High	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, Low			3.45	µs
		f_{SCL} range, Mid			0.9	
		f_{SCL} range, High			0.45	
Data Valid-Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, Low			3.45	µs
		f_{SCL} range, Mid			0.9	
		f_{SCL} range, High			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, Low			50	ns
		f_{SCL} range, Mid			50	
		f_{SCL} range, High			50	
Capacitive Load of Each Bus Line	C_B	(Note 3)			100	pF
SWITCHING CHARACTERISTICS (Note 3)						
Differential/Single-Ended Output Rise/Fall Time	t_R, t_F	20% to 80%, V_{OD}, 400mV differential R_L = 100Ω, 500mV single-ended R_L = 50Ω, serial bit rate = 1.74Gbps			250	ps
Total Serial-Output Jitter (Differential Output)	t_{TSOJ1}	1.74Gbps PRBS, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 7)		0.25		UI
Deterministic Serial-Output Jitter (Differential Output)	t_{DSOJ2}	1.74Gbps PRBS, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 7)		0.15		UI
Total Serial-Output Jitter (Single-Ended Output)	t_{TSOJ1}	1.74Gbps PRBS, measured at V_O/2, preemphasis disabled (Figure 3)		0.25		UI
Deterministic Serial-Output Jitter (Single-Ended Output)	t_{DSOJ2}	1.74Gbps PRBS, measured at V_O/2, preemphasis disabled (Figure 3)		0.15		UI
Parallel Data-Input Setup Time	t_{SET}	(Figure 8)	3			ns

AC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, R_L = 100Ω ±1% (differential), T_A = -40°C to +115°C, EP connected to GND, typical values are at V_{DVDD} = V_{AVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

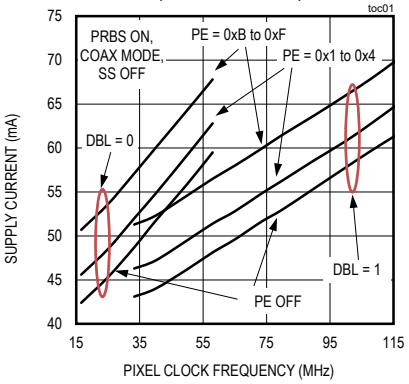
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Parallel Data Input Hold Time	t_{HOLD}	(Figure 8) (Note 3)	1			ns
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (Figure 9)			350	µs
Serializer Delay	t_{SD}	Spread spectrum enabled (Figure 10) (Notes 3, 6)			2065	Bits
		Spread spectrum disabled (Figure 10) (Notes 3, 6)			1095	
Link Start Time	t_{LOCK}	(Figure 11)			2	ms
Power-Up Time	t_{PU}	(Figure 12)			7	ms

Note 1: Limits are 100% production tested at T_A = +115°C. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.
Note 2: I_{IN} min is due to voltage drop across the internal pullup resistor.
Note 3: Not production tested. Guaranteed by design.
Note 4: Specified pin to ground.
Note 5: Specified pin to all supply/ground.
Note 6: Measured in serial link bit times. Bit time = 1/(30 x f_{PCLKIN}) for BWS = 0; bit time = 1/(40 x f_{PCLKIN}) for BWS = 1.

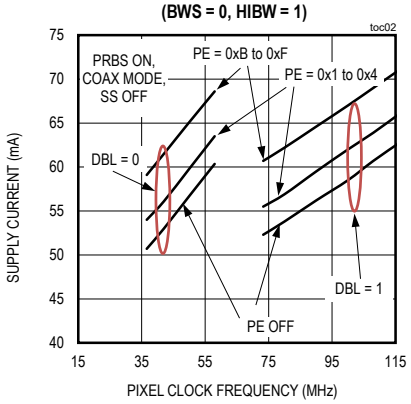
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = 1.8V, T_A = +25°C, unless otherwise noted.)

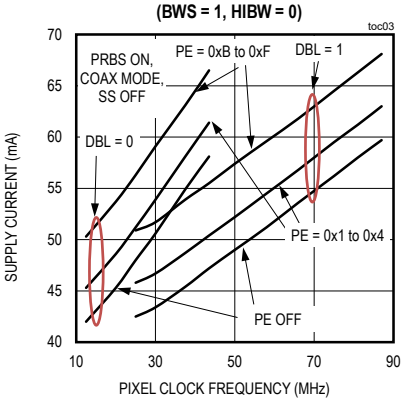
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 0, HIBW = 0)



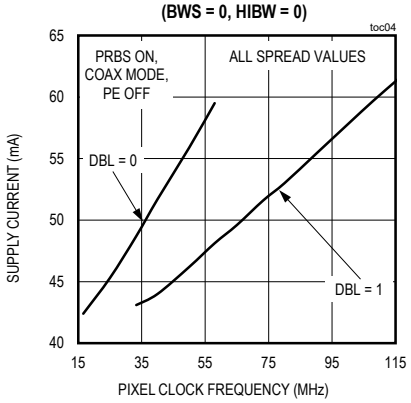
SUPPLY CURREN vs. PIXEL CLOCK FREQUENCY (BWS = 0, HIBW = 1)



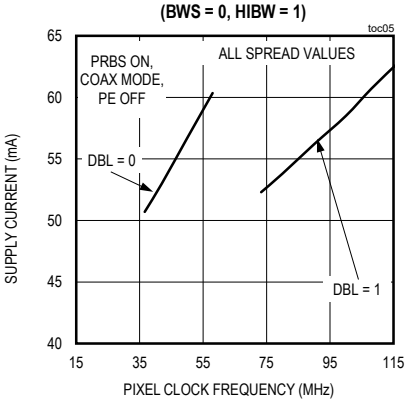
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 1, HIBW = 0)



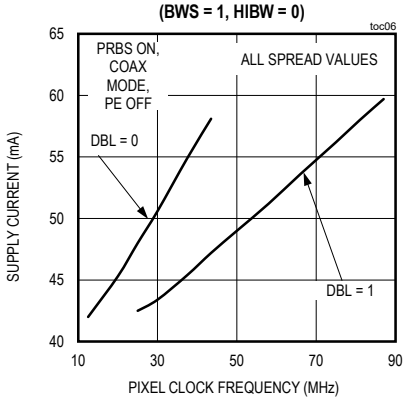
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 0, HIBW = 0)



SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 0, HIBW = 1)



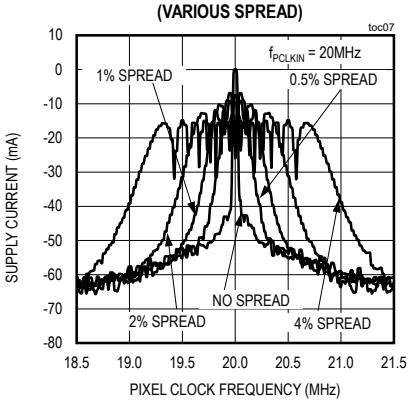
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 1, HIBW = 0)



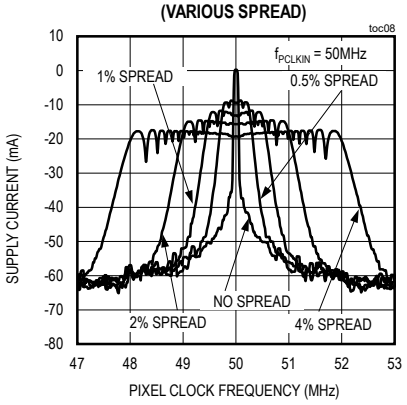
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.8V, T_A = +25°C, unless otherwise noted.)

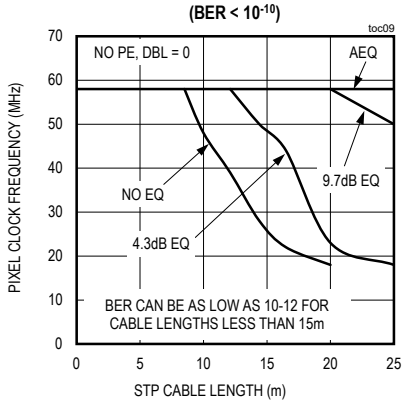
OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY (VARIOUS SPREAD)



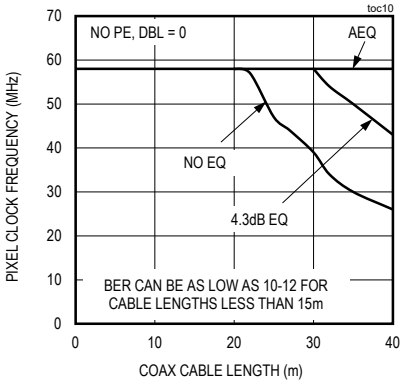
OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY (VARIOUS SPREAD)



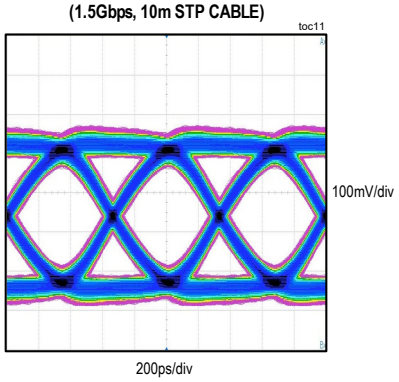
MAXIMUM PIXEL CLOCK FREQUENCY vs. STP CABLE LENGTH (BER < 10^{-10})



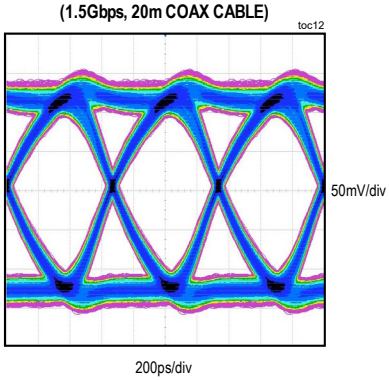
MAXIMUM PIXEL CLOCK FREQUENCY vs. COAX CABLE LENGTH (BER < 10^{-10})



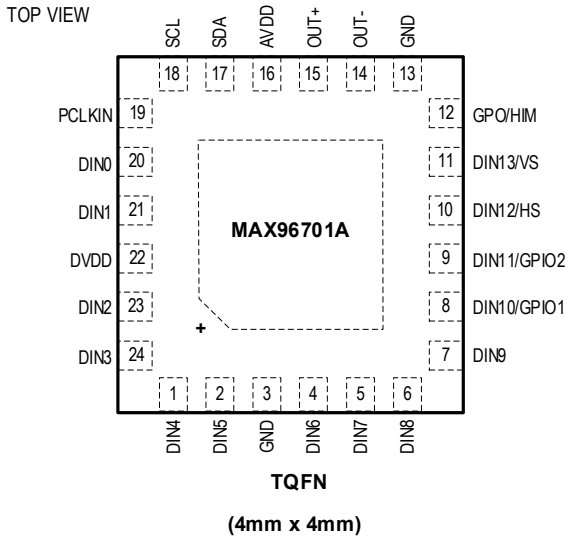
SERIAL LINK SWITCHING PATTERN WITH 4.4dB PREEMPHASIS (1.5Gbps, 10m STP CABLE)



SERIAL LINK SWITCHING PATTERN WITH 3.3dB PREEMPHASIS (1.5Gbps, 20m COAX CABLE)



Pin Configuration



TQFN

(4mm x 4mm)

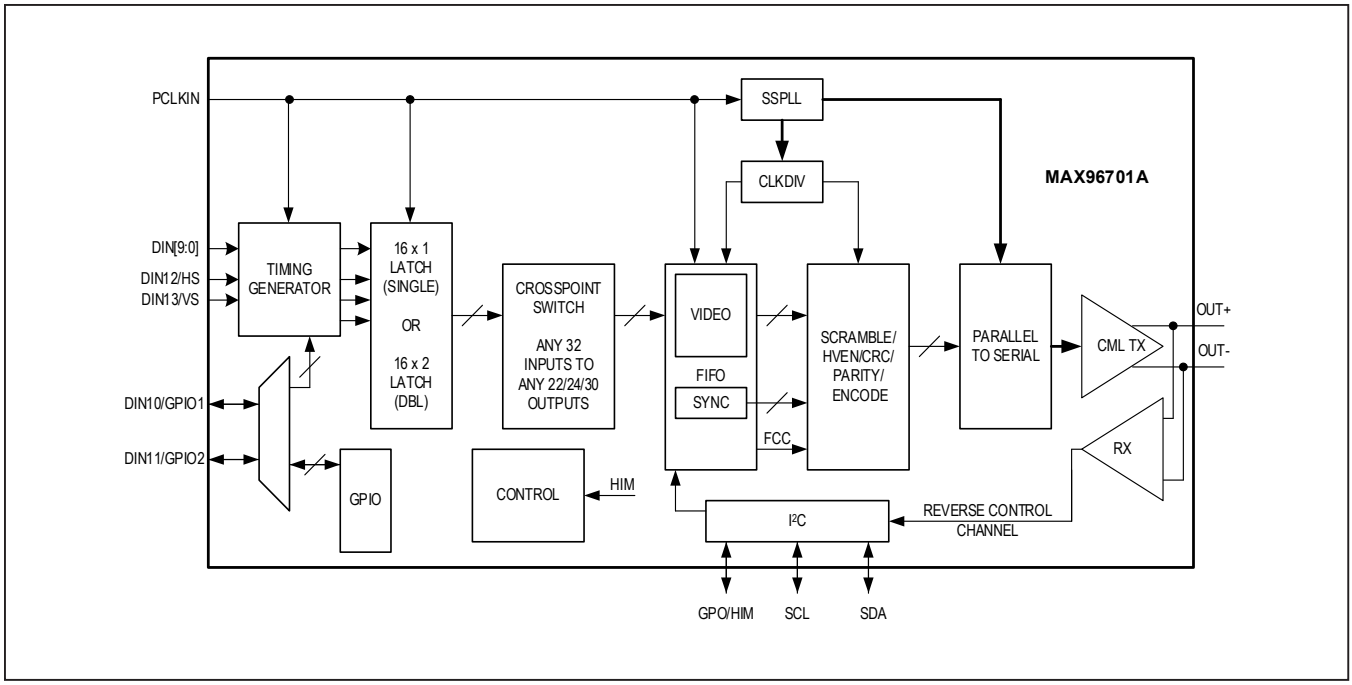
Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
POWER				
3, 13	GND	Analog and Digital Ground.		Power
16	AVDD	1.8V Analog Power Supply. Bypass AVDD to GND with 0.1µF, and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to AVDD.		Power
22	DVDD	1.8V Digital Power Supply. Bypass DVDD to GND with 0.1µF, and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.		Power
EP	—	Exposed Pad. EP is internally connected to device ground. Must connect EP to the PCB ground plane through a via array for proper thermal and electrical performance.		Power
HIGH-SPEED DIGITAL				
Single Function				
1	DIN4	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
2	DIN5	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
4	DIN6	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
5	DIN7	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
6	DIN8	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
7	DIN9	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
19	PCLKIN	Parallel Clock Input with Internal Pulldown to GND. Latches parallel data inputs and provides the PLL reference clock.	DVDD	Digital

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
20	DIN0	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
21	DIN1	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
23	DIN2	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
24	DIN3	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
Multifunction				
8	DIN10/GPIO1	Parallel Data Input/GPIO. Defaults to parallel data input on power-up. Parallel data input has internal pulldown to GND. GPIO1 has an open-drain input/output with internal 60kΩ pullup to DVDD.	DVDD	Digital
9	DIN11/GPIO2	Parallel Data Input/GPIO. Defaults to parallel data input on power-up. Parallel data input has internal pulldown to GND. GPIO2 has an open-drain input/output with internal 60kΩ pullup to DVDD.	DVDD	Digital
10	DIN12/HS	Parallel Data Input/Horizontal Sync with Internal Pulldown to GND. Defaults to parallel data input on power-up. Defaults to horizontal-sync input when HS/VS encoding is enabled, or when in high-bandwidth mode.	DVDD	Digital
11	DIN13/VS	Parallel Data Input/Vertical Sync with Internal Pulldown to GND. Defaults to parallel data input on power-up. Defaults to vertical-sync input when HS/VS encoding is enabled, or when in high-bandwidth mode.	DVDD	Digital
Configuration and Interface				
12	GPO/HIM	General-Purpose Output/High-Immunity Mode Input with internal Pulldown to GND. HIM is latched at power-up and switches to GPO output automatically after power-up. Connect HIM to DVDD with a 30kΩ resistor to set high, or leave open to set low. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the deserializer must be set to the same value. GPO output follows the state of the GPI (or INT) input on the GMSL deserializer. GPO is low upon power-up.	DVDD	Digital
14	OUT-	Inverting Coax/Twisted-Pair Serial Output	—	Digital
15	OUT+	Noninverting Coax/Twisted-Pair Serial Output	—	Digital
17	SDA	Serial Data. Input/output with internal 30kΩ pullup to DVDD. SDA is the SDA input/output of the serializer's I^2C master/slave. SDA has an open-drain driver and requires a pullup resistor.	DVDD	Digital
18	SCL	Serial Clock. Input/output with internal 30kΩ pullup to DVDD. SCL is the SCL input/output of the serializer's I^2C master/slave. SCL has an open-drain driver and requires a pullup resistor.	DVDD	Digital

Functional Block Diagram



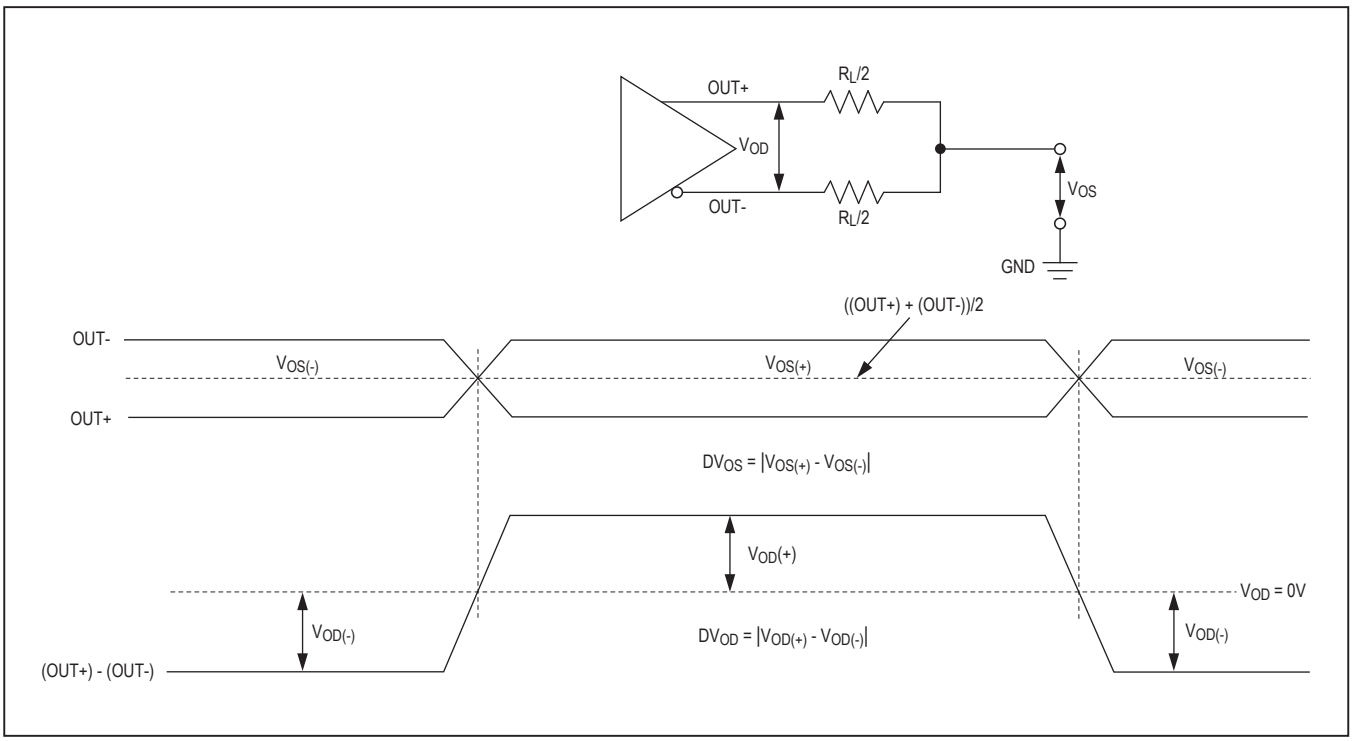


Figure 1. Serial-Output Parameters

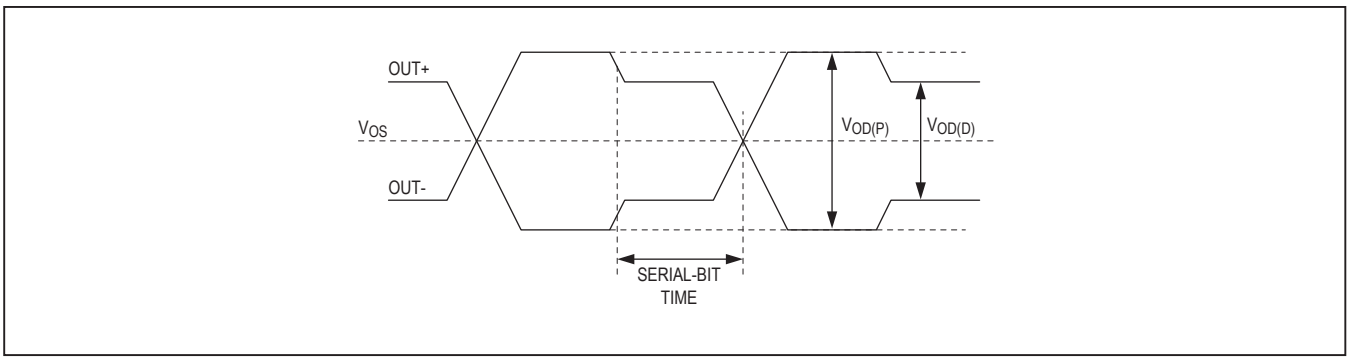


Figure 2. Output Waveforms at OUT+, OUT-

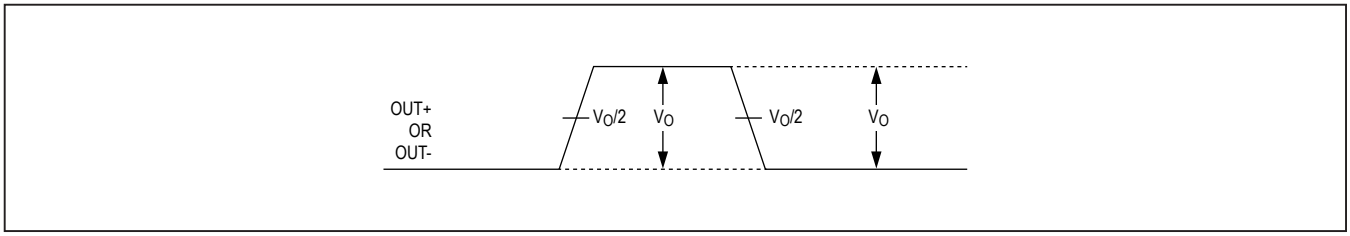


Figure 3. Single-Ended Output Template

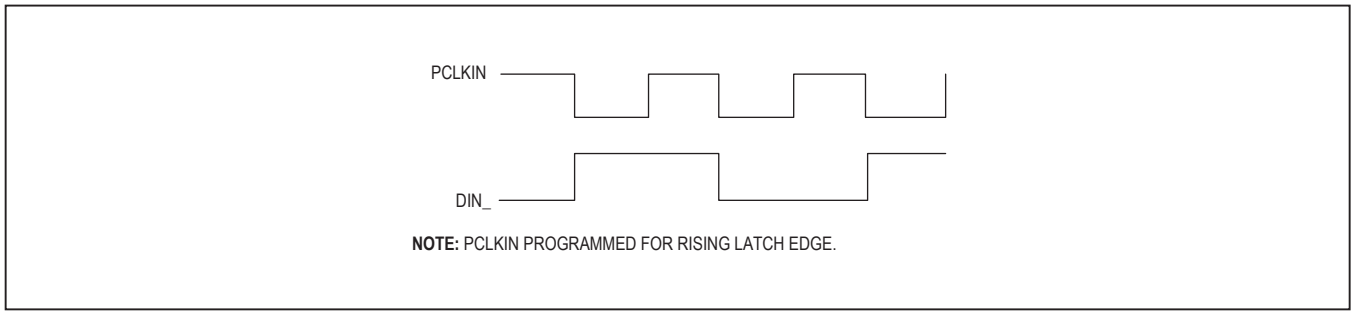


Figure 4. Worst-Case Pattern Input

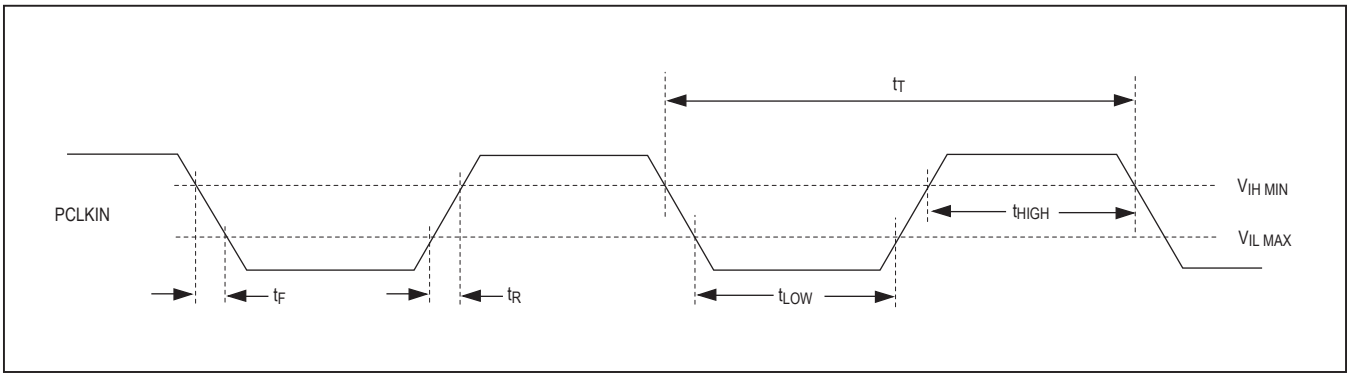


Figure 5. Parallel Clock Input Requirements

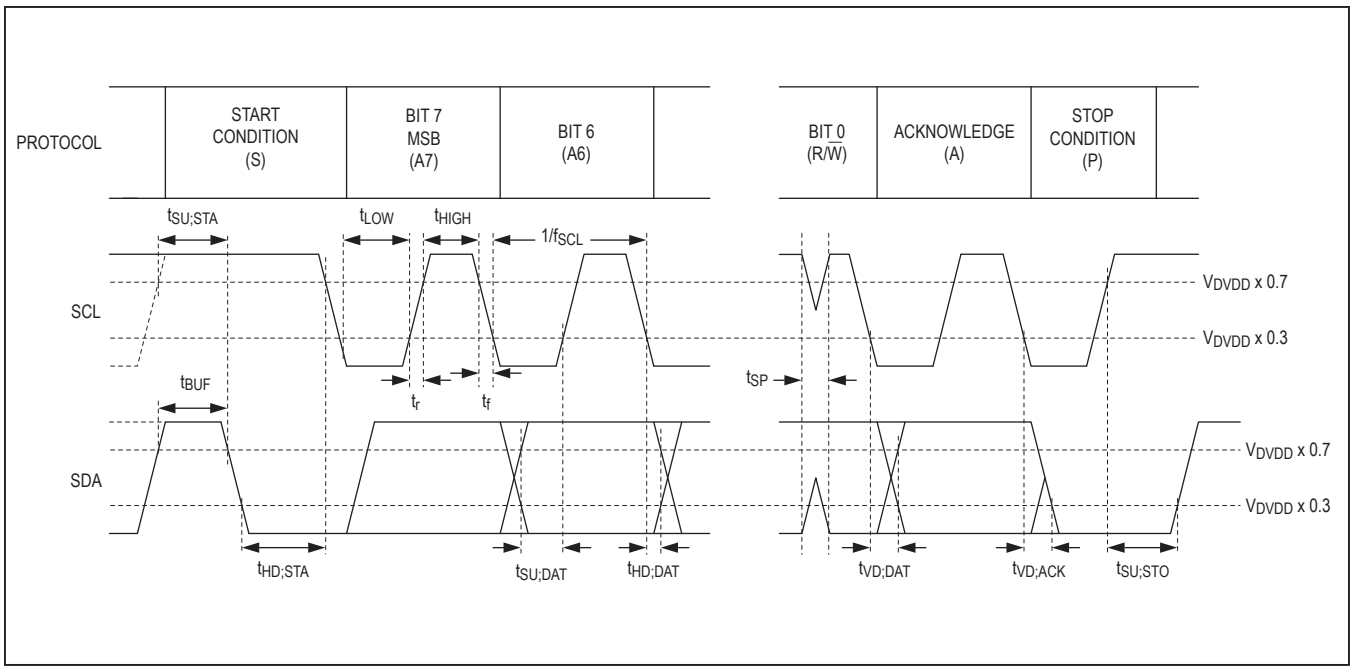


Figure 6. I²C Timing Parameters

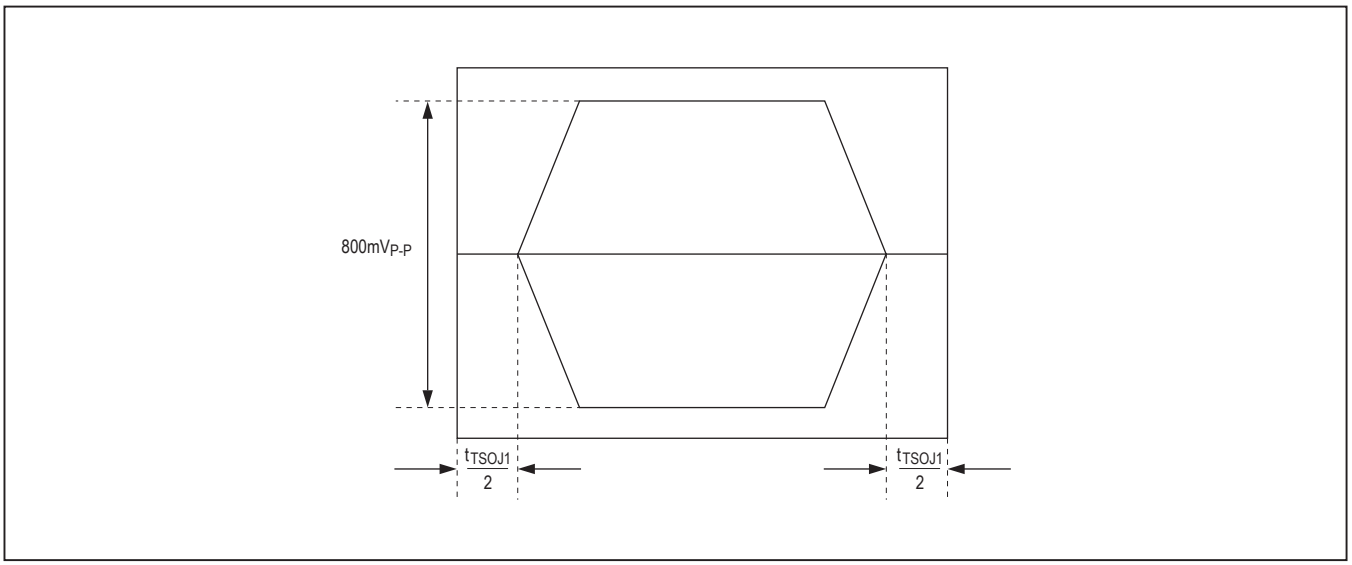


Figure 7. Differential Output Template

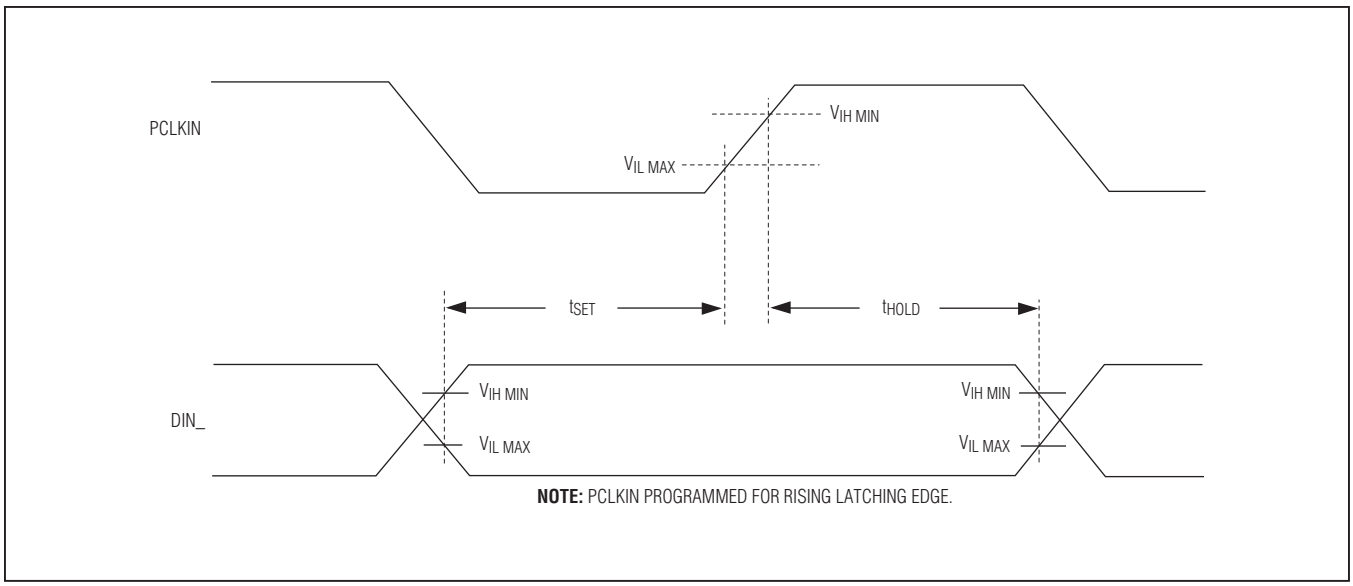


Figure 8. Input Setup and Hold Times

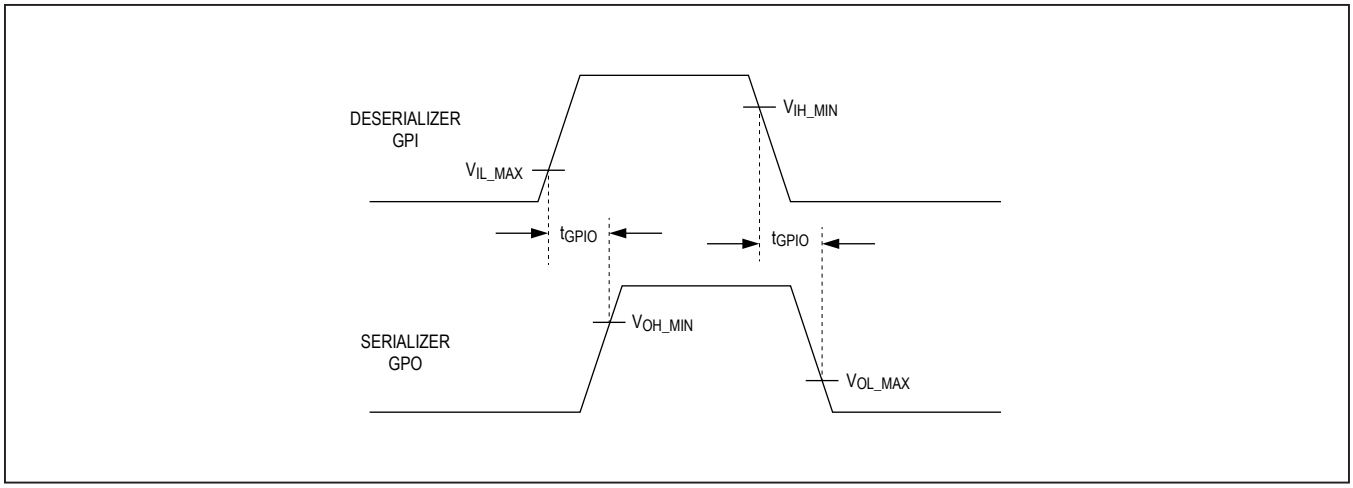


Figure 9. GPI-to-GPO Delay

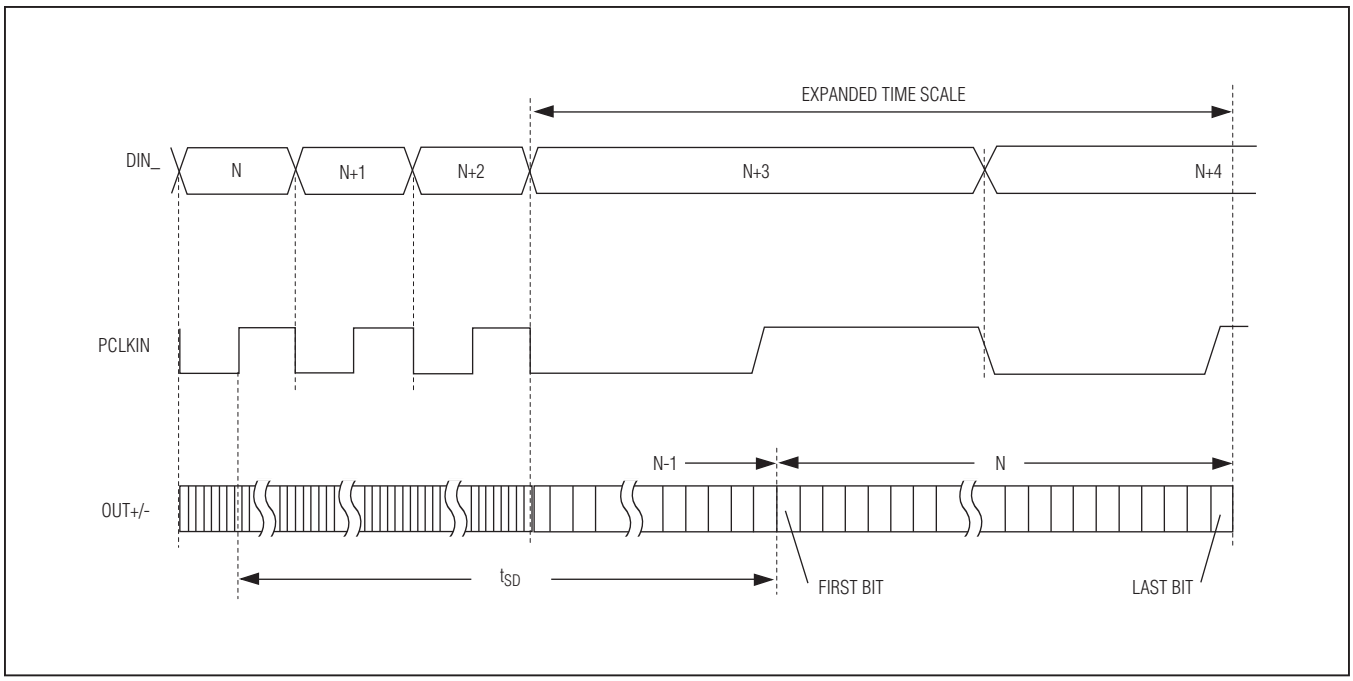


Figure 10. Serializer Delay

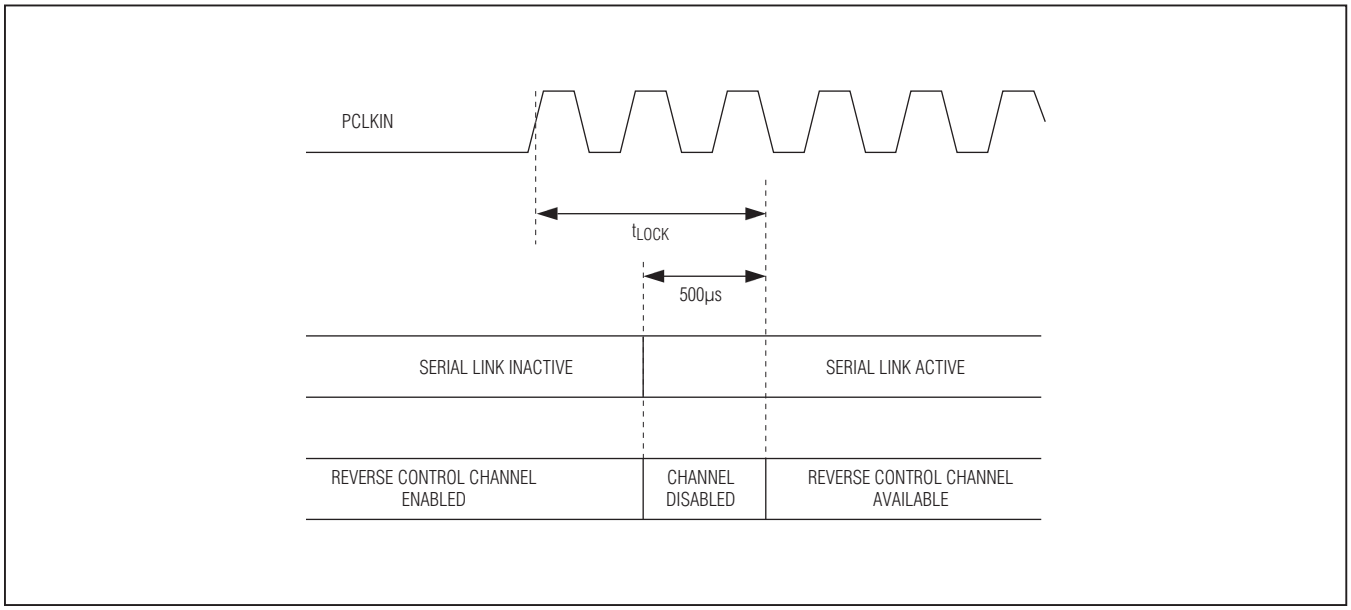


Figure 11. Link Startup Time

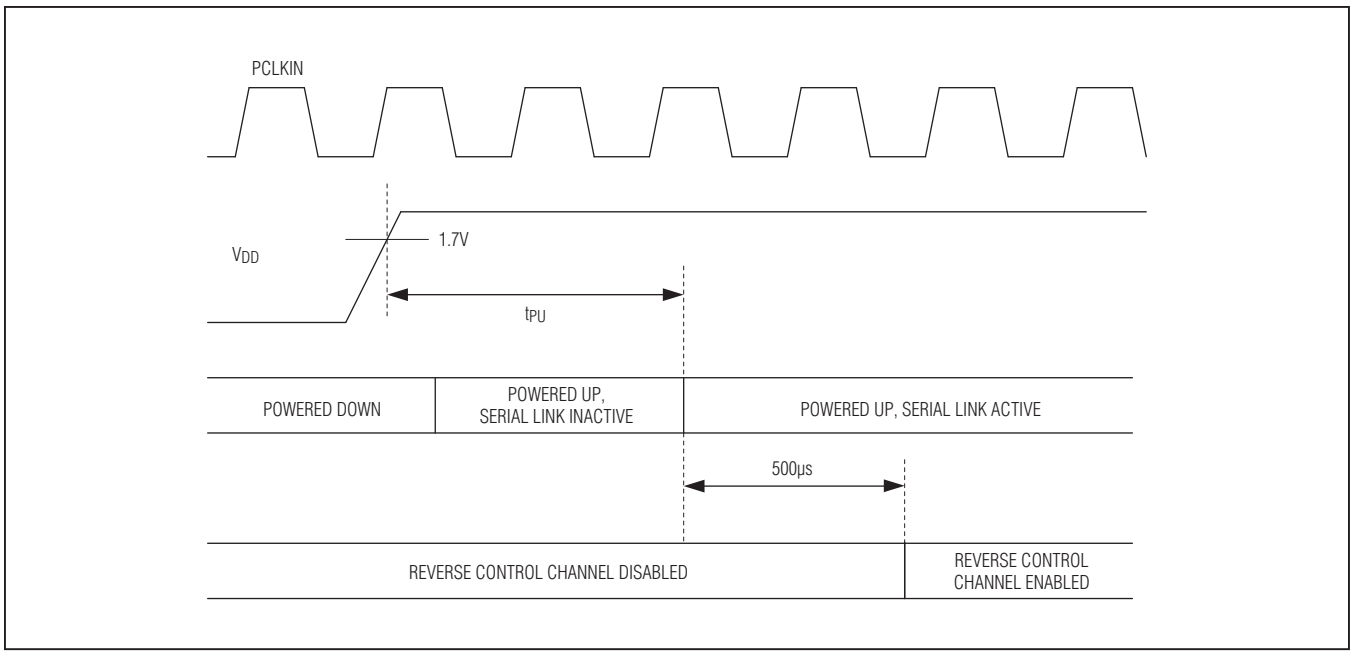


Figure 12. Power-Up Delay

Detailed Description

The MAX96701A is a compact device with features especially suited for automotive camera applications. The device operates at a variety of input widths and word rates up to a total serial-data rate up to 1.74Gbps. High-bandwidth mode offers a 116MHz parallel clock rate with 12 bits of video data and 2 bits of sync (HS/VS) data. An embedded 9.6kbps to 1Mbps control channel programs the serializer, deserializer, and any attached I^2C peripherals.

To promote safety applications, the device features CRC protection of video and control data. In addition, control-channel retransmission and high-immunity modes reduce the effects of bit errors corrupting communication. Preemphasis and a PRBS tester allow for in-system evaluation and optimization of the link quality.

The MAX96701A operates over the -40°C to +115°C automotive temperature range.

Serial Link Signaling and Data Format

The serializer scrambles the input parallel data and combines this with the forward control data. The data is then encoded for transmission and output as a single-serialized bitstream at several times the input word rate (depending on bus width). The deserializer receives the serial data and recovers the clock signal. The data is then deserialized, decoded, and descrambled into parallel output data and forward control data.

Operating Modes

The GMSL devices are configurable to operate in many modes depending on the application. These modes allow for a more efficient use of serial bandwidth. Most of these settings are set during system design, and are configured through register bits.

Video/Configuration Link

In normal operation, the serializer runs in video link mode (serializer SEREN = 1) with video data and control data sent across the serial link. Set SEREN = 0 in the serializer to turn off serialization. The serializer powers up in video link mode and requires a valid PCLK for operation.

A configuration link is available to set up the serializer, deserializer, and peripherals when PCLK is not available. Set SEREN = 0 and CLINK = 1 in the serializer to enable the configuration link (SEREN = 1 forces the serializer into video link mode). Once PCLK has been established, turn on the video link (SEREN = 1).

By default, video link mode requires a valid PCLK for operation. Set AUTO_CLINK bit = 1 and SEREN = 1 in the serializer to have the device automatically switch between the video link and configuration link whenever PCLK is not present.

Single/Double Mode

Single-/double-mode operation configures the available 1.74Gbps bandwidth into a variety of widths and word rates. Single-mode operation is compatible with all GMSL devices and serializers, yielding one parallel word for each serial word. Double mode serializes two half-width parallel words for each serial word, resulting in a 2x increase in the parallel word rate range (compared to single mode). Set DBL = 0 for single-mode operation and DBL = 1 for double-mode operation.

HS/VS Encoding

By default, GMSL assigns a video bit slot to HSYNC, VSYNC, and DE (if used). With HS/VS encoding, the device instead encodes special packets to sync signals to free up additional video bit slots. HS/VS encoding is on by default when the device is in high-bandwidth mode (HIBW = 1). DE is encoded only when HIBW = 1 and DE_EN = 1. Set HVEN = 1 to turn on HS/VS encoding when HIBW = 0 (DE, if enabled, uses up a video bit). HS/VS encoding requires that HSYNC, VSYNC, and DE (if used) remain high during the active video and low during the blanking period. Use HS/VS inversion when using reverse-polarity sync signals.

Error Detection

The serial link's 8b/10b encoding/decoding and 1-bit parity detect bit errors that occur on the serial link. An optional 6-bit CRC check is available at the expense of 6 video bits (when HIBW = 0). To activate 6-bit CRC mode, set PXL_CRC = 1 in the remote-side device first, then in the local-side device. When using 6-bit CRC mode, the available internal bus width is reduced by 6 bits in single-input mode (DBL = 0) and 3 bits in double-input mode (DBL = 1). Note that the input bus width may already have been reduced due to pin availability of the serializer or deserializer; thus, the reduction of bandwidth from CRC may not be visible (see Table 3).

An additional 32-bit video line CRC is available by setting LINE_CRC_EN = 1. When enabled, the serializer calculates the 32-bit CRC of the video line and sends this information during the blanking period. The deserializer compares the received CRC with the video line data. The deserializer's LINE_CRC_ERR bit latches when a CRC error is detected. LINE_CRC_ERR clears when read.

Bus Widths

The serial link has multiple bus-width settings that determine the parallel bus width and the resulting parallel word rate. The serial link operates to a maximum serial bit rate of 1.74Gbps. The BWS bit determines if each serial packet is 30 or 40 bits long, which translates to a maximum serial packet rate (and resulting maximum parallel word rate) of 58MHz or 43.5MHz when BWS = 0 or 1 respectively. Encoding translates the 24, 27, or 32 parallel bits into 30- or 40-bit serial packets. One bit is used for parity, while a second is reserved for the control channel. An additional 6 bits are used during optional 6-bit CRC. In addition, double mode splits the remaining word size in half, if used. The remaining bits can be used for video bits (minus any sync bits if H/V encoding is not used).

The following modes list the internal bus widths. The number of available input and output pins may limit the actual bus width available.

- 24-Bit Mode (Figure 13)

When BWS = 0 and HIBW = 0, the 30-bit serial packet corresponds with three 8b/10b symbols representing 24 bits (24-bit mode). After the parity and control channel, this leaves 16/22 bits of video data if CRC is/or is not used (single mode), or 8/11 bits of video data if CRC is/or is not used (double mode).

- 27-Bit High-Bandwidth Mode (Figure 14)

When BWS = 0 and HIBW = 1 (high-bandwidth mode), the 30-bit serial packet represents three 9b/10b symbols representing 27 bits. After the parity and control channel, this leaves 19/25 bits of video data if CRC is/or is not used (single mode), or 9/12 bits of video data if CRC is/or is not used (double mode)

- 32-Bit Mode (Figure 15)

When BWS = 1, the 40-bit serial packet corresponds with four 8b/10b symbols representing 32 bits (32-bit mode). After parity and control channel, this leaves 24/30 bits of video data if CRC is/or is not used (single mode), or 12/15 bits of video data if CRC is/or is not used (double mode).

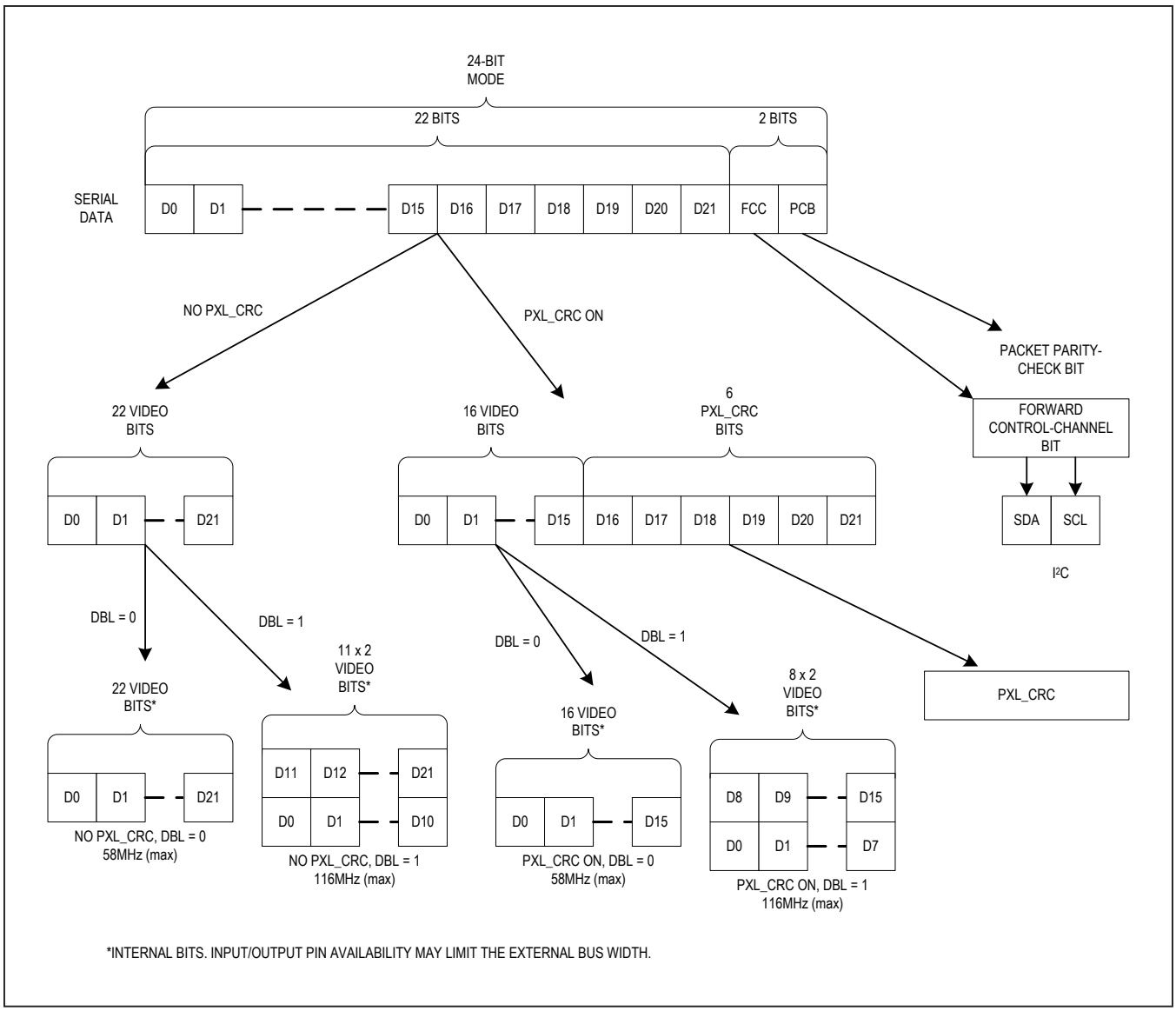


Figure 13. 24-Bit Mode Serial-Data Format

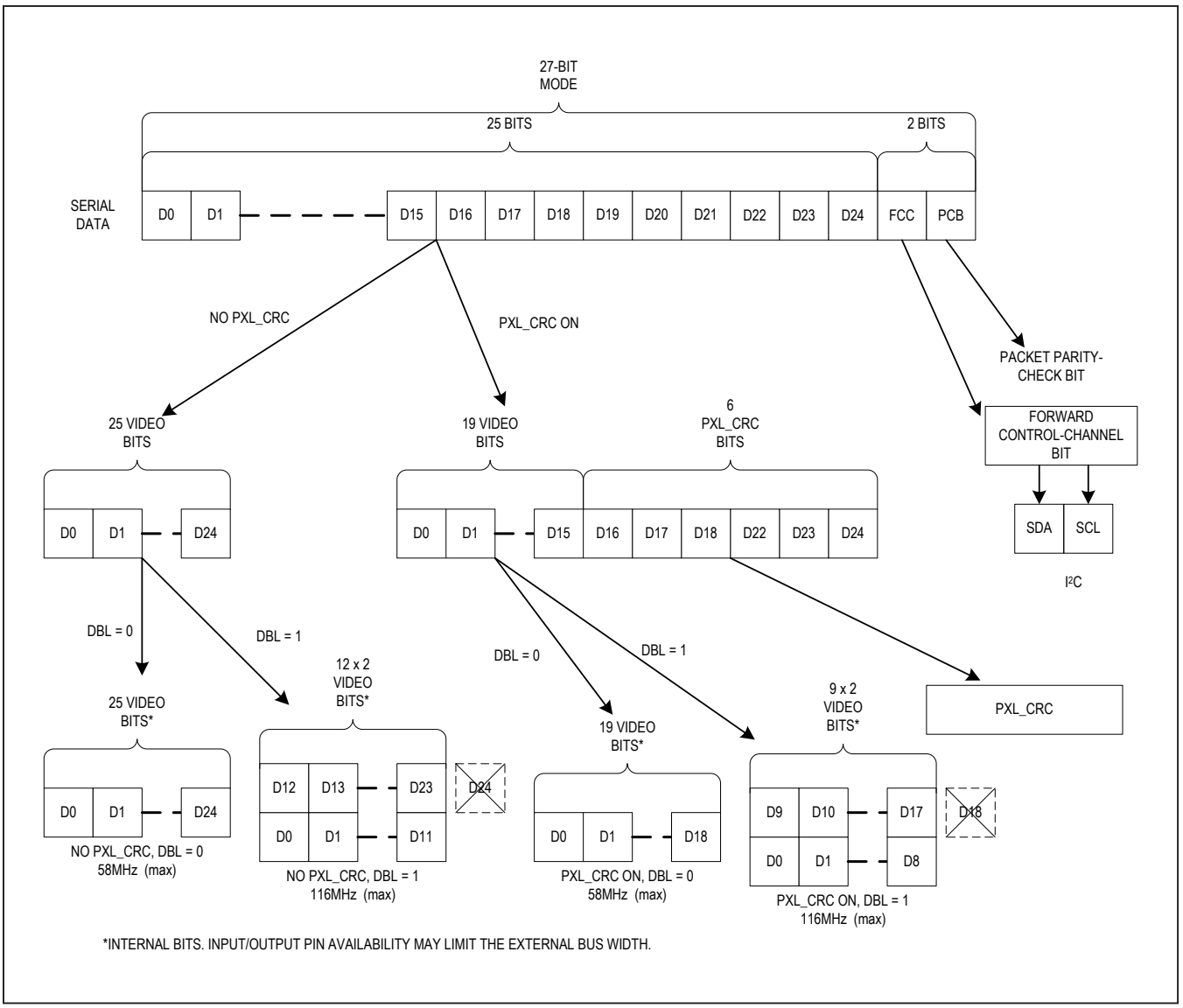


Figure 14. 27-Bit High-Bandwidth Mode Serial-Data Format

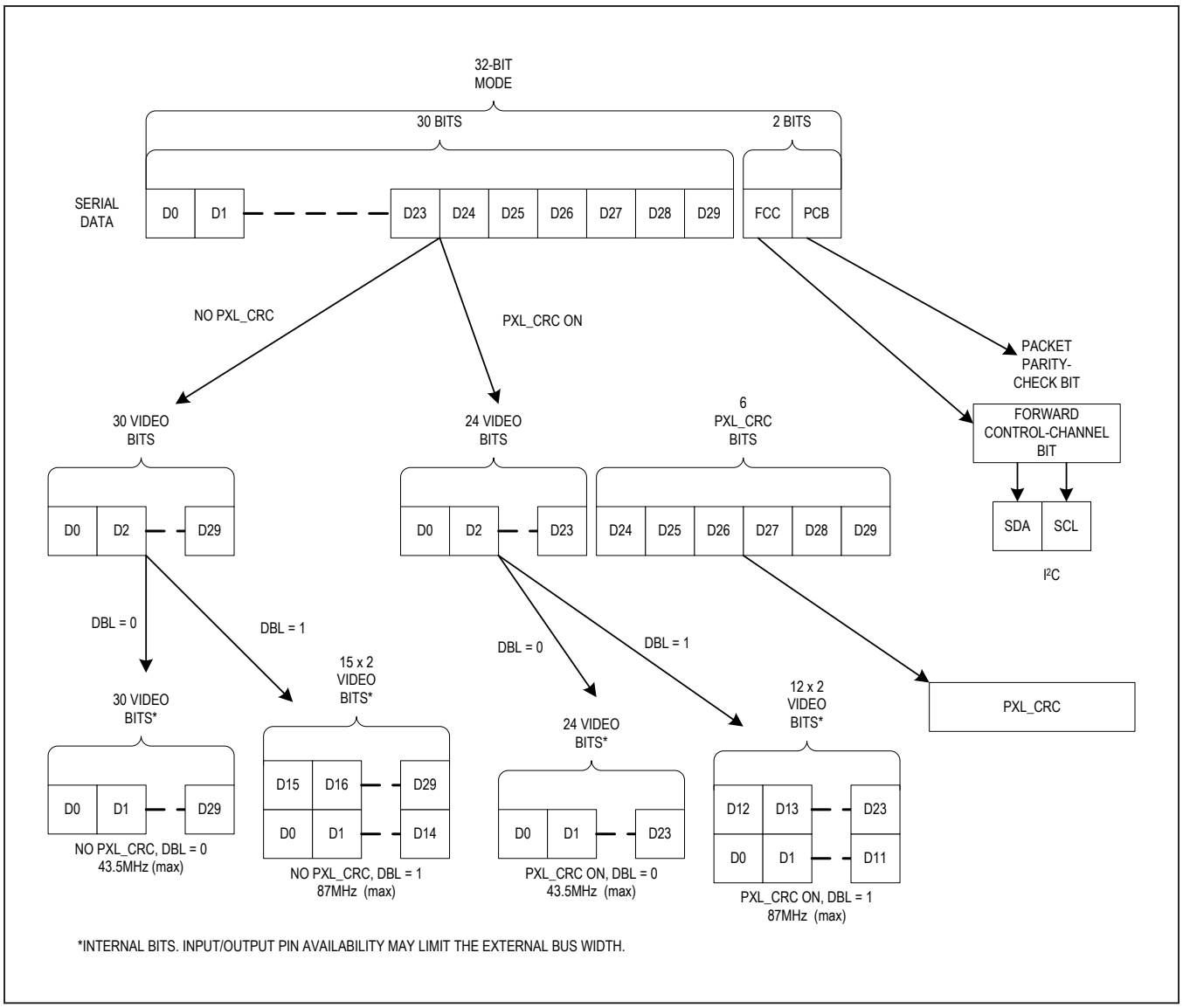


Figure 15. 32-Bit Mode Serial-Data Format

Control Channel and Register Programming

The control channel sends information across the serial link for control of the serializer, deserializer, and any attached peripherals. The control channel is multiplexed onto the serial link and is available with or without the video channel.

Forward Control Channel

Control data sent from the serializer to the deserializer is sent on the forward control channel. The data is encoded as one of the serial bits in the forward high-speed link. After deserialization, the forward control-channel data is extracted from the serial link. The forward control-channel bandwidth exceeds the maximum external control data rate, and all data sent on the forward control channel appears on the remote side after transmission delay of a few bit times.

Reverse Control Channel

Control data sent from the deserializer to the serializer is sent on the reverse control channel. The data is encoded as a series of 1µs pulses, with a maximum raw data rate of 1Mbps. High-immunity mode is available to increase the robustness of the reverse control channel at a reduced raw bit rate of 500kbps. In Table 1, setting the REV_FAST bit = 1 increases this rate back to 1Mbps. When the input data rate (after encoding) exceeds the reverse data rate, the input clock is held through clock stretching to slow the external clock to match the internal bit rate.

I²C Interface

The serial link connects the serializer and deserializer I²C interfaces together through the control channel. When an I²C master sends a command to one side of the link (local side) the control channel forwards this information to and from the other side of the link (remote side), allowing a single microcontroller to configure the serializer, deserializer, and peripherals. The microcontroller can be located on the serializer side (display applications) and the deserializer side (camera applications). Dual microcontroller operations are supported as long as a software-arbitration method is used. The serial link assumes that only one microcontroller is talking at any given time.

Remote-End Operation

When an I²C master initiates communication on the local slave device (the serializer/deserializer directly connected to the master), the remote-side device acts as a master device that sends data forwarded from the local-side device, and forwards any data received from peripherals attached to the remote-side device. This remote-side master device operates according to the timing settings in the I²C master setting register. Set the master settings to match the timing settings used by the external microcontroller.

Clock-Stretch Timing

The I²C interface uses clock stretching to allow time for data to be forwarded across the serial link. The master microcontroller, along with any attached peripherals, must accept clock stretching of the GMSL devices.

Packet-Based I²C

A packet-based control channel is available for enhanced error handling of the control channel. This control-channel method handles simultaneous GPI/GPO and I²C transmission, along with error detection and retransmission. To use packet-based control channel, first set ALLOW_PKTCC = 1 in the serializer. Then, set the PKTCC_EN bit in the deserializer. The PKTCC_EN bit in the serializer automatically sets itself when it sees the enable command from the deserializer.

Table 1. Reverse Control-Channel Modes

HIM PIN SETTING	REVFAST BIT	REVERSE CONTROL-CHANNEL MODE	MAXIMUM I²C BIT RATE (kBPS)
Low	X	Legacy reverse control-channel mode (compatible with all GMSL devices)	1000
High	0	High-immunity mode	500
	1	Fast high-immunity mode (requires HIBW = 0, serial-data rate > 1.25Gbps)	1000

X = Don't care.

Packet Protocol Summary

The packet-based control channel uses a synchronous, symbol-based system to send data across the control channel. Data to be sent across the control channel is split into symbols and stored in a transmit queue and then sent across the link. If both GPI and I2C data needs to be sent (e.g., when GPI transitions during an I2C transmission), the symbols from both commands are combined in the queue. If the transmit queue is empty, idle packets are sent across the link to maintain control-channel lock. Received I2C packets are output as determined by the microcontroller SCL rate (local device) or the programmed master bit rate (remote device). The device holds SCL low (clock stretch) until data has been received from the remote-side device.

Control-Channel Error Detection and Packet Retransmission

When the packet-based control channel is used, all packets are checked for errors through CRC. Using 1, 5, or 8 bits, CRC detects 1, 3, or 4 random bit errors in a packet. The transmitter retransmits packets whenever an error is detected. The transmitter sets a flag if a number of retries exceeds eight. The receiver filters out packets with errors.

GPO/GPI Control

GPO on the serializer follows GPI transitions on the deserializer. This GPO/GPI function can be used to transmit signals such as a frame sync in a surround-view camera system (see the *Providing a Frame Sync (Camera Applications)* section). Optionally, GPO can be set directly by register bits.

Spread Spectrum

The serializer contains a programmable spread-spectrum output to lower emission levels by spreading the clock-frequency peaks across a frequency spectrum. In addition, the serializer and deserializer can track a spread input clock, eliminating the need for multiple spread clocks.

Cable Type Configuration

The driver output is programmable for two kinds of cable,100Ω twisted pair and 50Ω coax (contact the factory for devices compatible with 75Ω cables). In coax mode, connect OUT+ to IN+ of the deserializer. Leave the unused IN_ pin unconnected, or connect it to ground through 50Ω, and a capacitor for increased power-supply rejection. Connect OUT- to V_{DD} through a 50Ω resistor (Figure 16).

Crossbar Switch

The crossbar switch routes data between the parallel input/output and the SerDes. The anything-to-anything routing assures the mapping between the video source and destination. For each crossbar output (XBO_) an input multiplexer selects from the available crossbar inputs (XBI_) using the CROSSBAR_ register bits (Figure 17). Multiple crossbar outputs can use the same crossbar input. By default, the sync signals share the same inputs as the MSBs of the video data.

Video Timing Generator

The serializer includes a programmable video timing generator to generate/retime the input sync signals. The timing generator can be used to modify a camera's input timing, filter out glitches in the sync signals, or to reduce the number of required input sync signals. Each sync signal can be individually retimed or left unmodified. Several registers determine the length of the timing parameters (in PCLK cycles) shown in Figure 18. Timing parameters include high/low period length, line count, and delay from the input VS signal.

The timing generator uses three different trigger modes, tracking, single trigger, and autorun. Tracking mode looks at the input VSYNC and locks once it receives three consecutive identical VSYNC signals. The tracker then continues to output the same identical signal, erasing any glitches that may appear on VSYNC. The tracker attempts to relock to a new signal if three consecutive input waveforms do not match the locked signal. Single trigger generates one generated frame for each input VSYNC edge. Autorun generates a new frame at the rate determined by the VSYNC high/low period. If a new VSYNC signal appears before a frame is complete in either single trigger or autorun modes, a new frame immediately starts, cutting the previous frame short.

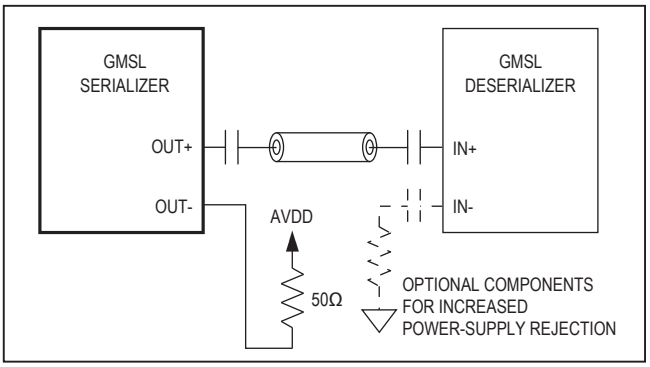


Figure 16. Coax Connection

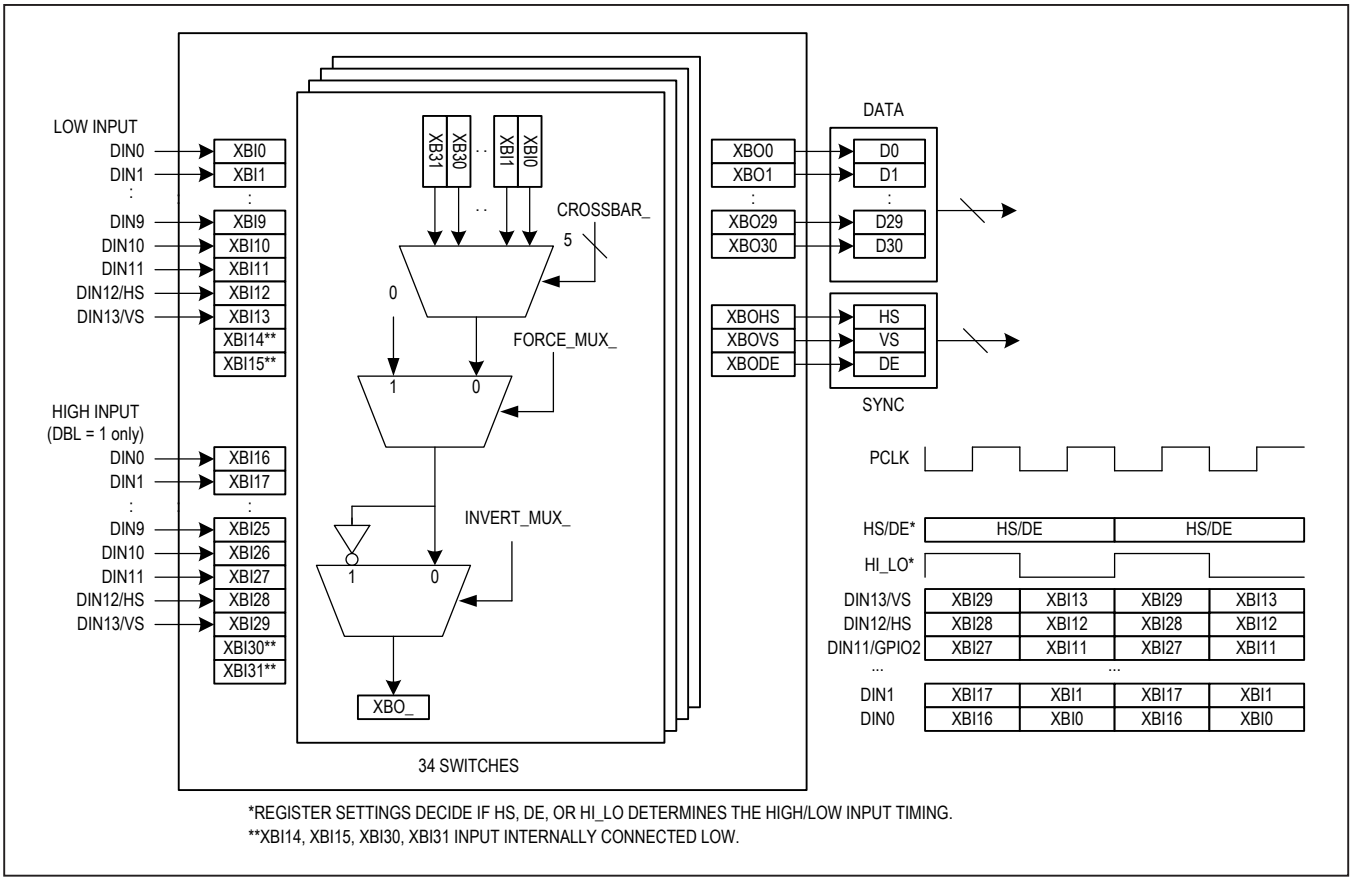


Figure 17. Crossbar Switch Dataflow

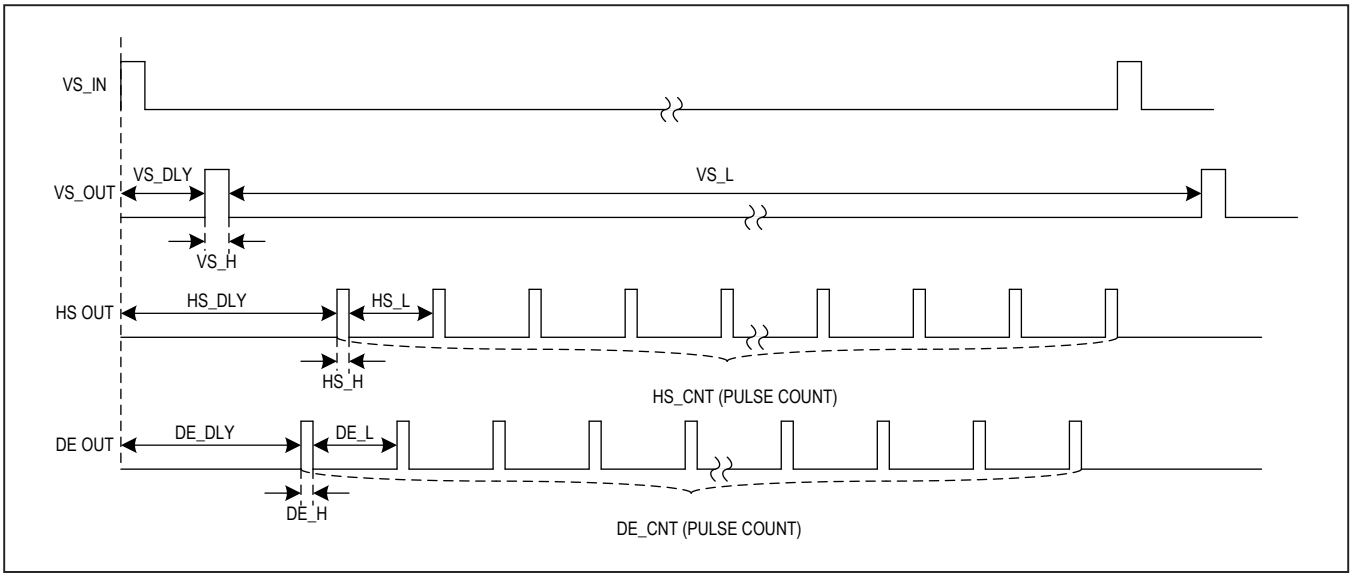


Figure 18. Sync Signal Format for Video-Timing Generation

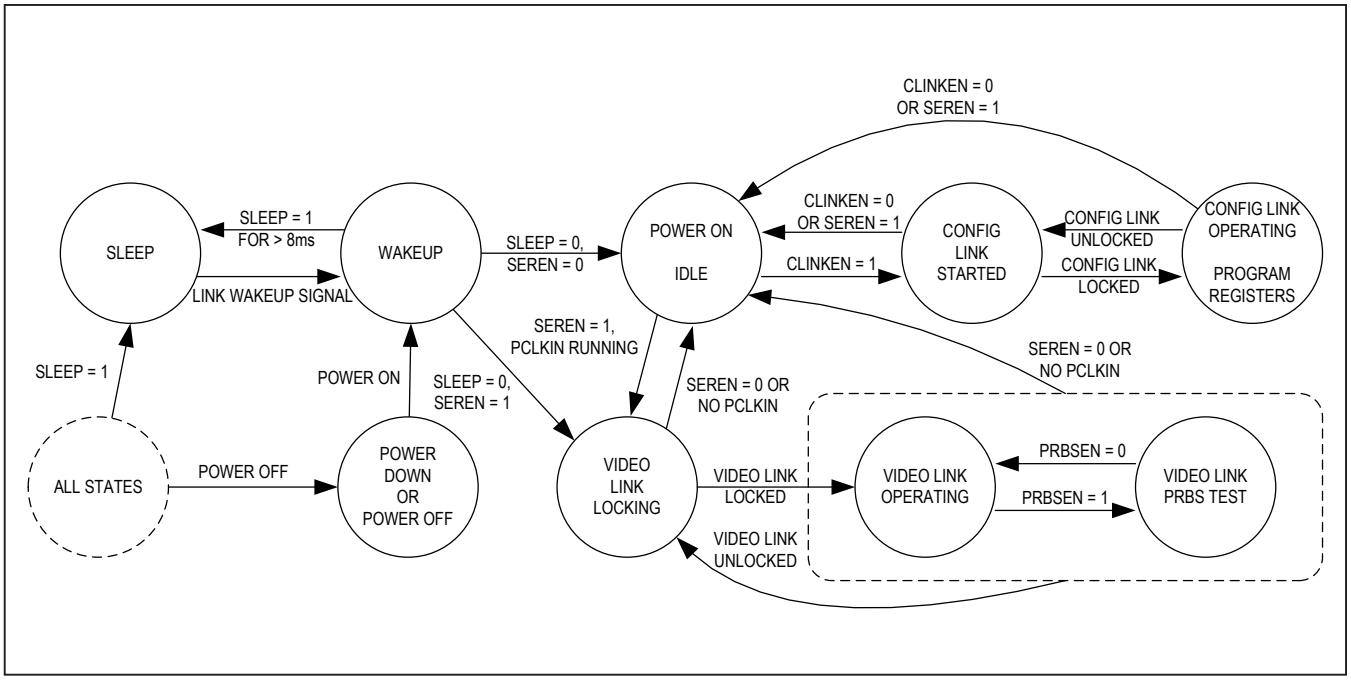


Figure 19. State Diagram

Shutdown/Sleep Modes

Several sleep and shutdown modes are available when full operation is not needed.

Configuration Link

When the high-speed video link is not needed, or unavailable, a configuration link can be used in its place. In configuration link mode, the parallel digital input/output is disabled, the LOCK pin remains low, and the serial link internally generates its own clock to allow full operation of the control channel (I^2C and GPIO).

Serialization Disable

When the serial link is not needed, such as when downstream devices are powered off, the user can disable serialization. In this mode, all forward communication is shut down. The user can reenable serialization either locally, or through the reverse channel.

Sleep Mode

To reduce power consumption further, the devices can be put into sleep mode. In this mode, all registers keep their programmed values, and all functions in the device are powered down except for the wake-up detectors on the local control interface, and the serial link. Any activity seen by the wake-up detectors temporarily turns on the control-channel interface. During this time, a microcontroller can command the device to exit sleep mode. See the *Shutdown/Sleep Modes* section.

Link Startup Procedure

Table 2 and Table 2a lists the startup procedure for image-sensing applications. The control channel is available after the video link or the configuration link is established. If the deserializer powers up after the serializer, the control channel becomes unavailable until 2ms after power-up.

Table 2. Link-Startup Procedure (PCLK not Present)*

NO.	µC	SERIALIZER	DESERIALIZER
—	**µC Connected to Deserializer**	**Set Configuration Inputs**	**Set Configuration Inputs**
1	Powers up (wait t_{PU}).	Powers up and loads default settings.	Powers up and loads default settings.
1a	Programs CLINKEN and/or AUTOCLINK bits. Wait 5ms after each command.	Establishes configuration link.	Locks to configuration link.
1b	Sets any additional configuration bits that are mismatched between the serializer and deserializer (e.g., BWS). Wait 5ms for lock after each command.	Configuration changed. Reestablishes configuration link if needed.	Configuration changed. Locks to configuration link.
2	Sets register 0x07 configuration bits in the serializer (DBL, BWS, HIBW, PXL_CRC, etc.). Wait 5ms.	Configuration changed. Reestablishes configuration link if needed.	Loss-of-lock may occur.
3	Sets register 0x07 configuration bits in the deserializer (DBL, BWS, HIBW, PXL_CRC, etc.). Wait 5ms for lock to reestablish.	—	Configuration changed. Locks to configuration/video link.
4	Writes rest of serializer/deserializer configuration bits.	Configuration changed.	Configuration changed.
5	Writes camera/peripheral configuration bits.	Forwards commands from µC to serializer.	Forwards commands to camera/ peripherals.
5a	When PCLK is available, set SEREN = 1. Wait 5ms for lock.	Enables video link.	Locks to video link.

**The link startup procedure assumes that the CXTP and HIM settings are matching at power-up. If these are not matching, set CXTP/HIGHIMM bits (reg 0x4D) in the serializer via control channel before applying PCLK.*

Table 2a. Link-Startup Procedure PCLK is Present*

NO.	µC	SERIALIZER	DESERIALIZER
—	**µC Connected to Deserializer**	**Set Configuration Inputs**	**Set Configuration Inputs**
1	Powers up (wait t_{PU}).	Powers up and loads default settings. Establishes video link when valid PCLK is available.	Powers up and loads default settings. Locks to video link signal if available.
2	Sets deserializer configuration bits that are mismatched between the serializer and deserializer. Wait 5ms for lock after each command.	—	Configuration changed. Locks to video link if lock was lost.
3	Set a single serializer configuration bit to the final setting. Wait 5ms.	Configuration changed. Reestablishes link if needed.	
4	Sets deserializer configuration bit to match the serializer. Wait 5ms for lock. Repeat from step 3 until all matched settings are set.	—	Configuration changed. Locks to video link if lock was lost.

**It is recommended to configure the serial link before applying PCLK (see Table 2).*

Register Map

GMSL Register Map

OFFSET	NAME	MSB							LSB
0x00	seraddr	SERADDR[6:0]							CFG-BLOCK
0x01	desaddr	DESADDR[6:0]							RSVD
0x02	ss	SS[2:0]			RSVD	PRNG[1:0]		SRNG[1:0]	
0x03	sdiv	AUTOFM[1:0]		SDIV[5:0]					
0x04	main_control	SEREN	CLINKEN	PRBSEN	SLEEP	RSVD[1:0]		REVCCEN	FWDCCEN
0x05	prbs_len	RSVD	RSVD	PRBS_LEN[1:0]		RSVD	RSVD	RSVD	RSVD
0x06	cmllvl_preemp	CMLLVL[3:0]				PREEMP[3:0]			
0x07	config	DBL	HIBW	BWS	ES	RSVD	HVEN	RSVD	PXL_CRC
0x08	rsvd_8	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
0x09	i2c_source A	I2C_SRC_A[6:0]							RSVD
0x0A	i2c_dest A	I2C_DST_A[6:0]							RSVD
0x0B	i2c_source B	I2C_SRC_B[6:0]							RSVD
0x0C	i2c_dest B	I2C_DST_B[6:0]							RSVD
0x0D	i2c_config	I2C_LOC_ACK	I2C_SLV_SH[1:0]		I2C_MST_BT[2:0]			I2C_SLV_TO[1:0]	
0x0E	gpio_en	RSVD	RSVD	RSVD	RSVD	RSVD	GPIO_EN_2	GPIO_EN_1	RSVD
0x0F	gpio_out	EN_SET_GPO	RSVD	RSVD	RSVD	RSVD	GPIO_OUT_2	GPIO_OUT_1	SET_GPO
0x10	gpio_in	RSVD	RSVD	RSVD	RSVD	RSVD	GPIO_IN_2	GPIO_IN_1	GPO_L
0x11	errg	ERRG_RATE[1:0]		ERRG_TYPE[1:0]		ERRG_CNT[1:0]		ERRG_PER	ERRG_EN
0x12	rsvd_12	RSVD	RSVD	RSVD	RSVD[4:0]				
0x13	pd	SOFT_PD	ALLOW_PKTCC	RSVD	RSVD	RSVD	RSVD	RSVD[1:0]	
0x14	pktcc_lock	RSVD[1:0]		RSVD	RSVD	RSVD	RSVD	CC_WBLOCK	REM_CCLOCK
0x15	input_status	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	OUT-PUTEN	PCLKDET
0x16	max_rt_err	RSVD	MAX_RT_ERR	RSVD[5:0]					
0x17	rsvd_17	RSVD[7:0]							
0x18	crc 0	CRC_VALUE_0[7:0]							
0x19	crc 1	CRC_VALUE_1[7:0]							
0x1A	crc 2	CRC_VALUE_2[7:0]							
0x1B	crc 3	CRC_VALUE_3[7:0]							
0x1C	cc_crc_errcnt	CC_CRC_ERRCNT[7:0]							
0x1D	rsvd_1d	RSVD[7:0]							

GMSL Register Map (continued)

OFFSET	NAME	MSB							LSB
0x1E	id	ID[7:0]							
0x1F	revision	RSVD	RSVD	RSVD	HDCPCAP	REVISION[3:0]			
0x20	crossbar 0	RSVD	FORCE_MUX_0	INVERT_MUX_0	CROSSBAR_0[4:0]				
0x21	crossbar 1	RSVD	FORCE_MUX_1	INVERT_MUX_1	CROSSBAR_1[4:0]				
0x22	crossbar 2	RSVD	FORCE_MUX_2	INVERT_MUX_2	CROSSBAR_2[4:0]				
0x23	crossbar 3	RSVD	FORCE_MUX_3	INVERT_MUX_3	CROSSBAR_3[4:0]				
0x24	crossbar 4	RSVD	FORCE_MUX_4	INVERT_MUX_4	CROSSBAR_4[4:0]				
0x25	crossbar 5	RSVD	FORCE_MUX_5	INVERT_MUX_5	CROSSBAR_5[4:0]				
0x26	crossbar 6	RSVD	FORCE_MUX_6	INVERT_MUX_6	CROSSBAR_6[4:0]				
0x27	crossbar 7	RSVD	FORCE_MUX_7	INVERT_MUX_7	CROSSBAR_7[4:0]				
0x28	crossbar 8	RSVD	FORCE_MUX_8	INVERT_MUX_8	CROSSBAR_8[4:0]				
0x29	crossbar 9	RSVD	FORCE_MUX_9	INVERT_MUX_9	CROSSBAR_9[4:0]				
0x2A	crossbar 10	RSVD	FORCE_MUX_10	INVERT_MUX_10	CROSSBAR_10[4:0]				
0x2B	crossbar 11	RSVD	FORCE_MUX_11	INVERT_MUX_11	CROSSBAR_11[4:0]				
0x2C	crossbar 12	RSVD	FORCE_MUX_12	INVERT_MUX_12	CROSSBAR_12[4:0]				
0x2D	crossbar 13	RSVD	FORCE_MUX_13	INVERT_MUX_13	CROSSBAR_13[4:0]				
0x2E	crossbar 14	RSVD	FORCE_MUX_14	INVERT_MUX_14	CROSSBAR_14[4:0]				
0x2F	crossbar 15	RSVD	FORCE_MUX_15	INVERT_MUX_15	CROSSBAR_15[4:0]				
0x30	crossbar 16	RSVD	FORCE_MUX_16	INVERT_MUX_16	CROSSBAR_16[4:0]				
0x31	crossbar 17	RSVD	FORCE_MUX_17	INVERT_MUX_17	CROSSBAR_17[4:0]				
0x32	crossbar 18	RSVD	FORCE_MUX_18	INVERT_MUX_18	CROSSBAR_18[4:0]				
0x33	crossbar 19	RSVD	FORCE_MUX_19	INVERT_MUX_19	CROSSBAR_19[4:0]				
0x34	crossbar 20	RSVD	FORCE_MUX_20	INVERT_MUX_20	CROSSBAR_20[4:0]				

GMSL Register Map (continued)

OFFSET	NAME	MSB							LSB
0x35	crossbar 21	RSVD	FORCE_ MUX_21	INVERT_ MUX_21	CROSSBAR_21[4:0]				
0x36	crossbar 22	RSVD	FORCE_ MUX_22	INVERT_ MUX_22	CROSSBAR_22[4:0]				
0x37	crossbar 23	RSVD	FORCE_ MUX_23	INVERT_ MUX_23	CROSSBAR_23[4:0]				
0x38	crossbar 24	RSVD	FORCE_ MUX_24	INVERT_ MUX_24	CROSSBAR_24[4:0]				
0x39	crossbar 25	RSVD	FORCE_ MUX_25	INVERT_ MUX_25	CROSSBAR_25[4:0]				
0x3A	crossbar 26	RSVD	FORCE_ MUX_26	INVERT_ MUX_26	CROSSBAR_26[4:0]				
0x3B	crossbar 27	RSVD	FORCE_ MUX_27	INVERT_ MUX_27	CROSSBAR_27[4:0]				
0x3C	crossbar 28	RSVD	FORCE_ MUX_28	INVERT_ MUX_28	CROSSBAR_28[4:0]				
0x3D	crossbar 29	RSVD	FORCE_ MUX_29	INVERT_ MUX_29	CROSSBAR_29[4:0]				
0x3E	crossbar 30	RSVD	FORCE_ MUX_30	INVERT_ MUX_30	CROSSBAR_30[4:0]				
0x3F	crossbar_hs	RSVD	FORCE_ MUX_HS	INVERT_ MUX_HS	CROSSBARHS[4:0]				
0x40	crossbar_vs	RSVD	FORCE_ MUX_VS	INVERT_ MUX_VS	CROSSBARVS[4:0]				
0x41	crossbar_de	RSVD	FORCE_ MUX_DE	INVERT_ MUX_DE	CROSSBARDE[4:0]				
0x42	link_config	LINE_CRC_LOC[1:0]		LINE_ CRC_EN	MAX_ RT_EN	RSVD	GPI_ COMP_ EN	GPI_RT_ EN	GPO_EN
0x43	sync_gen_config	RSVD	RSVD	GEN_VS	GEN_HS	GEN_DE	VS_ TRIG	VTG_MODE[1:0]	
0x44	vs_dly 2	VS_DLY[7:0]							
0x45	vs_dly 1	VS_DLY[7:0]							
0x46	vs_dly 0	VS_DLY[7:0]							
0x47	vs_h 2	VS_H[7:0]							
0x48	vs_h 1	VS_H[7:0]							
0x49	vs_h 0	VS_H[7:0]							
0x4A	vs_l 2	VS_L[7:0]							
0x4B	vs_l 1	VS_L[7:0]							
0x4C	vs_l 0	VS_L[7:0]							
0x4D	cxtp	HIGHIMM	CXTP	RSVD	RSVD	VSYNC_ INV	HSYNC_ INV	DE_INV	RSVD
0x4E	hs_dly 2	HS_DLY[7:0]							

GMSL Register Map (continued)

OFFSET	NAME	MSB							LSB
0x4F	hs_dly 1	HS_DLY[7:0]							
0x50	hs_dly 0	HS_DLY[7:0]							
0x51	rsvd_51	RSVD[7:0]							
0x52	rsvd_52	RSVD[7:0]							
0x53	rsvd_53	RSVD[7:0]							
0x54	hs_h 1	HS_H[7:0]							
0x55	hs_h 0	HS_H[7:0]							
0x56	hs_l 1	HS_L[7:0]							
0x57	hs_l 0	HS_L[7:0]							
0x58	hs_cnt 1	HS_CNT[7:0]							
0x59	hs_cnt 0	HS_CNT[7:0]							
0x5A	de_dly 2	DE_DLY[7:0]							
0x5B	de_dly 1	DE_DLY[7:0]							
0x5C	de_dly 0	DE_DLY[7:0]							
0x5D	rsvd_5D	RSVD[7:0]							
0x5E	rsvd_5E	RSVD[7:0]							
0x5F	rsvd_5F	RSVD[7:0]							
0x60	de_h 1	DE_H[7:0]							
0x61	de_h 0	DE_H[7:0]							
0x62	de_l 1	DE_L[7:0]							
0x63	de_l 0	DE_L[7:0]							
0x64	de_cnt 1	DE_CNT_1[7:0]							
0x65	de_cnt 0	DE_CNT_0[7:0]							
0x66	prbs_type	RSVD[1:0]		PRBS_ TYPE	REV_ FAST	DE_EN	DIS_ RWAKE	RSVD	CXSEL
0x67	dbl_align_to	RSVD[1:0]		AUTO_ CLINK	RSVD	RSVD	DBL_ALIGN_TO[2:0]		
0x68	cc_crc_length	RSVD	RSVD[2:0]			RSVD[1:0]		CC_CRC_ LENGTH[1:0]	
0x69	hi_lo	RSVD	EN_HI_ LO	INVERT_ HI_LO	CROSSBAR_HI_LO[4:0]				

0x96	rsvd_96	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD[1:0]
0x97	rsvd_97	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD[2:0]	
0x98	rsvd_98	RSVD[1:0]		RSVD[2:0]			RSVD[2:0]	
0x99	rsvd_99	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD[1:0]
0x9A	pktcc_en	RSVD[1:0]		RSVD[1:0]		PKTCC_ EN	RSVD[1:0]	RSVD

GMSL Register Map (continued)

OFFSET	NAME	MSB							LSB
0xC8	rsvd_c8	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
0xC9	rsvd_c9	RSVD[7:0]							
0xFC	rsvd_fc	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
0xFD	rsvd_fd	RSVD[7:0]							
0xFE	rsvd_fe	RSVD[3:0]				RSVD[3:0]			
0xFF	rsvd_ff	RSVD	RSVD	RSVD	RSVD	RSVD[3:0]			

seraddr (0x00)

BIT	7	6	5	4	3	2	1	0
Field	SERADDR[6:0]							CFGBLOCK
Reset	1000000b							0b
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SERADDR	7:1	**Serializer Address:** Serializer device address	0000000: Write/read device address is 0x00/0x01 0000001: Write/read device address is 0x02/0x03 1111111: Write/read device address is 0xFE/0xFF
CFG-BLOCK	0	**Configuration Block:** Set to 1 to make all registers read-only. Power-on reset to clear this bit.	0: Make all registers read/write 1: Make all registers read-only

desaddr (0x01)

BIT	7	6	5	4	3	2	1	0
Field	DESADDR[6:0]							RSVD
Reset	1001000b							0b
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DESADDR	7:1	**Deserializer Address:** Deserializer device address	0000000: Write/read device address is 0x00/0x01 0000001: Write/read device address is 0x02/0x03 1111111: Write/read device address is 0xFE/0xFF
RSVD	0	**Reserved:** Do not change from default value	0: Reserved

ss (0x02)

BIT	7	6	5	4	3	2	1	0
Field	SS[2:0]			RSVD	PRNG[1:0]		SRNG[1:0]	
Reset	010b			1b	11b		11b	
Access Type	Write, Read			Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SS	7:5	**Spread Spectrum:** Spread-spectrum setting	000: Spread is off 001: 0.5% Spread setting 010: 1.5% Spread setting (Default) 011: 2% Spread setting 100: Spread is off 101: 1% Spread setting 110: 3% Spread setting 111: 4% Spread setting
RSVD	4	**Reserved:** Do not change from default value	1: Reserved
PRNG	3:2	**Pixel Clock Range:** Pixel clock-range selection Stated ranges depend on DBL = setting	00: Select 12.5MHz to 25MHz (DBL = 0) or 25MHz to 50MHz (DBL = 1) pixel clock range 01: Select 25MHz to 58MHz (DBL = 0) or 50MHz to 116MHz (DBL = 1) pixel clock range 10: Automatically detect pixel clock range 11: Automatically detect pixel clock range.
SRNG	1:0	**Serial-Data Rate Range**	00: 0.5Gbps to 1Gbps serial-data range 01: 1Gbps to 1.74Gbps serial-data range 10: Automatically detect serial-data range 11: Automatically detect serial-data range

sdiv (0x03)

BIT	7	6	5	4	3	2	1	0
Field	AUTOFM[1:0]		SDIV[5:0]					
Reset	00b		000000b					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
AUTOFM	7:6	**Automatic Frequency Modulation:** Modulation-rate calibration interval	00: Calibration occurs once 01: Calibration occurs every 2ms 10: Calibration occurs every 16ms 11: Calibration occurs every 256ms
SDIV	5:0	**Sawtooth Divider:** Sawtooth divider value 0x00 sets the sawtooth divider to autocalibrate mode	000000: Sawtooth divider automatically calibrates the divider value 000001: Sawtooth divider set to 1 111111: Sawtooth divider set to 63

main_control (0x04)

BIT	7	6	5	4	3	2	1	0
Field	SEREN	CLINKEN	PRBSEN	SLEEP	RSVD[3:2]		REVCCEN	FWDCCEN
Reset	1b	0b	0b	0b	01b		1b	1b
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SEREN	7	**Serialization Enable:** Requires a valid PCLK for serialization	0: Disable serialization 1: Enable serialization
CLINKEN	6	**Configuration Link Enable:** Configuration link enabled only when the video link is not enabled (SEREN = 1)	0: Disable configuration link 1: Enable configuration link
PRBSEN	5	**PRBS Test Enable:** See the PRBS test section for more details	0: Disable PRBS test 1: Enable PRBS test
SLEEP	4	**Sleep Mode Enable:** Activates sleep mode (see the *Shutdown/Sleep Modes* section for more information)	0: Disable sleep mode 1: Enable sleep mode
RSVD	3:2	**Reserved:** Do not change from default value	01: Reserved
REVCCEN	1	**Reverse ControlChannel Enable:** Enable reverse control-channel receiver (data from deserializer)	0: Disable reverse control-channel receiver 1: Enable reverse control-channel receiver
FWDCCEN	0	**Forward Control Channel Enable:** Enable forward control channel receiver (data to deserializer)	0: Disable forward control channel transmitter 1: Enable forward control channel transmitter

prbs_len (0x05)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	PRBS_LEN[1:0]		RSVD	RSVD	RSVD	RSVD
Reset	0b	0b	00b		0b	0b	0b	0b
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
RSVD	6	**Reserved:** Do not change from default value	0: Reserved
PRBS_LEN	5:4	**PRBS Length:** PRBS test pattern length	00: Continuous bit pattern (infinite length) 01: 9.8Mbit length 10: 167.1Mbit length 11: 1341.5Mbit length
RSVD	3	**Reserved:** Do not change from default value	0: Reserved
RSVD	2	**Reserved:** Do not change from default value	0: Reserved
RSVD	1	**Reserved:** Do not change from default value	0: Reserved
RSVD	0	**Reserved:** Do not change from default value	0: Reserved

cmllvl_preemp (0x06)

BIT	7	6	5	4	3	2	1	0
Field	CMLLVL[3:0]				PREEMP[3:0]			
Reset	10X0b				0000b			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CMLLVL	7:4	**CML Level:** Output CML signal level = (register value) x 50mV Default level depends on cable type (CXTP)	0000: Do not use 0001: Do not use 0010: 100mV output 0011: 150mV output 0100: 200mV output 0101: 250mV output 0110: 300mV output 0111: 350mV output 1000: 400mV output (STP default) 1001: 450mV output 1010: 500mV output (coax default) 1011: Do not use 1100: Do not use 1101: Do not use 111X: Do not use
PREEMP	3:0	**Preemphasis Level:** Preemphasis setting	0000: Preemphasis off 0001: 1.2dB deemphasis 0010: 2.5dB deemphasis 0011: 4.1dB deemphasis 0100: 6.0dB deemphasis 0101: Do not use 011X: Do not use 1000: 1.1dB preemphasis 1001: 2.2dB preemphasis 1010: 3.3dB preemphasis 1011: 4.4dB preemphasis 1100: 6.0dB preemphasis 1101: 8.0dB preemphasis 1110: 10.5dB preemphasis 1111: 14.0dB preemphasis

config (0x07)

BIT	7	6	5	4	3	2	1	0
Field	DBL	HIBW	BWS	ES	RSVD	HVEN	RSVD	PXL_CRC
Reset	1b	0b	0b	0b	0b	1b	0b	0b
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DBL	7	**Double-Input Mode Enable:** Set high to enable double-input mode	0: Single-input mode 1: Double-input mode
HIBW	6	**High-Bandwidth Mode Enable:** High-bandwidth mode select (effective only when BWS = 0)	0: Use 24-bit mode when BWS = 0 1: Use high-bandwidth mode when BWS = 0
BWS	5	**Bus-Width Select**	0: 24-bit and high-bandwidth mode 1: 32-bit mode
ES	4	**Edge Select**	0: Parallel data clocked in on rising edge 1: Parallel data clocked in on falling edge
RSVD	3	**Reserved:** Do not change from default value	0: Reserved
HVEN	2	**HSYNC/VSYNC Encoding Enable**	0: Disable HS/VS encoding 1: Enable HS/VS encoding
RSVD	1	**Reserved:** Do not change from default value	0: Reserved
PXL_CRC	0	**Pixel CRC Type:** Pixel error-detection type	0: Serial data uses 1-bit parity 1: Serial data uses 6-bit CRC

rsvd_8 (0x08)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Reset	0b	0b	0b	0b	0b	0b	0b	0b
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
RSVD	6	**Reserved:** Do not change from default value	0: Reserved
RSVD	5	**Reserved:** Do not change from default value	0: Reserved
RSVD	4	**Reserved:** Do not change from default value	0: Reserved
RSVD	3	**Reserved:** Do not change from default value	0: Reserved
RSVD	2	**Reserved:** Do not change from default value	0: Reserved
RSVD	1	**Reserved:** Do not change from default value	0: Reserved
RSVD	0	**Reserved:** Do not change from default value	0: Reserved

i2c_source (0x09, 0x0B)

BIT	7	6	5	4	3	2	1	0
Field	I2C_SRC[6:0]							RSVD
Reset	0000000b							0b
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_SRC	7:1	**I²C Source:** I²C address translator source	0000000: Write/read device address is 0x00/0x01 0000001: Write/read device address is 0x02/0x03 1111111: Write/read device address is 0xFE/0xFF
RSVD	0	**Reserved:** Do not change from default value	0: Reserved

i2c_dest (0x0A, 0x0C)

BIT	7	6	5	4	3	2	1	0
Field	I2C_DST[6:0]							RSVD
Reset	0000000b							0b
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_DST	7:1	**I²C Destination:** I²C address translator destination	0000000: Write/read device address is 0x00/0x01 0000001: Write/read device address is 0x02/0x03 1111111: Write/read device address is 0xFE/0xFF
RSVD	0	**Reserved:** Do not change from default value	0: Reserved

i2c_config (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	I2C_LOC_ ACK	I2C_SLV_SH[1:0]		I2C_MST_BT[2:0]			I2C_SLV_TO[1:0]	
Reset	1b	01b		101b			10b	
Access Type	Write, Read	Write, Read		Write, Read			Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_LOC_ ACK	7	**I²C Local Acknowledge:** I²C-to-I²C slave generates local acknowledge when forward channel is not available	0: Do not send local autoacknowledge when control channel is absent 1: Send local autoacknowledge when control channel is absent
I2C_SLV_ SH	6:5	**I²C Slave Setup/Hold Time:** I²C-to-I²C slave setup and hold-time setting (setup, hold) (typ)	00: (352ns, 117ns) setup/hold time 01: (469ns, 234ns) setup/hold time 10: (938ns, 352ns) setup/hold time 11: (1406ns, 469ns) setup/hold time
I2C_MST_ BT	4:2	**I²C Master Bit Rate:** I²C-to-I²C master bit-rate setting (min, typ, max)	000: (6.61, 8.47, 9.92) kbps 001: (22.1, 28.3, 33.2) kbps 010: (66.1, 84.7, 99.2) kbps 011: (82, 105, 123) kbps 100: (136, 173, 203) kbps 101: (265, 339, 397) kbps 110: (417, 533, 625) kbps 111: (654, 837, 980) kbps
I2C_SLV_ TO	1:0	**I²C Slave Timeout:** I²C-to-I²C slave remote-side timeout setting (typ)	00: 64µs slave timeout 01: 256µs slave timeout 10: 1024µs slave timeout 11: Slave timeout disabled

gpio_en (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	GPIO_EN_2	GPIO_EN_1	RSVD
Reset	0b	0b	0b	0b	0b	0b	0b	0b
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
RSVD	6	**Reserved:** Do not change from default value	0: Reserved
RSVD	5	**Reserved:** Do not change from default value	0: Reserved
RSVD	4	**Reserved:** Do not change from default value	0: Reserved
RSVD	3	**Reserved:** Do not change from default value	0: Reserved
GPIO_EN_2	2	**GPIO Enable:** Disabled by default	0: Pin functions as a parallel input 1: Pin functions as a GPIO
GPIO_EN_1	1	**GPIO Enable:** Disabled by default	0: Pin functions as parallel input 1: Pin functions as GPIO
RSVD	0	**Reserved:** Do not change from default value	0: Reserved

gpio_out (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	EN_SET_ GPO	RSVD	RSVD	RSVD	RSVD	GPIO_ OUT_2	GPIO_ OUT_1	SET_GPO
Reset	0b	0b	1b	1b	1b	1b	1b	0b
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_SET_GPO	7	**Enable Set GPO:** Set to 1 to enable setting of GPO from SET_GPO	0: Disable setting of GPO through SET_GPO 1: Enable setting of GPO through SET_GPO
RSVD	6	**Reserved:** Do not change from default value	0: Reserved
RSVD	5	**Reserved:** Do not change from default value	1: Reserved
RSVD	4	**Reserved:** Do not change from default value	1: Reserved
RSVD	3	**Reserved:** Do not change from default value	1: Reserved
GPIO_OUT_2	2	**GPIO Output Level:** Pull down GPIO when 0	0: Set GPIO output level low 1: Set GPIO output level high
GPIO_OUT_1	1	**GPIO Output Level:** Pull down GPIO when 0	0: Set GPIO output level low 1: Set GPIO output level high
SET_GPO	0	**Set GPO Level:** Set GPO output high or low (when EN_SET_GPO = 1)	0: Set GPO output low 1: Set GPO output high

gpio_in (0x10)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	GPIO_IN_2	GPIO_IN_1	GPO_L
Reset	0b	0b	0b	0b	0b	Xb	Xb	0b
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved**	0: Reserved
RSVD	6	**Reserved**	0: Reserved
RSVD	5	**Reserved**	X: Reserved
RSVD	4	**Reserved**	X: Reserved
RSVD	3	**Reserved**	X: Reserved
GPIO_IN_2	2	**GPIO Input Level:** Input pin level of GPIO	0: GPIO input is low 1: GPIO input is high
GPIO_IN_1	1	**GPIO Input Level:** Input pin level of GPIO	0: GPIO input is low 1: GPIO input is high
GPO_L	0	**GPO Output Level**	0: GPO output level is low 1: GPO output level is high

errg (0x11)

BIT	7	6	5	4	3	2	1	0
Field	ERRG_RATE[1:0]		ERRG_TYPE[1:0]		ERRG_CNT[1:0]		ERRG_PER	ERRG_EN
Reset	0b		0b		0b		0b	0b
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_RATE	7:6	**Error-Generation Rate:** Error-generation rate, on average	00: Generate errors every 2560 bits 01: Generate errors every 40,960 bits 10: Generate errors every 655,360 bits 11: Generate errors every 10,485,760 bits
ERRG_TYPE	5:4	**Error-Generation Type:** Type of generated errors	00: Single-bit errors 01: 2 8b/10b symbols 10: 3 8b/10b symbols 11: 4 8b/10b symbols
ERRG_CNT	3:2	**Error-Generation Count:** Number of generated errors	00: Generate errors continuously 01: Generate16 errors 10: Generate 128 errors 11: Generate 1024 errors
ERRG_PER	1	**Periodic Error Generation Enable**	0: Generator creates errors randomly (based on error rate) 1: Generator creates errors periodically (based on error rate)
ERRG_EN	0	**Error Generator Enable**	0: Disable error generator 1: Enable error generator

rsvd_12 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD[4:0]				
Reset	0b	1b	0b	00000b				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
RSVD	6	**Reserved:** Do not change from default value	1: Reserved
RSVD	5	**Reserved:** Do not change from default value	0: Reserved
RSVD	4:0	**Reserved:** Do not change from default value	00000: Reserved

pd (0x13)

BIT	7	6	5	4	3	2	1	0
Field	SOFT_PD	ALLOW_ PKTCC	RSVD	RSVD	RSVD	RSVD	RSVD[1:0]	
Reset	0b	0b	0b	0b	0b	0b	10b	
Access Type	Write 1 to Set, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SOFT_PD	7	**Soft Power Down:** Set this bit to 1 to reset the device; this bit is cleared after the device resets	0: Normal operation 1: Reset the device (bit clears itself)
ALLOW_ PKTCC	6	**Allow Packet Control Channel:** Set this bit to 1 before turning on the packet-based control channel	0: Do not allow special signal to turn on packet-based control channel 1: Allow special signal to turn on packet-based control channel
RSVD	5	**Reserved:** Do not change from default value	0: Reserved
RSVD	4	**Reserved:** Do not change from default value	0: Reserved
RSVD	3	**Reserved:** Do not change from default value	0: Reserved
RSVD	2	**Reserved:** Do not change from default value	0: Reserved
RSVD	1:0	**Reserved:** Do not change from default value	10: Reserved

pktcc_lock (0x14)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD	RSVD	RSVD	RSVD	CC_ WBLOCK	REM_ CCLOCK
Reset	XXb		Xb	Xb	Xb	Xb	Xb	Xb
Access Type	Read Only		Read Only	Read Only	Read Clears All	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	**Reserved**	XX: Reserved
RSVD	5	**Reserved**	X: Reserved
RSVD	4	**Reserved**	X: Reserved
RSVD	3	**Reserved**	X: Reserved
RSVD	2	**Reserved**	X: Reserved
CC_ WBLOCK	1	**Control-Channel Word Boundary Locked**	0: Control-channel word boundary is not locked 1: Control-channel word boundary is locked
REM_ CCLOCK	0	**Remote-Side Control Channel Locked**	0: Remote side control channel is not locked 1: Remote side control channel is locked

input_status (0x15)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	OUTPUTEN	PCLKDET
Reset	Xb	Xb	Xb	0b	0b	0b	Xb	Xb
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved**	X: Reserved
RSVD	6	**Reserved**	X: Reserved
RSVD	5	**Reserved**	X: Reserved
RSVD	4	**Reserved**	0: Reserved
RSVD	3	**Reserved**	0: Reserved
RSVD	2	**Reserved**	0: Reserved
OUT-PUTEN	1	**Output Enabled**	0: Output disabled 1: Output enabled
PCLKDET	0	**PCLK Detected:** Valid PCLK detected	0: No valid PCLK detected 1: Valid PCLK detected

max_rt_err (0x16)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MAX_RT_ERR	RSVD[5:0]					
Reset	0b	Xb	XXXXXXb					
Access Type	Read Only	Read Clears All	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved**	0: Reserved
MAX_RT_ERR	6	**Maximum Retransmission Error:** maximum retransmission error bit Goes high if packet control channel hits maximum retransmission limit. Cleared when read	0: Device has not reached maximum retransmission limit. 1: Device has reached maximum retransmission limit.
RSVD	5:0	**Reserved**	XXXXXX: Reserved

rsvd_17 (0x17)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	XXXXXXXXb							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:0	**Reserved**	XXXXXXXX: Reserved

crc (0x18 to 0x1B)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE[7:0]							
Reset	XXXXXXXXb							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE	7:0	**CRC Value:** CRC output for latest line CRC_VALUE_3 to CRC_VALUE_0 represents CRC[31:0]	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

cc_crc_errcnt (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_ERRCNT[7:0]							
Reset	XXXXXXXXb							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERRCNT	7:0	**Control-Channel CRC Error Count:** Packet-based control-channel CRC error counter	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

rsvd_1d (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	XXXXXXXXb							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:0	**Reserved**	XXXXXXXX: Reserved

id (0x1E)

BIT	7	6	5	4	3	2	1	0
Field	ID[7:0]							
Reset	XXXXXXXXb							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ID	7:0	**Device ID:** 8-bit value depends on the GMSL device attached	01000101 Device is a MAX96701A

revision (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	HDCPCAP	REVISION[3:0]			
Reset	0b	0b	0b	Xb	XXXXb			
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved**	0: Reserved
RSVD	6	**Reserved**	0: Reserved
RSVD	5	**Reserved**	0: Reserved
HDCPCAP	4	**HDCP Capability:** 1 = HDCP capable	0: Device does not have HDCP 1: Device is HDCP capable
REVISION	3:0	**Device Revision**	0000: Value is 0 0001: Value is 1 1111: Value is 15

crossbar (0x20 to 0x3E)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	FORCE_ MUX	INVERT_ MUX	CROSSBAR[4:0]				
Reset	0b	0b	0b	XXXXXb				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
FORCE_ MUX	6	**Force Mux Output**	0: Input mapped to mux output 1: Force mux output low
INVERT_ MUX	5	**Invert Mux Output**	0: Do not invert mux output 1: Invert mux output
CROSS-BAR	4:0	**Crossbar Setting** Select 1 of 32 input signals. Default values connect Mux N with input N for flow-through routing (i.e., DIN_ mapped to DOUT_)	00000: Mux outputs data from input 0 00001: Mux outputs data from input 1 11111: Mux outputs data from input 31

crossbar_hs (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	FORCE_ MUX_HS	INVERT_ MUX_HS	CROSSBARHS[4:0]				
Reset	0b	0b	0b	01100b				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
FORCE_ MUX_HS	6	**Force Mux Output**	0: Input mapped to mux output 1: Force mux output low
INVERT_ MUX_HS	5	**Invert Mux Output**	0: Do not invert mux output 1: Invert mux output
CROSS-BARHS	4:0	**Crossbar Setting HS:** Select 1 of 16 input pins for HS. Default values connect HS with the corresponding named input pin. Use unconnected inputs (DIN14, DIN15) when generating sync signals with the timing generator.	00000: Mux sync signal from DIN0 00001: Mux sync signal from DIN1 01111: Mux sync signal from DIN15 1XXXX: **Do Not Use**

crossbar (0x40)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	FORCE_ MUX_VS	INVERT_ MUX_VS	CROSSBARVS[4:0]				
Reset	0b	0b	0b	01101b				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
FORCE_ MUX_VS	6	**Force Mux Output**	0: Input mapped to mux output 1: Force mux output low
INVERT_ MUX_VS	5	**Invert Mux Output**	0: Do not invert mux output 1: Invert mux output
CROSS-BARVS	4:0	**Crossbar Setting VS:** Select 1 of 16 input pins for VS. Default values connect VS with the corresponding named input pin. Use unconnected inputs (DIN14, DIN15) when generating sync signals with the timing generator.	00000: Mux sync signal from DIN0 00001: Mux sync signal from DIN1 01111: Mux sync signal from DIN15 1XXXX: **Do Not Use**

crossbar_de (0x41)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	FORCE_ MUX_DE	INVERT_ MUX_DE	CROSSBARDE[4:0]				
Reset	0b	0b	0b	01011b				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
FORCE_ MUX_DE	6	**Force Mux Output**	0: Input mapped to mux output. 1: Force mux output low.
INVERT_ MUX_DE	5	**Invert Mux Output**	0: Do not invert mux output. 1: Invert mux output.
CROSS-BARDE	4:0	**Crossbar Setting DE:** Select 1 of 16 input pins for DE. Default values connect DE with DIN11. Unconnected inputs (DIN14, DIN15) when generating sync signals with the timing generator.	00000: Mux sync signal from DIN0 00001: Mux sync signal from DIN1 01111: Mux sync signal from DIN15 1XXXX: **Do Not Use**

link_config (0x42)

BIT	7	6	5	4	3	2	1	0
Field	LINE_CRC_LOC[1:0]		LINE_CRC_ EN	MAX_RT_ EN	RSVD	GPI_ COMP_EN	GPI_RT_EN	GPO_EN
Reset	01b		0b	1b	1b	0b	1b	1b
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_ LOC	7:6	**Line CRC Location:** Video line CRC insertion location	00: CRC insertion at [1...4] 01: CRC insertion at [5...8] 10: CRC insertion at [9...12] 11: CRC insertion at [13...16]
LINE_CRC_ EN	5	**Line CRC Enable:** Video line CRC enable	0: Disable CRC 1: Enable CRC
MAX_RT_EN	4	**Maximum Retransmission Limit Enable**	0: Disable maximum retransmission limit 1: Enable maximum retransmission limit
RSVD	3	**Reserved:** Do not change from default value	1: Reserved
GPI_COMP_ EN	2	**GPI Compensation Enable**	0: Disable GPI compensation 1: Enable GPI compensation
GPI_RT_EN	1	**GPI Retransmission Enable**	0: Disable GPI retransmission 1: Enable GPI retransmission
GPO_EN	0	**GPO Enable:** Enable GPO pin	0: Disable GPO pin 1: Enable GPO pin

sync_gen_config (0x43)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	GEN_VS	GEN_HS	GEN_DE	VS_TRIG	VTG_MODE[1:0]	
Reset	0b	0b	0b	0b	0b	1b	01b	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
RSVD	6	**Reserved:** Do not change from default value	0: Reserved
GEN_VS	5	**VSYNC Generation:** Enable to generate VS output according to the timing definition	0: Disable VS output generation (VS used from input) 1: Enable VS output generation (VS internally generated)
GEN_HS	4	**HSYNC Generation:** Enable to generate HS utput according to the timing definition	0: Disable HS output generation (HS used from input) 1: Enable HS output generation (HS internally generated)
GEN_DE	3	**DE Generation:** Enable to generate DE output according to the timing definition	0: Disable DE output generation (DE used from input) 1: Enable DE output generation (DE internally generated)
VS_TRIG	2	**VSYNC Trigger Edge Select**	0: VS trigger uses falling edge 1: VS trigger uses rising edge
VTG_ MODE	1:0	**Video Timing Generator Mode**	00: VS input is tracked and then locked after three consecutive matches (three consecutive mismatches unlock tracking) 01: VS edge triggers one VS frame (current frame is extended/cut short to adjust timing to next trigger) 10: VS edge triggers VS generation (current frame is extended/cut short to adjust timing to next trigger) 11: Same as above

vs_dly (0x44 to 0x46)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY	7:0	**VSYNC Delay:** VS delay in terms of PCLK cycles; the output VS delay by VS_DELAY cycles from the input VS	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

vs_h (0x47 to 0x49)

BIT	7	6	5	4	3	2	1	0
Field	VS_H[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_H	7:0	**VSYNC High:** VS high period in terms of PCLK cycles	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

vs_l (0x4A to 0x4C)

BIT	7	6	5	4	3	2	1	0
Field	VS_L[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_L	7:0	**VSYNC Low:** VS low period in terms of PCLK cycles	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

cxtp (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	HIGHIMM	CXTP	RSVD	RSVD	VSYNC_INV	HSYNC_INV	DE_INV	RSVD
Reset	Xb	1b	0b	0b	0b	0b	0b	0b
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HIGHIMM	7	**High Immunity Mode:** Default value depends on the state of the HIM input	0: Use legacy reverse channel mode 1: Use high immunity mode
CXTP	6	**Coax/Twisted Pair Select:** Default to STP mode	0: Use differential output (STP mode) 1: Use dual single ended outputs (coax)
RSVD	5	**Reserved:** Do not change from default value	0: Reserved
RSVD	4	**Reserved:** Do not change from default value	0: Reserved
VSYNC_ INV	3	**VSYNC Inversion:** Invert output VSYNC in TIMING GEN	0: Do not invert VS in timing generator 1: Invert VS in timing generator
HSYNC_ INV	2	**HSYNC Inversion:** Invert output HSYNC in TIMING GEN	0: Do not invert HS in timing generator 1: Invert HS in timing generator
DE_INV	1	**DE Inversion:** Invert output DE in TIMING GEN	0: Do not invert DE in timing generator 1: Invert DE in timing generator
RSVD	0	**Reserved:** Do not change from default value	0: Reserved

hs_dly (0x4E to 0x50)

BIT	7	6	5	4	3	2	1	0
Field	HS_DLY[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_DLY	7:0	**VSYNC to HSYNC Delay:** VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [15:8])	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

rsvd (0x51 to 0x53, 0x5D to 0x5F)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:0	**Reserved:** Do not change from default value	00000000: Reserved

hs_h (0x54, 0x55)

BIT	7	6	5	4	3	2	1	0
Field	HS_H[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_H	7:0	**HSYNC High Period:** HS high period in terms of PCLK cycles	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

hs_l (0x56, 0x57)

BIT	7	6	5	4	3	2	1	0
Field	HS_L[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_L	7:0	**HSYNC Low Period:** HS low period in terms of PCLK cycles	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

hs_cnt (0x58, 0x59)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT	7:0	**HSYNC Count:** Lines per panel (bits [7:0]).	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

de_dly (0x5A to 0x5C)

BIT	7	6	5	4	3	2	1	0
Field	DE_DLY[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DLY	7:0	**VSYNC to DE:** VS falling edge to the rising edge of the first DE in terms of PCLK cycles	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

de_h (0x60, 0x61)

BIT	7	6	5	4	3	2	1	0
Field	DE_H[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_H	7:0	**DE High Period:** DE high period in terms of PCLK cycles	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

de_l (0x62, 0x63)

BIT	7	6	5	4	3	2	1	0
Field	DE_L[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_L	7:0	**DE Low Period:** DE low period in terms of PCLK cycles	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

de_cnt (0x64, 0x65)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT	7:0	**DE Count:** Active lines per panel	00000000: Value is 0 00000001: Value is 1 11111111: Value is 255

prbs_type (0x66)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		PRBS_ TYPE	REV_FAST	DE_EN	DIS_ RWAKE	RSVD	CXSEL
Reset	01b		1b	0b	0b	0b	0b	1b
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	**Reserved:** Do not change from default value	01: Reserved
PRBS_ TYPE	5	**PRBS Type:** PRBS type select	0: Select legacy PRBS mode 1: Select MAX9271–MAX9273 PRBS mode
REV_ FAST	4	**Reverse Channel Fast-Mode Enable**	0: Disable reverse channel fast mode 1: Enable reverse channel fast mode
DE_EN	3	**DE Enable:** Enable processing separate HS and DE signals	0: Disable separate processing of HS and DE signals 1: Enable separate processing of HS and DE signals
DIS_ RWAKE	2	**Disable Remote Wake-Up:** Disable wake-up receiver	0: Do not disable remote wake-up receiver 1: Disable remote wake-up receiver
RSVD	1	**Reserved:** Do not change from default value	0: Reserved
CXSEL	0	**Coax Select**	0: Coax cable connected to inverting output 1: Coax cable connected to noninverting output

dbl_align_to (0x67)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		AUTO_ CLINK	RSVD	RSVD	DBL_ALIGN_TO[2:0]		
Reset	11b		0b	0b	0b	111b		
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	**Reserved:** Do not change from default value	11: Reserved
AUTO_ CLINK	5	**Auto Configuration Link:** Automatic control of configuration link	0: Enable configuration link only when CLINKEN = 1 and SEREN = 0 1: Automatically enable configuration link when SEREN = 1 and PCLKDET = 0
RSVD	4	**Reserved:** Do not change from default value	0: Reserved
RSVD	3	**Reserved:** Do not change from default value	0: Reserved
DBL_ ALIGN_TO	2:0	**Double Alignment Mode:** Sets the alignment mode when DBL = 1 in the serializer and DBL = 0 in the deserializer. Set DBL_ALIGN_TO = 000 when an external high-low signal is used (EN_HI_LO =1).	000: Align at each rising edge of HS. Turn off alignment after HS is low (MAX9286). Use this setting when an external high/low signal is used. 001: Do not use 010: Force align 011: Do not use 100: Align at each rising edge of HS 101: Align at each rising edge of DE 110: Force align 111: No alignment done while in DBL mode

cc_crc_length (0x68)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD[2:0]			RSVD[1:0]		CC_CRC_LENGTH[1:0]	
Reset	0b	001b			10b		01b	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
RSVD	6:4	**Reserved:** Do not change from default value	001: Reserved
RSVD	3:2	**Reserved:** Do not change from default value	10: Reserved
CC_CRC_ LENGTH	1:0	**Control-Channel CRC Length**	00: 1-bit CC CRC length 01: 5-bit CC CRC length 10: 8-bit CC CRC length 11: **Do not use**

hi_lo (0x69)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	EN_HI_LO	INVERT_ HI_LO	CROSSBAR_HI_LO[4:0]				
Reset	0b	0b	0b	01101				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
EN_HI_LO	6	**Enable High/Low Signal Alignment**	0: Do not align using a Hi-Lo signal 1: Use a Hi-Lo signal to align input data
INVERT_ HI_LO	5	**Invert High/Low Signal Alignment**	0: Do not invert Hi-Lo signal 1: Invert Hi-Lo signal
CROSS-BAR_HI_ LO	4:0	**Crossbar High Low:** Select 1 of 16 input pins for the Hi-Lo signal. (effective when DBL_ALIGN_TO = 000)	00000: Mux Hi-Lo signal from DIN0 00001: Mux Hi-Lo signal from DIN1 01111: Mux Hi-Lo signal from DIN15 1XXXX: **Do Not Use**

rsvd_96 (0x96)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD[1:0]	
Reset	0b	0b	0b	0b	0b	1b	10b	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
RSVD	6	**Reserved:** Do not change from default value	0: Reserved
RSVD	5	**Reserved:** Do not change from default value	0: Reserved
RSVD	4	**Reserved:** Do not change from default value	0: Reserved
RSVD	3	**Reserved:** Do not change from default value	0: Reserved
RSVD	2	**Reserved:** Do not change from default value	1b: Reserved
RSVD	1:0	**Reserved:** Do not change from default value	10: Reserved

rsvd_97 (0x97)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD[2:0]		
Reset	0b	0b	0b	1b	1b	111b		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
RSVD	6	**Reserved:** Do not change from default value	0: Reserved
RSVD	5	**Reserved:** Do not change from default value	0: Reserved
RSVD	4	**Reserved:** Do not change from default value	1: Reserved
RSVD	3	**Reserved:** Do not change from default value	1: Reserved
RSVD	2:0	**Reserved:** Do not change from default value	111: Reserved

rsvd_98 (0x98)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD[2:0]			RSVD[2:0]		
Reset	01b		001b			010b		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	**Reserved:** Do not change from default value	01: Reserved
RSVD	5:3	**Reserved:** Do not change from default value	001: Reserved
RSVD	2:0	**Reserved:** Do not change from default value	010: Reserved

rsvd_99 (0x99)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD[1:0]	
Reset	0b	0b	0b	0b	1b	1b	01b	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
RSVD	6	**Reserved:** Do not change from default value	0: Reserved
RSVD	5	**Reserved:** Do not change from default value	0: Reserved
RSVD	4	**Reserved:** Do not change from default value	0: Reserved
RSVD	3	**Reserved:** Do not change from default value	1: Reserved
RSVD	2	**Reserved:** Do not change from default value	1: Reserved
RSVD	1:0	**Reserved:** Do not change from default value	01: Reserved

pktcc_en (0x9A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD[1:0]		PKTCC_EN	RSVD[1:0]		RSVD
Reset	00b		01b		0b	00b		0b
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	**Reserved:** Do not change from default value	00: Reserved
RSVD	5:4	**Reserved:** Do not change from default value	01: Reserved
PKTCC_ EN	3	**Packet-Based Control-Channel-Mode Enable.** Must set ALLOW_PKTCC before setting this bit. See the *Packet-Based I²C* section for details on operation of this bit.	0: Disable packet-based control-channel mode 1: Enable packet-based control-channel mode
RSVD	2:1	**Reserved:** Do not change from default value	00: Reserved
RSVD	0	**Reserved:** Do not change from default value	0: Reserved

rsvd_C8 (0xC8)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD[3:2]		RSVD[1:0]	
Reset	0b	Xb	Xb	Xb	10b		10b	
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only		Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved**	0: Reserved
RSVD	6	**Reserved**	X: Reserved
RSVD	5	**Reserved**	X: Reserved
RSVD	4	**Reserved**	X: Reserved
RSVD	3:2	**Reserved**	10: Reserved
RSVD	1:0	**Reserved**	10: Reserved

rsvd_c9 (0xC9)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	XXXXXXXXb							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:0	**Reserved**	XXXXXXXX: Reserved

rsvd_fc (0xFC)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Reset	0b	0b	0b	0b	0b	0b	0b	0b
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
RSVD	6	**Reserved:** Do not change from default value	0: Reserved
RSVD	5	**Reserved:** Do not change from default value	0: Reserved
RSVD	4	**Reserved:** Do not change from default value	0: Reserved
RSVD	3	**Reserved:** Do not change from default value	0: Reserved
RSVD	2	**Reserved:** Do not change from default value	0: Reserved
RSVD	1	**Reserved:** Do not change from default value	0: Reserved
RSVD	0	**Reserved:** Do not change from default value	0: Reserved

rsvd_fd (0xFD)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	00000000b							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:0	**Reserved:** Do not change from default value	00000000: Reserved

rsvd_fe (0xFE)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				RSVD[3:0]			
Reset	0000b				0000b			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:4	**Reserved:** Do not change from default value	0000: Reserved
RSVD	3:0	**Reserved:** Do not change from default value	0000: Reserved

rsvd_ff (0xFF)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD[3:0]			
Reset	0b	0b	0b	0b	XXXXb			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	**Reserved:** Do not change from default value	0: Reserved
RSVD	6	**Reserved:** Do not change from default value	0: Reserved
RSVD	5	**Reserved:** Do not change from default value	0: Reserved
RSVD	4	**Reserved:** Do not change from default value	0: Reserved
RSVD	3:0	**Reserved**	XXXX: Reserved

Applications Information

Parallel Interface

The CMOS parallel interface-data width is programmable and depends on the application. Using a larger width (BWS = 1) results in a lower-pixel clock rate, while a smaller width (BWS = 0) allows a higher-pixel clock rate.

Bus Data Width

The bus data width depends on the selected modes. The available bus width is less when using error detection or when in double mode (DBL = 1). Table 3 shows the available bit widths and default mapping for various modes.

Bus Data Rates

The bus data rate depends on the settings for BWS and DBL. Table 4 lists the available PCLK rates available for different bus-width settings. For lower PCLK rates, set DBL = 0 (if DBL = 1 in both the serializer and deserializer).

Table 3. Input Data-Width Selection

REGISTER BIT SETTINGS					INPUT MAPPING
DBL	BWS	HIBW	PXL_CRC	HVEN	
1	1	—	1	1	DIN11:0, HS, VS
1	1	—	1	0	DIN11:0
1	1	—	0	1	DIN11:0*, HS, VS
1	1	—	0	0	DIN13:0*
1	0	1	1	—	DIN8:0, HS, VS
1	0	1	0	—	DIN11:0, HS, VS
1	0	0	1	1	DIN7:0, HS, VS
1	0	0	1	0	DIN7:0
1	0	0	0	1	DIN10:0, HS, VS
1	0	0	0	0	DIN10:0
0	1	—	1	1	DIN11:0*, HS, VS
0	1	—	1	0	DIN13:0*
0	1	—	0	1	DIN11:0*, HS, VS
0	1	—	0	0	DIN13:0*
0	0	1	-	—	DIN11:0*, HS, VS
0	0	0	1	1	DIN11:0*, HS, VS
0	0	0	1	0	DIN13:0*
0	0	0	0	1	DIN11:0*, HS, VS
0	0	0	0	0	DIN13:0*

**The input bit width is limited by the number of available inputs.*

Table 4. Data-Rate Selection

DBL	BWS	HIBW	PCLK RANGE (MHz)
1	1	0	25 to 87
1	0	0	33.3 to 116
1	0	1	73.3 to 116
0	1	0	12.5 to 43.5
0	0	0	16.7 to 58
0	0	1	36.6 to 58

Crossbar Switch

By default, the crossbar switch connects the serializer input pins DIN_ and HS/VS (when HV encoding is used) to the corresponding deserializer output pins DOUT_ and HS/VS. Reprogram the crossbar switch when changing the input or output pin assignments, or when connecting to devices that do not have a DBL = 1 mode.

Crossbar-Switch Programming

Each crossbar-switch output can select any of the 14 DIN_ inputs for either high or low words (when DBL = 1) for a total of 32 possible inputs. Multiple outputs can share the same input. HS, VS, and DE remain the same for both word halves, and should be programmed to use the low-word input of the corresponding pin. To invert an input data bit, set the respective INVERT_MUX_ = 1. To force an output low, (and ignore the input) set the FORCE_MUX_ bit = 1. To force an output high set both INVERT_MUX_ and FORCE_MUX_ = 1.

Recommended Crossbar-Switch Program Procedure

The procedure to program the crossbar switch depends on the DBL settings on the serializer and deserializer. Devices without double mode can be assumed to have DBL = 0.

- Both Devices' DBL Set to the Same Value

1) For the crossbar-output equivalent of DIN0 (XBO0, XBO16) select which pin to map (e.g., DIN4→XBI4, XBI20).
2) Set the low- and high-input crossbar bits (CROSSBAR0, CROSSBAR 16) to the desired selected mapped input (e.g., CROSSBAR0 = 00100, CROSSBAR16 = 10100).
3) Repeat for the other crossbar outputs, making sure the set of high and low crossbar outputs are assigned to the same crossbar input set. In general, XBO[i] and XBO[i+16] should be assigned to XBI[j] and XBI[j+16].
4) For XBOHS, XBOVS, and XBODE, set crossbar to use the low-input pins (CROSSBAR_ = 00000 to 01111). Note that HS, VS, and DE use both the low and high input.

- Both Devices' DBL Do Not Match

1) Table 5, Table 6, and Table 7 list which crossbar output (XBO_) maps to each serial bit.
2) For each crossbar output, select which pin and high/low clock cycle (if needed) to map (e.g., DIN4 low input).
3) Set the crossbar bits (CROSSBAR_) to select the desired selected mapped input (e.g., CROSSBAR0 = 00100 maps DIN4 low input to XBO0).
4) Repeat for the other crossbar outputs; any unused serial bits should have a force low mapped to the respective crossbar output.
5) For XBOHS, XBOVS, and XBODE, set crossbar to use the low-input pins (CROSSBAR_ = 00000 to 01111). Note that HS, VS, and DE use both the low and high input.

Table 5. Crossbar Output to Serial Link Map (D23:0)

BIT SETTING						SERIAL BITS																					
DB	HV	BW	HB	CR	DE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0	0	0	0	0	X	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Z	Z	Z	Z	Z	Z	F	P
0	0	0	0	1	X	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	F	E	E	E	E	E	E	P
0	0	0	1	0	X	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Z	Z	Z	Z	Z	Z	F	P
0	0	0	1	1	X	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Z	Z	Z	F	E	E	E	P
0	0	1	0	0	X	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Z	Z	Z	Z	Z	Z	Z	Z
0	0	1	0	1	X	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Z	Z	Z	Z	Z	Z	Z	Z
0	1	0	0	0	X	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Z	Z	Z	Z	Z	Z	F	P
0	1	0	0	1	X	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	F	E	E	E	E	E	E	P
0	1	1	0	0	X	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Z	Z	Z	Z	Z	Z	Z	Z
0	1	1	0	1	X	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Z	Z	Z	Z	Z	Z	Z	Z
1	0	0	0	0	X	16	17	18	19	20	21	22	23	24	25	26	0	1	2	3	4	5	6	7	8	9	10	F	P
1	0	0	0	1	X	16	17	18	19	20	21	22	23	0	1	2	3	4	5	6	7	F	E	E	E	E	E	E	P
1	0	0	1	0	X	16	17	18	19	20	21	22	23	24	25	26	27	0	1	2	3	4	5	6	7	8	Z	F	P

Table 5. Crossbar Output to Serial Link Map (D23:0) (continued)

BIT SETTING						SERIAL BITS																					
DB	HV	BW	HB	CR	DE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
1	0	0	1	1	X	16	17	18	19	20	21	22	23	24	0	1	2	3	4	5	6	7	8	Z	F	E	E	E	P
1	0	1	0	0	X	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	0	1	2	3	4	5	6	7	8
1	0	1	0	1	1	16	17	18	19	20	21	22	23	24	25	26	DH	0	1	2	3	4	5	6	7	8	9	10	DL
1	0	1	0	1	0	16	17	18	19	20	21	22	23	24	25	26	27	0	1	2	3	4	5	6	7	8	9	10	11
1	1	0	0	0	1	16	17	18	19	20	21	22	23	24	25	DH	0	1	2	3	4	5	6	7	8	9	DL	F	P
1	1	0	0	0	0	16	17	18	19	20	21	22	23	24	25	26	0	1	2	3	4	5	6	7	8	9	10	F	P
1	1	0	0	1	1	16	17	18	19	20	21	22	DH	0	1	2	3	4	5	6	DL	F	E	E	E	E	E	E	P
1	1	0	0	1	0	16	17	18	19	20	21	22	23	0	1	2	3	4	5	6	7	F	E	E	E	E	E	E	P
1	1	1	0	0	X	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	0	1	2	3	4	5	6	7	8
1	1	1	0	1	1	16	17	18	19	20	21	22	23	24	25	26	DH	0	1	2	3	4	5	6	7	8	9	10	DL
1	1	1	0	1	0	16	17	18	19	20	21	22	23	24	25	26	27	0	1	2	3	4	5	6	7	8	9	10	11

Table 6. Crossbar Output to Serial Link Map (D31:24 and Special Packets)

BIT SETTING														SPECIAL PACKETS						
DB	HV	BW	HB	CR	DE	24	25	26	27	28	29	30	31	C0	C1	C2	C3	HS	VS	DE
0	0	0	0	0	X	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
0	0	0	0	1	X	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
0	0	0	1	0	X	Z	Z	Z	—	—	—	—	—	Z	Z	Z	Z	H	V	D
0	0	0	1	1	X	E	E	E	—	—	—	—	—	Z	Z	Z	Z	H	V	D
0	0	1	0	0	X	Z	Z	Z	Z	Z	Z	F	P	—	—	—	—	—	—	—
0	0	1	0	1	X	F	E	E	E	E	E	E	P	—	—	—	—	—	—	—
0	1	0	0	0	X	—	—	—	—	—	—	—	—	—	—	—	—	H	V	—
0	1	0	0	1	X	—	—	—	—	—	—	—	—	—	—	—	—	H	V	—
0	1	1	0	0	X	Z	Z	Z	Z	Z	Z	F	P	—	—	—	—	H	V	—
0	1	1	0	1	X	F	E	E	E	E	E	E	P	—	—	—	—	H	V	—
1	0	0	0	0	X	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
1	0	0	0	1	X	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
1	0	0	1	0	X	9	10	11	—	—	—	—	—	A	Z	A	A	H	V	D
1	0	0	1	1	X	E	E	E	—	—	—	—	—	A	Z	A	A	H	V	D
1	0	1	0	0	X	9	10	11	12	13	14	F	P	—	—	—	—	—	—	—
1	0	1	0	1	1	F	E	E	E	E	E	E	P	—	—	—	—	—	—	—
1	0	1	0	1	0	F	E	E	E	E	E	E	P	—	—	—	—	—	—	—
1	1	0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	HH/L	VH/L	—
1	1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	HH/L	VH/L	—
1	1	0	0	1	1	—	—	—	—	—	—	—	—	—	—	—	—	HH/L	VH/L	—
1	1	0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	HH/L	VH/L	—
1	1	1	0	0	X	9	10	11	12	13	14	F	P	—	—	—	—	HH/L	VH/L	—
1	1	1	0	1	1	F	E	E	E	E	E	E	P	—	—	—	—	HH/L	VH/L	—
1	1	1	0	1	0	F	E	E	E	E	E	E	P	-	-	-	-	HH/L	VH/L	-

Table 7. Legend

BIT SETTINGS		MAP INPUTS	
DB	Double-mode bit DBL	H	HSYNC (when DBL = 0 or HIBW = 1)
HV	H/V Encoding bit HVEN	V	VSYNC (when DBL = 0 or HIBW = 1)
BW	BWS bit	D	DE (when DBL = 0 or HIBW = 1)
HB	HIBW bit	HH	HSYNC (high word, DBL = 1)
CR	PXL_CRC bit	VH	VSYNC (high word, DBL = 1)
DE	DE = 1 when DEEN = 1 and not processed in RGB888 mode	DH	DE (high word, DBL = 1)
X	1 or 0	HL	HSYNC (low word, DBL = 1)
SPECIAL PACKETS		VL	VSYNC (low word, DBL = 1)
C0	CNT_0	DL	DE (low word, DBL = 1)
C1	CNT_1	#	XBO output from crossbar switch
C2	CNT_2	F	Internal forward control-channel bit
C3	CNT_3	E	Internal pixel CRC bit
BIT COLOR		P	Internal pixel parity bit
	Output bits from crossbar	—	Serial bit not sent
	Internal bits	Z	Zero
	Other output bits	A	Internal alignment bit (used when HIBW=1)
	Output bits from sync		

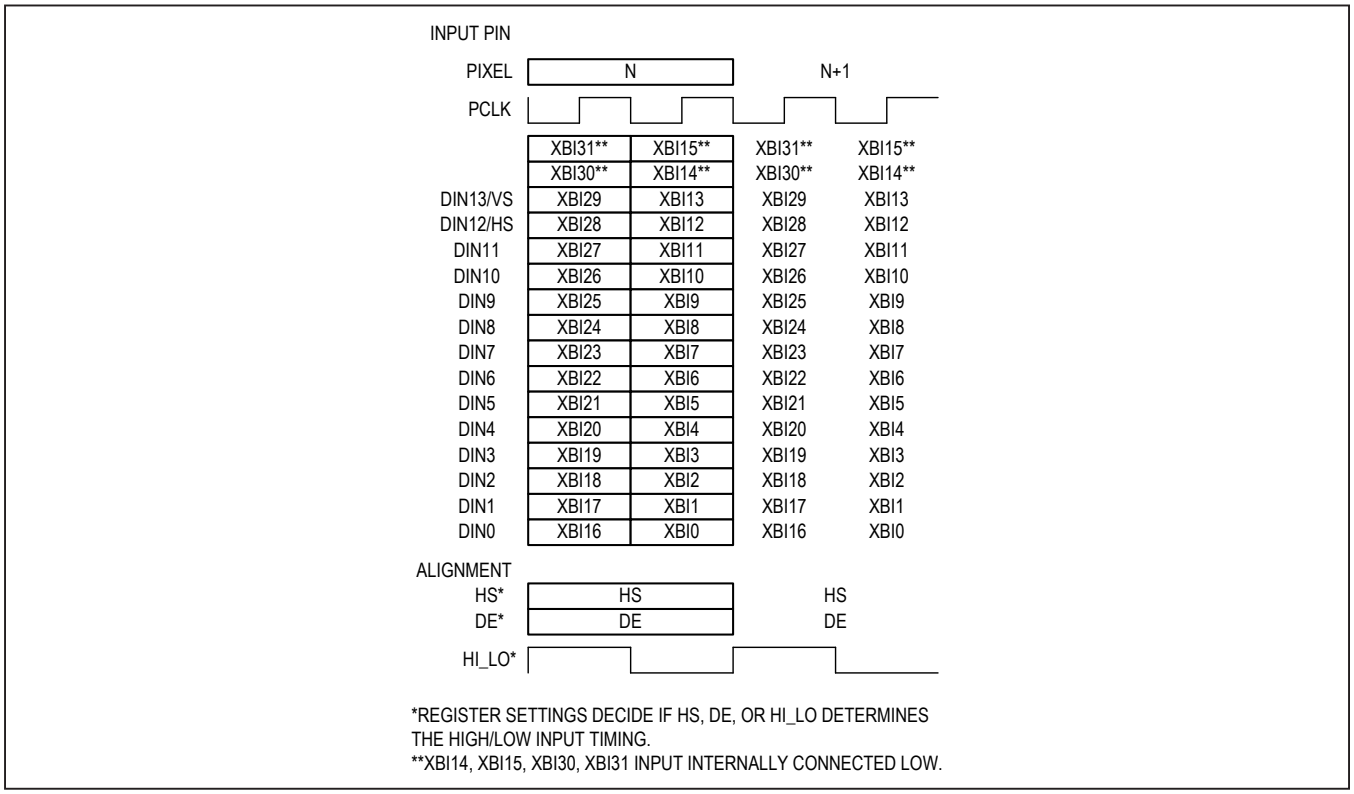


Figure 20. Crossbar-Switch Default Mapping

Timing-Generator Programming

Timing-generator parameters are stored in the registers as unsigned integers as PCLK periods. To prevent output glitches, program all timing-generator parameters while the device is in configuration-link mode, or when PCLK is not applied. By default, the timing generator is set to single trigger, and is disabled. Figure 18 show the timing waveforms under the default conditions with rising-edge trigger, and noninverted signals. Do not program the HSYNC or DE signals such that the total length exceeds the length of a VSYNC period (Table 8). All delay parameters are positive. To implement a negative delay, set the delay value subtracted from the VSYNC period (e.g., a delay value of VS_HIGH + VS_LOW - N creates a delay of -N PCLK cycles). Do not set any delay lengths larger than the VSYNC period.

Double-Mode Alignment

When DBL = 1 in both the serializer and deserializer, GMSL automatically keeps the pixels in order. Use double-mode alignment when DBL = 1 in the serializer and DBL = 0 (or is not supported) in the deserializer. Two different methods are available for double-mode alignment.

External High/Low Signal

To use an external alignment signal, set EN_HI_LO = 1, DBL_ALIGN_TO = 000, and select which input DIN_ pin to use by setting the CROSSBAR_HI_LO bits. The external signal designates whether the clocked word is the high or low word (e.g., for pixels [1H, 1L, 2H, 2L...] the high/low signal would be [1, 0, 1, 0...]).

Align from HS or DE

To align from a sync signal, set the DBL_ALIGN_TO to select the input signal. When using this mode, ensure that the signal used for alignment uses the same value for both the high and low word (e.g., for pixels [1H, 1L, 2H, 2L...], aligning on DE requires values of [DE1, DE1, DE2, DE2...]).

I^2C Interface

The control channel forwards I^2C commands from the microcontroller side to the other side of the GMSL link. The remote device acts as an I^2C master to the other peripherals connected to the remote-side device. I^2C-to-I^2C mode uses clock stretching to hold the microcontroller until the data and an acknowledge or not acknowledge have been sent across the link.

I^2C Bit Rate

The I^2C interface accepts bit rates from 9.6kbps to 1Mbps. The local I^2C rate is set by the microcontroller. The remote I^2C rate is set by the remote device. By default, the control channel is set up for a 400kbps I^2C bit rate. Program the I2C_MSTBT and SLV_SH bits (register 0x0D) to match the desired microcontroller I^2C rate.

Table 8. Timing-Generator Parameter Restrictions

SIGNAL	SIZE (BITS)	MIN VALUE (HEX)	MAXIMUM VALUE RESTRICTION (HEX)
VS_HIGH	24	1	VS_HIGH + VS_LOW < 0xFFFFFF
VS_LOW	24	1	VS_HIGH + VS_LOW < 0xFFFFFF
VS_DLY	24	0	VS_DLY < VS_HIGH + VS_LOW
HS_HIGH	16	1	(HS_HIGH + HS_LOW) x HS_CNT < VS_HIGH + VS_LOW
HS_LOW	16	1	(HS_HIGH + HS_LOW) x HS_CNT < VS_HIGH + VS_LOW
HS_CNT	16	1	(HS_HIGH + HS_LOW) x HS_CNT < VS_HIGH + VS_LOW
HS_DLY	24	0	HS_DLY < VS_HIGH + VS_LOW
DE_HIGH	16	1	(DE_HIGH + DE_LOW) x DE_CNT < VS_HIGH + VS_LOW
DE_LOW	16	1	(DE_HIGH + DE_LOW) x DE_CNT < VS_HIGH + VS_LOW
DE_CNT	16	1	(DE_HIGH + DE_LOW) x DE_CNT < VS_HIGH + VS_LOW
DE_DLY	24	0	DE_DLY < VS_HIGH + VS_LOW

Software Programming of Device Addresses

The serializer and deserializer have programmable device addresses. This allows multiple GMSL devices, along with I²C peripherals, to coexist on the same control channel. The serializer device address is in register 0x00 of each device, while the deserializer device address is in register 0x01 of each device. To change a device address, first write to the device whose address changes (register 0x00 of the serializer for serializer device address change, or register 0x01 of the deserializer for deserializer device address change). Then, write the same address into the corresponding register on the other device (register 0x00 of the deserializer for serializer device address change, or register 0x01 of the serializer for deserializer device address change).

I²C Address Translation

The device supports I²C address translation for up to two device addresses. Use address translation to assign unique device addresses to peripherals with limited I²C addresses. Source addresses (address to translate from) are stored in registers 0x09 and 0x0B. Destination addresses (address to translate to) are stored in registers 0x0A and 0x0C.

Configuration Blocking

The device can block changes to its registers. Set CFGBLOCK to make all registers read-only. Once set, the registers remain blocked until the supplies are removed.

Cascaded/Parallel Devices

GMSL supports both cascaded and parallel devices connected through I²C. When cascading or using parallel links, all I²C commands are forwarded to all links. Each link attempts to hold the control channel until it receives an acknowledge/not acknowledge from the remote-side device. It is important to keep the control channel active between links to prevent timeout. If a link is unused, keep the control channel clear by turning on the configuration link, disconnecting the I²C lines, or powering down the unused device.

Dual µC Control

Most systems use a single microcontroller; however µCs can reside on each side simultaneously and trade off in running the control channel. Contention occurs if both µCs attempt to use the control channel at the same time. It is up to the user to prevent this contention by implementing a higher level protocol. In addition, the control channel does not provide arbitration between I²C masters on both sides of the link. An acknowledge frame is not generated when communication fails due to contention. If communication across the serial link is not required, the µCs can disable the forward and reverse control channel using the FWDCCEN and REVCCEN bits (0x04, D[1:0]) in the serializer/deserializer. Communication across the serial link is stopped and contention between µCs cannot occur.

Device Address

The serializer/deserializer both have a 7-bit-long slave address stored in registers 0x00 and 0x01. The bit following a 7-bit slave address is the R/W bit, which is low for a write command and high for a read command. The default slave address is 0x80. After startup, a microcontroller can reprogram the slave address as needed.

Spread Spectrum

Program the SS bits in the serializer to turn off spread spectrum in the serializer (Table 9). If the deserializer driven by the serializer has programmable spread spectrum, do not enable spread for both at the same time or their interaction cancels benefits. The deserializer tracks the serializer's spread and passes the spread to the deserializer output. Some spread-spectrum amplitudes can only be used at lower PCLKIN frequencies (Table 10). When the spread spectrum is turned on or off, the serial link stops for several microseconds and then restarts in order for the deserializer to lose and relock to the new serial-data stream. Changing the spread-spectrum amplitude does not cause a loss of lock.

Manual Programming of the Spread-Spectrum Divider

By default, autodetection of the PCLKIN operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV: 0x03,D[5:0]) allows the user to set a modulation frequency (typically 20kHz) according to the PCLKIN frequency.

Equation:

Relation of modulation rate to the PCLKIN frequency:

$$f_M = f_{PCLKIN}/(MOD \times SDIV)$$

where:

f_M = Modulation frequency

f_{PCLKIN} = PCLKIN frequency

MOD = Modulation coefficient given in Table 11

SDIV = 6-bit SDIV setting, manually programmed by the µC

To program the SDIV setting, first look up the modulation coefficient according to the desired bus-width and spread-spectrum settings. Solve the above equation for SDIV using the desired pixel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 11, set SDIV to the maximum value.

Board Layout

Power-Supply Circuits and Bypassing

The serializer uses an AVDD and DVDD of 1.7V to 1.9V. All inputs and outputs, except for the serial output, derive power from DVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

High-Frequency Signals

Separate the LVCMOS logic signals and CML/coax high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML/coax, and LVCMOS logic signals. Layout STP-PCB traces close to each other for a 100Ω differential characteristic impedance. The trace dimensions depend on the type of trace used (microstrip or stripline).

Note: Two 50Ω PCB traces do not have 100Ω differential impedance when brought close together; the impedance goes down when the traces are brought closer. Use a 50Ω trace for the single-ended output when driving coax. Route the PCB traces for differential CML in parallel to maintain the differential characteristic impedance. Avoid via arrays. Keep PCB traces that make up a differential pair equal in length to avoid skew within the differential pair.

Table 9. Output Spread

SS	SPREAD (%)
000	No spread spectrum
001	±0.5% spread spectrum
010	±1.5% spread spectrum (power-up default)
011	±2% spread spectrum
100	No spread spectrum
101	±1% spread spectrum
110	±3% spread spectrum
111	±4% spread spectrum

Table 10. Spread Limitations

BWS = 0 MODE, PCLKIN FREQUENCY (MHz)	BWS = 1 MODE, PCLKIN FREQUENCY (MHz)	SERIAL LINK BIT RATE (MBPS)	AVAILABLE SPREAD RATES
< 33.3 (DBL = 0)	< 25 (DBL = 0)	< 1000	All rates available
< 66.6 (DBL = 1)	< 50 (DBL = 1)		
33.3 to 58 (DBL = 0)	25 to 43.5 (DBL = 0)	≥ 1000	1.5%, 1%, 0.5%
66.6 to 116 (DBL = 1)	50 to 87 (DBL = 1)		

Table 11. Modulation Coefficients and Maximum SDIV Settings

BWS	SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT (DEC)	SDIV UPPER LIMIT (DEC)
1	1	104	40
	0.5	104	63
	3	152	27
	1.5	152	54
	4	204	15
	2	204	30
0	1	80	52
	0.5	80	63
	3	112	37
	1.5	112	63
	4	152	21
	2	152	42

ESD Protection

ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. The serial outputs are rated for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are CS = 100pF and RD = 1.5kΩ (Figure 21). The IEC 61000-4-2 discharge components are CS = 150pF and RD = 330Ω (Figure 22). The ISO 10605 discharge components are CS = 330pF and RD = 2kΩ (Figure 23).

Compatibility with Other GMSL Devices

The device is designed to pair with the MAX96705–MAX96711 family of devices, but interoperates with any GMSL device. See Table 12 for operating limitations.

Device Configuration and Component Selection

Internal Input Pulldowns

The control and configuration inputs include a pulldown resistor to GND; external pulldown resistors are not needed.

Multifunction GPO/HIM

Functions as the GPO output, and as a configuration pin. On power-up, or when reverting from a power-down state, the pins act as the HIM input. After latching the input state, the pin becomes the GPO output. Connect a configuration input through a 30kΩ resistor to DVDD to set a high level. Leave the configuration input open to set a low level.

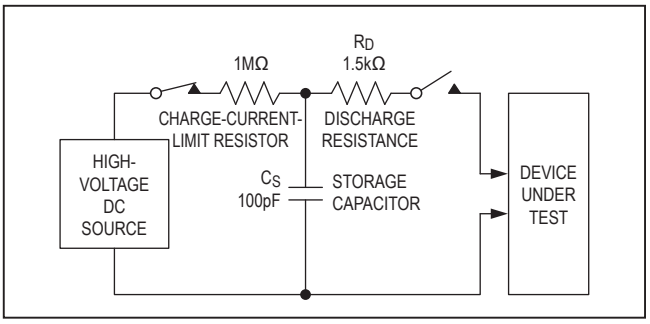


Figure 21. Human Body Model ESD Test Circuit

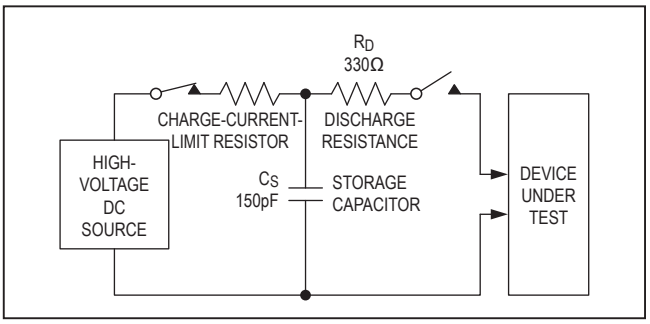


Figure 22. IEC 61000-4-2 Contact Discharge ESD Test Circuit

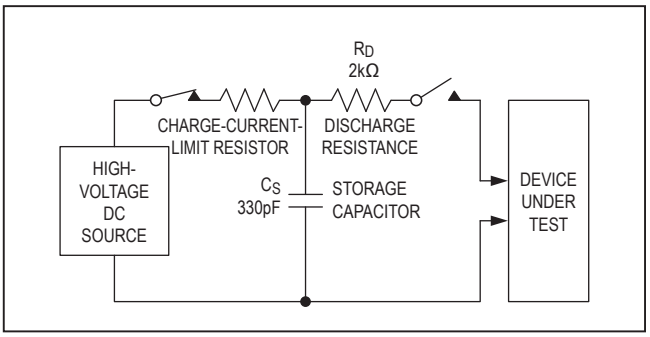


Figure 23. ISO 10605 Contact Discharge ESD Test Circuit

I²C Pullup Resistors

The I²C open-drain lines require a pullup resistor to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise may be required when choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the *I²C Port Timing* section in the *AC Electrical Characteristics* table for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time t_R = 0.85 x R_{PULLUP} x C_{BUS} < 300ns. The waveforms are not recognized if the transition time becomes too slow. GMSL supports I²C rates up to 1Mbps.

AC-Coupling Capacitors

Voltage droop and the digital-sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is fixed, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML/coax receiver termination resistor (R_{TR}), the CML/coax-driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is (C x (R_{TD} + R_{TR}))/4. R_{TD} and R_{TR} are required to match the transmission-line impedance (usually 100Ω differential, 50Ω single-ended). This leaves the capacitor selection to change the system time constant. Use 0.22µF or larger high-frequency, surface-mount ceramic capacitors with sufficient voltage rating to withstand a short to battery, to pass the lower speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower-parasitic effects to the high-speed signal.

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Coax cables typically have a characteristic impedance of 50Ω; contact the factory for 75Ω operation). Table 13 lists the suggested cables and connectors used in the GMSL link.

PRBS

The serializer includes a PRBS pattern generator that works with bit-error verification in the deserializer. To run the PRBS test, set PRBSEN = 1 (0x04, D5) in the deserializer, then in the serializer. To exit the PRBS test, set PRBSEN = 0 (0x04, D5) in the serializer. The deserializer automatically ends PRBS checking and sets the PRBS_OK bit high. During PRBS mode, the forward control channel is not available except to exit PRBS mode if autoacknowledge is enabled in the deserializer; otherwise, the remote control channel is not available at all.

Table 12. Feature Compatibility

SERIALIZER FEATURE	GMSL DESERIALIZER
HSYNC/VSYNC Encoding	If feature not supported in the deserializer, turn off in the serializer.
I^2C to I^2C	If feature not supported in the deserializer, do not use control channel.
Packet Control Channel	If feature not supported in the deserializer, use legacy control channel.
CRC Error Detection	If feature not supported in the deserializer, turn off in the serializer.
Double Input	If feature not supported in the deserializer, data is output as a single word at half the input frequency. Use crossbar switch and double alignment to correct input mapping.
Coax	If feature not supported in the deserializer, connect unused serial input through 200nF and 50Ω in series to AVDD, and set the reverse control-channel amplitude to 100mV.
I^2S Encoding	If supported in the deserializer, disable I^2S in the deserializer.
High-Bandwidth Mode	If feature not supported in the deserializer, turn off in the serializer.
High-Immunity Mode	If feature not supported in the deserializer, turn off in the serializer.
Low-Speed Mode	If supported in the deserializer, set DRS to 0 in the deserializer.

Table 13. Suggested Connectors and Cables for GMSL

VENDOR	CONNECTOR	CABLE	TYPE
Rosenberger	59S2AX-400A5-Y	Dacar 302	Coax
Rosenberger	D4S10A-40ML5-Z	Dacar 535-2	STP
Nissei	GT11L-2S	F-2WME AWG28	STP
JAE	MX38-FF	A-BW-Lxxxxx	STP

To run the PRBS with a 3Gbps SerDes, or when HIBW = 1, first set the PRBS_TYPE bit = 0 in the MAX967XX. Then set PRBSEN = 1 (0x04, D5) in the serializer and then in the deserializer. To exit the PRBS test, set PRBSEN = 0 (0x04, D5) in the deserializer, then in the serializer. PRBS_TYPE = 0 does not support DBL = 1.

During PRBS test, ERRB function changes to reflect PRBS errors only. ERRB goes low when any PRBS errors occur. ERRB goes high when the PRBS error counter is reset when PRBS_ERR is read. Normal ERRB function resumes when exiting the PRBS test.

GPI/GPO

GPO on the serializer follows GPI transitions on the deserializer. By default, the GPI-to-GPO delay is 0.35ms (max). Keep the time between GPI transitions to a minimum 0.35ms. GPI_IN the deserializer stores the GPI input state. GPO is low after power-up. The µC can set GPO by writing to the SET_GPO register bit.

Fast Detection of Loss-of-Lock

A measure of link quality is the recovery time from loss-of-synchronization. The host can be quickly notified of loss-of-lock by connecting the deserializer's LOCK output to the GPI input (when PKTCC_EN = 0). If other sources use the GPI input, such as a touch-screen controller, the µC can implement a routine to distinguish between interrupts from loss-of-sync and normal interrupts. Reverse control-channel communication does not require an active forward link to operate and accurately tracks the LOCK status of the GMSL link. LOCK asserts for video link only and not for the configuration link.

Providing a Frame Sync (Camera Applications)

The GPI and GPO provide a simple solution for camera applications that require a frame-sync signal from the ECU (e.g., surround-view systems). Connect the ECU frame-sync signal to the GPI input and connect the GPO output to the camera frame-sync input. GPI/GPO have a typical delay of 275µs in legacy mode and 21µs in packet mode (with 5-bit CRC). Skew between multiple GPI/GPO channels is 115µs (max) in legacy mode and 21µs (max) in packet mode. If a lower skew signal is required in legacy mode, connect the camera's frame-sync input to one of the serializer's GPIOs and use an I^2C broadcast-write command to change the GPIO output state. This has a maximum skew of 1.5µs, independent from the used I^2C bit rate. In packet-based control-channel mode, set GPI_COMP_EN = 1 in both the serializer and deserializer to turn on GPI/GPO compensation. This reduces the device-to-device skew to 0.35µs.

Entering/Exiting Sleep Mode

The procedure for entering and exiting sleep mode depends on the location of the microcontroller, and the type of control-channel interface used. If wake up from a remote (deserializer) side microcontroller is not needed or desired, set the DIS_RWAKE bit = 1 to shut down remote wake-up for further power savings.

Legacy Control Channel:

To enter sleep mode, set SLEEP = 1. The device sleeps after 8ms. To wake up the device, send an arbitrary control-channel command to the serializer (the serializer does not send an acknowledge), wait for 5ms for the chip to power up and then set SLEEP = 0 to make the wake-up permanent.

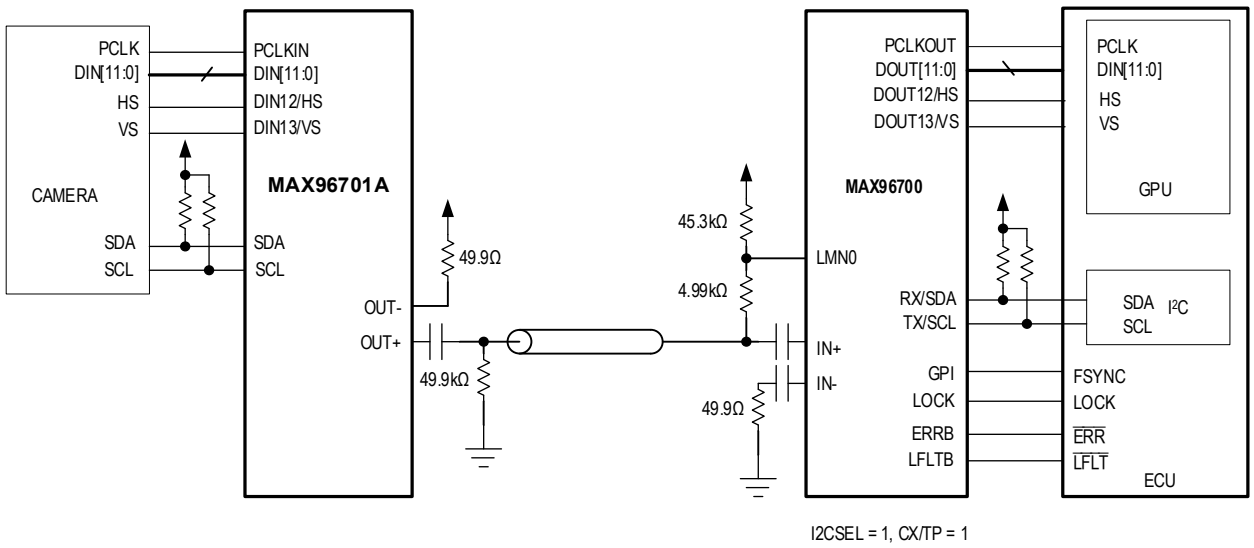
Packet-Based Control Channel:

- When µC is on the deserializer side, set SLEEP = 1 in serializer. Next set REVCCEN = 0 in the deserializer to stop reverse-control transmission to the serializer. The device sleeps after 8ms.

  To wake up the serializer, first set REVCCEN = 1, wait 8ms for the device to wake up and then set SLEEP = 0 to exit sleep mode permanently.
- When µC is on the serializer side, first set SLEEP = 1 in the deserializer. If the deserializer must remain awake, switch to legacy control-channel mode. Next, set SLEEP = 1 in the serializer. The device sleeps after 8ms.

  To wake up the device, send an arbitrary control-channel command to the serializer (the serializer does not send an acknowledge). Wait for 5ms for the chip to power up and then set SLEEP = 0 to make the wake-up permanent. The deserializer wakes up and clears its SLEEP bit when serialization is enabled and it locks to the serializer.

Typical Application Circuits



NOTE: NOT ALL PULLUP/PULLDOWN RESISTORS ARE SHOWN. SEE PIN DESCRIPTION FOR DETAILS.

CAMERA APPLICATION

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX96701AGTG/V+	-40°C to +115°C	24 TQFN-EP*
MAX96701AGTG/V+T	-40°C to +115°C	24 TQFN-EP*

/V denotes an automotive qualified product.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/21	Release for market intro	—
1	7/26	Release for public intro	—

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