

MAX78000 ERRATA SHEET

Revision A1 Errata

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc. may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Maxim has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

This errata sheet only applies to components of this revision. These components are branded on the top side of the package with a six-digit code in the form yywwRR, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and RR is the revision of the component. To obtain an errata sheet on other die revisions, visit the Maxim website at www.maximintegrated.com/errata.

1) BOOTLOADER SHA256 HASH CHECK COMMAND OUTPUTS INCORRECT RESULT WHEN LENGTH NOT A MULTIPLE OF 64 BYTES

Description:

Bootloader SHA256 Hash Check Command "H" outputs incorrect result when length is not a multiple of 64 bytes.

Workaround:

When issuing the "H" command, ensure that the requested HASH length is a multiple of 64 bytes.

2) CONVOLUTIONAL NEURAL NETWORK ACCELERATOR DOES NOT OPERATE RELIABLY WHEN V_{COREA} IS BELOW 1.0V

Description:

The CNN will not provide any reliable results if the V_{COREA} power supply pin drops below 1.0V.

Workaround:

To ensure proper operation of the CNN, the V_{COREA} power supply pin must be biased at 1.0V or higher. Refer to the device datasheet for V_{COREA} power supply pin operating range.

3) HIGH V_{REGI} SUPPLY CURRENT IN BACKUP (BKU) AND STANDBY (STB) MODES OF OPERATION

Description:

V_{REGI} supply current is higher than expected in BACKUP (BKU) and STANDBY (STB) modes of operation.

Workaround:

When it is desired to operate in BACKUP or STANDBY modes of operation, the V_{DDA} power supply pin should be biased to its lowest range of operation. This will minimize V_{REGI} current. Refer to the device datasheet for V_{DDA} power supply pin operating range.

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4) SPI MODE 1 AND MODE 3 FAIL AT MAXIMUM SERIAL CLOCK RATES

Description:

Both SPI0 and SPI1 include this limitation in both MASTER and SLAVE mode operation.

Workaround:

Operate the SPI0 at a maximum speed of 25MHz for both MASTER and SLAVE mode. Operate SPI1 at a maximum speed of 25MHz for MASTER mode and 12.5MHz for SLAVE mode.

5) USE OF WELR/RLR REGISTERS CAUSES EXECUTION HALT ON SUBSEQUENT RESETS

Description:

The WELR/RLR register is not reset on all forms of reset. It is only reset during a power-on cycle (POR).

Any use of WELR/RLR registers by user code or by issuing LOCK or PLOCK command to bootloader will cause an execution halt on all subsequent reset events other than POR.

Workarounds:

1. Do not use ROM Bootloader LOCK or PLOCK commands. These commands require writes to WELR/RLR.
2. Do not write WELR/RLR registers in user code.

If either of the above workarounds is required, the user must power cycle the device to avoid execution halt

6) ALL ADC/COMPARATOR INPUTS HAVE RESTRICTED OPERATING VOLTAGE RANGE.

Description:

The operating range of the ADC/Comparator inputs is restricted to maximum 1.8V.

Workaround:

None.

7) DEVICE WILL NOT EXIT FROM MICRO POWER MODE WHILE RUNNING FROM THE IBRO.

Description:

If the device is running from the IBRO and then subsequently enters the MICRO POWER mode, the device will not exit properly from the MICRO POWER mode as intended.

Workaround:

Set the System Clock (f_{SYS_CLK}) to operate from the IPO or the ISO before entering MICRO POWER Mode.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	07/2020	Initial release	—

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time.

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