Standalone USB Type-C and USB Power Delivery Controller

MAX77978

General Description

The MAX77978 is a highly integrated and robust stand-alone USB Type-C and power delivery (PD) controller capable of cable-plug and orientation detection on the Type-C connector.

The MAX77978 provides a fully PD3.2 V1.0-compliant solution that supports the extended power range (EPR) protocol.

The MAX777978 includes a RISC-V CPU, a USB-C PD controller, 16kBytes of MTP, and analog and digital peripherals. The device operates across the full power budget specified in the EPR (up to 48V V_{BUS}) and detects V_{BUS} voltages.

The IC also has a D+/D- USB switch integrated, supports USB2.0, eUSB, and UART, and includes V_{CONN} switches for USB-C PD.

The MAX77978 has also integrated BC1.2 charging detection for backward compatibility with legacy USB sources. SBUx Multiplexer is equipped to support AUXP and AUXN for Type-C alternate mode.

It also has an I^2C interface that the system can use to read/write and configure internal registers. An integrated I^2C controller engine can read and write to other devices in the system, allowing its firmware to configure related devices without the main processor's assistance.

The IC has five configurable GPIOs that can be used for detection, as interrupts, as a SID set, and as the enable/disable pin for external devices, or as ADC inputs.

The IC is available in a 3.4mm X 3.4mm, 0.5mm pitch, WLP package.

The MAX77978 is a highly customizable PD controller solution. Contact Analog Devices to explore how it meets customer-specific use cases.

Key Applications

- Smartphones
- Tablets
- Cameras
- Game Players
- Power Banks
- Industrial Equipment PoE to USB Type-C Adapters
- Handheld Devices
- Portable Devices
- Monitors
- Healthcare and Medical Devices
- Other USB Type-C Devices

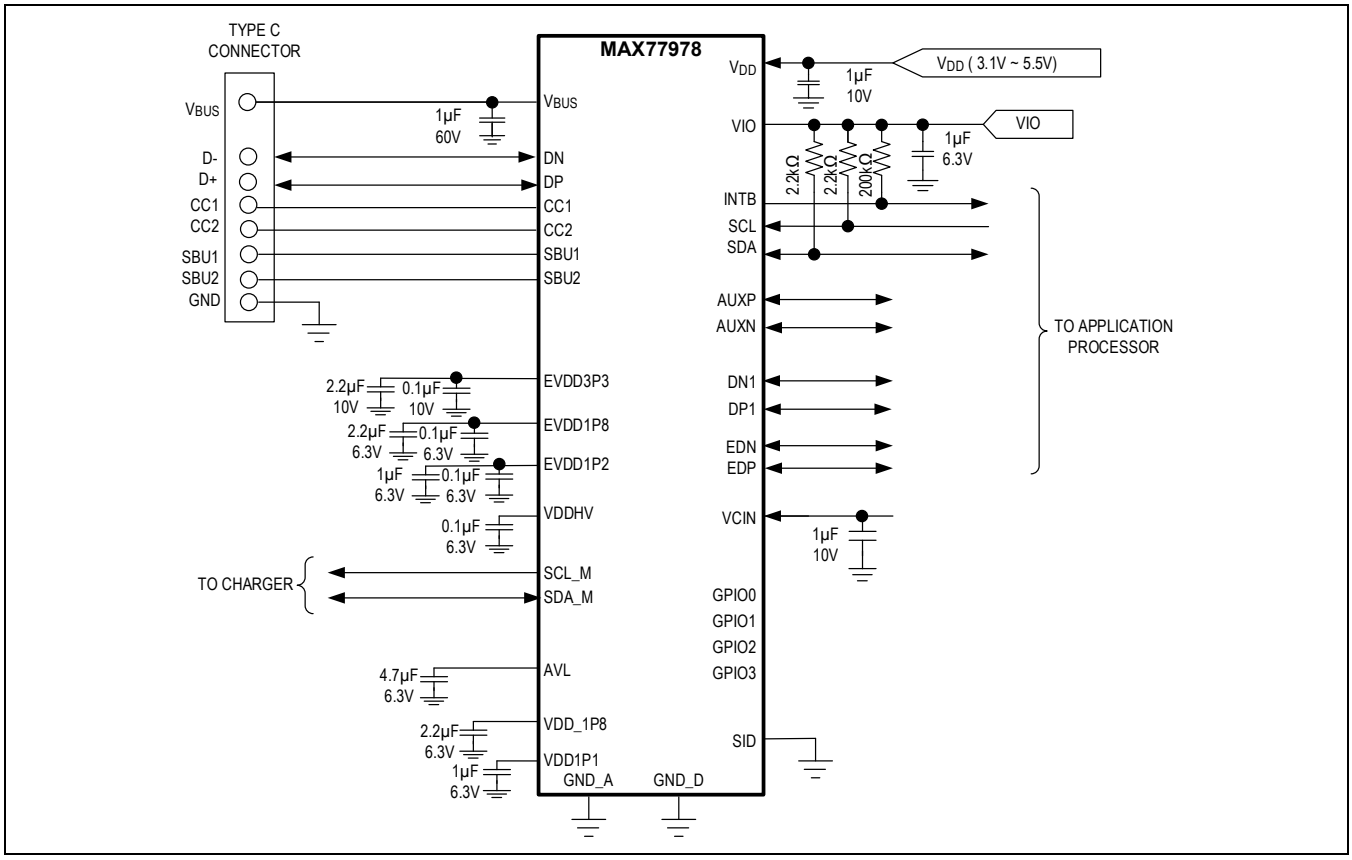
Benefits and Features

- MCU-Based Configuration
  - No Firmware Development Needed in Autonomous Configuration
  - Customizable Firmware Based on End Application Requirements
- RISC-V CPU and 16Kbyte MTP
  - USB Type-C Compliant Default Embedded Firmware
  - Supports Customizable Actions on Events
  - Firmware Updates for Future Specification Revisions
- USB Type-C Support and USB-PD Support
  - USB Type-C Version 2.3 and PD3.2 Compliant
  - Mode Configuration: Sink/Source/Dual Role Port
  - Programmable Power Supply (PPS) Sink Support
  - Fast Role Swap (FRS) Initial Sink Support
  - Alternate Mode Support and Integrated SBU Crossbar Mux
  - Integrated V_{CONN} Switch with OCP
  - Support Try.Snk State and Try.Src State
  - Debug Accessory Sink/Source Mode
- Supports BC1.2 Legacy/Proprietary Charger/ HVDCP Detection.
- Integrated D+/D- Switches for USB2.0 and UART
- Integrated eUSB2-USB 2.0 Repeater Compliant to USB Revision2.0 (Rev 1.2)
- Liquid Corrosion Mitigation Mode
- V_{DD} Operating Range, 3.1V – 5.5V
- High Voltage V_{BUS} (52V), DP/DN (16V), CC (52V)
- Short to V_{BUS} Protection on CC Pins and SBU Pins (50V)
- Dead Battery Support (SNK Mode Support When No V_{DD} Applied)
- I^2C Programmable Configuration (Three SIDs)
- I^2C Controller to Control the External Charger or DC-DC Converter
- 5 Configurable GPIOs (Including SID)

***Ordering Information* appears at end of data sheet.**

19-102128; Rev 0; 6/26

Simplified Block Diagram



Absolute Maximum Ratings

TOP and Interface Logic

V_{DD} to GND ..... -0.3V to +6.0V

V_{BUS} to GND ..... -0.3V to +52.0V

AVL to GND ..... -0.3V to +6.0V

VDD1P8 to GND ..... -0.3V to +2.2V

VDDHV to GND..... -0.3V to +6.0V

eVDD3P3 to GND .....-0.3V to Max (V_{DD} + 0.3,. 3.6)V

eVDD1P8 to GND ..... -0.3V to +2.2V

eVDD1P2 to GND ..... -0.3V to eVDD1P8+ 0.3V

VIO to GND ..... -0.3V to +6.0V

SCL, SDA, INTB, SCL_M, SDA_M to GND-0.3V to VIO + 0.3V

GND_A, GND_D to GND ..... -0.3V to +0.3V

USB Type-C

VCIN to GND..... -0.3V to +6.0V

DN, DP to GND.....-0.3V to +16.0V

CC1, CC2 to GND .....-0.3V to +52.0V

VDD1P1 to GND..... -0.3V to VDD1P8 + 0.3V

SBU1, SBU2 to GND .....-0.3V to +52.0V

DP1, DN1 to GND.....-0.3V to +6.0V

eDP, eDN to GND..... -0.3V to eVDD1P2 + 0.3V

AUXP, AUXN to GND .....-0.3V to +6.0V

SID to GND.....-0.3V to +6.0V

GPIO0, GPIO1, GPIO2, GPIO3,to GND -0.3V to VIO + 0.3V

Thermal Absolute Maximum Rating

Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 24.4mW/°C above +70°C.).21.0mW to 24.4mW

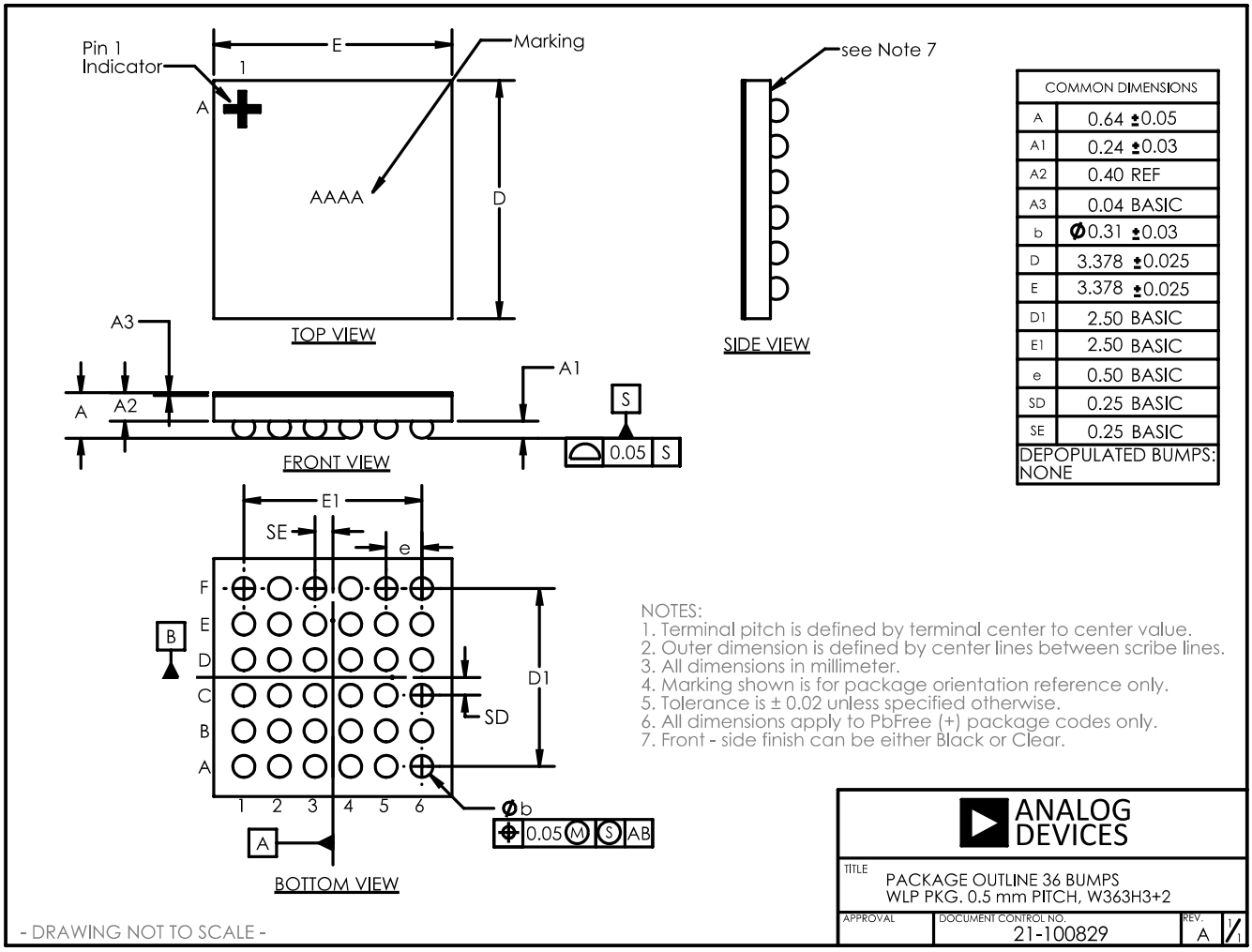
Operating Temperature Range..... -40°C to +85°C

Storage Temperature Range..... -65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE CODE	W363H3+2
Outline Number	21-100829
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	N/A
Junction-to-Case Thermal Resistance (θ_{JC})	N/A
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A



For the latest package outline information and land patterns (footprints), go to www.analog.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.analog.com/thermal-tutorial.

Electrical Characteristics

(Limits are 100% tested at T_A = = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL ELECTRICAL CHARACTERISTICS							
V_{DD} Operating Voltage	V_{DD}			3.1	3.3	+5.5	V
V_{DD} Factory Ship Supply Current	I_{FSHIP}	VIO = 0V, V_{BUS} = 0V	V_{DD} = 3.8V		2.4		µA
V_{DD} Standby Supply Current	$I_{STANDBY}$	Sink mode, chgDetEn = 1, VIO = 1.8V, V_{BUS} = 0V	V_{DD} = 3.8V		110		µA
		DRP mode(50%), chgDetEn = 1, VIO = 1.8V, V_{BUS} = 0V	V_{DD} = 3.8V		120		
	I_{SINKPD}	Sink mode, Stop mode, chgDetEn = 1, VIO = 1.8V, V_{BUS} = 5V, PD idle, eUSB on	V_{DD} = 3.8V		800		
V_{DD} Supply Current	$I_{eUSB2LS}$	Sink mode, Stop mode, chgDetEn = 1, VIO = 1.8V, V_{BUS} = 5V, PD idle, LS eUSB2 → USB2.0 enabled	V_{DD} = 3.8V		2112		µA
	$I_{eUSB2FS}$	Sink mode, Stop mode, chgDetEn = 1, VIO = 1.8V, V_{BUS} = 5V, PD idle, FS eUSB2 → USB2.0 enabled	V_{DD} = 3.8V		6991		
	$I_{eUSB2HS}$	Sink mode, Stop mode, chgDetEn = 1, VIO = 1.8V, V_{BUS} = 5V, PD idle, HS eUSB2 → USB2.0 enabled	V_{DD} = 3.8V		37819		
V_{BUS} Operating Voltage	V_{BUS}	$V_{VBUSDET\_R(max)}$ to MOV		+4		+51	V
V_{BUS} Supply Stand by Current	$I_{VBUS\_STANDBY}$	V_{BUS} = 5V, VIO = 1.8V, CCdetEn = 1, sink only, STOP mode	V_{DD} = 3.3V		150		µA
VIO Voltage	V_{IO}	VIO		1.62		5.5	V
I²C TARGET/LOGIC LEVEL							
SCL, SDA Input Low Level		T_A = +25 °C				0.3 x VIO	V
SCL, SDA Input High Level		T_A = +25 °C		0.7 x VIO			V
SCL, SDA Input Hysteresis		T_A = +25 °C			0.05 x VIO		V
SCL, SDA Logic Input Current		SDA = SCL = 5.5V		-10		+10	µA

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA Output Low Voltage		Sinking 20mA			0.4	V
Output Low Voltage INTB		I_{SINK} = 1mA			0.4	V
Output High Leakage INTB		V_{INTB} = 5.5V, T_A = +25°C	-1000		+1000	nA
I²C TARGET/TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		260			ns
CLK Low Period	t_{LOW}		500			ns
CLK High Period	t_{HIGH}		260			ns
Setup Time Repeated START Condition	$t_{SU;STA}$		260			ns
DATA Hold Time	$t_{HD;DAT}$		0			ns
DATA Valid Time	$t_{VD;DAT}$				450	ns
DATA Valid Acknowledge Time	$t_{VD;ACK}$				450	ns
Rise/Fall Time of SCL	t_{SCL}				120	ns
Rise/Fall Time of SDA	t_{SDA}				120	ns
DATA Setup time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		260			ns
Bus-Free Time Between STOP and START	t_{BUF}		500			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				50		ns
I²C TARGET/TIMING FOR HS-MODE (CB = 100pF)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Set-Up time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD;DAT}$		0			ns
Rise/Fall time of SCL	t_{SCL}		10		40	ns
Rise/Fall time of SDA	t_{SDA}		10		80	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TARGET/TIMING FOR HS-MODE (CB = 400pF)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		320			ns
CLK High Period	t_{HIGH}		120			ns
DATA Set-Up time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD;DAT}$		0			ns
Rise/Fall Time of SCL	t_{SCL}		20		80	ns
Rise/Fall Time of SDA	t_{SDA}		10		160	ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns
BC1.2 DETECTION						
DP/DN Operating Voltage	$V_{DPDNMAX}$		0		4	V
BC1.2 State Timeout	t_{TMO}		180	200	220	ms
Data Contact Detect Timeout	t_{DCDtmo}	DCDCpl = 0b1 (default), DCDCpl = 0b0	700	800	900	ms
Proprietary Charger Debounce	t_{PRDeb}		5	7.5	10	ms
Primary to Secondary Timer	$t_{PDSDWait}$		27	35	39	ms
Charger Detection Debounce	t_{CDDeb}		45	50	55	ms
VBUS64	V_{BUS64}	Rising/Falling. DP/DN. In percent of V_{BUS}. 3V < V_{BUS} < 5.5V	57	64	71	%
	$V_{BUS64\ H}$	Hysteresis		15		mV
	$t_{VBUS64\ DEB}$	Debounce		t_{PRDeb}		ms
VBUS47	V_{BUS47}	Rising/Falling. DP/DN. In percent of V_{BUS}. 3V < V_{BUS} < 5.5V	43.3	47	51.7	%
	$V_{BUS47\ H}$	Hysteresis		15		mV
	$t_{VBUS47\ DEB}$	Debounce		t_{PRDeb}		ms
VBUS31	V_{BUS31}	Rising/Falling. DP/DN. In percent of V_{BUS}. 3V < V_{BUS} < 5.5V	26	31	36	%
	$V_{BUS31\ H}$	Hysteresis		15		mV
	$t_{VBUS31\ DEB}$	Debounce		t_{PRDeb}		ms
R_{DM_DWN} Resistor	R_{DM_DWN}		14.25	20	24.8	kΩ
I_{DP_SRC} Current	I_{DP_SRC}/I_{DCD}	Accurate over 0V to 2.5V	-13	-10	-7	µA
I_{DM_SINK} Current	$I_{DM\_SINK}/I_{DATSINK}$	Accurate over 0.15V to 3.6V	50	80	110	µA

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{LGC} Threshold	V_{LGC}			1.62	1.7	1.9	V
V_{LGC} Hysteresis	V_{LGC_H}				0.015		V
V_{DAT_REF} Threshold	V_{DAT_REF}			0.25	0.32	0.4	V
V_{DAT_REF} Hysteresis	$V_{DAT\_REF\_H}$				0.015		V
VD33 Voltage	$V_{DP/DM\_3p3VSRC}/V_{SRC33}$	Tested at zero load and at 200µA load		2.6	3.0	3.3	V
VSRC33ILIM Current Limit	$I_{LIMVSRC33}$	Force 1.6V on DP/DN, measure current			1.5	3	mA
V_{DN_SRC} Voltage	V_{DN_SRC}/V_{SRC06}	Accurate over I_{LOAD} = 0 to 200µA		0.5	0.6	0.7	V
V_{DP_SRC} Voltage	V_{DP_SRC}/V_{SRC06}	Accurate over I_{LOAD} = 0 to 200µA		0.5	0.6	0.7	V
DP/DN OVER-VOLTAGE PROTECTION							
DP/DN OVP	$V_{OVDX\ R}$	Rising		4.2		4.65	V
	$V_{OVDX\ F}$	Falling		4.15		4.6	
	$V_{OVDX\ H}$	Hysteresis			70		mV
	$V_{OVDX\ DEB}$	Debounce (Falling)			30		µs
DP/DN Load Resistor	$V_{DP/DN}$	Load Resistor on DP/DN When OVP circuitry is enabled DP/DN < V_{AVL}		3	6.1	12	MΩ
DP/DN ANALOG SWITCH(DP1/DN1)							
Analog Signal Range	V_{DN1}, V_{DP1}	V_{AVL} = 3.0V, I_{DN}/ I_{DP} = 10mA, V_{DN}/ V_{DP} = 0V to 3.0V		0		V_{AVL}	V
On-Resistance	R_{ONUSB}	V_{AVL} = 3.0V, I_{DN}/ I_{DP} = 10mA, V_{DN}/ V_{DP} = 400mV			3.7	6.5	Ω
On-Resistance Match Between Channels	ΔR_{ONUSB}	V_{AVL} = 3.0V, I_{DN}/ I_{DP} = 10mA, V_{DN}/ V_{DP} = 0V to 3.0V				0.5	Ω
On-Resistance Flatness	$R_{FLATUSB}$	V_{AVL} = 3.0V, I_{DN}/ I_{DP} = 10mA, V_{DN}/ V_{DP} = 0V to 3.0V			0.1	0.4	Ω
Off Leakage Current	I_{LDN1}, I_{LDP1}	V_{AVL}= 4.2V; switch opened; V_{DN1} or V_{DP1} = +2.5V, 0.3V, measured at DN1 or DP1		-360		360	nA
	I_{LDN}, I_{LDP}	V_{AVL} = 4.2V; switch opened; V_{DN} or V_{DP} = +2.5V, 0.3V, measured at DN or DP		-360		1000	
DP/DN DYNAMIC PERFORMANCE(DP1/DN1)							
Analog Switch Turn-on Time	t_{ON}	I^2C Stop to Switch On; R_L= 50Ω			0.2	0.5	ms
Analog Switch Turn Off Time	t_{OFF}	I^2C Stop to Switch Off; R_L= 50Ω			0.1	0.5	ms
Break-Before-Make Delay Time	t_{BBM}	R_L= 50Ω; T_A = +25°C			15		µs
DN, DP On Capacitance	C_{ON}	Input capacitance guaranteed by design Not production tested	V = 0.5 VPP, DC bias = 0V, f = 240MHz, DN, DP connected to DN1, DP1		4	5	pF
eUSB2-USB 2.0 REPEATER							
eUSB2 Supply Voltage	p_vddio	eVDD1P2	Internal LDO output	1.08	1.2	1.32	V
	p_vdd3	eVDD3P3	Internal LDO output	3.03	3.3	3.43	
	p_vdd1p8	eVDD1P8	Internal LDO output		1.8		

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
-USB2.0 Pull-up and Pull-down Registers	$R_{PU\ USB2}$	Upstream Facing Port	1.425	1.5	1.575	kΩ
USB2.0 Pull-up and Pull-down Registers	$R_{PD\ USB2}$	Downstream Facing Port	14.25	15	15.75	kΩ
eUSB2 Pull-down Registers	$R_{PU\ eUSB2}$		4		10	kΩ
eUSB2 FS/LS Receiver	V_{ILe}	Rx Input Low Voltage			0.35 x p_vddio	V
	V_{IHe}	Rx Input High Voltage	0.65 x p_vddio			
	V_{RHYS}	Rx SE hysteresis		0.04 x p_vddio		
eUSB2 FS/LS Transmitter	V_{OLe}	Tx SE Output Low Voltage			0.15 x p_vddio	V
	V_{OHe}	Tx SE Output High Voltage	0.85 x p_vddio			
	$T_{RISE\ FALL\ TRM}$	Tx rise and fall time, 10% - 90%	2			ns
	$T_{RISE\ FALL\ MISM}$	Tx rise and fall mismatch			25	%
	$R_{SRC\ HS}$	Tx output res and HS source termination	32		48	Ω
	$T_{SE1\ SKEW}$	SE1 Differential Skew			245	ps
USB2.0 FS/LS Receiver	V_{ILU}	Rx Input Low Voltage			0.8	V
	V_{IHU}	Rx Input High Voltage	2			
	V_{DI}	Rx differential input sensitivity	0.2			
	V_{CM}	Rx differential common mode sensitivity	0.8		2.5	
USB2 FS/LS Transmitter	V_{OLU}	Tx SE output low voltage			0.3	V
	V_{OHU}	Tx SE output high voltage	2.8		3.6	
	V_{CRS}	Tx output signal crossover voltage	1.3		2	
	V_{DRV}	Tx driver output resistance	28		45	Ω
	$V_{IFR\ FS}$	Tx FS rise time	4		20	ns
	$V_{IFF\ FS}$	Tx FS fall time	4		20	
	$V_{IFRM\ FS}$	Tx FS differential rise and fall time matching	90		111.11	%
	$V_{FR\ LS}$	Tx LS rise time	75		300	ns
	$V_{FF\ LS}$	Tx LS fall time	75		300	
	$V_{FRM\ LS}$	Tx LS differential rise and fall time matching	80		125	%
	Z_{HSDRV}	HS termination	40		49.5	Ω
eUSB2 HS Receiver	$V_{RX\ DIF\ SENS}$	eUSB2 High Speed peak differential sensitivity	±60			mV
	$V_{RX\ DIF\ CM}$	eUSB2 High Speed common mode rejection	120		280	
	C_{RX}	eUSB2 High Speed receiver pad capacitance			2.5	pF
USB2.0 HS Receiver	$V_{RXU\ DIF\ SENS}$	USB2.0 High Speed receiver peak differential sensitivity	±100			mV
	V_{HSCM}	USB2.0 High Speed data signaling common mode voltage range	-100		500	

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
	C_{HSLOAD}	USB2.0 High Speed capacitance to ground				10	pF
eUSB2 HS Transmitter	$V_{TX\ DIF\ TERM}$	eUSB2 High Speed transmit differential voltage terminated		165		245	mV
	$V_{TX\ CM}$	eUSB2 High Speed transmit common mode voltage		170		230	
	$V_{TX\ CM\ AC}$	eUSB2 High Speed transmit common mode AC	50MHz – 480MHz	-30		30	mV_{pk}
	$T_{RISE\ FALL\ TRM}$	eUSB2 HS transmit rise and fall time	20%-80%	100			ps
	$T_{D\ FALL\ TRM}$	eUSB2 HS transmit rise and fall time mismatch				25	%
USB2.0 HS Transmitter	V_{HSOH}	USB2.0 High Speed data signaling high output level		360		440	mV
	V_{HSOL}	USB2.0 High Speed data signaling low output level		-10		10	
	V_{HSOI}	USB2.0 High Speed data idle output level		-10		10	
	T_{HSR}, T_{HSF}	USB2.0 HS transmit rise and fall time	10% - 90%	300			ps
	V_{CHIRPJ}	USB2.0 CHIRP J differential output level		700		1100	mV
	V_{CHIRPK}	USB2.0 HS CHIRP K differential output level		-900		-500	
eUSB2 Squelch Detector	$V_{squelch\ dif}$	eUSB2 squelch detection threshold		60		110	mV
	$T_{delay\ e}$	eUSB2 squelch detector delay				2	HS UI
	$V_{RX\ DIF\ CM}$	eUSB2 High Speed receiver common mode rejection		120		280	mV
USB2.0 Squelch Detector	V_{HSSQ}	USB2.0 squelch detection threshold		100	125	150	mV
	V_{HSCM}	USB2.0 High Speed receiver common mode rejection		-100		500	
	$T_{delay\ u}$	USB2.0 squelch detector delay				2	HS UI
USB2.0 HS disconnect Detector	V_{HSDSC}	USB2.0 HS disconnect detect threshold		525	575	625	mV
CC DETECTION							
CC Operating Voltage	V_{CCMAX}			0		5.5	V
CC Pin Voltage, in DFP 1.5A Mode	V_{CC_PIN}	Measured at CC pins with 126kΩ load, $I_{DFP1.5\_CC}$ enable and V_{AVL} ≥ 2.6V		1.85			V
CC Pin Voltage, in DFP 3.0A Mode	V_{CC_PIN}	Measured at CC pins with 126kΩ load, $I_{DFP3.0\_CC}$ enable and V_{AVL} ≥ 3.65V		3.1			V
CC Pin Clamp Voltage	V_{CC_CLAMP}	60µA ≤ I_{CC} ≤ 600µA		0.88	1.1	1.32	V
CC UFP Pull-down Resistance	R_d			-10%	5.1	+10%	kΩ
	R_a			0.8	1	1.2	
CC DFP Low-Power Mode	V_{DFPLP_CC}	V_{AVL} ≥ 2.6V, I_{DFPULP_CC} current source enabled, 1.1V clamp diabled		1.2			V
CC DFP Ultra-Low-Power Current Source	I_{DFPULP_CC}	Measured at CC = 0.5V and CC = 1.0V, T_A = +25°C		-10%	1	+10%	µA
CC DFP Low-Power Current Source	I_{DFPLP_CC}	Measured at CC = 0.5V and CC = 1.0V, T_A = +25°C		-10%	5	+10%	µA
CC DFP 0.5A Current Source	$I_{DFP0.5\_CC}$			-20%	80	+20%	µA
CC DFP 1.5A Current Source	$I_{DFP1.5\_CC}$			-8%	180	+8%	µA

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CC DFP 3A Current Source	I_{DFP3A_CC}		-8%	330	+8%	µA
CC RA RD Threshold	$V_{RA\_RD0.5}$		0.15	0.2	0.25	V
CC UFP 0.5A RD Threshold	$V_{UFP\_RD0.5}$		0.61	0.66	0.7	V
CC UFP 0.5A RD Hysteresis	$V_{UFP\_RD0.5\_H}$			0.015		V
CC UFP 1.5A RD Threshold	$V_{UFP\_RD1.5}$		1.16	1.23	1.31	V
CC UFP 1.5A RD Hysteresis	$V_{UFP\_RD1.5\_H}$			0.015		V
CC DFP V_{OPEN} Detect Threshold	V_{DFP_VOPEN}		1.5	1.575	1.65	V
CC DFP V_{OPEN} Detect Hysteresis	$V_{DFP\_VOPEN\_H}$			0.030		V
CC DFP V_{OPEN} With 3.0A Detect Threshold	$V_{DFP\_VOPEN3A}$	V_{AVL} ≥ 3.5V	2.45	2.6	2.75	V
CC DFP V_{OPEN} With 3.0A Detect Hysteresis	$V_{DFP\_VOPEN3A\_H}$	V_{AVL} ≥ 3.5V		0.030		V
CC Pin Power-Up Time	$t_{ClampSwap}$	Max time allowed from removal of voltage clamp until a 5.1kΩ resistor attached			15	ms
CC Detection Debounce	t_{CCDeb}		100	119	200	ms
DRP Transition Time	$t_{DRPTrans}$	Time for a role swap from DFP to UFP or the reverse is completed			1	ms
V_{CONN} Enable Time	$t_{VCONNON}$				2	ms
V_{CONN} Disable Time	$t_{VCONNOFF}$	Time from UFP detached or as directed by I^2C command until V_{CONN} is removed			35	ms
CC Pin Current Change Time	$I_{SINKADJ}$	Time from CC pin changes state in UFP mode until current drawn from DFP reaches a new value			60	ms
VBUSDET	$V_{VBUSDET\_R}$	Rising	3.6	3.8	4.0	V
	$V_{VBUSDET\_F}$	Falling	3.1			
	$V_{VBUSDET\_H}$	Hysteresis		300		mV
	$V_{VBUSDET\_DEB}$	Debounce	9	10	11	ms
VSAFE5V	V_{SAFE5V_R}	Rising		5.157		V
	V_{SAFE5V_F}	Falling		5.119		
	V_{SAFE5V_H}	Hysteresis		38.5		mV
VSAFE0V	V_{SAFE0V_R}	Rising	0.66	0.73	0.81	V
	V_{SAFE0V_F}	Falling	0.60	0.67	0.75	
	V_{SAFE0V_H}	Hysteresis		60		mV
	V_{SAFE0V_DEB}		9	10	11	ms
V_{BUS} On Time	t_{VBUSON}	Time from UFP is attached until V_{BUS} ON			275	ms
V_{BUS} Off Time	$t_{VBUSOFF}$	Time from UFP is detached until V_{BUS} reaches VSAFE0V			650	ms
V_{BUS} Input Self-Discharge Resistance	$R_{VBU\_SD\_USB}$			10		kΩ

(Limits are 100% tested at T_A = = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CC1/2 Water Comp Threshold	V_{CC_Comp}	1.0V Comp		-8%	1.00	+8%	V
		0.8V Comp		-8%	0.8	+8%	
		0.6V Comp		-8%	0.6	+8%	
		0.4V Comp		-8%	0.4	+8%	
CC1/2 Water Comp Hysteresis	$V_{CC\_Comp\_H}$				0.015		V
CC OVER-VOLTAGE PROTECTION							
CC OVP	CC_{OVP_R}	Rising		5.5		6.0	V
	CC_{OVP_F}	Falling		5.5		6.0	
	CC_{OVP_H}	Hysteresis			50		mV
	t_{OVCC_DEB}	Debounce	Falling only		30		µs
SBU DETECTION							
SBU Operational Voltage	V_{SBUMAX}					5.5	V
SBU Ultra Low Power Current Source	I_{SBU_ULP}	Measured at SBUx = 0.5V and at SBUx = 1.0V, T_A = +25°C		-10%	1	+10%	µA
SBU Current Source Maximum Bias Voltage	V_{SBU_BIAS}	1uA current source enabled, SBU is opened		1.1		1.5	V
SBU Safe Pull-Down	R_{SBU_SSPD}			-40%	43	+40%	kΩ
SBU OVER-VOLTAGE PROTECTION							
SBU OVP	V_{OVSBU_R}	Rising		3.6		4	V
	V_{OVSBU_F}	Falling		3.6		4	
	V_{OVSBU_H}	Hysteresis			50		mV
	V_{OVSBU_DEB}	Debounce	Falling		60		µs
SBU1/SBU2 Load Resistor	R_{SBU}	Load Resistor on SBU1/SBU2 When OVP circuitry is enabled SBU1/SBU2< VAVL		3	6.1	12	MΩ
SBU ANALOG SWITCH (AUXP/AUXN)							
Analog Signal Range	V_{AUXP}, V_{AUXN}			0		V_{AVL}	
On-Resistance	R_{ONSBU}	R_{ONSBU}	V_{AVL} = 3.0V, I_{SBU1}/I_{SBU2} = 10mA, V_{SBU1}/V_{SBU2} = 0V to 3.0V		14	30	Ω
On-Resistance Match Between Channels	ΔR_{ONSBU}	ΔR_{ONSBU}	V_{AVL} = 3.0V, I_{SBU1}/I_{SBU2} = 10mA, V_{SBU1}/V_{SBU2} = 1.5V			2.5	Ω
On-Resistance Flatness	$R_{FLATSBU}$	$R_{FLATSBU}$	V_{AVL} = 3.0V, I_{SBU1}/I_{SBU2} = 10mA, V_{SBU1}/V_{SBU2} = 0V to 3.0V		0.5	2	Ω
Off Leakage Current	I_{LSBUX_1}, I_{LSBUX_2}	I_{LSBUX_1}, I_{LSBUX_2}	V_{AVL} = 4.2V; switch open; V_{AUXP} or V_{AUXN} = 0.3V, +2.5V; V_{SBU1} or V_{SBU2} = +2.5V, 0.3V	-360		+360	nA

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SBU DYNAMIC PERFORMANCE (AUXP/AUXN)						
Analog Switch Turn-On Time	t_{ON}	I^2C Stop to Switch On; R_L= 50Ω		0.2	0.5	ms
Analog Switch Turn Off Time	t_{OFF}	I^2C Stop to Switch On; R_L= 50Ω		0.1	0.5	ms
Break-Before-Make Delay Time	t_{BBM}	R_L= 50Ω; T_A = +25°C		15		µs
SBU1, SBU2 On Capacitance	C_{ON}	Input capacitance guaranteed by design, not production tested		15	20	pF
VCIN DETECTION						
VCIN_PRES	$V_{CIN\_PRES\_R}$	Rising	0.7		1.95	V
	$V_{CIN\_PRES\_F}$	Falling	0.2		1.45	
	$V_{CIN\_PRES\_H}$	Hysteresis		300		mV
VCIN_OK	$V_{CIN\_OK\_R}$	Rising	2.5	2.75	3.0	V
	$V_{CIN\_OK\_F}$	Falling	2.47	2.72	2.97	
	$V_{CIN\_OK\_H}$	Hysteresis		30		mV
V_{CONN} SWITCH						
V_{CONN} SW Ron	$R_{ONVCONNSW}$	V_{CONN} = 4.75V, I_L = 500mA		500	900	mΩ
OCP Short Circuit Protection	OCP_ISCP	800mA	700	800	910	mA
OCP programmable step	OCP_ISTEP	Programmable range is 200mA to 500mA	200		500	mA
OCP accuracy	OCP_ACC	V_{CONN} = 5V, T_A = +25ºC	0	15	30	%
OCP interrupt debounce time T1	t_{Deb1}	From generating internal INT to RISC-V		3		ms
Wait time before turning off T2	t_{Deb2}	From generating internal INT to RISC-V		12		ms
Turn-on time at 90%	t_{VCONN_ON}	Time from V_{CONN} Switch enable to CC settled at 90% of the final value with V_{CONN} = 5V		1	2	ms
Turn off time at 10%	t_{VCONN_OFF}	Time from V_{CONN} Switch disable to CC settled at 10% of the final value with VCIN = 3.0V / Time from V_{CONN} Switch disable to CC settled at 10% of the final value with V_{CONN} = 5V		0.05	0.5	ms
V_{CONN} Leakage Current	I_{VCONN_OFF}	VCONN SW OFF, VCONN BST OFF, V_{CONN} = 5.5V			5	µA
V_{CONN} Soft Start Current	$I_{VCONNSST}$		0.3	0.48	0.75	A
V_{CONN} Soft Start Disable time	$T_{VCONNSSTDIS}$		540	600	660	µs
V_{CONN} Soft Start Fail time	$T_{VCONNFAIL}$		0.9	1	1.1	ms
V_{CONN} Present threshold	$V_{VCONPRES\_R}$		2.1	2.25	2.4	V
V_{CONN} Presents Hysteresis	$V_{VCONPRES\_H}$			15		mV
PD CONTROLLER/BMC LDO						
BMC LDO - Input Voltage	VDD1P8		1.7	1.8	1.9	V

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BMC LDO - Output Voltage	VDD1P1	V_{AVL} = 3.8V, for I_L = 1mA		1.05	1.125	1.2	V
BMC LDO - Current Limit	VDD1P1_ILIM	V_{AVL} = 3.8V		5	11	19	mA
BMC LDO - Minimum Output Capacitance	VDD1P1_C			0.75	1		µF
BMC LDO - Power Down Consumption	I_{VDD1P1_OFF}	VDD1P8			0.1		µA
BMC LDO - Power Up Consumption	I_{VDD1P1_ON}				5	12	µA
BMC LDO – Turn-on Time	VDD1P1_STARTUP	From BMC_PWDN_LDO= 0 to V1P1 = 95% of final value		30		300	µs
BMC LDO - Output Pull-down Current	I_{VDD1P1}	VDD1P1 = 1.125V and BMC_EN_EXTRALOAD_LDO_VCC = 1		330	500	750	µA
PD CONTROLLER/BMC TRANSMITTER							
BMC BIT Rate	$f_{Bitrate}$			270	300	330	kbps
Unit Interval for BMC Bus	t_{UI}			3.03		3.7	µs
Time Until BMC Bus Drive End	$t_{EndDriveBMC}$	Time to cease driving the line after the end of the last bit of the frame. The min value is limited by $t_{HoldLowBMC}$				23	µs
Transmit Hold Time	$t_{HoldLowBMC}$	Time to cease driving the line after the final high-to-low transition		1			µs
BMC TX Rise Time	t_{Rise}	10% to 90% with no load on CC wires		300	410	540	ns
BMC TX Fall Time	t_{Fall}	90% to 10% with no load on CC wires		300	410	540	ns
BMC TX Swing	V_{SWING}	Applies to no load and with max load defined by cable/receiver model for both Sink and Source		1.05	1.125	1.2	V
BMC Driver Output Impedance	Z_{Driver}	Source output impedance at the Nyquist frequency of [USB 2.0] low speed (750kHz)			42	75	Ω
VBUS MONITORING							
ADC RANGE		VBUS_VOLT_MON = 1, adcEN = 0		0x00		0xFF	
LSB		VBUS_VOLTAGE [9:0]			25.0014		mV
ACCURACY		0.5V < V_{BUS} < 2.5V		-50		+50	mV
		V_{BUS} > 2.5V		-2		+2	%
SAMPLING RATE						6	ms
CC ADC RANGE 1							
ADC RANGE		ADCIN SEL = 0x01 or 0x03	ccLadderDis = 0 or 1	0x00		0xFF	
LSB		ADCIN SEL = 0x01 or 0x03	ccLadderDis = 0		10.0724		mV
			ccLadderDis = 1		4.8351		
ACCURACY		ADCIN SEL = 0x01 or 0x03	VBADC = 0b00100	-3		+3	LSB
CC ADC RANGE 2							
RANGE		ADCIN SEL = 0x02 or 0x04	ccLadderDis = 0 or 1	0x00		0xFF	
LSB			ccLadderDis = 0		6.1032		mV

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		ADCIN SEL = 0x02 or 0x04	ccLadderDis = 1		4.8351		
ACCURACY		ADCIN SEL = 0x02 or 0x04		-3		+3	LSB
SBU ADC RANGE							
ADC RANGE		ADCIN SEL = 0x05 or 0x06		0x00		0xFF	
LSB		ADCIN SEL = 0x05 or 0x06			4.8372		mV
ACCURACY		ADCIN SEL = 0x05 or 0x06		-3		+3	LSB
GPIO0 ADC RANGE							
ADC RANGE		ADCIN SEL = 0x08	GPIO_SCALE_ADC = 0 or 1	0x00		0xFF	
LSB		ADCIN SEL = 0x08	GPIO_SCALE_ADC = 0		4.8384		mV
			GPIO_SCALE_ADC = 1		19.329		
ACCURACY		ADCIN SEL = 0x08	GPIO_SCALE_ADC = 0 or 1	-3		+3	LSB
GPIO1 ADC RANGE							
ADC RANGE		ADCIN SEL = 0x09	GPIO_SCALE_ADC = 0 or 1	0x00		0xFF	
LSB		ADCIN SEL = 0x09	GPIO_SCALE_ADC = 0		4.8384		mV
			GPIO_SCALE_ADC = 1		19.329		
ACCURACY		ADCIN SEL = 0x09	GPIO_SCALE_ADC = 0 or 1	-3		+3	LSB
GPIO0, 1, 2, 3							
Input Low Voltage	V_{IL}					0.3 x V_{IO}	V
Input High Voltage	V_{IH}			0.7 x V_{IO}			V
Input Hysteresis (Schmitt)	V_{IHYS}				0.1 x V_{IO}		V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA				0.4	V
Output High Voltage	V_{OH}	I_{SINK} = 2mA		0.7 x V_{IO}			V
Input Leakage Current	I_L	T_A = +25°C			100		nA
Input Pull-up Resistor	R_{PU}				100		kΩ
Input Pull-down Resistor	R_{PD}				100		kΩ
I²C CONTROLLER/LOGIC LEVEL							
SCL_M, SDA_M Input Low Level		T_A = +25°C				0.3 x V_{IO}	V
SCL_M, SDA_M Input High Level		T_A = +25°C		0.7 x V_{IO}		V_{IO}	V
SCL_M, SDA_M Input Hysteresis		T_A = +25°C			0.05 x V_{IO}		V
SCL_M, SDA_M Logic Input Current		SCL_M = SD_AM = VIO = 5.5V		-1000		+1000	nA
SCL_M, SDA_M Input Capacitance					10		pF

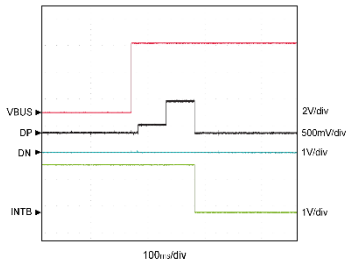
(Limits are 100% tested at T_A = = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCL_M, SDA_M Output High Voltage		Sinking 3mA	VIO = HV			0.4	V
SCL_M, SDA_M Output Low Voltage		Sinking 3mA	VIO = LV			0.2 x V_{IO}	V
SCL_M, SDA_M Input Leakage Current	I_{LK}	T_A = +25°C		-1000		+1000	nA
		T_A = +85°C			100		
I²C CONTROLLER/TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS							
Clock Frequency	f_{SCL}					1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$			0.26			µs
CLK Low Period	t_{LOW}			0.5			µs
CLK High Period	t_{HIGH}			0.26			µs
Setup Time Repeated START Condition	$t_{SU;STA}$			0.26			µs
DATA Hold Time	$t_{HD:DAT}$			0			µs
DATA Valid Time	$t_{VD:DAT}$					0.45	µs
DATA Valid Acknowledge Time	$t_{VD:ACK}$					0.45	µs
DATA Setup time	$t_{SU;DAT}$			50			ns
Setup Time for STOP Condition	$t_{SU;STO}$			0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}			0.5			µs
Pulse Width of Spikes that Must be Suppressed by the Input Filter					50		ns
MTP							
V_{DD} Input Supply	VDD_MTP	Reading, erasing, programming		3.1		5.5	V
V_{DD} Current Consumption	$I_{VDD\_MTP\_ERASE}$	Erasing			8		mA
	$I_{VDD\_MTP\_PROG}$	Programming			16		
MTP Erasing/ Programming Time	t_{MTP_ERASE}	Erasing (1 page = 128 x 32-bits word)			100		ms
	t_{MTP_PROG}	Programing			500		µs/32-bit word
MTP Write Capacity	NWrite	VDD1P8 = 2V, VCIN = 5.5V			100		Write
MTP Data Retention	t_{MTP}	VDD1P8 = 2V, VCIN = 5.5V			10		Year
ESD RATINGS							
Human Body Model (HBM)		All pins				±4000	V
Charged Device Model (CDM)		All pins				±1250	V

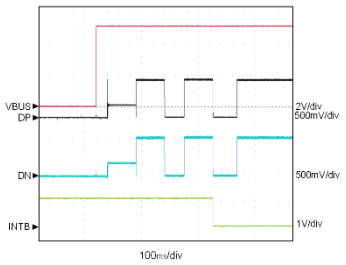
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

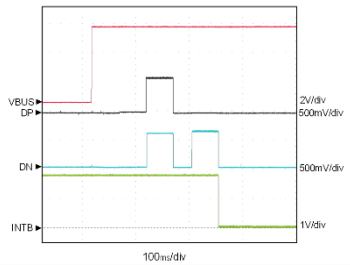
DETECTION STANDARD DOWNSTREAM PORT (SDP)



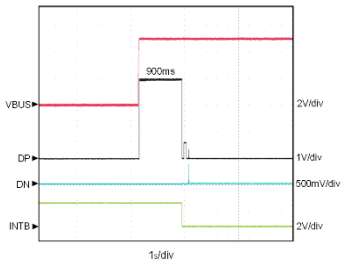
CHARGER DETECTION DEDICATED CHARGING PORT (DCP)



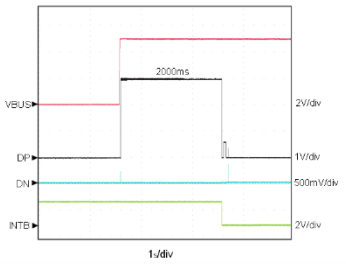
CHARGER DETECTION STANDARD DOWNSTREAM PORT (CDP)



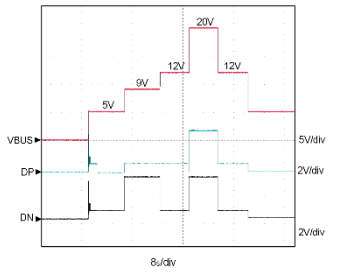
CHARGER DETECTION DATA CONTACT DETECT TIMEOUT 800ms



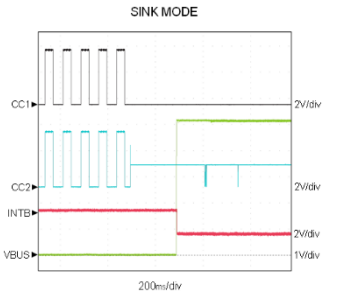
CHARGER DETECTION DATA CONTACT DETECT TIMEOUT 2000ms



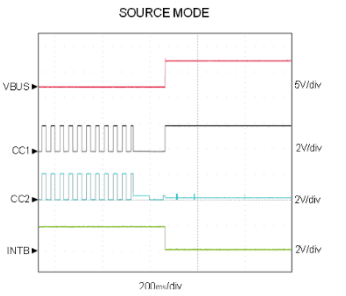
HIGH VOLTAGE DEDICATED CHAERGING PORT (HVDCP)



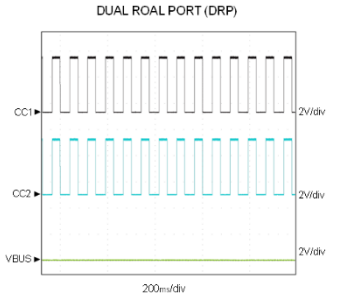
SINK MODE



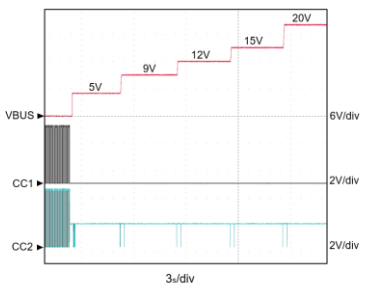
SOURCE MODE



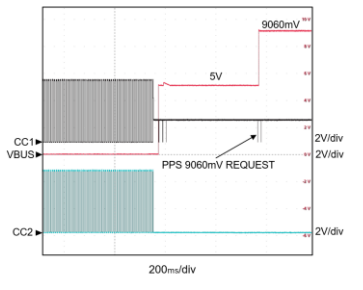
DUAL ROAL PORT (DRP)



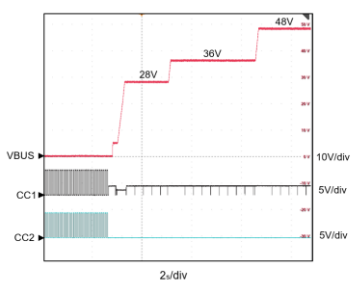
USB-PD FIXED SUPPLY PDO 5V - 20V



USB PD 3.0 PPS, 9060mV, 2.5A SETTING

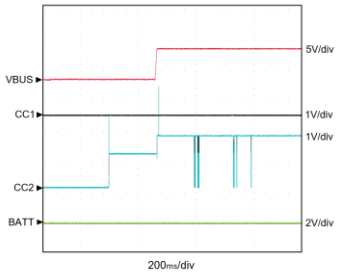


EXTENDED POWER RANGE CHARGE MODE - 28V, 36V, 48V

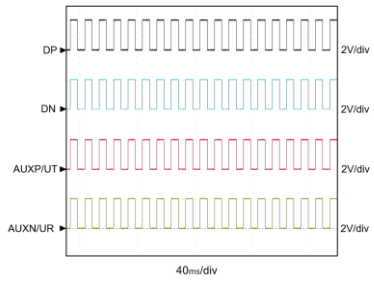


(T_A = +25°C, unless otherwise noted.)

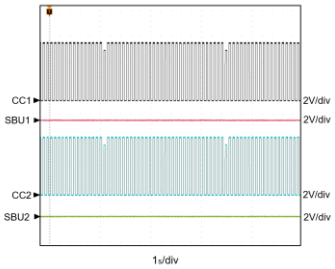
DEAD BATTERY MODE



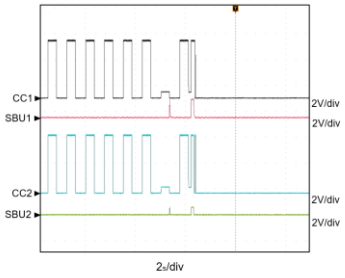
USB DP/DN TO MUX SWITCH TO UART @100Hz



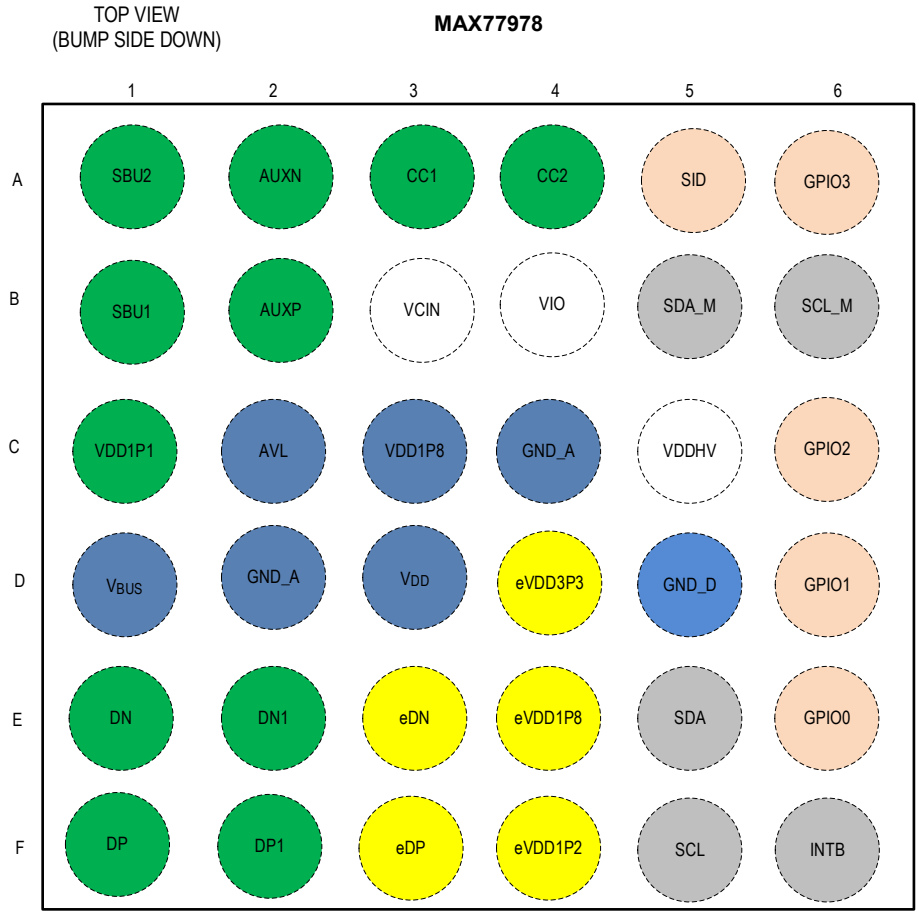
LIQUID CORROSION MITIGATION MODE



LIQUID CORROSION MITIGATION MODE



Pin Configurations



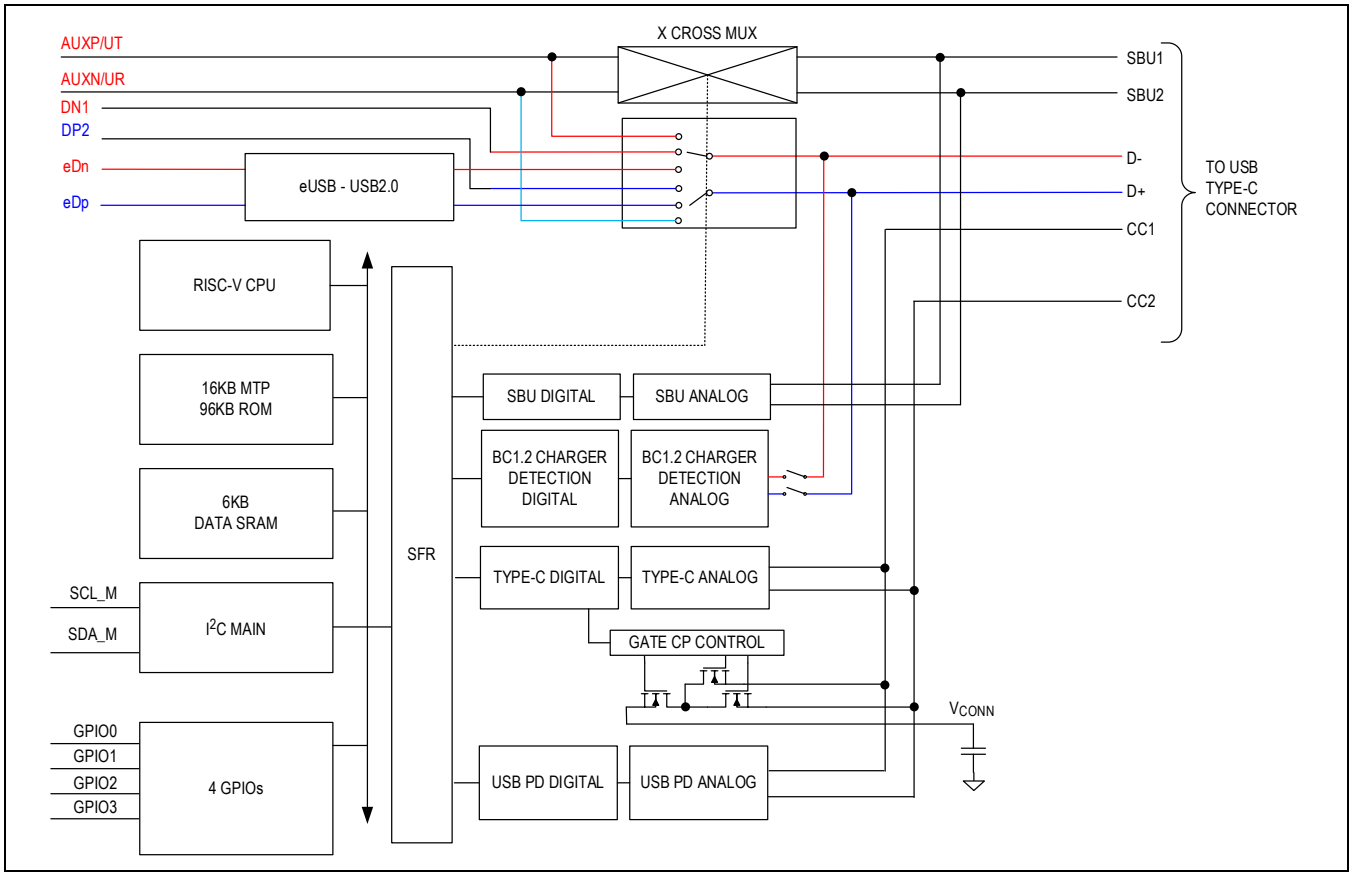
WLP
(3.4mm X 3.4mm 0.5 mm pitch)

Pin Descriptions

PIN	NAME	FUNCTION
B4	VIO	Input for system I/O voltage. Connect a 1µF/6.3V ceramic capacitor to ground.
D1	V_{BUS}	V_{BUS}—Input supply for the internal circuitry when V_{DD} is not present. Bypass V_{BUS} to GND with a 1µF (minimum) ceramic capacitor.
D3	V_{DD}	Power input. V_{DD} supplies power to the internal circuitry when V_{BUS} is not present. Bypass V_{DD} to GND with a 1µF (minimum) ceramic capacitor.
C2	AVL	Analog voltage level. The output of the on-chip LDO powers on-chip and low-noise circuits. Bypass to GND with a 4.7µF/10V ceramic capacitor. Powering external loads from AVL is not recommended, except for pull-up resistors.
C3	VDD1P8	1.8V internal LDO output. Bypass this pin to ground with a 1µF/6.3V ceramic capacitor.
C1	VDD1P1	Digital supply voltage of 1.1V. Bypass with a 1µF/6.3V ceramic capacitor.
E5	SDA	I^2C serial data. Requires an external 2.2kΩ pull-up resistor to VIO.
F5	SCL	I^2C serial clock. Requires an external 2.2kΩ pull-up resistor to VIO.
F6	INTB	Interrupt output. Active-low open-drain output. Requires a 200kΩ pull-up resistor to VIO.
E2	DN1	USB input D-

F2	DP1	USB input D+
E1	DN	Common negative output 1. Connects to D- on USB Type-C connector.
F1	DP	Common positive output 2. Connects to D+ on the USB Type-C connector.
F3	eDP	eUSB input D+
E3	eDN	eUSB input D-
A3	CC1	USB Type-C CC pin 1
A4	CC2	USB Type-C CC pin 2
B3	VCIN	V_{CONN} —Provides power supply to the unused CC pin, if required.
E6	GPIO0	GPIO0 and ADC Input 0.
D6	GPIO1	GPIO1 and ADC Input 1.
C6	GPIO2	GPIO2
A6	GPIO3	GPIO3
A5	SID	Used for I²C target ID (SID) selection at power-up. Tie this pin to GND, or use an external 470kΩ ±10% pull-up or pull-down resistor. See Table 9. After power-up completes, this pin functions as a GPIO pin.
D4	eVDD3P3	3.3V internal LDO output in eUSB re-driver. Bypass this pin to ground with a 2.2µF/10V ceramic capacitor. Add a 0.1µF/10V capacitor in parallel to improve high-frequency performance.
E4	eVDD1P8	1.8V internal LDO output in eUSB re-driver. Bypass this pin to ground with a 2.2µF/6.3V ceramic capacitor. Add a 0.1µF/6.3V capacitor in parallel to improve high-frequency performance.
F4	eVDD1P2	1.2V internal LDO output in eUSB re-driver. Bypass this pin to ground with a 1µF/6.3V ceramic capacitor. Add a 0.1µF/6.3V capacitor in parallel to improve high-frequency performance.
C5	VDDHV	Internal LDO output in eUSB re-driver. Bypass this pin to ground with a 0.1µF/6.3V ceramic capacitor.
D2	GND_A	Analog GND
C4		
D5	GND_D	Digital GND
B5	SDA_M	Controller I²C serial Data. Add an external 2.2kΩ pull-up resistor to VIO.
B6	SCL_M	Controller I²C serial clock. Requires an external 2.2kΩ pull-up resistor to VIO.
B1	SBU1	SBU1—USB Type-C sideband use (SBU1). Functions as a moisture detection channel.
A1	SBU2	SBU2—USB Type-C sideband use (SBU2). Functions as a moisture detection channel.
B2	AUXP	AUXP—DisplayPort AUX positive I/O. Connects to the DisplayPort source through an AC-coupling capacitor. This pin requires a 100kΩ resistor to GND in addition to the AC-coupling capacitor.
A2	AUXN	AUXN—DisplayPort AUX negative I/O. Connects to the DisplayPort source through an AC-coupling capacitor. This pin requires a 100kΩ resistor to 3.3V in addition to the AC-coupling capacitor.

Functional Diagrams



Detailed Description

Overview

The MAX77978 is a fully integrated USB Type-C and USB power delivery (USB PD) management device that supports cable attach and plug orientation detection.

The MAX77978 communicates with the cable and with the USB Type-C and PD device at the opposite end of the cable. The device supports BC1.2 charger detection for backward compatibility with legacy chargers. The IC also integrates a USB switch that supports USB 2.0 and eUSB.

The MAX77978 includes the following main functional blocks:

- USB PD controller
- Type-C detection, including cable attach, orientation detection, and power-role detection
- BC1.2 detection, including HVDCP configuration
- Integrated USB switch for USB 2.0 and eUSB
- Power management circuitry
- Digital core, including RISC-V CPU, MTP, and GPIOs

The USB PD controller provides the physical layer (PHY) for the USB PD protocol. USB PD data is transmitted on either CC1 or CC2, depending on cable orientation.

The Type-C detection analog circuitry automatically detects cable attach and plug orientation.

The MAX77978 supports BC1.2 operation as a portable device or downstream port. The BC1.2 specification defines mechanisms that allow USB devices to draw current above the standard USB limits of 500mA for USB 2.0 and 900mA for USB 3.0.

Through the mechanisms defined in the BC1.2 specification, devices draw up to 1.5A. Detection and advertisement of a higher-current-capable port occur over the USB 2.0 D+ and D- lines after connection.

The BC1.2 specification defines three port types:

- Standard downstream port (SDP)
- Charging downstream port (CDP)
- Dedicated charging port (DCP)

BC1.2 defines a charging port as a downstream-facing USB port that provides power for charging portable equipment. Under this definition, CDP and DCP are charging ports.

The MAX77978 includes high-bandwidth analog switches for D+ and D- pass-through and supports level shifting for eUSB.

The power management circuitry receives and distributes power for the MAX77978 internal circuitry. The device operates from either V_{DD} or V_{BUS}. V_{DD} is the primary supply input. When V_{DD} is unavailable, and V_{BUS} is present, the device enters dead-battery mode, in which a high-voltage LDO steps V_{BUS} down to AVL.

The MAX77978 includes multiple digital interfaces for communication with external devices. The device operates as an I^2C target under host processor control and integrates an I^2C controller for external I^2C devices such as a super-speed mux or retimer.

USB Power Delivery (PD)

BMC

This block provides the physical interface between the USB PD protocol layer and the CC pin. In transmit mode, it encodes the data using bi-phase mark coding (BMC) and drives the CC line at the required voltage levels. In receive mode, it extracts the BMC data from the CC line and converts it into baseband signaling for the protocol layer.

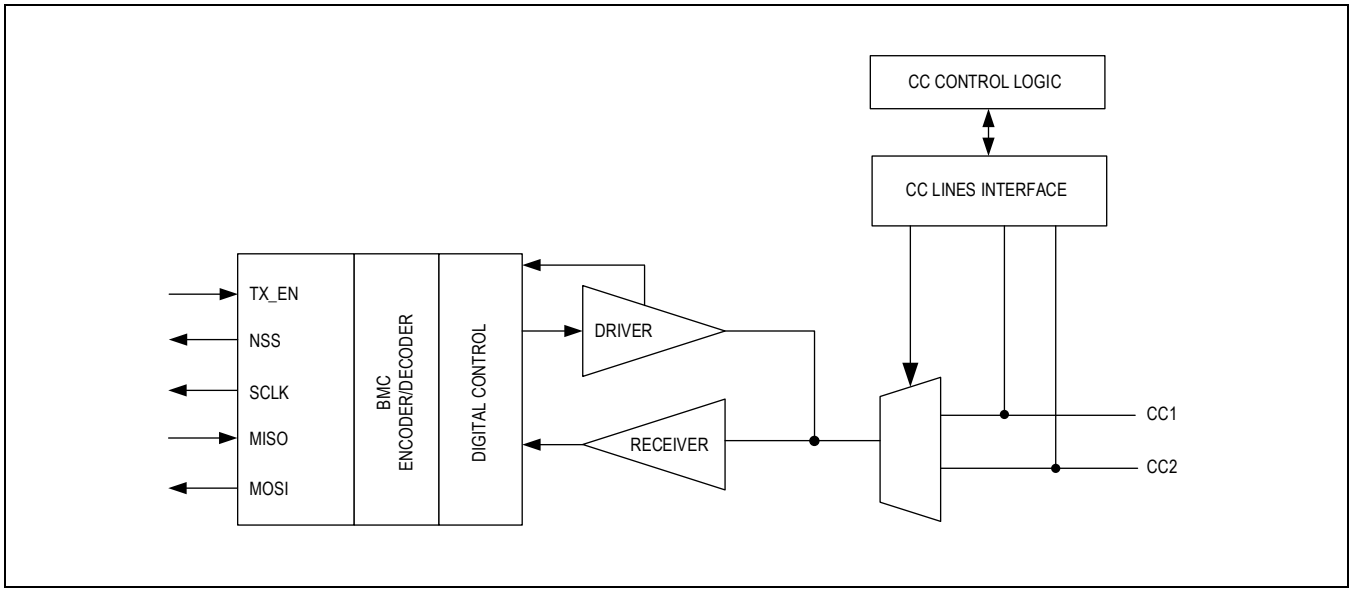


Figure 1. BMC block diagram

BMC Interface Behavior

The BMC block on the MAX77978 uses the connected CC pin for USB Power Delivery communication once an attachment is detected. Although the CC control logic remains responsible for managing the CC line, the BMC communication circuitry operates alongside it without interfering, because its drive activity is very brief and aligned with the CC logic's debounce timing constraints.

In practice, the BMC block performs both BMC encoding and decoding and monitors activity on the CC line, so the external MCU does not need to handle that detection itself. By default, the block stays in receive mode (Rx), listening for incoming communication. Transmit mode (Tx) is only enabled automatically when the internal MCU asserts the TX_EN signal.

Tx Mode

When TX_EN is asserted by the MCU, the BMC block enters Tx mode.

- The NSS signal is driven low, indicating to the MCU SPI/MSP target interface that data transmission on the CC line is active. The MCU provides the data.
- The MAX77978 drives NSS low, indicating to the MCU SPI/MSP target interface that data is requested on the MISO line.
- The MAX77978 drives the SCLK signal.
- The MCU presents transmit data on the MISO line. The MAX77978 samples the data on the rising edge of SCLK. Data are stable at this edge.
- The BMC block encodes the sampled data from the MISO line and drives the CC line in accordance with the USB PD standard.

When all data are transmitted, the MCU drives TX_EN low to indicate the end of transmission. The MAX77978 terminates transmission with the corresponding trailing-edge termination. The device then returns to the default state and releases the CC line from the BMC driver to the pull-up/pull-down CC line interface.

Rx Mode

Rx mode is the default state of the BMC interface. In this mode, the receiver listens to the connected CC line. It does not drive the CC line interfaces or interact with the CC control logic. When data are detected and received on the CC line, according to the activity defined in the USB PD specification, the BMC interface:

- Drives the NSS signal low.
- Outputs the recovered clock on the SCLK signal.
- Outputs the recovered data on the MOSI line to the connected MCU.

The data are valid on the falling edge of SCLK and are sampled on this edge by the MCU SPI/MSP interface. When no more data are detected on the CC line, the NSS signal goes high.

Protocol Layer

The protocol layer is responsible for managing messages to and from the physical layer. It automatically handles protocol receive timeouts, the message counter, the retry counter, and GoodCRC messages. It also communicates with the internal policy engine.

Policy Engine

The policy engine manages power negotiation with the connected device based on its source role. It implements the complete state machine that controls protocol-layer message formation and scheduling. The policy engine uses the protocol layer to send and receive messages. It also interprets input from the device policy manager to enforce port policy and directs the protocol layer to transmit the appropriate messages.

USB Type-C Detection

Figure 2 shows the plug-and-orientation detection block for each CCx pin (CC1 and CC2). Each pin uses identical detection circuitry.

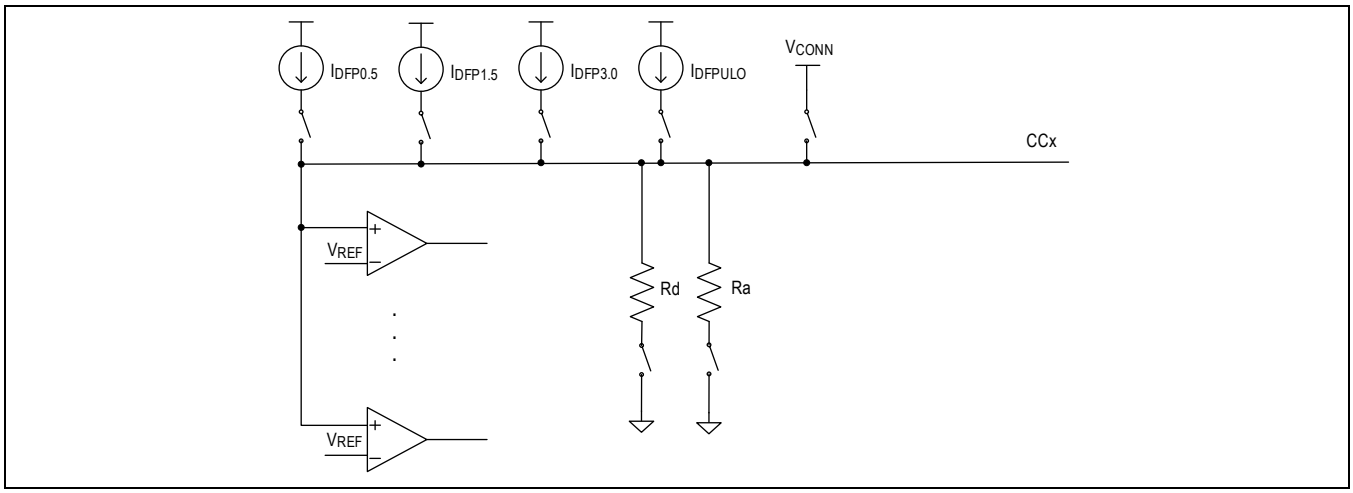


Figure 2. Type-C detection block

Configured as a Source

When configured as a Source, the MAX77978 detects whether a cable or a Sink is attached by monitoring the CC1 and CC2 pins. In the unattached state, the device monitors the voltage on these pins to determine whether anything is connected.

Table 1. Source terminal state

CC1	CC2	CONNECTION STATE	EXPECTED ACTION
Open	Open	Nothing attached	Continue monitoring both CCx pins for attachment.
Rd	Open	Sink attached	Monitor CC1 for detachment.
Open	Rd	Sink attached	Monitor CC2 for detachment
Ra	Open	Powered Cable – No UFP attached	Monitor CC2 for a Sink attach and CC1 for a cable detachment.
Open	Ra	Powered Cable – No UFP attached	Monitor CC1 for a Sink attach and CC2 for a cable detachment.
Ra	Rd	Powered Cable – UFP attached	Provide power on V_{CONN} (CC1), then monitor CC2 for a Sink detach.CC1 is not monitored for detachment.
Rd	Ra	Powered Cable – UFP attached	Provide power on V_{CONN} (CC2), then monitor CC1 for a Sink detach.CC2 is not monitored for a detachment.
Rd	Rd	Debug Accessory Mode attached	Sense either CCx pin for detachment.
Ra	Ra	Liquid corrosion mitigation mode attached	Sense either CCx pin for detachment.

In Source mode, the MAX77978 drives a current of $I_{DFP0.5}$ on each CCx pin and monitors the resulting voltage to determine the connection state. When a Sink is attached, a pull-down resistor Rd to ground is present. The $I_{DFP0.5}$ current flows through Rd, creating a voltage on the CCx pin. The MAX77978 uses $I_{DFP0.5}$ as the default current advertisement, and the application firmware can later change this to $I_{DFP1.5}$ or $I_{DFP3.0}$.

If the CCx pin is connected to the V_{CONN} input of an active cable, a different pull-down resistance, Ra, is present. In this case, the lower voltage on the CCx pin enables the PD controller to detect an active cable.

The voltage on CCx is also monitored to detect disconnection, based on which Rp current source is active. After a connection has been detected, if the voltage on CCx rises above the disconnect threshold for t_{CCDeb}, the system registers a disconnection.

The MAX77978 also includes an ultra-low current source, I_{DFPULO}, to measure the impedance between the CCx pins and ground. This feature is useful for detecting moisture on the CCx pins in the USB Type-C receptacle.

Configured as a Sink

The MAX77978 can be configured as a UFP only by setting the register bit to Sink Only Mode. In UFP mode, the device continuously presents a pull-down resistor (Rd) on both CC pins. It monitors the CC pins for the voltage level corresponding to the Type-C current advertisement from the connected DFP. The MAX77978 debounces the CC pins and waits for V_{BUS} detection before successfully attaching. As a UFP, it detects the advertised current level of the DFP and reports it to the system through the I2C STATUS_ register once, when entering the attached SNK state.

Configured as a DRP

The MAX77978 can be configured to operate in DRP mode by setting the appropriate register accordingly. In this mode, the device toggles between DFP and UFP operation. When acting as a DFP, the MAX77978 complies with the requirements and behavior defined for a DFP in the USB Type-C specification. When acting as a UFP, it operates according to the requirements defined for a UFP in the USB Type-C Specification.

Try.SNK Support

The MAX77978 operates as a dual-role port (DRP) by default, meaning it can function either as a power sink/USB data peripheral or as a power source/USB data host. Its USB Type-C state machine alternates between Source and Sink states approximately every 75 ms. As a result, when the IC is connected to another DRP device, such as a PC with a USB Type-C port, the initial source/sink role is assigned unpredictably.

If the desired behavior is for the mobile phone to assume the sink role when connected to a PC, the MAX77978 supports Try.SNK mode. When enabled, Try.SNK causes the device to strongly prefer the sink role when attached to a standard DRP partner. However, if both connected devices have **Try.SNK** enabled, the final role assignment again becomes unpredictable.

DebugAcessory.SRC Support

When operating in the source power role, the IC can detect a debug and test system (DTS). A debug accessory is identified when both the CC1 and CC2 pins are pulled down to ground through Rd resistors by the attached device.

DebugAcessory.SNK Support

The IC detects a connection to a DTS when it is operating in the sink power role. A debug accessory is detected when the connected device pulls both the CC1 and CC2 pins up with Rp resistors. The voltage present on the CC pins indicates the plug orientation and the advertised current capability.

Table 2. Rp/Rp Charging Current Values for a DTS Source

MODE OF OPERATION	CC1	CC2
Default USB power	Rp for 3A	Rp for 1.5A
USB Type-C current at 1.5A	Rp for 1.5A	Rp for default
USB Type-C current at 3A	Rp for 3A	Rp for default

USB BC1.2 Detection

Description

USB charger detection is BC1.2 compliant and supports automatic detection of several common proprietary charger types.

USB charger detection is controlled through the I2C register map using the following bits:

- **ChgDetEn**: enables charger detection.
- **ChgDetMan**: manually requests a new charger detection cycle.

The charger detection state machine complies with the USB BC1.2 specification and detects SDP, CDP, and DCP charger types. If D+/D− are open, ChgTyp reports SDP, as required by the BC1.2 specification.

In addition to BC1.2 charger detection, the device detects a limited set of proprietary charger types, including Apple, Samsung, and generic 500 mA chargers. The device always reports the detected SDP, CDP, or DCP type, as well as any detected proprietary charger type.

For example, a Samsung charger presents a D+/D− short with bias on D+/D−. This bias causes a BC1.2-compliant detection state machine to identify the charger as a DCP. Accordingly, the device reports the charger as both DCP and Samsung.

The device also automatically sets the V_{BUS} input current limit based on the detected BC1.2 charger type.

The operating status of the charger detection state machine is reported by the ChgTypRun interrupt bit in the USB I^2C register map.

Table 3. Charger Type Detection Table

USB BC1.2 DETECTED CHARGER TYPE	
ChgTyp VALUE	**CHARGER DETECTED**
00	No V_{BUS}
01	SDP
10	CDP
11	DCP

Note: *Charge detect running state is indicated until the charger detection state machine is complete.*

Table 4. Proprietary Detection Table

		D+				
		0 – 3.2V	**0.32V - 31%**	**31 - 47%**	**47 - 64%**	**64 - 100%**
D-	**0 – 0.32V**	Unknown	Unknown	Unknown	Unknown	Unknown
	0.25V - 31%	Unknown	Samsung	Unknown	Unknown	Unknown
	31 - 47%	Unknown	Unknown	Apple 0.5A	Apple 2.0A	Unknown
	47 - 64%	Unknown	Unknown	Apple 1.0A	Apple 12W	Unknown
	64 - 100%	Unknown	Unknown	Unknown	Unknown	Unknown

Examples of ChgTyp and PrChgTyp values found for common chargers on the market.

Table 5. Proprietary Charger Detection List

T_A	ChgTyp	PrChgTyp
DCP	0x03 DCP	0x00 unknown
SDP	0x01 SDP	0x00 unknown
CDP	0x02 CDP	0x00 unknown
Samsung 2A DCP	0x03 DCP	0x01 Samsung
Apple 500mA	0x01 SDP	0x02 Apple 500mA
Apple 1A	0x02 CDP	0x03 Apple 1A
Apple 2A	0x01 SDP	0x04 Apple 2A
Apple12W	0x03 DCP	0x05 Apple 12W

Table 6. HVDCP Detection

VOLTAGE ON D+/D-		QC2.0 VOLTAGE	QC2.0 AutoSet MODE VOLTAGE FOR SUCCESS REPLY	
D+	**D-**	**ADAPTER VOLTAGE**	**MINIMUM**	**MAXIMUM**
0.6V	0.6V	12V	10.5V	13.5V
3.3V	0.6V	9V	7.5V	10.5V
3.3V	3.3V	20V	18.5V	No Max
0.6V	3.3V	Reserved	NA	NA
0.6V	Ground	5V	4.0V	6.0V

Power Management and Power Supplies

The MAX77978 power management block includes a power selector that selects between V_{DD} and V_{BUS}. It transitions seamlessly between V_{DD} and V_{BUS}.

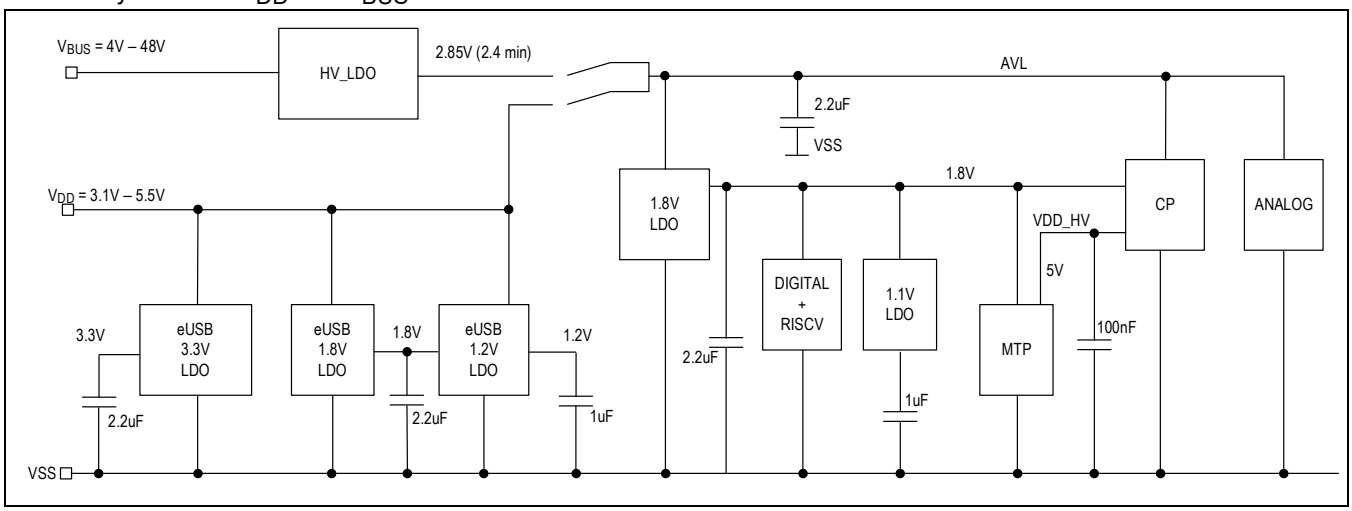


Figure 3. Power management block

The MAX77978 generates the voltages required to power its internal circuitry. The generated power rails are VDD1P8, VDD1P1, VDDHV, eVDD3P3, eVDD1P8, eVDD1P2, and AVL.

The MAX77978 provides power-management support to reduce application power consumption. It supports Standby mode and FSHIP mode.

During dead-battery operation, the MAX77978 applies voltage clamps to both CC pins, allowing the system to operate as a power sink.

V_{BUS} LDO

The MAX77978 includes an internal high-voltage LDO that converts V_{BUS} to AVL to power internal device circuitry. The V_{BUS} LDO operates only when V_{DD} is low, during the dead-battery condition. The V_{BUS} LDO is powered from V_{BUS}.

Table 7. General GPIO

#	TYPE	DEFAULT	POWER DOMAIN	ADDITIONAL FUNCTION
GPIO0	Push-Pull	Output OD	V_{IO}	ADC
GPIO1	Push-Pull	Output OD	V_{IO}	ADC
GPIO2	Push-Pull	Output OD	V_{IO}	V_{BUS} discharge enable (Active high or low)
GPIO3	Push-Pull	Output OD	V_{IO}	FRS signal detection * (Active high or low)

**: when FRS signal detected, GPIO2 toggle to force charger enable reverse boost to provide OTG*

eUSB2-USB2.0 Repeater

The MAX77978 configures a USB 2.0-compliant port on a lower-voltage application processor. The device integrates a USB-compliant eUSB2/USB 2.0 repeater that converts USB-to-eUSB signals and supports both device and host modes. It supports USB low-speed (LS), full-speed (FS), and high-speed (HS) signals.

The MAX77978 provides compensation settings through register bits. These settings optimize compensation for eUSB channel loss profiles and improve jitter performance.

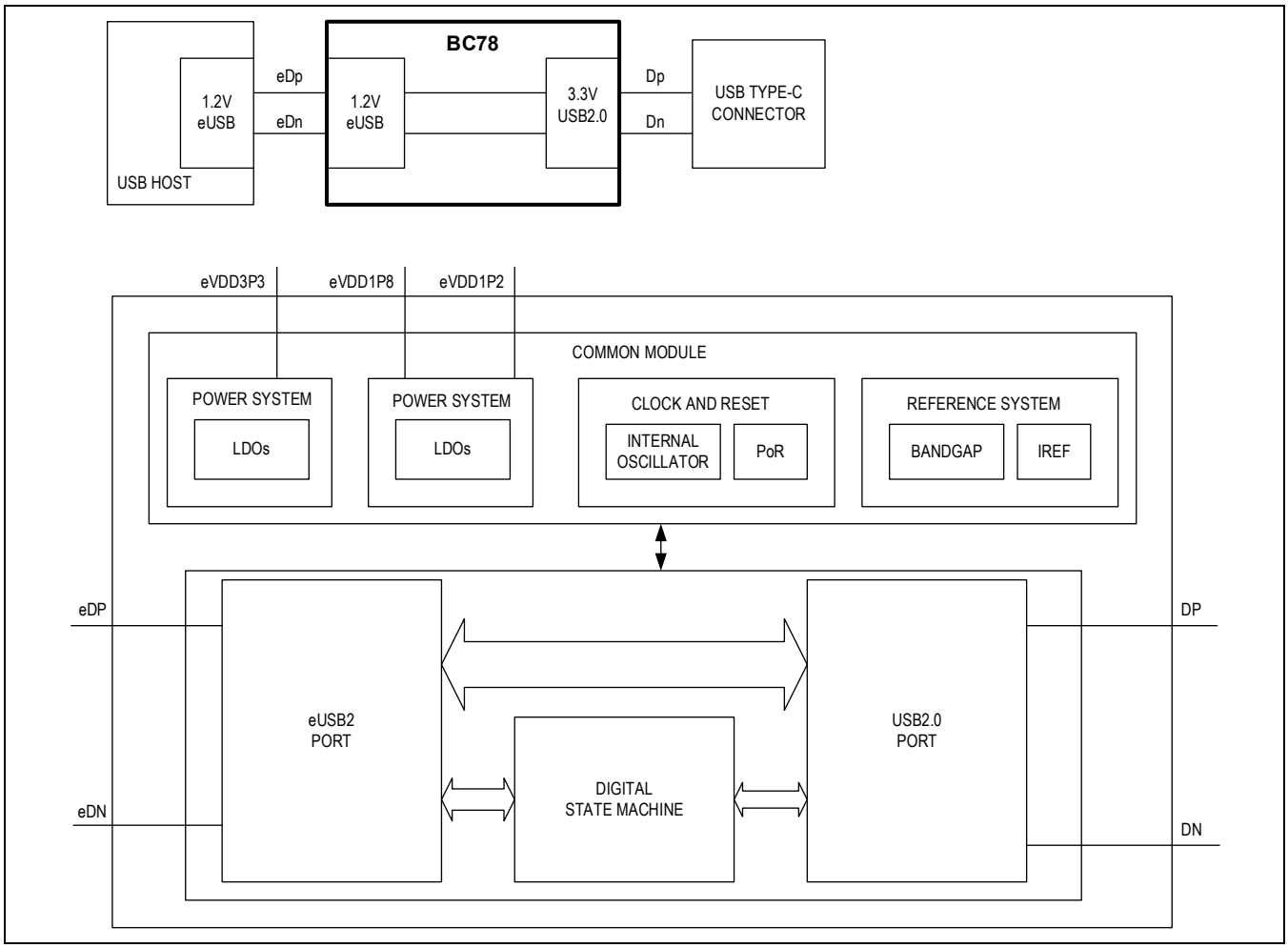


Figure 4. eUSB2-USB2.0 repeater system block diagram

The internal USB switch routing is controlled by the EUSB_CTRL and VENDOR_USBSW_CTRL opcode commands. Depending on the command setting, DP and DN are routed to eDP/eDN for eUSB operation or to DP1/DN1 for USB 2.0 operation. Both routing configurations support bidirectional signal paths.

V_{CONN} Switch

Description

The MAX77978 integrates a V_{CONN} switch that connects V_{CIN} to either CC1 or CC2. After CC detection identifies Ra on one CC pin, the V_{CONN} switch routes V_{CIN} to the unused CC pin.

The device also provides a programmable V_{CONN} current limit from 200mA to 900mA in 100mA steps. If the V_{CONN} load current exceeds the programmed current limit for 3ms, the device generates an interrupt to the application processor (AP). To continue supplying V_{CONN} power, the AP must program a higher current limit or disable the current limit within 12ms. Otherwise, the device turns off the V_{CONN} switch 12ms after the interrupt is generated.

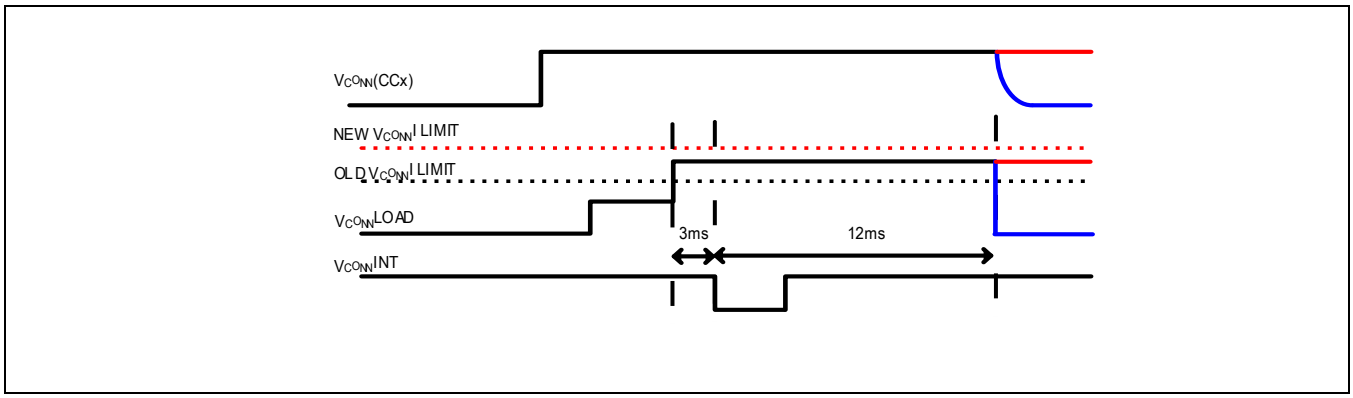


Figure 5. V_{CONN} overcurrent protection operation

Type C Alt Mode and SBU Mux

The MAX77978 integrates an SBU crossbar mux to support USB Type-C Alt Mode operation. Firmware configures the mux setting automatically based on the active CC pin.

When CC1 is the active channel, the mux routes SBU1 to AUXP and SBU2 to AUXN. When CC2 is the active channel, the mux routes SBU2 to AUXP and SBU1 to AUXN.

UART Support

The MAX77978 supports a UART signal path by reconfiguring the internal D+/D− switch. When VENDOR_USBSW_CTRL (0x93) selects the AUX path, DP routes to AUXP (UT) and DN routes to AUXN (UR), enabling UART communication through the USB connector.

FSHIP Mode

1. **Entering FSHIP mode.** The MAX77978 enters FSHIP mode when the opcode command 0x91 0x01 is issued. In FSHIP mode, the device minimizes power consumption and draws the typical I_{FSHIP} supply current.
2. **Exiting FSHIP mode.** The MAX77978 exits FSHIP mode automatically upon detection of a valid V_{BUS}. To resume normal operation, V_{BUS} must be applied to the device.

Dead Battery Mode

Dead battery mode allows a battery-powered system to draw power from V_{BUS} when the battery is discharged, enabling battery charging to begin. This mode also supports systems powered only from V_{BUS}.

Dead battery mode is supported only in sink power role and dual power role configurations. In dead battery mode, the MAX77978 presents an Rd termination on the CC pins and advertises sink capability even when the device is not powered.

When a source connects to a USB Type-C port with the MAX77978 in dead battery mode, the source detects the 1.1V active clamp, establishes a source-to-sink connection, and applies V_{BUS}. The MAX77978 is then powered through the V_{DD} pin when V_{DD} is connected to V_{BUS} on the USB Type-C receptacle side.

ADC

The MAX77978 ADC is shown in *Figure 6*. The ADC is an 8-bit successive approximation ADC. The ADC input is an analog input mux that supports multiple inputs from various voltages within the device.

The output from the ADC is available for reading and use by application firmware.

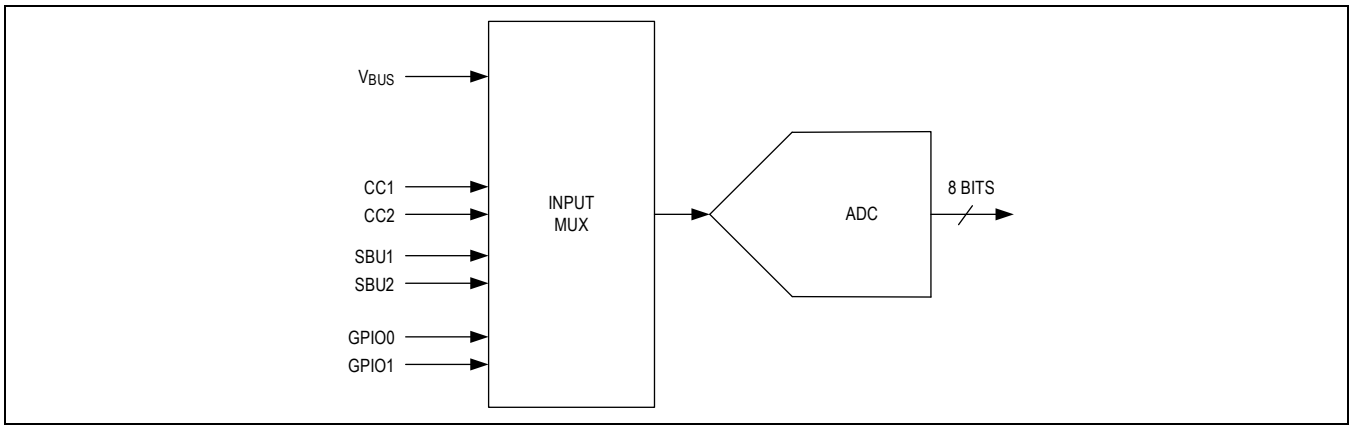


Figure 6. ADC block

System Faults

The IC monitors the system for the following faults:

- Undervoltage lockout
- VIO fault

VIO Fault

When VIO falls below 1.0V, the IC goes into the shutdown state.

Once VIO voltages rise higher than 1.3V, the IC comes out of shutdown state.

Reset

The IC has different levels of reset as follows:

- VDD1P8 < 1.775V (Typ.)
- Software Reset (SW_RESET = 0x0F)

WDT Reset

1. The MAX77978 restarts the watchdog timer with a 1.86s timeout period.
2. If the watchdog timer is not refreshed before the timeout expires, the device performs the following actions:
   a) The MAX77978 reboots.
   b) The MAX77978 updates the USB_STUATS2 register (0x09) to indicate the system message. A value of 0x03 corresponds to a watchdog timeout event (MA_SYSERROR_BOOT_WDT).

Firmware (FW) Recovery Function

The MAX77978 includes a FW recovery function. If an FW update fails, the FW version reads FF.FF. In this condition, the device supports recovery using ROM firmware FE.ED.

To restore the production FW, the application processor (AP) issues the following opcode command: 0xDF 0xDA 0xA5 0xAD 0x78.

The FW recovery opcode command is valid only when the FW version reads FF.FF. Analog Devices provides a sample kernel driver to support FW recovery.

Liquid Corrosion Mitigation Mode

The MAX77978 supports moisture detection and dry detection on the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector to help mitigate corrosion caused by liquid ingress. Contaminants such as water, sweat, or salt solution can create a leakage path to GND and reduce the effective pin impedance well below the open-circuit condition. The device detects this condition by sourcing a low-level current into the selected pin and measuring the resulting pin voltage.

The selected pin is routed through an analog input mux to both a comparator and an ADC, as shown in *Figure 7*. The comparator provides a fast, threshold-based indication, and the ADC provides a digitized measurement. The ADC input mux supports monitoring of CC1, CC2, SBU1, and SBU2.

When a wet or dry condition is detected, the MAX77978 sets the Wtr bit in the CC_STATUS1 register and asserts the WtrI interrupt in CC_INT to notify the application processor.

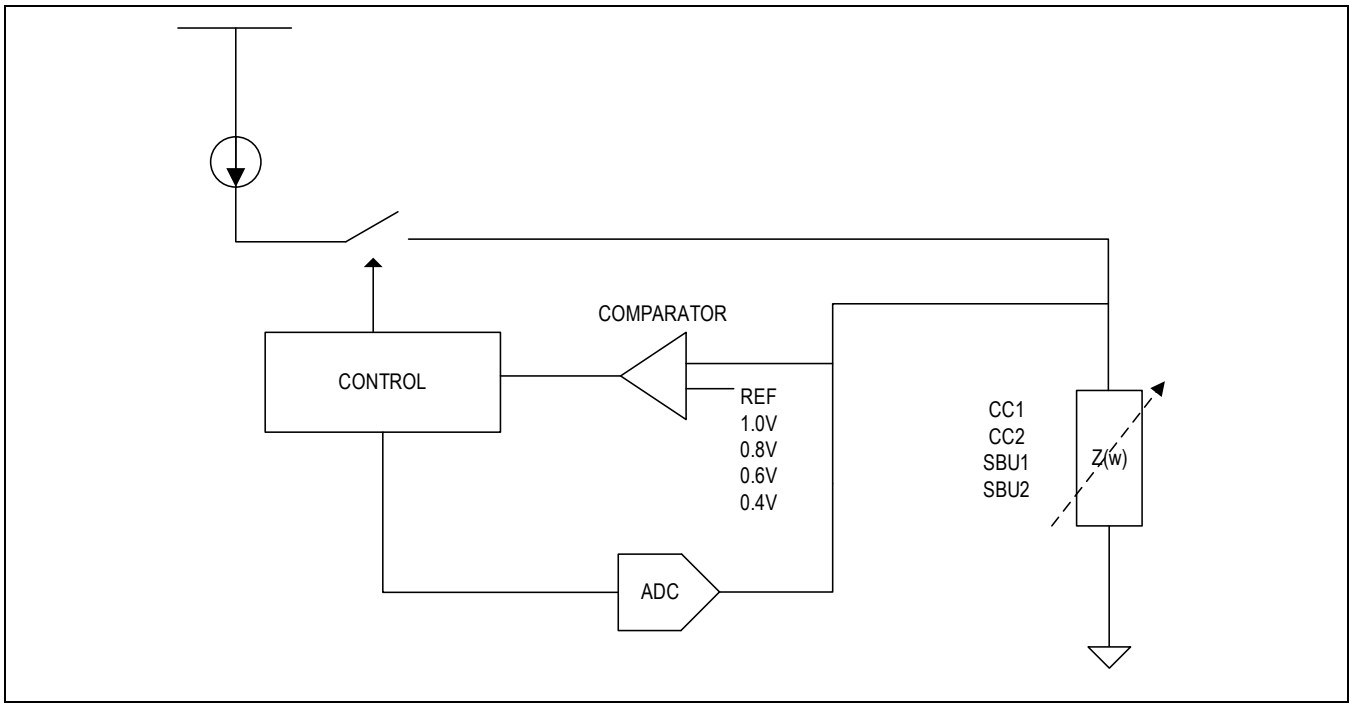


Figure 7. Moisture detection ADC/comparator block

Liquid Corrsion Mitigation Mode Sequence

1. **Mitigation Mode Entry.** Moisture detection runs periodically while the port is unattached and is integrated into the DRP toggle cycle. During each detection cycle, the device applies a low-level current to CC1 and CC2 and compares the resulting pin voltage against the CC moisture threshold. If either CC pin voltage is below the threshold, the device schedules an SBU measurement and compares the resulting SBU1 and SBU2 voltages against the SBU moisture threshold, as shown in *Figure 8*. When both the CC and SBU measurements indicate a wet condition, the connector is declared wet, and the MAX77978 enters corrosion mitigation mode. The CC and SBU moisture thresholds are independently programmable through the ccWtrSel and sbuWtrSel fields.
2. **Dry Detection.** In corrosion mitigation mode, the MAX77978 periodically applies the measurement current to SBU1 and SBU2 and compares the resulting voltages against the SBU dry threshold, as shown in *Figure 9*. While either SBU pin voltage remains below the threshold, the device remains in dry detection mode and continues toggling the SBU at the programmed period.
3. **Mitigation Exit.** When both SBU1 and SBU2 voltages rise above the SBU dry threshold, the MAX77978 schedules a CC measurement after a programmable delay and compares the resulting CC1 and CC2 voltages against the CC dry threshold. If both CC pin voltages exceed the threshold, the connector is declared dry. The device clears Wtr in CC_STATUS1, asserts WtrI to notify the application processor, exits corrosion mitigation mode, and resumes normal DRP operation. If either CC pin voltage remains below the threshold, the device returns to dry detection mode and continues toggling the SBU.

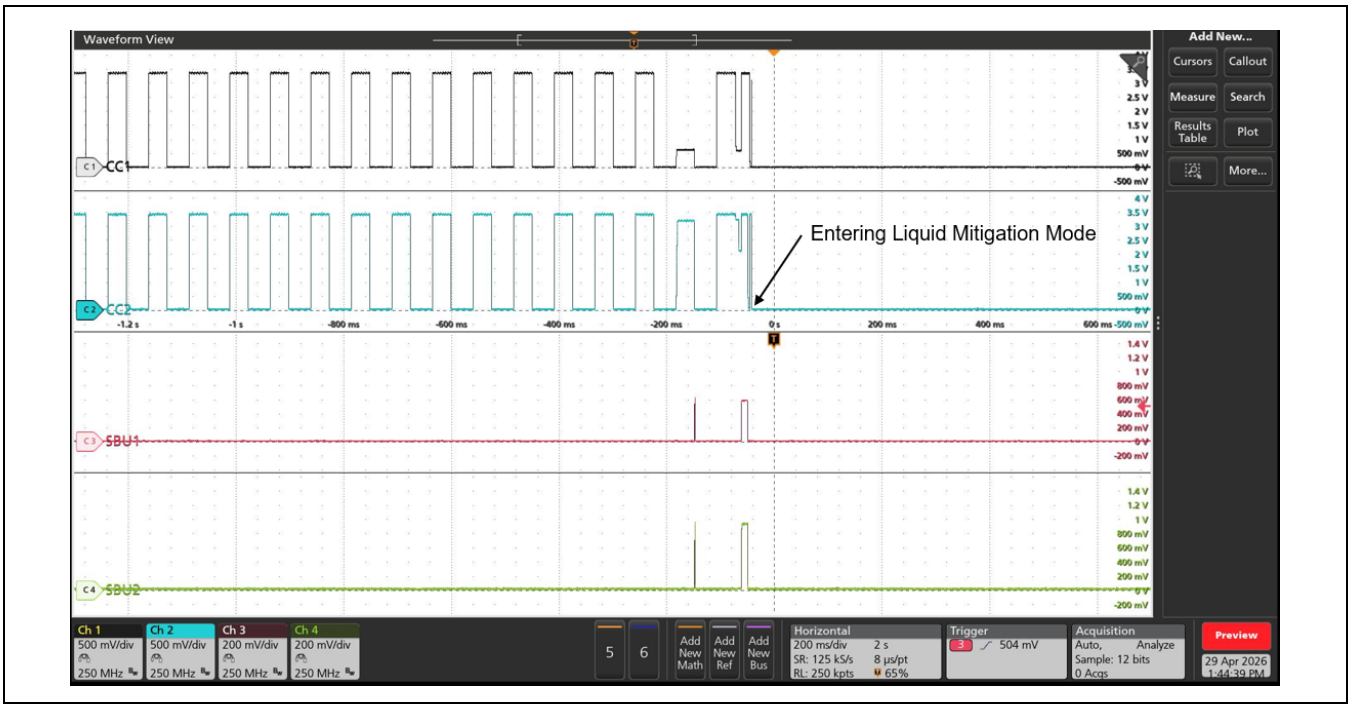


Figure 8. CC and SBU waveforms at entry into corrosion mitigation mode

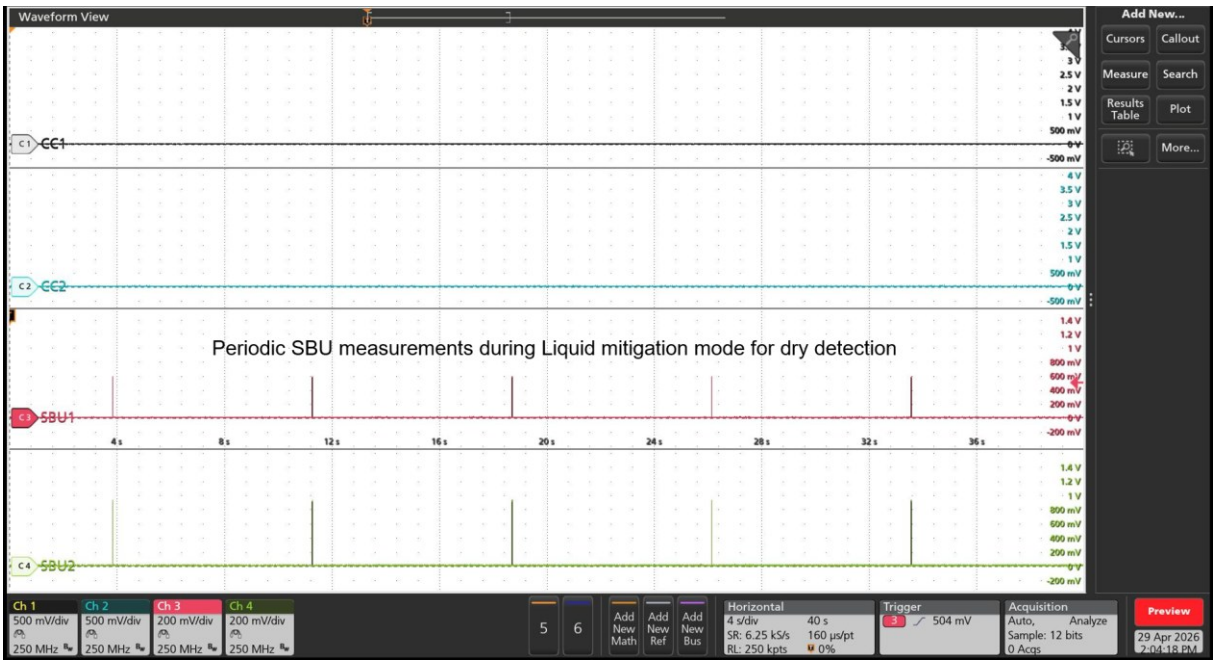


Figure 9. CC and SBU waveforms at corrosion mitigation mode

Figure 10. CC and SBU waveforms at exiting corrosion mitigation mode

AVS (Adjustable Voltage Supply) Function

The MAX77978 supports the adjustable voltage supply (AVS) feature defined in the USB PD 3.2 specification. AVS allows the sink to request finely adjustable output voltage and current from the source in 100mV steps, rather than selecting only fixed PDOs. This capability allows the application to optimize power delivery for system efficiency and battery charging profiles. The MAX77978 supports both SPR AVS and EPR AVS, up to the full 240W EPR range.

To request an AVS voltage, the application processor (AP) issues the SrcCap AVS request opcode command (0x28) with the target PDO position, output voltage, and operating current. After the source accepts the request, V_{BUS} transitions to the requested voltage.

By issuing successive AVS requests with increasing voltage values, the AP can sweep V_{BUS} smoothly across the supported range. *Figure 11* shows V_{BUS} ramping from 9V to 20V in 100mV steps using successive AVS requests.

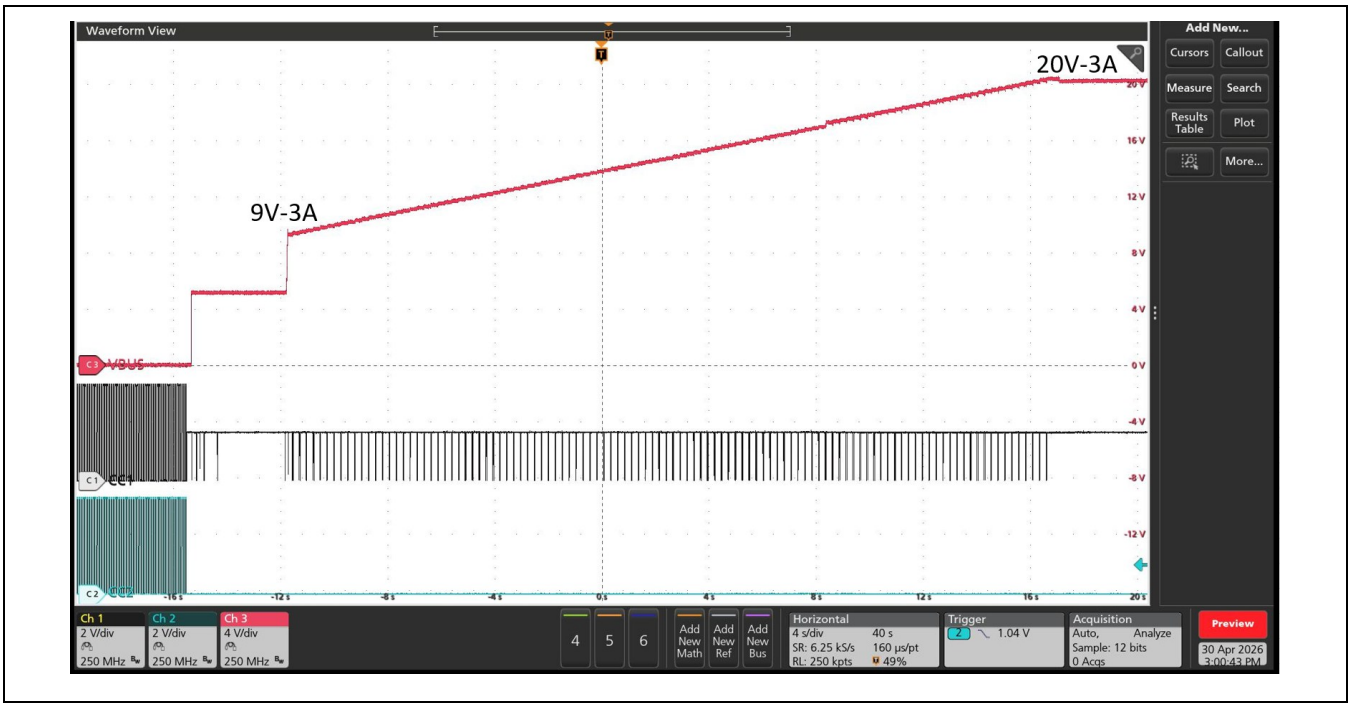


Figure 11. AVS waveform from 9V to 20V through successive AVS requests.

Extended Power Range (EPR)

The MAX77978 supports USB PD 3.2 extended power range (EPR) operation in both Source and Sink roles. The device supports EPR contracts of 28V at 5A (140W), 36V at 5A (180W), and 48V at 5A (240W), in addition to standard SPR fixed PDOs. EPR adjustable voltage supply (AVS) APDOs are also supported.

Entry into EPR mode is initiated by the sink with an EPR_Mode (Enter) message. The source responds with Enter Acknowledged, reconfirms cable EPR capability through SOP' Discover Identity, and then issues Enter Succeeded, followed by a chunked EPR_Source_Capabilities message that includes all SPR PDOs, EPR PDOs, and the AVS APDO.

Once in EPR mode, the sink and source exchange EPR_KeepAlive Extended Control messages as required by the USB PD specification to maintain the contract. EPR mode exists on EPR_Mode (Exit), KeepAlive timeout, Hard Reset, or detach.

Table 8. PD communication Log captured during EPR Mode Entry to 48V Contract

#	MESSAGE	DATA ROLE	POWER ROLE	SOP	DURATION (µs)	DELTA (µs)
0	Source_Capabilities (Fixed 5V-3A, 9V-3A, 12V-3A, 15V-3A, 20V-3A)	DFP	SRC	SOP	1,286	737
1	GoodCRC	UFP	SNK	SOP	503	76
2	Request (Object pos: 1, 5V/3A)	UFP	SNK	SOP	636	923
3	GoodCRC	DFP	SRC	SOP	496	33
4	Accept	DFP	SRC	SOP	497	859
5	GoodCRC	UFP	SNK	SOP	503	77
6	PS_RDY	DFP	SRC	SOP	497	31,714
7	GoodCRC	UFP	SNK	SOP	504	76
8	EPR_Mode (Enter)	UFP	SNK	SOP	636	4,061,549
9	GoodCRC	DFP	SRC	SOP	497	32
10	EPR_Mode (Enter Acknowledged)	DFP	SRC	SOP	628	959
11	GoodCRC	UFP	SNK	SOP	504	76
12	EPR_Mode (Enter Succeeded)	DFP	SRC	SOP	628	6,242
13	GoodCRC	UFP	SNK	SOP	503	76
14	EPR_Source_Capabilities (Chunk #0 resp)	DFP	SRC	SOP	1,435	18,766
15	GoodCRC	UFP	SNK	SOP	503	76
16	EPR_Source_Capabilities (Chunk #1 req)	UFP	SNK	SOP	637	758
17	GoodCRC	DFP	SRC	SOP	498	31
18	EPR_Source_Capabilities (Chunk #1 resp, Fixed 28V-5A, 36V-5A, 48V-5A)	DFP	SRC	SOP	1,023	698
19	GoodCRC	UFP	SNK	SOP	503	77
20	EPR_Request (Object pos:10, 48V-5A)	UFP	SNK	SOP	770	304,349
21	GoodCRC	DFP	SRC	SOP	497	32
22	Accept	DFP	SRC	SOP	498	926
23	GoodCRC	UFP	SNK	SOP	503	76

24	PS_RDY	DFP	SRC	SOP	497	691,180
25	GoodCRC	UFP	SNK	SOP	502	76
26	Extended_Control_MSG (EPR_KeepAlive)	UFP	SNK	SOP	636	342,470
27	GoodCRC	DFP	SRC	SOP	497	32
28	Extended_Control_MSG (EPR_KeepAlive_Ack)	DFP	SRC	SOP	628	1,696
29	GoodCRC	UFP	SNK	SOP	503	76
39	Extended_Control_MSG (EPR_KeepAlive)	UFP	SNK	SOP	636	342,773
31	GoodCRC	DFP	SRC	SOP	497	32
32	Extended_Control_MSG (EPR_KeepAlive_Ack)	DFP	SRC	SOP	628	1,751
33	GoodCRC	DFP	SNK	SOP	503	76

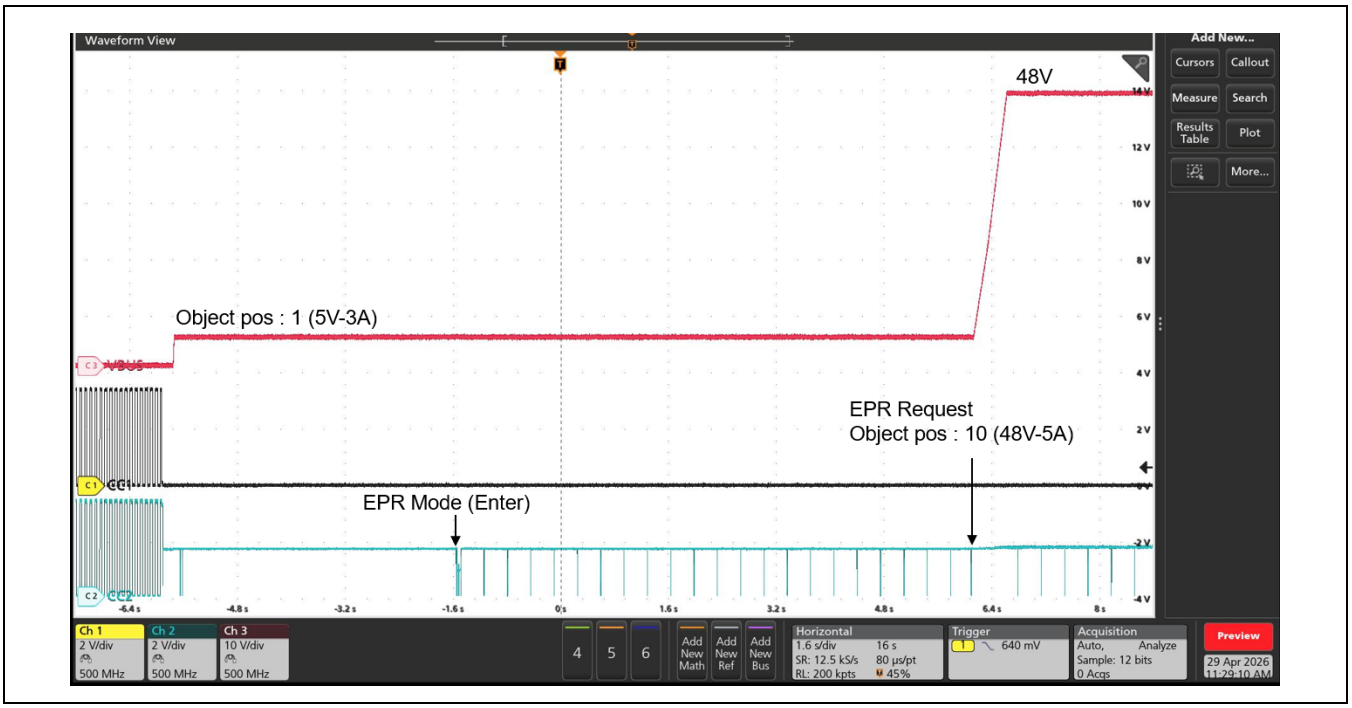


Figure 12. EPR mode 48V contract

I²C Serial Interface

The I²C serial bus consists of a bidirectional serial data line (SDA) and a serial clock line (SCL). I²C is an open-drain bus. SDA and SCL require pull-up resistors with a value of 500Ω or greater. Optional 24Ω series resistors on the SDA and SCL lines help protect the device inputs from high-voltage bus spikes. The series resistors also minimize crosstalk and undershoot on the bus lines.

System Configuration

The I²C bus is a multi-controller bus. The maximum number of devices that can attach to the bus is limited only by bus capacitance.

Figure 13 shows an example of a typical I²C system. A device on the I²C bus that sends data is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates data transfer and generates the SCL clock signal to control it is the controller. Any device addressed by the controller is considered a target. When the MAX77978 I²C-compatible interface is operating, it is a transmitter on the I²C bus, and it can be both a transmitter and a receiver.

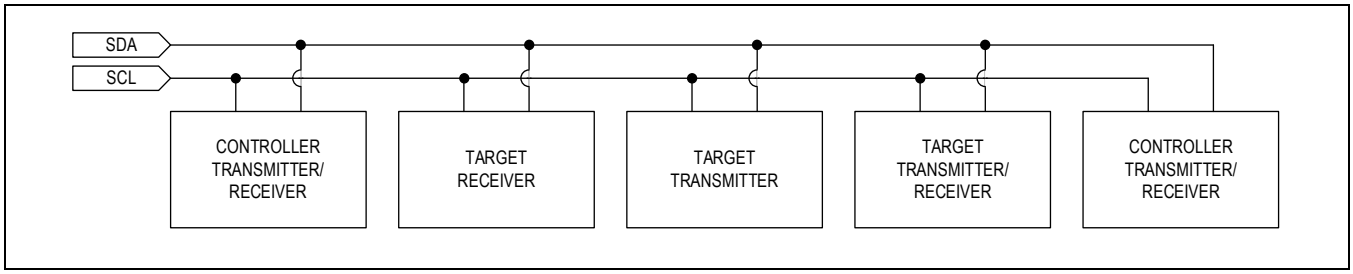


Figure 13. Functional logic diagram for communications controller

Bit Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA remains stable during the high portion of the SCL clock pulse. Changes on SDA while SCL is high indicate control signals, specifically START and STOP conditions.

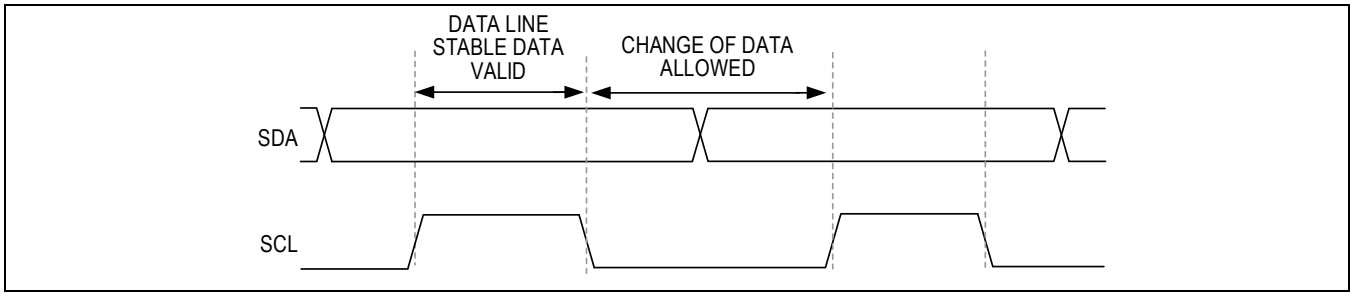


Figure 14. I²C Bit transfer

START and STOP Conditions

When the I²C serial interface is inactive, SDA and SCL are idle high. A controller initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA while SCL is high. A STOP condition is a low-to-high transition on SDA while SCL is high.

A START condition from the controller indicates the beginning of a transmission to the device. The controller terminates the transmission by issuing a NOT ACKNOWLEDGE followed by a STOP condition.

A STOP condition releases the bus. To issue a series of commands, the controller can issue repeated START (Sr) conditions instead of a STOP condition to maintain control of the bus. In general, a repeated START condition is functionally equivalent to a START condition.

When the device detects a STOP condition or an incorrect address, it disconnects SCL from the I²C serial interface internally until the next START condition, thereby minimizing digital noise and feedthrough.

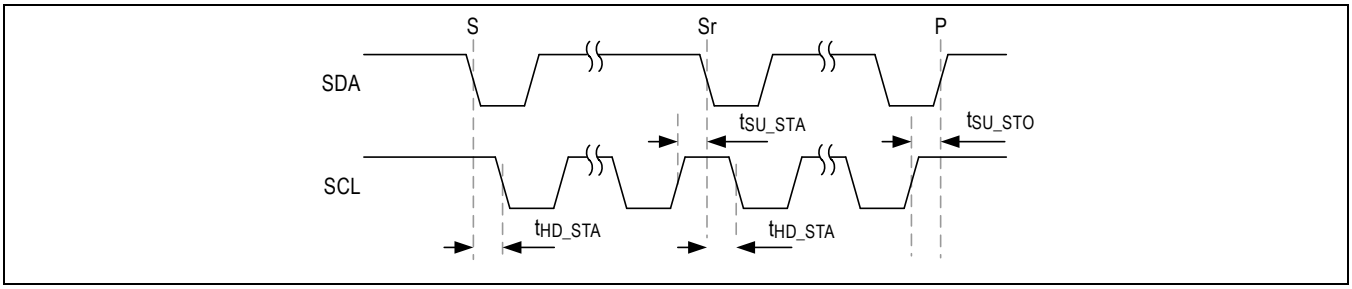


Figure 15. I²C start and stop

Acknowledge

Both the I²C bus controller and the target IC generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each 9-bit data packet. To generate an ACKNOWLEDGE (A), the receiving device pulls SDA low before the rising edge of the acknowledge-related clock pulse (the ninth pulse) and keeps it low during the high period of the clock pulse. To generate a NOT ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault occurs. In the event of an unsuccessful data transfer, the bus controller reattempts communication at a later time.

Target Address

The IC operates as an I²C target, both a transmitter and a receiver. The target address of the IC is 0x4A/0x4B, 0x4C/0x4D, or 0x4E/0x4F, depending on the SID pin configuration. The least significant bit indicates the read/write operation: 1 indicates read, and 0 indicates write.

Table 9. I²C Target Address

SID	TARGET ADDRESS (7-BIT)	TARGET ADDRESS (WRITE)	TARGET ADDRESS (READ)
GND	010 0101	0x4A (0100 1010)	0x4B (0100 1011)
Pull-up (470kΩ ±10%) to VIO	010 0110	0x4C (0100 1100)	0x4D (0100 1101)
Pull-down (470kΩ ±10%) to GND	010 0111	0x4E (0100 1110)	0x4F (0100 1111)

Clock Stretching

In general, the controller device generates the I²C bus clock signal. The I²C specification allows a slow target device to alter the clock signal by holding the clock line low. This process is commonly referred to as clock stretching. The IC does not use clock stretching to hold the clock line low.

General Call Address

The IC does not support the I²C general call address. If the IC detects the general call address (00000000b), it does not issue an ACKNOWLEDGE (A).

Communication Speed

The IC provides an I²C Revision 3.0-compatible serial interface that supports operation up to 1MHz.

- I²C revision 3 compatible serial communications channel
  - 0Hz to 100kHz (Standard Mode)
  - 0Hz to 400kHz (Fast Mode)
  - 0Hz to 1MHz (Fast-Mode Plus)
- Does not support I²C clock stretching

Operation in standard mode, fast mode, and fast-mode plus does not require any special protocol. The main consideration when varying the bus speed across this range is the interaction between bus capacitance and pull-up resistance. Higher time constants created by bus capacitance and pull-up resistance C x RC \times RC x R slow bus operation. Therefore, as bus speed increases, pull-up resistance decreases to maintain a reasonable time constant. Refer to the *Pull-up*

Resistor Sizing section of the I2C Revision 3.0 specification for guidance on pull-up resistor selection. In general, for a bus capacitance of 200pF, a 100kHz bus uses 5.6kΩ pull-up resistors, a 400kHz bus uses approximately 1.5kΩ pull-up resistors, and a 1MHz bus uses 680Ω pull-up resistors. Note that the pull-up resistor dissipates power when the open-drain bus is low. Lower pull-up resistance results in higher power dissipation V2/R.

Operation in high-speed mode requires special considerations. For a complete list of considerations, refer to the I2C Revision 3.0 specification. The major considerations for the IC are as follows:

- The I2C bus controller uses current-source pull-ups to shorten signal rise times.
- The I2C target uses a different set of input filters on SDA and SCL to accommodate the higher bus speed.
- The communication protocol uses the high-speed controller code.

At power-up and after each STOP condition, the IC input filters are set to standard, fast, or fast-plus mode, that is, 0Hz to 1MHz. To switch the input filters to high-speed mode, use the high-speed controller code protocol described in the *Communication Protocols* section.

Communication Protocols

The IC supports register read and write operations.

Writing to a Single Register

Figure 16 shows the protocol the I2C controller uses to write a single byte of data to the IC. This protocol is equivalent to the SMBus *Write Byte* protocol.

The *Write Byte* protocol is as follows:

1. The controller issues a START condition (S).
2. The controller sends the 7-bit target address followed by the write bit R/$\overline{W}$ = 0.
3. The addressed target issues an ACKNOWLEDGE (A) by pulling SDA low.
4. The controller sends an 8-bit register pointer.
5. The target acknowledges the register pointer.
6. The controller sends one data byte.
7. The target acknowledges the data byte. At the rising edge of SCL, the data byte loads into the addressed register and becomes active.
8. The controller issues a STOP condition (P) or a repeated START condition (Sr). Issuing P ensures that the bus input filters are set to 1MHz or slower. Issuing a repeated START condition (Sr) leaves the bus input filters in their current state.

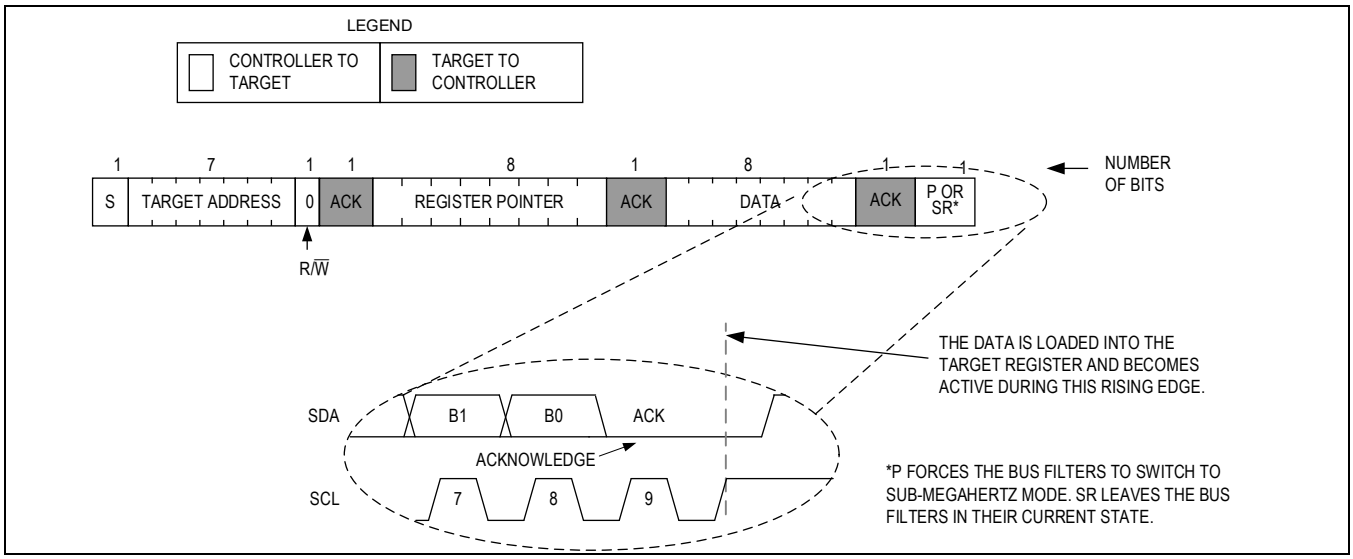


Figure 16. Writing to a single register

Writing to Sequential Registers

Figure 17 shows the protocol for writing to sequential registers. This protocol is similar to the *Write Byte* protocol, except that the controller continues to write after the first data byte. When the controller completes the write operation, it issues a STOP condition or a repeated START condition.

The *Writing to Sequential Registers* protocol is as follows:

1. The controller issues a START condition (S).
2. The controller sends the 7-bit target address followed by the write bit R/$\overline{W}$ = 0.
3. The addressed target issues an ACKNOWLEDGE (A) by pulling SDA low.
4. The controller sends an 8-bit register pointer.
5. The target acknowledges the register pointer.
6. The controller sends one data byte.
7. The target acknowledges the data byte. At the rising edge of SCL, the data byte loads into the addressed register and becomes active.
8. Steps 6 and 7 repeat as many times as required by the controller.
9. During the last acknowledge-related clock pulse, the target issues an ACKNOWLEDGE (A).
10. The controller issues a STOP condition (P) or a repeated START condition (Sr). Issuing P ensures that the bus input filters are set to 1MHz or slower. Issuing a repeated START condition (Sr) leaves the bus input filters in their current state.

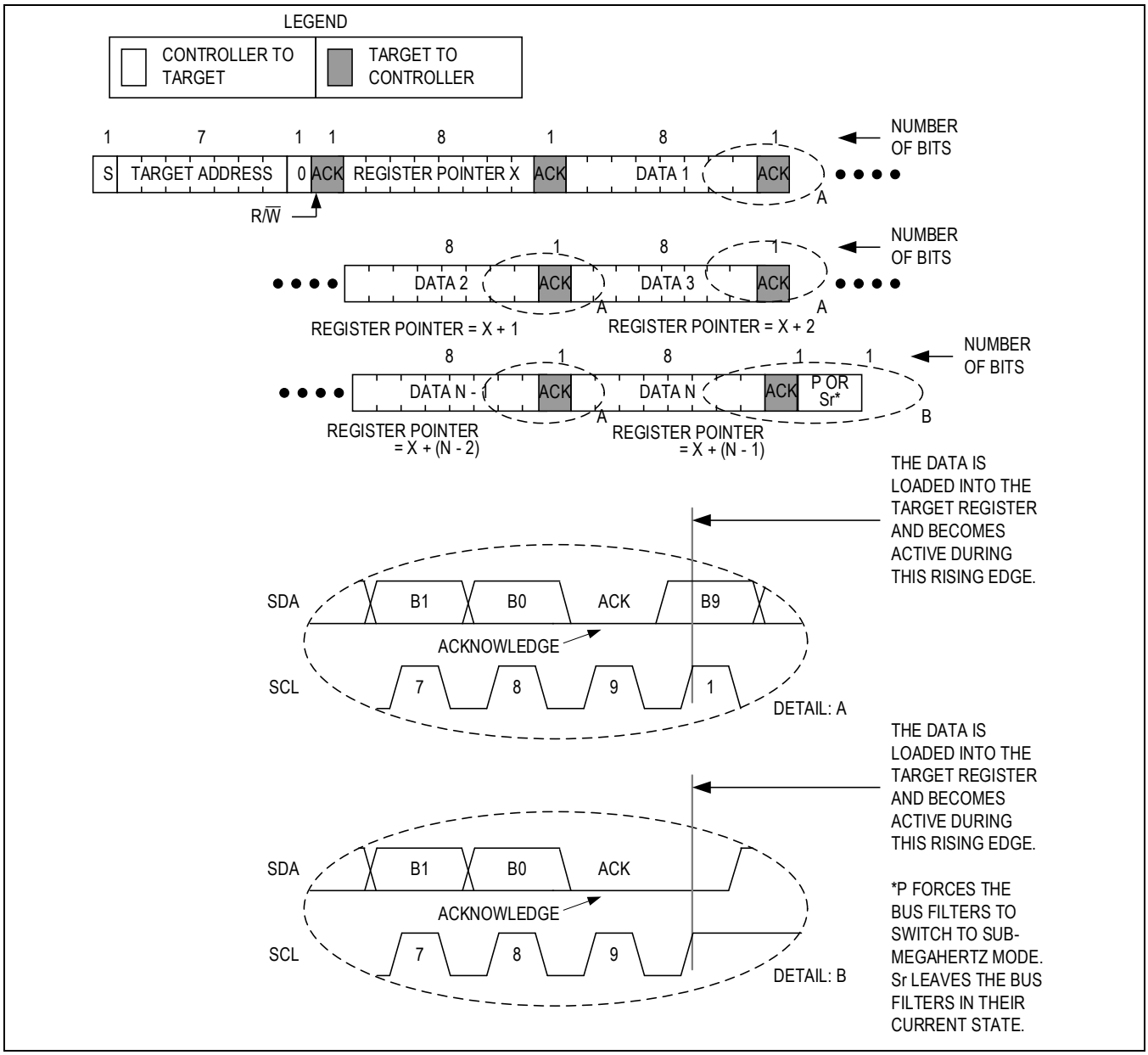


Figure 17. Writing to sequential registers

Reading from a Single Register

The I2C controller reads one byte of data from the IC. This protocol is equivalent to the SMBus *Read Byte* protocol.

The *Read Byte* protocol is as follows:

1. The controller issues a START condition (S).
2. The controller sends the 7-bit target address followed by the write bit R/$\overline{W}$ = 0.
3. The addressed target issues an ACKNOWLEDGE (A) by pulling SDA low.
4. The controller sends an 8-bit register pointer.
5. The target acknowledges the register pointer.
6. The controller issues a repeated START condition (Sr).
7. The controller sends the 7-bit target address followed by the read bit R/$\overline{W}$ = 1.
8. The addressed target issues an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed target places 8 bits of data on the bus from the location specified by the register pointer.

10. The controller issues a NOT ACKNOWLEDGE (nA).
11. The controller issues a STOP condition (P) or a repeated START condition (Sr). Issuing P ensures that the bus input filters are set to 1MHz or slower. Issuing a repeated START condition (Sr) leaves the bus input filters in their current state.

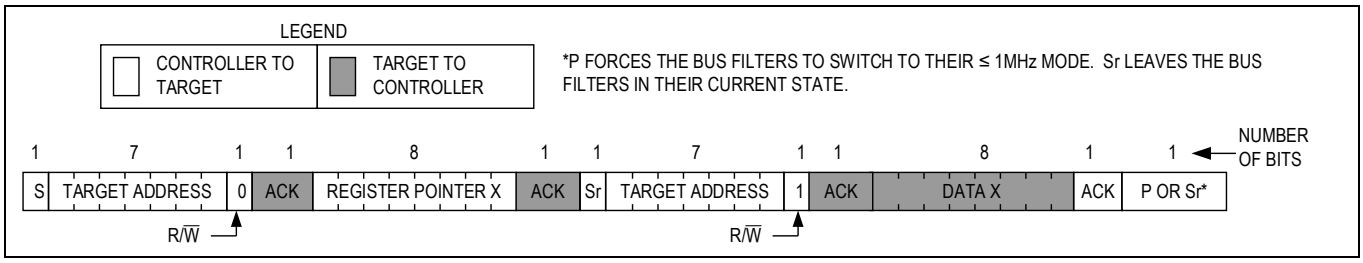


Figure 18. Reading from a single register

Reading from Sequential Registers

Figure 19 shows the protocol for reading from sequential registers. This protocol is similar to the *Read Byte* protocol, except that the controller issues an ACKNOWLEDGE (A) to indicate that it requires additional data. When the controller receives all required data, it issues a NOT ACKNOWLEDGE (nA) and a STOP condition (P) to terminate the transmission.

The *Continuous Read from Sequential Registers* protocol is as follows:

1. The controller issues a START condition (S).
2. The controller sends the 7-bit target address followed by the write bit R/$\overline{W}$ = 0.
3. The addressed target issues an ACKNOWLEDGE (A) by pulling SDA low.
4. The controller sends an 8-bit register pointer.
5. The target acknowledges the register pointer.
6. The controller issues a repeated START condition (Sr).
7. The controller sends the 7-bit target address followed by the read bit R/$\overline{W}$ = 1.
8. The addressed target issues an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed target places 8 bits of data on the bus from the location specified by the register pointer.
10. The controller issues an ACKNOWLEDGE (A) to indicate that it requires additional data.
11. Steps 9 and 10 repeat as many times as required by the controller. After the last data byte, the controller issues a NOT ACKNOWLEDGE (nA) to indicate that no additional data is required.
12. The controller issues a STOP condition (P) or a repeated START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set to 1MHz or slower. Issuing a repeated START condition (Sr) leaves the bus input filters in their current state.

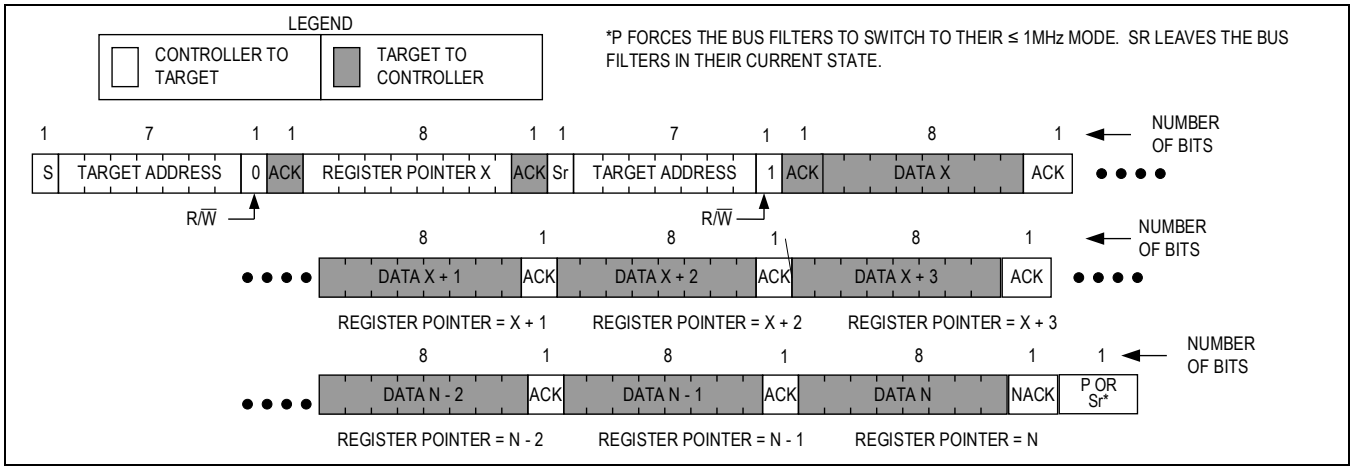


Figure 19. Reading from sequential registers

Engaging HS-Mode for Operation up to 3.4MHz

Figure 20 shows the protocol for engaging HS mode operation. HS mode supports bus operation at speeds up to 3.4MHz.

The *Engaging HS Mode* protocol is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The controller issues a START condition (S).
3. The controller sends the 8-bit controller code 0000 1xx0b, where xx represents don't-care bits.
4. The addressed target issues a NOT ACKNOWLEDGE (nA).
5. The controller can then increase the bus speed up to 3.4MHz and issue any read or write operation.

The controller can continue to issue high-speed read and write operations until it issues a STOP condition (P). Issuing a STOP condition (P) ensures that the bus input filters are set to 1MHz or slower.

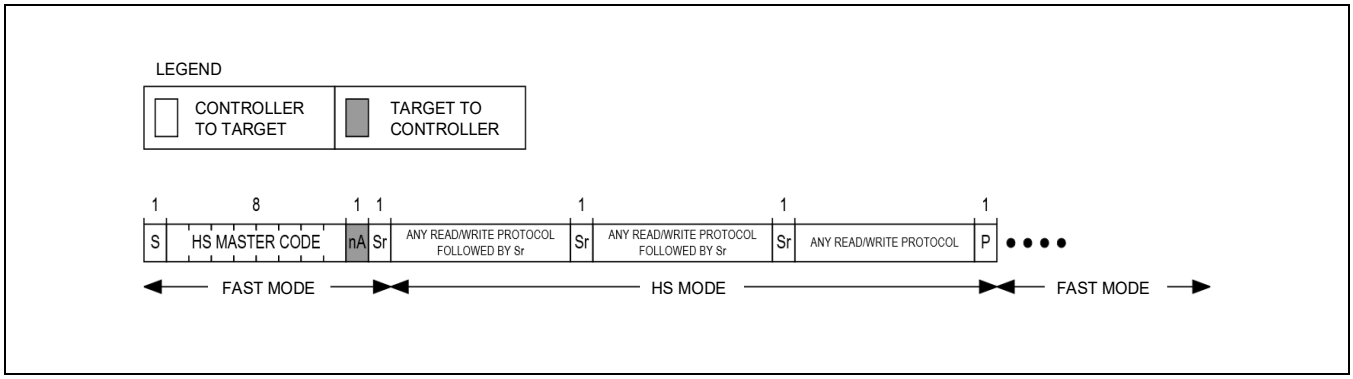


Figure 20. Engaging HS-mode

The MAX77978 I2C interface supports the HS mode extension feature. This feature maintains high-speed operation after a STOP condition. This capability eliminates the need for the I2C controller to issue the HS controller code while the HS controller remains in HS mode for multiple read or write cycles.

As shown in Figure 21 HS extension mode is enabled by setting the HS_EXT bit in the I2C_CFG register (Address 0x15) while operating in LS mode only. Entering HS extension mode from HS mode is not supported.

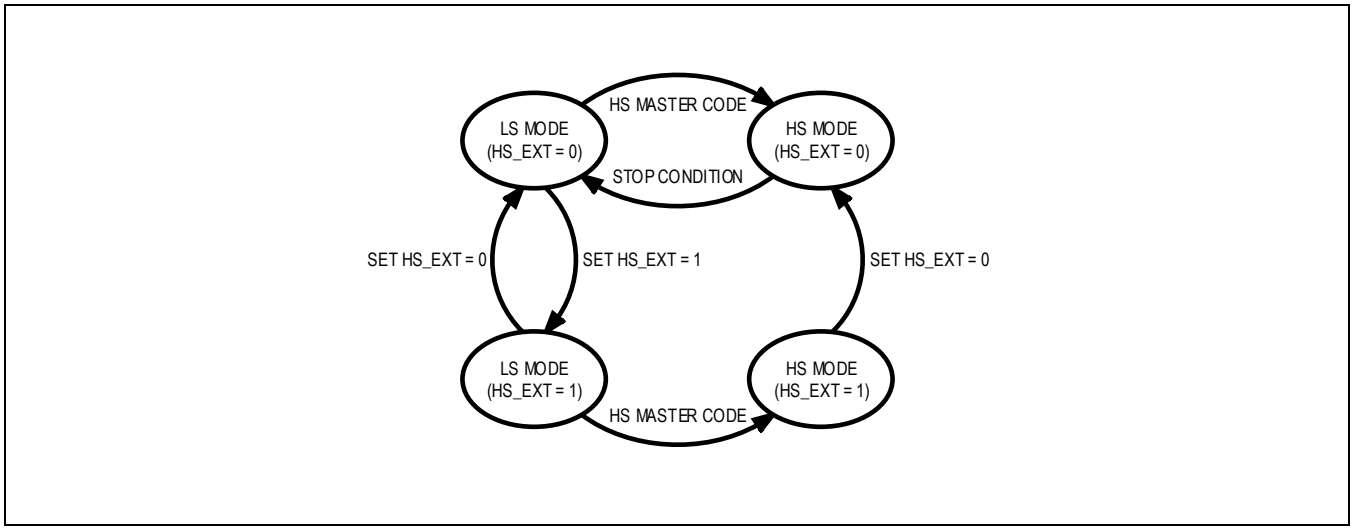


Figure 21. I2C Operating mode state diagram

Applications Information

Source Only Mode

The MAX77978 supports source-only mode for applications such as travel adapters. It complies with the USB Type-C and USB PD 3.2 specifications and supports both SPR and EPR PDOs.

In source mode, the device advertises its power capabilities through Source_Capabilities messages and controls the CC pins using configurable Rp current levels of 80µA, 150µA, and 330µA.

The MAX77978 manages Type-C attach and detach detection and monitors the CC pin status to maintain proper source operation.

V_{BUS} power is provided by an external power stage, which the MAX77978 controls through the GPIO or I^2C interface.

The device supports programmable configuration of operating mode, PDOs, and system behavior through its register interface.

Sink Only Mode

The MAX77978 operates in sink mode by monitoring the CC pins and initiating USB PD negotiation in response to Source_Capabilities messages from the connected power source. It generates a Request message based on the configured PDO preferences, enabling dynamic selection of voltage and current.

The sink role is established by asserting Rd on the CC pins. The device supports SPR operation and, depending on the system configuration, PPS and EPR modes.

The MAX77978 manages Type-C attach and detach detection and monitors CC pin status to maintain proper sink operation. PDO configuration and PD behavior are programmable through the device register interface.

HVDCP

The MAX77978 supports the high-voltage dedicated charging port (HVDCP) configuration, enabling compatibility with high-voltage adapters.

HVDCP operation is achieved by driving specific voltage levels on the D+/D− lines to request higher output voltages from the connected adapter. Based on the applied D+/D− signaling, the adapter adjusts the V_{BUS} level accordingly.

The device provides manual control of the D+/D− lines, allowing firmware to generate the required signaling patterns for HVDCP negotiation. The system monitors the resulting V_{BUS} level to confirm a successful voltage transition.

See *Table 6* for the supported D+/D− voltage combinations and corresponding adapter output voltages.

FW update

The firmware is updated through the AP, the MAX77978 GUI, or the MAX77978 dongle board.

1. **System application processor (AP):** At boot time, the AP compares the firmware version in the hex file with the version in the target device to determine whether an update is required. Issues related to RAM, data decryption, or MTP read/write operations can prevent Secure FW mode from proceeding.
2. **ADI dongle board:** The dongle board supports firmware update through the DP/DN interface. In this mode, the DP/DN lines are internally reconfigured and used as a communication interface for firmware upload.

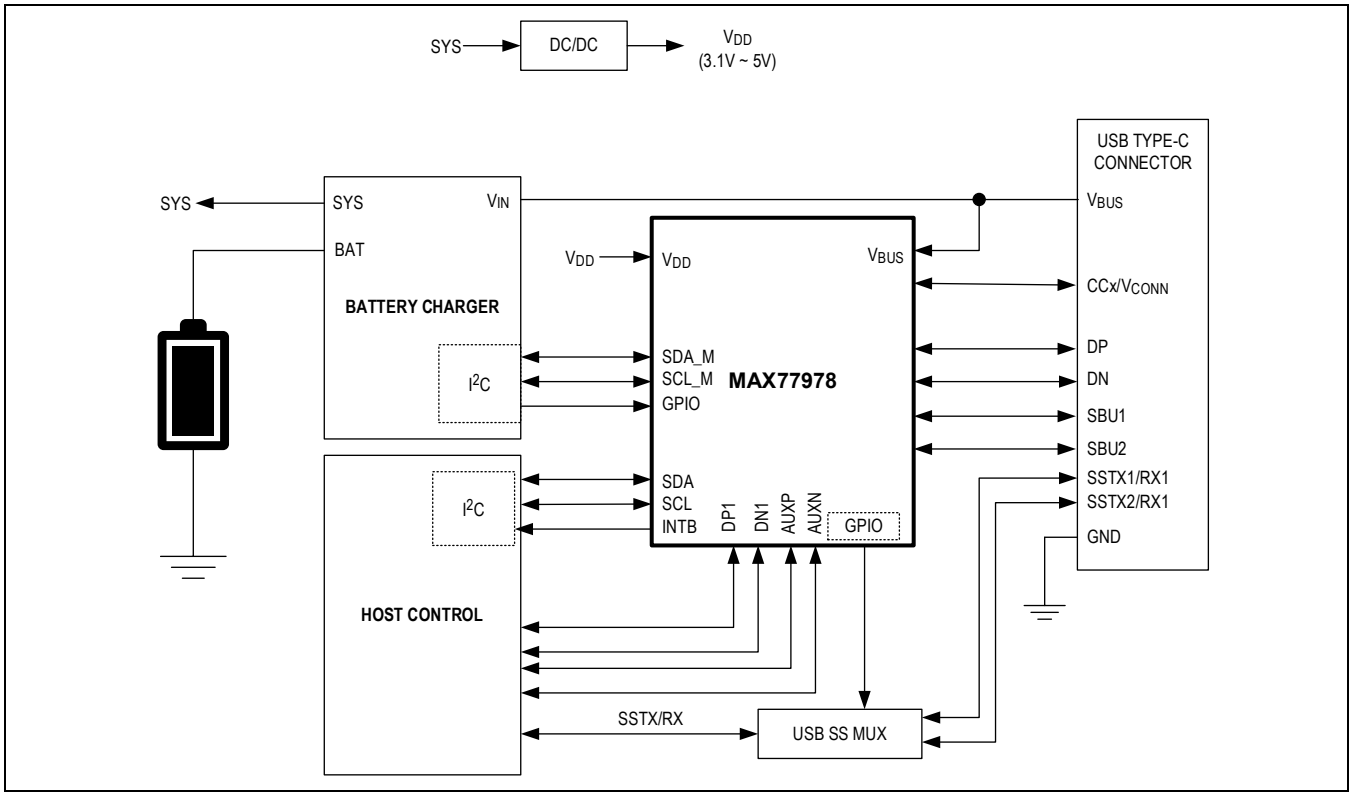
eUSB Set

The eUSB repeater and internal switch controls are typically configured through opcode commands such as EUSB_CTL and VENDOR_USBSW_CTRL. These commands enable repeater operation, control the D+/D− line states, and manage autoresume operation. These features help maintain signal integrity and minimize jitter across lossy eUSB channels. These configurations are particularly useful in embedded platforms with strict power and timing constraints, such as secure boot media and firmware hubs.

1. To issue the EUSB_CTL opcode command (0x7D/0x7E), set EUSB2_RPTR_EN to enable the eUSB2 repeater module and set AUTO_RESUME_EN to enable eUSB2 repeater autoresume operation.
2. To issue the VENDOR_USBSW_CTRL opcode command (0x67/0x68), enable the internal switch connections from DN to eDN and from DP to eDP.
3. Opcode commands with the EUSB_ prefix optimize compensation for eUSB channel loss profiles and improve jitter performance.

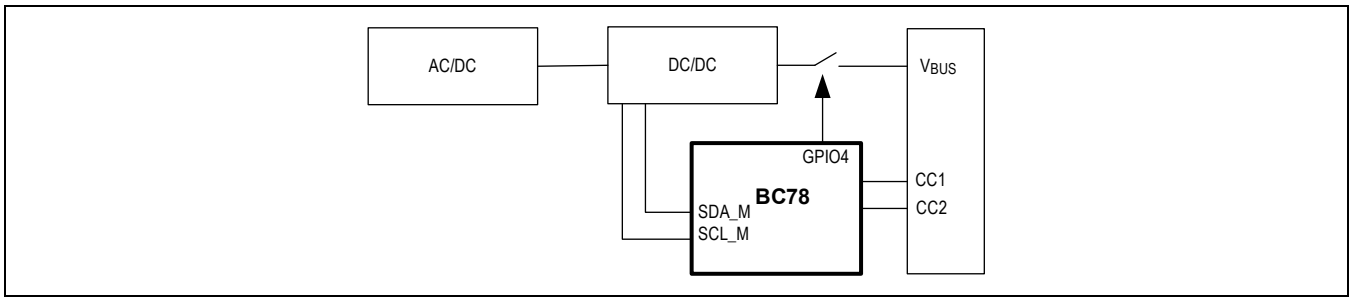
Typical Application Circuits

SINK Application

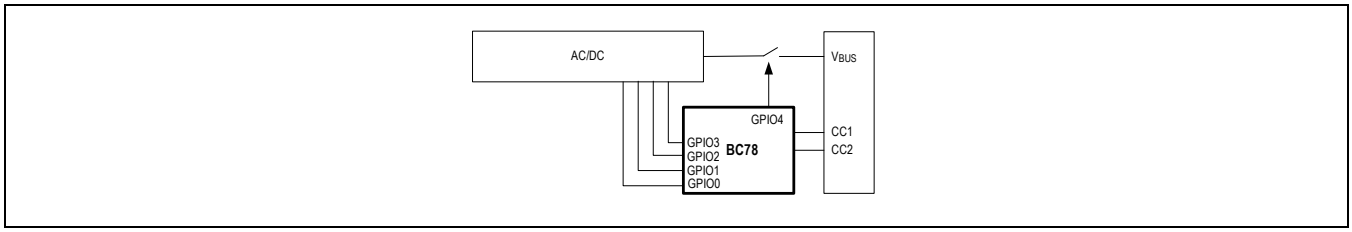


SOURCE Application

I2C Control



GPIO Control



Register Map

FUNC

I²C Target Address

The MAX77978 has a total of 3 target addresses. See Table 9 for more information.

Functional Reset Conditions

The IC has different levels of reset as follows:

- **Type S:** Registers are reset each time when VDD1P8 < VDD_OK_F
- **Type O:** Registers are reset each time when VDD1P8 < VDD_OK_F or when the software reset command is transmitted (SW_RESET = 0x0F)

Functional Register Reset Type Summary

	REGISTER ADDRESS (HEX)	REGISTER FUNCTION	REGISTER NAME	RESET TYPE
USBC SID (functional registers)				
USBC	0x00	USBC	DEVICE_ID	S
USBC	0x01	USBC	DEVICE_REV	S
USBC	0x02	USBC	FW_REV	S
USBC	0x03	USBC	FW_SUB_VER	S
USBC	0x04	USBC	UIC_INT	O
USBC	0x05	USBC	CC_INT	O
USBC	0x06	USBC	PD_INT	O
USBC	0x07	USBC	ACTION_INT	O
USBC	0x08	USBC	USBC_STATUS1	S
USBC	0x09	USBC	USBC_STATUS2	S
USBC	0x0A	USBC	BC_STATUS	S
USBC	0x0B	USBC	DP_STATUS	S
USBC	0x0C	USBC	CC_STATUS0	S
USBC	0x0D	USBC	CC_STATUS1	S
USBC	0x0E	USBC	PD_STATUS0	S
USBC	0x0F	USBC	PD_STATUS1	S

	REGISTER ADDRESS (HEX)	REGISTER FUNCTION	REGISTER NAME	RESET TYPE
USBC	0x10	USBC	UIC_INT_M	O
USBC	0x11	USBC	CC_INT_M	O
USBC	0x12	USBC	PD_INT_M	O
USBC	0x13	USBC	ACTION_INT_M	O
USBC	0x21	USBC	AP_DATAOUT0	O
USBC	0x22	USBC	AP_DATAOUT1	O
USBC	0x23	USBC	AP_DATAOUT2	O
USBC	0x24	USBC	AP_DATAOUT3	O
USBC	0x25	USBC	AP_DATAOUT4	O
USBC	0x26	USBC	AP_DATAOUT5	O
USBC	0x27	USBC	AP_DATAOUT6	O
USBC	0x28	USBC	AP_DATAOUT7	O
USBC	0x29	USBC	AP_DATAOUT8	O
USBC	0x2A	USBC	AP_DATAOUT9	O
USBC	0x2B	USBC	AP_DATAOUT10	O
USBC	0x2C	USBC	AP_DATAOUT11	O
USBC	0x2D	USBC	AP_DATAOUT12	O
USBC	0x2E	USBC	AP_DATAOUT13	O
USBC	0x2F	USBC	AP_DATAOUT14	O
USBC	0x30	USBC	AP_DATAOUT15	O
USBC	0x31	USBC	AP_DATAOUT16	O
USBC	0x32	USBC	AP_DATAOUT17	O
USBC	0x33	USBC	AP_DATAOUT18	O
USBC	0x34	USBC	AP_DATAOUT19	O
USBC	0x35	USBC	AP_DATAOUT20	O
USBC	0x36	USBC	AP_DATAOUT21	O

	REGISTER ADDRESS (HEX)	REGISTER FUNCTION	REGISTER NAME	RESET TYPE
USBC	0x37	USBC	AP_DATAOUT22	O
USBC	0x38	USBC	AP_DATAOUT23	O
USBC	0x39	USBC	AP_DATAOUT24	O
USBC	0x3A	USBC	AP_DATAOUT25	O
USBC	0x3B	USBC	AP_DATAOUT26	O
USBC	0x3C	USBC	AP_DATAOUT27	O
USBC	0x3D	USBC	AP_DATAOUT28	O
USBC	0x3E	USBC	AP_DATAOUT29	O
USBC	0x3F	USBC	AP_DATAOUT30	O
USBC	0x40	USBC	AP_DATAOUT31	O
USBC	0x41	USBC	AP_DATAOUT32	O
USBC	0x51	USBC	AP_DATAIN0	S
USBC	0x52	USBC	AP_DATAIN1	S
USBC	0x53	USBC	AP_DATAIN2	S
USBC	0x54	USBC	AP_DATAIN3	S
USBC	0x55	USBC	AP_DATAIN4	S
USBC	0x56	USBC	AP_DATAIN5	S
USBC	0x57	USBC	AP_DATAIN6	S
USBC	0x58	USBC	AP_DATAIN7	S
USBC	0x59	USBC	AP_DATAIN8	S
USBC	0x5A	USBC	AP_DATAIN9	S
USBC	0x5B	USBC	AP_DATAIN10	S
USBC	0x5C	USBC	AP_DATAIN11	S
USBC	0x5D	USBC	AP_DATAIN12	S
USBC	0x5E	USBC	AP_DATAIN13	S
USBC	0x5F	USBC	AP_DATAIN14	S

	REGISTER ADDRESS (HEX)	REGISTER FUNCTION	REGISTER NAME	RESET TYPE
USBC	0x60	USBC	AP_DATAIN15	S
USBC	0x61	USBC	AP_DATAIN16	S
USBC	0x62	USBC	AP_DATAIN17	S
USBC	0x63	USBC	AP_DATAIN18	S
USBC	0x64	USBC	AP_DATAIN19	S
USBC	0x65	USBC	AP_DATAIN20	S
USBC	0x66	USBC	AP_DATAIN21	S
USBC	0x67	USBC	AP_DATAIN22	S
USBC	0x68	USBC	AP_DATAIN23	S
USBC	0x69	USBC	AP_DATAIN24	S
USBC	0x6A	USBC	AP_DATAIN25	S
USBC	0x6B	USBC	AP_DATAIN26	S
USBC	0x6C	USBC	AP_DATAIN27	S
USBC	0x6D	USBC	AP_DATAIN28	S
USBC	0x6E	USBC	AP_DATAIN29	S
USBC	0x6F	USBC	AP_DATAIN30	S
USBC	0x70	USBC	AP_DATAIN31	S
USBC	0x71	USBC	AP_DATAIN32	S
USBC	0x80	USBC	SW_RESET	S

ADDRESS	NAME	MSB							LSB
USBC_FUNC									
0x00	DEVICE_ID[7:0]	DeviceId[7:0]							
0x01	DEVICE_REV[7:0]	DeviceRev[7:0]							
0x02	FW_REV[7:0]	FwRev[7:0]							
0x03	FW_SUB_VER[7:0]	FwSubRev[7:0]							

ADDRESS	NAME	MSB							LSB
0x04	UIC_INT[7:0]	APCmdResI	SYSMsgI	VBUSDetI	VbADCI	DCDTmoI	StopModeI	ChgTypI	AttachedHoldI
0x05	CC_INT[7:0]	VCONNOCPI	VSAFE0VI	–	WtrI	CCPinStatI	CCIStatI	CCVcnStatI	CCStatI
0x06	PD_INT[7:0]	PDMsgI	PSRDYI	DataRoleI	RSVD	RSVD	DisplayPortI	RSVD	RSVD
0x07	ACTION_INT[7:0]	Action7I	Action6I	Action5I	Action4I	Action3I	Action2I	Action1I	Action0I
0x09	USBC_STATUS2[7:0]	SYSMsg[7:0]							
0x0A	BC_STATUS[7:0]	VBUSDet	RSVD	PrChgTyp[2:0]			DCDTmo	ChgTyp[1:0]	
0x0B	DP_STATUS[7:0]	DP_ExitMode	DP_Attention	DP_Configure	DP_Status	DP_EnterMode	DP_DiscoverMode	DP_DiscoverSVID	DP_DiscoverIdentity
0x0C	CC_STATUS0[7:0]	CCPinStat[1:0]		CCIStat[1:0]		CCVcnStat	CCStat[2:0]		
0x0D	CC_STATUS1[7:0]	RSVD	RSVD	VCONN_OCP	–	Vsafte0V	–	Wtr	RSVD
0x0E	PD_STATUS0[7:0]	PDMsg[7:0]							
0x0F	PD_STATUS1[7:0]	DataRole	PowerRole	–	PSRDY	–	–	–	–
0x10	UIC_INT_M[7:0]	APCmdResM	SYSMsgM	VBUSDetM	VbADCM	DCDTmoM	StopModeM	ChgTypM	AttachedHoldM
0x11	CC_INT_M[7:0]	VCONNOCPM	VSAFE0VM	–	WtrM	CCPinStatM	CCIStatM	CCVcnStatM	CCStatM
0x12	PD_INT_M[7:0]	PDMsgM	PSRDYM	DataRoleM	RSVD	RSVD	DisplayPortM	RSVD	RSVD
0x13	ACTION_INT_M[7:0]	Action7M	Action6M	Action5M	Action4M	Action3M	Action2M	Action1M	Action0M
0x14	VBUS_VOLTAGE_L[7:0]	VBUS_VOLTAGE7_0[7:0]							
0x15	VBUS_VOLTAGE_H[7:0]	RSVD[4:0]					VBUS_VOLTAGE10_8[2:0]		
TOP_FUNC									

Register Details

DEVICE_ID (0x0)

BIT	7	6	5	4	3	2	1	0
Field	DeviceId[7:0]							
Reset	0x78							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DeviceId	7:0	Device ID

DEVICE_REV (0x1)

BIT	7	6	5	4	3	2	1	0
Field	DeviceRev[7:0]							
Reset	0x01							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DeviceRev	7:0	Device Revision

FW_REV (0x2)

BIT	7	6	5	4	3	2	1	0
Field	FwRev[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FwRev	7:0	FW Revision

FW_SUB_VER (0x3)

BIT	7	6	5	4	3	2	1	0
Field	FwSubRev[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FwSubRev	7:0	FW Revision

UIC_INT (0x4)

BIT	7	6	5	4	3	2	1	0
Field	APCmdResI	SYSMsgI	VBUSDetI	VbADCI	DCDTmoI	StopModeI	ChgTypI	AttachedHoldI
Reset	0x0	0x0	0x0	0x0	0x0	0b0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
APCmdResI	7	AP Command Response Interrupt	0x0: No interrupt. 0x1: AP command response pending.
SYSMsgI	6	USBC System Message Interrupt	0x0: No interrupt. 0x1: USBC system message pending.
VBUSDetI	5	V_{BUS} Detection Interrupt	0x0: No interrupt. 0x1: New V_{BUSDet} status interrupt.
VbADCI	4	V_{BUS} Voltage ADC Interrupt	0x0: No interrupt. 0x1: New VbADC status interrupt.
DCDTmoI	3	DCD Timer Interrupt	0x0: No interrupt. 0x1: New DCDTmo status interrupt.
StopModeI	2	Stop Mode Interrupt	0x0: No interrupt. 0x1: New stop mode status interrupt.
ChgTypI	1	Charger Type Interrupt	0x0: No interrupt. 0x1: New ChgTyp status interrupt.
AttachedHoldI	0	Attached Hold Interrupt	0x0: No interrupt. 0x1: New attached hold status interrupt.

CC_INT (0x5)

BIT	7	6	5	4	3	2	1	0
Field	VCONNOCPI	VSAFE0VI	–	WtrI	CCPinStatI	CCIStatI	CCVcnStatI	CCStatI
Reset	0x0	0x0	–	0x0	0x0	0x0	0x0	0x0

Access Type	Read Clears All	Read Clears All	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
VCONNOCPI	7	V_{CONN} OCP Interrupt	0x0: No interrupt. 0x1: New V_{CONN}OCP status interrupt.
VSAFE0VI	6	VSAFE0V Interrupt	0x0: No interrupt. 0x1: New VSAFE0V status interrupt.
WtrI	4	Moisture/Dry Interrupt	0x0: No interrupt. 0x1: New moisture/dry status interrupt.
CCPinStatI	3	CC Pin State Interrupt	0x0: No interrupt. 0x1: New CCPinStat status interrupt.
CCIStatI	2	CCIStat Interrupt	0x0: No interrupt. 0x1: New CCIStat status interrupt.
CCVcnStatI	1	CCVcnStat Interrupt	0x0: No interrupt. 0x1: New CCVcnStat status interrupt.
CCStatI	0	CCStat Interrupt	0x0: No interrupt. 0x1: New CCStat status interrupt.

PD_INT (0x6)

BIT	7	6	5	4	3	2	1	0
Field	PDMsgI	PSRDYI	DataRoleI	RSVD	RSVD	DisplayPortI	RSVD	RSVD
Reset								
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
PDMsgI	7	PD Message Interrupt	0x0: No Interrupt 0x1: New PD message Issued
PSRDYI	6	PSRDY Message Interrupt	0x0: No Interrupt 0x1: New PDRDY message Issued
DataRoleI	5	Data Role Interrupt	0x0: No Interrupt 0x1: DataRole status is changed
RSVD	4	Reserved	
RSVD	3	Reserved	
DisplayPortI	2	DisplayPort Status Update Interrupt	0x0: No Interrupt 0x1: New DisplayPort Status Update Interrupt
RSVD	1	Reserved	
RSVD	0	Reserved	

ACTION_INT (0x7)

BIT	7	6	5	4	3	2	1	0

Field	Action7I	Action6I	Action5I	Action4I	Action3I	Action2I	Action1I	Action0I
Reset				0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
Action7I	7	Action Table Interrupt 7	0x0: No Interrupt 0x1: Action table set interrupt 7.
Action6I	6	Action Table Interrupt 6	0x0: No Interrupt 0x1: Action table set interrupt 6.
Action5I	5	Action Table Interrupt 5	0x0: No Interrupt 0x1: Action table set interrupt 5.
Action4I	4	Action Table Interrupt 4	0x0: No interrupt 0x1: Action table set interrupt 4.
Action3I	3	Action Table Interrupt 3	0x0: No interrupt. 0x1: Action table set interrupt 3.
Action2I	2	Action Table Interrupt 2	0x0: No interrupt. 0x1: Action table set interrupt 2.
Action1I	1	Action Table Interrupt 1	0x0: No interrupt 0x1: Action table set interrupt 1.
Action0I	0	Action Table Interrupt 0	0x0: No interrupt. 0x1: Action table set interrupt 0.

USBC_STATUS2 (0x9)

BIT	7	6	5	4	3	2	1	0
Field	SYSMsg[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
SYSMsg	7:0	SYSMsg	0x03: MA_SYSERROR_BOOT_WDT 0x05: MA_SYS_BOOT 0x06: MA_SYS_EUSB_IRQ 0x31: MA_SYSERROR_APCMD_UNKNOWN 0x32: MA_SYSERROR_APCMD_INPROGRESS 0x33: MA_SYSERROR_APCMD_FAIL 0x60: MA_SYS_DP_5V_SHORT 0x61: MA_SYS_DN_5V_SHORT 0x62: MA_SYS_SBU1_5V_SHORT 0x63: MA_SYS_SBU2_5V_SHORT 0x65: MA_SYS_CC1_5V_SHORT 0x66: MA_SYS_CC2_5V_SHORT 0x80: MA_SYSERROR_USER_PD_COLLISION 0xC0: MA_SYS_MTP_WRITEFAIL 0xC1: MA_SYS_MTP_READFAIL 0xC2: MA_SYS_MTP_ERASEFAIL 0xC3: MA_SYS_MTP_CUSTOMINFONOTSET 0xC4: MA_SYS_MTP_OVERACTIONBLKSIZE 0xDB: MA_SYSERROR_OPCODE_TIMEXP 0xE0: MA_SYSERROR_FIRMWAREERROR

BITFIELD	BITS	DESCRIPTION	DECODE
			0xEA: MA_SYS_EXECUTE_I2C_WRITEBURST_FAIL 0xEB: MA_SYS_EXECUTE_I2C_READBURST_FAIL 0xEC: MA_SYS_EXECUTE_I2C_READ_FAIL 0xED: MA_SYS_EXECUTE_I2C_WRITE_FAIL 0xEF: MA_SYS_EXECUTE_I2C_FAULT

BC_STATUS (0xA)

BIT	7	6	5	4	3	2	1	0
Field	VBUSDet	RSVD	PrChgTyp[2:0]			DCDTmo	ChgTyp[1:0]	
Reset	0x0	0b0	0x000			0x0	0x00	
Access Type	Read Only	Read Only	Read Only			Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
VBUSDet	7	VBUS Detected	0x0: VBUS < V_VBDET 0x1: VBUS > V_VBDET
RSVD	6	Reserved	
PrChgTyp	5:3	Output of Charger Detection, combined with PrChgTyp, determines which charger is detected	0x0: Unknown 0x1: Samsung 2A 0x2: Apple 500mA 0x3: Apple 1A 0x4: Apple 2A 0x5: Apple 12W
DCDTmo	2	During Charger Detection, DCD Detection Timed Out. Indicates D+/D- are open. BC1.2 detection continues as required by BC1.2 specification but SDP most likely is found.	0x0: No timeout or detection has not run. 0x1: DCD timeout occurred.
ChgTyp	1:0	Output of Charger Detection, combined with PrChgTyp, determines which charger is detected	0x0: Nothing attached 0x1: SDP 0x2: CDP 0x3: DCP

DP_STATUS (0xB)

BIT	7	6	5	4	3	2	1	0
Field	DP_ExitMode	DP_Attention	DP_Configure	DP_Status	DP_EnterMode	DP_DiscoverMode	DP_DiscoverSVID	DP_DiscoverIdentity
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DP_ExitMode	7	Display Port Exit Mode	0x0: No interrupt. 0x1: DisplayPort Exit mode message.
DP_Attention	6	Display port Attention Message	0x0: No interrupt. 0x1: DisplayPort Attention message.
DP_Configure	5	Display port Configure message	0x0: No interrupt. 0x1: DisplayPort Configure message.
DP_Status	4	Display Port Status message	0x0: No interrupt. 0x1: DisplayPort Status message.
DP_EnterMode	3	Display Port Enter Mode	0x0: No interrupt 0x1: DisplayPort Enter mode message.
DP_DiscoverMode	2	Display Port Discover Mode	0x0: No interrupt 0x1: DisplayPort Discover mode message.
DP_DiscoverSVID	1	Display Port Discover SVID	0x0: No interrupt 0x1: DisplayPort Discover SVID message.
DP_DiscoverIdentity	0	Display Port Discover Identity	0x0: No interrupt 0x1: DisplayPort Discover identity message.

CC_STATUS0 (0xC)

BIT	7	6	5	4	3	2	1	0
Field	CCPinStat[1:0]		CCIStat[1:0]		CCVcnStat	CCStat[2:0]		
Reset	0b00		0b00		0b0	0b000		
Access Type	Read Only		Read Only		Read Only	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
CCPinStat	7:6	Output of Active CC Pin	0b00: No determination 0b01: CC1 Active 0b10: CC2 Active 0b11: RFU
CCIStat	5:4	CC Pin Detected and Allows V_{BUS} Current in UFP Mode	0b00: Not in UFP mode 0b01: 500mA 0b10: 1.5A 0b11: 3.0A
CCVcnStat	3	Status of V_{CONN} Output	0b0: V_{CONN} disabled 0b1: V_{CONN} enabled
CCStat	2:0	CC Pin State Machine Detection	0b000: No connection 0b001: SINK 0b010: SOURCE 0b011: Liquid corrosion mitigation mode 0b100: DebugSrc accessory 0b101: Error 0b110: Disabled 0b111: DebugSnk accessory

CC_STATUS1 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	VCONN_OCP	–	Vsafte0V	–	Wtr	RSVD

Reset	0b0	0b0		–		–		0b0
Access Type	Read Only	Read Only	Read Only	–	Read Only	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved	
RSVD	6	Reserved	
VCONN_OCP	5	VCONN Overcurrent Detection	0x0: VCONN current < VCONN_ILIM 0x1: VCONN current > VCONN_ILIM
Vsafte0V	3	Status of VBUS detection. Valid only in Attached.SRC_CCx, Attached.SNK_CCx status	0x0: VBUS < VSAFE0V 0x1: VBUUS > VSAFE0V
Wtr	1	Moisture/Dry Status	0x0: Dry 0x1: Moisture
RSVD	0	Reserved.	

PD_STATUS0 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	PDMsg[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PDMsg	7:0	PD Message	0x00: Nothing happened 0x01: Sink_PD_PSRdy_Received 0x02: Sink_PD_Error_Recovery 0x03: Sink_PD_SenderResponseTimer_Timeout 0x04: Source_PSRdy_Sent 0x05: Source_PD_Error_Recovery 0x06: Source_PD_SenderResponseTimer_Timeout 0x07: PD_DR_Swap_Request_Received 0x08: PD_PR_Swap_Request_Received 0x09: PD_V_{CONN}_Swap_Request_Received 0X11: VDM Attention_Message_Received 0x0A: Received PD Message in illegal state 0x0B: Sink_PD_Evaluate_State, SrcCap_Received 0x11: VDM Attention Message Received 0x12: Reject_Received 0x13: Not_Supported_Received 0x14: PD_PR_Swap_SNKTOSRC_Cleanup 0x15: PD_PR_Swap_SRCTOSNK_Cleanup 0x16: HardReset_Received 0x17: PD_PowerSupply_VbusEnable 0x18: PD_PowerSupply_VbusDisable 0x19: HardReset_Sent 0x1A: PD_PR_Swap_SRCTOSWAP 0x1B: PD_PR_Swap_SWAPTOSNK 0x1C: PD_PR_Swap_SNKTOSWAP 0x1D: PD_PR_Swap_SWAPTOSRC 0x20: Sink_PD_Disabled 0x21: Source_PD_Disabled

BITFIELD	BITS	DESCRIPTION	DECODE
			0x30: Get_Source_Capabilities_Extended_Received 0x31: Get_Status_Received 0x32: Get_Battery_Cap_Received 0x33: Get_Battery_Status_Received 0x34: Get_Manufacturer_Info_Received 0x35: Source_Capabilities_Extended_Received 0x36: Status_Received 0x37: Battery_Capabilities_Received 0x38: Battery_Status_Received 0x39: Manufacturer_Info_Received 0x3A: Security_Request_Received 0x3B: Security_Response_Received 0x3C: Firmware_Update_Request_Received 0x3D: Firmware_Update_Response_Received 0x3E: Alert_Received 0x40: VDM_NAK_Received 0x41: VDM_BUSY_Received 0x42: VDM_ACK_Received 0x43: VDM_REQ_Received 0x63: DiscoverMode_Received 0x65: PD_Status_Received

PD_STATUS1 (0xF)

BIT	7	6	5	4	3	2	1	0
Field	DataRole	PowerRole	–	PSRDY	–	–	–	–
Reset	0x0	0x0	–	0x0	–	–	–	–
Access Type	Read Only	Read Only	–	Read Only	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DataRole	7	Current Data Role	0x0: UFP 0x1: DFP
PowerRole	6	Power Role	0x0: Sink 0x1: Source
PSRDY	4	PSRDY Received as Sink	0x0: Nothing happened 0x1: PSRDY received

UIC_INT_M (0x10)

BIT	7	6	5	4	3	2	1	0
Field	APCmdResM	SYSMsgM	VBUSDetM	VbADCM	DCDTmoM	StopModeM	ChgTypM	AttachedHoldM
Reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
APCmdResM	7	APCmdRes Interrupt Mask	0x0: Unmask 0x1: Mask

BITFIELD	BITS	DESCRIPTION	DECODE
SYSMsgM	6	SYSMsg Interrupt Mask	0x0: Unmask 0x1: Mask
VBUSDetM	5	VBUSDet Interrupt Mask	0x0: Unmask 0x1: Mask
VbADCM	4	VbADC Interrupt Mask	0x0: Unmask 0x1: Mask
DCDTmoM	3	DCDTmo Interrupt Mask	0x0: Unmask 0x1: Mask
StopModeM	2	Fake V_{BUS} Interrupt Mask	0x0: Unmask 0x1: Mask
ChgTypM	1	ChgTyp Interrupt Mask	0x0: Unmask 0x1: Mask
AttachedHoldM	0	UIDADC Interrupt Mask	0x0: Unmask 0x1: Mask

CC_INT_M (0x11)

BIT	7	6	5	4	3	2	1	0
Field	VCONNOCPM	VSAFE0VM	–	WtrM	CCPinStatM	CCIStatM	CCVcnStatM	CCStatM
Reset	0x1	0x1	–	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VCONNOCPM	7	VCONNOCP Interrupt Mask	0x0: Unmask 0x1: Mask
VSAFE0VM	6	VSAFE0V Interrupt Mask	0x0: Unmask 0x1: Mask
WtrM	4	Wtr Interrupt Mask	0x0: Unmask 0x1: Mask
CCPinStatM	3	CCPinStat Interrupt Mask	0x0: Unmask 0x1: Mask
CCIStatM	2	CCIStat Interrupt Mask	0x0: Unmask 0x1: Mask
CCVcnStatM	1	CCVcnStat Interrupt Mask	0x0: Unmask 0x1: Mask
CCStatM	0	CCStat Interrupt Mask	0x0: Unmask 0x1: Mask

PD_INT_M (0x12)

BIT	7	6	5	4	3	2	1	0
Field	PDMsgM	PSRDYM	DataRoleM	RSVD	RSVD	DisplayPortM	RSVD	RSVD
Reset	0x1	0x1	0x1	0b1	0b1	0x1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PDMsgM	7	PD Message Interrupt mask	0x0: Unmask 0x1: Mask
PSRDYM	6	PSRDY Message Interrupt Mask	0x0: Unmask 0x1: Mask
DataRoleM	5	Data Role Interrupt Mask	0x0: Unmask 0x1: Mask
RSVD	4	Reserved	
RSVD	3	Reserved	
DisplayPortM	2	DisplayPort Status Update Interrupt Mask	0x0: Unmask 0x1: Mask
RSVD	1	Reserved	
RSVD	0	Reserved	

ACTION_INT_M (0x13)

BIT	7	6	5	4	3	2	1	0
Field	Action7M	Action6M	Action5M	Action4M	Action3M	Action2M	Action1M	Action0M
Reset				0xF	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Action7M	7	Action Table Interrupt 7 Mask	0x0: Unmask 0x1: Mask
Action6M	6	Action Table Interrupt 6 Mask	0x0: Unmask 0x1: Mask
Action5M	5	Action Table Interrupt 5 Mask	0x0: Unmask 0x1: Mask
Action4M	4	Action Table Interrupt 4 Mask	0x0: Unmask 0x1: Mask
Action3M	3	Action Table Interrupt 3 Mask	0x0: Unmask 0x1: Mask
Action2M	2	Action Table Interrupt 2 Mask	0x0: Unmask 0x1: Mask
Action1M	1	Action Table Interrupt 1 Mask	0x0: Unmask 0x1: Mask
Action0M	0	Action Table Interrupt 0 Mask	0b0: Unmask 0b1: Mask

VBUS_VOLTAGE_L (0x14)

BIT	7	6	5	4	3	2	1	0
Field	VBUS_VOLTAGE7_0[7:0]							
Reset								

Access Type	Read Only

BITFIELD	BITS	DESCRIPTION
VBUS_VOLTAGE7_0	7:0	VBUS Voltage Low bits [7:0]. The LSB is 0.025 V.

VBUS_VOLTAGE_H (0x15)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[4:0]					VBUS_VOLTAGE10_8[2:0]		
Reset								
Access Type	Read Only					Read Only		

BITFIELD	BITS	DESCRIPTION
RSVD	7:3	Reserved
VBUS_VOLTAGE10_8	2:0	VBUS Voltage High bits[2:0]. The LSB is 0.025 V.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	FW VERSION	DP/DN SWITCH SETTING
MAX77978EWX+T	-40°C to +85°C	6x6 WLP, 0.5mm pitch, 3.41mm x 3.41mm	02.1E	SDP/CDP: Close
				DCP: Open
MAX77978EWX+	-40°C to +85°C	6x6 WLP, 0.5mm pitch, 3.41mm x 3.41mm	02.1E	SDP/CDP: Close
				DCP: Open

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/26	Release for Market Intro	—