MAX77928

10A 3:1/2:1/1:1 Switched-Capacitor Direct Charger for 1S Li-Ion Battery

General Description

The MAX77928 is a 10A bi-directional 3:1/2:1/1:1 switched-capacitor converter (SCC) Direct Charger for a 1S Li-ion battery.

For 1S charging configurations, the device can operate in forward mode as a step-down switched-capacitor converter with a 3:1 or 2:1 input-voltage-to-output-voltage conversion ratio. For OTG power configurations, it can operate in reverse mode as a step-up converter with a 1:3 or 1:2 voltage conversion ratio. For both directions, bypass mode (1:1 conversion ratio) is supported. These modes are I^2C configurable.

The device integrates 2-channel gate drivers to drive external MOSFET(s) or GaN FET(s) for overvoltage protection or input selection.

The device can regulate the output voltage and input current. The regulation targets for these are I^2C programmable.

The device has various protection features such as input undervoltage lockout, input overvoltage lockout, output undervoltage lockout, output overvoltage lockout, overcurrent protection, flying capacitor short/open detection, reverse current protection, thermal regulation, alarm and shutdown, and watchdog timer.

The device has a 12-bit ADC that can measure VIN voltage, PMID voltage, VEXT1 voltage, VEXT2 voltage, input current, output voltage, battery differential voltage, thermistor voltage, and die temperature.

The device has an I^2C interface that supports 1.8V rail and 1.2V rail without a VIO pin, with an SCL clock rate of up to 1.0MHz. Programmable options are provided for flexible application use cases.

The MAX77928 is available in a 0.4mm pitch, 4.568mm x 3.368mm, 88-bump (11 x 8) wafer-level package (WLP).

Applications

- Smartphones
- Tablets
- Single Cell Li-Ion Charger
- Portable Devices

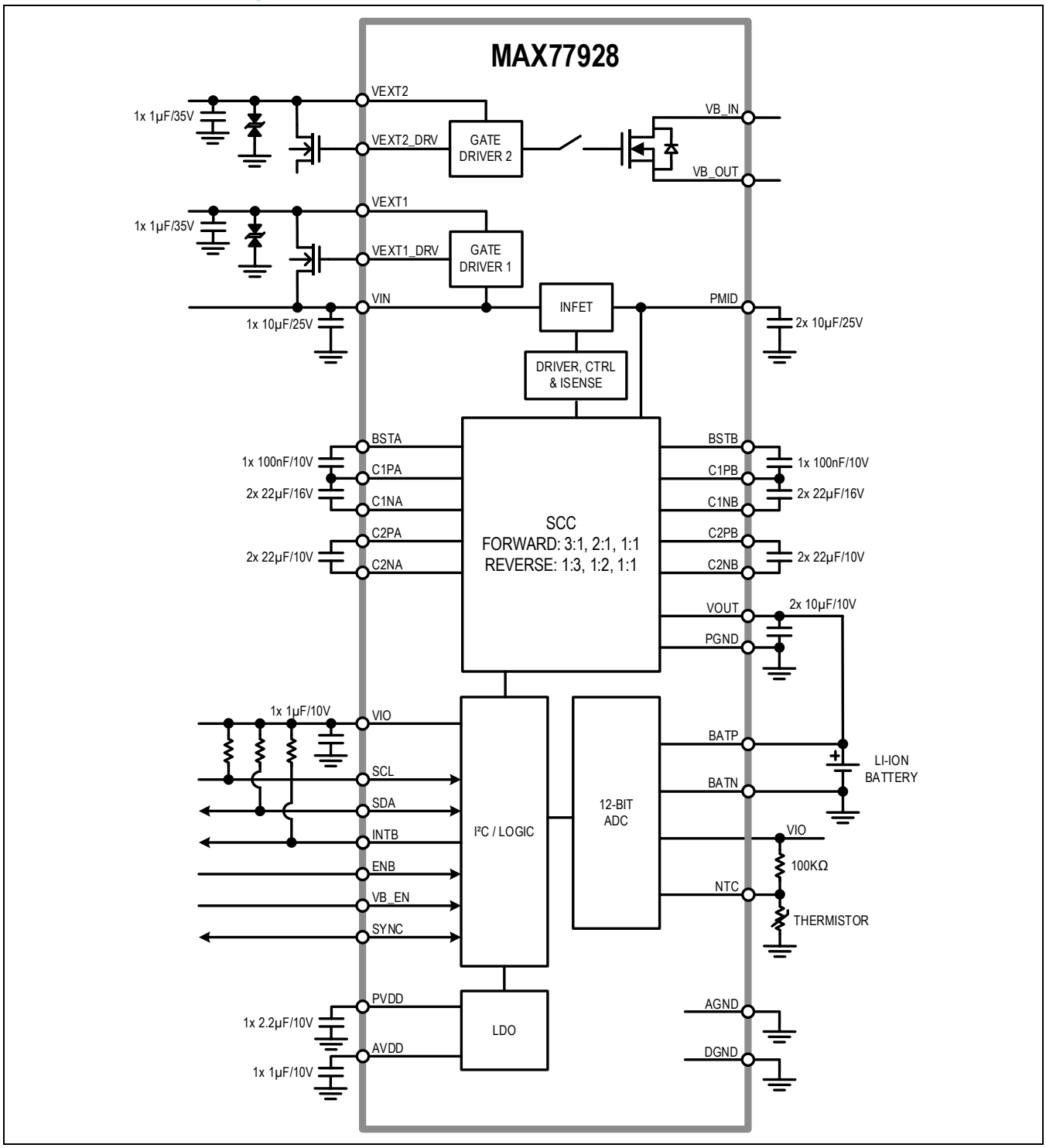
Benefits and Features

- 10A Bi-Directional Switched-Capacitor Converter
  - Integrated Power Switches
  - Dual-Phase Configuration, 180-Degree Interleaved
  - 2.5V to 16.9V Input Operating Range
  - 3:1/2:1/1:1 from VIN to VOUT for Battery Charging
  - 1:3/1:2/1:1 from VOUT to VIN for OTG Mode
  - 96.2% Efficiency at 4.4V, 9A Output with 3:1 Ratio and Total 8 x 22µF 0603 C_{FLY}
  - Programmable Switching Frequency from 200kHz to 1.5MHz
- 2-Channel Gate Drivers to Drive External MOSFET(s) or GaN FET(s) for OVP or Input Selection
- Integrated VB FET with 24V AMR and 40mΩ Switch
- Regulations
  - Input Current Regulation
  - Battery Voltage Regulation
  - Thermal Regulation
- 12-Bit ADC
  - VIN/PMID/VEXT1/VEXT2/VOUT/Battery Differential Voltage Measurement
  - Input Current Measurement
  - External Thermistor Voltage Measurement
  - Die Temperature Measurement
- Protections
  - VIN/VOUT/VEXT1/VEXT2 UVLO and OVLO
  - Overcurrent Protection for Both Directions
  - Flying Capacitor Short/Open Protection
  - Battery (BATP – BATN) OVLO
  - Output-to-Input Reverse Current Protection
  - NTC Overtemperature Shutdown
  - Die Temperature Alarms and Thermal Shutdown
  - Watchdog Timer
  - BST UVLO and PVDD UVLO
- Frequency Dithering
- Skip Mode and Audio Mode
- Chip Enable Input and VB FET Auto Mode Enable
- Frequency Synchronization for Parallel Operation
- I^2C Interface
- 0.4mm Pitch, 11 x 8 WLP Package

***Ordering Information* appears at end of data sheet.**

19-102048; Rev 0; 10/25

Simplified Block Diagram



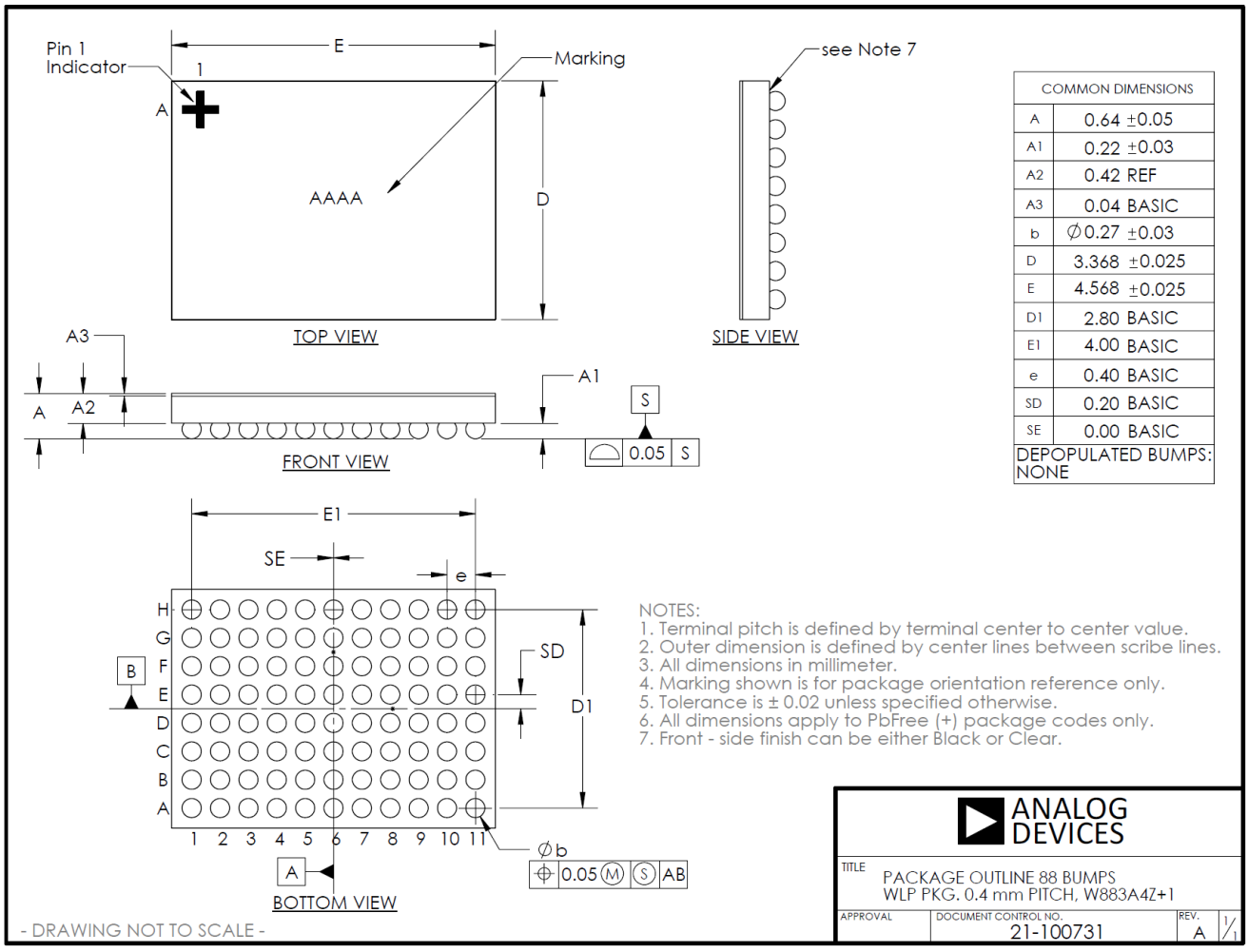
Absolute Maximum Ratings

VEXT1 to AGND ..... -0.3V to +38.0V
VEXT2 to AGND ..... -0.3V to +24.0V
VEXT1_DRV, VEXT2_DRV to AGND ..... -0.3V to +30.0V
VEXT1_DRV to VEXT1 ..... -38.0V to +6.0V
VEXT2_DRV to VEXT2 ..... -24.0V to +6.0V
VB_IN to AGND ..... -0.3V to +24.0V
VB_OUT to AGND ..... -0.3V to +24.0V
VIN to PGND ..... -0.3V to +24.0V
VIN to PMID ..... -17.6V to +17.6V
PMID to C1Px ..... -0.3V to +6.0V
PMID to PGND ..... -0.3V to +17.6V
BSTx to PGND ..... -0.3V to +23.6V
BSTx to C1Px ..... -0.3V to +6.0V
C1Px to C2Px ..... -0.3V to +17.6V
C1Px to PGND ..... -0.3V to +17.6V
C2Px to VOUT ..... -0.3V to +6.0V
C2Px to PGND ..... -0.3V to +12.0V
VOUT to C1Nx, C2Nx ..... -0.3V to +6.0V
C1Nx, C2Nx to PGND ..... -0.3V to +6.0V
VOUT to PGND ..... -0.3V to +6.0V
PVDD to PGND ..... -0.3V to +6.0V
AVDD to AGND ..... -0.3V to +2.2V
BATP to AGND ..... VOUT - 0.6V to VOUT + 0.3V
BATN to AGND ..... -0.6V to +0.6V
BATP to BATN ..... -0.3V to +6.0V
NTC to AGND ..... -0.3V to +6.0V
ENB, VB_EN, SYNC, INTB, VIO to AGND ..... -0.3V to +2.2V
SCL, SDA to AGND ..... -0.3V to +2.2V
AGND, DGND to PGND ..... -0.3V to +0.3V
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 28.46mW/°C above +70°C.) 2276.69mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	W883A4+1
Outline Number	21-100731
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Single Layer Board:	
Junction-to-Ambient (θ_{JA})	—
Junction-to-Case Thermal Resistance (θ_{JC})	—
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	35.14°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	—



For the latest package outline information and land patterns (footprints), go to *www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html*.

Electrical Characteristics

(VIN = +11.4V, VOUT = +3.8V, VIO = +1.8V, VEXT1 = 0V, VEXT2 = VIN, VB_IN = 0V, VB_OUT = 0V, C_{FLY1} = 2 x 22µF, C_{FLY2} = 2 x 22µF, f_{SW} = 857kHz, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL INPUT SUPPLY						
Deep Shutdown Supply Current	$I_{VOUT\_DEEP\_SHDN}$	VEXT2 = VIN = 0V, VOUT = 4.4V, VIO = 0V, ENB = HIGH, I²C is inactive, T_A = +25°C		4.2	6.5	µA
Shutdown Supply Current	$I_{VOUT\_SHDN\_NPLGIN}$	VEXT2 = VIN = 0V, VOUT = 4.4V, VIO = 1.8V, ENB = HIGH, I²C is active, T_A = +25°C		14.5	25	µA
	$I_{VIO\_SHDN\_NPLGIN}$	VEXT2 = VIN = 0V, VOUT = 4.4V, VIO = 1.8V, ENB = HIGH, I²C is active, T_A = +25°C		0.5	1	
	$I_{VEXT2\_SHDN\_PLGIN}$	VEXT2 = VIN = 5V, VOUT = 4.4V, VIO = 1.8V, ENB = HIGH, I²C is active, T_A = +25°C		45	55	
	$I_{VOUT\_SHDN\_PLGIN}$	VEXT2 = VIN = 5V, VOUT = 4.4V, VIO = 1.8V, ENB = HIGH, I²C is active, T_A = +25°C		141	165	
	$I_{VIO\_SHDN\_PLGIN}$	VEXT2 = VIN = 5V, VOUT = 4.4V, VIO = 1.8V, ENB = HIGH, I²C is active, T_A = +25°C		0.5	1	
Standby Quiescent Current	$I_{Q\_EXT\_DRV\_ON}$	VOUT = 4.4V, VIO = 1.8V, ENB = LOW, OPERATION_MODE[2:0] = 0x0, (VEXT1 = VIN = 15V, VEXT1_DRV is ON) or (VEXT2 = VIN = 15V, VEXT2_DRV is ON), EXT_DRV_LPM_EN = 1, T_A = +25°C		145	200	µA
	$I_{Q\_VEXT2\_STBY}$	VEXT2 = VIN = 15V, VOUT = 4.4V, VIO = 1.8V, ENB = LOW, OPERATION_MODE[2:0] = 0x0, VEXT1 = 0, VEXT1_DRV is OFF, VEXT2_DRV is OFF, EXT_DRV_LPM_EN = 1, T_A = +25°C		100	120	
Forward Quiescent Current	$I_{Q\_FWD\_3TO1}$	VIN = 13.2V, VOUT = 4.4V, VIO = 1.8V, IVOUT = 0A, ENB = LOW, OPERATION_MODE[2:0] = 0x1, T_A = +25°C		21	27	mA
	$I_{Q\_FWD\_2TO1}$	VIN = 8.8V, VOUT = 4.4V, VIO = 1.8V, IVOUT = 0A, ENB = LOW, OPERATION_MODE[2:0] = 0x2, T_A = +25°C		23	31	
	$I_{Q\_FWD\_1TO1}$	VIN = 4.4V, VOUT = 4.4V, VIO = 1.8V, IVOUT = 0A, ENB = LOW, OPERATION_MODE[2:0] = 0x3, T_A = +25°C		0.8	2.1	
Reverse Quiescent Current	$I_{Q\_RVS\_1TO3}$	VOUT = 4.4V, IVIN = 0A, VIO = 1.8V, ENB = LOW, OPERATION_MODE[2:0] = 0x6, SKIP = 0, AUDIO = 0, T_A = +25°C		63	78	mA
	$I_{Q\_RVS\_1TO3\_SKIP}$	VOUT = 4.4V, IVIN = 0A, VIO = 1.8V, ENB = LOW, OPERATION_MODE[2:0] = 0x6, SKIP = 1, AUDIO = 0, T_A = +25°C		5	6.1	

(VIN = +11.4V, VOUT = +3.8V, VIO = +1.8V, VEXT1 = 0V, VEXT2 = VIN, VB_IN = 0V, VB_OUT = 0V, C_{FLY1} = 2 x 22µF, C_{FLY2} = 2 x 22µF, f_{SW} = 857kHz, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	$I_{Q\_RVS\_1TO3\_AUDIO}$	VOUT = 4.4V, IVIN = 0A, VIO = 1.8V, ENB = LOW, OPERATION_MODE[2:0] = 0x6, SKIP = 1, AUDIO = 1, T_A = +25°C		5	6.2	
	$I_{Q\_RVS\_1TO2}$	VOUT = 4.4V, IVIN = 0A, VIO = 1.8V, ENB = LOW, OPERATION_MODE[2:0] = 0x5, SKIP = 0, AUDIO = 0, T_A = +25°C		33	48	
	$I_{Q\_RVS\_1TO2\_SKIP}$	VOUT = 4.4V, IVIN = 0A, VIO = 1.8V, ENB = LOW, OPERATION_MODE[2:0] = 0x5, SKIP = 1, AUDIO = 0, T_A = +25°C		3.3	4.2	
	$I_{Q\_RVS\_1TO2\_AUDIO}$	VOUT = 4.4V, IVIN = 0A, VIO = 1.8V, ENB = LOW, OPERATION_MODE[2:0] = 0x5, SKIP = 1, AUDIO = 1, T_A = +25°C		3.3	4.2	
	$I_{Q\_RVS\_1TO1}$	VOUT = 4.4V, IVIN = 0A, VIO = 1.8V, ENB = LOW, OPERATION_MODE[2:0] = 0x4, T_A = +25°C		0.7	2	
VIN/VOUT UNDERVOLTAGE LOCKOUT						
VIN Undervoltage Lockout Threshold	V_{VIN_UVLO}	Rising	3.15	3.3	3.45	V
		Falling	2.4	2.55	2.7	
VOUT Undervoltage Lockout Threshold	V_{VOUT_UVLO}	Rising	3.0	3.1	3.2	V
		Falling	2.9	3.0	3.1	
VOUT Undervoltage Lockout Threshold for Reverse Soft-Start	$V_{VOUT\_UVLO\_RVS\_SS}$	Rising	3.2	3.3	3.4	V
		Falling	3.1	3.2	3.3	
VIN/VOUT OVERVOLTAGE LOCKOUT						
VIN Overvoltage Lockout Threshold	$V_{VIN\_OVLO\_1}$	Rising, I²C-programmable options: 5.2V, 5.3V, 5.4V, 5.5V; default 5.4V, OPERATION_MODE[2:0] = 0x3 or 0x4		5.4		V
		Hysteresis		0.1		
		Accuracy	-2.5		+2.5	%
	$V_{VIN\_OVLO\_2}$	Rising, I²C-programmable options: 10.4V, 10.6V, 10.8V, 11V; default 10.8V, OPERATION_MODE[2:0] = 0x2 or 0x5		10.8		V
		Hysteresis		0.22		
		Accuracy	-2.5		+2.5	%
	$V_{VIN\_OVLO\_3}$	Rising, I²C-programmable options: 15.6V, 15.9V, 16.2V, 16.5V; default 16.2V, OPERATION_MODE[2:0] = 0x1 or 0x6		16.2		V
		Hysteresis		0.3		
		Accuracy	-2.5		+2.5	%
VOUT Overvoltage Lockout Threshold	V_{VOUT_OVLO}	Rising, I²C-programmable options: 4.9V, 5.1V; default 4.9V		4.9		V
		Hysteresis		0.1		
		Accuracy	-2.5		+2.5	%
THERMAL ALARMS AND SHUTDOWN						
Thermal Alarm	T_{INT}	T_J rising, 15°C hysteresis		140		°C
Thermal Shutdown	T_{SHDN}	T_J rising, 15°C hysteresis		155		°C
VEXT1/2 FET CONTROL						

(VIN = +11.4V, VOUT = +3.8V, VIO = +1.8V, VEXT1 = 0V, VEXT2 = VIN, VB_IN = 0V, VB_OUT = 0V, C_{FLY1} = 2 x 22µF, C_{FLY2} = 2 x 22µF, f_{SW} = 857kHz, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VEXT1/2 Undervoltage Lockout Threshold	V_{VEXT_UVLO}	Rising	3.2	3.3	3.4	V
		Falling	2.5	2.6	2.7	
VEXT1/2 Overvoltage Lockout Threshold	V_{VEXT_OVLO}	Rising, I²C-programmable options: 6.5V, 13V, 13.5V, 17V, 17.5V, 18V, 18.5V, 19V; default 13.5V		13.5		V
		Hysteresis, $VEXT_X$ = 13.5V		0.26		
		Accuracy, VEXTx_OVP_TH[2:0] = 13.5V	-2.5		+2.5	%
VEXT1/2 Gate Drive Voltage (Output HIGH Level)	$V_{VEXT\_DRV\_LV}$	VEXTx_DRV_VOLT = 0, 0µA VEXTx_DRV output current, VEXTx = 11.4V, EXT_DRV_LPM_EN = 0			5.25	V
		VEXTx_DRV_VOLT = 0, 5µA VEXTx_DRV output current, VEXTx = 11.4V, EXT_DRV_LPM_EN = 0	4.75			
		VEXTx_DRV_VOLT = 0, 20µA VEXTx_DRV output current, VEXTx = 11.4V, EXT_DRV_LPM_EN = 0	4.5			
	$V_{VEXT\_DRV\_HV}$	VEXTx_DRV_VOLT = 1, 20µA VEXTx_DRV output current, VEXTx = 11.4V, EXT_DRV_LPM_EN = 0	4.8	5.1		
VEXT1/2 Gate Drive Voltage (Output LOW Level)	$V_{VEXT\_DRV\_LOW}$			0		V
Auto Turn-On Debounce Time	$t_{DEB\_VEXT\_AUTO}$	EXTx_SW_CTRL1 = 1		140.4	144.9	µs
Turn-On Response Time	t_{ON_VEXT}	R_L = 100Ω, C_{VIN} = 1µF, time from VIN = 0.1 x VEXTx to VIN = 0.9 x VEXTx		1	5	ms
VEXT1/2 Turn-On Slew Rate		Measured at VEXTx, C_{VEXTx} = 1µF, VIN = 15V, EXTx_SW_CTRL1 = 0, EXTx_SW_CTRL2 from 0 to 1, EXT2_GATE_CTRL = 0, EXT_SW_RVS_TURN_ON_SPEED[1:0] = 0x2, slew rate from VEXTx = 0.1 x VIN to VEXTx = 0.9 x VIN (*Note 1*)		14.6		mV/µs
Turn-Off Response Time	t_{OFF_VEXT}	R_L = 100Ω, C_{VIN} = 1µF, VEXTx from 0V to 24V at 14V/µs (*Note 1*)		44		ns
Manual Turn-On Delay Time	$t_{ON\_DELAY\_VEXT\_MANUAL}$	EXTx_SW_CTRL1 = 0, EXTx_SW_CTRL2 from 0 to 1		0.15	5	ms
Manual Turn-Off Delay Time	$t_{OFF\_DELAY\_VEXT\_MANUAL}$	EXTx_SW_CTRL1 = 0, EXTx_SW_CTRL2 from 1 to 0		0.1	5	ms
VEXT1 Discharge Resistance	R_{DIS_VEXT1}	EXT1_DISCHG_CTRL1 = 1		1		kΩ
VEXT2 Discharge Resistance	R_{DIS_VEXT2}	EXT2_DISCHG_CTRL1 = 1		10		kΩ
VEXT1 Discharge-On Delay Time	$t_{ON\_DELAY\_DIS\_VEXT1}$			0.9	5	µs
VEXT2 Discharge-On Delay Time	$t_{ON\_DELAY\_DIS\_VEXT2}$			2.5	5	µs
VEXT1 Discharge-Off Delay Time	$t_{OFF\_DELAY\_DIS\_VEXT1}$			0.35	5	µs
VEXT2 Discharge-Off Delay Time	$t_{OFF\_DELAY\_DIS\_VEXT2}$			1	5	µs

(VIN = +11.4V, VOUT = +3.8V, VIO = +1.8V, VEXT1 = 0V, VEXT2 = VIN, VB_IN = 0V, VB_OUT = 0V, C_{FLY1} = 2 x 22µF, C_{FLY2} = 2 x 22µF, f_{SW} = 857kHz, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXT SW Open Detection Threshold	$V_{OPEN\_DET\_EXT\_SW}$	Measured between VEXTx and VIN, rising, I²C-programmable options: 0.5V, 1V, 2V, 3V; default 0.5V		0.5		V
VOLTAGE BLOCKING FET						
VB FET Resistance	R_{DSON_VB}			40		mΩ
ENB, VB_EN, INTB, AND SYNC						
VIO Input Range	V_{VIO}	VIO = 1.8V	1.7	1.8	1.9	V
		VIO = 1.2V	1.1	1.2	1.3	
ENB Debounce Time	t_{DEB_ENB}			10		ms
ENB Input Low-Level	V_{IL_ENB}				0.3 x VIO	V
ENB Input High-Level	V_{IH_ENB}		0.7 x VIO			V
VB_EN Input Low Level	$V_{IL\_VB\_EN}$				0.4	V
VB_EN Input High Level	$V_{IH\_VB\_EN}$		1.1			V
ENB, VB_EN Input Current	I_{LK_EN}	ENB = VB_EN = 1.8V	-1		+1	µA
INTB Output Low-Level	V_{OL_INTB}	Sinking 4mA			0.3	V
SYNC Input Low-Level	V_{IL_SYNC}				0.4	V
SYNC Input High-Level	V_{IH_SYNC}		1.1			V
SYNC Output Low-Level	V_{OL_SYNC}				0.03	V
SYNC Output High-Level	V_{IOH_SYNC}		1.5			V
SYNC Output Phase Shift		f_{SW} = 1000kHz		90		°
SWITCHED CAPACITOR CONVERTER						
Forward Heavy Load Efficiency	η_{HEAVY_FWD}	Measured from VIN to VOUT, VOUT = 4.4V, IVOUT = 9A (*Note 1*)		96.2		%
Forward Medium Load Efficiency	η_{HEAVY_FWD}	Measured from VB_OUT to VOUT, VOUT = 4.4V, IVOUT = 4.5A (*Note 1*)		96.6		%
INFET ON Resistance	R_{DSON_INFET}			11.6		mΩ
S1, S3, S4, S5, S6, S7 ON Resistance	R_{DSON}			6.2		mΩ
S2 ON Resistance	R_{DSON}			9.2		mΩ
Switching Frequency Range	f_{SW}	I²C-programmable options: 200kHz, 300kHz, 400kHz, 500kHz, 600kHz, 666kHz, 750kHz, 857kHz, 1000kHz, 1200kHz, 1500kHz; default 857kHz	200		1500	kHz
Switching Frequency Accuracy	f_{SW_ACC}		-10		+10	%
Dead Time	t_{DDT}	*Note 1*		13		ns
LINEAR REGULATORS						
AVDD Linear Regulator Output Voltage	V_{AVDD}		1.71	1.8	1.89	V
PVDD Linear Regulator Output Voltage	V_{PVDD}	VEXT1 = 10V or VEXT2 = 10V	4	5	6	V
INTERNAL PULLUP/PULLDOWN/DISCHARGE RESISTANCE						

(VIN = +11.4V, VOUT = +3.8V, VIO = +1.8V, VEXT1 = 0V, VEXT2 = VIN, VB_IN = 0V, VB_OUT = 0V, C_{FLY1} = 2 x 22µF, C_{FLY2} = 2 x 22µF, f_{SW} = 857kHz, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENB Pullup Resistance	R_{PU_ENB}	Pulled up to VIO		4		MΩ
VIN Discharge Resistance	R_{DIS_VIN}	VIN_DISCHG_EN = 1, pulled down to AGND		10		kΩ
INPUT REGULATION						
Input Current Regulation Range	I_{IN_REG}	I²C-programmable with IIN_REG[6:0] with 50mA step	0.5		5.5	A
Input Current Regulation Accuracy (≥ 2A)	$I_{IN\_REG\_ACC}$	I_{IN_REG} ≥ 2A, T_J = +25°C	-2.5		+2.5	%
		I_{IN_REG} ≥ 2A, T_J = 0°C to +85°C (*Note 2*)	-4		+4	
Input Current Regulation Accuracy (< 2A)	$I_{IN\_REG\_ACC}$	I_{IN_REG} < 2A, T_J = +25°C	-7		+7	%
		I_{IN_REG} < 2A, T_J = 0°C to +85°C (*Note 2*)	-16		+16	
Input Current Regulation Dynamic Response	$I_{IN\_REG\_TRAN}$	I_{IN} overshoot measured, I_{IN_REG} = 2.7A, VOUT current slew rate = 80mA/µs (*Note 1*)		0.7		A
I_{IN_REF} Auto Tracking Step	$I_{IN\_REF\_AUTO\_TRACK}$	IIN_REG_TRACK_EN = 1, I²C-programmable options: 200mA, 300mA; default 200mA		200		mA
Battery (BATP – BATN) Voltage Regulation Range	V_{BATT_REG}	I²C-programmable with VBATT_REG[7:0] with 5mV step	3.8		4.55	V
Battery (BATP – BATN) Voltage Regulation Accuracy	$V_{BATT\_REG\_ACC}$	V_{BATT_REG} = 4.4V, T_A = +25°C	-0.2		+0.2	%
		V_{BATT_REG} = 4.4V, T_A = 0°C to +85°C (*Note 2*)	-0.445		+0.445	
PROTECTION						
Watchdog Timer Range	t_{WD}	WD_TIMER_EN = 1, I²C-programmable options: 4s, 8s, 16s, 32s; default 4s	4		32	s
Forward OCP Offset Range	I_{OCP_FWD}	I²C-programmable with CHGR_OCP[3:0] from 110mV to 335mV with 15mV step; default: 230mV	110	230	335	mV
Forward OCP Offset Accuracy	$I_{OCP\_FWD\_ACC}$	CHGR_OCP[3:0] = 230mV	-15		+15	%
Reverse OCP Offset Range	I_{OCP_RVS}	I²C-programmable with RVSBST_OCP[3:0] from 70mV to 295mV with 15mV step; default: 190mV	70	190	295	mV
Reverse OCP Offset Accuracy	$I_{OCP\_RVS\_ACC}$	RVSBST_OCP[3:0] = 190mV	-15		+15	%
Reverse Current Protection	I_{RCP}	I²C-programmable with CHGR_RCP[2:0] from 0mV to 70mV with 10mV step; default: 0mV	-10	0	+10	mV
Battery (BATP – BATN) OVP Range	V_{BATT_OVP}	I²C-programmable with VBAT_OVP_TH[6:0] from 4V to 4.6V with 5mV step; default: 4.5V	4	4.5	4.6	V
Battery (BATP – BATN) OVP Accuracy	$V_{BATT\_OVP\_ACC}$		-2.5		+2.5	%
Input Current OCP Range	I_{IN_OCP}	I²C-programmable with IIN_OCP[5:0] from 0.5A to 6A with 0.1A step; default: 1A	0.5		6	A
Input Current OCP Accuracy (≥ 2A)	$I_{IN\_OCP\_ACC}$	I_{IN_OCP} ≥ 2A, T_J = +25°C	-2.5		+2.5	%
		I_{IN_OCP} ≥ 2A, T_J = 0°C to +85°C (*Note 2*)	-4		+4	
	$I_{IN\_OCP\_ACC}$	I_{IN_OCP} < 2A, T_J = +25°C	-6		+6	%

(VIN = +11.4V, VOUT = +3.8V, VIO = +1.8V, VEXT1 = 0V, VEXT2 = VIN, VB_IN = 0V, VB_OUT = 0V, C_{FLY1} = 2 x 22µF, C_{FLY2} = 2 x 22µF, f_{SW} = 857kHz, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current OCP Accuracy (< 2A)		I_{IN_OCP} < 2A, T_J = 0°C to +85°C (*Note 2*)	-8		+8	
Input Current UCP Range	I_{IN_UCP}	I^2C-programmable with IIN_UCP[2:0] from 0.1A to 0.8A with 0.1A step; default: 0.1A	0.1		0.8	A
Input Current UCP Accuracy	$I_{IN\_UCP\_ACC}$	T_J = +25°C	-20		+25	mA
ADC						
ADC Resolution	RES			12		Bits
VIN Voltage Measurement Range		With a resolution of 4.395mV	0		18	V
VIN Voltage Measurement Accuracy (≥ 3.3V)		VIN ≥ 3.3V	-0.5		+0.5	%
VIN Voltage Measurement Accuracy (< 3.3V)		VIN < 3.3V	-1		+1	%
PMID Voltage Measurement Range		With a resolution of 4.395mV	0		18	V
PMID Voltage Measurement Accuracy (≥ 3.3V)		PMID ≥ 3.3V	-0.5		+0.5	%
PMID Voltage Measurement Accuracy (< 3.3V)		PMID < 3.3V	-1		+1	%
VEXT1 Voltage Measurement Range		With a resolution of 4.395mV	0		18	V
VEXT1 Voltage Measurement Accuracy (≥ 3.3V)		VEXT1 ≥ 3.3V	-0.5		+0.5	%
VEXT1 Voltage Measurement Accuracy (< 3.3V)		VEXT1 < 3.3V	-1		+1	%
VEXT2 Voltage Measurement Range		With a resolution of 4.395mV	0		18	V
VEXT2 Voltage Measurement Accuracy (≥ 3.3V)		VEXT2 ≥ 3.3V	-0.5		+0.5	%
VEXT2 Voltage Measurement Accuracy (< 3.3V)		VEXT2 < 3.3V	-1		+1	%
VOUT Voltage Measurement Range		With a resolution of 1.221mV	0		5	V
VOUT Voltage Measurement Accuracy (≥ 3.1V)		VOUT ≥ 3.1V	-0.5		+0.5	%
VOUT Voltage Measurement Accuracy (< 3.1V)		VOUT < 3.1V	-0.7		+0.7	%
Battery (BATP – BATN) Voltage Measurement Range		With a resolution of 1.221mV	0		5	V

(VIN = +11.4V, VOUT = +3.8V, VIO = +1.8V, VEXT1 = 0V, VEXT2 = VIN, VB_IN = 0V, VB_OUT = 0V, C_{FLY1} = 2 x 22µF, C_{FLY2} = 2 x 22µF, f_{SW} = 857kHz, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery (BATP – BATN) Voltage Measurement Accuracy (≥ 3.1V)		BATP – BATN ≥ 3.1V	-0.5		+0.5	%
Battery (BATP – BATN) Voltage Measurement Accuracy (< 3.1V)		BATP – BATN < 3.1V	-0.7		+0.7	%
NTC Voltage Measurement Range		With a resolution of 0.464mV	0		1.9	V
NTC Voltage Measurement Accuracy			-2		+2	%
TDIE Temperature Measurement Range		With a resolution of 0.081°C	-166		+165	°C
TDIE Temperature Measurement Accuracy			-10		+10	°C
IIN Current Measurement Range		With a resolution of 1.563mA	0		6	A
IIN Current Measurement Accuracy (≥ 2A)		IIN ≥ 2A	-3		+3	%
IIN Current Measurement Accuracy (< 2A)		IIN < 2A	-8		+8	%
SDA AND SCL I/O STAGE						
SCL, SDA Input Low-Level	V_{IL_I2C}				0.3 x VIO	V
SCL, SDA Input High-Level	V_{IH_I2C}		0.7 x VIO			V
SCL, SDA Input Hysteresis	V_{HYS_I2C}			0.05 x VIO		V
SCL, SDA Input Current	I_{LK_I2C}	VIO = SCL = SDA = 1.8V	-1		+1	µA
SCL, SDA Input Capacitance		*Note 1*		10		pF
SDA Output Low-Level	V_{OL_SDA}	Sinking 4mA			0.3	V
I²C-COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Setup Time (Repeated) START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD;DAT}$		0			µs
DATA Valid Time	$t_{VD;DAT}$				0.45	µs
DATA Valid Acknowledge Time	$t_{VD;ACK}$				0.45	µs
DATA Setup time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs

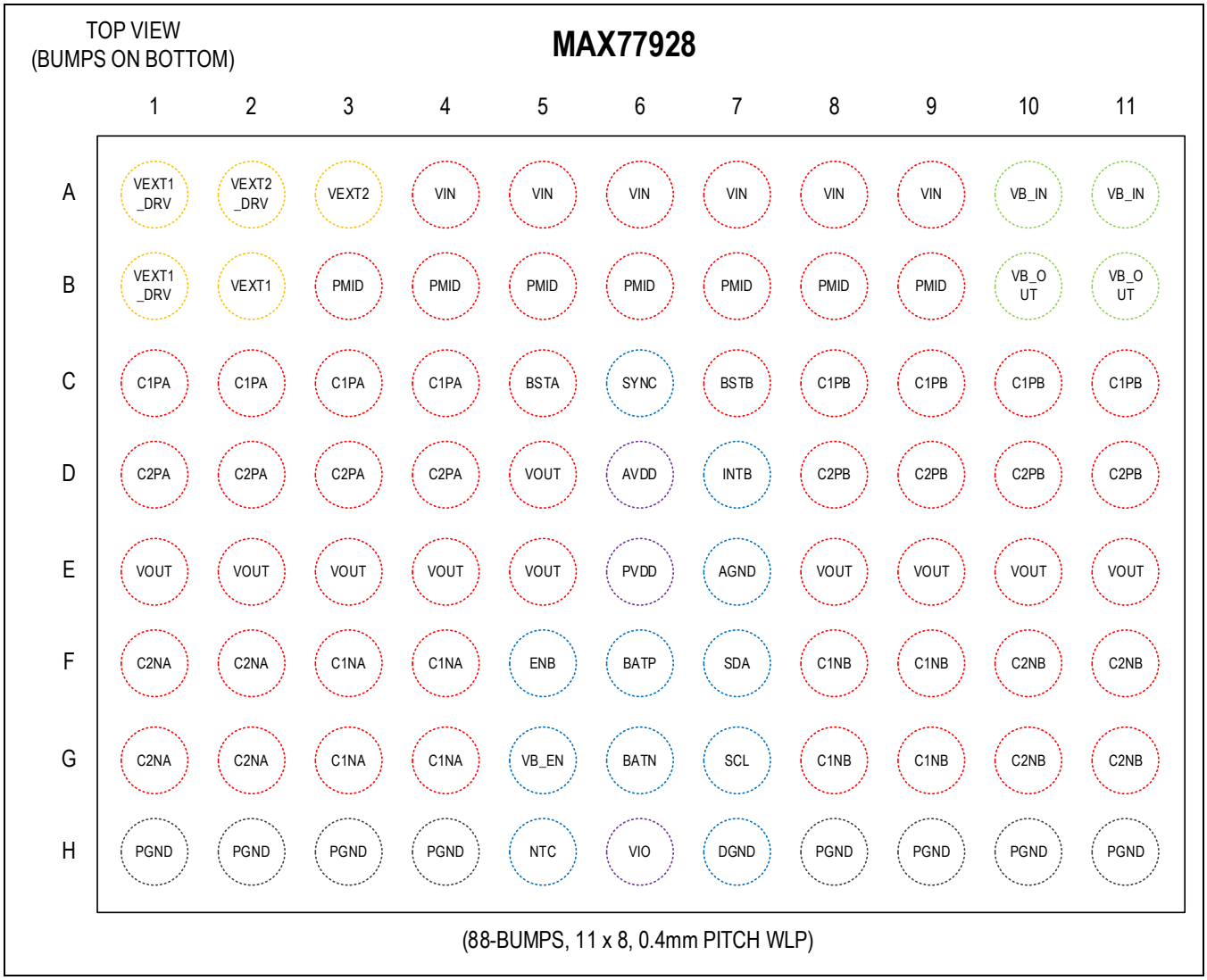
(VIN = +11.4V, VOUT = +3.8V, VIO = +1.8V, VEXT1 = 0V, VEXT2 = VIN, VB_IN = 0V, VB_OUT = 0V, C_{FLY1} = 2 x 22µF, C_{FLY2} = 2 x 22µF, f_{SW} = 857kHz, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Pulse Width of Spikes that must be Suppressed by the Input Filter				50		ns
I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (C_B = 100pF)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time (Repeated) START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Setup time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD;DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that must be Suppressed by the Input Filter				10		ns
I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (C_B = 400pF)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time (Repeated) START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		320			ns
CLK High Period	t_{HIGH}		120			ns
DATA Setup time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD;DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that must be Suppressed by the Input Filter				10		ns

Note 1: Internal design target.

Note 2: Characterized by ATE. Not production tested.

Pin Configurations



Pin Descriptions

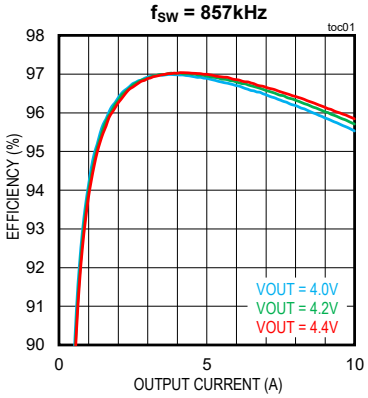
PIN	NAME	FUNCTION	Type
A4, A5, A6, A7, A8, A9	VIN	Switched Capacitor Converter Input for Forward Direction and Output for Reverse Direction. Connect 1 x 10µF/25V capacitor between VIN and PGND.	Power
B3, B4, B5, B6, B7, B8, B9	PMID	Bypass Output of INFET. Connect 2 x 10µF/25V capacitors between PMID and PGND.	Power
C5	BSTA	Supply Input for Internal Gate Driver. Connect a 100nF bootstrap capacitor between BSTA and C1PA.	Analog
C7	BSTB	Supply Input for Internal Gate Driver. Connect a 100nF bootstrap capacitor between BSTB and C1PB.	Analog
C1, C2, C3, C4	C1PA	Flying Capacitor 1 Positive Terminal for Phase A. Connecting 2 x 22µF/16V capacitors between C1PA and C1NA is suggested.	Power
D1, D2, D3, D4	C2PA	Flying Capacitor 2 Positive Terminal for Phase A. Connecting 2 x 22µF/10V capacitors between C2PA and C2NA is suggested.	Power
F3, F4, G3, G4	C1NA	Flying Capacitor 1 Negative Terminal for Phase A	Power
F1, F2, G1, G2	C2NA	Flying Capacitor 2 Negative Terminal for Phase A	Power
C8, C9, C10, C11	C1PB	Flying Capacitor 1 Positive Terminal for Phase B. Connecting 2 x 22µF/16V capacitors between C1PB and C1NB is suggested.	Power
D8, D9, D10, D11	C2PB	Flying Capacitor 2 Positive Terminal for Phase B. Connecting 2 x 22µF/10V capacitors between C2PB and C2NB is suggested.	Power
F8, F9, G8, G9	C1NB	Flying Capacitor 1 Negative Terminal for Phase B	Power
F10, F11, G10, G11	C2NB	Flying Capacitor 2 Negative Terminal for Phase B	Power
E1, E2, E3, E4, E8, E9, E10, E11, D5, E5	VOUT	Switched Capacitor Converter Output for Forward Direction and Input for Reverse Direction. Connect 2 x 10µF capacitors between VOUT and PGND.	Power
H1, H2, H3, H4, H8, H9, H10, H11	PGND	Power Ground	Power
A10, A11	VB_IN	Voltage Blocking FET Input. If this pin is not used, tie it to AGND.	Power
B10, B11	VB_OUT	Voltage Blocking FET Output. If this pin is not used, tie it to AGND.	Power
B2	VEXT1	VEXT1 FET Voltage Input. Connect a 1µF between VEXT1 and AGND. If VEXT1_DRV is not used, tie VEXT1 pin to AGND. If both VEXT1_DRV and VEXT2_DRV are not used, at least one pin of VEXT1 and VEXT2 (can be either pin) must be tied to VIN. If VEXT1_DRV is not used and VEXT1 is tied to VIN, the 1µF bypass cap for VEXT1 is not needed.	Analog
A1, B1	VEXT1_DRV	Gate Driver Output for VEXT1 FET. If this pin is not used, leave it unconnected.	Analog
A3	VEXT2	VEXT2 FET Voltage Input. Connect a 1 x 1µF/35V between VEXT2 and AGND. If VEXT2_DRV is not used, tie VEXT2 pin to AGND. If both VEXT1_DRV and VEXT2_DRV are not used, at least one pin of VEXT1 and VEXT2 (can be either pin) must be tied to VIN. If VEXT2_DRV is not used and VEXT2 is tied to VIN, the 1µF bypass cap for VEXT2 is not needed.	Analog
A2	VEXT2_DRV	Gate Driver Output for VEXT2 FET (External or Internal VB FET). If this pin is not used, leave it unconnected.	Analog
D6	AVDD	1.8V Linear Regulator Output for Internal Use. Connect a 1 x 1µF/10V between AVDD and AGND. Do not apply an external load.	Analog

E6	PVDD	Linear Regulator Output for Internal Power Stage. Connect a 1 x 2.2µF/10V between PVDD and PGND. Do not apply an external load.	Analog
H6	VIO	I/O Supply Voltage Input. Connect a 1 x 1µF/10V capacitor between VIO and DGND.	Analog
E7	AGND	Analog GND. Connect to the system ground directly rather than PGND.	Analog
H7	DGND	Digital GND. Connect to the system ground directly rather than PGND.	Digital
G7	SCL	I^2C Serial Clock. Connect a 2.2kΩ pullup resistor to VIO.	Digital Input
F7	SDA	I^2C Serial Data. Connect a 2.2kΩ pullup resistor to VIO.	Digital I/O
D7	INTB	Interrupt Output. Active-low, open-drain output pin. Connect a 100kΩ pullup resistor to VIO. If this pin is not used, leave it unconnected.	Digital Output
F6	BATP	Battery Positive Differential Sense Connection. Connect to the positive terminal close to the battery.	Analog
G6	BATN	Battery Negative Differential Sense Connection. Connect to the negative or ground terminal close to the battery.	Analog
F5	ENB	Chip Enable Input. Active-low. ENB has an internal pullup resistor to VIO, therefore ENB must not be left unconnected.	Digital Input
G5	VB_EN	Enable Input for Auto Control of VEXT1_DRV and VEXT2_DRV. This pin also changes VEXT1_DRV's internal pulldown and I^2C address. See *VB_EN* for more details.	Digital Input
H5	NTC	Thermistor Connection. Connect an external N-type thermistor between NTC and DGND. Connect an external resistor between VIO and NTC. 100kΩ is recommended. If this pin is not used, tie it to DGND.	Analog
C6	SYNC	Synchronization Input/Output for Parallel Operation. If this pin is not used, leave it unconnected.	Digital I/O

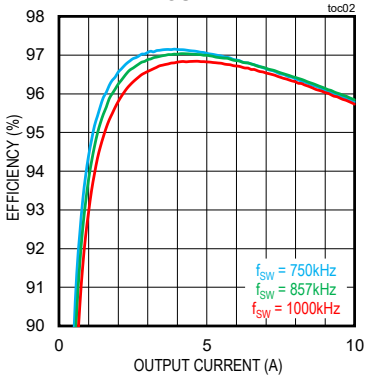
Typical Operating Characteristics

C_{FLY1} = C_{FLY2} = 2x CL10A226MO7JZNC (22µF, 16V, 0603) per phase, T_A = +25°C, unless otherwise noted.

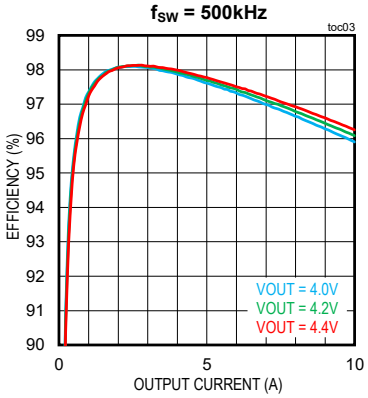
SCC FORWARD 3:1 EFFICIENCY
f_{SW} = 857kHz



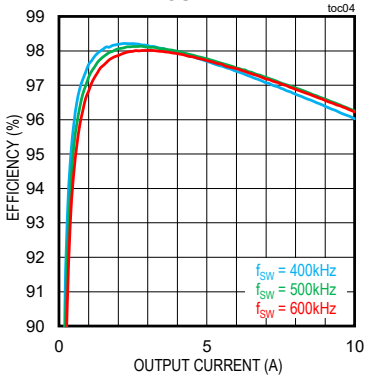
SCC FORWARD 3:1 EFFICIENCY
VOUT = 4.4V



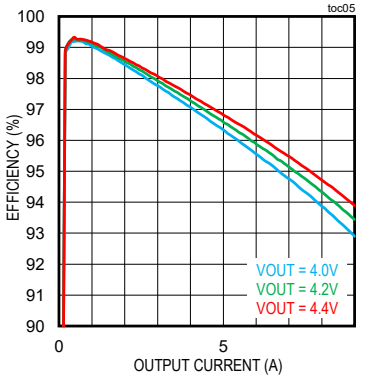
SCC FORWARD 2:1 EFFICIENCY
f_{SW} = 500kHz



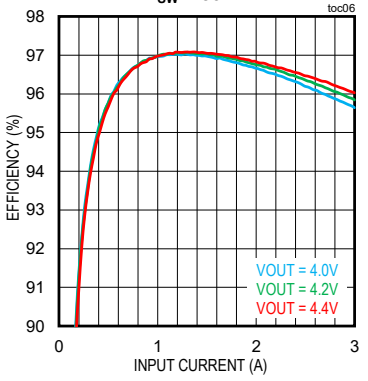
SCC FORWARD 2:1 EFFICIENCY
VOUT = 4.4V



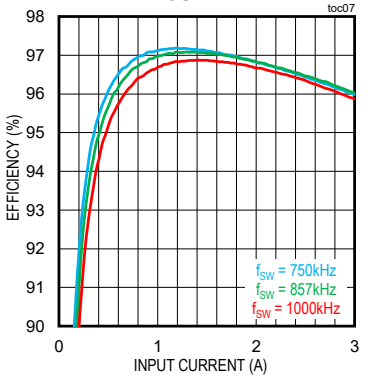
SCC FORWARD 1:1 EFFICIENCY



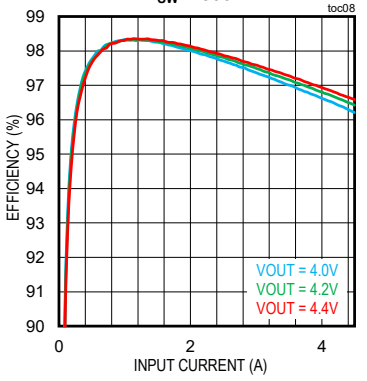
SCC REVERSE 1:3 EFFICIENCY
f_{SW} = 857kHz



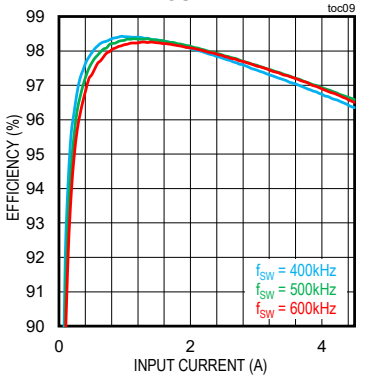
SCC REVERSE 1:3 EFFICIENCY
VOUT = 4.4V



SCC REVERSE 1:2 EFFICIENCY
f_{SW} = 500kHz

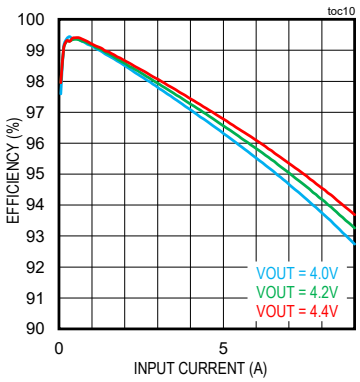


SCC REVERSE 1:2 EFFICIENCY
VOUT = 4.4V



C_{FLY1} = C_{FLY2} = 2x CL10A226MO7JZNC (22µF, 16V, 0603) per phase, T_A = +25°C, unless otherwise noted.

SCC REVERSE 1:1 EFFICIENCY



Detailed Description

The MAX77928 is a complete solution that integrates multiple ratios (3:1 or 2:1 or 1:1) switched-capacitor converter, 2-channel gate drivers for external FETs, a voltage blocking FET, voltage/current regulations, and ADC to charge the 1S battery up to 10A efficiently and safely in cooperation with a USB Type-C Programmable Power Supply (PPS) adapter or without the PPS adapter (limited to 2:1 mode).

3:1/2:1/1:1 Switched-Capacitor Converter

As shown in *Figure 1*, the IC's SCC adopts a Dickson topology configurable to a 3:1/2:1/1:1 power conversion ratio. A two-phase design (phase A and phase B), with a 180-degree phase difference, minimizes the switching ripple.

Every phase operates at 50% duty in 3:1/2:1 modes. INFET is always on during normal operation.

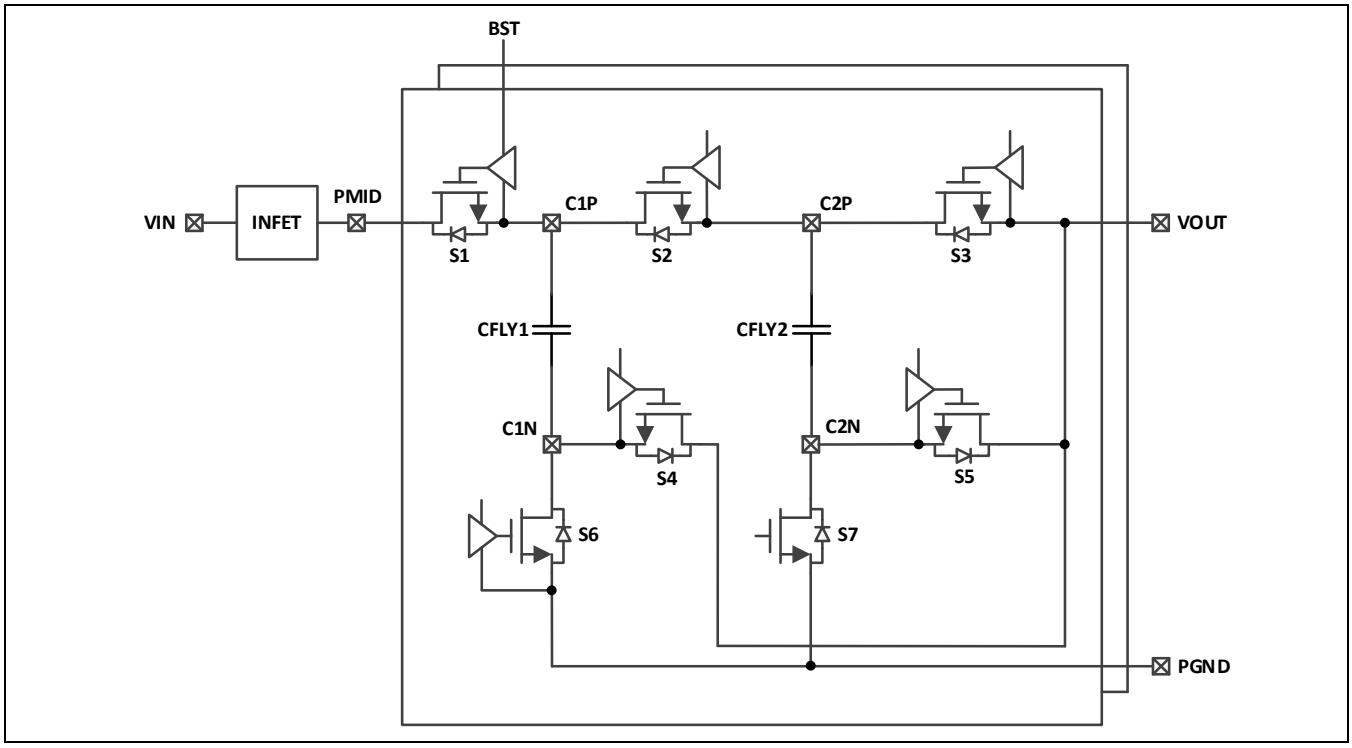


Figure 1. Switched-Capacitor Converter

Forward 3:1 Operation

If OPERATION_MODE[2:0] is set to 0x1, the IC is configured to 3:1 mode. For each switching cycle, S1, S3, S4, and S7 turn on at the same time for 50% duty, and S2, S5, and S6 turn on at the same time for the other 50% duty.

When V_{VIN} is set to 3x V_{VOUT} and the SCC is enabled, the IC initiates the following soft-start procedures:

- PMID is charged up to V_{VOUT}.
- S1 and S2 turn on.
- C_{FLY1} and C_{FLY2} are charged by the internal current sink up to V_{VOUT}.
- C_{FLY1} and C_{FLY2} are checked for open or short faults.
- S2 turns off, and S7 turns on. PMID is charged to V_{VIN}. C_{FLY1} is charged up to 2x V_{VOUT} – V_{DROP}, where V_{DROP} is the body diode drop voltage.
- The SCC starts switching. C_{FLY1} is charged up to 2x V_{VOUT}.
- The INFET turns on.
- A CHGR_SSDONE_INT interrupt is generated.

If the soft-start procedure fails in any of the steps above, a CHGR_SS_FAULT_INT interrupt is generated.

After the soft-start is completed, the IC operates as a switched-capacitor voltage divider with a 3:1 ratio.

Forward 2:1 Operation

If OPERATION_MODE[2:0] is set to 0x2, the IC is configured to 2:1 mode. For each switching cycle, S1, S4, and S5 turn on at the same time for 50% duty, and S3, S6, and S7 turn on at the same time for the other 50% duty. S2 is always on.

When V_{VIN} is set to 2x V_{VOUT} and the SCC is enabled, the IC initiates the following soft-start procedures:

- PMID is charged up to V_{VOUT}.
- S1 and S2 turn on.
- C_{FLY1} and C_{FLY2} are charged by the internal current sink up to V_{VOUT}.
- C_{FLY1} and C_{FLY2} are checked for open or short faults.
- S1 turns off, and S6 and S7 turn on. PMID is charged to V_{VIN}.
- The SCC starts switching.
- The INFET turns on.
- A CHGR_SSDONE_INT interrupt is generated.

If the soft-start procedure fails in any of the steps above, a CHGR_SS_FAULT_INT interrupt is generated.

After the soft-start is completed, the IC operates as a switched-capacitor voltage divider with a 2:1 ratio.

Reverse Boost 1:3 Operation

If OPERATION_MODE[2:0] is set to 0x6, the IC is configured to reverse boost 1:3 mode. For each switching cycle, S1, S3, S4, and S7 turn on at the same time for 50% duty, and S2, S5, and S6 turn on at the same time for the other 50% duty.

When the SCC is enabled, the IC initiates the following soft-start procedures:

- If RVSBST_VIN_VALID_EN = 1, VIN voltage is checked. If $V_{VIN} > V_{VIN\_UVLO}$, reverse soft-start is aborted. An RVSBST_VIN_VALID_INT interrupt is generated.
- V_{VOUT} must be higher than $V_{VOUT\_UVLO\_RVS\_SS}$.
- PMID is charged up to V_{VOUT}.
- C_{FLY1} and C_{FLY2} are charged by internal current sink up to $V_{VOUT} – 2x\ V_{DROP}$ and $V_{VOUT} – V_{DROP}$, respectively, where V_{DROP} is the body diode drop voltage.
- C_{FLY1} and C_{FLY2} are checked for open or short faults.
- S4, S5, S6, and S7 start switching. C_{FLY1} is charged up to $2x\ V_{VOUT} – 2x\ V_{DROP}$. PMID is charged up to $3x\ V_{VOUT} – 3x\ V_{DROP}$.
- S1, S2, and S3 start switching. C_{FLY1} and C_{FLY2} are charged up to $2x\ V_{VOUT}$ and V_{VOUT}, respectively. PMID is charged up to $3x\ V_{VOUT}$.
- The INFET turns on.
- A RVSBST_SSDONE_INT interrupt is generated.

If the soft-start procedure fails in any of the steps above, an RVSBST_SS_FAULT_INT interrupt is generated.

After the soft-start is completed, the IC operates as a switched-capacitor voltage multiplier with a 1:3 ratio.

Reverse Boost 1:2 Operation

If OPERATION_MODE[2:0] is set to 0x5, the IC is configured to reverse boost 1:2 mode. For each switching cycle, S1, S4, and S5 turn on at the same time for 50% duty, and S3, S6, and S7 turn on at the same time for the other 50% duty. S2 is always on.

When the SCC is enabled, the IC initiates the following soft-start procedures:

- If RVSBST_VIN_VALID_EN = 1, VIN voltage is checked. If $V_{VIN} > V_{VIN\_UVLO}$, reverse soft-start is aborted. An RVSBST_VIN_VALID_INT interrupt is generated.
- V_{VOUT} must be higher than $V_{VOUT\_UVLO\_RVS\_SS}$.
- PMID is charged up to V_{VOUT}.
- C_{FLY1} and C_{FLY2} are charged by internal current sink up to $V_{VOUT} – 2x\ V_{DROP}$ and $V_{VOUT} – V_{DROP}$, respectively, where V_{DROP} is the body diode drop voltage.
- C_{FLY1} and C_{FLY2} are checked for open or short faults.
- S4, S5, S6, and S7 start switching. PMID is charged up to $2x\ V_{VOUT} – 3x\ V_{DROP}$.

- S1, S2, and S3 start switching. C_{FLY1} and C_{FLY2} are both charged up to V_{VOUT}. PMID is charged up to 2x V_{VOUT}.
- The INFET turns on.
- A RVSBST_SSDONE_INT interrupt is generated.

If the soft-start procedure fails in any of the steps above, an RVSBST_SS_FAULT_INT interrupt is generated.

After the soft-start is completed, the IC operates as a switched-capacitor voltage multiplier with a 1:2 ratio.

Forward 1:1 Operation

If OPERATION_MODE[2:0] is set to 0x3, the IC is configured to forward 1:1 mode. S1, S2, S3, S6, and S7 are always on. S4 and S5 are always off.

When V_{VIN} is set to V_{VOUT} and the SCC is enabled, the IC initiates the following soft-start procedures:

- V_{VOUT} must be higher than $V_{VOUT\_UVLO\_RVS\_SS}$.
- PMID is charged up to V_{VOUT}.
- Internal charge pump turns on. S1, S2, and S3 turn on.
- C_{FLY1} and C_{FLY2} are charged by the internal current sink up to V_{VOUT}.
- C_{FLY1} and C_{FLY2} are checked for open or short faults.
- S6 and S7 turn on.
- The INFET turns on.
- A CHGR_SSDONE_INT interrupt is generated.

If the soft-start procedure fails in any of the steps above, a CHGR_SS_FAULT_INT interrupt is generated.

After the soft-start is completed, the IC operates as a bypass from VIN to VOUT.

Reverse 1:1 Operation

If OPERATION_MODE[2:0] is set to 0x4, the IC is configured to reverse 1:1 mode. S1, S2, S3, S6, and S7 are always on. S4 and S5 are always off.

When the SCC is enabled, the IC initiates the following soft-start procedures:

- If RVSBST_VIN_VALID_EN = 1, VIN voltage is checked. If $V_{VIN} > V_{VIN\_UVLO}$, reverse soft-start is aborted. An RVSBST_VIN_VALID_INT interrupt is generated.
- V_{VOUT} must be higher than $V_{VOUT\_UVLO\_RVS\_SS}$.
- PMID is charged up to V_{VOUT}.
- Internal charge pump turns on. S1, S2, and S3 turn on.
- C_{FLY1} and C_{FLY2} are charged by the internal current sink up to V_{VOUT}.
- C_{FLY1} and C_{FLY2} are checked for open or short faults.
- S6 and S7 turn on.
- The INFET turns on.
- A RVSBST_SSDONE_INT interrupt is generated.

If the soft-start procedure fails in any of the steps above, an RVSBST_SS_FAULT_INT interrupt is generated.

After the soft-start is completed, the IC operates as a bypass from VOUT to VIN.

Skip Mode and Fixed-Frequency Mode

In forward mode (battery charging), the SCC always works in fixed-frequency mode. In reverse boost mode (OTG mode), the SCC supports both auto-skip mode and fixed-frequency mode.

In the fixed-frequency mode, the SCC provides unregulated V_{PMID}/N (ratio) voltage at VOUT in a forward direction, and it provides unregulated V_{VOUT} x N voltage at PMID in a reverse direction. The switching frequency can be configured by FREQ[3:0]. FREQ[3:0] cannot be changed on the fly in the Active state.

To enable the SCC to automatically enter skip mode when the load current is low (auto-skip mode), set SKIP = 1. To configure the SCC to always operate in the fixed-frequency mode, set SKIP = 0. In auto-skip mode, the threshold between skip operation and fixed-frequency operation is configured by VSKIP[2:0] and ISKIP[2:0]. When $V_{VOUT} - V_{PMID}/N$ is lower than VSKIP[2:0] and I_{IN} is lower than ISKIP[2:0], the SCC enters skip mode, and the SCC transitions from skip mode to fixed-frequency mode when $V_{VOUT} - V_{PMID}/N$ is higher than VSKIP[2:0] or I_{IN} is higher than ISKIP[2:0]. By

doing it this way, the SCC saves power in light loads, provides high efficiency at the entire load range, and maintains V_{PMID} close to V_{VOUT} x N.

Audio Mode

When the SCC operates in skip mode, the skip frequency can be observed at audio frequency of which frequency ranges from 20Hz to 20kHz. It may create audible noise in multilayer chip capacitor on the PCB. The IC provides audio mode which keeps the minimum skip frequency at f_{SW_AUD} (25kHz typical for all switching frequency options).

Frequency Dithering

EMI emissions with a dominant peak frequency can be produced from SCC operation. Frequency dithering can reduce the peak emission of the SCC by spreading the emission over a frequency band. The IC includes a frequency dithering feature applicable to all synthesized frequencies (from 200kHz up to 1.5MHz). Dithering can be disabled or enabled by DTHR and programmed to different spreads by DTHR_DEPTH (3%, 6%).

SCC State Diagram

Figure 2 shows the operation states of SCC and conditions to trigger state transitions. All registers are reset to their default value for each state transition from the Standby state to the Shutdown state. ENB input and STANDBY_MODE_SET bit control the state transition between the Shutdown state and the Standby state. OPERATION_MODE[2:0] controls the state transition between the Standby state and the Active state.

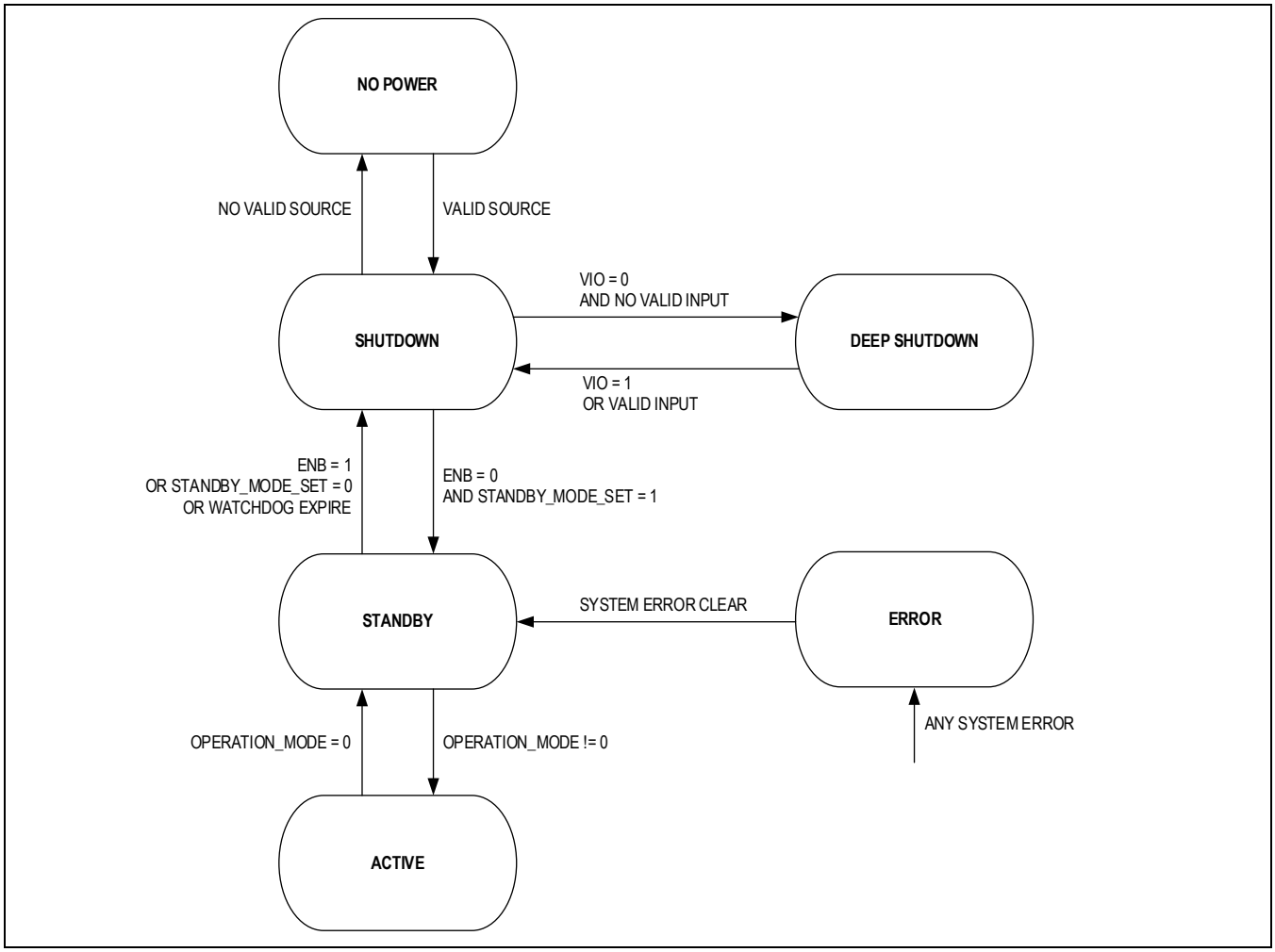


Figure 2. SCC State Diagram

Enable/Disable by ENB

The IC can be enabled or disabled by digitally controlling the ENB pin, an active-low enable pin.

If ENB is pulled low longer than debounce time t_{DEB_ENB} (10ms typical) and STANDBY_MODE_SET is set to 1, the SCC goes to the Standby state. Users can decide which Active state is enabled by setting OPERATION_MODE[2:0].

If ENB is pulled high longer than debounce time t_{DEB_ENB} (10ms typical), the SCC turns off and state goes to Shutdown state. At any Shutdown state entry, all registers are reset.

Frequency Synchronization for Parallel Operation (SYNC)

If there are two MAX77928 in the system, their clock for switching frequency can be synchronized out of phase to avoid overlapping switching noise. Users can enable the frequency synchronization feature by SYNC_EN = 1. SYNC_ROLE sets one of the MAX77928 as master and the other as slave. The SYNC pin of the two MAX77928 must be connected. The master MAX77928 shifts its clock phase by 90 degrees or 180 degrees (programmable by SCC_PH_SEL) and outputs at its SYNC pin, while the slave MAX77928 receives the shifted clock signal at its SYNC pin and uses it for the SCC operation. The switching frequency of the two MAX77928 must be set to the same setting for this feature to operate correctly.

If SYNC_EN = 0, the SYNC pin can be configured by SYNC_OUT[1:0] as a push-pull output to enable/disable external OVP device.

External Gate Drivers and VB FET

The IC provides 2-channel gate drivers (VEXT1_DRV and VEXT2_DRV) to drive external MOSFET(s) or GaN FET(s) or internal VB FET for overvoltage protection or dual-input selection purposes. A voltage-blocking (VB) FET is integrated to withstand 24V input voltage and can be used to replace an external FET. EXT2_GATE_CTRL selects the external switch and VB FET to be driven by VEXT2_DRV.

The gate driver input is automatically identified based on the *SCC State Diagram*. In reverse modes of Active state (OPERATION_MODE = 0x4 or 0x5 or 0x6), VIN is identified as the input. In all other states, VEXTx is identified as the input. See the *System Configurations* section for EXT switch configurations.

When VEXTx_DRV is on, the gate driver outputs a constant gate-drive voltage between VEXTx_DRV and the input (VEXTx or VIN). The gate-drive voltage can be programmed by VEXTx_DRV_VOLT. The low-voltage option $V_{VEXT\_DRV\_LV}$ (VEXTx_DRV_VOLT = 0) is designed for driving a GaN FET, and the high-voltage option $V_{VEXT\_DRV\_HV}$ (VEXTx_DRV_VOLT = 1) is for driving MOSFET(s). When VEXTx_DRV is off, it is pulled down to AGND to ensure the switch is off.

In non-Active states, IC's quiescent current for gate drivers can be reduced by enabling gate drivers' low power mode (EXT_DRV_LPM_EN = 1).

Turn-on and -off of Gate Drivers

Both gate drivers can be independently configured to auto mode or manual mode by EXTx_SW_CTRL1. In reverse modes of the Active state, only manual mode is allowed, and EXTx_SW_CTRL1 = 1 is ignored. In auto mode, the gate driver turns on if the input (VEXTx) voltage is higher than V_{VEXTx_UVLO} and lower than V_{VEXTx_OVLO}. In manual mode, the gate driver turns on if EXTx_SW_CTRL2 (gate driver enable in manual mode) is 1 and the input (VEXTx or VIN) voltage is higher than V_{VEXTx_UVLO} or V_{VIN_UVLO}, and VEXTx voltage is lower than V_{VEXTx_OVLO}. EXTx_SW_CTRL2 = 1 (manual on) is reset to 0 when the input (VEXTx or VIN) voltage falls below its UVLO level.

OVP settings (enable, debounce time, and overvoltage threshold) of VEXT1 and VEXT2 can be independently configured in registers VEXT1_OVP_CFG and VEXT2_OVP_CFG.

VEXT1_DRV and VEXT2_DRV are allowed to be simultaneously on only if both gate drivers are in auto mode or both are in manual mode. If one is in auto mode while the other is in manual mode, simultaneously on is forbidden to avoid shorting CHGIN to WCIN. For the forbidden case, if one of VEXT1_DRV and VEXT2_DRV is already on, the other cannot turn on even if the turn-on condition is satisfied.

The gate drivers' turn-on speed in reverse modes of the Active state can be programmed by EXT_SW_RVS_TURN_ON_SPEED[1:0] to limit the voltage ramp rate when VBUS is powered up in OTG mode. This feature applies to VEXT2 only if VEXT2_DRV drives an external switch (EXT2_GATE_CTRL = 0).

Active discharge of VEXTx can be enabled/disabled by EXTx_DISCHG_CTRL1. EXTx_DISCHG_CTRL1 is reset to 0 when VEXTx falls below 0.3V and EXTx_DISCHG_CTRL2 is 1.

VB_EN

VB_EN pin configures the default mode of EXT1 switch (default value of EXT1_SW_CTRL1), VEXT1_DRV's level when it is off, default mode of EXT2 switch (default value of EXT2_SW_CTRL1), default connection of EXT2_DRV pin (default value of EXT2_GATE_CTRL), and I2C slave address for supporting two MAX77928 on the same I2C bus. All configurations are latched at IC POR. See *Table 1* for details.

If VEXT1_DRV's level is configured to be unconnected when it is off, an external 2MΩ resistor between VEXT1_DRV (Gate of EXT1 switch) and VEXT1 (Source of EXT1 switch) is required to discharge VEXT1_DRV to VEXT1 when VEXT1_DRV is off.

Table 1. VB_EN Configurations

VB_EN CONNECTION	DEFAULT VALUE OF EXT1_SW_CTRL1	VEXT1_DRV's LEVEL WHEN OFF	DEFAULT VALUE OF EXT2_SW_CTRL1	DEFAULT VALUE OF EXT2_GATE_CTRL	I2C SLAVE ADDRESS (7-BIT)
AVDD	1 = Auto Mode	Pulled down to AGND	1 = Auto Mode	1 = Internal VB FET	0b 100 0000
Unconnected	0 = Manual Mode	Unconnected	0 = Manual Mode	0 = External Switch	0b 100 0000
AGND	1 = Auto Mode	Pulled down to AGND	0 = Manual Mode	0 = External Switch	0b 100 1000

System Configurations

The IC supports seven system configurations as detailed in *Figure 3*.

System Configuration 1

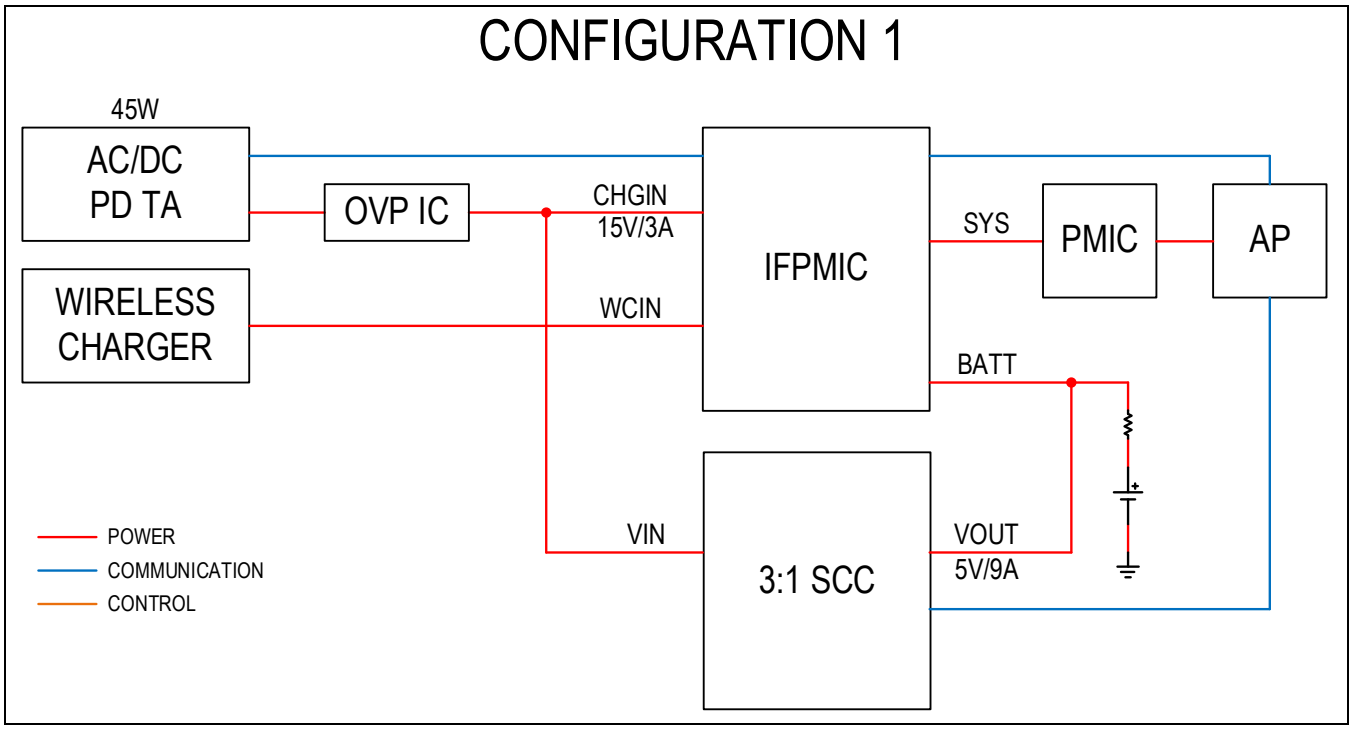


Figure 3. System Configuration 1

Table 2. System Configuration 1 Connection

SINGLE INPUT							
PIN	**VB_EN**	**VEXT1**	**VEXT1_DRV**	**VEXT2**	**VEXT2_DRV**	**VB_IN**	**VB_OUT**
Connection	Unconnected	AGND	AGND	VIN	Open	AGND	AGND

Table 3. System Configuration 1 Register Value

POWER PATH	EXT1_SW_CTRL1	EXT1_SW_CTRL2	EXT2_SW_CTRL1	EXT2_SW_CTRL2	EXT2_GATE_CTRL
Charging	0: Manual	0: Disabled	0: Manual	0: Disabled	0: External switch
OTG/Reverse	0: Manual	0: Disabled	0: Manual	0: Disabled	0: External switch

System Configuration 2

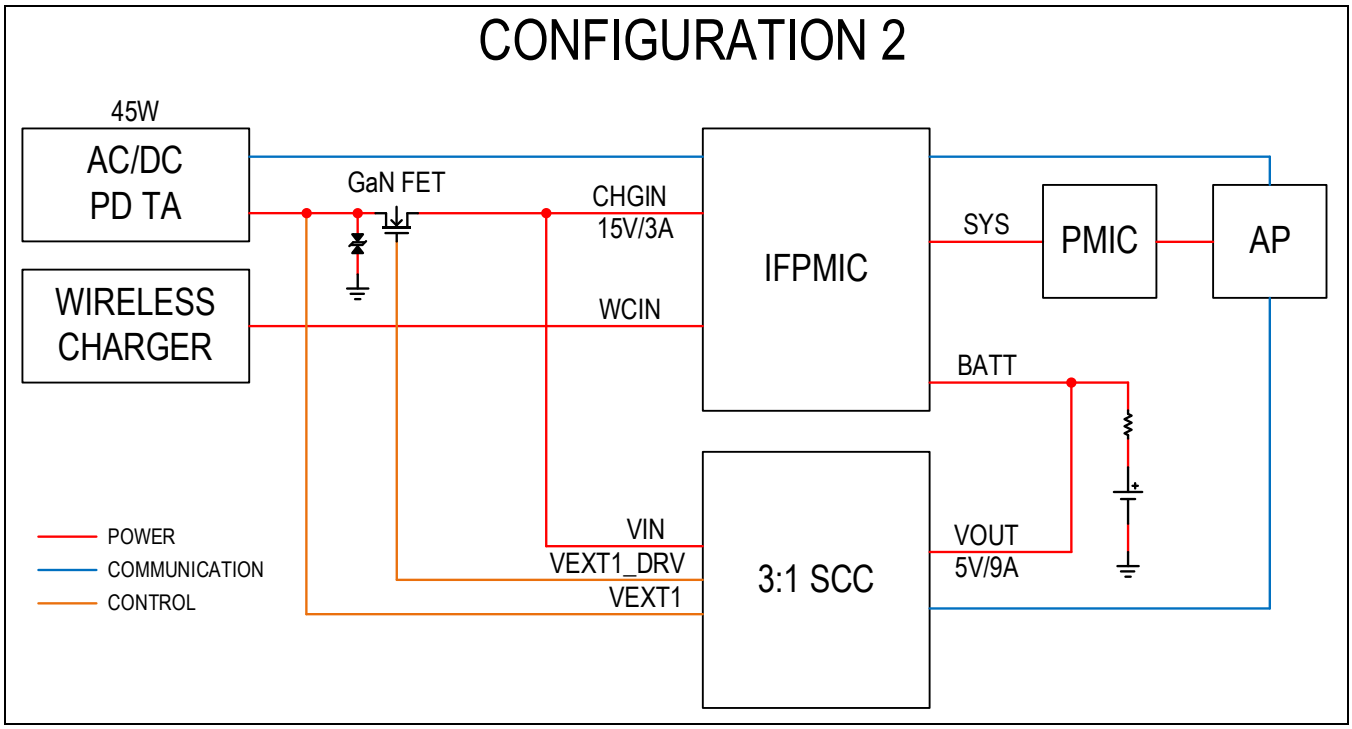


Figure 4. System Configuration 2

Table 4. System Configuration 2 Connection

SINGLE INPUT							
PIN	**VB_EN**	**VEXT1**	**VEXT1_DRV**	**VEXT2**	**VEXT2_DRV**	**VB_IN**	**VB_OUT**
Connection	AGND	VBUS	EXT1 switch gate	VIN	Open	AGND	AGND

Table 5. System Configuration 2 Register Value

POWER PATH	EXT1_SW_CTRL1	EXT1_SW_CTRL2	EXT2_SW_CTRL1	EXT2_SW_CTRL2	EXT2_GATE_CTRL
Charging	1: Auto	0: Disabled	0: Manual	0: Disabled	0: External switch
OTG/Reverse	0: Manual	1: Enabled	0: Manual	0: Disabled	0: External switch

System Configuration 3

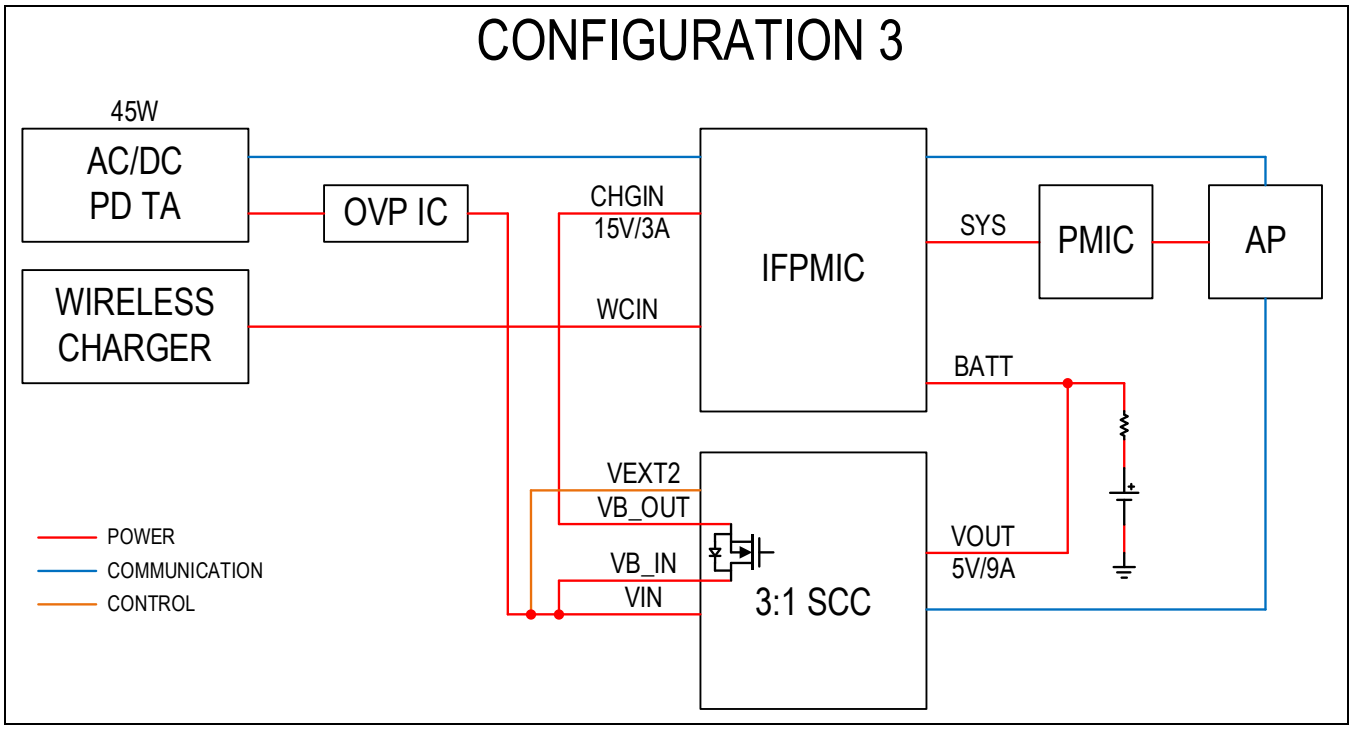


Figure 5. System Configuration 3

Table 6. System Configuration 3 Connection

SINGLE INPUT							
PIN	**VB_EN**	**VEXT1**	**VEXT1_DRV**	**VEXT2**	**VEXT2_DRV**	**VB_IN**	**VB_OUT**
Connection	AVDD	AGND	Open	VIN	VB FET Gate	VIN	CHGIN

Table 7. System Configuration 3 Register Value

POWER PATH	EXT1_SW_CTRL1	EXT1_SW_CTRL2	EXT2_SW_CTRL1	EXT2_SW_CTRL2	EXT2_GATE_CTRL
Charging	1: Auto	0: Disabled	1: Auto	0: Disabled	1: Internal VB FET
OTG/Reverse	1: Auto	0: Disabled	0: Manual	1: Enabled	1: Internal VB FET

System Configuration 4

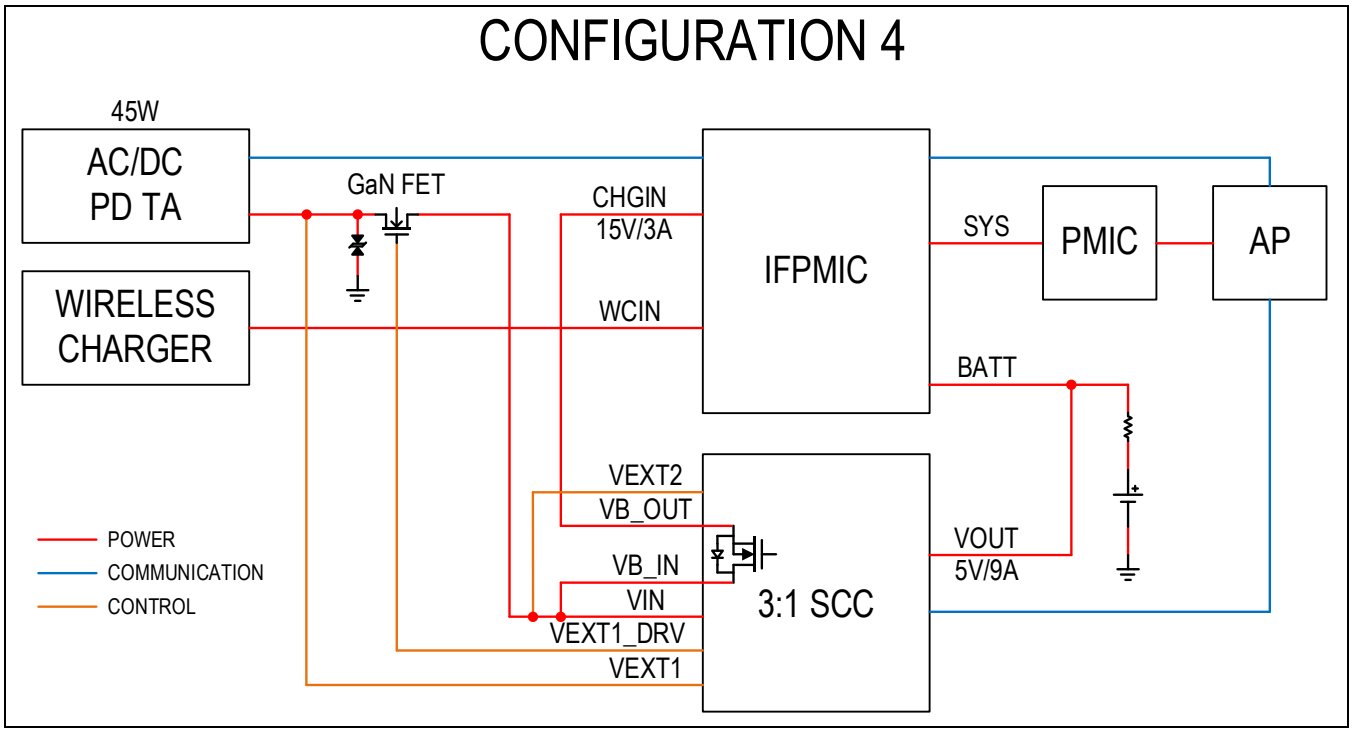


Figure 6. System Configuration 4

Table 8. System Configuration 4 Connection

SINGLE INPUT							
PIN	**VB_EN**	**VEXT1**	**VEXT1_DRV**	**VEXT2**	**VEXT2_DRV**	**VB_IN**	**VB_OUT**
Connection	AVDD	VBUS	EXT1 switch gate	VIN	VB FET Gate	VIN	CHGIN

Table 9. System Configuration 4 Register Value

POWER PATH	EXT1_SW_CTRL1	EXT1_SW_CTRL2	EXT2_SW_CTRL1	EXT2_SW_CTRL2	EXT2_GATE_CTRL
Charging	1: Auto	0: Disabled	1: Auto	0: Disabled	1: Internal VB FET
OTG/Reverse	0: Manual	1: Enabled	0: Manual	1: Enabled	1: Internal VB FET

System Configuration 5

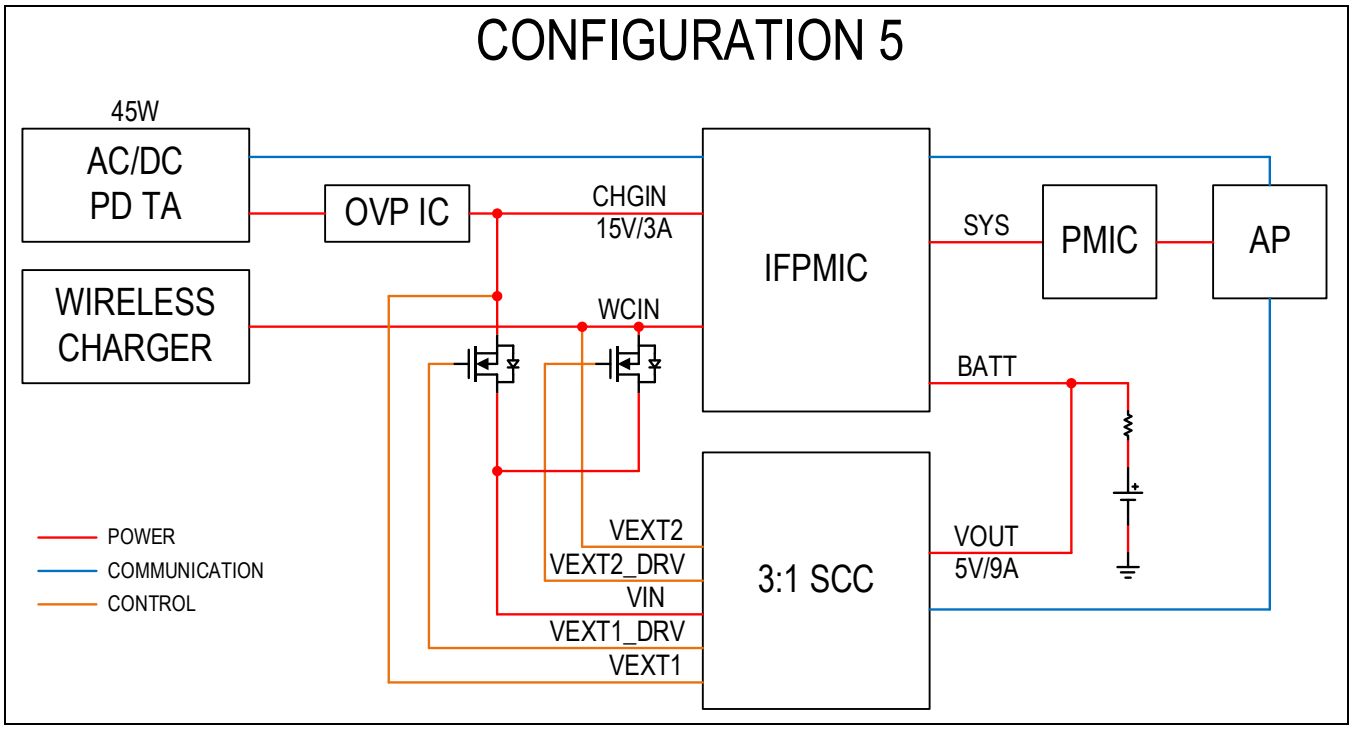


Figure 7. System Configuration 5

Table 10. System Configuration 5 Connection

DUAL INPUT							
PIN	**VB_EN**	**VEXT1**	**VEXT1_DRV**	**VEXT2**	**VEXT2_DRV**	**VB_IN**	**VB_OUT**
Connection	AGND	CHGIN	EXT1 Switch Gate	WCIN	EXT2 Switch Gate	AGND	AGND

Table 11. System Configuration 5 Register Value

POWER PATH	EXT1_SW_CTRL1	EXT1_SW_CTRL2	EXT2_SW_CTRL1	EXT2_SW_CTRL2	EXT2_GATE_CTRL
Charging from CHGIN	1: Auto	0: Disabled	0: Manual	0: Disabled	0: External switch
Charging from WCIN	0: Manual	0: Disabled	0: Manual	1: Enabled	0: External switch
OTG/Reverse to CHGIN	0: Manual	1: Enabled	0: Manual	0: Disabled	0: External switch
OTG/Reverse to WCIN	0: Manual	0: Disabled	0: Manual	1: Enabled	0: External switch
Complex	0: Manual	1: Enabled	0: Manual	1: Enabled	0: External switch

System Configuration 6

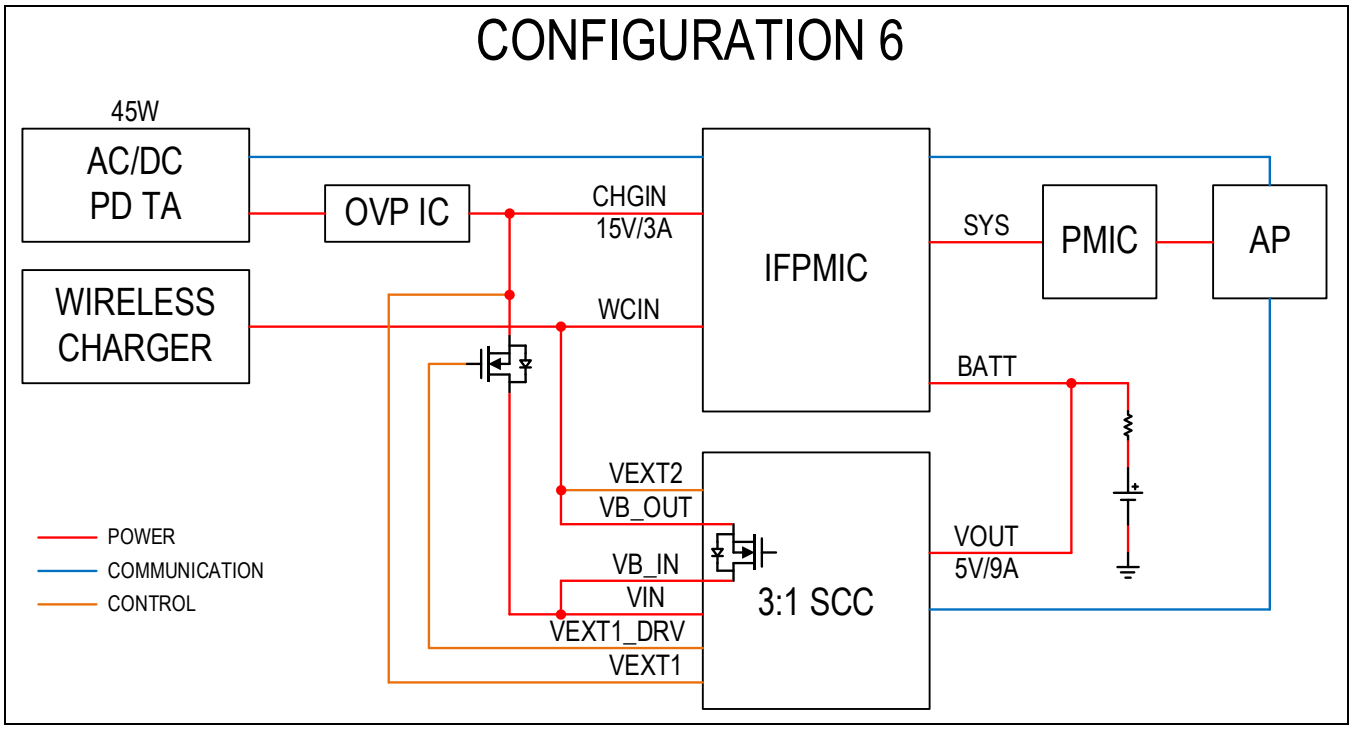


Figure 8. System Configuration 6

Table 12. System Configuration 6 Connection

DUAL INPUT							
PIN	**VB_EN**	**VEXT1**	**VEXT1_DRV**	**VEXT2**	**VEXT2_DRV**	**VB_IN**	**VB_OUT**
Connection	AGND	CHGIN	EXT1 Switch Gate	WCIN	VB FET Gate	VIN	WCIN

Table 13. System Configuration 6 Register Value

POWER PATH	EXT1_SW_CTRL1	EXT1_SW_CTRL2	EXT2_SW_CTRL1	EXT2_SW_CTRL2	EXT2_GATE_CTRL
Charging from CHGIN	1: Auto	0: Disabled	0: Manual	0: Disabled	1: Internal VB FET
Charging from WCIN	0: Manual	0: Disabled	0: Manual	1: Enabled	1: Internal VB FET
OTG/Reverse to CHGIN	0: Manual	1: Enabled	0: Manual	0: Disabled	1: Internal VB FET
OTG/Reverse to WCIN	0: Manual	0: Disabled	0: Manual	1: Enabled	1: Internal VB FET
Complex	0: Manual	1: Enabled	0: Manual	1: Enabled	1: Internal VB FET

System Configuration 7

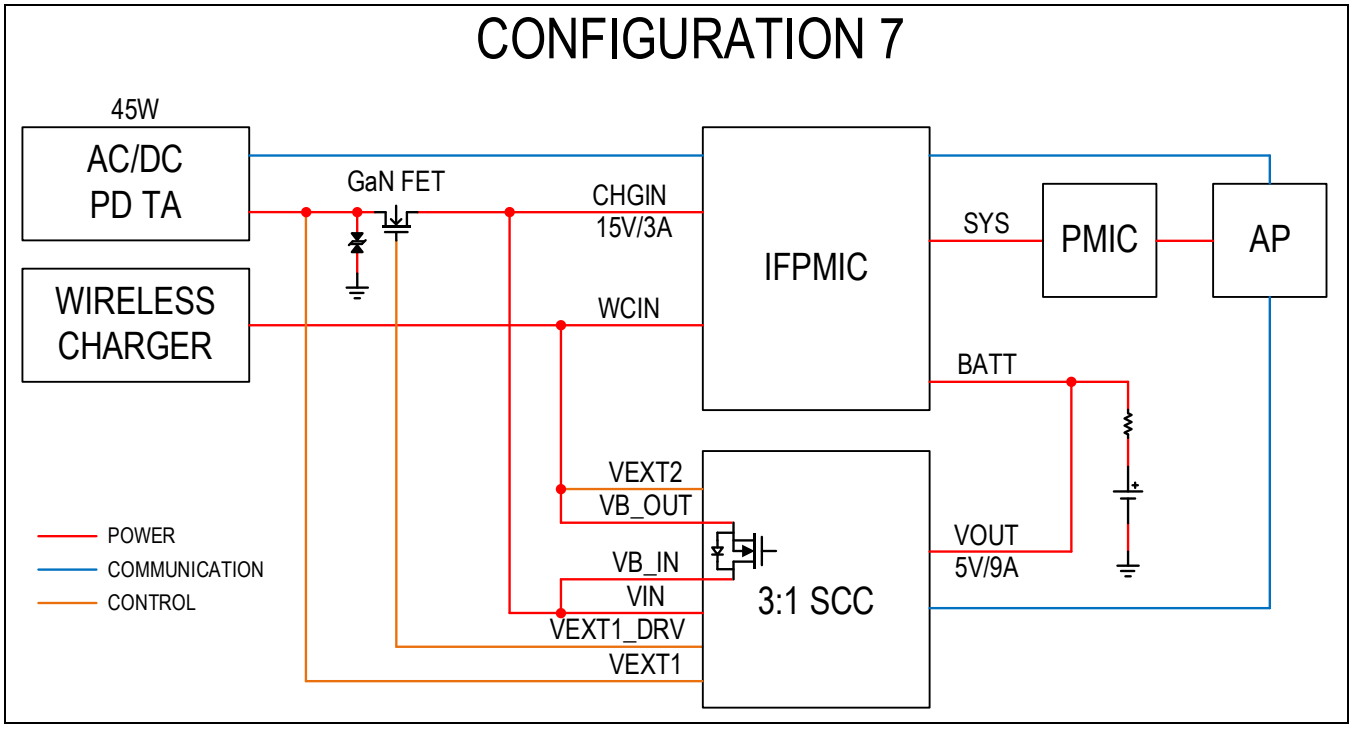


Figure 9. System Configuration 7

Table 14. System Configuration 7 Connection

DUAL INPUT							
PIN	**VB_EN**	**VEXT1**	**VEXT1_DRV**	**VEXT2**	**VEXT2_DRV**	**VB_IN**	**VB_OUT**
Connection	AGND	VBUS	EXT1 switch Gate	WCIN	VB FET Gate	VIN	WCIN

Table 15. System Configuration 7 Register Value

POWER PATH	EXT1_SW_CTRL1	EXT1_SW_CTRL2	EXT2_SW_CTRL1	EXT2_SW_CTRL2	EXT2_GATE_CTRL
Charging from CHGIN	1: Auto	0: Disabled	0: Manual	0: Disabled	1: Internal VB FET
Charging from WCIN	0: Manual	0: Disabled	0: Manual	1: Enabled	1: Internal VB FET
OTG/Reverse to CHGIN	0: Manual	1: Enabled	0: Manual	0: Disabled	1: Internal VB FET
OTG/Reverse to WCIN	0: Manual	0: Disabled	0: Manual	1: Enabled	1: Internal VB FET
Complex	0: Manual	1: Enabled	0: Manual	1: Enabled	1: Internal VB FET

EXT Switch Open Detection

After the gate driver turns on, the IC can detect if the external switch is open by checking the voltage difference between VEXTx and VIN. If the voltage difference (VIN – VEXTx in reverse modes of Active states and VEXTx – VIN in other modes/states) is higher than $V_{OPEN\_DET\_EXT\_SW}$ for a certain debounce time, an EXTx_SW_OPEN_INT interrupt is generated. $V_{OPEN\_DET\_EXT\_SW}$ can be programmed by EXTx_SW_OPEN_DET_TH[1:0] and the debounce time can be programmed by EXTx_SW_OPEN_DET_DEB. EXTx_SW_OPEN_DET_OFF programs if the open detection automatically disables 200ms after switch turn-on or it remains always enabled after switch turn-on.

Regulations

Battery Voltage, Input Current, and Die Temperature Regulations

When charging a battery with a switched-capacitor converter, the controller or application processor needs to control VIN voltage continuously to maintain the charging current (CC) and the termination voltage (CV) to maximize charging efficiency. When the control unit/AP cannot regulate VIN or under the condition of a load transient, undesired high charging current or high voltage can occur. To mitigate the risk, the IC integrates input current regulation and BATP – BATN voltage regulation. When the input current or battery voltage is higher than the regulation target, the regulation loop engages by increasing the headroom of the INFET switch so that the current or voltage settles down to the target for safety. The Input current regulation can be programmed by IIN_REG[6:0] through I^2C from 500mA to 5500mA. The BATP – BATN voltage regulation can be programmed by VBATT_REG[7:0] from 3.8V to 4.55V.

If INFET is in regulation mode, the power dissipation of the INFET increases and may heat up the chip to an undesired temperature. The IC also integrates a local (INFET) die temperature regulation feature and a regulation timer. Until the regulation timer expires, the control unit can adjust the input voltage down to bring the SCC out of regulation mode. The SCC is disabled by the regulation timer when it expires, and a REG_TIMEOUT_INT interrupt is generated. The regulation timer can be programmed by REG_TIMER[2:0].

The loop regulation status is shown in the status bits IIN_REG_S, VBATT_REG_S, and TEMP_REG_S. The local die temperature regulation target can be programmed through I^2C using the TEMP_REG[2:0] bits.

Loop regulation is available only in forward 3:1 and forward 2:1 modes.

Input Current Regulation Auto Tracking

The IC supports auto-tracking of the input current regulation target when the input current drops to keep the regulation target close to the input current and suppress any current overshoot when entering the input current regulation loop. If the current difference between IIN_REG[6:0] and the input current sensed at INFET is maintained higher than the offset (200mA or 300mA, programmable by IIN_REG_TRACK_STEP) for a specific period, IIN_REG[6:0] is lowered by half of IIN_REG_TRACK_STEP (100mA or 150mA). *Figure 10* shows continuous tracking of IIN_REG[6:0] when the input current drops during charge.

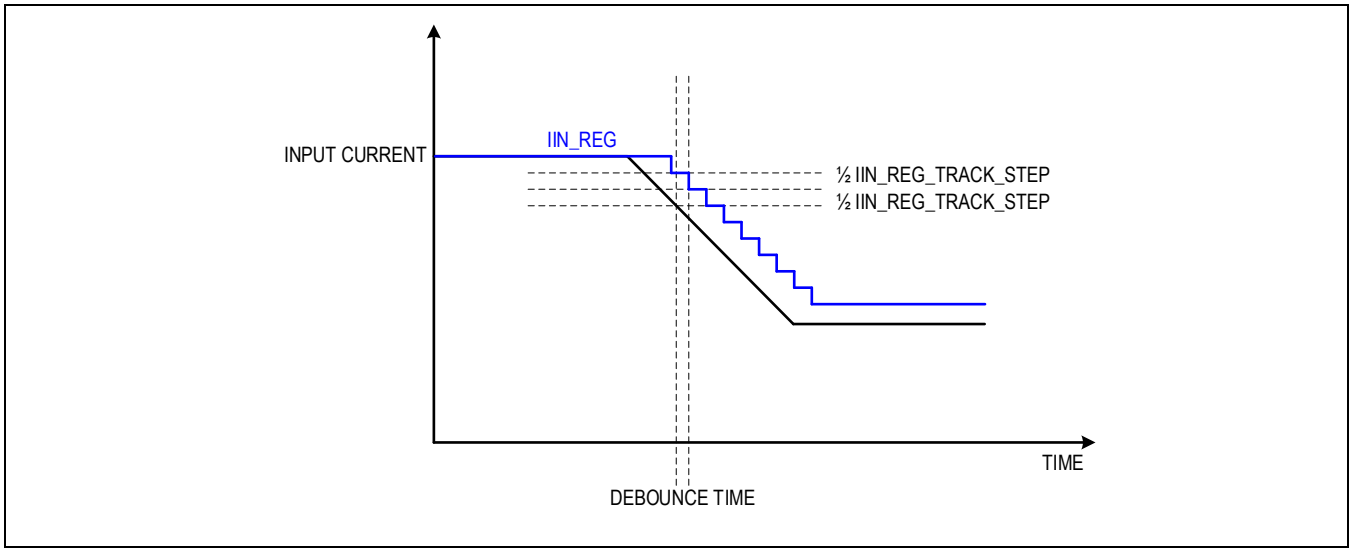


Figure 10. IIN_REG Auto Tracking

To enable the feature, IIN_REG_TRACK_EN needs to be set to 1. Also, input current sense relies on ADC; therefore, ADC and the input current channel must be enabled.

The debounce time for each IIN_REG[6:0] tracking depends on the period of each ADC burst conversion and how many conversions are counted (programmable by IIN_TRACK_CNT_NUM[3:0]), or it can be calculated as ((CONV_NUM[1:0] x Number of channels enabled + 1 dummy) x 1ms + 0.4ms + INTERVAL[1:0]) x IIN_TRACK_CNT_NUM[3:0]. For example, if CONV_NUM[1:0] = 8 samples, Number of channels enabled = 9, INTERVAL[1:0] = 10ms, IIN_TRACK_CNT_NUM[3:0] = 1, Debounce time for IIN_REG_TRACK = ((8 samples x 9 channels + 1 dummy) x 1ms + 0.4ms + 10ms) x 1 = 83.4ms.

Each time IIN_REG[6:0] is lowered by the auto-tracking feature, an IIN_REG_TRACK_INT interrupt is generated.

Protection Features

Input and Output Overvoltage Lockout (VIN OVLO and VOUT OVLO)

The IC provides input overvoltage lockout (VIN OVLO) and output overvoltage lockout (VOUT OVLO) to protect the internal power stage. When V_{VIN} is higher than V_{VIN_OVLO}, or V_{VOUT} is higher than V_{VOUT_OVLO}, the SCC stops operation, and the state goes to the Error state. A VIN_OVP_INT or VOUT_OVP_INT interrupt is generated. The VIN_OVP_S or VOUT_OVP_S status bit is set.

Threshold of VIN OVLO is programmable by VIN_OVP_TH[1:0] and it automatically adjusts for different conversion ratio (3:1/2:1/1:1 mode). Threshold of VOUT OVLO is programmable by VOUT_OVP_TH bit. Debounce time is programmable by VIN_OVP_DEG and VOUT_OVP_DEG, respectively.

VEXT1 and VEXT2 Overvoltage Lockout (VEXT1 OVLO and VEXT2 OVLO)

The IC also provides VEXT1 overvoltage lockout (VEXT1 OVLO) and VEXT2 overvoltage lockout (VEXT2 OVLO) to protect the downstream device. When V_{VEXTx} is higher than V_{VEXT_OVLO}, VEXTx_DRV pulls low to turn off the switch. A VEXTx_OVP_INT interrupt is generated. VEXTx_OVP_S status bit is set.

Threshold of VEXTx OVLO is programmable by VEXTx_OVP_TH[2:0]. Debounce time is programmable by VEXTx_OVP_DEG[1:0].

Battery (BATP – BATN) Overvoltage Lockout (VBATT OVLO)

If the battery voltage is too high during charging, the IC provides a battery (BATP – BATN) overvoltage lockout (VBATT OVLO). When $V_{BATP} – V_{BATN}$ is higher than V_{BATT_OVP}, the SCC stops operation and the state goes to the Error state. A $V_{BATT\_OVP\_INT}$ interrupt is generated.

Threshold of VBATT OVLO is programmable by VBATT_OVP_TH[6:0]. Debounce time is programmable by $V_{BATT\_OVP\_DEG}$.

Overcurrent Protections (CHGR OCP and RVSBST OCP)

The IC provides overcurrent protections which trigger when $V_{PMID}/N – V_{VOUT} > I_{OCP\_FWD}$ (programmable by CHGR_OCP[3:0]) in the forward/charging direction or $V_{VOUT} – V_{PMID}/N > I_{OCP\_RVS}$ (programmable by RVSBST_OCP[3:0]) in the reverse/discharging direction, where N is the conversion ratio. Overcurrent protections help detect hard short quickly and protect the power stage. The SCC stops operation and state goes to Error state. A CHGR_OCP_INT interrupt or RVSBST_OCP_INT interrupt is generated. Debounce time of the overcurrent protections can be programmed by CHGR_OCP_DEG[2:0] and RVSBST_OCP_DEG[2:0], respectively.

Reverse Current Protection (CHGR RCP)

In forward/charging operation, when the input voltage is set lower than N (ratio) x V_{VOUT}, current can flow from battery to input. The IC provides a reverse current protection feature to disable the SCC when $V_{VOUT} – V_{PMID}/N > I_{RCP}$ (programmable by CHGR_RCP[2:0]). A CHGR_RCP_INT interrupt is generated. Debounce time can be programmed by CHGR_RCP_DEG[2:0].

Input Current Overcurrent Protection (IIN OCP)

The IC senses the input current at INFET for IIN OCP and IIN UCP. For both forward and reverse directions, when the input current is higher than I_{IN_OCP} (programmable by IIN_OCP[5:0]), the SCC stops operation and state goes to Error state. An IIN_OCP_INT interrupt is generated. Debounce time can be programmed by IIN_OCP_DEG[1:0].

Adapter Unplug Detection by Input Current Undercurrent Protection (IIN UCP)

In the Active state, when the IC is powered by an external supply at VIN, its voltage may stay at N (ratio) x V_{VOUT} even after removing the input supply. The IC provides a feature that disables the switcher if the input current is too low (IIN_UCP). An IIN_UCP_INT interrupt is generated. With this feature, when the input supply is removed, the VIN of the IC is automatically disconnected from the VOUT. I_{IN_UCP} is programmable by IIN_UCP[2:0]. Debounce time can be programmed by IIN_UCP_DEG[2:0].

In SCC startup, V_{VIN} can be close to N x V_{VOUT}, which means the input current can be very low, and it can trigger IIN UCP. To prevent this undesired event, by setting IIN_DELAY_TIMER[2:0], the user has enough time to adjust the input voltage to make the input current higher than IIN_UCP[2:0]. During this delay time, IIN UCP is ignored. This timer shares the same resource of REG_TIMER. After IIN_DELAY_TIMER expires, the REG_TIMER starts counting when input current regulation or battery voltage regulation is engaged. In the case of updating IIN_DELAY_TIMER[2:0] or REG_TIMER[2:0] on the fly, they must be set to OFF first and then set to the new value.

VIN Short Protection

On top of RVSBST OCP, CHGR RCP, and IIN OCP, the IC provides another layer of protection against a VIN hard short to PGND. After INFET turns on, if the voltage difference between PMID and VIN is higher than V_{VIN_SHORT}, the SCC stops operation and the state goes to an Error state. A VIN_SHORT_INT interrupt is generated.

Threshold of VIN short protection is programmable by VIN_SHORT_TH[1:0]. Debounce time is programmable by VIN_SHORT_DEG[2:0].

Thermal Alarm and Shutdown

The IC has a thermal protection circuit that monitors the temperature of the die. If the die temperature exceeds +155°C (T_{SHDN}), a thermal shutdown event is initiated, the IC enters the Error state, and a T_SHDN_INT interrupt is generated. After the thermal shutdown, if the die temperature reduces by 15°C, the thermal shutdown is deasserted and the user can re-enable the SCC again.

In addition to the +155°C threshold, there is an additional comparator for thermal alarm which trips at +140°C. A T_ALARM_INT interrupt is generated.

Flying Capacitor Open/Short Detection

During soft-start, the IC charges C_{FLY1} and C_{FLY2} close to the VOUT level. After charging the capacitors for t_{OPEN} (80µs typical), the IC detects the voltage of each of the C1Nx and C2Nx pins. If the voltage is lower than 0.6V (typical), a C_{FLY} open fault is detected. The soft-start terminates, the state goes to an Error state, and a CFLY_OPEN_INT interrupt is generated.

After charging the capacitors for t_{SHORT} (3ms typical by default, programmable by SS_T[2:0]), the IC also detects flying capacitor shorts by checking the voltage of the C1Nx and C2Nx pins. If the voltage is higher than 0.9V (typical), a C_{FLY} short fault is detected. The soft-start terminates, the state goes to an Error state, and a CFLY_SHORT_INT interrupt is generated.

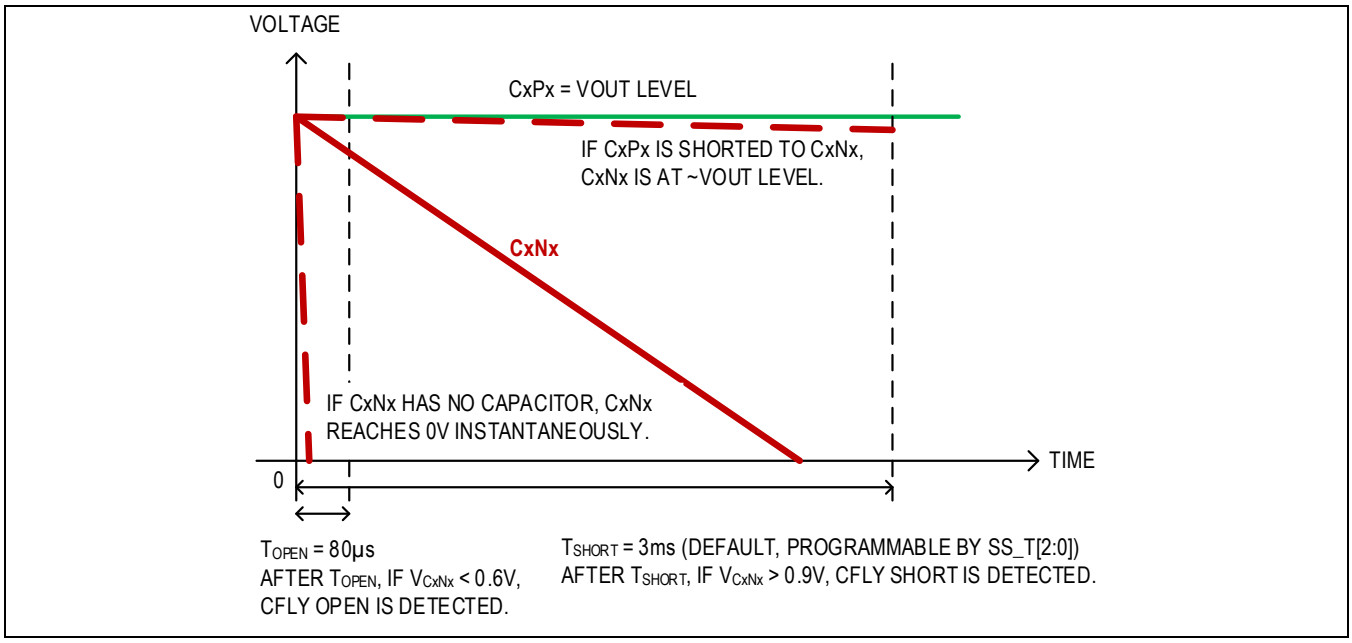


Figure 11. C_{FLY} Open/Short Detection

BST and PVDD Undervoltage Protection (BST UVP and PVDD UVP)

BSTA/B and PVDD are critical supplies for gate drivers during SCC operation. If their voltage levels are too low, the SCC stops operation and state goes to Error state. A BST_UVP_INT interrupt or PVDD_UVP_INT interrupt is generated.

Watchdog Timer

For proper battery charging, the control unit must control input voltage continuously to maintain a constant charge current. Sometimes, the control unit cannot adjust V_{VIN} on time or is stuck in an infinite software loop. The IC provides a watchdog timer function that disables the SCC operation when the timer expires. State also goes to Shutdown state. The timer can be programmed with WD_TIMER[1:0] and cleared by WDTCLR[1:0]. Note that updating the timer value does not clear the timer. Therefore, in case of changing timer value, the timer can only be cleared by WDTCLR[1:0]. In the case of updating WD_TIMER[1:0] on the fly, it must be set to OFF first and then set to the new value.

Timeout of watchdog only changes the SCC state machine. EXT1 and EXT2 gate drivers are not impacted. If a gate driver is on before watchdog timeout, and the watchdog timeout changes the SCC state to Shutdown state, triggering a reset, the gate driver remains on without interrupt (assuming turn-on condition still satisfies).

ADC

The IC has a 9-channel 12-bit ADC that monitors VIN voltage, PMID voltage, VEXT1 voltage, VEXT2 voltage, VOUT voltage, differential voltage between BATP and BATN, NTC voltage, die temperature, and input current. Users can decide which channel to monitor or skip by setting the ADC_CFG1 and ADC_CFG2 registers.

The ADC can be enabled in the Standby state and Active state. The ADC cannot be enabled in the Shutdown state and Deep Shutdown state. The ADC has two enable modes, which are configurable by ADC_EN and ADC_EN_BATTONLY.

- With ADC_EN = 1, the ADC is enabled only when $V_{VIN} > V_{VIN\_UVLO}$. This automatically disables the ADC with battery only to save power, and the AP does not need to be controlled manually. Note that, in reverse modes of the Active state, ADC_EN = 1 does not enable the ADC even with $V_{VIN} > V_{VIN\_UVLO}$, because the battery is the power source for VIN.
- With ADC_EN_BATTONLY = 1, the ADC is always enabled regardless of VIN voltage.

The number of sampling and averaging is programmable from 4 samples to 32 samples by the CONV_NUM [1:0] bitfield. The interval between adjacent burst conversions is programmable by INTERVAL[1:0].

Figure 12 shows an example of monitoring BATP – BATN, IIN, VIN, and VOUT channels (T = 1ms). At the end of each burst conversion, an ADC_EOC_INT interrupt is generated.

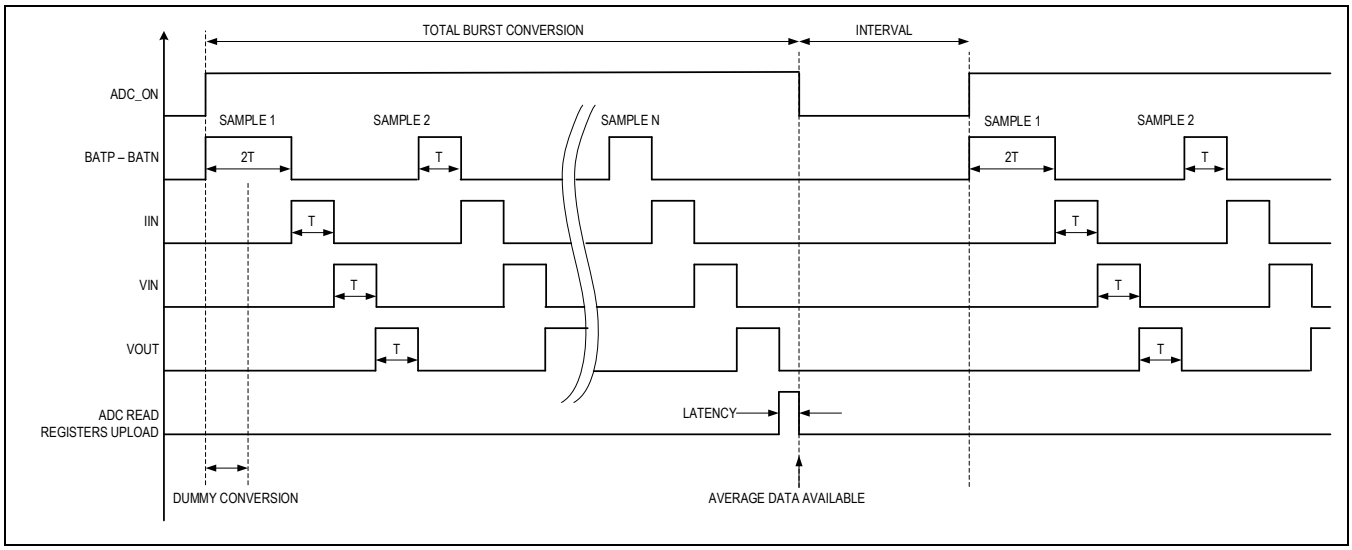


Figure 12. ADC Conversion Timing Diagram

NTC Overtemperature Alert

If temperature sensed by the onboard thermistor increases, NTC voltage decreases. User can enable an NTC overtemperature alert by setting NTC_OT_EN bit. NTC overtemperature threshold is programmable by NTC_OT_TH1 and NTC_OT_TH2 registers. An NTC_OT_INT interrupt is generated when NTC ADC readout is lower than NTC_OT_TH.

I²C Interface Description

Main I²C Interface

The IC acts as a slave transmitter/receiver and has the following slave addresses:

- If VB_EN is connected to AVDD or unconnected,
  Slave Address (7-bit) 100 0000
  Slave Address (Write) 0x80 1000 0000
  Slave Address (Read) 0x81 1000 0001
- If VB_EN is connected to AGND,
  Slave Address (7-bit) 100 1000
  Slave Address (Write) 0x90 1001 0000
  Slave Address (Read) 0x91 1001 0001

I²C Rail and Speed

The I²C block is compatible with both 1.8V rail and 1.2V rail with the VIO pin. It supports a maximum clock rate of up to 3.4MHz.

I²C Bit Transfer

One data bit is transferred for each clock pulse. The data on SDA must remain stable during the high portion of the clock pulse, as changes in data during this time are interpreted as a control signal.

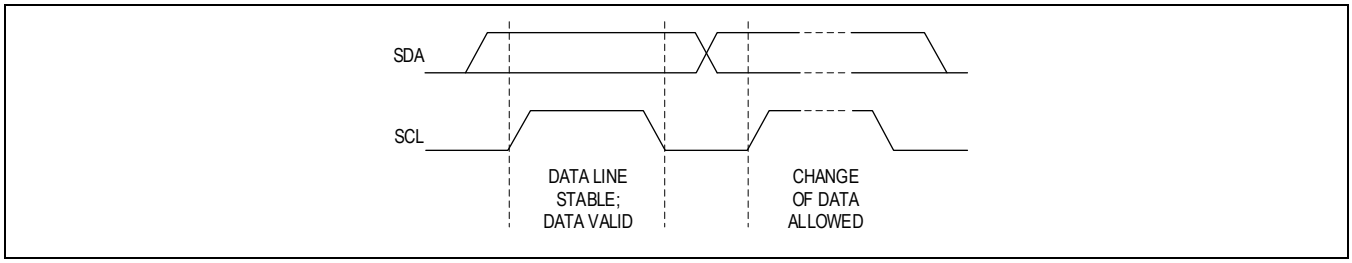


Figure 13. I²C Bit Transfer

I²C Start and Stop Conditions

Both SDA and SCL remain High when the bus is not busy. A high-to-low transition of SDA, while SCL is high is defined as the Start (S) condition. A low-to-high transition of SDA while SCL is high is defined as the Stop (P) condition.

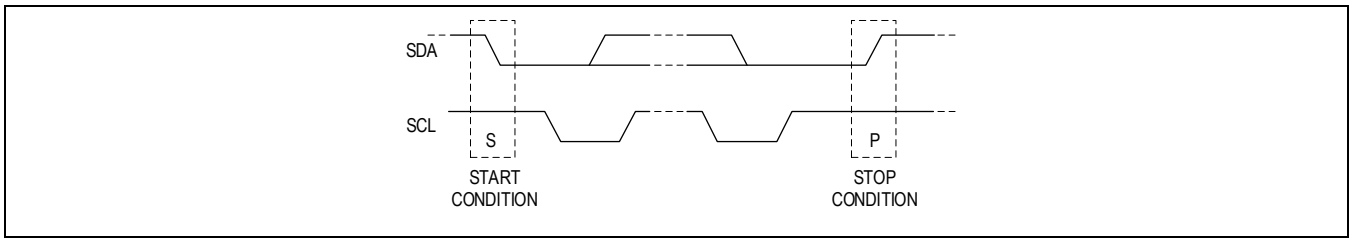


Figure 14. I²C Start and Stop

I²C System Configuration

A device on the I2C bus that generates a “message” is called a “Transmitter,” and a device that receives the message is a “Receiver”. The device that controls the message is the “Master,” and the devices that are controlled by the “Master” are called “Slaves”.

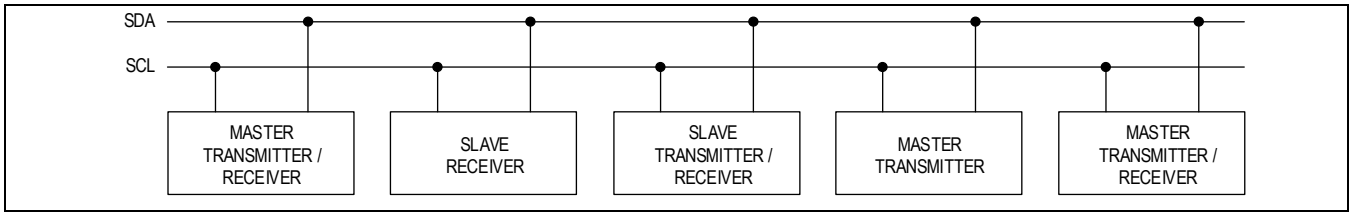


Figure 15. System Configurations

I²C Acknowledge

The number of data bytes between the start and stop conditions for the Transmitter and Receiver is unlimited.

Each 8-bit byte is followed by an Acknowledge bit. The Acknowledge bit is a high-level signal put on SDA by the transmitter during which time the master generates an extra acknowledge-related clock pulse. A slave receiver that is addressed must generate an acknowledge after each byte it receives. Also, a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge-clock pulse so that the SDA line is stable and low during the high period of the acknowledge-clock pulse (setup and hold times must also be met). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a stop condition.

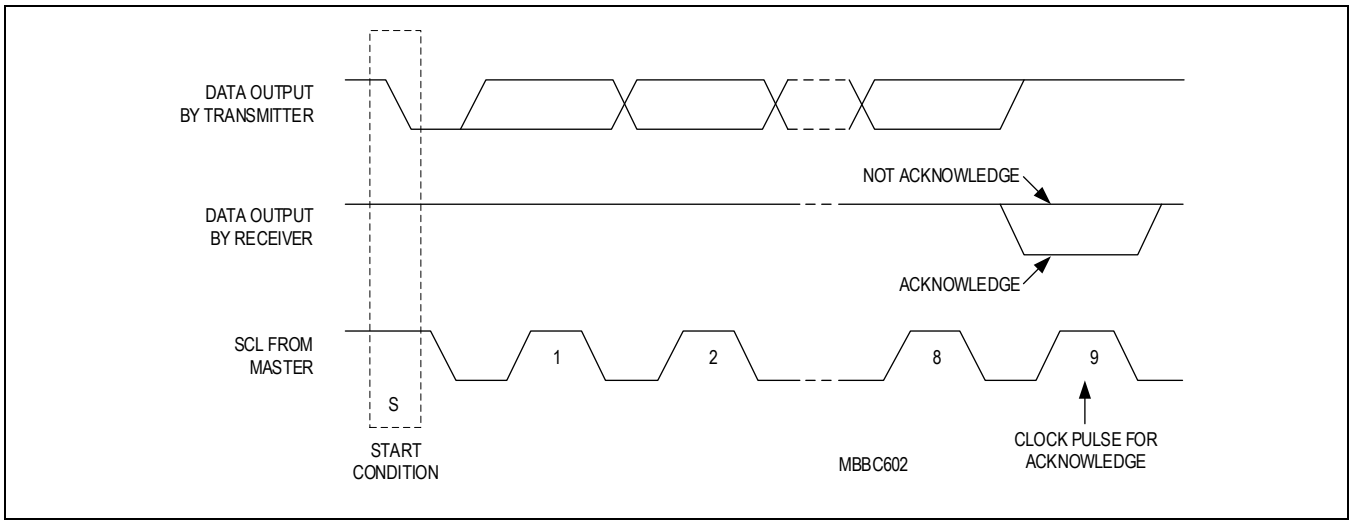


Figure 16. I²C Acknowledge

Master Transmits (Write Mode)

When the master writes to the slave, use the following format.

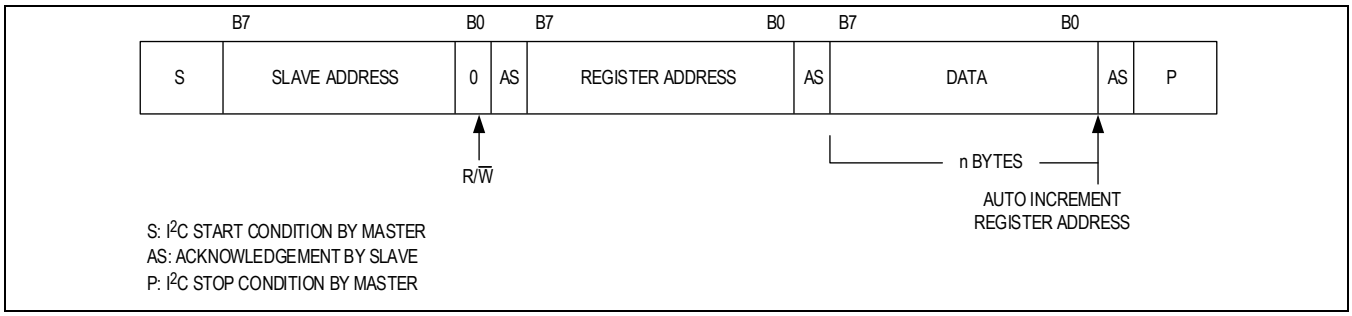


Figure 17. I²C Master Transmits

Master reads after setting the register address (Write Register Address and Read data)

To read a specific register, use the following format.

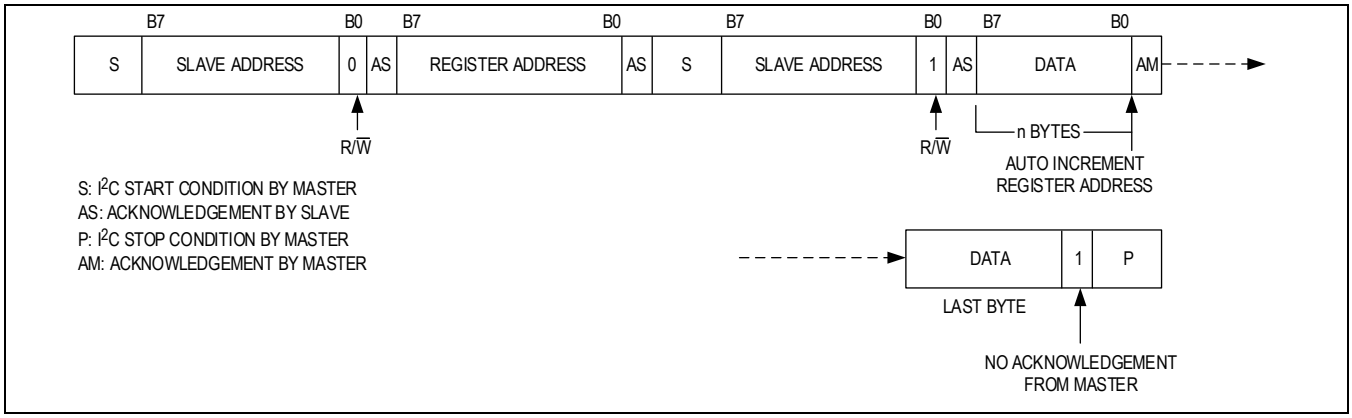


Figure 18. I²C Master Reads After Setting Register Address

Master reads register data without setting register address (Read mode)

To read registers continuously starting from the first address, use the following format.

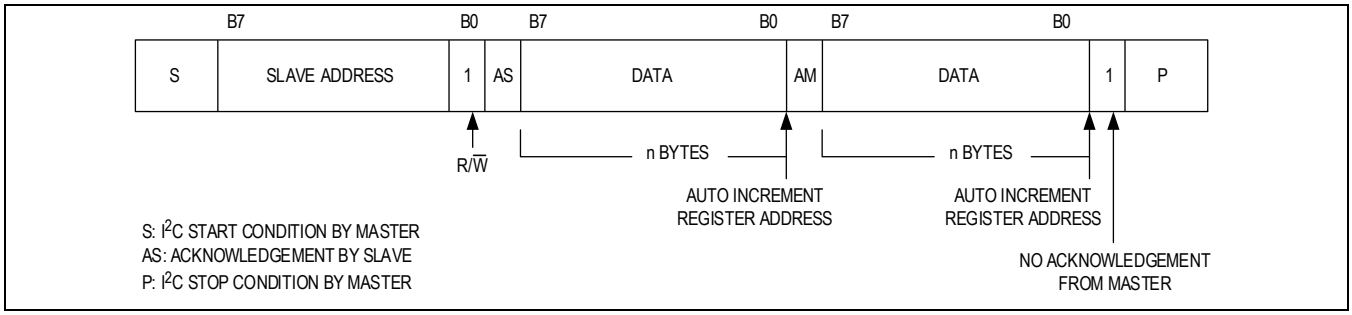


Figure 19. I²C Master Block Read

Register Map

Functional Registers

ADDRESS	NAME	MSB							LSB
Func									
0x00	Revision[7:0]	REVISION_ID[2:0]			OTP_ID[1:0]		VENDOR_ID[2:0]		
0x01	SW_RST[7:0]	SW_RST[7:0]							
0x02	INT_SRC1[7:0]	VIN_OVP_INT	VIN_UVLO_INT	VOUT_OVP_INT	VOUT_UVLO_INT	RVSBST_UVLO_INT	VBATT_OVP_INT	T_SHDN_INT	T_ALARM_INT
0x03	INT_SRC2[7:0]	CHGR_SSDONE_INT	CHGR_SS_FAULT_INT	CHGR_OCP_INT	CHGR_RCP_INT	RVSBST_SSDONE_INT	RVSBST_SS_FAULT_INT	RVSBST_OCP_INT	RVSBST_VIN_VALID_INT
0x04	INT_SRC3[7:0]	IIN_REG_INT	VBATT_REG_INT	TEMP_REG_INT	IIN_REG_TRACK_INT	REG_TIMEOUT_INT	IIN_OCP_INT	IIN_UCP_INT	VIN_SHORT_INT
0x05	INT_SRC4[7:0]	SPARE_INTSRC4_7	VEXT1_OVP_INT	VEXT1_UVLO_INT	EXT1_SW_OPEN_INT	SPARE_INTSRC4_3	VEXT2_OVP_INT	VEXT2_UVLO_INT	EXT2_SW_OPEN_INT
0x06	INT_SRC5[7:0]	PVDD_UVP_INT	CFLY_OPEN_INT	CFLY_SHORT_INT	BST_UVP_INT	ADC_EOC_INT	WT_INT	NTC_OT_INT	SPARE_INTSRC5_0
0x07	INT_SRC1_M[7:0]	VIN_OVP_M	VIN_UVLO_M	VOUT_OVP_M	VOUT_UVLO_M	RVSBST_UVLO_M	VBATT_OVP_M	T_SHDN_M	T_ALARM_M
0x08	INT_SRC2_M[7:0]	CHGR_SSDONE_M	CHGR_SS_FAULT_M	CHGR_OCP_M	CHGR_RCP_M	RVSBST_SSDONE_M	RVSBST_SS_FAULT_M	RVSBST_OCP_M	RVSBST_VIN_VALID_M
0x09	INT_SRC3_M[7:0]	IIN_REG_M	VBATT_REG_M	TEMP_REG_M	IIN_REG_TRACK_M	REG_TIMEOUT_M	IIN_OCP_M	IIN_UCP_M	VIN_SHORT_M
0x0A	INT_SRC4_M[7:0]	SPARE_INT_SRC4_M7	VEXT1_OVP_M	VEXT1_UVLO_M	EXT1_SW_OPEN_M	SPARE_INT_SRC4_M3	VEXT2_OVP_M	VEXT2_UVLO_M	EXT2_SW_OPEN_M
0x0B	INT_SRC5_M[7:0]	PVDD_UVP_M	CFLY_OPEN_M	CFLY_SHORT_M	BST_UVP_M	ADC_EOC_M	WT_M	NTC_OT_M	SPARE_INT_SRC5_M0
0x0C	STATUS1[7:0]	VIN_OVP_S	VIN_UVLO_S	VOUT_OVP_S	VOUT_UVLO_S	RVSBST_UVLO_S	SPARE_STATUS1_2	T_SHDN_S	T_ALARM_S
0x0D	STATUS2[7:0]	IIN_REG_S	VBATT_REG_S	TEMP_REG_S	SPARE_STATUS2_4_0[4:0]				
0x0E	STATUS3[7:0]	SPARE_STATUS3_7	VEXT1_OVP_S	VEXT1_UVLO_S	EXT1_SW_OPEN_S	SPARE_STATUS3_3	VEXT2_OVP_S	VEXT2_UVLO_S	EXT2_SW_OPEN_S

ADDRESS	NAME	MSB							LSB
0x10	EXT1_SW_CTRL[7:0]	EXT_SW_RVS_TURN_ON_SPEED[1:0]		VEXT1_DRV_VOLT	EXT1_DISCHG_CTRL2	EXT1_DISCHG_CTRL1	SPR_2	EXT1_SW_CTRL2	EXT1_SW_CTRL1
0x11	EXT2_SW_CTRL[7:0]	EXT_DRV_LPM_EN	SPR_6	VEXT2_DRV_VOLT	EXT2_DISCHG_CTRL2	EXT2_DISCHG_CTRL1	EXT2_GATE_CTRL	EXT2_SW_CTRL2	EXT2_SW_CTRL1
0x12	VEXT1_OVP_CFG[7:0]	SPR_7_6[1:0]		VEXT1_OVP_TH[2:0]			VEXT1_OVP_DEG[1:0]		VEXT1_OVP_EN
0x13	VEXT2_OVP_CFG[7:0]	SPR_7_6[1:0]		VEXT2_OVP_TH[2:0]			VEXT2_OVP_DEG[1:0]		VEXT2_OVP_EN
0x14	EXT1_SW_OPEN_DET_CFG[7:0]	SPR_7_5[2:0]			EXT1_SW_OPEN_DET_OFF	EXT1_SW_OPEN_DET_TH[1:0]		EXT1_SW_OPEN_DET_DEB	EXT1_SW_OPEN_DET_EN
0x15	EXT2_SW_OPEN_DET_CFG[7:0]	SPR_7_5[2:0]			EXT2_SW_OPEN_DET_OFF	EXT2_SW_OPEN_DET_TH[1:0]		EXT2_SW_OPEN_DET_DEB	EXT2_SW_OPEN_DET_EN
0x16	SCC_EN[7:0]	SCC_PH_SEL	RVSBST_VIN_VALID_EN	VIN_DISCHG_EN	STANDBY_MODE_SET	SPARE_3	OPERATION_MODE[2:0]		
0x17	FSW_CFG[7:0]	DTHR_DEPTH	DTHR	SYNC_ROLE	SYNC_EN	FREQ[3:0]			
0x18	SKIP_CFG[7:0]	ISKIP[2:0]			VSKIP[2:0]			SKIP	AUDIO
0x19	SS_CFG[7:0]	SS_I[1:0]		SS_T[2:0]			SPARE_2_0[2:0]		
0x1A	IIN_REG[7:0]	IIN_REG[6:0]							IIN_REG_EN
0x1B	IIN_REG_TRACK[7:0]	VBATT_REG_EN	SPARE_6	IIN_TRACK_CNT_NUM[3:0]				IIN_REG_TRACK_STEP	IIN_REG_TRACK_EN
0x1C	VBATT_REG[7:0]	VBATT_REG[7:0]							
0x1D	TEMP_REG[7:0]	SPARE_7_3[4:0]					TEMP_REG[2:0]		
0x1E	RT_CFG[7:0]	SYNC_OUT[1:0]		IIN_DELAY_TIMER[2:0]			REG_TIMER[2:0]		
0x1F	VIN_OVP_CFG[7:0]	SPARE_7_4[3:0]				VIN_OVP_TH[1:0]		VIN_OVP_DEG	VIN_OVP_EN
0x20	VOUT_OVP_CFG[7:0]	SPARE_7_5[2:0]			VBATT_OVP_DEG	SPARE_3	VOUT_OVP_TH	VOUT_OVP_DEG	VOUT_OVP_EN

ADDRESS	NAME	MSB							LSB
0x21	VBATT_OVP_CFG[7:0]	VBATT_OVP_TH[6:0]							VBATT_OVP_EN
0x22	CHGR_OCP_CFG[7:0]	CHGR_OCP[3:0]				CHGR_OCP_DEG[2:0]			CHGR_OCP_EN
0x23	RVSBST_OCP_CFG[7:0]	RVSBST_OCP[3:0]				RVSBST_OCP_DEG[2:0]			RVSBST_OCP_EN
0x24	CHGR_RCP_CFG[7:0]	SPARE_7	CHGR_RCP[2:0]			CHGR_RCP_DEG[2:0]			CHGR_RCP_EN
0x25	IIN_OCP_CFG[7:0]	SPARE_7	IIN_OCP[5:0]						IIN_OCP_EN
0x26	IIN_OCP_DEG_CFG[7:0]	SPARE_7_2[5:0]						IIN_OCP_DEG[1:0]	
0x27	IIN_UCP_CFG[7:0]	SPARE_7	IIN_UCP[2:0]			IIN_UCP_DEG[2:0]			IIN_UCP_EN
0x28	VIN_SHORT_CFG[7:0]	SPARE_7_6[1:0]		VIN_SHORT_TH[1:0]		VIN_SHORT_DEG[2:0]			VIN_SHORT_EN
0x29	WT_CFG[7:0]	WDTCLR[1:0]		SPARE_5_3[2:0]			WD_TIMER[1:0]		WD_TIMER_EN
0x30	ADC_EN[7:0]	SPARE_7_2[5:0]						ADC_EN_BATTONLY	ADC_EN
0x31	ADC_CFG1[7:0]	TDIE_READ_EN	NTC_READ_EN	VBATT_READ_EN	VOUT_READ_EN	VEXT2_READ_EN	VEXT1_READ_EN	PMID_READ_EN	VIN_READ_EN
0x32	ADC_CFG2[7:0]	IIN_READ_EN	NTC_OT_EN	INTERVAL[1:0]		RSVD[1:0]		CONV_NUM[1:0]	
0x33	NTC_OT_TH1[7:0]	NTC_OT_TH_11_4[7:0]							
0x34	NTC_OT_TH2[7:0]	NTC_OT_TH_3_0[3:0]				SPARE_3_0[3:0]			
0x35	ADC_VIN_READ1[7:0]	VIN_READ_11_4[7:0]							
0x36	ADC_VIN_READ2[7:0]	VIN_READ_3_0[3:0]				SPARE_3_0[3:0]			

ADDRESS	NAME	MSB							LSB
0x37	ADC_PMID_READ1[7:0]	PMID_READ_11_4[7:0]							
0x38	ADC_PMID_READ2[7:0]	PMID_READ_3_0[3:0]				SPARE_3_0[3:0]			
0x39	ADC_VEXT1_READ1[7:0]	VEXT1_READ_11_4[7:0]							
0x3A	ADC_VEXT1_READ2[7:0]	VEXT1_READ_3_0[3:0]				SPARE_3_0[3:0]			
0x3B	ADC_VEXT2_READ1[7:0]	VEXT2_READ_11_4[7:0]							
0x3C	ADC_VEXT2_READ2[7:0]	VEXT2_READ_3_0[3:0]				SPARE_3_0[3:0]			
0x3D	ADC_VOUT_READ1[7:0]	VOUT_READ_11_4[7:0]							
0x3E	ADC_VOUT_READ2[7:0]	VOUT_READ_3_0[3:0]				SPARE_3_0[3:0]			
0x3F	ADC_VBATT_READ1[7:0]	VBATT_READ_11_4[7:0]							
0x40	ADC_VBATT_READ2[7:0]	VBATT_READ_3_0[3:0]				SPARE_3_0[3:0]			
0x41	ADC_NTC_READ1[7:0]	NTC_READ_11_4[7:0]							
0x42	ADC_NTC_READ2[7:0]	NTC_READ_3_0[3:0]				SPARE_3_0[3:0]			
0x43	ADC_TDIE_READ1[7:0]	TDIE_READ_11_4[7:0]							
0x44	ADC_TDIE_READ2[7:0]	TDIE_READ_3_0[3:0]				SPARE_3_0[3:0]			
0x45	ADC_IIN_READ1[7:0]	IIN_READ_11_4[7:0]							
0x46	ADC_IIN_READ2[7:0]	IIN_READ_3_0[3:0]				SPARE_3_0[3:0]			

Register Details

Revision (0x0)

Chip Revision and OTP Register

BIT	7	6	5	4	3	2	1	0
Field	REVISION_ID[2:0]			OTP_ID[1:0]		VENDOR_ID[2:0]		
Reset	0x4			0x0		0x0		
Access Type	Read Only			Read Only		Read Only		

BITFIELD	BITS	DESCRIPTION
REVISION_ID	7:5	Revision ID
OTP_ID	4:3	OTP ID
VENDOR_ID	2:0	Vendor ID

SW_RST (0x1)

Software Reset Register

BIT	7	6	5	4	3	2	1	0
Field	SW_RST[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SW_RST	7:0	Software Reset	0xA5: O-type registers are reset. SW_RST register is auto-clear as under O-type reset control. All others: No reset

INT_SRC1 (0x2)

Interrupt Source Register 1

BIT	7	6	5	4	3	2	1	0
Field	VIN_OVP_INT	VIN_UVLO_INT	VOUT_OVP_INT	VOUT_UVLO_INT	RVSBST_UVLO_INT	VBATT_OVP_INT	T_SHDN_INT	T_ALARM_INT
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
VIN_OVP_INT	7	VIN OVP Interrupt	0x0 0x1: VIN OVP interrupt triggered
VIN_UVLO_INT	6	VIN UVLO Interrupt	0x0 0x1: VIN UVLO interrupt triggered
VOUT_OVP_INT	5	VOUT OVP Interrupt	0x0 0x1: VOUT OVP interrupt triggered
VOUT_UVLO_INT	4	VOUT UVLO Interrupt	0x0 0x1: VOUT UVLO interrupt triggered
RVSBST_UVLO_INT	3	Reverse Boost Mode VOUT Startup UVLO Interrupt	0x0 0x1: Reverse Boost Mode VOUT Startup UVLO interrupt triggered
VBATT_OVP_INT	2	Battery (BATP – BATN) OVP Interrupt	0x0 0x1: Battery OVP interrupt triggered
T_SHDN_INT	1	Thermal Shutdown (155°C) Interrupt	0x0 0x1: Thermal Shutdown (155°C) interrupt triggered
T_ALARM_INT	0	Thermal Warning (140°C) Interrupt	0x0 0x1: Thermal Warning (140°C) interrupt triggered

INT_SRC2 (0x3)

Interrupt Source Register 2

BIT	7	6	5	4	3	2	1	0
Field	CHGR_SSDONE_INT	CHGR_SS_FAULT_INT	CHGR_OCP_INT	CHGR_RCP_INT	RVSBST_SSDONE_INT	RVSBST_SS_FAULT_INT	RVSBST_OCP_INT	RVSBST_VIN_VALID_INT
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
CHGR_SSDONE_INT	7	Charging Mode Soft-start Done Interrupt	0x0 0x1: Charging Mode Soft-start Done interrupt triggered
CHGR_SS_FAULT_INT	6	Charging Mode Soft-start Fault Interrupt	0x0 0x1: Charging Mode Soft-start Fault interrupt triggered
CHGR_OCP_INT	5	Charging Mode OCP Interrupt	0x0 0x1: Charging Mode OCP interrupt triggered
CHGR_RCP_INT	4	Charging Mode RCP Interrupt	0x0 0x1: Charging Mode RCP interrupt triggered
RVSBST_SSDONE_INT	3	Reverse Boost Mode Soft-start Done Interrupt	0x0 0x1: Reverse Boost Mode Soft-start Done interrupt triggered
RVSBST_SS_FAULT_INT	2	Reverse Boost Mode Soft-start Fault Interupt	0x0 0x1: Reverse Boost Mode Soft-start Fault interupt triggered

BITFIELD	BITS	DESCRIPTION	DECODE
RVSBST_OCP_INT	1	Reverse Boost Mode OCP interrupt	0x0 0x1: Reverse Boost Mode OCP interrupt triggered
RVSBST_VIN_VALID_INT	0	Valid VIN before Reverse Boost Mode Startup Interrupt	0x0 0x1: Valid VIN before Reverse Boost Mode Startup interrupt triggered

INT_SRC3 (0x4)

Interrupt Source Register 3

BIT	7	6	5	4	3	2	1	0
Field	IIN_REG_INT	VBATT_REG_INT	TEMP_REG_INT	IIN_REG_TRACK_INT	REG_TIMEOUT_INT	IIN_OCP_INT	IIN_UCP_INT	VIN_SHORT_INT
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
IIN_REG_INT	7	Input Current Regulation Interrupt	0x0 0x1: Input Current Regulation interrupt triggered
VBATT_REG_INT	6	Battery (BATP – BATN) Voltage Regulation Interrupt	0x0 0x1: Battery Voltage Regulation interrupt triggered
TEMP_REG_INT	5	Local Die Temperature Regulation Interrupt	0x0 0x1: Local Die Temperature Regulation interrupt triggered
IIN_REG_TRACK_INT	4	Input Current Regulation Auto Tracking Interrupt	0x0 0x1: Input Current Regulation Auto Tracking interrupt triggered
REG_TIMEOUT_INT	3	Regulation Timeout Interrupt	0x0 0x1: Regulation Timeout interrupt triggered
IIN_OCP_INT	2	Input Current OCP interrupt	0x0 0x1: Input Current OCP interrupt triggered
IIN_UCP_INT	1	Input Current UCP interrupt	0x0 0x1: Input Current UCP interrupt triggered
VIN_SHORT_INT	0	VIN Short Protection Interrupt	0x0 0x1: VIN Short Protection interrupt triggered

INT_SRC4 (0x5)

Interrupt Source Register 4

BIT	7	6	5	4	3	2	1	0
Field	SPARE_INTSRC4_7	VEXT1_OVP_INT	VEXT1_UVLO_INT	EXT1_SW_OPEN_INT	SPARE_INTSRC4_3	VEXT2_OVP_INT	VEXT2_UVLO_INT	EXT2_SW_OPEN_INT

Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_INTSRC4_7	7		
VEXT1_OVP_INT	6	VEXT1 OVP Interrupt	0x0 0x1: VEXT1 OVP interrupt triggered
VEXT1_UVLO_INT	5	VEXT1 UVLO Interrupt	0x0 0x1: VEXT1 UVLO interrupt triggered
EXT1_SW_OPEN_INT	4	EXT1 SW Open Interrupt	0x0 0x1: EXT1 SW Open interrupt triggered
SPARE_INTSRC4_3	3		
VEXT2_OVP_INT	2	VEXT2 OVP Interrupt	0x0 0x1: VEXT2 OVP interrupt triggered
VEXT2_UVLO_INT	1	VEXT2 UVLO Interrupt	0x0 0x1: VEXT2 UVLO interrupt triggered
EXT2_SW_OPEN_INT	0	EXT2 SW Open Interrupt	0x0 0x1: EXT2 SW Open interrupt triggered

INT_SRC5 (0x6)

Interrupt Source Register 5

BIT	7	6	5	4	3	2	1	0
Field	PVDD_UVP_INT	CFLY_OPEN_INT	CFLY_SHORT_INT	BST_UVP_INT	ADC_EOC_INT	WT_INT	NTC_OT_INT	SPARE_INTSRC5_0
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
PVDD_UVP_INT	7	PVDD UVP Interrupt	0x0 0x1: PVDD UVP interrupt triggered
CFLY_OPEN_INT	6	Flying Capacitor Open Interrupt	0x0 0x1: Flying Capacitor Open interrupt triggered
CFLY_SHORT_INT	5	Flying Capacitor Short Interrupt	0x0 0x1: Flying Capacitor Short interrupt triggered
BST_UVP_INT	4	Bootstrap Capacitor UVP Interrupt	0x0 0x1: Bootstrap Capacitor UVP interrupt triggered
ADC_EOC_INT	3	ADC Read Done Interrupt	0x0 0x1: ADC Read Done interrupt triggered
WT_INT	2	Watchdog Timer Interrupt	0x0 0x1: Watchdog Timer interrupt triggered

BITFIELD	BITS	DESCRIPTION	DECODE
NTC_OT_INT	1	NTC Overtemperature Interrupt	0x0 0x1: NTC Overtemperature interrupt triggered
SPARE_INTSRC5_0	0		

INT_SRC1_M (0x7)

Interrupt Source Mask Register 1

BIT	7	6	5	4	3	2	1	0
Field	VIN_OVP_M	VIN_UVLO_M	VOUT_OVP_M	VOUT_UVLO_M	RVSBST_UVLO_M	VBATT_OVP_M	T_SHDN_M	T_ALARM_M
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VIN_OVP_M	7	VIN OVP Interrupt Mask	0x0: Enable VIN_OVP_INT 0x1: Mask VIN_OVP_INT
VIN_UVLO_M	6	VIN UVLO Interrupt Mask	0x0: Enable VIN_UVLO_INT 0x1: Mask VIN_UVLO_INT
VOUT_OVP_M	5	VOUT OVP Interrupt Mask	0x0: Enable VOUT_OVP_INT 0x1: Mask VOUT_OVP_INT
VOUT_UVLO_M	4	VOUT UVLO Interrupt Mask	0x0: Enable VOUT_UVLO_INT 0x1: Mask VOUT_UVLO_INT
RVSBST_UVLO_M	3	Reverse Boost Mode VOUT Startup UVLO Interrupt Mask	0x0: Enable RVSBST_UVLO_INT 0x1: Mask RVSBST_UVLO_INT
VBATT_OVP_M	2	Battery (BATP – BATN) OVP Interrupt Mask	0x0: Enable VBATT_OVP_INT 0x1: Mask VBATT_OVP_INT
T_SHDN_M	1	Thermal Shutdown Interrupt Mask	0x0: Enable T_SHDN_INT 0x1: Mask T_SHDN_INT
T_ALARM_M	0	Thermal Alarm Interrupt Mask	0x0: Enable T_ALARM_INT 0x1: Mask T_ALARM_INT

INT_SRC2_M (0x8)

Interrupt Source Mask Register 2

BIT	7	6	5	4	3	2	1	0
Field	CHGR_SSDONE_M	CHGR_SS_FAULT_M	CHGR_OCP_M	CHGR_RCP_M	RVSBST_SSDONE_M	RVSBST_SS_FAULT_M	RVSBST_OCP_M	RVSBST_VIN_VALID_M
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CHGR_SSDONE_M	7	Charging Mode Soft-start Done Interrupt Mask	0x0: Enable CHGR_SSDONE_INT 0x1: Mask CHGR_SSDONE_INT
CHGR_SS_FAULT_M	6	Charging Mode Soft-start Fault Mask	0x0: Enable CHGR_SS_FAULT_INT 0x1: Mask CHGR_SS_FAULT_INT
CHGR_OCP_M	5	Charging Mode OCP Interrupt Mask	0x0: Enable CHGR_OCP_INT 0x1: Mask CHGR_OCP_INT
CHGR_RCP_M	4	Charging Mode RCP Interrupt Mask	0x0: Enable CHGR_RCP_INT 0x1: Mask CHGR_RCP_INT
RVSBST_SSDONE_M	3	Reverse Boost Soft-start Done Interrupt Mask	0x0: Enable RVSBST_SSDONE_INT 0x1: Mask RVSBST_SSDONE_INT
RVSBST_SS_FAULT_M	2	Reverse Boost Mode Soft-start Fault Interrupt Mask	0x0: Enable RVSBST_SS_FAULT_INT 0x1: Mask RVSBST_SS_FAULT_INT
RVSBST_OCP_M	1	Reverse Boost Mode OCP Interrupt Mask	0x0: Enable RVSBST_OCP_INT 0x1: Mask RVSBST_OCP_INT
RVSBST_VIN_VALID_M	0	Valid VIN before Reverse Boost Mode Startup Interrupt Mask	0x0: Enable RVSBST_VIN_VALID_INT 0x1: Mask RVSBST_VIN_VALID_INT

INT_SRC3_M (0x9)

Interrupt Source Mask Register 3

BIT	7	6	5	4	3	2	1	0
Field	IIN_REG_M	VBATT_REG_M	TEMP_REG_M	IIN_REG_TRACK_M	REG_TIMEOUT_M	IIN_OCP_M	IIN_UCP_M	VIN_SHORT_M
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IIN_REG_M	7	Input Current Regulation Interrupt Mask	0x0: Enable IIN_REG_INT 0x1: Mask IIN_REG_INT
VBATT_REG_M	6	Battery (BATP – BATN) Voltage Regulation Interrupt Mask	0x0: Enable VBATT_REG_INT 0x1: Mask VBATT_REG_INT
TEMP_REG_M	5	Local Die Temperature Regulation Interrupt Mask	0x0: Enable TEMP_REG_INT 0x1: Mask TEMP_REG_INT
IIN_REG_TRACK_M	4	Input Current Regulation Auto Tracking Interrupt Mask	0x0: Enable IIN_REG_TRACK_INT 0x1: Mask IIN_REG_TRACK_INT
REG_TIMEOUT_M	3	Regulation Timeout Interrupt Mask	0x0: Enable REG_TIMEOUT_INT 0x1: Mask REG_TIMEOUT_INT
IIN_OCP_M	2	Input Current OCP Interrupt Mask	0x0: Enable IIN_OCP_INT 0x1: Mask IIN_OCP_INT
IIN_UCP_M	1	Input Current UCP Interrupt Mask	0x0: Enable IIN_UCP_INT 0x1: Mask IIN_UCP_INT
VIN_SHORT_M	0	VIN Short Protection Interrupt Mask	0x0: Enable VIN_SHORT_INT 0x1: Mask VIN_SHORT_INT

INT_SRC4_M (0xA)

Interrupt Source Mask Register 4

BIT	7	6	5	4	3	2	1	0
Field	SPARE_INT_SRC4_M7	VEXT1_OVP_M	VEXT1_UVLO_M	EXT1_SW_OPEN_M	SPARE_INT_SRC4_M3	VEXT2_OVP_M	VEXT2_UVLO_M	EXT2_SW_OPEN_M
Reset	0x0	0x0	0x1	0x0	0x0	0x0	0x1	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_INT_SRC4_M7	7		
VEXT1_OVP_M	6	VEXT1 OVP Interrupt Mask	0x0: Enable VEXT1_OVP_INT 0x1: Mask VEXT1_OVP_INT
VEXT1_UVLO_M	5	VEXT1 UVLO Interrupt Mask	0x0: Enable VEXT1_UVLO_INT 0x1: Mask VEXT1_UVLO_INT
EXT1_SW_OPEN_M	4	EXT1 SW Open Interrupt Mask	0x0: Enable EXT1_SW_OPEN_INT 0x1: Mask EXT1_SW_OPEN_INT
SPARE_INT_SRC4_M3	3		
VEXT2_OVP_M	2	VEXT2 OVP Interrupt Mask	0x0: Enable VEXT2_OVP_INT 0x1: Mask VEXT2_OVP_INT
VEXT2_UVLO_M	1	VEXT2 UVLO Interrupt Mask	0x0: Enable VEXT2_UVLO_INT 0x1: Mask VEXT2_UVLO_INT
EXT2_SW_OPEN_M	0	EXT2 SW Open Interrupt Mask	0x0: Enable EXT2_SW_OPEN_INT 0x1: Mask EXT2_SW_OPEN_INT

INT_SRC5_M (0xB)

Interrupt Source Mask Register 5

BIT	7	6	5	4	3	2	1	0
Field	PVDD_UVP_M	CFLY_OPEN_M	CFLY_SHORT_M	BST_UVP_M	ADC_EOC_M	WT_M	NTC_OT_M	SPARE_INT_SRC5_M0
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PVDD_UVP_M	7	PVDD UVP Interrupt Mask	0x0: Enable PVDD_UVP_INT 0x1: Enable PVDD_UVP_INT
CFLY_OPEN_M	6	Flying Capacitor Open Interrupt Mask	0x0: Enable CFLY_OPEN_INT 0x1: Mask CFLY_OPEN_INT
CFLY_SHORT_M	5	Flying Capacitor Short Interrupt Mask	0x0: Enable CFLY_SHORT_INT 0x1: Enable CFLY_SHORT_INT

BITFIELD	BITS	DESCRIPTION	DECODE
BST_UVP_M	4	Bootstrap Capacitor UVP Interrupt Mask	0x0: Enable BST_UVP_INT 0x1: Enable BST_UVP_INT
ADC_EOC_M	3	ADC Read Done Interrupt Mask	0x0: Enable ADC_READ_DONE_INT 0x1: Mask ADC_READ_DONE_INT
WT_M	2	Watchdog Timer Interrupt Mask	0x0: Enable WT_INT 0x1: Mask WT_INT
NTC_OT_M	1	NTC Overtemperature Interrupt Mask	0x0: Enable NTC_OT_INT 0x1: Mask NTC_OT_INT
SPARE_INT_SRC5_M0	0		

STATUS1 (0xC)

Status Register 1

BIT	7	6	5	4	3	2	1	0
Field	VIN_OVP_S	VIN_UVLO_S	VOUT_OVP_S	VOUT_UVLO_S	RVSBST_UVLO_S	SPARE_STATUS1_2	T_SHDN_S	T_ALARM_S
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VIN_OVP_S	7	VIN OVP Status	0x0: VIN < VIN_OVLO 0x1: VIN ≥ VIN_OVLO
VIN_UVLO_S	6	VIN UVLO Status	0x0: VIN > VIN_UVLO 0x1: VIN ≤ VIN_UVLO
VOUT_OVP_S	5	VOUT OVP Status	0x0: VOUT < VOUT_OVLO 0x1: VOUT ≥ VOUT_OVLO
VOUT_UVLO_S	4	VOUT UVLO Status	0x0: VOUT > VOUT_UVLO 0x1: VOUT ≤ VOUT_UVLO
RVSBST_UVLO_S	3	Reverse Boost Mode VOUT Startup UVLO Status	0x0: VOUT > VOUT_UVLO_RVS_SS 0x1: VOUT ≤ VOUT_UVLO_RVS_SS
SPARE_STATUS1_2	2		
T_SHDN_S	1	Thermal Shutdown Status	0x0: Junction temperature (T_J) < 155°C 0x1: Junction temperature (T_J) ≥ 155°C
T_ALARM_S	0	Thermal Alarm Status	0x0: Junction temperature (T_J) < 140°C 0x1: Junction temperature (T_J) ≥ 140°C

STATUS2 (0xD)

Status Register 2

BIT	7	6	5	4	3	2	1	0
Field	IIN_REG_S	VBATT_REG_S	TEMP_REG_S	SPARE_STATUS2_4_0[4:0]				
Reset	0x0	0x0	0x0	0x00				

Access Type	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
IIN_REG_S	7	Input Current Regulation Status	0x0: Input current is not being regulated 0x1: Input current is being regulated by IIN_REG[6:0]
VBATT_REG_S	6	Battery (BATP – BATN) Voltage Regulation Status	0x0: Battery voltage is not being regulated 0x1: Battery voltage is being regulated by VBATT_REG[7:0]
TEMP_REG_S	5	Local Die Temperature Regulation Status	0x0: Local die temperature is not being regulated 0x1: Local die temperature is being regulated by TEMP_REG[2:0]
SPARE_STATUS2_4_0	4:0		

STATUS3 (0xE)

Status Register 3

BIT	7	6	5	4	3	2	1	0
Field	SPARE_STATUS3_7	VEXT1_OVP_S	VEXT1_UVLO_S	EXT1_SW_OPEN_S	SPARE_STATUS3_3	VEXT2_OVP_S	VEXT2_UVLO_S	EXT2_SW_OPEN_S
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_STATUS3_7	7		
VEXT1_OVP_S	6	VEXT1 OVP Status	0x0: VEXT1 < VEXT1_OVLO 0x1: VEXT1 ≥ VEXT1_OVLO
VEXT1_UVLO_S	5	VEXT1 UVLO Status	0x0: VEXT1 > VEXT_UVLO 0x1: VEXT1 ≤ VEXT_UVLO
EXT1_SW_OPEN_S	4	EXT1 SW Open Status	0x0: VEXT1 - VIN < VOPEN_DET_EXT_SW or EXT1 SW Open Detection is disabled 0x1: VEXT1 - VIN ≥ VOPEN_DET_EXT_SW
SPARE_STATUS3_3	3		
VEXT2_OVP_S	2	VEXT2 OVP Status	0x0: VEXT2 < VEXT2_OVLO 0x1: VEXT2 ≥ VEXT2_OVLO
VEXT2_UVLO_S	1	VEXT2 UVLO Status	0x0: VEXT2 > VEXT_UVLO 0x1: VEXT2 ≤ VEXT_UVLO
EXT2_SW_OPEN_S	0	EXT2 SW Open Status	0x0: VEXT2 - VIN < VOPEN_DET_EXT_SW or EXT2 SW Open Detection is disabled 0x1: VEXT2 - VIN ≥ VOPEN_DET_EXT_SW

EXT1_SW_CTRL (0x10)

EXT1 Switch Control Register

BIT	7	6	5	4	3	2	1	0
Field	EXT_SW_RVS_TURN_ON_SPEED[1:0]		VEXT1_DRV_VOLT	EXT1_DISCHG_CTRL2	EXT1_DISCHG_CTRL1	SPR_2	EXT1_SW_CTRL2	EXT1_SW_CTRL1
Reset	0x2		0x0	0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EXT_SW_RVS_TURN_ON_SPEED	7:6	EXT Switch Turn-on Speed Control for Reverse Mode. Applies to both VEXT1_DRV and VEXT2_DRV.	0x0: Very fast 0x1: Fast 0x2: Medium 0x3: Slow
VEXT1_DRV_VOLT	5	VEXT1_DRV Gate Drive Voltage Selection	0x0: Low VEXT1_DRV gate drive voltage for GaN FET 0x1: High VEXT1_DRV gate drive voltage for MOSFET(s)
EXT1_DISCHG_CTRL2	4	EXT1 Active Discharge Enable Reset	0x0: Do not reset EXT1_DISCHG_CTRL1. 0x1: Reset EXT1_DISCHG_CTRL1 to 0x0 when VEXT1 falls below 0.3V.
EXT1_DISCHG_CTRL1	3	EXT1 Active Discharge Enable. This bit is reset to 0x0 when VEXT1 falls below 0.3V and EXT1_DISCHG_CTRL2 = 0x1.	0x0: Disable EXT1 active discharge 0x1: Enable EXT1 active discharge
SPR_2	2		
EXT1_SW_CTRL2	1	EXT1 Switch Enable in Manual Mode. This bit is valid only when EXT1_SW_CTRL1 = 0 (manual mode). This bit is reset to 0x0 when fault of VIN_UVLO (reverse modes) or VEXT1_UVLO (all other states) occurs.	0x0: Disable EXT1 switch in Manual mode 0x1: Enable EXT1 switch in Manual mode
EXT1_SW_CTRL1	0	EXT1 Switch Auto Mode Enable	0x0: Manual mode 0x1: Auto mode

EXT2_SW_CTRL (0x11)

EXT2 Switch Control Register

BIT	7	6	5	4	3	2	1	0
Field	EXT_DRV_LPM_EN	SPR_6	VEXT2_DRV_VOLT	EXT2_DISCHG_CTRL2	EXT2_DISCHG_CTRL1	EXT2_GATE_CTRL	EXT2_SW_CTRL2	EXT2_SW_CTRL1
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EXT_DRV_LPM_EN	7	Gate Driver Low Power Mode in Non-Active States Enable. Applies to both VEXT1_DRV and VEXT2_DRV.	0x0: Disable low power mode 0x1: Enable low power mode
SPR_6	6		
VEXT2_DRV_VOLT	5	VEXT2_DRV Gate Drive Voltage Selection	0x0: Low VEXT2_DRV gate drive voltage for GaN FET 0x1: High VEXT2_DRV gate drive voltage for MOSFET(s)
EXT2_DISCHG_CTRL2	4	EXT2 Active Discharge Enable Reset	0x0: Do not reset EXT2_DISCHG_CTRL1. 0x1: Reset EXT2_DISCHG_CTRL1 to 0x0 when VEXT2 falls below 0.3V.
EXT2_DISCHG_CTRL1	3	EXT2 Active Discharge Enable. This bit is reset to 0x0 when VEXT2 falls below 0.3V and EXT2_DISCHG_CTRL2 = 0x1.	0x0: Disable EXT2 active discharge 0x1: Enable EXT2 active discharge
EXT2_GATE_CTRL	2	EXT2_DRV Gate Select	0x0: External switch. Default value if VB_EN = Low or Unconnected. 0x1: Internal VB FET. Default value if VB_EN = High.
EXT2_SW_CTRL2	1	EXT2 Switch Enable in Manual Mode. This bit is valid only when EXT2_SW_CTRL1 = 0 (manual mode). This bit is reset to 0x0 when fault of VIN_UVLO (reverse modes) or VEXT2_UVLO (all other states) occurs.	0x0: Disable EXT2 switch in Manual mode 0x1: Enable EXT2 switch in Manual mode
EXT2_SW_CTRL1	0	EXT2 Switch Auto Mode Enable	0x0: Manual mode. Default value if VB_EN = Low or Unconnected. 0x1: Auto mode. Default value if VB_EN = High.

VEXT1_OVP_CFG (0x12)

VEXT1 Overvoltage Protection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_6[1:0]		VEXT1_OVP_TH[2:0]			VEXT1_OVP_DEG[1:0]		VEXT1_OVP_EN
Reset	0x0		0x2			0x0		0x1
Access Type	Write, Read		Write, Read			Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_6	7:6		
VEXT1_OVP_TH	5:3	VEXT1 OVP Threshold (V)	0x0: 6.5 0x1: 13 0x2: 13.5 0x3: 17 0x4: 17.5 0x5: 18 0x6: 18.5 0x7: 19
VEXT1_OVP_DEG	2:1	VEXT1 OVP Deglich Time	0x0: No extra deglitch 0x1: 100µs 0x2: 20ms 0x3: 100ms
VEXT1_OVP_EN	0	VEXT1 OVP Enable	0x0: Disable VEXT1 OVP 0x1: Enable VEXT1 OVP

VEXT2_OVP_CFG (0x13)

VEXT2 Overvoltage Protection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_6[1:0]		VEXT2_OVP_TH[2:0]			VEXT2_OVP_DEG[1:0]		VEXT2_OVP_EN
Reset	0x0		0x2			0x0		0x1
Access Type	Write, Read		Write, Read			Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_6	7:6		
VEXT2_OVP_TH	5:3	VEXT2 OVP Threshold (V)	0x0: 6.5 0x1: 13 0x2: 13.5 0x3: 17 0x4: 17.5 0x5: 18 0x6: 18.5 0x7: 19
VEXT2_OVP_DEG	2:1	VEXT2 OVP Deglich Time	0x0: No extra deglitch 0x1: 100µs 0x2: 20ms 0x3: 100ms
VEXT2_OVP_EN	0	VEXT2 OVP Enable	0x0: Disable VEXT2 OVP 0x1: Enable VEXT2 OVP

EXT1_SW_OPEN_DET_CFG (0x14)

EXT1 Switch Open Detection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_5[2:0]			EXT1_SW_OPEN_DET_OFF	EXT1_SW_OPEN_DET_TH[1:0]		EXT1_SW_OPEN_DET_DEB	EXT1_SW_OPEN_DET_EN
Reset	0x0			0x0	0x0		0x0	0x1
Access Type	Write, Read			Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_5	7:5		
EXT1_SW_OPEN_DET_OFF	4	EXT1 Switch Open Detection Auto Disable	0x0: Auto disable EXT1 Switch Open Detection 200ms after switch turn-on 0x1: Keep EXT1 Switch Open Detection always enabled after switch turn-on
EXT1_SW_OPEN_DET_TH	3:2	EXT1 Switch Open Detection Threshold (V)	0x0: 0.5 0x1: 1 0x2: 2 0x3: 3

BITFIELD	BITS	DESCRIPTION	DECODE
EXT1_SW_OPEN_DET_DEB	1	EXT1 Switch Open Detection Debounce Time (ms)	0x0: 20 0x1: 100
EXT1_SW_OPEN_DET_EN	0	EXT1 Switch Open Detection Enable	0x0: Disable EXT1 Switch Open Detection 0x1: Enable EXT1 Switch Open Detection

EXT2_SW_OPEN_DET_CFG (0x15)

EXT2 Switch Open Detection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_5[2:0]			EXT2_SW_OPEN_DET_OFF	EXT2_SW_OPEN_DET_TH[1:0]		EXT2_SW_OPEN_DET_DEB	EXT2_SW_OPEN_DET_EN
Reset	0x0			0x0	0x0		0x0	0x1
Access Type	Write, Read			Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_5	7:5		
EXT2_SW_OPEN_DET_OFF	4	EXT2 Switch Open Detection Auto Disable	0x0: Auto disable EXT2 Switch Open Detection 200ms after switch turn-on 0x1: Keep EXT2 Switch Open Detection always enabled after switch turn-on
EXT2_SW_OPEN_DET_TH	3:2	EXT2 Switch Open Detection Threshold (V)	0x0: 0.5 0x1: 1 0x2: 2 0x3: 3
EXT2_SW_OPEN_DET_DEB	1	EXT2 Switch Open Detection Debounce Time (ms)	0x0: 20 0x1: 100
EXT2_SW_OPEN_DET_EN	0	EXT2 Switch Open Detection Enable	0x0: Disable EXT2 Switch Open Detection 0x1: Enable EXT2 Switch Open Detection

SCC_EN (0x16)

SCC Enable Register

BIT	7	6	5	4	3	2	1	0
Field	SCC_PH_SEL	RVSBST_VIN_VALID_EN	VIN_DISCHG_EN	STANDBY_MODE_SET	SPARE_3	OPERATION_MODE[2:0]		
Reset	0x0	0x0	0x0	0x0	0x0	0x0		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SCC_PH_SEL	7	Frequency Synchronization Clock Phase Shift by Master (degree)	0x0: 90 0x1: 180
RVSBST_VIN_VALID_EN	6	Valid VIN before Reverse Boost Mode Startup Enable	0x0: Disable valid VIN detection 0x1: Enable valid VIN detection
VIN_DISCHG_EN	5	VIN Active Discharge Enable for Standby State	0x0: Always disable VIN active discharge in Standby state 0x1: Always enable VIN active discharge in Standby state
STANDBY_MODE_SET	4	Standby State Control. This bitfield is valid only in Shutdown and Standby states. This bitfield is not reset by O-type reset.	0x0: Shutdown State 0x1: Standby State
SPARE_3	3		
OPERATION_MODE	2:0	Active State Mode Control. This bitfield is valid only in Standby and Active states.	0x0: Standby State 0x1: Forward 3:1 Mode 0x2: Forward 2:1 Mode 0x3: Forward 1:1 Mode 0x4: Reverse 1:1 Mode 0x5: Reverse 1:2 Mode 0x6: Reverse 1:3 Mode

FSW_CFG (0x17)

Swichting Frequency Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	DTHR_DEPTH	DTHR	SYNC_ROLE	SYNC_EN	FREQ[3:0]			
Reset	0x0	0x0	0x0	0x0	0x7			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
DTHR_DEPTH	7	Frequency Dithering Depth	0x0: 3% 0x1: 6%
DTHR	6	Frequency Dithering	0x0: Disable frequency dithering 0x1: Enable frequency dithering
SYNC_ROLE	5	Frequency Synchronization Role Configuration	0x0: Slave (receive clock on SYNC) 0x1: Master (send clock on SYNC)
SYNC_EN	4	Frequency Synchronization Enable	0x0: Disable frequency synchronization 0x1: Enable frequency synchronization
FREQ	3:0	Switching Frequency (kHz)	0x0: 200 0x1: 300 0x2: 400 0x3: 500 0x4: 600 0x5: 666 0x6: 750 0x7: 857 0x8: 1000 0x9: 1200 0xA: 1500

SKIP_CFG (0x18)

Skip Mode Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	ISKIP[2:0]			VSKIP[2:0]			SKIP	AUDIO
Reset	0x3			0x4			0x1	0x0
Access Type	Write, Read			Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ISKIP	7:5	Skip Mode Current Threshold (mA)	0x0: 100 0x1: 200 0x2: 300 0x3: 400 0x4: 500 0x5: 600 0x6: 700 0x7: 800
VSKIP	4:2	Skip Mode Voltage Threshold (mV). Defined as VOUT – PMID / N, where N is the conversion ratio.	0x0: 10 0x1: 20 0x2: 40 0x3: 60 0x4: 80 0x5: 100 0x6: 120 0x7: 140
SKIP	1	Skip Mode Enable	0x0: Disable Skip mode, Fixed-Frequency 0x1: Enable Skip mode, Auto-Skip
AUDIO	0	Audio Mode Enable	0x0: Minimum SKIP Frequency not bounded 0x1: Minimum SKIP Frequency bounded at 20kHz

SS_CFG (0x19)

Soft-start Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SS_I[1:0]		SS_T[2:0]			SPARE_2_0[2:0]		
Reset	0x1		0x2			0x0		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SS_I	7:6	Soft-start Current (mA)	0x0: 50 0x1: 100 0x2: 100 0x3: 100
SS_T	5:3	Flying Capacitor Open/Short Detection Timer (ms)	0x0: 1 0x1: 2 0x2: 3 0x3: 4 0x4: 5 0x5: 6

BITFIELD	BITS	DESCRIPTION	DECODE
			0x6: 7 0x7: 8
SPARE_2_0	2:0		

IIN_REG (0x1A)

Input Current Regulation Threshold Register

BIT	7	6	5	4	3	2	1	0
Field	IIN_REG[6:0]							IIN_REG_EN
Reset	0x00							0x1
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IIN_REG	7:1	Input Current Regulation Threshold (mA)	0x00: 500 0x01: 550 0x02: 600 0x03: 650 0x04: 700 0x05: 750 0x06: 800 0x07: 850 0x08: 900 0x09: 950 0x0A: 1000 0x0B: 1050 0x0C: 1100 0x0D: 1150 0x0E: 1200 0x0F: 1250 0x10: 1300 0x11: 1350 0x12: 1400 0x13: 1450 0x14: 1500 0x15: 1550 0x16: 1600 0x17: 1650 0x18: 1700 0x19: 1750 0x1A: 1800 0x1B: 1850 0x1C: 1900 0x1D: 1950 0x1E: 2000 0x1F: 2050 0x20: 2100 0x21: 2150 0x22: 2200 0x23: 2250 0x24: 2300 0x25: 2350 0x26: 2400 0x27: 2450 0x28: 2500 0x29: 2550 0x2A: 2600 0x2B: 2650

BITFIELD	BITS	DESCRIPTION	DECODE
			0x2C: 2700 0x2D: 2750 0x2E: 2800 0x2F: 2850 0x30: 2900 0x31: 2950 0x32: 3000 0x33: 3050 0x34: 3100 0x35: 3150 0x36: 3200 0x37: 3250 0x38: 3300 0x39: 3350 0x3A: 3400 0x3B: 3450 0x3C: 3500 0x3D: 3550 0x3E: 3600 0x3F: 3650 0x40: 3700 0x41: 3750 0x42: 3800 0x43: 3850 0x44: 3900 0x45: 3950 0x46: 4000 0x47: 4050 0x48: 4100 0x49: 4150 0x4A: 4200 0x4B: 4250 0x4C: 4300 0x4D: 4350 0x4E: 4400 0x4F: 4450 0x50: 4500 0x51: 4550 0x52: 4600 0x53: 4650 0x54: 4700 0x55: 4750 0x56: 4800 0x57: 4850 0x58: 4900 0x59: 4950 0x5A: 5000 0x5B: 5050 0x5C: 5100 0x5D: 5150 0x5E: 5200 0x5F: 5250 0x60: 5300 0x61: 5350 0x62: 5400 0x63: 5450 0x64: 5500
IIN_REG_EN	0	Input Current Regulation Enable	0x0: Disable input current regulation 0x1: Enable input current regulation

IIN_REG_TRACK (0x1B)

Input Current Regulation Auto Tracking Register

BIT	7	6	5	4	3	2	1	0

Field	VBATT_REG_EN	SPARE_6	IIN_TRACK_CNT_NUM[3:0]	IIN_REG_TRACK_STEP	IIN_REG_TRACK_EN
Reset	0x1	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VBATT_REG_EN	7	Battery (BATP – BATN) Voltage Regulation Enable	0x0: Disable battery (BATP – BATN) voltage regulation 0x1: Enable battery (BATP – BATN) voltage regulation
SPARE_6	6		
IIN_TRACK_CNT_NUM	5:2	Input Current Regulation Auto Tracking Counter	0x0: 1 0x1: 1 0x2: 2 0x3: 3 0x4: 4 0x5: 5 0x6: 6 0x7: 7 0x8: 8 0x9: 9 0xA: 10 0xB: 11 0xC: 12 0xD: 13 0xE: 14 0xF: 15
IIN_REG_TRACK_STEP	1	Input Current Regulation Auto Tracking Step (mA)	0x0: 200 0x1: 300
IIN_REG_TRACK_EN	0	Input Current Regulation Auto Tracking Enable	0x0: Disable input current regulation auto tracking 0x1: Enable input current regulation auto tracking

VBATT_REG (0x1C)

Battery (BATP – BATN) Voltage Regulation Threshold Register

BIT	7	6	5	4	3	2	1	0
Field	VBATT_REG[7:0]							
Reset	0x78							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VBATT_REG	7:0	Battery (BATP – BATN) Voltage Regulation Threshold (V)	0x00: 3.8 0x01: 3.805 0x02: 3.81 0x03: 3.815 0x04: 3.82 0x05: 3.825 0x06: 3.83 0x07: 3.835 0x08: 3.84

BITFIELD	BITS	DESCRIPTION	DECODE
			0x09: 3.845 0x0A: 3.85 0x0B: 3.855 0x0C: 3.86 0x0D: 3.865 0x0E: 3.87 0x0F: 3.875 0x10: 3.88 0x11: 3.885 0x12: 3.89 0x13: 3.895 0x14: 3.9 0x15: 3.905 0x16: 3.91 0x17: 3.915 0x18: 3.92 0x19: 3.925 0x1A: 3.93 0x1B: 3.935 0x1C: 3.94 0x1D: 3.945 0x1E: 3.95 0x1F: 3.955 0x20: 3.96 0x21: 3.965 0x22: 3.97 0x23: 3.975 0x24: 3.98 0x25: 3.985 0x26: 3.99 0x27: 3.995 0x28: 4 0x29: 4.005 0x2A: 4.01 0x2B: 4.015 0x2C: 4.02 0x2D: 4.025 0x2E: 4.03 0x2F: 4.035 0x30: 4.04 0x31: 4.045 0x32: 4.05 0x33: 4.055 0x34: 4.06 0x35: 4.065 0x36: 4.07 0x37: 4.075 0x38: 4.08 0x39: 4.085 0x3A: 4.09 0x3B: 4.095 0x3C: 4.1 0x3D: 4.105 0x3E: 4.11 0x3F: 4.115 0x40: 4.12 0x41: 4.125 0x42: 4.13 0x43: 4.135 0x44: 4.14 0x45: 4.145 0x46: 4.15 0x47: 4.155 0x48: 4.16 0x49: 4.165 0x4A: 4.17 0x4B: 4.175 0x4C: 4.18 0x4D: 4.185 0x4E: 4.19

BITFIELD	BITS	DESCRIPTION	DECODE
			0x4F: 4.195 0x50: 4.2 0x51: 4.205 0x52: 4.21 0x53: 4.215 0x54: 4.22 0x55: 4.225 0x56: 4.23 0x57: 4.235 0x58: 4.24 0x59: 4.245 0x5A: 4.25 0x5B: 4.255 0x5C: 4.26 0x5D: 4.265 0x5E: 4.27 0x5F: 4.275 0x60: 4.28 0x61: 4.285 0x62: 4.29 0x63: 4.295 0x64: 4.3 0x65: 4.305 0x66: 4.31 0x67: 4.315 0x68: 4.32 0x69: 4.325 0x6A: 4.33 0x6B: 4.335 0x6C: 4.34 0x6D: 4.345 0x6E: 4.35 0x6F: 4.355 0x70: 4.36 0x71: 4.365 0x72: 4.37 0x73: 4.375 0x74: 4.38 0x75: 4.385 0x76: 4.39 0x77: 4.395 0x78: 4.4 0x79: 4.405 0x7A: 4.41 0x7B: 4.415 0x7C: 4.42 0x7D: 4.425 0x7E: 4.43 0x7F: 4.435 0x80: 4.44 0x81: 4.445 0x82: 4.45 0x83: 4.455 0x84: 4.46 0x85: 4.465 0x86: 4.47 0x87: 4.475 0x88: 4.48 0x89: 4.485 0x8A: 4.49 0x8B: 4.495 0x8C: 4.5 0x8D: 4.505 0x8E: 4.51 0x8F: 4.515 0x90: 4.52 0x91: 4.525 0x92: 4.53 0x93: 4.535 0x94: 4.54

BITFIELD	BITS	DESCRIPTION	DECODE
			0x95: 4.545 0x96: 4.55

TEMP_REG (0x1D)

Local Die Temperature Regulation Threshold Register

BIT	7	6	5	4	3	2	1	0
Field	SPARE_7_3[4:0]					TEMP_REG[2:0]		
Reset	0x00					0x7		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_7_3	7:3		
TEMP_REG	2:0	Local Die Temperature Regulation Threshold	0x0: OFF 0x1: 100°C 0x2: 105°C 0x3: 110°C 0x4: 115°C 0x5: 120°C 0x6: 125°C 0x7: 130°C

RT_CFG (0x1E)

Regulation Timer Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SYNC_OUT[1:0]		IIN_DELAY_TIMER[2:0]			REG_TIMER[2:0]		
Reset	0x0		0x3			0x3		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SYNC_OUT	7:6	SYNC Pin Output Level When SYNC_EN = 0	0x0: Hi-Z 0x1: Low 0x2: High 0x3: Prohibited
IIN_DELAY_TIMER	5:3	Invalid Input Current Detection	0x0: OFF 0x1: 200ms 0x2: 400ms 0x3: 800ms 0x4: 1.6s 0x5: 3.2s 0x6: 6.4s 0x7: 12.8s

BITFIELD	BITS	DESCRIPTION	DECODE
REG_TIMER	2:0	Regulation Timer	0x0: OFF 0x1: 200ms 0x2: 400ms 0x3: 800ms 0x4: 1.6s 0x5: 3.2s 0x6: 6.4s 0x7: 12.8s

VIN_OVP_CFG (0x1F)

VIN Overvoltage Protection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SPARE_7_4[3:0]				VIN_OVP_TH[1:0]		VIN_OVP_DEG	VIN_OVP_EN
Reset	0x0				0x2		0x0	0x1
Access Type	Write, Read				Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_7_4	7:4		
VIN_OVP_TH	3:2	VIN OVP Threshold	0x0: 5.2V (1:1), 10.4V (2:1/1:2), 15.6V (3:1/1:3) 0x1: 5.3V (1:1), 10.6V (2:1/1:2), 15.9V (3:1/1:3) 0x2: 5.4V (1:1), 10.8V (2:1/1:2), 16.2V (3:1/1:3) 0x3: 5.5V (1:1), 11.0V (2:1/1:2), 16.5V (3:1/1:3)
VIN_OVP_DEG	1	VIN OVP Deglich Time	0x0: No extra deglitch 0x1: 80µs
VIN_OVP_EN	0	VIN OVP Enable	0x0: Disable VIN OVP 0x1: Enable VIN OVP

VOUT_OVP_CFG (0x20)

VOUT Overvoltage Protection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SPARE_7_5[2:0]			VBATT_OVP_DEG	SPARE_3	VOUT_OVP_TH	VOUT_OVP_DEG	VOUT_OVP_EN
Reset	0x0			0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_7_5	7:5		
VBATT_OVP_DEG	4	Battery (BATP – BATN) OVP Deglich Time	0x0: No extra deglitch 0x1: 100µs

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_3	3		
VOUT_OVP_TH	2	VOUT OVP Threshold (V)	0x0: 4.9 0x1: 5.1
VOUT_OVP_DEG	1	VOUT OVP Deglich Time	0x0: No extra deglitch 0x1: 100µs
VOUT_OVP_EN	0	VOUT OVP Enable	0x0: Disable VOUT OVP 0x1: Enable VOUT OVP

VBATT_OVP_CFG (0x21)

Battery (BATP – BATN) Overvoltage Protection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	VBATT_OVP_TH[6:0]							VBATT_OVP_EN
Reset	0x64							0x1
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VBATT_OVP_TH	7:1	Battery (BATP – BATN) OVP Threshold (V)	0x00: 4 0x01: 4.005 0x02: 4.01 0x03: 4.015 0x04: 4.02 0x05: 4.025 0x06: 4.03 0x07: 4.035 0x08: 4.04 0x09: 4.045 0x0A: 4.05 0x0B: 4.055 0x0C: 4.06 0x0D: 4.065 0x0E: 4.07 0x0F: 4.075 0x10: 4.08 0x11: 4.085 0x12: 4.09 0x13: 4.095 0x14: 4.1 0x15: 4.105 0x16: 4.11 0x17: 4.115 0x18: 4.12 0x19: 4.125 0x1A: 4.13 0x1B: 4.135 0x1C: 4.14 0x1D: 4.145 0x1E: 4.15 0x1F: 4.155 0x20: 4.16 0x21: 4.165 0x22: 4.17 0x23: 4.175 0x24: 4.18 0x25: 4.185 0x26: 4.19

BITFIELD	BITS	DESCRIPTION	DECODE
			0x27: 4.195 0x28: 4.2 0x29: 4.205 0x2A: 4.21 0x2B: 4.215 0x2C: 4.22 0x2D: 4.225 0x2E: 4.23 0x2F: 4.235 0x30: 4.24 0x31: 4.245 0x32: 4.25 0x33: 4.255 0x34: 4.26 0x35: 4.265 0x36: 4.27 0x37: 4.275 0x38: 4.28 0x39: 4.285 0x3A: 4.29 0x3B: 4.295 0x3C: 4.3 0x3D: 4.305 0x3E: 4.31 0x3F: 4.315 0x40: 4.32 0x41: 4.325 0x42: 4.33 0x43: 4.335 0x44: 4.34 0x45: 4.345 0x46: 4.35 0x47: 4.355 0x48: 4.36 0x49: 4.365 0x4A: 4.37 0x4B: 4.375 0x4C: 4.38 0x4D: 4.385 0x4E: 4.39 0x4F: 4.395 0x50: 4.4 0x51: 4.405 0x52: 4.41 0x53: 4.415 0x54: 4.42 0x55: 4.425 0x56: 4.43 0x57: 4.435 0x58: 4.44 0x59: 4.445 0x5A: 4.45 0x5B: 4.455 0x5C: 4.46 0x5D: 4.465 0x5E: 4.47 0x5F: 4.475 0x60: 4.48 0x61: 4.485 0x62: 4.49 0x63: 4.495 0x64: 4.5 0x65: 4.505 0x66: 4.51 0x67: 4.515 0x68: 4.52 0x69: 4.525 0x6A: 4.53 0x6B: 4.535 0x6C: 4.54

BITFIELD	BITS	DESCRIPTION	DECODE
			0x6D: 4.545 0x6E: 4.55 0x6F: 4.555 0x70: 4.56 0x71: 4.565 0x72: 4.57 0x73: 4.575 0x74: 4.58 0x75: 4.585 0x76: 4.59 0x77: 4.595 0x78: 4.6
VBATT_OVP_EN	0	Battery (BATP – BATN) OVP Enable	0x0: Disable Battery (BATP – BATN) OVP 0x1: Enable Battery (BATP – BATN) OVP

CHGR_OCP_CFG (0x22)

Charging Mode Overcurrent Protection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	CHGR_OCP[3:0]				CHGR_OCP_DEG[2:0]			CHGR_OCP_EN
Reset	0x8				0x0			0x1
Access Type	Write, Read				Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CHGR_OCP	7:4	Charging Mode OCP Threshold (mV). Defined as PMID / N – VOUT, where N is the conversion ratio.	0x0: 110 0x1: 125 0x2: 140 0x3: 155 0x4: 170 0x5: 185 0x6: 200 0x7: 215 0x8: 230 0x9: 245 0xA: 260 0xB: 275 0xC: 290 0xD: 305 0xE: 320 0xF: 335
CHGR_OCP_DEG	3:1	Charging Mode OCP Deglitch Timing	0x0: No extra deglitch 0x1: 10µs 0x2: 50µs 0x3: 4ms 0x4: 10ms 0x5: 20ms 0x6: 50ms
CHGR_OCP_EN	0	Charging Mode OCP Enable	0x0: Disable CHGR_OCP 0x1: Enable CHGR_OCP

RVSBST_OCP_CFG (0x23)

Reverse Boost Mode Overcurrent Protection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	RVSBST_OCP[3:0]				RVSBST_OCP_DEG[2:0]			RVSBST_OCP_EN
Reset	0x8				0x0			0x1
Access Type	Write, Read				Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RVSBST_OCP	7:4	Reverse Boost Mode OCP Threshold (mV). Defined as VOUT – PMID / N, where N is the conversion ratio.	0x0: 70 0x1: 85 0x2: 100 0x3: 115 0x4: 130 0x5: 145 0x6: 160 0x7: 175 0x8: 190 0x9: 205 0xA: 220 0xB: 235 0xC: 250 0xD: 265 0xE: 280 0xF: 295
RVSBST_OCP_DEG	3:1	Reverse Boost Mode OCP Deglitch Timing	0x0: No extra deglitch 0x1: 10µs 0x2: 50µs 0x3: 4ms 0x4: 10ms 0x5: 20ms 0x6: 50ms
RVSBST_OCP_EN	0	Reverse Boost Mode OCP Enable	0x0: Disable RVSBST_OCP 0x1: Enable RVSBST_OCP

CHGR_RCP_CFG (0x24)

Charging Mode Reverse Current Protection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SPARE_7	CHGR_RCP[2:0]			CHGR_RCP_DEG[2:0]			CHGR_RCP_EN
Reset	0x0	0x0			0x5			0x1
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_7	7		

BITFIELD	BITS	DESCRIPTION	DECODE
CHGR_RCP	6:4	Charging Mode RCP Threshold (mV). Defined as VOUT – PMID / N, where N is the conversion ratio.	0x0: 0 0x1: 10 0x2: 20 0x3: 30 0x4: 40 0x5: 50 0x6: 60 0x7: 70
CHGR_RCP_DEG	3:1	Charging Mode RCP Deglitch Timing	0x0: No extra deglitch 0x1: 10µs 0x2: 50µs 0x3: 4ms 0x4: 10ms 0x5: 20ms 0x6: 50ms
CHGR_RCP_EN	0	Charging Mode RCP Enable	0x0: Disable CHGR_RCP 0x1: Enable CHGR_RCP

IIN_OCP_CFG (0x25)

Input Current Overcurrent Protection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SPARE_7	IIN_OCP[5:0]						IIN_OCP_EN
Reset	0x0	0x05						0x1
Access Type	Write, Read	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_7	7		
IIN_OCP	6:1	Input Current OCP Threshold (mA). Same threshold is applied to both charging mode and reverse boost mode.	0x00: 500 0x01: 600 0x02: 700 0x03: 800 0x04: 900 0x05: 1000 0x06: 1100 0x07: 1200 0x08: 1300 0x09: 1400 0x0A: 1500 0x0B: 1600 0x0C: 1700 0x0D: 1800 0x0E: 1900 0x0F: 2000 0x10: 2100 0x11: 2200 0x12: 2300 0x13: 2400 0x14: 2500 0x15: 2600 0x16: 2700 0x17: 2800 0x18: 2900 0x19: 3000 0x1A: 3100 0x1B: 3200

BITFIELD	BITS	DESCRIPTION	DECODE
			0x1C: 3300 0x1D: 3400 0x1E: 3500 0x1F: 3600 0x20: 3700 0x21: 3800 0x22: 3900 0x23: 4000 0x24: 4100 0x25: 4200 0x26: 4300 0x27: 4400 0x28: 4500 0x29: 4600 0x2A: 4700 0x2B: 4800 0x2C: 4900 0x2D: 5000 0x2E: 5100 0x2F: 5200 0x30: 5300 0x31: 5400 0x32: 5500 0x33: 5600 0x34: 5700 0x35: 5800 0x36: 5900 0x37: 6000
IIN_OCP_EN	0	Input Current OCP Enable	0x0: Disable IIN_OCP 0x1: Enable IIN_OCP

IIN_OCP_DEG_CFG (0x26)

Input Current Overcurrent Protection Deglitch Time Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SPARE_7_2[5:0]						IIN_OCP_DEG[1:0]	
Reset	0x00						0x1	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_7_2	7:2		
IIN_OCP_DEG	1:0	Input Current OCP Deglich Time	0x0: No extra deglitch 0x1: 10µs 0x2: 100us 0x3: 1ms

IIN_UCP_CFG (0x27)

Input Current Undercurrent Protection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SPARE_7	IIN_UCP[2:0]			IIN_UCP_DEG[2:0]			IIN_UCP_EN

Reset	0x0	0x0	0x5	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_7	7		
IIN_UCP	6:4	Input Current UCP (mA)	0x0: 100 0x1: 200 0x2: 300 0x3: 400 0x4: 500 0x5: 600 0x6: 700 0x7: 800
IIN_UCP_DEG	3:1	Input Current UCP Deglitch Timing	0x0: No extra deglitch 0x1: 10µs 0x2: 100µs 0x3: 4ms 0x4: 5ms 0x5: 20ms 0x6: 50ms
IIN_UCP_EN	0	Input Current UCP Enable	0x0: Disable IIN_UCP 0x1: Enable IIN_UCP

VIN_SHORT_CFG (0x28)

VIN Short Protection Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SPARE_7_6[1:0]		VIN_SHORT_TH[1:0]		VIN_SHORT_DEG[2:0]			VIN_SHORT_EN
Reset	0x0		0x3		0x0			0x1
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_7_6	7:6		
VIN_SHORT_TH	5:4	VIN Short Protection Threshold (V). Defined as PMID – VIN when INFET is on.	0x0: Reserved 0x1: Reserved 0x2: 0.15 0x3: 0.1
VIN_SHORT_DEG	3:1	VIN Short Protection Deglitch Timing	0x0: No extra deglitch 0x1: 10µs 0x2: 50µs 0x3: 4ms 0x4: 10ms 0x5: 20ms 0x6: 50ms
VIN_SHORT_EN	0	VIN Short Protection Enable	0x0: Disable VIN Short Protection 0x1: Enable VIN Short Protection

WT_CFG (0x29)

Watchdog Timer Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	WDTCLR[1:0]		SPARE_5_3[2:0]			WD_TIMER[1:0]		WD_TIMER_EN
Reset	0x0		0x0			0x0		0x0
Access Type	Write, Read		Write, Read			Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WDTCLR	7:6	Watchdog Timer Clear and Restart	0x0: Not Clear 0x1: Clear and restart watchdog timer 0x2: Reserved. Do not use. 0x3: Reserved. Do not use.
SPARE_5_3	5:3		
WD_TIMER	2:1	Watchdog Timer (s)	0x0: 4 0x1: 8 0x2: 16 0x3: 32
WD_TIMER_EN	0	Watchdog Timer Enable	0x0: Disable watchdog timer 0x1: Enable watchdog timer

ADC_EN (0x30)

ADC Enable Register

BIT	7	6	5	4	3	2	1	0
Field	SPARE_7_2[5:0]						ADC_EN_BATTONLY	ADC_EN
Reset	0x00						0x0	0x1
Access Type	Write, Read						Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPARE_7_2	7:2		
ADC_EN_BATTONLY	1	ADC Enable with Battery Only	0x0: Disable ADC 0x1: Enable ADC regardless of VIN voltage
ADC_EN	0	ADC Enable	0x0: Disable ADC 0x1: Enable ADC only when VIN > VIN_UVLO

ADC_CFG1 (0x31)

ADC Configuration Register 1

BIT	7	6	5	4	3	2	1	0

Field	TDIE_READ_EN	NTC_READ_EN	VBATT_READ_EN	VOUT_READ_EN	VEXT2_READ_EN	VEXT1_READ_EN	PMID_READ_EN	VIN_READ_EN
Reset	0x1	0x0	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TDIE_READ_EN	7	TDIE ADC Enable	0x0 0x1: Enable TDIE ADC
NTC_READ_EN	6	NTC ADC Enable	0x0 0x1: Enable NTC ADC
VBATT_READ_EN	5	VBATT ADC Enable	0x0 0x1: Enable VBATT ADC
VOUT_READ_EN	4	VOUT ADC Enable	0x0 0x1: Enable VOUT ADC
VEXT2_READ_EN	3	VEXT2 ADC Enable	0x0 0x1: Enable VEXT2 ADC
VEXT1_READ_EN	2	VEXT1 ADC Enable	0x0 0x1: Enable VEXT1 ADC
PMID_READ_EN	1	PMID ADC Enable	0x0 0x1: Enable PMID ADC
VIN_READ_EN	0	VIN ADC Enable	0x0 0x1: Enable VIN ADC

ADC_CFG2 (0x32)

ADC Configuration Register 2

BIT	7	6	5	4	3	2	1	0
Field	IIN_READ_EN	NTC_OT_EN	INTERVAL[1:0]		RSVD[1:0]		CONV_NUM[1:0]	
Reset	0x1	0x0	0x0		0x2		0x1	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
IIN_READ_EN	7	IIN ADC Enable	0x0 0x1: Enable IIN ADC
NTC_OT_EN	6	NTC Overtemperature Enable	0x0 0x1: Enable NTC OT
INTERVAL	5:4	ADC Interval Timing	0x0: 406µs 0x1: 10ms 0x2: 40ms 0x3: 100ms
RSVD	3:2	Reserved	

BITFIELD	BITS	DESCRIPTION	DECODE
CONV_NUM	1:0	Conversion Number	0x0: 4 samples 0x1: 8 samples 0x2: 16 samples 0x3: 32 samples

NTC_OT_TH1 (0x33)

NTC Overtemperature Threshold Register 1

BIT	7	6	5	4	3	2	1	0
Field	NTC_OT_TH_11_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
NTC_OT_TH_11_4	7:0	NTC OT Threshold 1	NTC_OT_TH = (NTC_OT_TH_11_4[7:0] | NTC_OT_TH_3_0[3:0]) * 0.464mV

NTC_OT_TH2 (0x34)

NTC Overtemperature Threshold Register 2

BIT	7	6	5	4	3	2	1	0
Field	NTC_OT_TH_3_0[3:0]				SPARE_3_0[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
NTC_OT_TH_3_0	7:4	NTC OT Threshold 2	NTC_OT_TH = (NTC_OT_TH_11_4[7:0] | NTC_OT_TH_3_0[3:0]) * 0.464mV
SPARE_3_0	3:0		

ADC_VIN_READ1 (0x35)

ADC Input Voltage Read 1

BIT	7	6	5	4	3	2	1	0
Field	VIN_READ_11_4[7:0]							

Reset	0x00
Access Type	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VIN_READ_11_4	7:0	ADC Input Voltage Read 1	VIN_READ = (VIN_READ_11_4[7:0] | VIN_READ_3_0[3:0]) * 4.395mV ADC_VIN_READ is a 12bit ADC comprising of upper 8 bit from ADC_VIN_READ1[7:0] and lower 4 bit from ADC_VIN_READ2[7:4]. The LSB has a value of 4.395mV.

ADC_VIN_READ2 (0x36)

ADC Input Voltage Read 2

BIT	7	6	5	4	3	2	1	0
Field	VIN_READ_3_0[3:0]				SPARE_3_0[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
VIN_READ_3_0	7:4	ADC Input Voltage Read 2	VIN_READ = (VIN_READ_11_4[7:0] | VIN_READ_3_0[3:0]) * 4.395mV ADC_VIN_READ is a 12bit ADC comprising of upper 8 bit from ADC_VIN_READ1[7:0] and lower 4 bit from ADC_VIN_READ2[7:4]. The LSB has a value of 4.395mV.
SPARE_3_0	3:0		

ADC_PMID_READ1 (0x37)

ADC PMID Voltage Read 1

BIT	7	6	5	4	3	2	1	0
Field	PMID_READ_11_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PMID_READ_11_4	7:0	ADC PMID Voltage Read 1	PMID_READ = (PMID_READ_11_4[7:0] | PMID_READ_3_0[3:0]) * 4.395mV ADC_PMID_READ is a 12bit ADC comprising of upper 8 bit from ADC_PMID_READ1[7:0] and lower 4 bit from ADC_PMID_READ2[7:4]. The LSB has a value of 4.395mV.

ADC_PMID_READ2 (0x38)

ADC PMID Voltage Read 2

BIT	7	6	5	4	3	2	1	0
Field	PMID_READ_3_0[3:0]				SPARE_3_0[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
PMID_READ_3_0	7:4	ADC PMID Voltage Read 2	PMID_READ = (PMID_READ_11_4[7:0] | PMID_READ_3_0[3:0]) * 4.395mV ADC_PMID_READ is a 12bit ADC comprising of upper 8 bit from ADC_PMID_READ1[7:0] and lower 4 bit from ADC_PMID_READ2[7:4]. The LSB has a value of 4.395mV.
SPARE_3_0	3:0		

ADC_VEXT1_READ1 (0x39)

ADC VEXT1 Voltage Read 1

BIT	7	6	5	4	3	2	1	0
Field	VEXT1_READ_11_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
VEXT1_READ_11_4	7:0	ADC VEXT1 Voltage Read 1	VEXT1_READ = (VEXT1_READ_11_4[7:0] | VEXT1_READ_3_0[3:0]) * 4.395mV

BITFIELD	BITS	DESCRIPTION	DECODE
			ADC_VEXT1_READ is a 12bit ADC comprising of upper 8 bit from ADC_VEXT1_READ1[7:0] and lower 4 bit from ADC_VEXT1_READ2[7:4]. The LSB has a value of 4.395mV.

ADC_VEXT1_READ2 (0x3A)

ADC VEXT1 Voltage Read 2

BIT	7	6	5	4	3	2	1	0
Field	VEXT1_READ_3_0[3:0]				SPARE_3_0[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
VEXT1_READ_3_0	7:4	ADC VEXT1 Voltage Read 2	VEXT1_READ = (VEXT1_READ_11_4[7:0] | VEXT1_READ_3_0[3:0]) * 4.395mV ADC_VEXT1_READ is a 12bit ADC comprising of upper 8 bit from ADC_VEXT1_READ1[7:0] and lower 4 bit from ADC_VEXT1_READ2[7:4]. The LSB has a value of 4.395mV.
SPARE_3_0	3:0		

ADC_VEXT2_READ1 (0x3B)

ADC VEXT2 Voltage Read 1

BIT	7	6	5	4	3	2	1	0
Field	VEXT2_READ_11_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
VEXT2_READ_11_4	7:0	ADC VEXT2 Voltage Read 1	VEXT2_READ = (VEXT2_READ_11_4[7:0] | VEXT2_READ_3_0[3:0]) * 4.395mV ADC_VEXT2_READ is a 12bit ADC comprising of upper 8 bit from ADC_VEXT2_READ1[7:0] and lower 4 bit

BITFIELD	BITS	DESCRIPTION	DECODE
			from ADC_VEXT2_READ2[7:4]. The LSB has a value of 4.395mV.

ADC_VEXT2_READ2 (0x3C)

ADC VEXT2 Voltage Read 2

BIT	7	6	5	4	3	2	1	0
Field	VEXT2_READ_3_0[3:0]				SPARE_3_0[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
VEXT2_READ_3_0	7:4	ADC VEXT2 Voltage Read 2	VEXT2_READ = (VEXT2_READ_11_4[7:0] | VEXT2_READ_3_0[3:0]) * 4.395mV ADC_VEXT2_READ is a 12bit ADC comprising of upper 8 bit from ADC_VEXT2_READ1[7:0] and lower 4 bit from ADC_VEXT2_READ2[7:4]. The LSB has a value of 4.395mV.
SPARE_3_0	3:0		

ADC_VOUT_READ1 (0x3D)

ADC Output Voltage Read 1

BIT	7	6	5	4	3	2	1	0
Field	VOUT_READ_11_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
VOUT_READ_11_4	7:0	ADC Output Voltage Read 1	VOUT_READ = (VOUT_READ_11_4[7:0] | VOUT_READ_3_0[3:0]) * 1.221mV ADC_VOUT_READ is a 12bit ADC comprising of upper 8 bit from ADC_VOUT_READ1[7:0] and lower 4 bit from ADC_VOUT_READ2[7:4]. The LSB has a value of 1.221mV.

ADC_VOUT_READ2 (0x3E)

ADC Output Voltage Read 2

BIT	7	6	5	4	3	2	1	0
Field	VOUT_READ_3_0[3:0]				SPARE_3_0[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
VOUT_READ_3_0	7:4	ADC Output Voltage Read 2	VOUT_READ = (VOUT_READ_11_4[7:0] | VOUT_READ_3_0[3:0]) * 1.221mV ADC_VOUT_READ is a 12bit ADC comprising of upper 8 bit from ADC_VOUT_READ1[7:0] and lower 4 bit from ADC_VOUT_READ2[7:4]. The LSB has a value of 1.221mV.
SPARE_3_0	3:0		

ADC_VBATT_READ1 (0x3F)

ADC Battery Voltage Read 1

BIT	7	6	5	4	3	2	1	0
Field	VBATT_READ_11_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
VBATT_READ_11_4	7:0	ADC Battery Voltage Read 1	VBATT_READ = (VBATT_READ_11_4[7:0] | VBATT_READ_3_0[3:0]) * 1.221mV ADC_VBATT_READ is a 12bit ADC comprising of upper 8 bit from ADC_VBATT_READ1[7:0] and lower 4 bit from ADC_VBATT_READ2[7:4]. The LSB has a value of 1.221mV.

ADC_VBATT_READ2 (0x40)

ADC Battery Voltage Read 2

BIT	7	6	5	4	3	2	1	0

Field	VBATT_READ_3_0[3:0]	SPARE_3_0[3:0]
Reset	0x0	0x0
Access Type	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VBATT_READ_3_0	7:4	ADC Battery Voltage Read 2	VBATT_READ = (VBATT_READ_11_4[7:0] | VBATT_READ_3_0[3:0]) * 1.221mV ADC_VBATT_READ is a 12bit ADC comprising of upper 8 bit from ADC_VBATT_READ1[7:0] and lower 4 bit from ADC_VBATT_READ2[7:4]. The LSB has a value of 1.221mV.
SPARE_3_0	3:0		

ADC_NTC_READ1 (0x41)

ADC NTC Voltage Read 1

BIT	7	6	5	4	3	2	1	0
Field	NTC_READ_11_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
NTC_READ_11_4	7:0	ADC NTC Voltage Read 1	NTC_READ = (NTC_READ_11_4[7:0] | NTC_READ_3_0[3:0]) * 0.464mV ADC_NTC_READ is a 12bit ADC comprising of upper 8 bit from ADC_NTC_READ1[7:0] and lower 4 bit from ADC_NTC_READ2[7:4]. The LSB has a value of 0.464mV.

ADC_NTC_READ2 (0x42)

ADC NTC Voltage Read 2

BIT	7	6	5	4	3	2	1	0
Field	NTC_READ_3_0[3:0]				SPARE_3_0[3:0]			
Reset	0x0				0x0			

Access Type	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
NTC_READ_3_0	7:4	ADC NTC Voltage Read 2	NTC_READ = (NTC_READ_11_4[7:0] | NTC_READ_3_0[3:0]) * 0.464mV ADC_NTC_READ is a 12bit ADC comprising of upper 8 bit from ADC_NTC_READ1[7:0] and lower 4 bit from ADC_NTC_READ2[7:4]. The LSB has a value of 0.464mV.
SPARE_3_0	3:0		

ADC_TDIE_READ1 (0x43)

ADC Die Temperature Read 1

BIT	7	6	5	4	3	2	1	0
Field	TDIE_READ_11_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
TDIE_READ_11_4	7:0	ADC Die Temperature Read 1	2's complement: if bit 7 of TDIE_READ_11_4[7:0] is 0, TDIE_READ = (TDIE_READ_11_4[7:0] | TDIE_READ_3_0[3:0]) * 0.081°C; if bit 7 of TDIE_READ_11_4[7:0] is 1, TDIE_READ = { (TDIE_READ_11_4[7:0] | TDIE_READ_3_0[3:0]) + 1 } * -0.081°C ADC_TDIE_READ is a 12bit ADC comprising of upper 8 bit from ADC_TDIE_READ1[7:0] and lower 4 bit from ADC_TDIE_READ2[7:4]. The LSB has a value of 0.081°C.

ADC_TDIE_READ2 (0x44)

ADC Die Temperature Read 2

BIT	7	6	5	4	3	2	1	0
Field	TDIE_READ_3_0[3:0]				SPARE_3_0[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
TDIE_READ_3_0	7:4	ADC Die Temperature Read 2	2's complement: if bit 7 of TDIE_READ_11_4[7:0] is 0, TDIE_READ = (TDIE_READ_11_4[7:0] | TDIE_READ_3_0[3:0]) * 0.081ºC; if bit 7 of TDIE_READ_11_4[7:0] is 1, TDIE_READ = { (TDIE_READ_11_4[7:0] | TDIE_READ_3_0[3:0]) + 1 } * -0.081ºC ADC_TDIE_READ is a 12bit ADC comprising of upper 8 bit from ADC_TDIE_READ1[7:0] and lower 4 bit from ADC_TDIE_READ2[7:4]. The LSB has a value of 0.081ºC.
SPARE_3_0	3:0		

ADC_IIN_READ1 (0x45)

ADC Input Current Read 1

BIT	7	6	5	4	3	2	1	0
Field	IIN_READ_11_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
IIN_READ_11_4	7:0	ADC Input Current Read 1	IIN_READ = (IIN_READ_11_4[7:0] | IIN_READ_3_0[3:0]) * 1.563mA ADC_IIN_READ is a 12bit ADC comprising of upper 8 bit from ADC_IIN_READ1[7:0] and lower 4 bit from ADC_IIN_READ2[7:4]. The LSB has a value of 1.563mA. Direction of the input current is from VIN to PMID in forward modes and from PMID to VIN in reverse modes.

ADC_IIN_READ2 (0x46)

ADC Input Current Read 2

BIT	7	6	5	4	3	2	1	0
Field	IIN_READ_3_0[3:0]				SPARE_3_0[3:0]			
Reset	0x0				0x0			

Access Type	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
IIN_READ_3_0	7:4	ADC Input Current Read 2	IIN_READ = (IIN_READ_11_4[7:0] | IIN_READ_3_0[3:0]) * 1.563mA ADC_IIN_READ is a 12bit ADC comprising of upper 8 bit from ADC_IIN_READ1[7:0] and lower 4 bit from ADC_IIN_READ2[7:4]. The LSB has a value of 1.563mA. Direction of the input current is from VIN to PMID in forward modes and from PMID to VIN in reverse modes.
SPARE_3_0	3:0		

Applications Information

The flying capacitors, C_{FLY1} and C_{FLY2}, must have low impedance at the switching frequency. For better efficiency, it is recommended to select 2x22µF 16V for C_{FLY1} and 2x22µF 10V for C_{FLY2}.

The output capacitor, C_{OUT}, is required to keep the output voltage ripple small and must have low impedance at the switching frequency. The recommended minimum output capacitance is 2x10µF.

Ceramic capacitors with X5R or X7R dielectric are highly recommended for C_{FLY1}, C_{FLY2}, and C_{OUT} due to their small size, low ESR, and small temperature coefficients.

Table 16. Suggested VIN and PMID Capacitor

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (in)	DIMENSIONS L x W x H (mm)
Samsung	CL10A106MA8NRN	10	25	X5R	0603	1.6 x 0.8 x 0.8
Murata	GRM188R61E106MA73	10	25	X5R	0603	1.6 x 0.8 x 0.8

Table 17. Suggested Flying Capacitor

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (in)	DIMENSIONS L x W x H (mm)
Samsung	CL10A226MO7JZN	22	16	X5R	0603	1.6 x 0.8 x 0.7
Murata	GRM188R61C226ME01	22	16	X5R	0603	1.6 x 0.8 x 0.8
Samsung	CL21A226MOCLRN	22	16	X5R	0805	2.0 x 1.25 x 0.85
Murata	GRM219R61C226ME15	22	16	X5R	0805	2.0 x 1.25 x 0.85
Samsung	CL10A226MP8NUN	22	10	X5R	0603	1.6 x 0.8 x 0.8
Murata	GRM187R61A226ME15	22	10	X5R	0603	1.6 x 0.8 x 0.7
Samsung	CL21A226MPCLRN	22	10	X5R	0805	2.0 x 1.25 x 0.85

Table 18. Suggested VOUT Capacitor

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (in)	DIMENSIONS L x W x H (mm)
Samsung	CL05A106MP6NUN	10	10	X5R	0402	1.0 x 0.5 x 0.6
Murata	GRM155R61A106ME18	10	10	X5R	0402	1.0 x 0.5 x 0.5

Table 19. Suggested VEXT Capacitor

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (in)	DIMENSIONS L x W x H (mm)
Samsung	CL05A105KL5NRN	1	35	X5R	0402	1.0 x 0.5 x 0.5
Murata	GRM155R6YA105ME11	1	35	X5R	0402	1.0 x 0.5 x 0.5

Table 20. Suggested BST Capacitor

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (in)	DIMENSIONS L x W x H (mm)
Samsung	CL03A104MP3NNN	0.1	10	X5R	0201	0.6 x 0.3 x 0.3
Murata	GRM033R61A104ME15	0.1	10	X5R	0201	0.6 x 0.3 x 0.3

Table 21. Suggested PVDD Capacitor

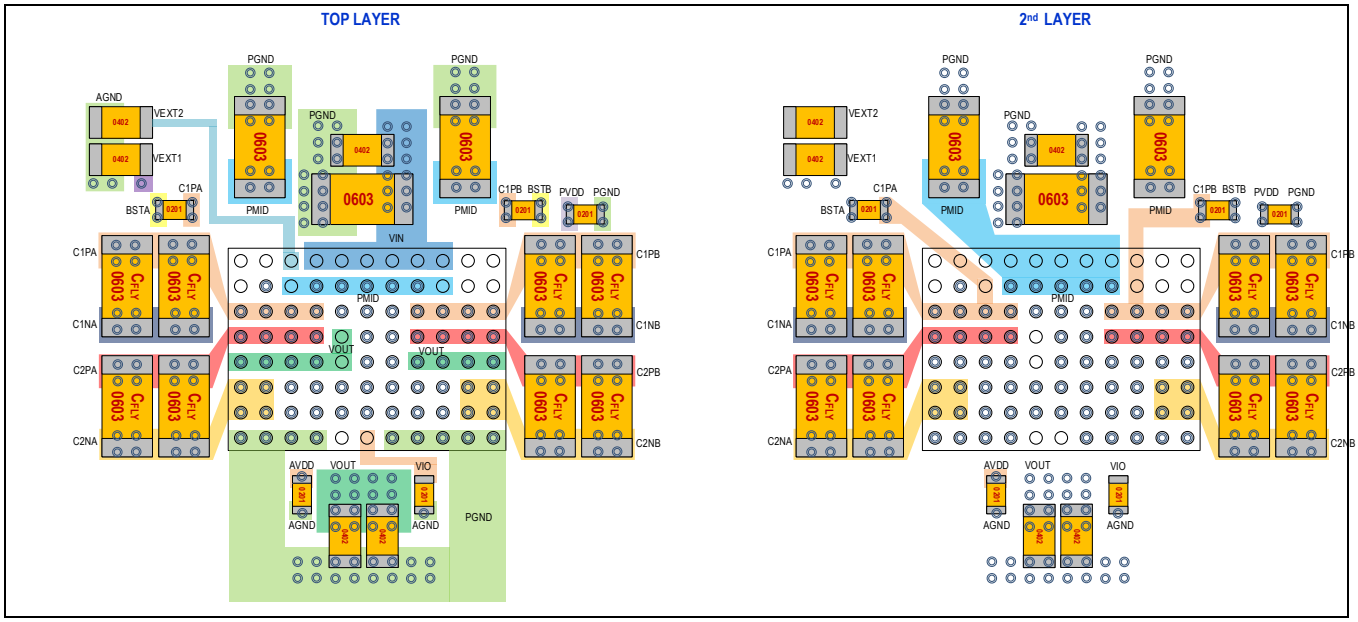
MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (in)	DIMENSIONS L x W x H (mm)
Samsung	CL03A225MP3CRN	2.2	10	X5R	0201	0.6 x 0.3 x 0.3
Murata	GRM033R61A225ME47	2.2	10	X5R	0201	0.6 x 0.3 x 0.3

Table 22. Suggested AVDD Capacitor

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (in)	DIMENSIONS L x W x H (mm)
Samsung	CL03A105MP3NSN	1	10	X5R	0201	0.6 x 0.3 x 0.3
Murata	GRM033R61A105ME01	1	10	X5R	0201	0.6 x 0.3 x 0.3

Layout Guide

1. Connect all bypass capacitors VIN, PMID, VOUT, VEXT, BST, PVDD, AVDD, VIO, and flying capacitors C_{FLY1} and C_{FLY2} as close to the IC as possible.
2. All power traces between phase A and phase B must be as symmetrical as possible. For example, the C1PA and C1PB traces must be symmetrical.
3. Add multiple vias near the PMID/VOUT/PGND/C1Px/C1Nx/C2Px/C2Nx pins of the IC to bring them down to the inner layers. These traces must be duplicated on multiple layers to minimize the impedance.
4. Do not directly tie AGND of AVDD to PGND on the top layer. Add a via to AGND and connect it to a clean system ground plane on the inner layers. Ensure the connection point of AGND is not on the current return path of PGND.
5. Traces from inner pins, especially BSTA, BSTB, PVDD, and AVDD, to their corresponding bypass capacitors must be as short and wide as possible.
6. For connection to BSTA/BSTB, use more than one via to lower the via impedance.



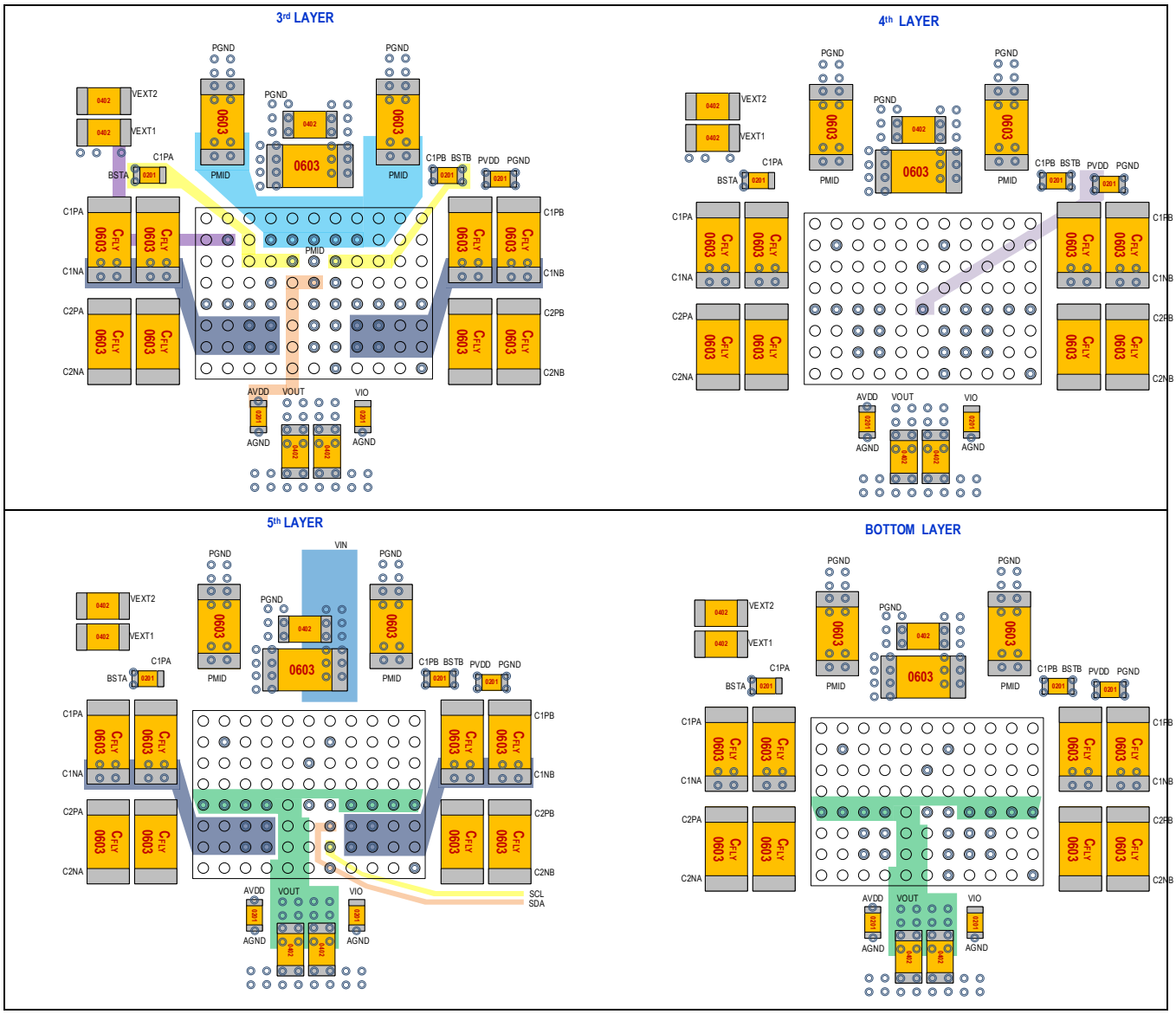


Figure 20. PCB Layout Example

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX77928EWN+	-40°C to +85°C	88 WLP (0.4mm Pitch)
MAX77928EWN+T	-40°C to +85°C	88 WLP (0.4mm Pitch)

+Denotes a lead (Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/25	Release for Market Intro	—