2.5V to 16V Input, 5A Switching Current High-Efficiency Buck-Boost Converter with External Clock Synchronization

MAX77845

General Description

The MAX77845 is a high-efficiency, high-performance buck-boost converter. It supports a wide input voltage range of 2.5V to 16V, enabling direct conversion from sources such as up to 3-cell Li+ batteries, USB power delivery (PD), and 12V DC supply rails. The converter provides a wide output voltage range of 3V to 15V, making it suitable for a broad range of applications.

The device delivers up to 4.5A of output current in buck mode and up to 3A in boost mode. It operates in PWM mode and incorporates an automatic SKIP mode to enhance efficiency under light load conditions. With a peak efficiency of 94%, a low quiescent current, and a compact solution size, the MAX77845 is well-suited for battery-powered, space-constrained designs.

The default output voltage is 5V when using internal feedback resistors. It can be configured to other default output voltages using external feedback resistors. Additionally, the output voltage is dynamically adjustable through an I^2C-compatible interface.

The device includes dedicated control pins EN, BIASEN, POKB/INTB, FPWM/SYNC, and SEL for direct hardware control. Additional configuration options, including soft-start time, DVS slew rate, switching current limit, and switching frequency, can be accessed through the I^2C interface. The programmable switching frequency and support for external clock synchronization facilitate system optimization in noise-sensitive environments.

The R_{SEL} pin and I^2C-programmable current limit enable the use of lower-profile, smaller external components that are optimized for specific applications. The MAX77845 integrates a comprehensive set of protection features to ensure safe operation under abnormal conditions.

The device is available in a 2.82mm × 1.69mm, 28-bump wafer-level package (WLP).

Applications

- USB Power Delivery (USB-PD) OTG
- USB VBUS Supply and Dual Role Power (DRP) Ports
- DSLR, DSLR Lens
- Display Power
- Up to 3-Cell Li-Ion Battery Applications
- Wireless Charging Accessories
- AR/VR ToF Bias Power
- Notebook Computer, Tablet PC

Benefits and Features

- Wide Input Voltage Range: 2.5V to 16V
- I^2C-Programmable Output Voltage: 3V to 15V
- Maximum Output Current
  - Buck Mode: Up to 4.5A
  - Boost Mode: Up to 3A (V_{IN} = 3.7V, V_{OUT} = 5V)
- 5A Typical Peak Inductor Switching Current
- Automatic SKIP Mode and Forced-PWM Mode
- External Clock Synchronization up to 2.60MHz
- R_{SEL} Configuration
  - I^2C Interface Target Address
  - Switching Frequency
  - Switching Current Limit Threshold
  - Internal/External Feedback Resistors
- I^2C Programming (Optional)
  - Output Voltage (DVS)
  - DVS Slew Rate
  - Soft-Start Time
  - Switching Current Limit Threshold
  - Switching Frequency
  - Forced-PWM Mode (FPWM) Operation
  - Loop Compensation
  - Power-OK (POK) and Fault Status/Interrupts
- Soft-Start and Output Active Discharge
- Open-Drain POK Status/Fault Interrupts Pin
- Protection Features
  - Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Short-Circuit Protection (SCP)
  - Overvoltage Protection (OVP)
  - Thermal Shutdown (T_{SHDN})
- Available in 2.82mm x 1.69mm 28-bump WLP

***Ordering Information* appears at end of data sheet.**

19-102052; Rev 0; 11/25

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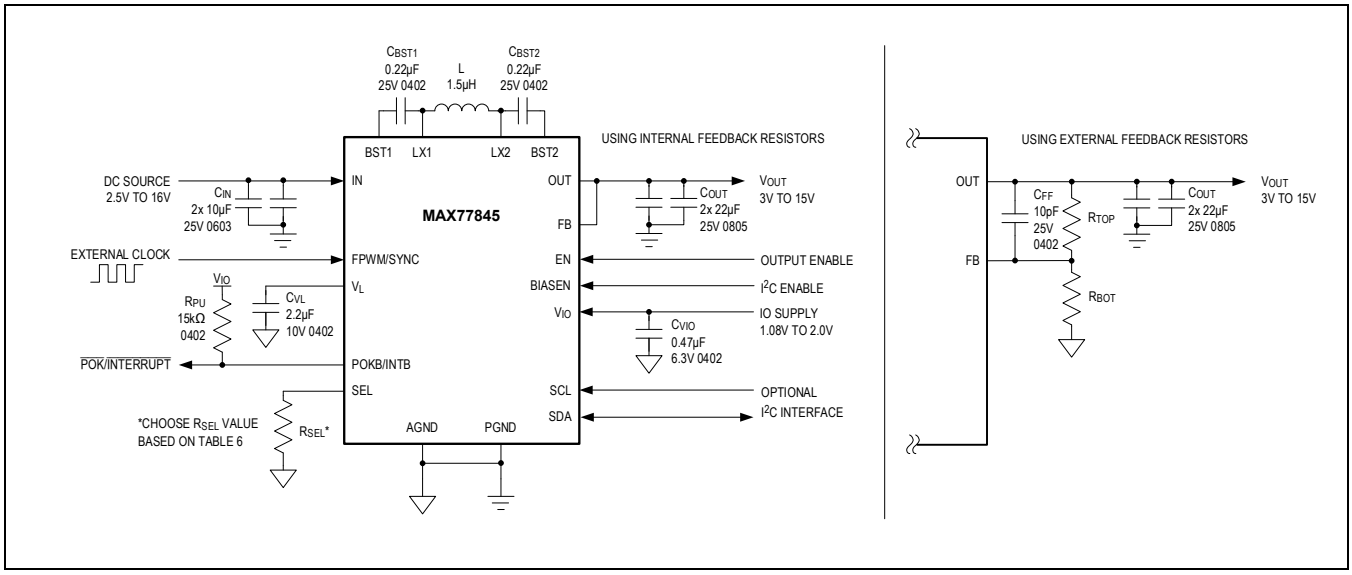
Simplified Application Diagram



Absolute Maximum Ratings

IN, LX1, LX2, OUT, FB to PGND ..... -0.3V to +17.6V

BST1, BST2 to AGND..... -0.3V to +20.0V

BST1 to LX1, BST2 to LX2 ..... -0.3V to +2.2V

SCL, SDA, POKB/INTB to AGND, PGND . -0.3V to V_{IO} + 0.3V

V_L, V_{IO}, SEL, EN, BIASEN, to AGND, PGND ... -0.3V to +2.0V

FPWM/SYNC to AGND, PGND ..... -0.3V to +6.0V

PGND to AGND ..... -0.3V to +0.3V

Continuous Power Dissipation.....

WLP Package (T_A = +70°C, derate 19.76mW/°C above +70°C (*Note 1*))..... 1581mW

Maximum Junction Temperature.....+150°C

Storage Temperature Range..... -65°C to +150°C

Soldering Temperature (reflow).....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages*.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

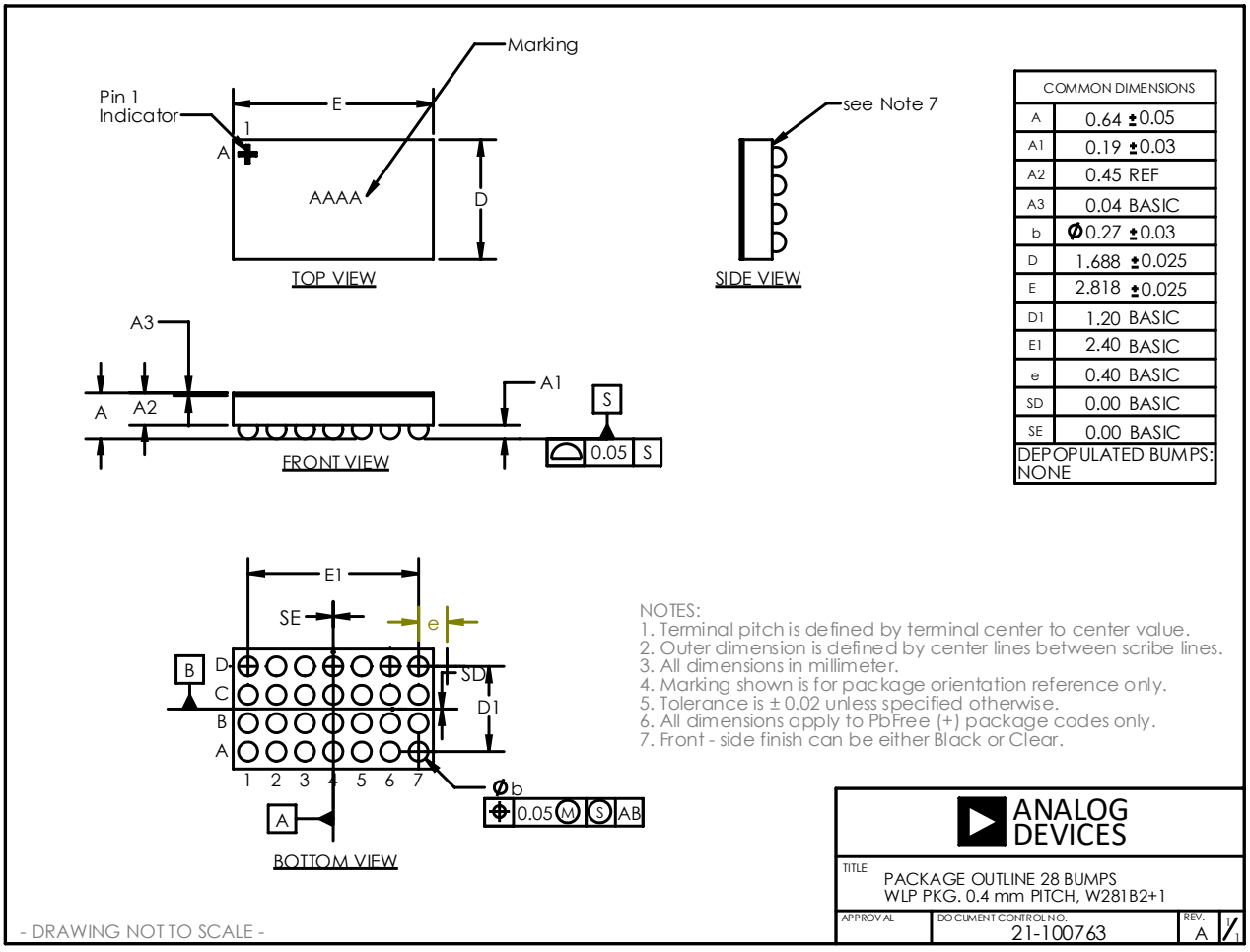
Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE
Input Voltage Range	V_{IN}		2.5V to 16V
Output Voltage Range	V_{OUT}		3V to 15V
Output Current Range	I_{OUT}	For continuous operation at 4.5A, the junction temperature (T_J) is limited to +105ºC. If the junction temperature is higher than 105ºC, the expected lifetime at 4.5A continuous operation is derated	0A to 4.5A
Junction Temperature Range	T_J		-40°C to +125°C

Package Information

28 WLP

Package Code	W281B2+1
Outline Number	21-100763
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θJA)	50.60 (°C/W)



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.04 BASIC
b	Ø0.27 ±0.03
D	1.688 ±0.025
E	2.818 ±0.025
D1	1.20 BASIC
E1	2.40 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

ANALOG DEVICES

TITLE: PACKAGE OUTLINE 28 BUMPS WLP PKG. 0.4 mm PITCH, W281B2+1

APPROVAL | DOCUMENT CONTROL NO. 21-100763 | REV. A | 1/1

For the latest package outline information and land patterns (footprints), go to [www.analog.com/packages.](www.analog.com/packages) Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *[www.analog.com/thermal-tutorial.](www.analog.com/thermal-tutorial)*

Electrical Characteristics

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY							
Input Voltage Range	V_{IN}			2.5		16	V
Input Undervoltage Lockout (UVLO)	V_{UVLO_R}	V_{IN} rising		2.3	2.4	2.5	V
Input Undervoltage Lockout (UVLO) Hysteresis	V_{UVLO_HYS}	$V_{UVLO_R} - V_{UVLO_F}$			300		mV
Shutdown Supply Current	I_{SHDN}	EN = LOW, T_J = -40°C to +85°C	BIASEN = LOW		2	6	µA
			BIASEN = HIGH		20	65	
Quiescent Supply Current	I_Q	EN = HIGH, R_{SEL} = short to GND, no switching	SKIP mode, T_J = -40°C to +85°C		60	88	µA
			FPWM mode		4		mA
OUTPUT VOLTAGE							
Output Voltage Regulation Range	V_{OUT}			3.0		15	V
Output Voltage Accuracy	V_{OUT_ACC}	V_{IN} = 2.5V to 16V, V_{OUT} = 3.0V to 15V, I_{OUT} = 0mA, using internal feedback resistors	SKIP mode, T_J = -40°C to +65°C	-1.0		+4.5	%
			FPWM mode	-1.0		+2.0	
FB Accuracy	V_{FB_ACC}	VREF[9:0] = 0x096 to 0x2ED		-1.0		+2.0	%
V_L INTERNAL SUPPLY							
V_L Regulator Voltage	V_{VL}			1.65	1.8	1.89	V
V_{IO} SUPPLY							
V_{IO} Voltage Range	V_{VIO}			1.08		2.0	V
V_{IO} Valid Threshold	$V_{VIO_VALID_R}$	V_{IO} rising		0.965	1.02	1.08	V
	$V_{VIO_VALID_F}$	V_{IO} falling		0.85	0.9	0.955	
V_{IO} Bias Current	I_{VIO}	No I^2C interface (SDA and SCL unconnected)				2.0	µA
		f_{SCL} = f_{SDA} = 1MHz			50		
BUCK-BOOST REGULATOR							
Switching Frequency	f_{SW}	I_{OUT} = 0mA, FPWM mode	FREQ[1:0] = 00	1.10	1.20	1.30	MHz
			FREQ[1:0] = 01	1.38	1.50	1.62	
			FREQ[1:0] = 10	1.66	1.80	1.94	
			FREQ[1:0] = 11	1.93	2.10	2.27	
Startup Delay Time	t_{SUDLY}				100		µs
Soft-Start Time	t_{SS}	VREF[9:0] = 0x0FA, measured from OUT starts ramping to stops ramping, C_{OUT} = 44µF, I_{OUT} = 0mA	SS_TM[1:0] = 00		1		ms
			SS_TM[1:0] = 01 (default)		2		
			SS_TM[1:0] = 10		4		
			SS_TM[1:0] = 11		8		
	I_{LIM_SS}	ILIM[1:0] = 10 or 11 (I_{LIM} < 3.4A)			I_{LIM}		A

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Soft-Start Switching Current Limit		ILIM[1:0] = 00 or 01 (I_{LIM} ≥ 3.4A)		3.4		
High-Side Switching Current Limit	I_{LIM}	ILIM[1:0] = 00	4.3	5.0	6.3	A
		ILIM[1:0] = 01 (I^2C only, not available with R_{SEL}) (*Note 2*)	2.9	3.4	4.6	
		ILIM[1:0] = 10 (*Note 2*)	1.5	1.8	2.9	
		ILIM[1:0] = 11 (I^2C only, not available with R_{SEL}) (*Note 2*)	0.85	1.0	2.0	
Valley Current Limit	I_{LIM_VALLEY}	ILIM[1:0] = 00 or 01 (*Note 2*)		1.8		A
		ILIM[1:0] = 10 or 11 (*Note 2*)		0.3		
Skip Mode Switching Current Limit	I_{LIM_SKIP}	SKIP mode (*Note 2*)		1.4		A
Line Regulation	$\Delta V/V_{IN}$	V_{IN} = 2.5V to 16V, V_{OUT} = 5V, I_{OUT} = 0mA and 1A, FPWM mode		± 0.3		%/V
Load Regulation	$\Delta V/V_{OUT}$	V_{IN} ≥ 4V, V_{OUT} = 5V, I_{OUT} = 0mA to 3A, FPWM mode		± 0.6		%/A
Internal Reference Voltage	V_{REF}	VREF[9:0] = 0x096, code clamped below this level		0.18311		V
		VREF[9:0] = 0x0FA, default value		0.30518		
		VREF[9:0] = 0x2ED, code clamped above this level		0.91431		
Internal Reference Voltage Programmable Range	V_{REF}	VREF[9:0] = 0x096 to 0x2ED	0.18311		0.91431	V
Internal Reference DVS Ramp Rate	$\Delta V_{REF}/\Delta t$	DVS_SR[1:0] = 00 (default)		4/3		mV/µs
		DVS_SR[1:0] = 01		2/3		
		DVS_SR[1:0] = 10		1/3		
		DVS_SR[1:0] = 11		1/6		
FB Input Leakage Current	I_{FB_LK}		-1		+1	µA
High-Side MOSFET On Resistance	R_{DSON_HS}	IN to LX1, LX2 to OUT		25	40	mΩ
Low-Side MOSFET On Resistance	R_{DSON_LS}	LX1 to PGND, LX2 to PGND		30	50	mΩ
OVERVOLTAGE PROTECTION						
Overvoltage Threshold	V_{OVP_R}	V_{OUT} rising	15.85	16.40	16.95	V
	V_{OVP_F}	V_{OUT} falling	15.25	15.50	16.20	
ACTIVE DISCHARGE						
Output Active Discharge Current	I_{AD}	AD_EN = 1, EN = LOW or V_{IN} < V_{UVLO_F}, V_{OUT} = 15V		5		mA
ENABLE CONTROL INPUTS						
EN, BIASEN Input LOW Voltage	V_{EN_IL}				0.4	V
EN, BIASEN Input HIGH Voltage	V_{EN_IH}		0.9			V
EN Internal Pulldown Current	I_{EN_PD}	EN = HIGH, pulldown current to AGND		0.1		µA

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIASEN Internal Pulldown Resistance	R_{BIASEN_PD}	Pulldown resistance to AGND		800		kΩ
FPWM/SYNC CONTROL INPUT						
FPWM/SYNC Input LOW Voltage	V_{FPWM_IL}				0.4	V
FPWM/SYNC Input HIGH Voltage	V_{FPWM_IH}		0.9			V
Valid Synchronization Range	f_{SYNC}	FREQ[1:0] = 00 (1.2MHz)	0.84		1.50	MHz
		FREQ[1:0] = 01 (1.5MHz)	1.05		1.88	
		FREQ[1:0] = 10 (1.8MHz)	1.26		2.25	
		FREQ[1:0] = 11 (2.1MHz)	1.47		2.60	
POWER-OK (POK) AND INTERRUPT OUTPUT						
Output LOW Voltage	V_{OL}	$I_{POKB/INTB}$ = 1mA			0.3	V
POK Threshold	V_{POK_R}	V_{OUT} rising, expressed as a percentage of the target V_{OUT} voltage	90	95		%
	V_{POK_F}	V_{OUT} falling, expressed as a percentage of the target V_{OUT} voltage		85		
THERMAL PROTECTION						
Thermal-Shutdown Threshold	T_{SHDN_R}	T_J rising (*Note 2*)		150		ºC
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}	$T_{SHDN_R} - T_{SHDN_F}$ (*Note 2*)		20		ºC

Electrical Characteristics–I²C Serial Interface

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O STAGE						
SCL, SDA Input HIGH Voltage	V_{IH}		0.7 x V_{VIO}			V
SCL, SDA Input LOW Voltage	V_{IL}				0.3 x V_{VIO}	V
SCL, SDA Input Hysteresis	V_{HYS}	Fast mode/Fast-mode plus	0.05 x V_{VIO}			V
		High-speed mode	0.1 x V_{VIO}			
SDA Output LOW Voltage	V_{OL}	I_{SINK} = 2mA (Fast mode/Fast-mode plus) or 3mA (High-speed mode)			0.2 x V_{VIO}	V
SCL, SDA Input Capacitance	C_I				10	pF
SCL, SDA Input Leakage Current	I_{LK}		-10	0.001	+10	µA
TIMING (FAST MODE)						
Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Condition	t_{BUSF}		1.3			µs
Hold Time (REPEATED) START Condition	t_{HD_START}		0.6			µs
SCL LOW Period	t_{LOW}		1.3			µs
SCL HIGH Period	t_{HIGH}		0.6			µs
Setup Time (REPEATED) START Condition	t_{SU_START}		0.6			µs
DATA Setup Time	T_{SU_DATA}		100			ns
SCL, SDA Receiving Rise Time	t_{R_REV}		20		300	ns
SCL, SDA Receiving Fall Time	t_{F_REV}		20 x (V_{VIO} /5.5V)		300	ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Data Valid Time	t_{VD_DATA}				900	ns
Data Valid Acknowledge Time	t_{VD_ACK}				900	ns
Bus Capacitance	C_B	(*Note 3*)			400	pF
Pulse Width of Suppressed Spikes	t_{SP}				140	ns
TIMING (FAST-MODE PLUS)						
Clock Frequency	f_{SCL}		0		1000	kHz
Bus Free Time Between STOP and START Condition	t_{BUSF}		0.5			µs

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time (REPEATED) START Condition	t_{HD_START}		0.26			µs
SCL LOW Period	t_{LOW}		0.5			µs
SCL HIGH Period	t_{HIGH}		0.26			µs
Setup Time (REPEATED) START Condition	t_{SU_START}		0.26			µs
DATA Setup Time	T_{SU_DATA}		50			ns
SCL, SDA Receiving Rise Time	t_{R_REV}				120	ns
SCL, SDA Receiving Fall Time	t_{F_REV}		20 x (V_{VIO} /5.5V)		120	ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Data Valid Time	t_{VD_DATA}				450	ns
Data Valid Acknowledge Time	t_{VD_ACK}				450	ns
Bus Capacitance	C_B	(*Note 3*)			550	pF
Pulse Width of Suppressed Spikes	t_{SP}				140	ns
TIMING (HIGH-SPEED MODE, BUS CAPACITANCE = 100pF)						
Clock Frequency	f_{SCL}				3.4	MHz
Hold Time (REPEATED) START Condition	t_{HD_START}		160			ns
SCL LOW Period	t_{LOW}		160			ns
SCL HIGH Period	t_{HIGH}		60			ns
Setup Time (REPEATED) START Condition	t_{SU_START}		160			ns
DATA Hold Time	t_{HD_DATA}				95	ns
DATA Setup Time	T_{SU_DATA}		10			ns
SCL Rise Time	t_{R_SCL}		10		50	ns
SCL Fall Time	t_{F_SCL}		10		50	ns
SDA Rise Time	t_{R_SDA}		10		80	ns
SDA Fall Time	t_{F_SDA}		10		80	ns
Setup Time for STOP Condition	t_{SU_STOP}		160			ns
Bus Capacitance	C_B	(*Note 3*)			100	pF
Pulse Width of Suppressed Spikes	t_{SP}				30	ns

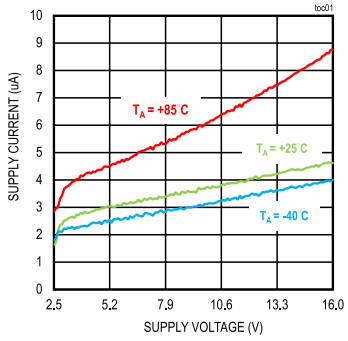
Note 2: Characterized by ATE or bench test. Not production tested.

Note 3: Internal design target. Not production tested.

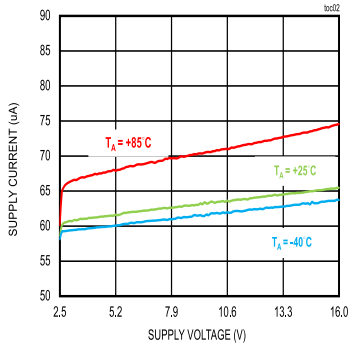
Typical Operating Characteristics

(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (COILCRAFT XGL4020-152ME), C_{OUT} = 2x 22µF, FPWM = 0, I_{LIM}[1:0] = 0x0 (5.0A), f_{SW} = 2.1MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted. Note: Measurement limited by switching current limit. Actual maximum output current depends on system thermal performance.)

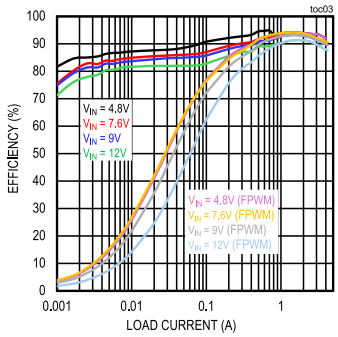
SHUTDOWN CURRENT



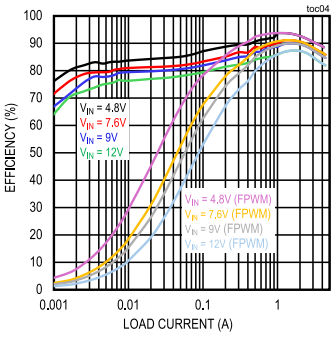
QUIESCENT CURRENT



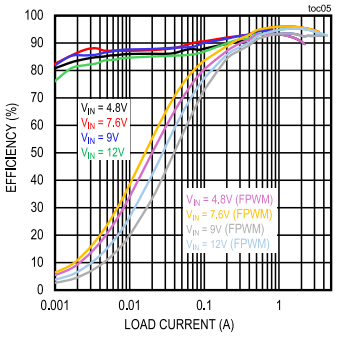
EFFICIENCY 5V OUTPUT



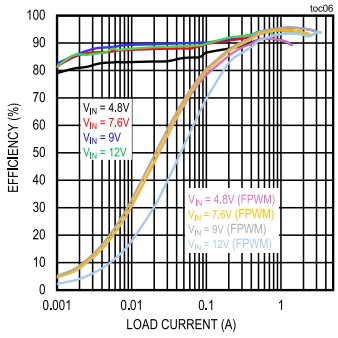
EFFICIENCY 3.3V OUTPUT



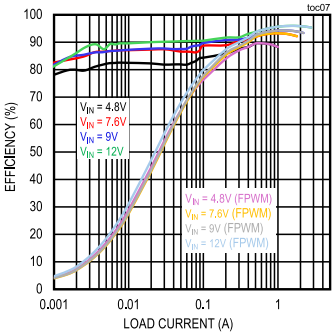
EFFICIENCY 9V OUTPUT



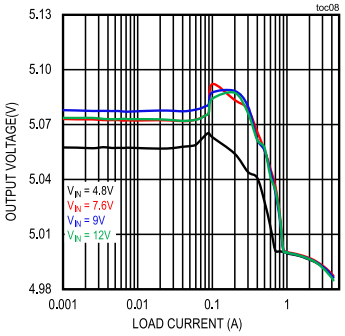
EFFICIENCY 12V OUTPUT



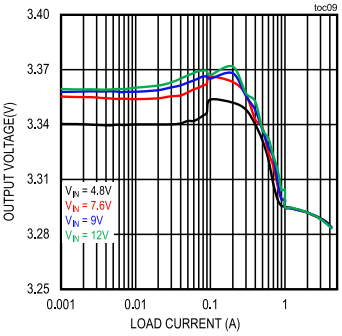
EFFICIENCY 15V OUTPUT



LOAD REGULATION 5V OUTPUT



LOAD REGULATION 3.3V OUTPUT



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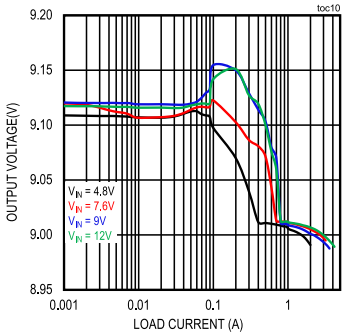
9V OUTPUT



LOAD REGULATION
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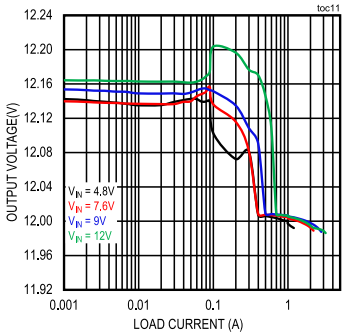

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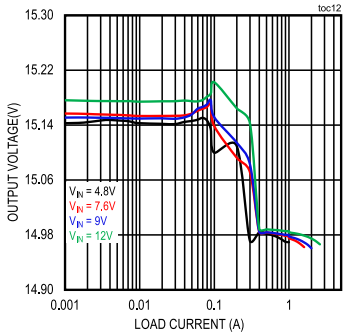

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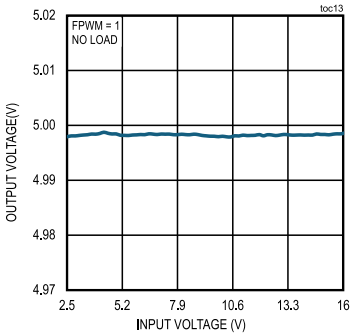
5V OUTPUT



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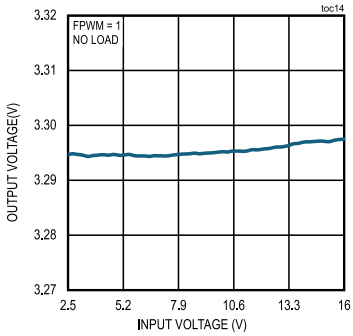
3.3V OUTPUT



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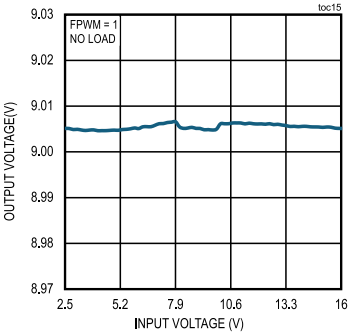

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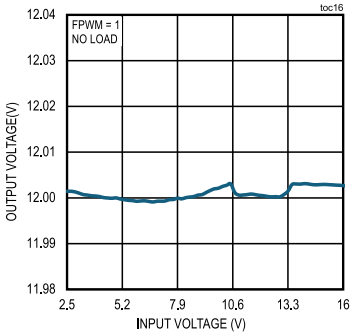
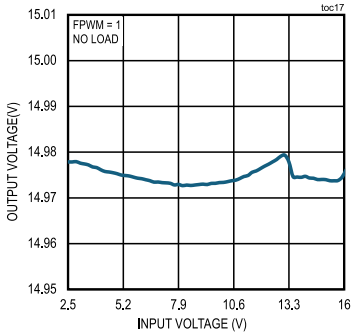
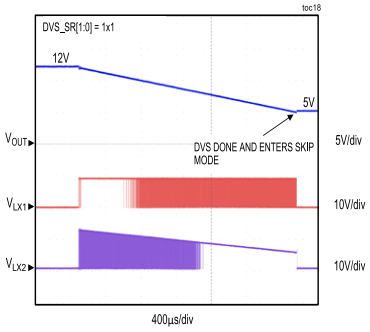
12V OUTPUT



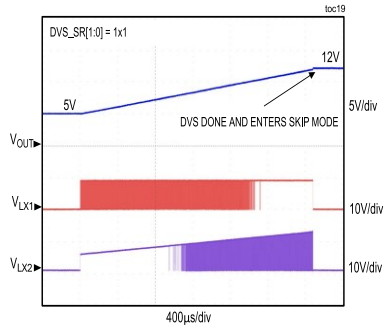
LINE REGULATION
12V OUTPUT



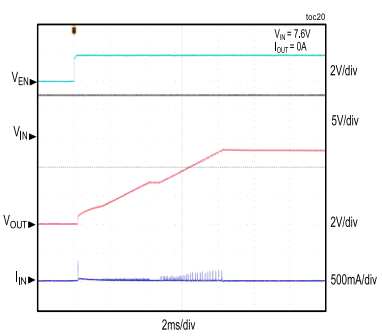
DYNAMIC VOLTAGE SCALING



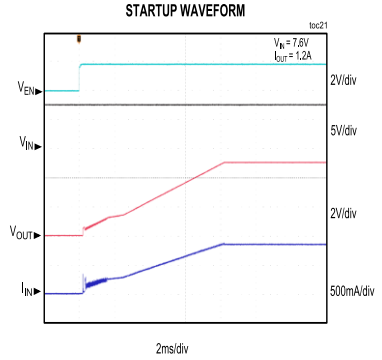
DYNAMIC VOLTAGE SCALING



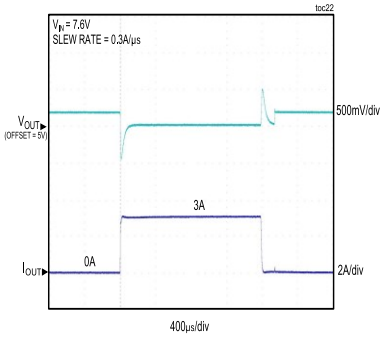
STARTUP WAVEFORM



STARTUP WAVEFORM



LOAD TRANSIENT RESPONSE
5V OUTPUT



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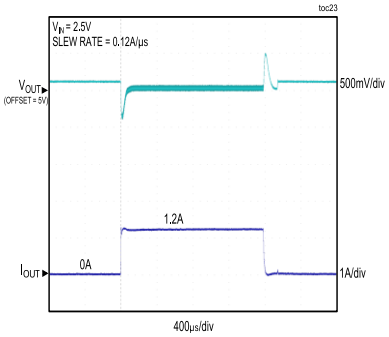
5V OUTPUT



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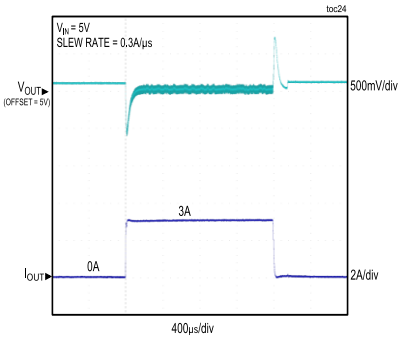
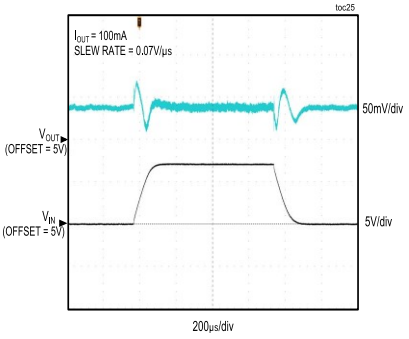
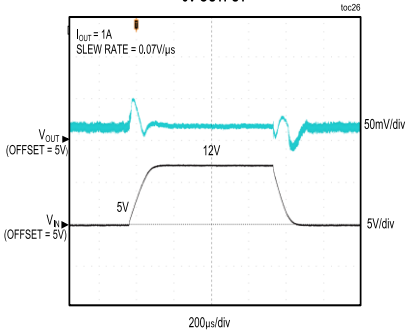
5V OUTPUT



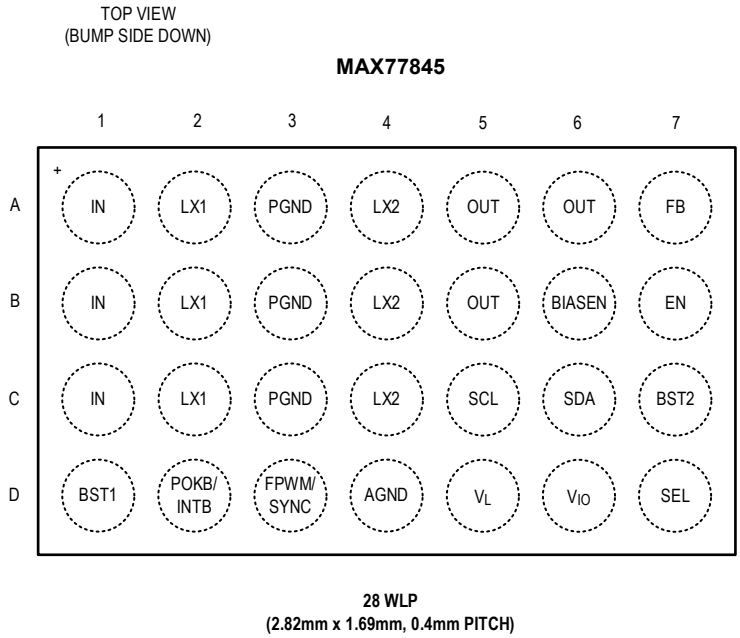
LINE TRANSIENT RESPONSE
5V OUTPUT



LINE TRANSIENT RESPONSE
5V OUTPUT



Pin Configurations

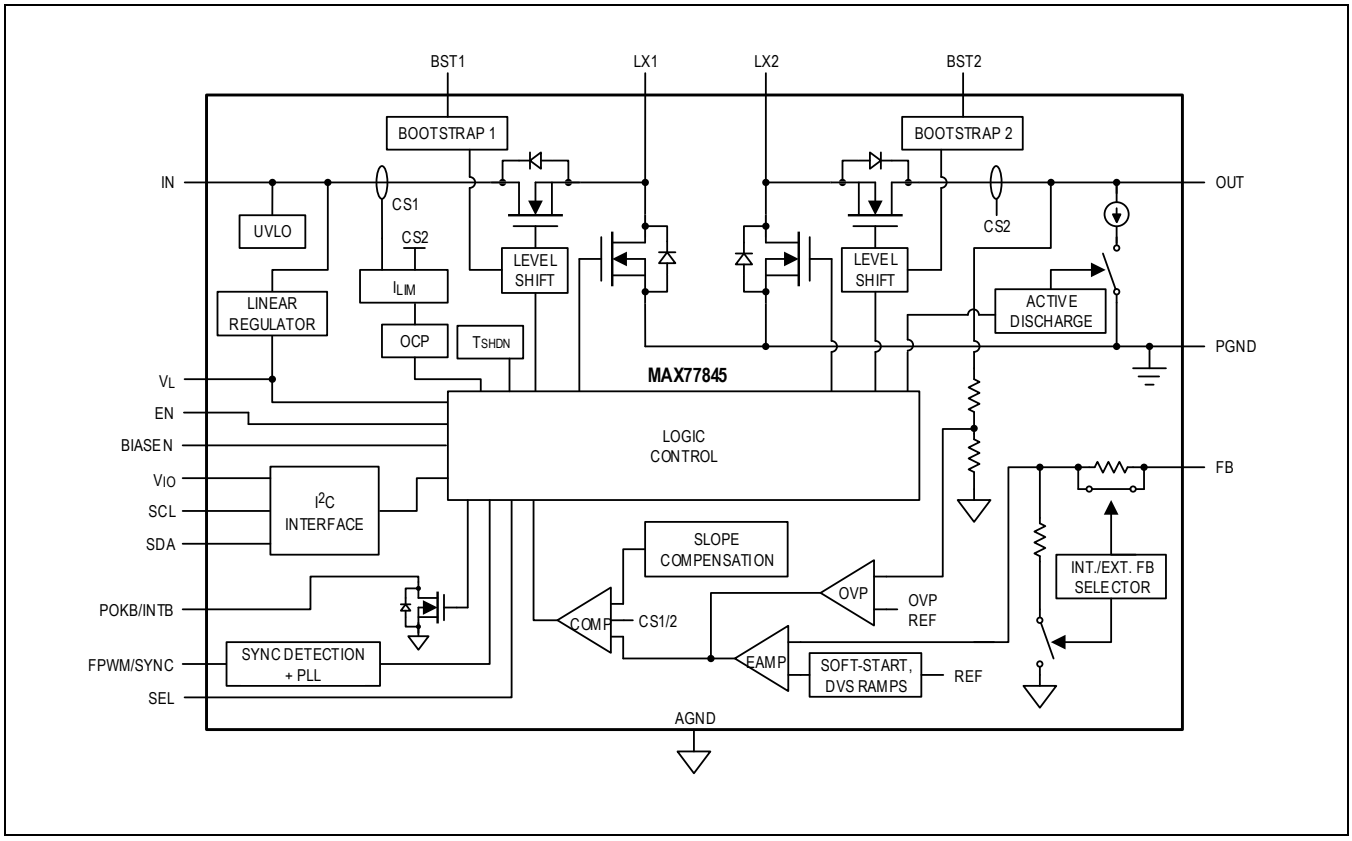


Pin Descriptions

PIN	NAME	FUNCTION	Type
A1, B1, C1	IN	Buck-Boost Input. Bypass to PGND with two 25V 10µF ceramic capacitors as close as possible.	Power Input
A2, B2, C2	LX1	Buck-Boost Switching Node 1	Power
A3, B3, C3	PGND	Power Ground. Connect to AGND on the PCB.	Ground
A4, B4, C4	LX2	Buck-Boost Switching Node 2	Power
A5, A6, B5	OUT	Buck-Boost Output. Bypass to PGND with two 25V 22µF ceramic capacitors as close as possible.	Power Output
A7	FB	Using Internal Feedback Resistors: Output Voltage Sense Input. Connect to the output at the point-of-load (close to output capacitor). Using External Feedback Resistors: Output Voltage Feedback Input. Connect to the center tap of an external resistor divider from OUT to AGND to set the output voltage.	Analog
B6	BIASEN	Active-High Internal Supply Enable Input. Pulldown internally with 800kΩ resistance. Connect to logic HIGH to enable I^2C interface and V_L before enabling buck-boost output.	Digital Input
B7	EN	Active-High Buck-Boost Enable Input. Pulldown internally with 0.1µA current source.	Digital Input
C5	SCL	I^2C Serial Interface Clock (High-Z in OFF State). Pullup to V_{IO} with a 1.5kΩ to 2.2kΩ resistor. Connect to AGND if not used.	Digital Input
C6	SDA	I^2C Serial Interface Data (High-Z in OFF State). Pullup to V_{IO} with a 1.5kΩ to 2.2kΩ resistor. Connect to AGND if not used.	Digital I/O
C7	BST2	LX2 High-Side FET Driver Supply. Connect a 25V 0.22µF ceramic capacitor between BST2 and LX2.	Power Input

D1	BST1	LX1 High-Side FET Driver Supply. Connect a 25V 0.22µF ceramic capacitor between BST1 and LX1.	Power Input
D2	POKB/INTB	Active-Low Open-Drain Status/Interrupt Output. Pullup to logic HIGH with a 15kΩ resistor. Do not connect to this pin if not in use.	Digital Output
D3	FPWM/SYNC	Active-High Forced-PWM Mode Control and External Clock Synchronization Input. Connect to AGND to enable SKIP mode, connect to logic HIGH to Force PWM mode, or connect to an external clock to enable externally synchronized FPWM mode.	Digital Input
D4	AGND	Analog Ground. Connect to PGND on the PCB.	Ground
D5	V_L	Low-Voltage Internal Supply. Powered from IN. Bypass to AGND with a 10V 2.2µF ceramic capacitor. Do not load this pin externally.	Analog
D6	V_{IO}	IO Voltage Supply. Bypass to AGND with a 6.3V 0.47µF ceramic capacitor. The I^2C serial interface is enabled when IN and V_{IO} are valid. Registers are held in reset, and the regulator remains disabled when the voltage on this pin is invalid. Connect this pin to V_L in standalone mode of operation.	Power Input
D7	SEL	Configuration Selection. Connect a resistor between SEL and AGND to configure internal/external feedback, switching current limit, and I^2C serial interface address.	Analog

Functional Diagrams



Detailed Description

General Description

The MAX77845 is a high-efficiency, high-performance buck-boost converter. It supports a wide input voltage range from 2.5V to 16V, enabling direct conversion from various sources, including up to 3-cell Li-ion batteries, USB Power Delivery (USB PD), and 12V DC supply rails. Its wide output voltage range of 3V to 15V accommodates a broad range of applications.

The device delivers an output current of up to 4.5A in Buck mode and up to 3A in Boost mode. It operates in PWM mode and incorporates automatic SKIP mode to enhance light-load efficiency. With a peak efficiency of 94%, low quiescent current, and compact solution size, the MAX77845 is well-suited for battery-powered, space-constrained designs.

The default output voltage is 5V when using internal feedback resistors. Alternate default voltages can be configured using external feedback resistors. Output voltage is also adjustable dynamically through an I2C-compatible interface.

Dedicated control pins EN, BIASEN, POKB/INTB, FPWM/SYNC, and SEL enable direct hardware control. Additional programmable features, including soft-start time, dynamic voltage scaling (DVS) slew rate, switching current limit, and switching frequency, are accessible through the I2C-compatible interface. Programmable switching frequency and external clock synchronization support system optimization for noise-sensitive environments.

The R_{SEL} pin and I2C-configurable switching current limit allow the use of low-profile, compact external components optimized for specific applications. Integrated protection features ensure safe operation under abnormal conditions.

The MAX77845 is available in a compact 2.82mm × 1.69mm, 28-bump wafer-level package (WLP).

Enable Control

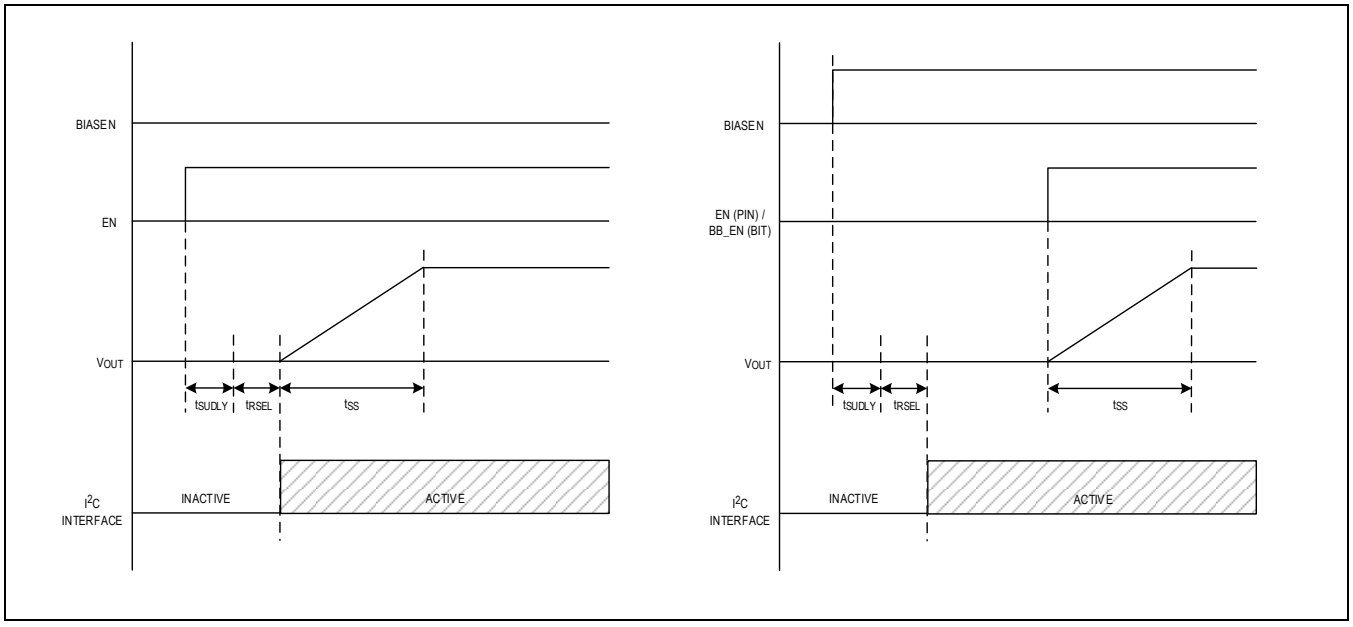


Figure 1. Start-Up Waveform

Pulling either the BIASEN or EN pin high to enable the IC's internal bias circuitry (V_L). As soon as the V_L supply becomes stable (typically within 100µs (t_{SUDLY})), the IC reads the R_{SEL} value for configuring the device (which takes typically 200µs (t_{RSEL})). See the *SEL Pin Configuration* section for more information. Provide a valid V_{IO} voltage to enable the I2C interface. Pull the EN pin high or set the BB_EN bit through I2C to initiate the buck-boost soft-start process (see the *Soft-Start* section). Enabling the I2C interface by pulling the BIASEN pin high (without pulling the EN pin high) allows the host processor to modify configuration settings before activating the Buck-Boost output.

It is possible to use the internal regulator V_L to provide power to the V_{IO} pin, or to use V_{IN} to control the EN pin. See the *Non-I2C and Standalone Configuration* section for more information.

After the buck-boost startup, pull the EN pin low and clear the BB_EN bit through I²C to disable the buck-boost output. To disable V_L and completely shut down the IC, pull both EN and BIASEN pins low. *Table 1* details the interaction between the EN pin, the BIASEN pin, and the BB_EN bit. While the BIASEN pin remains high, the I²C interface is enabled, and all register settings are kept.

Table 1. Enable Logic

EN (PIN)	BIASEN (PIN)	BB_EN (BIT)	V_L AND I²C SERIAL INTERFACE	BUCK-BOOST OUTPUT	REGISTER RESET	INPUT CURRENT (TYP)
Low	Low	X	Disabled	Disabled	True	2µA
Low	High	0 (default)	Enabled	Disabled	False	20µA
Low	High	1	Enabled	Enabled	False	50µA
High	X	X	Enabled	Enabled	False	50µA

**Input current numbers are typical values, at no load, and in SKIP mode (no switching).*

Soft-Start

The IC has an internal soft-start timer (t_{SS}) that controls the ramp time of the output as the buck-boost is starting. Soft-start limits inrush current during buck-boost startup. The SS_TM sets the timer [1:0] bitfield, with default values of 2ms to the default V_{REF} 0.30518V. Length of t_{SS} depends on the set V_{REF} value. If the switching current limit threshold I_{LIM} is set to 5A (ILIM[1:0] = 0b00), I_{LIM} is temporarily reduced to 3.4A during soft-start and returns to normal after t_{SS} finishes. DVS is disabled during soft-start. If VREF[9:0] is changed during soft-start, DVS starts after soft-start completes.

When the OCP_LCH bit is set (MAX77845C default), if V_{OUT} fails to reach POK level V_{POK_R} (typically 95% of the V_{OUT} target) after t_{SS} finishes, the IC enters soft-start fault, sets POK_I fault interrupt, and latches off. See the *Immediate Latch-Off Conditions* section for more information.

Table 2. Soft-Start Current Limit

ILIM[1:0] BITFIELD	NORMAL CURRENT LIMIT (I_{LIM}) (A)	SOFT-START CURRENT LIMIT (I_{LIM_SS}) (A)
00 (0x0)	5.0	3.4
01 (0x1)	3.4	
10 (0x2)	1.8	1.8
11 (0x3)	1.0	1.0

Immediate Latch-Off Conditions

The IC automatically shuts down to protect itself under specific fault conditions. Events in the following categories indicate potentially hazardous system states.

Under **immediate shutdown conditions**, the IC disables the buck-boost output, turns off the I²C interface, and resets all registers until the fault condition clears.

Under **latch-off conditions**, the IC disables the buck-boost output and clears the BB_EN bit if set, while keeping the I²C interface active and preserving register values.

Immediate Shutdown Condition:

- Undervoltage Lockout (UVLO)

Latch-Off Conditions:

- Thermal Shutdown (T_{SHDN})
- Overcurrent Protection (OCP)
- Output Short-Circuit Protection (SCP)
- Soft-Start Fault

To recover from latch-off after the fault clears, set the BB_EN bit or power cycle the EN pin.

Output Active Discharge

The IC integrates an internal active discharge switch between OUT and PGND for discharging the output capacitor when the buck-boost output is disabled (by a shutdown event or by any conditions described in the *Immediate Latch-Off Conditions* section, except for thermal shutdown). The discharge current is 5mA (typ). When the active discharge is enabled, all enable control signals (EN pin, BIASEN pin, BB_EN bit) are ignored. After V_{OUT} has discharged below 1V (typ) or active discharge has been enabled for 128ms (typ), whichever occurs sooner, active discharge is disabled. When the buck-boost regulator is operating, the internal discharging switch is disconnected from the output. Active discharge can be completely disabled (that is, it does not turn on when the buck-boost output is disabled) by clearing the AD_EN bit through I^2C.

Note: Active discharge function is disabled when V_{OUT} discharged below 1V. Customers are advised to account for this behavior in their application design.

Buck-Boost Regulator Control Scheme

The buck-boost regulator employs a four-switch H-bridge topology to maintain output voltage regulation across the input voltage range. It operates using a fixed-frequency pulse-width modulation (PWM) control scheme. The switching frequency is configured through the FREQ[1:0] bitfield.

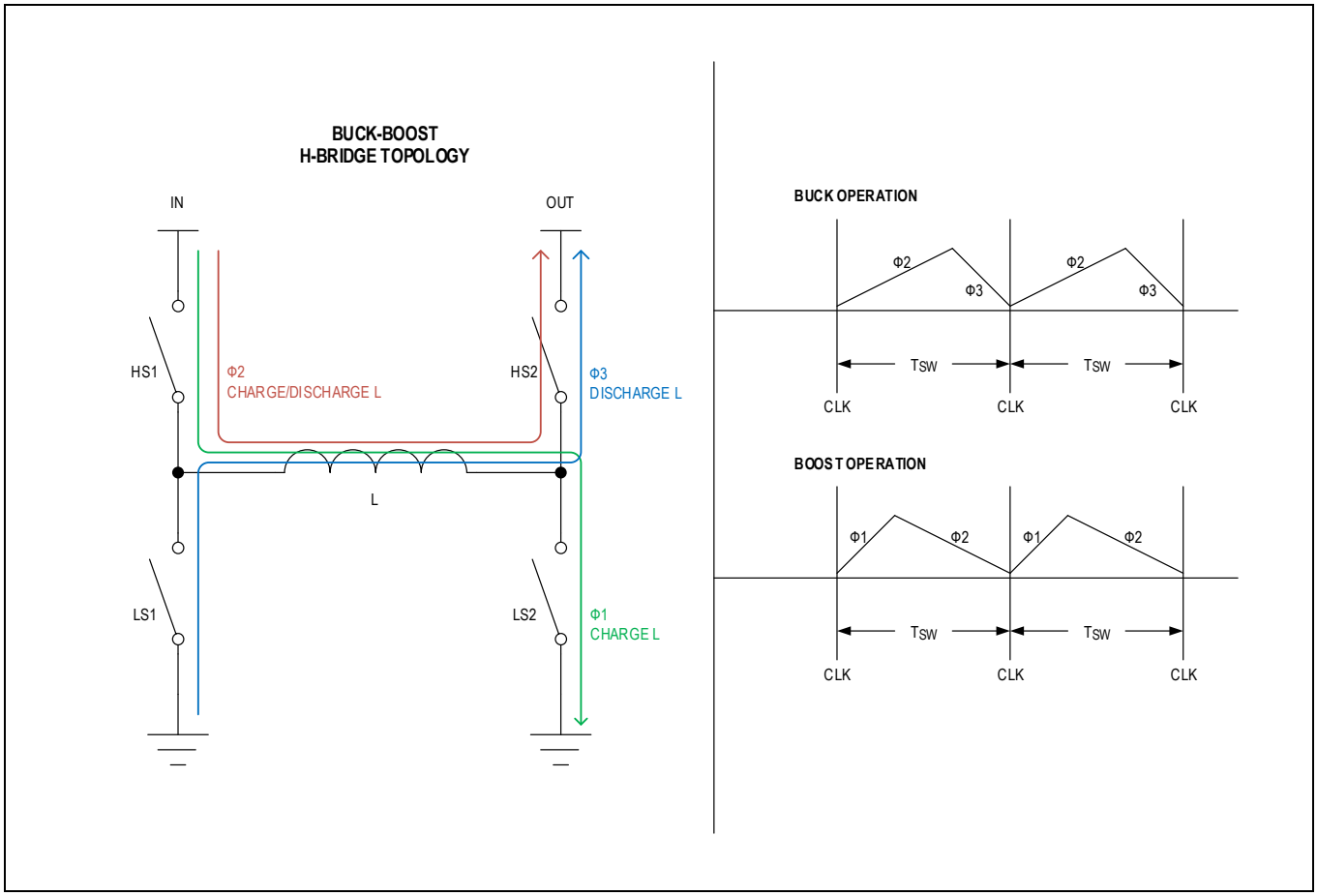


Figure 2. Buck-Boost H-Bridge Topology

Mode Control (FPWM)

At no-load or light-load conditions, the IC transitions to SKIP mode operation to improve efficiency. In SKIP mode, the IC terminates switching and enters sleep mode when the output voltage V_{OUT} approaches the SKIP mode upper threshold, V_{SKIP_UPPER} (typically 3% above the V_{OUT} target). The IC wakes up and resumes switching when V_{OUT} falls below the SKIP mode lower threshold, V_{SKIP_LOWER} (typically 1% above the V_{OUT} target). As a result, V_{OUT} is regulated between V_{SKIP_UPPER} and V_{SKIP_LOWER}, and the V_{OUT} ripple frequency changes depending on the load condition. The IC automatically transitions from SKIP mode to PWM mode when load current exceeds a certain threshold.

FPWM/SYNC pin is an active-high digital input that controls the buck-boost regulator's mode. Pull the FPWM/SYNC pin low to enable automatic SKIP mode. Pull the FPWM/SYNC pin high to enable forced-PWM (FPWM) mode. Always drive this pin to prevent mode chatter. FPWM mode enables the buck-boost regulator to operate at a constant frequency, particularly at light loads, and is beneficial for applications requiring the lowest output ripple. In contrast, SKIP mode helps maximize the buck-boost regulator's efficiency at light loads. FPWM mode can also be enabled by setting the FPWM bit through I^2C. FPWM/SYNC input can also be used for external clock synchronization. See the *External Clock Synchronization (SYNC)* section for more information.

Table 3. Buck-Boost Mode Control

FPWM/SYNC (PIN)	FPWM (BIT)	BUCK-BOOST MODE
Low	0	Automatic SKIP mode
High	X	FPWM mode (internal clock)
Low/High	1	FPWM mode (internal clock)
Clock (within f_{SYNC})	X	FPWM mode (external clock)

Regardless of the buck-boost mode setting, the IC enters FPWM mode when V_{OUT} is changed to a different target (DVS) to speed up the transition time. During DVS events that transition from a higher V_{OUT} to a lower one, the IC enters FPWM mode when V_{OUT} falls below V_{SKIP_LOWER} of the old V_{TARGET} and stays in FPWM mode until V_{OUT} falls below V_{SKIP_UPPER} of the new V_{TARGET}. Then V_{OUT} naturally drops based on the output load condition until it falls to V_{SKIP_LOWER}, at which point the SKIP mode switching cycle resumes. *Figure 3* illustrates this operation during DVS.

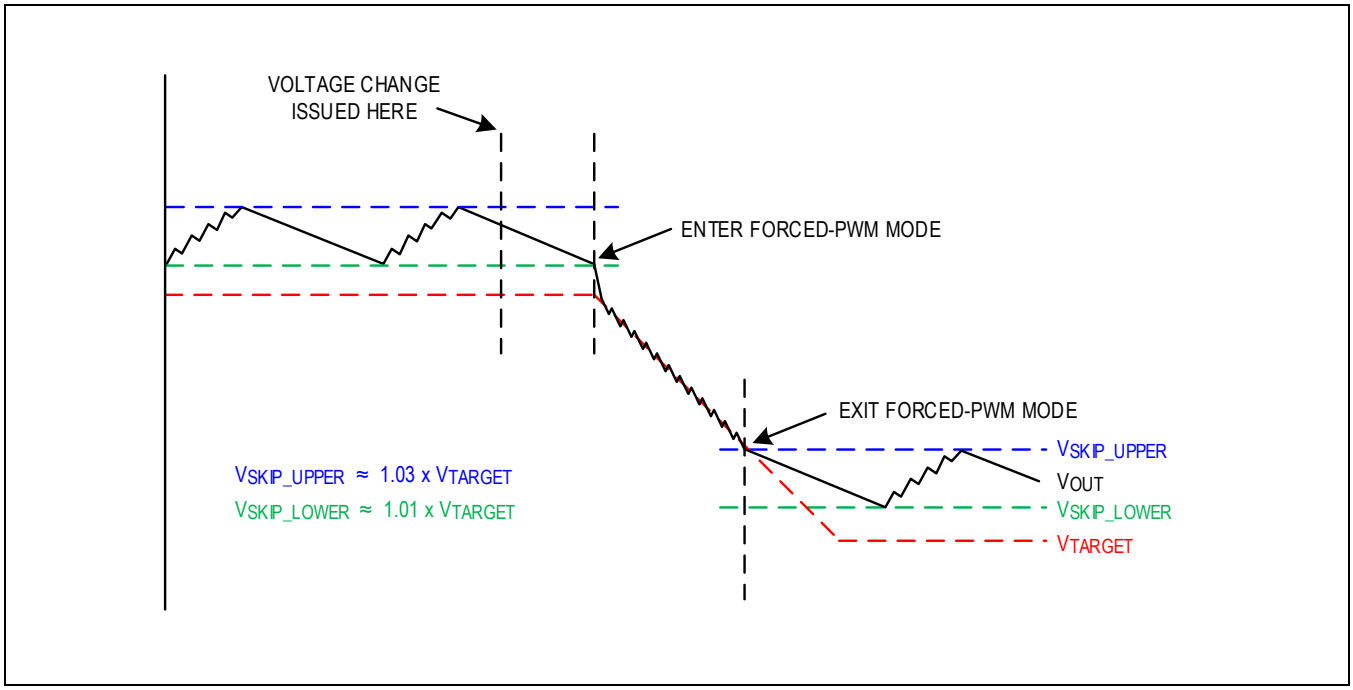


Figure 3. SKIP Mode Threshold and FPWM Mode Operation During DVS

External Clock Synchronization (SYNC)

Provide an external clock signal (close to 50% duty cycle) to FPWM/SYNC with a frequency inside the valid range (f_{SYNC}) to enable externally synchronized FPWM mode. The valid lockable range shifts depending on the chosen internal switching frequency FREQ[1:0]. External synchronization can only occur after the buck-boost output is enabled, the soft-start process is complete, and the external signal's frequency is stable. An internal digital state machine evaluates the external clock frequency on a cycle-by-cycle basis to determine if the signal's frequency is within the valid range. Suppose the logic detects 10 consecutive cycles within the valid range. In that case, the buck-boost immediately synchronizes the beginning of the next on-time cycle with the rising edge of the external clock on FPWM/SYNC. The SYNC status bit is set. The converter maintains on-time synchronization as long as each subsequent external clock cycle remains within the valid range. If the logic detects invalid external clock cycles (rising edges that occur too quickly or too slowly), the converter immediately reverts to its internal oscillator. The SYNC status bit is cleared, and the SYNC_I interrupt bit is set. The converter returns to SKIP mode when the FPWM bit is set to zero and FPWM/SYNC asserts low for approximately 5µs.

Table 4. Valid Synchronization Frequency Range (f_{SYNC})

FREQ[1:0] BITFIELD	INTERNAL SWITCHING FREQUENCY (TYP) (MHz)	MINIMUM VALID SYNC FREQUENCY (MHz)	MAXIMUM VALID SYNC FREQUENCY (MHz)
00 (0x0)	1.2	0.84	1.50
01 (0x1)	1.5	1.05	1.88
10 (0x2)	1.8	1.26	2.25
11 (0x3)	2.1	1.47	2.60

Output Voltage Configuration

The IC supports a wide output voltage range between 3V and 15V. The use of internal feedback resistors provides benefits of fewer external components and less overall solution size, while the use of external feedback resistors allows for customizable output voltage V_{OUT} at startup without using the I²C serial interface. The selection between using internal or external feedback resistors is configurable by R_{SEL}. See the *SEL Pin Configuration* section for more information.

Internal Feedback Resistor Configuration

When using internal feedback resistors, the V_{OUT} range is between 3V and 15V in 20mV steps. The default V_{OUT} is 5V (V_{REF} = 0.30518V). Use the appropriate R_{SEL} value to configure the IC for using internal feedback resistors, and connect the FB pin directly to the OUT pin at the local output capacitor.

External Feedback Resistor Configuration

When using external feedback resistors, the actual output voltage range and step size depend on the ratio of the external feedback resistor to the internal feedback resistor. Use the appropriate R_{SEL} value to configure the IC for use with external feedback resistors. Connect a resistor divider between OUT, FB, and AGND, as shown in *Figure 4*. It is also recommended to add a 10 pF feedforward capacitor (CFF) in parallel with the top feedback resistor (R_{TOP}). Choose R_{TOP} (from OUT to FB) between 150kΩ and 330kΩ. Resistors with 1% tolerance (or better) are highly recommended to keep the accuracy of V_{OUT}. Calculate the value of R_{BOT} (from FB to AGND) for the desired V_{OUT} at startup with the following equation:

$$R_{BOT} = \frac{R_{TOP} \times V_{REF}}{V_{OUT} - V_{REF}}, V_{OUT} \leq V_{OVP}$$

where V_{REF} is the default internal reference voltage.

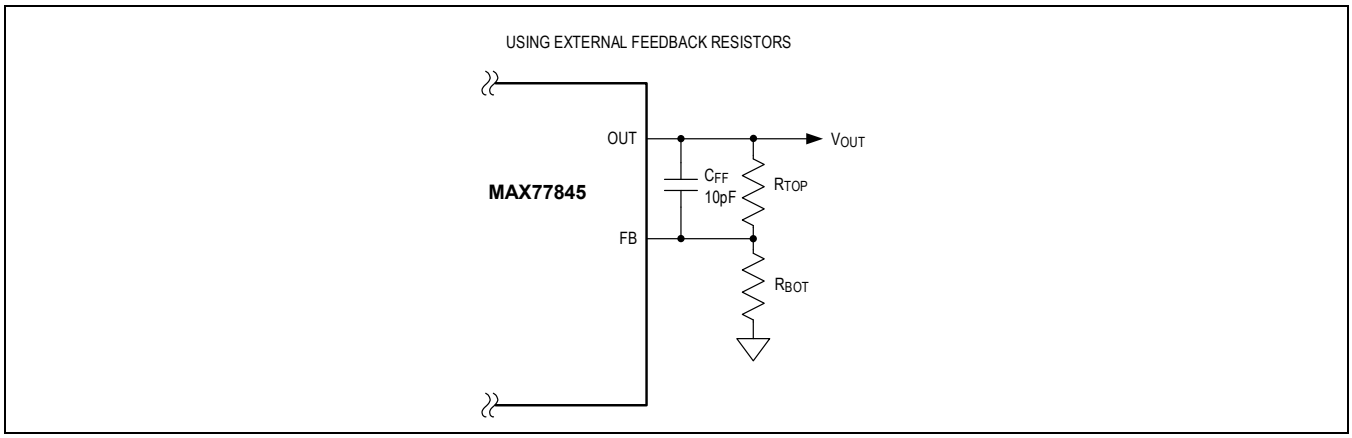


Figure 4. Connecting External Feedback Resistors

With a default V_{REF} of 0.30518V, Table 5 lists the recommended external feedback resistor values (in E192 series) for typical startup output voltages.

Table 5. Feedback Resistor Value Recommendations

DEFAULT V_{REF} (V)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	STARTUP V_{OUT} (V)	PROGRAMMABLE V_{OUT} RANGE (V)	V_{OUT} STEP SIZE (mV)
0.30518	205	23.2	3	3.0 to 9.0	12
	162	16.5	3.3	3.0 to 9.9	13.2
	Internal Feedback Resistors		5	3.0 to 15	20
	160	5.62	9	5.4 to 15	36
	182	4.75	12	7.2 to 15	48
	180	3.74	15	9.0 to 15	60

Dynamic Voltage Scaling (DVS)

V_{OUT} is dynamically adjustable by programming V_{REF} through the I²C serial interface. The bitfield VREF[9:0] sets the V_{REF}. V_{REF} ranges between 0.18311V and 0.91431V in 1.22mV steps. When using internal feedback resistors, V_{OUT} ranges between 3V and 15V in 20mV steps, and it can be calculated with the following equation:

$$V_{OUT} = V_{REF} \times 16.4$$

When using external feedback resistors, the V_{OUT} range and step size vary depending on the values of the external feedback resistors. The V_{OUT} step size can be calculated with the following equation:

$$V_{OUT_STEP} = \left(\frac{1.22mV}{R_{BOT}}\right) \times (R_{BOT} + R_{TOP})$$

To calculate the V_{OUT} range, use the following equation and plug in the minimum V_{REF} of 0.18311V and maximum V_{REF} of 0.91431V:

$$V_{OUT} = \left(\frac{V_{REF}}{R_{BOT}}\right) \times (R_{BOT} + R_{TOP}), V_{OUT} \le V_{OVP}$$

Note that V_{OUT} cannot exceed output voltage range, or it triggers overvoltage protection. See the *Overvoltage Protection (OVP)* section for more information.

The bitfield DVS_SR[1:0] sets the V_{REF} DVS ramp rate ($\Delta V_{REF}/\Delta t$), with the default value of 4/3mV/µs. The actual V_{OUT} DVS ramp rate ($\Delta V_{OUT}/\Delta t$) can be calculated from the V_{REF} DVS ramp rate ($\Delta V_{REF}/\Delta t$) using the above equations for external feedback resistors. For example, if using internal feedback resistors, the default $\Delta V_{REF}/\Delta t$ of 4/3mV/µs corresponds to the $\Delta V_{OUT}/\Delta t$ of 21.87mV/µs.

SEL Pin Configuration

The SEL pin allows a single resistor (R_{SEL}) to be connected from the SEL pin to AGND, which configures the switching frequency, high-side switching current limit threshold (I_{LIM}), I²C serial interface target address, and the use of internal or external feedback resistors. Resistors with 1% tolerance (or better) should be used for R_{SEL}. *Table 6* lists the nominal R_{SEL} values along with their corresponding settings. R_{SEL} decoded settings are used to set initial values upon enabling the IC. Afterwards, all settings can be changed through the I²C interface. Additionally, two OTP configurations are available for I_{LIM} selection: 5A/3.4A or 1A/1.8A.

Table 6. R_{SEL} Selection Table

R_{SEL} (Ω)	I²C ADDRESS (7-BIT)	TYPICAL I_{LIM} (A)		SWITCHING FREQUENCY (MHz)	R_{FB} SELECTION
		OTP = 0	OTP = 1		
GND	110 0110 (0x66)	5.0	1	2.1	External feedback resistors
200	110 0111 (0x67)				
309	110 1110 (0x6E)				
422	110 1111 (0x6F)				
536	110 0110 (0x66)	3.4	1.8		
649	110 0111 (0x67)				
768	110 1110 (0x6E)				
909	110 1111 (0x6F)				
1050	110 0110 (0x66)	5.0	1	1.5	
1210	110 0111 (0x67)				
1400	110 1110 (0x6E)				
1620	110 1111 (0x6F)				
1870	110 0110 (0x66)	3.4	1.8		
2150	110 0111 (0x67)				
2490	110 1110 (0x6E)				
2870	110 1111 (0x6F)				
3740	110 0110 (0x66)	5.0	1	2.1	Internal feedback resistors
8060	110 0111 (0x67)				
12400	110 1110 (0x6E)				
16900	110 1111 (0x6F)				
21500	110 0110 (0x66)	3.4	1.8		
26100	110 0111 (0x67)				
30900	110 1110 (0x6E)				
36500	110 1111 (0x6F)				
42200	110 0110 (0x66)	5.0	1	1.5	
48700	110 0111 (0x67)				
56200	110 1110 (0x6E)				
64900	110 1111 (0x6F)				
75000	110 0110 (0x66)	3.4	1.8		
86600	110 0111 (0x67)				
100000	110 1110 (0x6E)				
OPEN	110 1111 (0x6F)				

Internal Compensation Options

For designs looking to optimize its performance, the COMP[2:0] bitfield for internal compensation adjustment is available through the I2C serial interface. For those systems that do not utilize the I2C serial interface, stability can still be optimized by adjusting output capacitance. In general, performance can be further optimized by lowering the COMP[2:0] bitfield value or by adding additional output capacitance.

Power-OK (POK)

The IC features Power-OK (POK) comparator to monitor the regulation status of Buck-Boost output. The POK monitor continuously updates based on actual V_{OUT} level while the buck-boost regulator is enabled. The POK status bit clears when V_{OUT} falls below 85% (typical) of the target voltage, and set when V_{OUT} rises above 95% (typical) of the target voltage. During DVS event, POK monitor update is temporarily disabled, and POK status bit holds the value prior to DVS event. POK monitor update resumes after DVS finishes. POK_I fault interrupt sets when POK status bit transitions from 1 to 0 or when soft-start fault occurs.

Fault Event Status/Interrupts

The IC includes fault status/interrupts to signal any hazardous states. The fault status bits in register 0x10 (STAT) reflect the IC's real-time status, while the interrupt bit in register 0x11 (INT) is triggered and latched once the corresponding fault state occurs, and it is cleared when read. Any of the following fault events asserts the corresponding bits in the STAT and INT registers.

- SYNC: See the *External Clock Synchronization (SYNC)* section
- POK: See the *Power-OK (POK)* section
- OVP: See the *Overvoltage Protection (OVP)* section
- SCP: See the *Output Short-Circuit Protection (SCP)* section
- TSHDN: See the *Thermal Shutdown (T_{SHDN})* section
- OCP: See the *Overcurrent Protection (OCP)* section

The fault interrupt bits can be masked off by setting the corresponding mask bitfield in register 0x12 (MASK). For example, when the T_{SHDN_M} bitfield is 1, the T_{SHDN_I} bitfield is not set when a thermal shutdown event occurs.

Table 7. Fault Status/Interrupt Bit Change Condition

FUNCTION	STATUS BIT SET CONDITION	STATUS BIT RESET CONDITION	INTERRUPT BIT SET CONDITION	INTERRUPT BIT RESET CONDITION
SYNC	Buck-boost sync'd to external clock	Buck-boost sync'd to internal clock	SYNC status bit transitions from 1 → 0	INT register is read
POK	$V_{OUT} > V_{POK_R}$	$V_{OUT} < V_{POK_F}$	POK status bit is 0, or a soft-start fault occurs	
OVP	$V_{OUT} > V_{OVP_R}$	$V_{OUT} < V_{OVP_F}$	Corresponding fault status bit transitions from 0 → 1	
SCP	$V_{OUT} < V_{SCP_TH}$	$V_{OUT} > V_{SCP_TH}$		
T_{SHDN}	$T_J > T_{SHDN_R}$	$T_J < T_{SHDN_F}$		
OCP	$I_L > I_{LIM}$	$I_L < I_{LIM}$ in the next clock cycle		

**With all fault interrupt bits unmasked (MASK = 0x00)*

POKB/INTB Output Pin

POKB/INTB is an active-low, open-drain digital output pin. Connect the POKB/INTB pin with a 15kΩ pull-up resistor to V_{IO}. This pin can be configured as either a POK pin or a fault interrupt pin, selectable by the POKBINTB bit in register 0x15 (BB_CFG2).

- POKBINTB = 0: POK pin (POKB).
- POKBINTB = 1: Fault interrupt pin (INTB).

When the pin is configured as a POK pin, the digital output signal on the POKB/INTB pin is the logical NOT of the POK status bit; that is, the pin is logic LOW when V_{OUT} is below the POK threshold. *Table 8* shows the truth table for the POKB/INTB pin when configured as a POK pin.

Table 8. POKB/INTB Pin Truth Table (POKBINTB = 0b0)

V_{OUT} CONDITION	POK BIT	POKB/INTB PIN
V_{OUT} < POK falling threshold	0	HIGH
V_{OUT} > POK rising threshold	1	LOW

When the pin is configured as a fault interrupt pin, the signal on the POKB/INTB pin is a logical NOR of all bits in the fault interrupt register (0x11, INT). In other words, the pin is logic LOW when an unmasked fault interrupt event occurs. *Table 9* shows the truth table of the POKB/INTB pin when the pin is configured as a fault interrupt pin, with all interrupt bits unmasked (MASK = 0x00).

Table 9. POKB/INTB Pin Truth Table (POKBINTB = 0b1)

SYNC_I BIT	POK_I BIT	OVP_I BIT	SCP_I BIT	TSHDN_I BIT	OCP_I BIT	POKB/INTB PIN
0	0	0	0	0	0	HIGH
1	X	X	X	X	X	LOW
X	1	X	X	X	X	LOW
X	X	1	X	X	X	LOW
X	X	X	1	X	X	LOW
X	X	X	X	1	X	LOW
X	X	X	X	X	1	LOW

**With all fault interrupt bits unmasked (MASK = 0x00)*

Protection Features

Undervoltage Lockout (UVLO)

The IC's undervoltage lockout (UVLO) feature prevents operation in abnormal input conditions. Regardless of BIASEN or EN pin status, the IC is in a shutdown state, and all registers are reset until the following conditions are cleared.

- IN UVLO: V_{IN} < Input UVLO Falling Threshold (V_{UVLO_F})
- V_{IO} UVLO: V_{VIO} < V_{IO} Valid Falling Threshold ($V_{VIO_VALID_F}$)

Overvoltage Protection (OVP)

The IC's overvoltage protection feature ensures that the output voltage V_{OUT} never exceeds the overvoltage limit threshold (V_{OVP}, 16.4V typical). In this fault condition, V_{OUT} rises to V_{OVP}. The IC detects overvoltage, sets OVP status and OVP_I interrupt bits, and activates overvoltage protection by disabling high-side MOSFETs and enabling low-side MOSFETs until V_{OUT} drops below the overvoltage release threshold (V_{OVP_REL}, 15.5V typical). As a result, V_{OUT} regulates between V_{OVP} and V_{OVP_REL}. When V_{OUT} falls below V_{OVP_REL}, OVP status bit self-clears.

Overcurrent Protection (OCP)

The IC features a robust switching-current limit scheme that protects the IC and the inductor during overload and fast-transient conditions. The current-sensing circuit uses current information from the high-side MOSFETs to determine the peak switching current ($R_{DS(ON)}$ x I_L). The bitfield ILIM[2:0] sets the peak switching inductor current limit I_{LIM}.

When the inductor current (I_L) reaches the programmed I_{LIM}, the IC enters the OCP state, setting the OCP status bit and the OCP_I interrupt bit. The inductor charging phase terminates, and the discharging phase (Φ3) begins for the rest of the switching period. The charging phase starts again at the next clock cycle. The OCP status bit self-clears when the inductor current no longer reaches I_{LIM} in the next clock cycle.

OCP_LCH bit controls the IC latch-off behavior in OCP state. When set, the IC activates a 200µs (typ) latch-off timer. When the timer expires (that is when I_L has reached I_{LIM} continuously for 200µs), the IC latches off the buck-boost regulator. If prior to latch-off, the overcurrent event disappears and I_L no longer reaches I_{LIM}, the timer reset.

Output Short-Circuit Protection (SCP)

If, during operation, V_{OUT} drops below the output short-circuit threshold, V_{SCP_TH} (selectable by the SCP_TH bit, as shown in *Table 10*), the IC enters the SCP state, sets the SCP status bit, and sets the SCP_I interrupt bit. Similar to the OCP state, the inductor charging phase terminates when I_L reaches the programmed I_{LIM}, and the discharging phase (Φ3) begins. However, unlike the OCP state, the discharging phase does not terminate until the inductor current falls below the valley current limit threshold (I_{LIM_VALLEY}), at which point the inductor charging phase follows. As a result, the effective switching frequency in the SCP state differs from the regular switching frequency set in the FREQ[1:0] register bitfield or the external clock. See *Table 11* for available I_{LIM} options and their corresponding I_{LIM_VALLEY} values.

SCP_LCH bit controls the IC latch-off behaviour in the SCP state. When set, the IC activates a 200µs (typ) latch-off timer. When the timer expires (that is, when V_{OUT} is below V_{SCP_TH} continuously for 200µs), the IC latches off the buck-boost regulator. If, prior to latch-off, the short-circuit event disappears and V_{OUT} reaches V_{SCP_TH}, the timer is reset.

Table 10. Output Short-Circuit Protection Thresholds

SCP_TH BITFIELD	SCP FALLING THRESHOLD	SCP RISING THRESHOLD
0	30% of V_{OUT} target	40% of V_{OUT} target
1	60% of V_{OUT} target	70% of V_{OUT} target

Table 11. Switching Current Limit Options

ILIM[1:0] BITFIELD	NORMAL CURRENT LIMIT (I_{LIM}) (A)	VALLEY CURRENT LIMIT (I_{LIM_VALLEY}) (A)
00 (0x0)	5.0	1.8
01 (0x1)	3.4	
10 (0x2)	1.8	0.3
11 (0x3)	1.0	

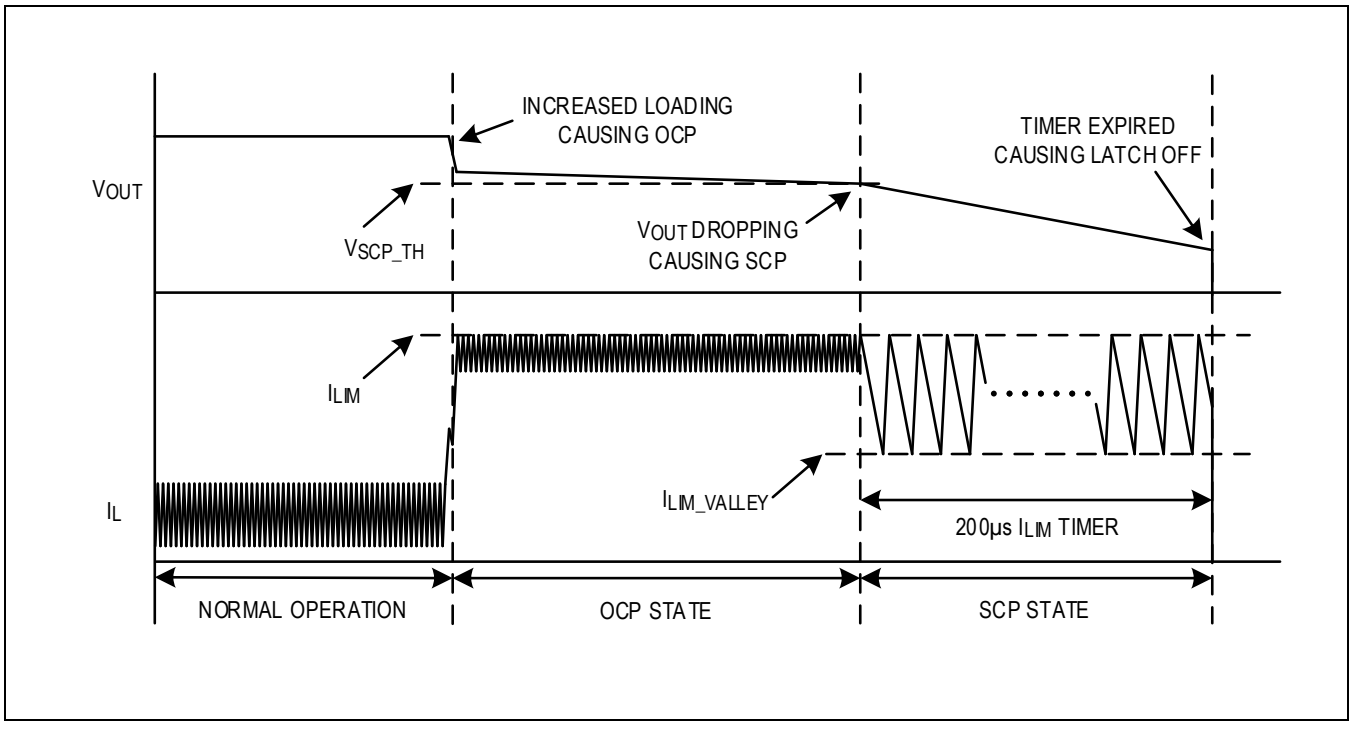


Figure 5. Overcurrent and Output Short-Circuit Behavior when OCP_LCH = 0 and SCP_LCH = 1 (MAX77845B Default)

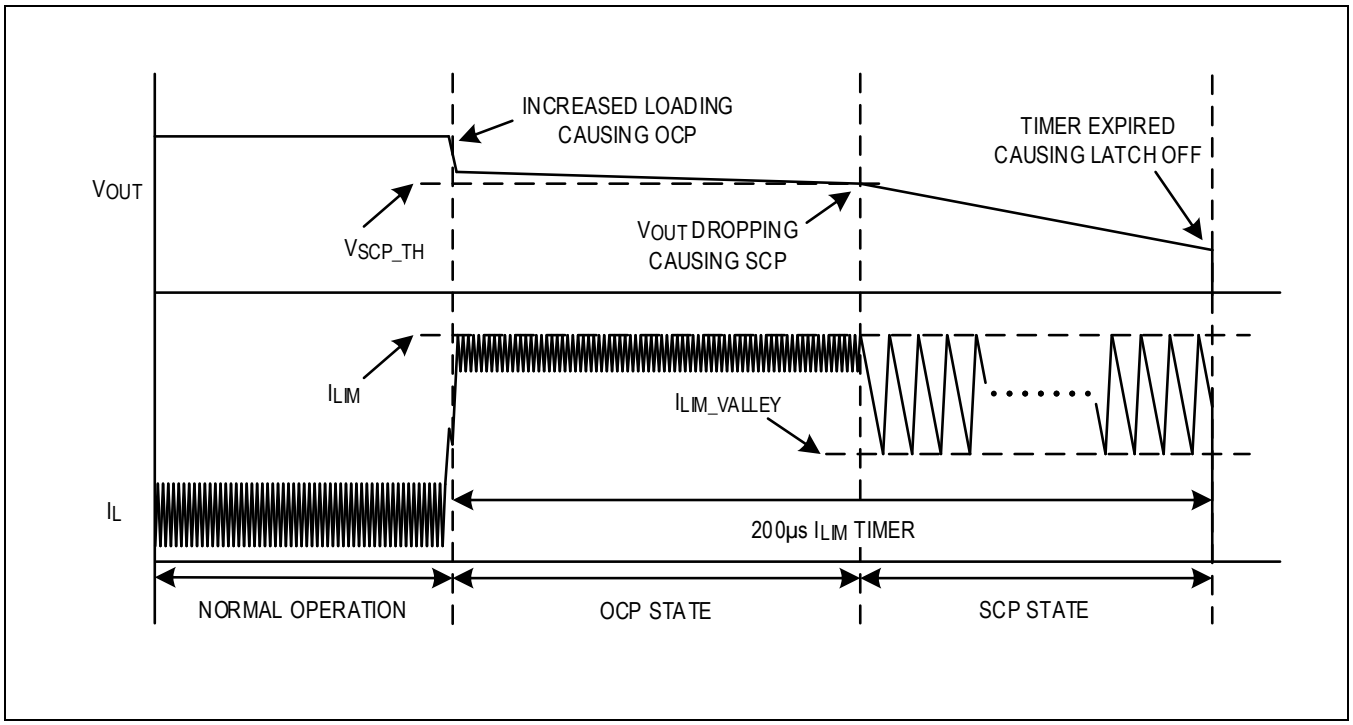


Figure 6. Overcurrent and Output Short-Circuit Behavior when OCP_LCH = 1 and SCP_LCH = 1 (MAX77845C Default)

Thermal Shutdown (T_{SHDN})

The IC contains an internal thermal protection circuit that monitors die temperature. The IC enters thermal shutdown (T_{SHDN}) when junction temperature (T_J) exceeds thermal shutdown rising threshold (T_{SHDN_R}, 150ºC typ). The IC is latched off and T_{SHDN} status and T_{SHDN_I} interrupt bits are set. Unlike other latch-off events, output active discharge is not activated even if AD_EN bit is 1. T_{SHDN} status bit self-clears when T_J falls below thermal shutdown hysteresis (T_{SHDN_HYS}, 20ºC typ).

Detailed Description–I²C Serial Interface

General Description

The I²C-compatible 2-wire serial interface is used for setting output voltage and other functions. See the *Register Map* for available settings.

The I²C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I²C bus is a multi-controller bus. The maximum number of devices that can be attached to the bus is limited only by the bus capacitance.

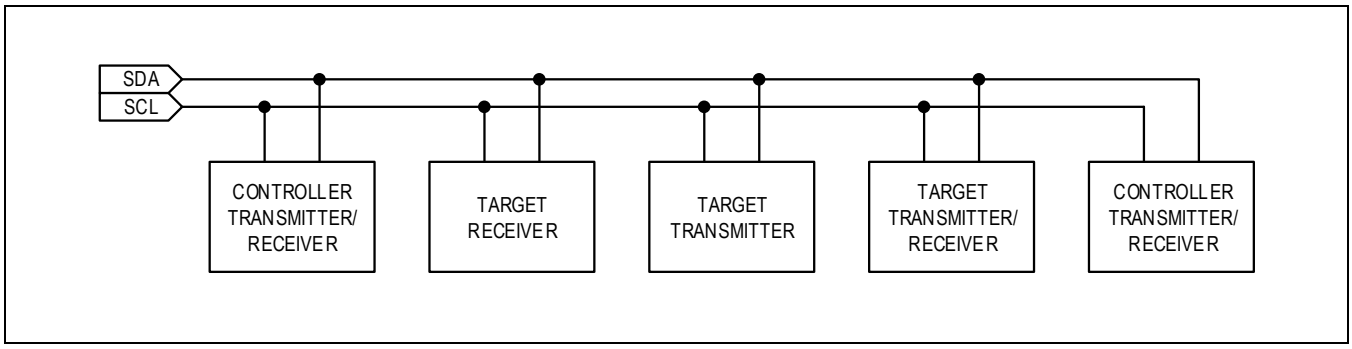


Figure 7. Functional Logic Diagram for the Communications Controller

Figure 8 shows an example of a typical I²C bus system. A device on the I²C bus that sends data to the bus is called a “transmitter.” A device that receives data from the bus is called a "receiver.” A device that initiates a data transfer and generates SCL clock signals to control the data transfer is called a “controller.” Any device being addressed by the controller is called a “target.” The MAX77845 is a target on the I²C bus and can function as both a transmitter and a receiver.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on the SDA must remain stable during the HIGH portion of the SCL clock pulse. Changes in the SDA while the SCL is HIGH are control signals (START and STOP conditions).

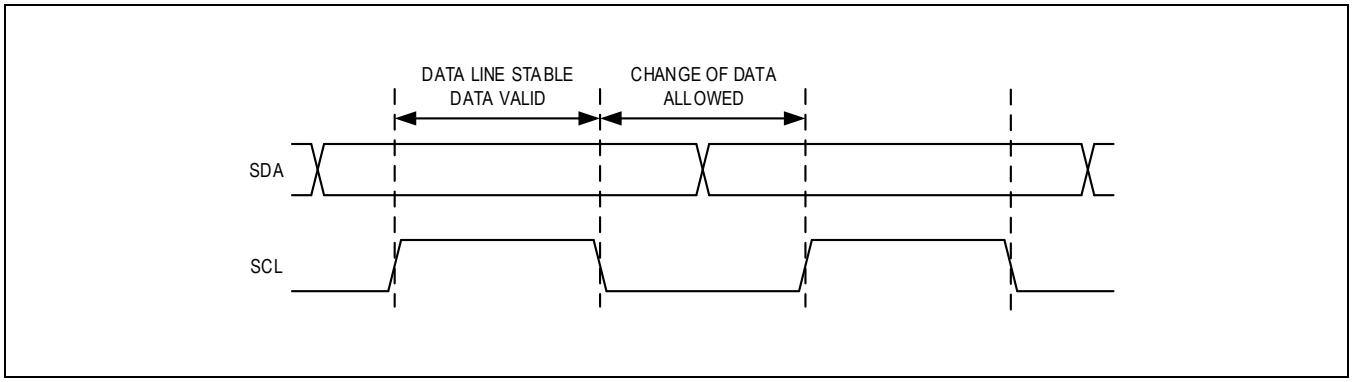


Figure 8. I²C Bit Transfer

START and STOP Conditions

When the I2C serial interface is inactive, SDA and SCL are idle HIGH. A controller device initiates communication by issuing a START condition (S). A START condition (S) is a HIGH-to-LOW transition on the SDA while the SCL is HIGH. A STOP condition (P) is a LOW-to-HIGH transition on the SDA while the SCL is HIGH.

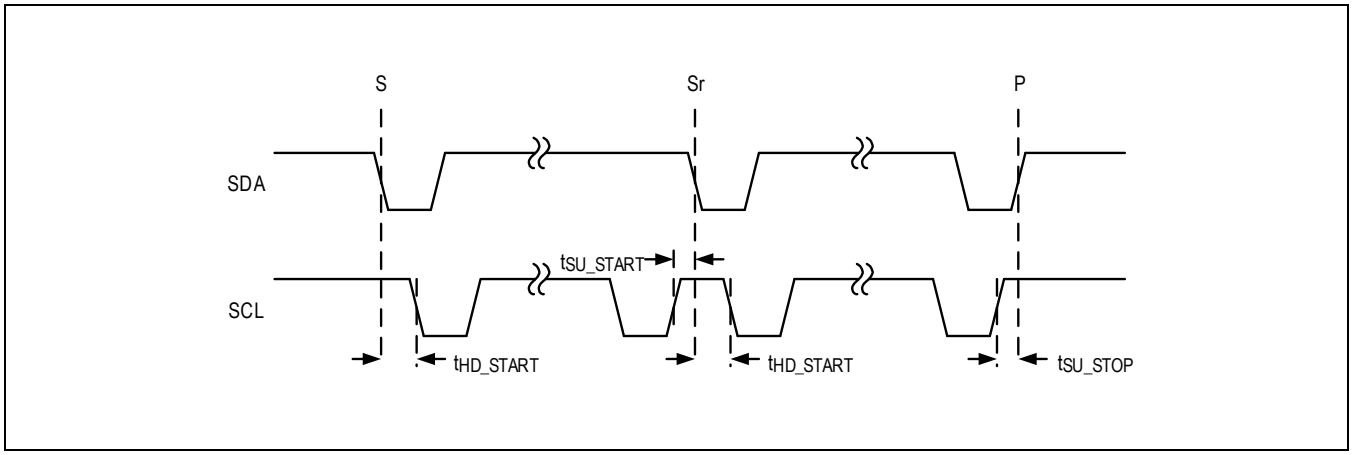


Figure 9. START and STOP Conditions

A START condition (S) from the controller device signals the beginning of a transmission. The controller terminates transmission by issuing a NOT-ACKNOWLEDGE (nA) followed by a STOP condition (P).

A STOP condition (P) frees the bus. To issue a series of commands to the target, the controller can use REPEATED START (Sr) commands instead of a STOP condition (P) to maintain control of the bus. In general, a REPEATED START (Sr) command is functionally equivalent to a regular START condition (S).

When a STOP condition (P) or an incorrect address is detected, the MAX77845 internally disconnects the SCL from the I2C serial interface until the next START condition (S) is detected, minimizing digital noise and feed-through.

Acknowledge Bit

Both the I2C bus controller device and target devices generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine-bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull the SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it LOW during the HIGH portion of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows the SDA to be pulled HIGH before the rising edge of the acknowledge-related clock pulse and maintains this HIGH state during the HIGH portion of the clock pulse.

Monitoring the acknowledge bits allows for the detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus controller should reattempt communication later.

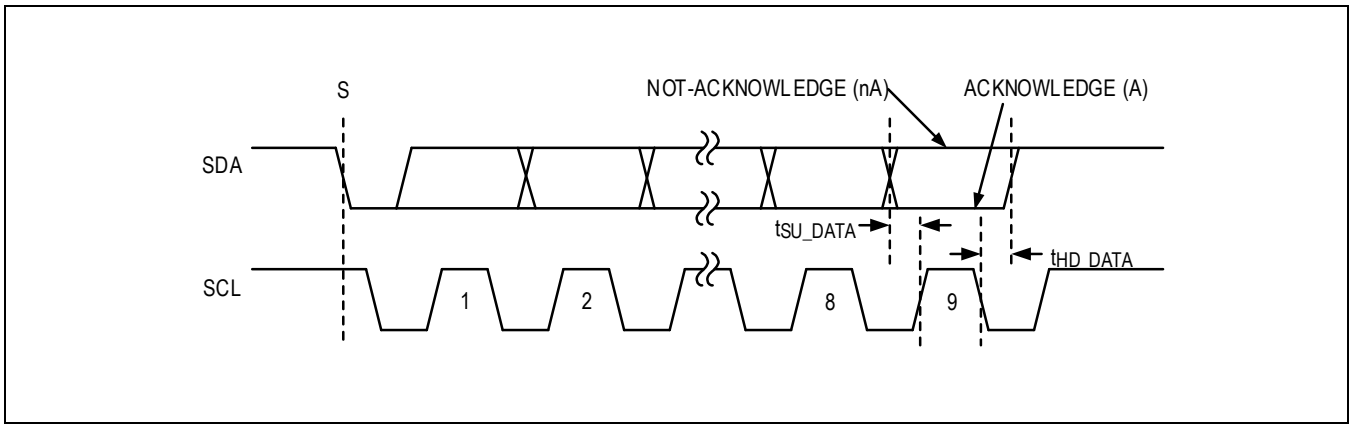


Figure 10. Acknowledge Bit

Target Address

Table 12 shows the available I²C target addresses of the MAX77845. The MAX77845 supports up to four different target addresses through R_{SEL} programming, allowing multiple devices on the same I²C bus line to be used simultaneously or resolving conflicts between target addresses in the system. See *Table 2* for the available R_{SEL} values and their corresponding I²C target addresses.

Table 12. MAX77845 I²C Target Addresses

7-BIT TARGET ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
110 0110 (0x66)	1100 1100 (0xCC)	1100 1101 (0xCD)
110 0111 (0x67)	1100 1110 (0xCE)	1100 1111 (0xCF)
110 1110 (0x6E)	1101 1100 (0xDC)	1101 1101 (0xDD)
110 1111 (0x6F)	1101 1110 (0xDE)	1101 1111 (0xDF)

Figure 11 shows the 7-bit target address at 0x66.

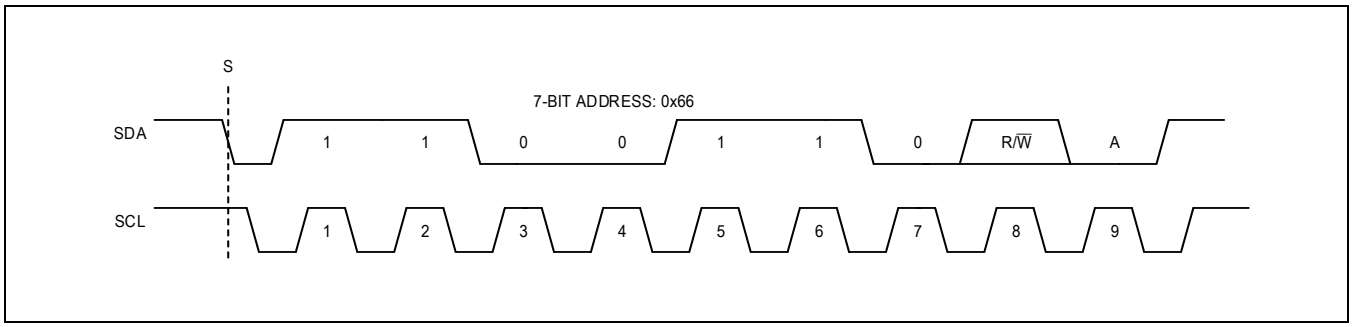


Figure 11. Target Address Byte Example

Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the controller device. The I²C specification allows slow target devices to alter the clock signal by holding down the clock line. The process in which a target device holds down the clock line is typically called clock stretching. The MAX77845 does not use any form of clock stretching to hold down the clock line.

General Call Address

The MAX77845 does not implement the I²C specification "General Call Address." The MAX77845 does not issue an ACKNOWLEDGE (A) if it detects the "General Call Address" (0000 0000).

Communication Speed

The MAX77845 supports the following communication speeds:

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast-mode plus)
- 0Hz to 3.4MHz (high-speed mode)

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The primary consideration when adjusting the bus speed within this range is the combination of the bus capacitance and pullup resistors. Higher time constants, created by the bus capacitance and pullup resistance (C x R), slow the bus operation. Therefore, when increasing bus speed, the pullup resistance must be decreased to maintain a reasonable time constant. In general, for a bus capacitance of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor dissipates power when the open-drain bus is at a low voltage. The lower the value of the pullup resistor, the higher the power dissipation (V^2/R).

Operating in high-speed mode requires some special considerations. The primary considerations with respect to the MAX77845 are as follows:

- The controller device shall use current source pullups to shorten the signal rise times.
- The target device must use a different set of input filters on its SDA and SCL lines to accommodate the higher bus speed.
- The communication protocols need to utilize the high-speed controller code.

At power-up and after each STOP condition (P), the MAX77845 input filters are set to standard mode, fast mode, or fast mode plus (that is 0Hz to 1MHz). To switch the input filters to high-speed mode, use the protocol described in the *Engage in High-Speed Mode* section.

Communication Protocols

The MAX77845 supports both writing to and reading from its registers.

Writing to a Single Register

Figure 12 shows the protocol for writing to a single register. This protocol is the same as the “Write Byte” protocol in the SMBus specification.

The “Write Byte” protocol is as follows:

1. The controller sends a START condition (S).
2. The controller sends the 7-bit target address followed by a write bit ($R/\overline{W} = 0$).
3. The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The controller sends an 8-bit register pointer.
5. The target acknowledges the register pointer.
6. The controller sends a data byte.
7. The target acknowledges the data byte. At the rising edge of the SCL, the data byte is loaded into its target register, and the data becomes active.
8. The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for operation at 1MHz or slower. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

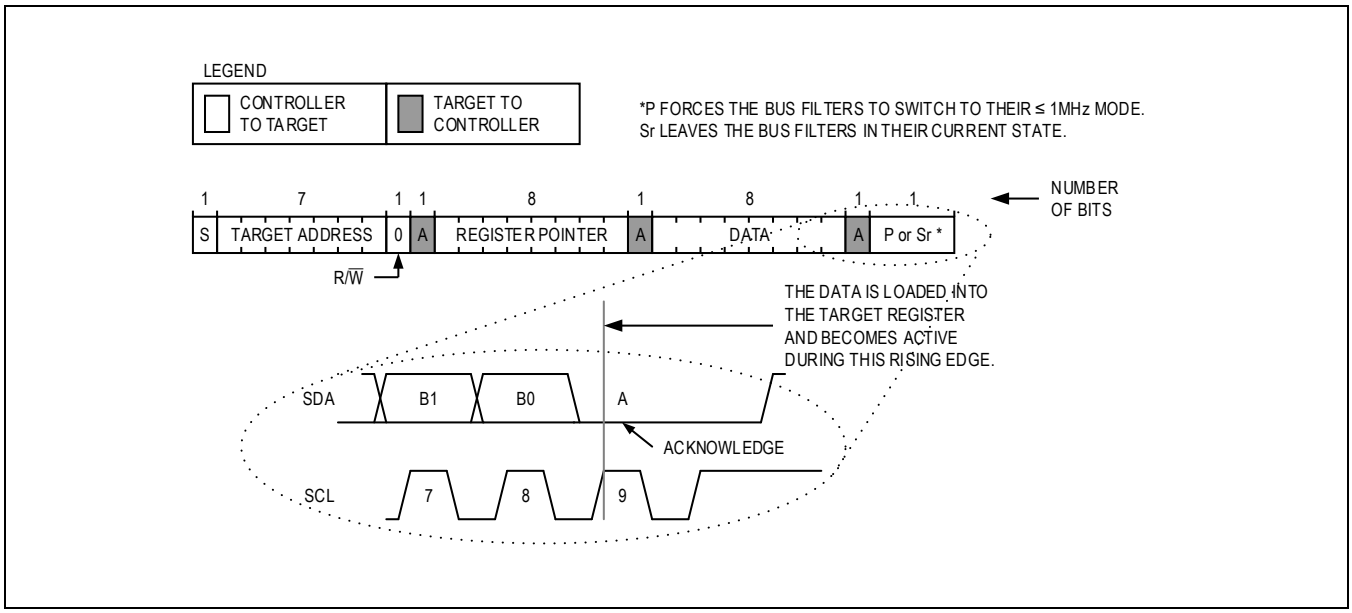


Figure 12. Writing to a Single Register

Writing to Sequential Registers

Figure 13 shows the protocol for writing to sequential registers. This protocol is similar to the “Write Byte” protocol, except that the controller device continues to write after the target device receives the first byte of data. When the controller is done writing data, it issues a STOP condition (P) or REPEATED START condition (Sr).

The “Writing to Sequential Registers” protocol is as follows:

1. The controller sends a START condition (S).
2. The controller sends the 7-bit target address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The controller sends an 8-bit register pointer.
5. The target acknowledges the register pointer.
6. The controller sends a data byte.
7. The target acknowledges the data byte. At the rising edge of the SCL, the data byte is loaded into its target register, and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the controller requires.
9. During the last acknowledge-related clock pulse, the target issues an ACKNOWLEDGE (A).
10. The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for operation at 1MHz or slower. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

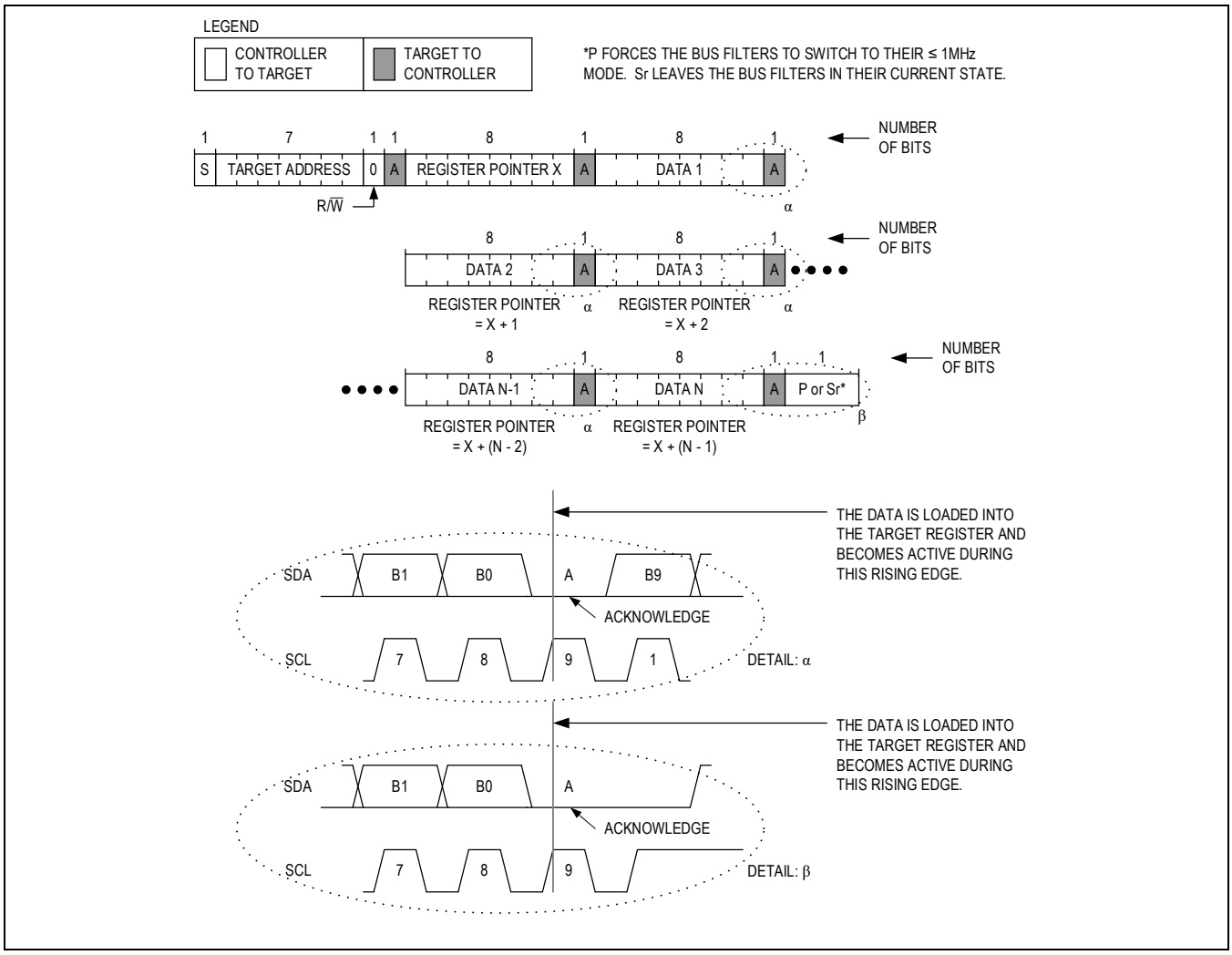


Figure 13. Writing to Sequential Registers

Reading from a Single Register

Figure 14 shows the protocol for reading from a single register. This protocol is identical to the “Read Byte” protocol specified in the SMBus standard.

The “Read Byte” protocol is as follows:

1. The controller sends a START condition (S).
2. The controller sends the 7-bit target address followed by a write bit ($R/\overline{W}$ = 0).
3. The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The controller sends an 8-bit register pointer.
5. The target acknowledges the register pointer.
6. The controller sends a REPEATED START command (Sr).
7. The controller sends the 7-bit target address followed by a read bit ($R/\overline{W}$ = 1).
8. The addressed target asserts an ACKNOWLEDGE (A) by pulling SDA LOW
9. The addressed target places 8 bits of data from the location specified by the register pointer on the bus.
10. The controller issues a NOT-ACKNOWLEDGE (nA).
11. The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for operation at 1MHz or slower. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

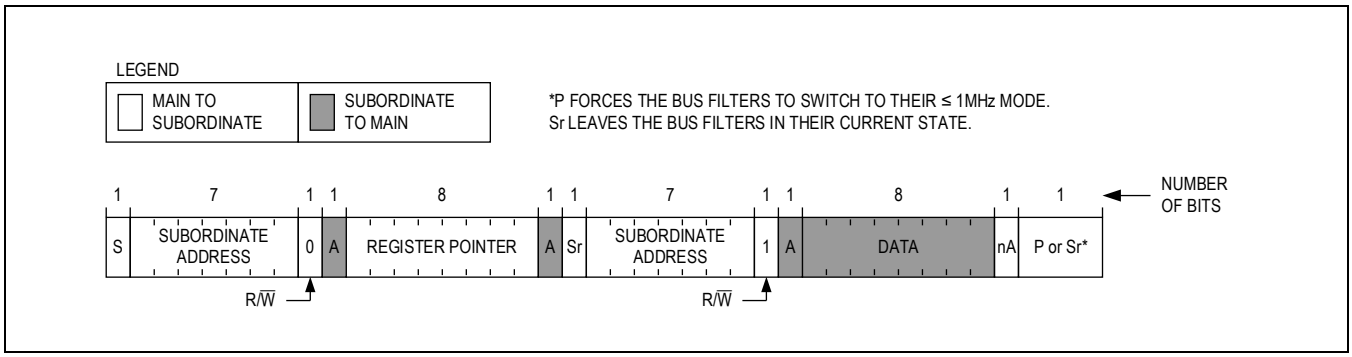


Figure 14. Reading from a Single Register

Reading from Sequential Registers

Figure 15 shows the protocol for reading from sequential registers. This protocol is similar to the “Read Byte” protocol, except the controller device issues an ACKNOWLEDGE (A) to signal the target device that it wants more data. When the controller device has all the data it requires, it issues a NOT-ACKNOWLEDGE (nA) and a STOP condition (P) to end the transmission.

The “Continuous Read from Sequential Registers” protocol is as follows:

1. The controller sends a START condition (S).
2. The controller sends the 7-bit target address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The controller sends an 8-bit register pointer.
5. The target acknowledges the register pointer.
6. The controller sends a REPEATED START command (Sr).
7. The controller sends the 7-bit target address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
9. The addressed target places 8 bits of data from the location specified by the register pointer on the bus.
10. The controller issues an ACKNOWLEDGE (A) signalling the target that it wishes to receive more data.
11. Steps 9 and 10 are repeated as many times as the controller requires. Following the last byte of data, the controller must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12. The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for operation at 1MHz or slower. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

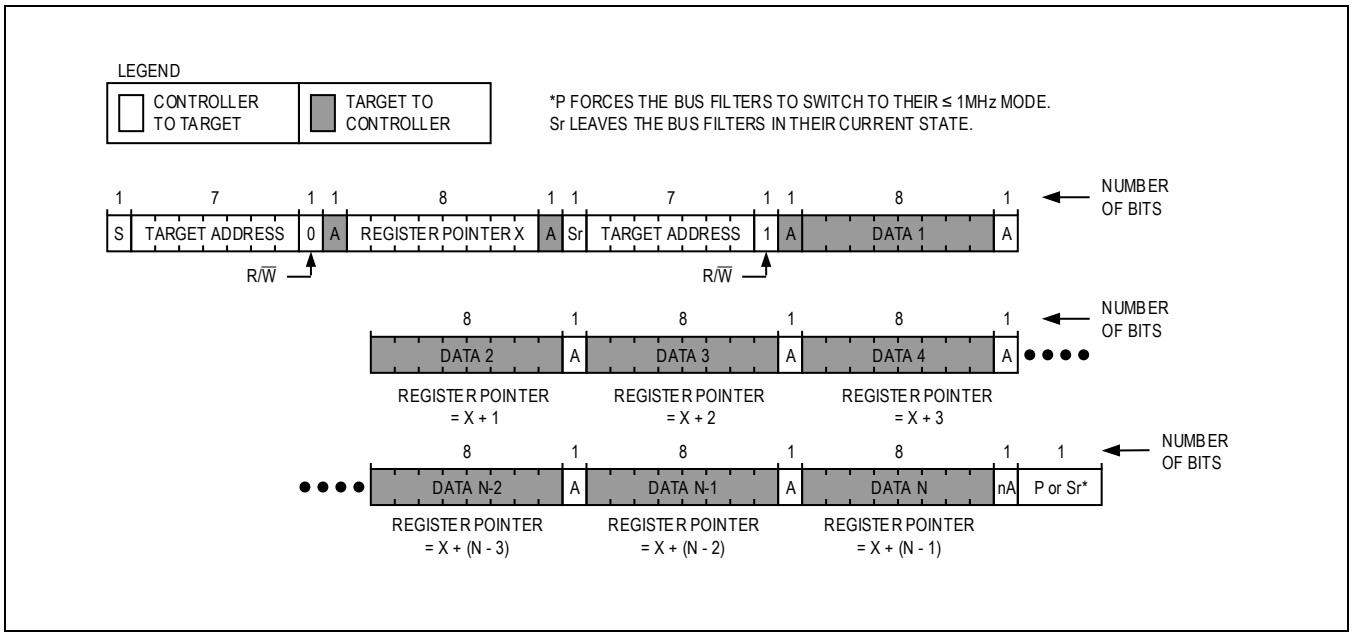


Figure 15. Reading from Sequential Registers

Engage in High-Speed Mode

Figure 16 illustrates the protocol for engaging in high-speed mode operation, which enables the bus to operate at speeds of up to 3.4MHz.

The protocol to engage in high-speed mode is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The controller sends a START condition (S).
3. The controller sends the 8-bit controller code 0000 1xx0, where ‘xx’ are don’t care bits.
4. The addressed target issues a NOT-ACKNOWLEDGE (nA).
5. The controller can now increase its bus speed up to 3.4MHz and issue any read/write operation.

The controller can continue to issue high-speed read/write operations until a STOP condition (P) is issued. Issuing a STOP condition (P) ensures that the bus input filters are set for operation at 1MHz or slower.

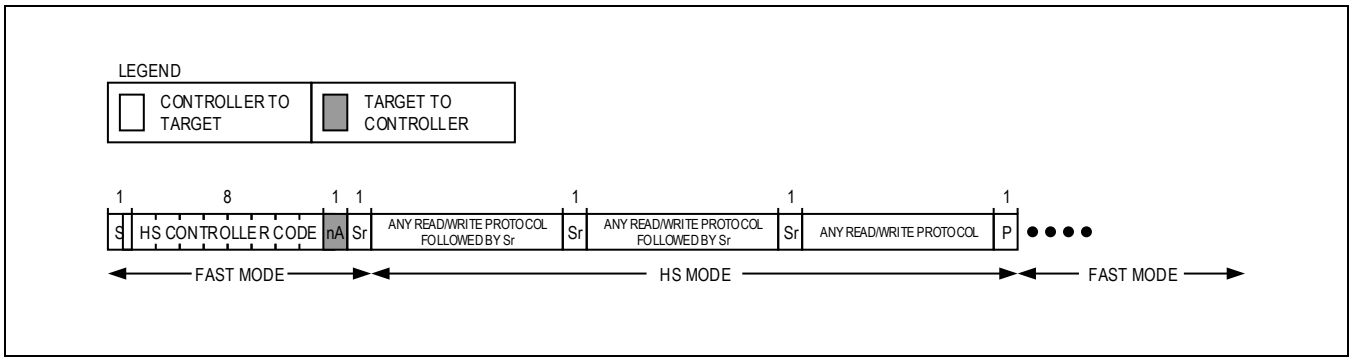


Figure 16. Engage in High-Speed Mode Protocol

High-Speed Mode Extension

The MAX77845 supports the high-speed mode extension feature. This feature keeps the IC in high-speed mode operation even after receiving a STOP condition (P). This eliminates the need for the controller device to reissue the command for engaging high-speed mode when the controller device wants to remain in high-speed mode for multiple read/write cycles.

Figure 17 shows the I2C mode transition state diagram. Write 1 to the HS_EXT bitfield to enable the high-speed mode extension when the MAX77845 is in low-speed mode. Enabling the high-speed mode extension when the MAX77845 is in high-speed mode is not supported.

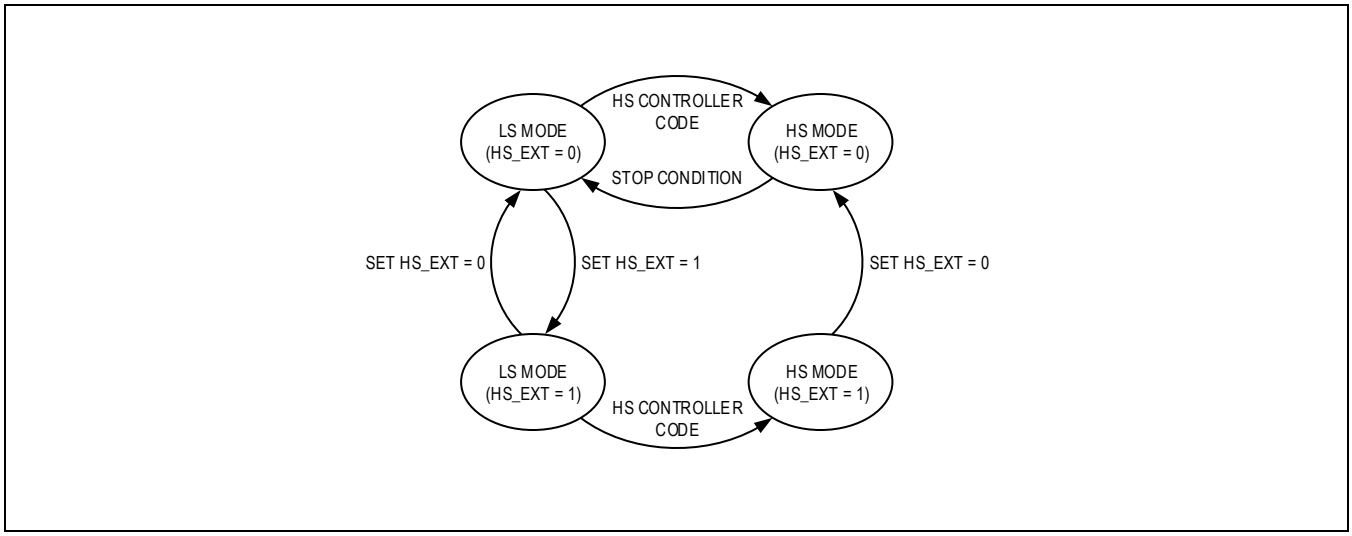


Figure 17. I2C Operating Mode State Diagram

Applications Information

Considerations for Low Output Voltage

The minimum on-time for the MAX77845 is 110ns (typical), which limits the input voltage range for low output voltage conditions. Use the equation below to calculate the maximum input voltage for a given minimum output voltage. With a bounded input voltage range, output voltages lower than 3V can be achieved. However, do not operate the device with output voltages below 2.5V.

$$V_{IN_MAX} = V_{OUT} / (110ns \times f_{SW})$$

For example, with 2.5V output and 2.1MHz switching frequency, the maximum input voltage is 10.82V.

Software (I^2C) Control

Control the IC using software commands sent over the I^2C serial interface.

Assert V_{IO} valid and connect SDA and SCL to a serial host to enable the serial bus and complete software control of the IC. When using software, the serial host can accomplish the following:

- Access power-OK and individual fault status with SYNC, POK, OVP, TSHDN, and OCP bitfields.
- Access individual fault interrupt with SYNC_I, POK_I, OVP_I, TSHDN_I, and OCP_I bitfields.
- Configure individual fault interrupt mask with SYNC_M, POK_M, OVP_M, TSHDN_M, and OCP_M bitfields.
- Configure POKB/INTB pin as a POK pin (POKB) or a fault interrupt pin (INTB) with POKBINTB[0] bitfield.
- Configure overcurrent protection and output short-circuit protection latch off behavior with SCP_LCH and OCP_LCH bitfields.
- Configure output short-circuit trigger threshold with SCP_TH bitfield.
- Configure internal compensation option with COMP[2:0] bitfield.
- Configure switching frequency with FREQ[1:0] bitfield.
- Configure switching current limit threshold (I_{LIM}) with ILIM[1:0] bitfield.
- Configure active discharge enable with AD_EN bitfield.
- Enable buck-boost output with the BB_EN bitfield.
- Configure regulation mode (SKIP, FPWM) with the FPWM bitfield.
- Configure soft-start time with SS_TM[1:0] bitfield.
- Configure output voltage (V_{OUT}) by setting internal reference voltage (V_{REF}) with VREF_U[1:0] and VREF_L[7:0] bitfields.
- Start V_{OUT} DVS with DVS_STR bitfield.
- Configure V_{OUT} DVS slew rate with DVS_SR[1:0] bitfield.

The configuration registers reset when V_{IO} becomes invalid, when IN falls below UVLO falling threshold (V_{UVLO_F}), or when both EN and BIASEN are logic LOW. See the *Detailed Description – I^2C Serial Interface* and *Register Map* section for more information.

Non-I^2C and Standalone Operation

The MAX77845 can operate without I^2C software control. The switching frequency and switching current limit can be configured by a resistor (R_{SEL}) connecting the SEL pin to AGND. External feedback resistors can be used to configure the output voltage. See the *SEL Pin Configuration* section and the *Output Voltage Configuration* section for additional information. If the I^2C serial interface is not in use, connect the SCL and SDA pins to V_{IO} to avoid unwanted behavior.

Moreover, the IC is capable of standalone operation, in which the IC starts up whenever V_{IN} is valid, and it does not require a separate supply for the V_{IO} pin. This is useful for systems without a host controller, or the IC is the only power supply in the system. To configure the IC for standalone operation, connect a 510kΩ resistor from the IN pin to the EN pin. Tie the BIASEN to the EN pin. The IC clamps the voltage at the EN and BIASEN pins internally to make sure it does not exceed the absolute maximum rating. If the system does not have a separate supply to power the V_{IO} pin, connect the V_{IO} pin to the V_L pin so that the internal regulator can supply the V_{IO} voltage. Connections for standalone operation are shown in *Figure 18*.

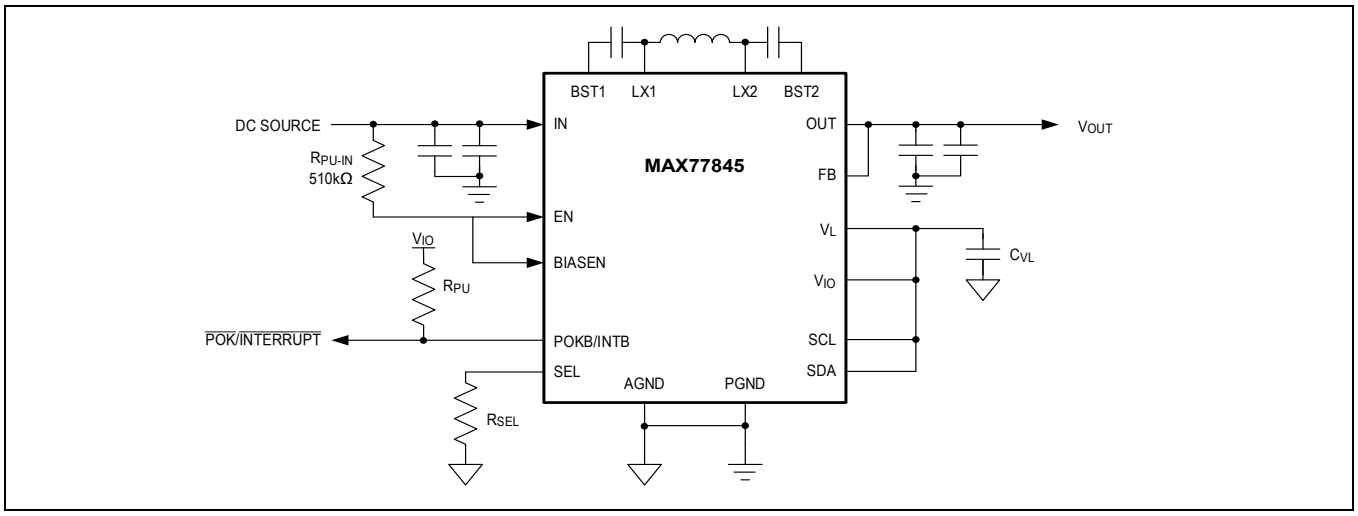


Figure 18. Connections for Standalone Operation

Inductor Selection

An inductor with a saturation current rating (I_{SAT}) greater than or equal to the typical high-side switching current limit threshold (I_{LIM}) setting is recommended. In general, inductors with lower saturation current and higher DCR ratings are physically small. Higher values of DCR reduce converter efficiency. Choose the RMS current rating (I_{RMS}) of the inductor (the current at which the temperature rises appreciably) based on the expected load current.

The chosen inductor value should ensure that the peak inductor ripple current (I_{PEAK}) is below the I_{LIM} setting, allowing the converter to maintain regulation. A 1.5 µH inductor is recommended throughout the converter's operating range. See *Table 13* for recommended inductors.

Table 13. Inductor Recommendations

VENDOR	PART NUMBER	NOMINAL INDUCTANCE (µH)	TYPICAL DCR (mΩ)	I_{SAT} (A)	I_{RMS} (A)	DIMENSIONS L x W x H (mm)	I_{LIM} SETUP
Coilcraft	XGL4020-152MEC	1.5	13	7.5	11.1	4.0 x 4.0 x 2.1	ILIM[1:0] = 00 (5.0A)
Murata	DFE322520F-1R5M#	1.5	29 (max)	5.2	4	3.2 x 2.5 x 2.0	ILIM[1:0] = 00 (5.0A)
Samsung	CIGW252012TM1R5ML#	1.5	40 (max)	3.4	4.2	2.5 x 2.0 x 1.2	ILIM[1:0] = 01 (3.4A)
Cyntec	HTEH25201T-1R5MSR	1.5	35	4	4	2.5 x 2.0 x 1.0	ILIM[1:0] = 01 (3.4A)
Murata	DFE201612E-1R5M#	1.5	72 (max)	3.2	2.3	2.0 x 1.6 x 1.2	ILIM[1:0] = 10 (1.8A)
Samsung	CIGW201610GL1R5ML#	1.5	75 (max)	2.1	2.4	2.0 x 1.6 x 1.0	ILIM[1:0] = 10 (1.8A)

Input Capacitor Selection

For most applications, bypass the IN pin with two 25V, 10µF nominal ceramic input capacitors (C_{IN}) that maintain an effective capacitance of 1µF or higher at their working voltage. Effective C_{IN} is the actual capacitance value seen from the converter input during operation. Larger values improve decoupling for the converter, but increase inrush current from the voltage supply when connected. C_{IN} reduces the current peaks drawn from the input power source and reduces switching noise in the system. The ESR/ESL of the C_{IN} and its series PCB trace should be very low (< 15mΩ and < 2nH) at frequencies up to the converter's switching frequency.

Pay special attention to the capacitor's voltage rating, initial tolerance, temperature variation, and DC bias characteristic when selecting C_{IN}. Ceramic capacitors with X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, smaller case-size capacitors derate more heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

Output Capacitor Selection

Sufficient output capacitance (C_{OUT}) is required for stable operation of the converter. Choose effective C_{OUT} to be 8.2µF minimum. Effective C_{OUT} is the actual capacitance value seen by the converter output during operation. Larger values (above the required effective minimum) improve load transient performance but increase input surge currents during soft-start and output voltage changes. The output filter capacitor must have low enough ESR for frequencies up to the converter's switching frequency to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. For most applications, two 25V 22µF capacitors are recommended for C_{OUT}.

Pay special attention to capacitor's voltage rating, initial tolerance, variation with temperature, and DC bias characteristic when selecting C_{OUT}. Ceramic capacitors with X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, smaller case-size capacitors derate more heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

Other Required Component Selection

Table 14 illustrates the requirements for other required components.

Table 14. Other Component Selection Requirements

SYMBOL	COMPONENT DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
C_{BST}	High-Side FET Driver Bootstrap Capacitor	Suggested Capacitance		0.22		µF
C_{VL}	V_L Regulator Bypass Capacitor	Effective Capacitance	0.5		3	µF
		Equivalent Series Resistance (ESR)			100	mΩ
C_{VIO}	V_{IO} Regulator Bypass Capacitor	Effective Capacitance	0.3		1.5	µF
		Equivalent Series Resistance (ESR)			100	mΩ
R_{SEL}	SEL Pin Resistor	Acceptable Tolerance	-1		+1	%
R_{PU}	POKB/INTB Pullup Resistor	Suggested Resistance		15		kΩ

PCB Layout Guidelines

Careful circuit board layout is crucial for achieving low switching power losses and ensuring clean, stable operation. A high-density interconnect (HDI) PCB is required to route to the EN, FPWM/SYNC, and POKB/INTB pins. *Figure 19* shows an example layout for the MAX77845 WLP package.

When designing the PCB, follow these guidelines:

- Place the input capacitors (C_{IN}) and output capacitors (C_{OUT}) immediately next to the IN pin and OUT pin of the IC, respectively. Since the IC operates at a high switching frequency, this placement is critical for minimizing parasitic inductance within the input and output current loops, which can cause high voltage spikes and damage the internal switching MOSFETs.
- Place the inductor next to the LX bumps (as close as possible) and make the traces between the LX bumps and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer (see *Figure 19*), ensure to include sufficient vias to minimize trace impedance. Routing LX traces across multiple layers is recommended to reduce trace impedance further. Furthermore, do not allow LX traces to occupy an excessive amount of space. The voltage on this node switches very quickly, and additional area creates more radiated emissions.
- Route LX nodes to their corresponding bootstrap capacitor (C_{BST}) as short as possible. Prioritize CBST placement to minimize the trace length to the IC.
- Connect the inner PGND bumps to the low-impedance ground plane on the PCB with vias placed next to the bumps. Do not create PGND islands, as PGND islands risk interrupting the hot loops. Connect AGND and AGND island to the low-impedance ground plane on the PCB (the same net as PGND).
- Keep the power traces and load connections short and wide. This is essential for high converter efficiency.
- Do not neglect the ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the *Output Capacitor Selection* section and refer to the *Tutorial 5527* for more information.

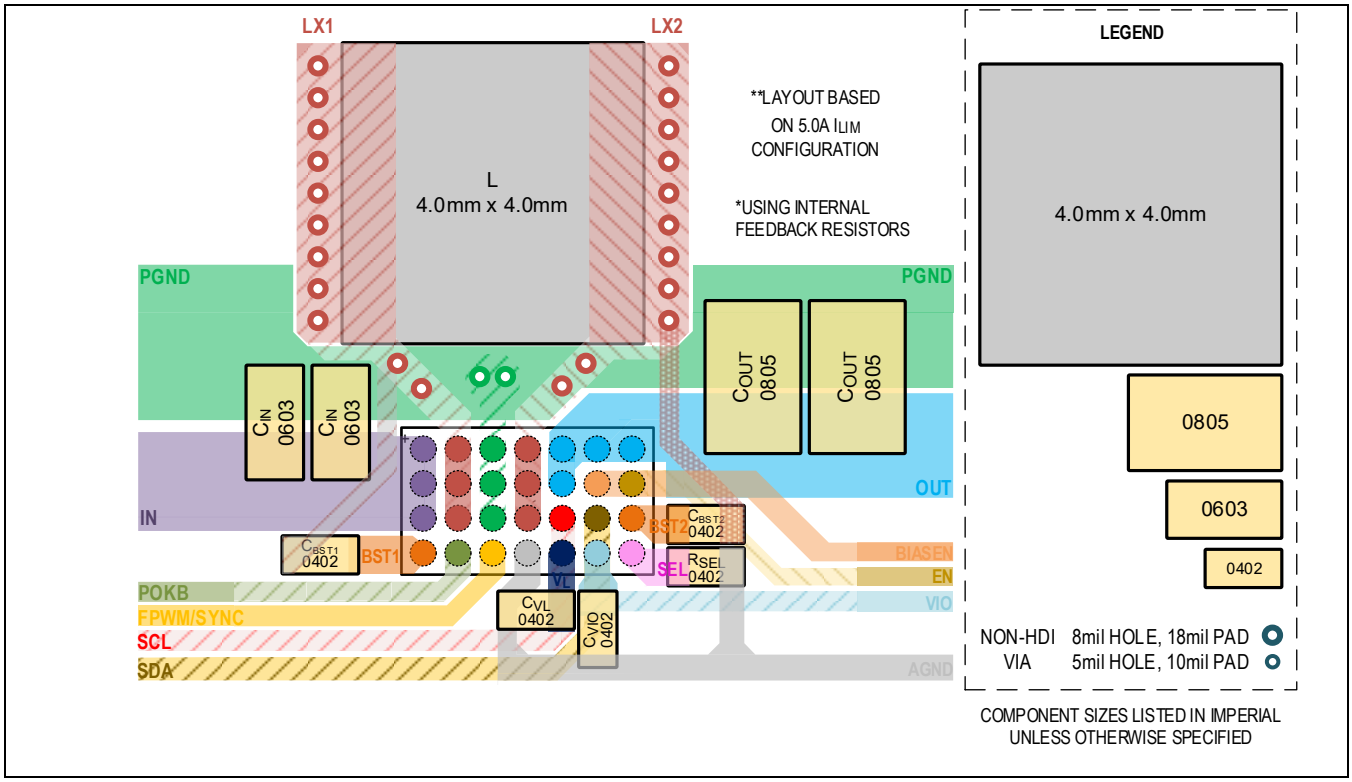


Figure 19. PCB Layout Recommendation for 28 WLP Package

Register Map

User Registers

Registers reset when shut down.

ADDRESS	NAME	MSB							LSB
User Registers									
0x10	STAT[7:0]	RSVD[1:0]		SYNC	POK	OVP	SCP	TSHDN	OCP
0x11	INT[7:0]	RSVD[1:0]		SYNC_I	POK_I	OVP_I	SCP_I	TSHDN_I	OCP_I
0x12	MASK[7:0]	RSVD[1:0]		SYNC_M	POK_M	OVP_M	SCP_M	TSHDN_M	OCP_M
0x13	LCH_CFG[7:0]	RSVD[4:0]					SCP_LCH	RSVD	OCP_LCH
0x14	BB_CFG1[7:0]	COMP[2:0]			FREQ[1:0]		SCP_TH	ILIM[1:0]	
0x15	BB_CFG2[7:0]	AD_EN	BB_EN	FPWM	POKBINTB	SS_TM[1:0]		DVS_SR[1:0]	
0x16	VREF_CFG1[7:0]	RSVD[4:0]					DVS_STR	VREF_U[1:0]	
0x17	VREF_CFG2[7:0]	VREF_L[7:0]							
0x18	I2C_CFG[7:0]	RSVD[6:0]							HS_EXT

Register Details

STAT (0x10)

POK and Fault Status Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		SYNC	POK	OVP	SCP	TSHDN	OCP
Reset	0b00		0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only		Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	Reserved. Reads back 0.	N/A
SYNC	5	External Clock Synchronization Status	0: Buck-boost is NOT synchronized to external clock. 1: Buck-boost is synchronized to external clock. This status bit indicate instantaneous value.
POK	4	Power-OK Status	0: Output voltage is below POK threshold. 1: Output voltage is above POK threshold.

BITFIELD	BITS	DESCRIPTION	DECODE
			This status bit indicate instantaneous value.
OVP	3	Overvoltage Protection Status	0: Output voltage is below OVP threshold. 1: Output voltage is above OVP threshold. This status bit indicate instantaneous value.
SCP	2	Ouput Short-Circuit Protection Status	0: Output voltage is above SCP threshold. 1: Output voltage is below SCP threshold. This status bit indicate instantaneous value.
TSHDN	1	Thermal Shutdown Status	0: Die temperature is below T_{SHDN} threshold. 1: Die temperature is above T_{SHDN} threshold. This status bit indicate instantaneous value.
OCP	0	Overcurrent Protection Status	0: Switching current is below set limit. 1: Switching current is above set limit. This status bit indicate instantaneous value.

INT (0x11)

POK and Fault Interrupt Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		SYNC_I	POK_I	OVP_I	SCP_I	TSHDN_I	OCP_I
Reset	0b00		0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All		Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	Reserved. Reads back 0.	N/A
SYNC_I	5	External Clock Synchronization Fault Interrupt	0: SYNC fault has NOT been detected. 1: SYNC fault has been detected. This bit latches once triggered. Interrupt clears after read.
POK_I	4	Power-OK Fault Interrupt	0: POK fault has NOT been detected. 1: POK fault has been detected. This bit latches once triggered. Interrupt clears after read.
OVP_I	3	Overvoltage Protection Fault Interrupt	0: OVP fault has NOT been detected. 1: OVP fault has been detected. This bit latches once triggered. Interrupt clears after read.

BITFIELD	BITS	DESCRIPTION	DECODE
SCP_I	2	Ouput Short-Circuit Protection Fault Interrupt	0: SCP fault has NOT been detected. 1: SCP fault has been detected. This bit latches once triggered. Interrupt clears after read.
TSHDN_I	1	Thermal Shutdown Fault Interrupt	0: TSHDN fault has NOT been detected. 1: TSHDN fault has been detected. This bit latches once triggered. Interrupt clears after read.
OCP_I	0	Overcurrent Protection Fault Interrupt	0: OCP fault has NOT been detected. 1: OCP fault has been detected. This bit latches once triggered. Interrupt clears after read.

MASK (0x12)

POK and Fault Interrupt Mask Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		SYNC_M	POK_M	OVP_M	SCP_M	TSHDN_M	OCP_M
Reset	0b00		0b1	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	Reserved	N/A
SYNC_M	5	External Clock Synchronization Fault Interrupt Mask	0: External clock synchronization fault interrupt is NOT masked. 1: External clock synchronization fault interrupt is masked (Default).
POK_M	4	Power-OK Fault Interrupt Mask	0: Power-OK fault interrupt is NOT masked (Default). 1: Power-OK fault interrupt is masked.
OVP_M	3	Overvoltage Protection Fault Interrupt Mask	0: Overvoltage protection fault interrupt is NOT masked (Default). 1: Overvoltage protection fault interrupt is masked.
SCP_M	2	Ouput Short-Circuit Protection Fault Interrupt Mask	0: Output short circuit protection fault interrupt is NOT masked (Default). 1: Output short circuit protection fault interrupt is masked.
TSHDN_M	1	Thermal Shutdown Fault Interrupt Mask	0: Thermal shutdown fault interrupt is NOT masked (Default). 1: Thermal shutdown fault interrupt is masked.
OCP_M	0	Overcurrent Protection Fault Interrupt Mask	0: Overcurrent protection fault interrupt is NOT masked (Default). 1: Overcurrent protection fault interrupt is masked.

LCH_CFG (0x13)

Fault Latch-Off Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD[4:0]					SCP_LCH	RSVD	OCP_LCH
Reset	0b00000					0b1	0b0	OTP
Access Type	Write, Read					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:3	Reserved	N/A
SCP_LCH	2	Ouput Short-Circuit Protection Latch-Off Control	0: Output short circuit protection latch-off is disabled. 1: Output short circuit protection latch-off is enabled (Default).
RSVD	1	Reserved	N/A
OCP_LCH	0	Overcurrent Protection Latch-Off Control	0: Overcurrent protection latch-off is disabled. 1: Overcurrent protection latch-off is enabled.

BB_CFG1 (0x14)

Buck-Boost Configuration Register 1

BIT	7	6	5	4	3	2	1	0
Field	COMP[2:0]			FREQ[1:0]		SCP_TH	ILIM[1:0]	
Reset	0b010			0b11		0b1	0b00	
Access Type	Write, Read			Write, Read		Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
COMP	7:5	Internal Compensation R_C Option (Bandwidth)	000: R_C = 30kΩ, Buck mode R_C = 20kΩ, Boost mode 001: R_C = 45kΩ, Buck mode R_C = 30kΩ, Boost mode 010: R_C = 60kΩ, Buck mode R_C = 45kΩ, Boost mode (Default) 011: R_C = 70kΩ, Buck mode R_C = 50kΩ, Boost mode 100: R_C = 80kΩ, Buck mode R_C = 55kΩ, Boost mode 101: R_C = 90kΩ, Buck mode R_C = 60kΩ, Boost mode 110: R_C = 110kΩ, Buck mode R_C = 75kΩ, Boost mode 111: R_C = 150kΩ, Buck mode R_C = 100kΩ, Boost mode
FREQ	4:3	Switching Frequency	00: 1.2MHz 01: 1.5MHz 10: 1.8MHz 11: 2.1MHz
SCP_TH	2	Ouput Short Circuit Protection Detection Threshold	0: 30% of output voltage target 1: 60% of output voltage target (Default)
ILIM	1:0	High-Side Switching Current Limit	00: 5.0A 01: 3.4A

BITFIELD	BITS	DESCRIPTION	DECODE
			10: 1.8A 11: 1.0A

BB_CFG2 (0x15)

Buck-Boost Configuration Register 2

BIT	7	6	5	4	3	2	1	0
Field	AD_EN	BB_EN	FPWM	POKBINTB	SS_TM[1:0]		DVS_SR[1:0]	
Reset	OTP	0b0	0b0	0b0	OTP		0b00	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
AD_EN	7	Active Discharge Enable	0: Active discharge is disabled during shutdown. 1: Active discharge is enabled during shutdown (Default).
BB_EN	6	Buck-Boost Output Software Enable	0: Buck-boost output is disabled (Default). 1: Buck-boost output is enabled. 'OR' logic with EN pin input.
FPWM	5	Forced-PWM Mode	0: Forced-PWM mode is disabled (Default). 1: Forced-PWM mode is enabled. 'OR' logic with FPWM/SYNC pin input.
POKBINTB	4	POKB/INTB Pin Configuration	0: POKB/INTB pin configured as POKB pin (reflection of POK bit in STAT register) (Default). 1: POKB/INTB pin is configured as INTB pin (reflection of INT register).
SS_TM	3:2	Soft-Start Time	00: 1ms 01: 2ms 10: 4ms 11: 8ms
DVS_SR	1:0	Internal Reference DVS Slew Rate. See the *Output Voltage Configuration* section for equations to convert V_{REF} DVS slew rate to V_{OUT} DVS slew rate.	00: 4/3mV/µs (Default) 01: 2/3mV/µs 10: 1/3mV/µs 11: 1/6mV/µs

VREF_CFG1 (0x16)

Internal Reference Configuration Register 1

BIT	7	6	5	4	3	2	1	0
Field	RSVD[4:0]					DVS_STR	VREF_U[1:0]	
Reset	0b00000					0b0	0b00	
Access Type	Write, Read					Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:3	Reserved	N/A
DVS_STR	2	DVS Start	Initiates DVS to apply new VREF. This bit self-clears after DVS is done, or if there is no change to VREF[9:0].
VREF_U	1:0	Internal Reference Voltage Upper Bits	See VREF_L[7:0] for decode values

VREF_CFG2 (0x17)

Internal Reference Configuration Register 2

BIT	7	6	5	4	3	2	1	0
Field	VREF_L[7:0]							
Reset	0xFA							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VREF_L	7:0	Internal Reference Voltage Lower Bits	VREF[9:0] bitfield is a combination of VREF_U[1:0] and VREF_L[7:0], in which VREF_U[1:0] represents the upper 2 bits and VREF_L[7:0] represents the lower 8 bits. After updating VREF[9:0], write 0b1 to DVS_STR (or within the same I²C transaction writing VREF_U[1:0]) to apply the new value. The decode of VREF[9:0] bitfield is as follows: 0x000–0x095: 0.18311V 0x096–0x2ED: 1.22mV/LSB in a linear transfer function between 0.18311V (0x096) and 0.91431V (0x2ED) 0x2EC–0x3FF: 0.91431V Default: 0x0FA: 0.30518V

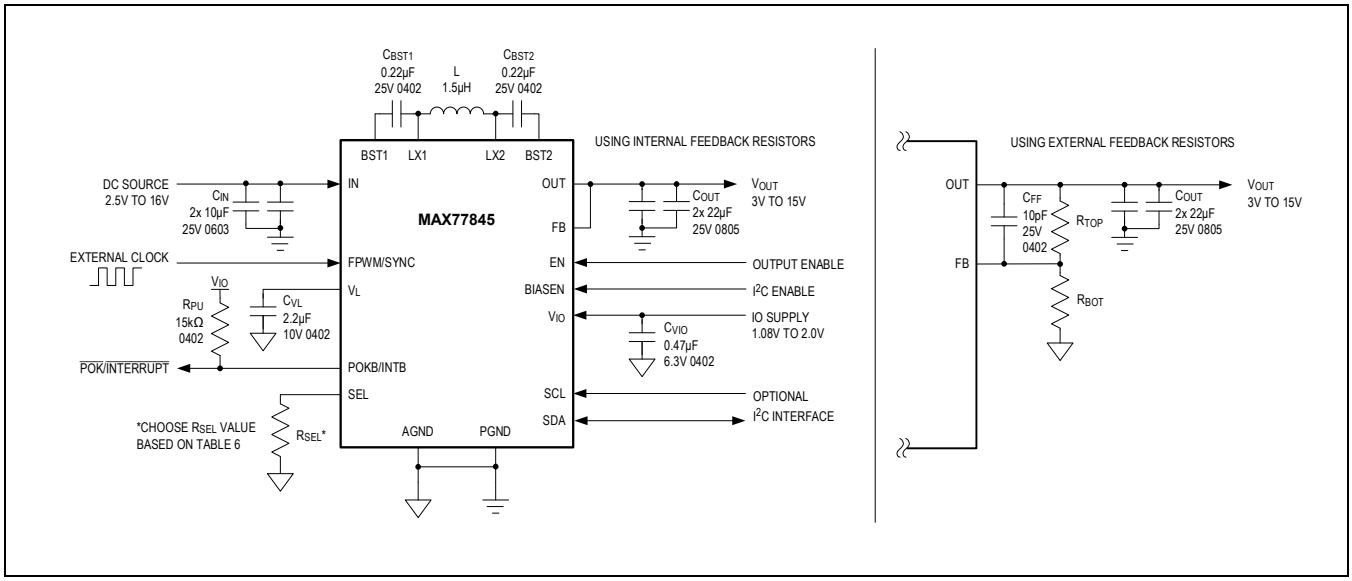
I2C_CFG (0x18)

I²C Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD[6:0]							HS_EXT
Reset	0b0000000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:1	Reserved	N/A
HS_EXT	0	I²C High-Speed Mode Extension Control	0: I²C high-speed mode extension is disabled (Default). 1: I²C high-speed mode extension is enabled.

Typical Application Circuits



Ordering Information

PART NUMBER	DEFAULT OUTPUT VOLTAGE (V)	DEFAULT SOFT-START TIME (ms)	DEFAULT OCP LATCH-OFF	DEFAULT SCP LATCH-OFF	PIN-PACKAGE
MAX77845BEWI+T	5	2	Disabled	Enabled	28 WLP
MAX77845CEWI+T			Enabled		28 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

For other default options, contact sales representatives for availability.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/25	Release for Market Intro	—

Notes

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