MAX77726/MAX77727

22V, 3A Synchronous Buck Converter with Ultrasonic Mode

General Description

The MAX77726/MAX77727 provide power supply solutions for nano-power applications where size and efficiency are critical. They feature 4.6A inductor peak current protection and can deliver up to 3A output current. See the *Simplified Application Diagram*.

The MAX77726's output voltages can be logically set through the VSEL pins for four specific output voltages. Physical enable pin and mode pin settings provide intuitive control.

The MAX77727's output voltages are programmable through I²C. It also allows MODE and enables selection through the I²C interface and status reading.

Applications

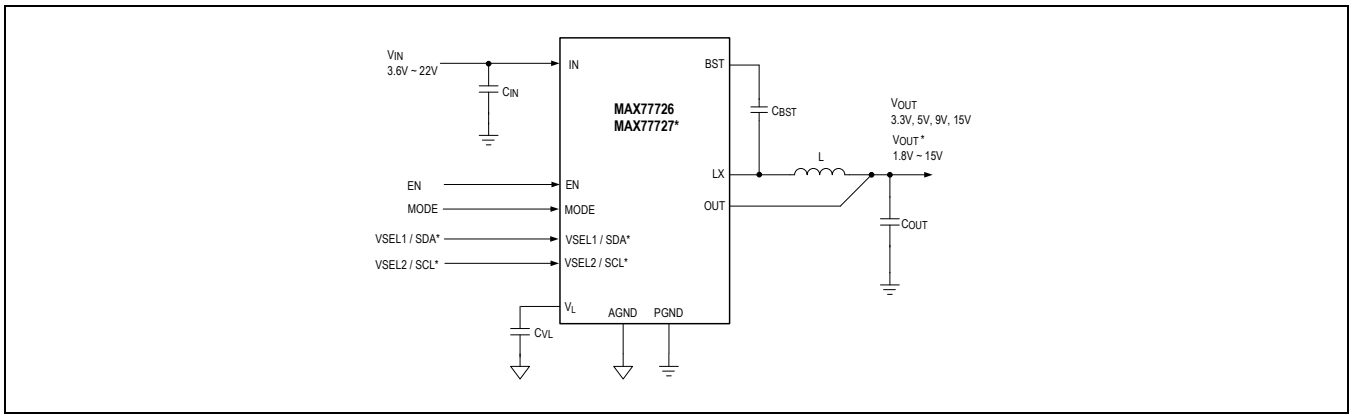
- USB Sourced Devices
- Portable Electronics
- 12V Distributed Power Bus Applications

Benefits and Features

- 3.6V to 22V Input Voltage Range
- 1.8V to 15V Output Voltage Range
- Low Current Consumption and High Efficiency
  - 100nA Shutdown Current
  - 800nA Quiescent Current in Low Power Mode
  - 96% Peak Efficiency
- Integrated 50mΩ and 45mΩ Power MOSFETs
- Up to 4.6A Inductor Peak Current Limit
- MAX77726 Provides 3.3V, 5V, 9V, and 15V Regulation Target Voltage Selection using Two VSEL Pins
- MAX77727 Provides Output Voltage Programmable from 1.8V to 15V Through I²C (with 100mV Resolution in the Range from 1.8V to 4.9V, and 250mV Resolution in the Range from 5V to 15V
- MAX77726 Provides Pin Selectable Ultrasonic Mode
- MAX77727 Provides I²C Selectable for Forced PWM Mode
- Output Active Discharge Feature
- Ease of Use and Small Solution Size
  - Cycle-by-Cycle Inductor Peak Current Limit, UVLO, Output Short Circuit, Over-Temperature Protection Features
  - 12-Pin, 0.4mm Pitch, 0.65mm Height Wafer-Level Package (WLP)
  - Use of Chip Type Inductors and Ceramic Capacitors
- 1.32mm x 1.77mm, 12-WLP, 0.4mm Pitch Package

Ordering Information **appears at end of data sheet.**

Simplified Application Diagram



19-102096; Rev 0; 12/25

Absolute Maximum Ratings

IN, LX to PGND ..... -0.3V to 26.0V

BST to LX (*Note1*) ..... -0.3V to 2.0V

PGND to AGND ..... -0.3V to 0.3V

V_L to AGND ..... -0.3V to 2.0V

OUT to AGND ..... -0.3V to 16.0V

EN to AGND ..... -0.3V to 26.0V

MODE, VSEL1, VSEL2, SDA, SCL to AGND ..... -0.3V to 6.0V

Continuous Power Dissipation at T_A = 70°C (Derate 13.73mW/°C above +70°C) 1098mW

Junction Temperature Range ..... -40°C to 125°C

Maximum Junction Temperature ..... 150°C

Storage Temperature Range ..... -65°C to 150°C

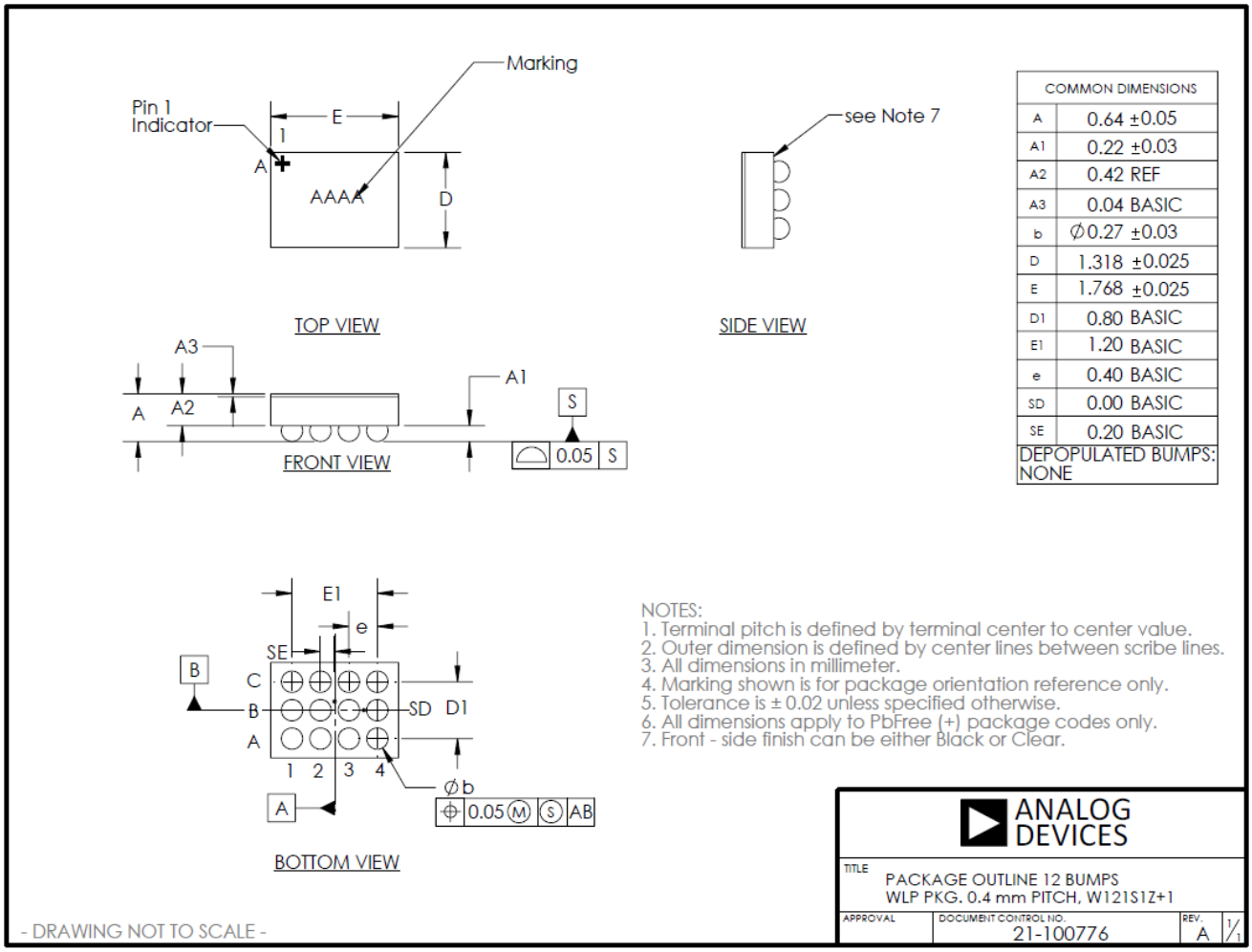
Soldering Temperature (Reflow) ..... 260°C

Note 1: The LX pin has internal clamps to GND and IN. These diodes may be forward-biased during switching transitions.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	W121S1Z+1
Outline Number	21-100776
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	72.82°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A



For the latest package outline information and land patterns (footprints), go to *www.analog.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.analog.com/thermal-tutorial*.

Electrical Characteristics

(T_A = ≈ T_J, V_{IN} = 9V, V_{OUT} = 3.3V, Typical values are at T_A ≈ T_J = +25°C. Limits are 100% production tested at T_J = +25°C. The MAX77726/MAX77727 is tested under pulsed load conditions such that T_A ≈ T_J. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization using statistical process control methods (Note 2).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY							
Operating Input Voltage Range	V_{IN}			3.6		22.0	V
Undervoltage Lockout (UVLO)	V_{UVLO_R}	V_{IN} rising		3.40	3.50	3.60	V
	V_{UVLO_F}	V_{IN} falling		3.20	3.30	3.40	
Shutdown Current	I_{SD}	EN = low, V_{IN} < 22V, T_J = +25°C			0.125	0.2	µA
Quiescent Current (LPM)	I_{Q_LPM}	EN = high, LPM, not switching, T_J = +25°C			0.8	2.0	µA
Quiescent Current (USM)	$I_{Q\_USM\_77726}$	EN = high, USM, switching, T_J = +25°C	MAX77726 only *Note 4*		5500		µA
	$I_{Q\_USM\_77727}$	EN = high, USM, switching, T_J = +25°C	MAX77727 only *Note 4*		2500		
OUTPUT VOLTAGE ACCURACY							
Output Voltage Range	V_{OUT}	Guaranteed by output voltage accuracy		1.8		15.0	V
Output Voltage Shift	V_{OUT_SHIFT}	V_{OUT} = 5 to 15V	MAX77726 only		+1		%
Output Voltage Accuracy	V_{OUT_ACC}	During CCM operation	*Note 3*	-2.0		+2.0	%
Low-Power Mode Regulation	$V_{OUT\_ACC\_LPM}$	Percentage of output voltage target level	In low power mode	+1.0	+2.75	+4.0	%
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = V_{OUT_TARGET} + 300mV to 22V, CCM operation	*Note 4*		±0.1		%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	During CCM operation	*Note 4*		0.35		%/A
POWER STAGE							
High-Side MOSFET Peak Current Limit	I_{LIM}	*Note 5*		4.2	4.6	5.2	A
High-Side MOSFET On Resistance	R_{DSON_HS}	I_{LX} = -300mA			50	90	mΩ
Low-Side MOSFET On Resistance	R_{DSON_LS}	I_{LX} = 300mA			45	80	mΩ
SWITCHING CHARACTERISTICS							
Switching Frequency	f_{SW}	V_{IN} = 9V, V_{OUT} = 3.3V, L = 2.2µH, during CCM operation	*Note 4*		1.2		MHz
Minimum Switching Frequency	f_{SW_MIN}	Pulses initiated by ultrasonic timer; C_{OUT} = 100µF		27	33		kHz
Maximum Duty Cycle Operation	DC_{MAX}	*Note 4*			100		%
ACTIVE DISCHARGE							

(T_A = ≈ T_J, V_{IN} = 9V, V_{OUT} = 3.3V, Typical values are at T_A ≈ T_J = +25°C. Limits are 100% production tested at T_J = +25°C. The MAX77726/MAX77727 is tested under pulsed load conditions such that T_A ≈ T_J. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization using statistical process control methods (Note 2).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Discharge Time	t_{OUT_DIS}	V_{OUT} = 5V, EN = low, C_{OUT} = 100µF, when V_{OUT} discharged to 100mV	Note 4		22		ms
		V_{OUT} = 15V, EN = low, C_{OUT} = 100µF, when V_{OUT} discharged to 100mV	Note 4		51		
TIMING							
Turn-On Delay Time	t_{DLY_EN}	From EN = high to soft-start, T_J = -40°C to +125°C	MAX77726 only		2.5		ms
Soft-Start Time	t_{SS}	V_{IN} = 9V, V_{OUT} = 3.3V, L = 2.2µH, C_{OUT} = 100µF	MAX77726 only Note 4		0.8		ms
EN, MODE, VSEL1, AND VSEL2 SIGNAL LEVELS							
Input High Level	V_{IH}	EN, MODE, VSEL1, VSEL2,		1.0			V
Input Low Level	V_{IL}	MODE, VSEL1, VSEL2				0.4	V
		EN				0.3	
			T_J = 0°C to +125°C			0.35	
Pulldown Resistance		EN, MODE, VSEL1, VSEL2			300		kΩ
THERMAL PROTECTION							
Thermal Shutdown Threshold	T_{SD}	T_J rising			150		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}				20		°C
SDA AND SCL I/O STAGE (Note 6)							
SCL, SDA Input High Voltage	V_{IH}	SCL, SDA pulled to 1.8V		1.0			V
SCL, SDA Input Low Voltage	V_{IL}	SCL, SDA pulled to 1.8V				0.4	V
SCL, SDA Input Leakage Current	$I_{SCL\_SDA\_LKG}$	SCL, SDA pulled to 1.8V, V_{SCL} = V_{SDA} = 0V and 6V		-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 3mA				0.4	V
SCL, SDA Pin Capacitance	C_{IN}	SCL, SDA pulled to 1.8V			10		pF
Fall Time from V_{IH} to V_{IL}	t_{FALL}					120	ns
I^2C Enable Time	t_{I2C_EN}	EN = high to first I^2C command			3.5		ms
I^2C-COMPATIBLE INTERFACE TIMING (STANDARD AND FAST MODE) (Note 6)							
Clock Frequency	f_{SCL}			0		400	kHz
Hold Time (REPEATED) START Condition	t_{HD_STA}			0.5			µs

(T_A = ≈ T_J, V_{IN} = 9V, V_{OUT} = 3.3V, Typical values are at T_A ≈ T_J = +25°C. Limits are 100% production tested at T_J = +25°C. The MAX77726/MAX77727 is tested under pulsed load conditions such that T_A ≈ T_J. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization using statistical process control methods (Note 2).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Low Period	t_{LOW}		1.3			µs
SCL High Period	t_{HIGH}		0.6			µs
Setup Time (REPEATED) START Condition	t_{SU_STA}		0.6			µs
Data Hold Time	t_{HD_DAT}		0			ns
Data Setup Time	t_{SU_DAT}		100			ns
Setup Time for STOP Condition	t_{SU_STO}		0.5			µs
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		50		ns

Note 2: Specific operating conditions, board layout, rated package thermal impedance, and other environmental factors determine the maximum ambient temperature consistent with this specification.

Note 3: Does not include ripple.

Note 4: Not production tested. Design guidance only.

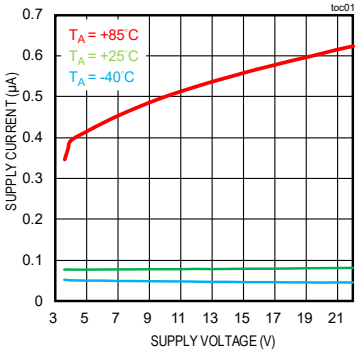
Note 5: This is a DC measurement.

Note 6: Applicable to MAX77727. Design guidance only. Not Production tested.

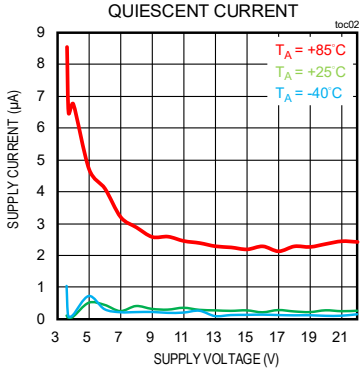
Typical Operating Characteristics

(V_{IN} = 9V, V_{OUT} = 3.3V, L = 2.2µH (HBLE041H-2R2MS), C_{OUT} = 3x22µF + 1x47µF, T_A = +25°C, unless otherwise noted.)

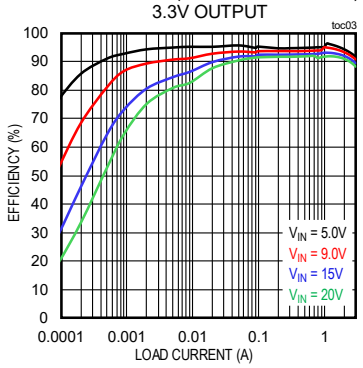
SHUTDOWN CURRENT



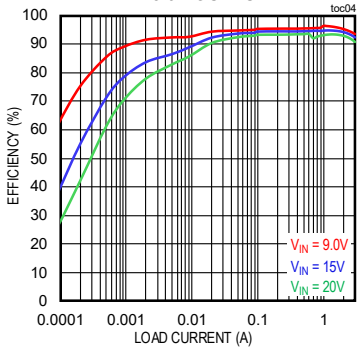
QUIESCENT CURRENT



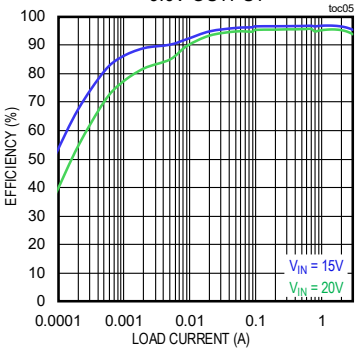
EFFICIENCY (LOW POWER MODE)
3.3V OUTPUT



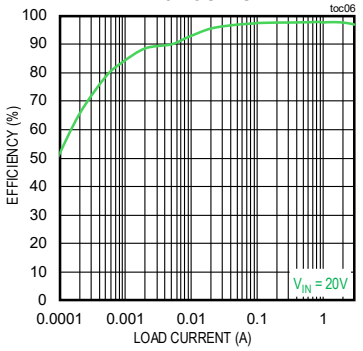
EFFICIENCY (LOW POWER MODE)
5.0V OUTPUT



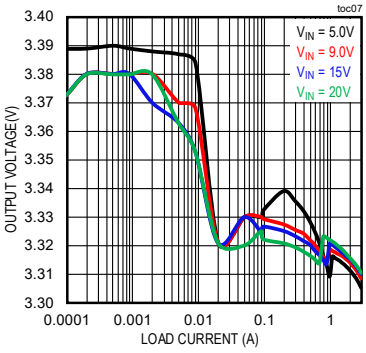
EFFICIENCY (LOW POWER MODE)
9.0V OUTPUT



EFFICIENCY (LOW POWER MODE)
15V OUTPUT



MAX77726
LOAD REGULATION
3.3V OUTPUT



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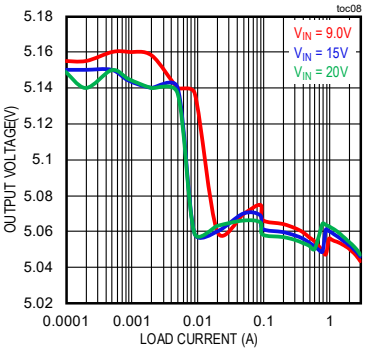
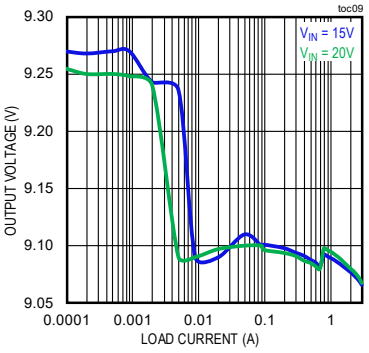
LOAD REGULATION
5.0V OUTPUT

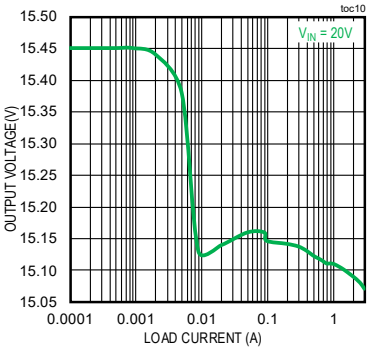


MAX77726
LOAD REGULATION
9.0V OUTPUT

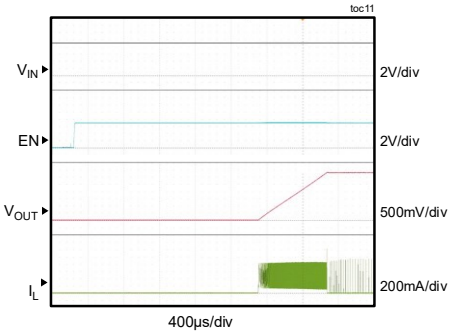


(V_{IN} = 9V, V_{OUT} = 3.3V, L = 2.2µH (HBLE041H-2R2MS), C_{OUT} = 3x22µF + 1x47µF, T_A = +25°C, unless otherwise noted.)

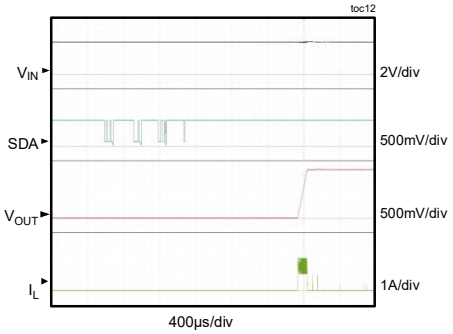
MAX77726
LOAD REGULATION
15V OUTPUT



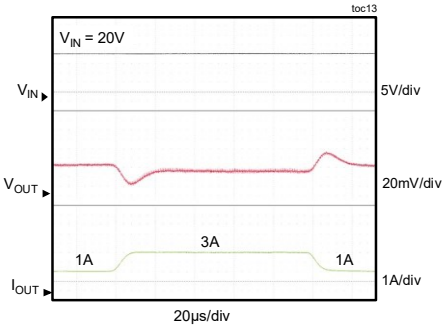
MAX77726
START UP
3.3V OUTPUT



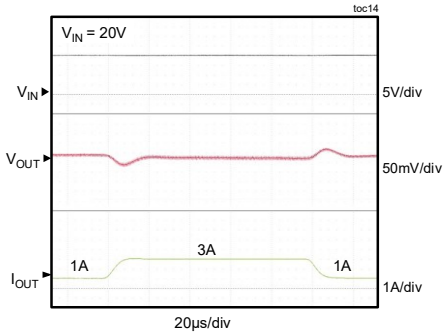
MAX77727
START UP
3.3V OUTPUT



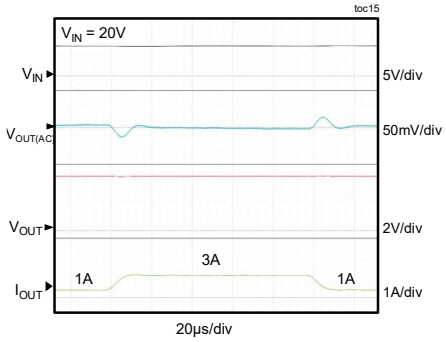
MAX77726
LOAD TRANSIENT
3.3V OUTPUT



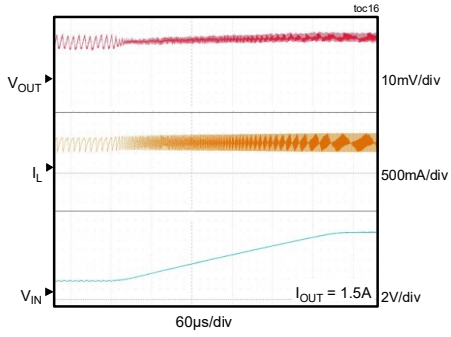
MAX77726
LOAD TRANSIENT
5.0V OUTPUT



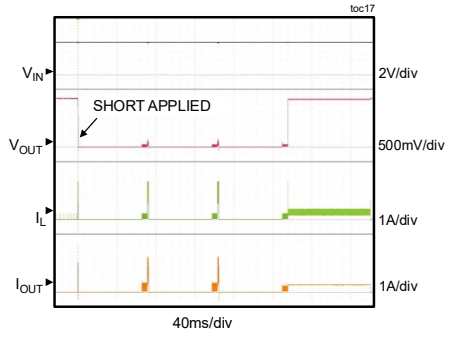
MAX77726
LOAD TRANSIENT
15V OUTPUT



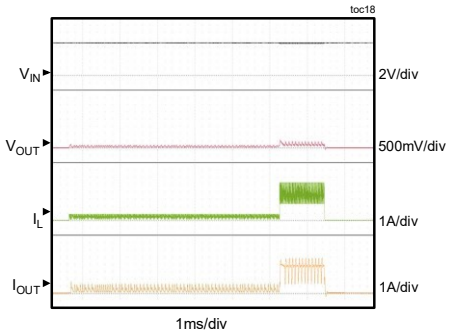
MAX77726
LINE TRANSIENT
3.3V OUTPUT



SHORT-CIRCUIT RESPONSE
3.3V OUTPUT



SHORT-CIRCUIT RESPONSE
3.3V OUTPUT



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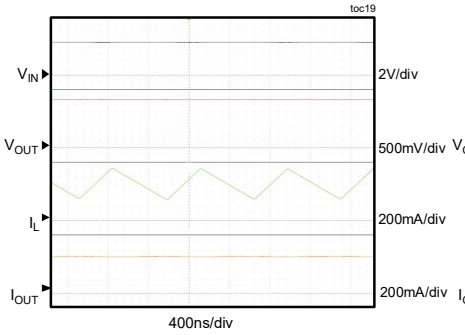
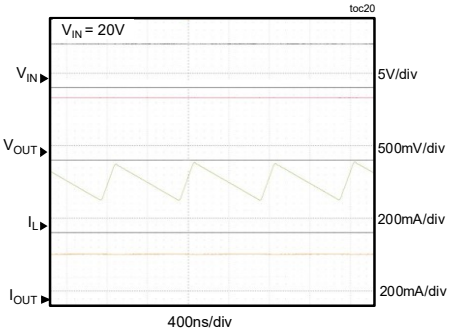
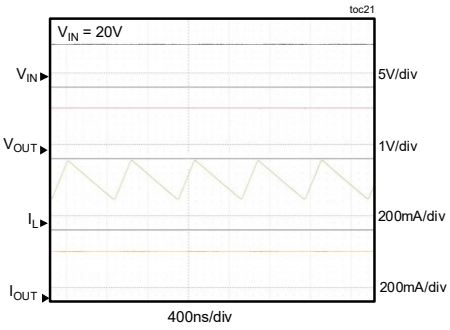
SWITCHING WAVEFORM
3.3V OUTPUT



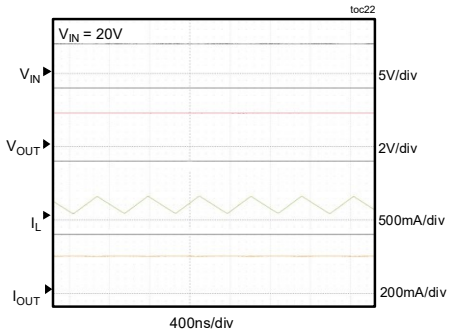
SWITCHING WAVEFORM
3.3V OUTPUT



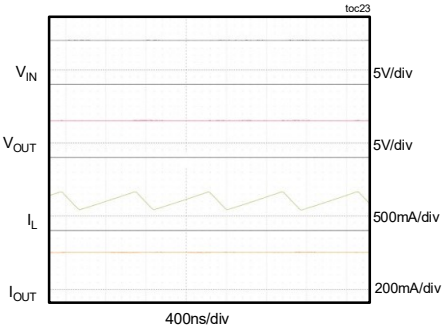
SWITCHING WAVEFORM
5.0V OUTPUT



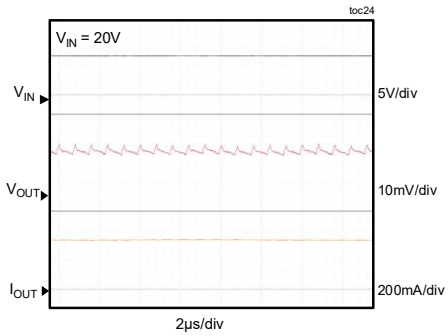
SWITCHING WAVEFORM
9.0V OUTPUT



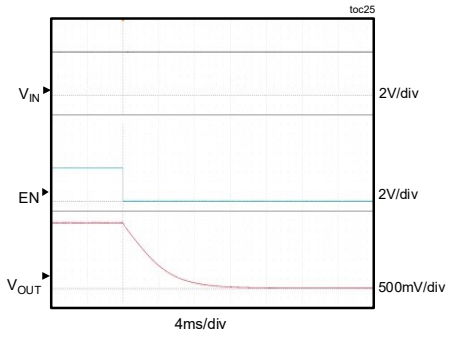
SWITCHING WAVEFORM
15V OUTPUT



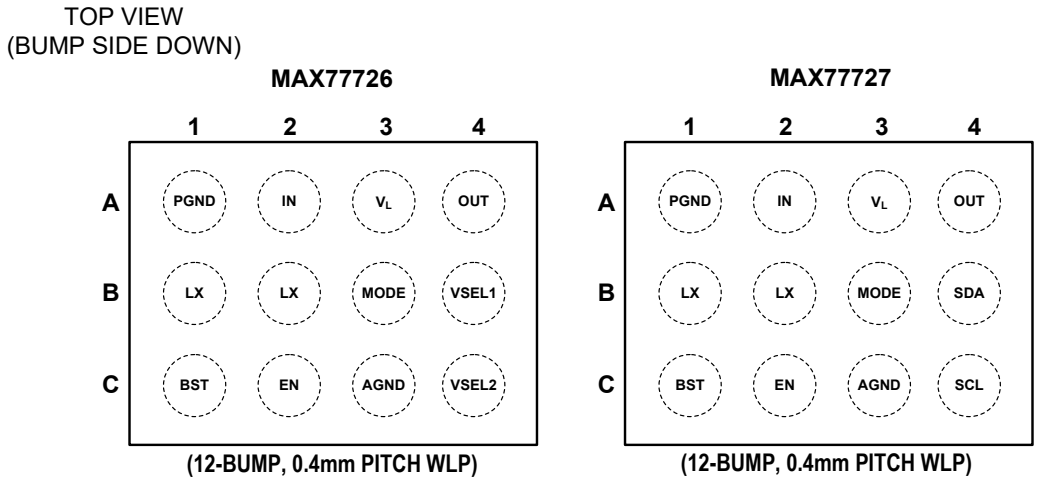
OUTPUT VOLTAGE RIPPLE
3.3V OUTPUT



ENABLE SHUTDOWN WAVEFORM
3.3V OUTPUT



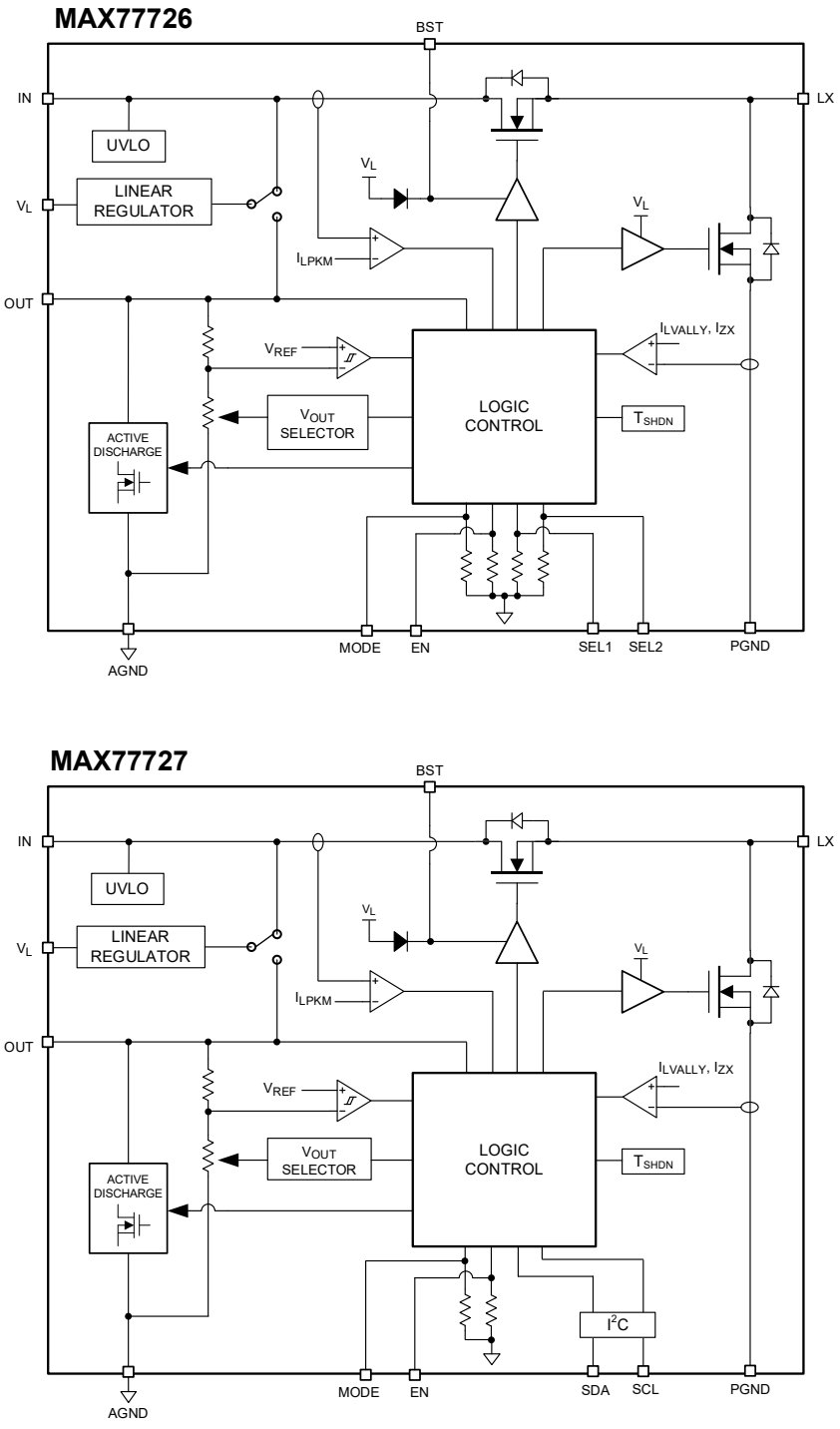
Pin Configurations



Pin Descriptions

PIN	NAME	FUNCTION	Type
A1	PGND	Power Ground Pin. Connect to the system ground.	Ground
A2	IN	Input Supply Pin. Bypass the pin to ground with a 10µF ceramic capacitor. Connect the capacitor to the IN and PGND pins with short connections. Depending on the specific application requirements, more capacitance may be needed.	Power
A3	V_L	1.8V Internal Regulator Output Pin. Connect a 1.0µF capacitor between this pin and AGND.	Power
A4	OUT	Output Voltage Sense Pin. Connect to the output-voltage capacitor or remote system voltage sensing point.	Analog
B1, B2	LX	Switching Node Pins. Connect the inductor between the pin and the output voltage node.	Power
B3	MODE	**MAX77726**: Mode Select Pin for Ultrasonic Mode (USM) and Low Power Mode (LPM) in light load. The pin is active after the soft-start ends, and the output reaches regulation. It has an internal 300kΩ pulldown resistor. **MAX77727**: Tie to MODE Pin to AGND. Using Register to switch mode between LPM, USM, and FPWM.	Digital
B4	VSEL1	**MAX77726**: Voltage Select Pin 1. It has an internal 300kΩ pulldown resistor.	Digital
B4	SDA	**MAX77727**: I^2C data input/output.	Digital
C1	BST	Bootstrap Pin for Driving High-Side MOSFET. Connect a 0.22µF capacitor between the LX and BST pins with minimum loop inductance.	Power
C2	EN	Enable Input Pin. Force this pin to a value higher than 1.0V to enable the converter. Force this pin below 0.3V to disable the device. Once disabled, the output gets discharged through an active discharge circuit. Connect to IN if the feature is not used. It has an internal 300kΩ pulldown resistor.	Digital
C3	AGND	Analog Ground Pin. Connect to the system ground net.	Ground
C4	VSEL2	**MAX77726**: Voltage Select Pin 2. It has an internal 300kΩ pulldown resistor.	Digital
C4	SCL	**MAX77727**: I^2C clock input.	Digital

Functional Block Diagrams



Detailed Description

The MAX77726/MAX77727 are small, high-efficiency nano power step-down (buck) DC-DC converters. The step-down converter uses synchronous rectification and internal current mode compensation. The buck operates on an input supply voltage between 3.6V and 22V. See the *Functional Block Diagrams* for more details.

The MAX77726/MAX77727 buck converter uses a current-control hysteretic topology. The buck converter senses the inductor current to implement a pseudo-fixed inductor ripple current, yielding an approximately 1.2MHz switching frequency in CCM operation under typical operating conditions (V_{IN} = 9V, V_{OUT} = 3.3V with a 2.2µH inductor). The switching frequency varies depending on operating conditions to accommodate the pseudo-fixed inductor current ripple.

During DCM operation, the buck converter turns on the high-side MOSFET until the inductor current reaches the desired current limit threshold. The buck converter then turns on the low-side MOSFET to deliver the energy stored in the inductor until the inductor current falls below I_{ZX} (zero crossing). When zero crossing is no longer detected due to an increased load current, the buck controller increases the peak current limit threshold and repeats the process. When zero crossing is no longer detected, the part transitions into CCM.

Once the sensed output voltage at the OUT pin reaches the percentage of output voltage target level ($V_{OUT\_ACC\_LPM}$) of low-power mode, the buck converter goes into low-power mode by turning off control circuits whenever the inducto current zero crossing is detected. In low-power mode, the controller wakes up every 40ms to check if the output voltage is still higher than $V_{OUT\_ACC\_LPM}$. If the output voltage hits $V_{OUT\_ACC\_LPM}$ while the buck controller is awake, it initiates LX switching. In case the output voltage drops below $V_{OUT\_ACC\_LPM}$ by 10mV, the buck controller exits low-power mode immediately.

Output Enable Control

The MAX77726 includes an EN pin that can be used to turn on the device. It can be connected to a separate supply and pulled up to IN. When the EN pin is pulled HIGH, the MAX77726 enters the soft-start process to bring the buck converter to the output target voltage. When the EN pin goes low, the MAX77726 stops switching immediately and turns on the output voltage active discharge circuit described in the *Output Voltage Active Discharge* section. The MAX77727 also introduces an ENABLE register, which is disabled by default. Users must turn it ON through the I²C interface. See *Table 1* for the EN function.

Table 1. Enable of MAX77726 and MAX77727

	ENABLE PIN	ENABLE REGISTER	BUCK CONVERTER
MAX77726	0	X	Disabled
	1	X	**Enabled**
MAX77727	0	X	Disabled
	1	0	Disabled
	1	1	**Enabled**

Startup

When the EN pin goes logic HIGH on MAX77726 or MAX77727, the internal reference circuit and the bias circuits start up and the output voltage target levels are loaded from OTP memory. In the MAX77727, the I²C function is enabled as well. Once the Enable command is given (EN pin for MAX77726, EN register for MAX77727), within about 2.5ms of startup delay time, the Buck initiates the soft-start. The soft-start function is to prevent the Buck from drawing too much current from the input source (due to an inrush current to the output capacitors). After burst initiates, the startup timer begins counting approximately 5ms (typical). During this interval, the OCP function is blanked to ensure a successful startup. Once the timer expires, OCP detection becomes active. Users should ensure sufficient current ability design margin for application conditions.

Shutdown

When the EN pin (or EN register) is pulled to the logic LOW threshold, the buck converter stops switching and turns on the output voltage discharge circuit until the output is discharged.

Output Voltage Target

The MAX77726 features VSEL1 and VSEL2 pins, allowing quick and easy output voltage configuration by applying different logic levels. It supports preset voltages of 3.3V, 5V, 9V, and 15V. See *Table 2* for details on VSEL pin settings.

In contrast, the MAX77727 has a default output of 1.8V and requires I²C communication for voltage adjustment. It offers fine resolution with 100mV steps from 1.8V to 4.9V and 250mV steps from 5V to 15V. Transitions from high to low are achieved using the active discharge circuit at OUT. Contact Analog Devices if other output target levels are desired.

Output Voltage Compensation

For high-current applications, the MAX77726 implements an automatic output voltage offset mechanism that raises the regulated output voltage by +1% across the entire load range (V_{OUT} = 5V to 15V). For example, when the output is programmed to 5V, the device delivers approximately 5.05V at the output. This intentional offset compensates for resistive voltage drops along the power delivery path, ensuring that the point-of-load voltage remains within specification under full-load conditions. Note that this output voltage compensation applies only to the MAX77726 HV range (V_{OUT} = 5V to 15V). For requirements regarding MAX77727 HV, contact Analog Devices for further support.

Switch Current Limit

The MAX77726/MAX77727 provides a cycle-by-cycle switch current limit (ILIM) at the high-side MOSFET. When the peak current limit is triggered, the buck turns off the high-side MOSFET immediately, and the low-side MOSFET begins discharging the inductor current. The high-side MOSFET stays off until the inductor current reaches 50% of the ILIM. In case the MAX77726/MAX77727 detects peak current limit events more than 128 times consecutively, the MAX77726/MAX77727 enters hiccup mode and keeps both high-side and low-side MOSFETs off for about 60ms before attempting to start up again. When zero crossing is detected at the low-side MOSFET, both the high-side and the low-side MOSFETs are turned off (Hi-Z state of LX node) until the voltage at the OUT pin falls below its target output voltage.

Excessive parasitic inductance on long output traces may induce negative voltage transients at V_{OUT} during over-current protection (OCP) events, which can potentially damage the device. To suppress such negative ringing, it is recommended to place an external Schottky barrier diode (SBD) across the output to provide clamping protection.

Output Voltage Active Discharge

When the MAX77726/MAX77727 is disabled by the EN pin, EN Register, or a UVLO fault event occurs, the active discharge circuit is engaged to discharge the energy stored at the output capacitor. When the active discharge circuit is activated, a open loop current source (FET) is connected between the OUT pin and AGND. Due to the FET-based discharge structure, the discharge current is not regulated. Based on the intrinsic MOSFET characteristics, V_{OUT} (i.e., V_{DS}) directly influences the discharge current as well. At V_{OUT} = 15V, the discharge current is typically around 50mA, with a maximum current of approximately 200mA (guaranteed by design). System designers should carefully verify power-down sequencing behavior, consider that variations in discharge current may be significant, and assess MOSFET power dissipation for suitability.

Undervoltage Lockout

When the input voltage falls below the UVLO falling threshold (V_{UVLO_F}) during the operation, the MAX77726/MAX77727 disables the buck output immediately. If the EN pin is kept HIGH, the MAX77726/MAX77727 automatically reinitiates the startup procedure when the input voltage rises above the UVLO rising threshold (V_{UVLO_R}).

Thermal Shutdown

When the junction temperature exceeds 150ºC (typ), the buck converter output is disabled and is not allowed to restart until the junction temperature drops below the thermal shutdown hysteresis level (130ºC, typ).

Applications Information

Voltage Selection (MAX77726)

Output voltage is selected according to *Table 2*.

Table 2. VSEL Pin and V_{OUT} Set

VSEL1	VSEL2	V_{OUT} (V)
H	H	15.0
H	L	9.0
L	H	3.3
L	L	5.0

The VSEL1 and VSEL2 pins have internal 300kΩ pulldown resistors.

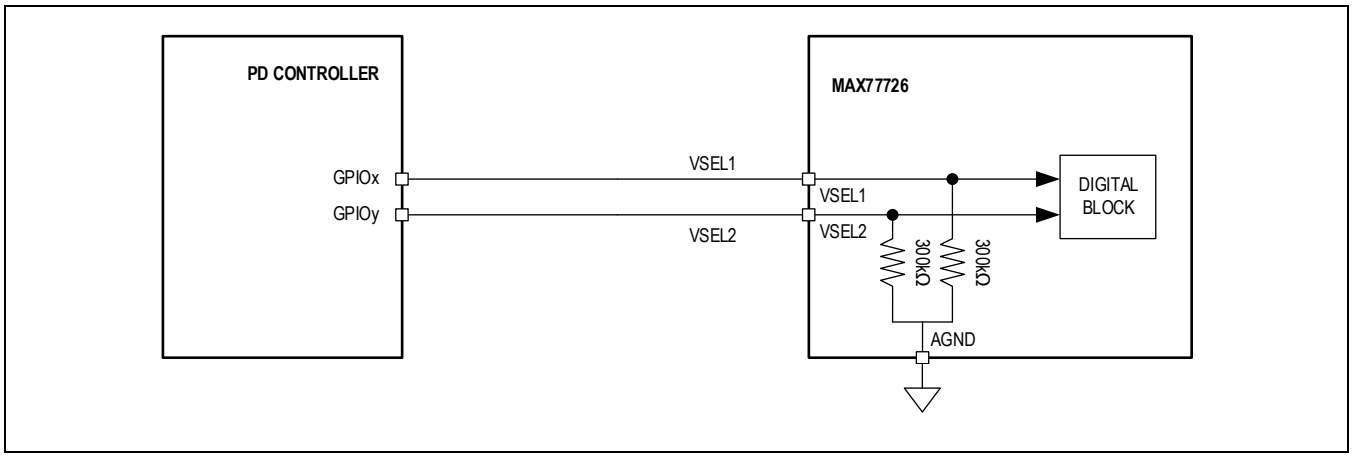


Figure 1. Pulldown Resistor for VSELx

Mode Selection

The MAX77726/MAX77727 devices offer not only the ultra-low quiescent current Low Power Mode (LPM), but also provide flexible operating-mode options, including Ultrasonic Mode (USM) and Forced PWM Mode (FPWM). *Table 3*. shows the configuration options for USM and FPWM on the MAX77726 and MAX77727.

- USM: The converter seamlessly operates at a minimum switching frequency of 33kHz (typical) to avoid acoustic noise interference while operating at light loads in Ultrasonic Mode (USM). Selecting Ultrasonic Mode is done by setting the MODE pin or the MODE register.

- FPWM: The converter maintains a constant switching frequency across the entire output-load range, enabling fast transient response and ripple performance. The inductor current is allowed to go negative (reverse current) during the off-time to maintain Continuous Conduction Mode (CCM), ensuring the switching frequency remains constant even at light loads or no-load conditions. The FPWM feature is currently enabled only on the MAX77727. For FPWM support on the MAX77726, contact Analog Devices.

Table 3. LPM/USM/FPWM Selection on MAX77726/MAX77727

	MODE PIN STATE	BCK_CNFG2 BIT [6]	BCK_CNFG1 BIT [5]	OPERATION
MAX77726	0	N/A	N/A	Low Power Mode
	1	N/A	N/A	Ultrasonic Mode
MAX77727	0	0	0	Low Power Mode
	0	1	0	Ultrasonic Mode
	0	0	1	Forced PWM Mode

Dropout Mode Selection

The MAX77726/MAX77727 automatically enters Dropout Mode when the high-side MOSFET on-time exceeds approximately 20µs. This condition typically occurs when V_{IN} approaches V_{OUT}, and the converter can no longer maintain normal buck-switching operation. In Dropout Mode, the high-side MOSFET is fully turned on, allowing V_{OUT} to follow V_{IN} minus conduction losses.

As V_{IN} approaches V_{OUT}, the switching frequency in Buck Mode (DCM/CCM/USM) gradually decreases and may fall into very low-frequency ranges due to the internal control mechanism. To avoid any frequency-band oscillation between Buck Mode and Dropout Mode, it is recommended to maintain sufficient voltage headroom, such as keeping V_{OUT} at least 1.5V below V_{IN}. ($V_{OUT} \le V_{IN} - 1.5V$).

During operation in Dropout Mode, V_{IN} should remain equal to or below the target V_{OUT} level. For heavy loading, special attention should be given to the effective input capacitance, which must directly sustain the load current. An effective input capacitance of greater than 10µF (after accounting for DC bias and component tolerance) is recommended to maintain a stable input voltage ripple during dropout operation.

Inductor Selection

Choose an inductor with a saturation current that is greater than or equal to the maximum peak current limit setting (ILIM). Inductors with lower saturation current and higher DCR ratings tend to be physically small. Higher DCR values reduce buck efficiency. Choose the RMS current rating of the inductor (the current at which temperature rises appreciably) based on the system's expected load current. The chosen inductor value should ensure that the peak inductor ripple current (I_{PEAK}) is below the high-side MOSFET peak current limit (I_{LIM}) so that the buck can maintain voltage regulation. 2.2µH value inductors are recommended through the operation range of the device.

Input Capacitor Selection

Sufficient input capacitance (C_{IN}) helps minimize V_{IN} ripple. For typical buck operation, choose the input capacitor (C_{IN}) to be a 10µF nominal capacitor that maintains 2µF effective capacitance. For C_{IN} requirements during Dropout Mode operation, refer to the *Dropout Mode Selection* section. Larger values improve the decoupling of the buck converter but increase inrush current from the voltage supply when connected. C_{IN} reduces the current peaks drawn from the input power source during buck operation and filters the switching noise in the system.

Output Capacitor Selection

Sufficient output capacitance (C_{OUT}) is required for the stable operation of the buck. Effective C_{OUT} is the actual capacitance value seen by the buck output during operation. Choose an effective C_{OUT} carefully, considering the capacitor's initial tolerance, temperature variation, and derating under DC bias. Ceramic capacitors with X5R or X7R dielectric are highly recommended for their small size, low ESR, and low temperature coefficients. All ceramic capacitors derate under DC bias voltage (effective capacitance decreases as DC bias increases). Generally, small-case-size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information or contact Analog Devices for further support.

The output capacitor must meet the effective minimum capacitance requirement to ensure appropriate output-voltage ripple and to avoid any false triggering of the FBHI threshold. *Table 4* shows the typical minimum C_{OUT} range for each V_{OUT} interval under no-load conditions. System designers should evaluate the actual load profile and the DVS application range when determining the final output-capacitance value.

Table 4. Recommended Minimum Effective Output Capacitance

V_{OUT} RANGE (V)	RECOMMENDED MINIMUM EFFECTIVE OUTPUT CAPACITANCE (µF)
$1.8 \le V_{OUT} < 3.3$	120
$3.3 \le V_{OUT} < 5$	80
$5 \le V_{OUT} < 15$	60
$V_{OUT} = 15$	20

Increasing C_{OUT} benefits the output ripple and load transient response. However, designers must evaluate the impact on the startup inrush current within the soft-start duration and verify that the phase margin remains adequate for loop stability. See the *Startup* section for additional guidance on startup design considerations. *Table. 5* shows the recommended maximum C_{OUT} for typical no-load applications. For applications operating outside the capacitance ranges listed in *Table 5*, contact Analog Devices to ensure a comprehensive system-level evaluation.

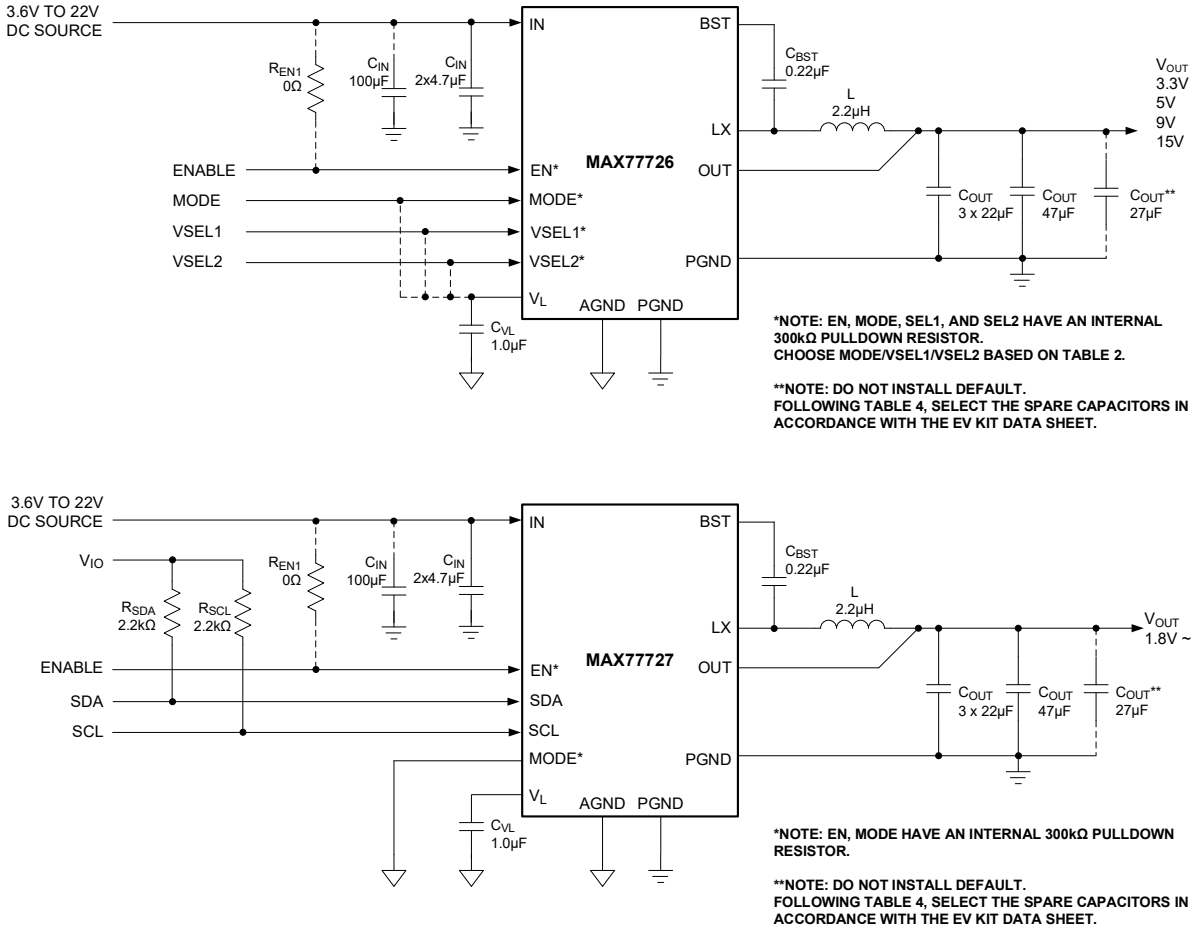
Table 5. Recommended Maximum Effective Output Capacitance

V_{OUT} RANGE (V)	RECOMMENDED MAXIMUM EFFECTIVE OUTPUT CAPACITANCE (µF)
$1.8 \le V_{OUT} \le 4.9$	200
$5 \le V_{OUT} \le 15$	100

Bootstrap Capacitor Selection

Sufficient bootstrap capacitance is required to ensure that the internal gate drive for the switch MOSFETs is properly biased. Select a bootstrap capacitor C_{BST} value of 0.22µF. Ensure that the voltage rating of the bootstrap capacitor is a minimum of 2.5V. For a stable MOSFET gate driver supply, we recommend ensuring that the minimum effective capacitance at a 1.8V DC bias is greater than 0.18µF (approximately -20% of 0.22µF).

Typical Application Circuit



Layout Guidelines

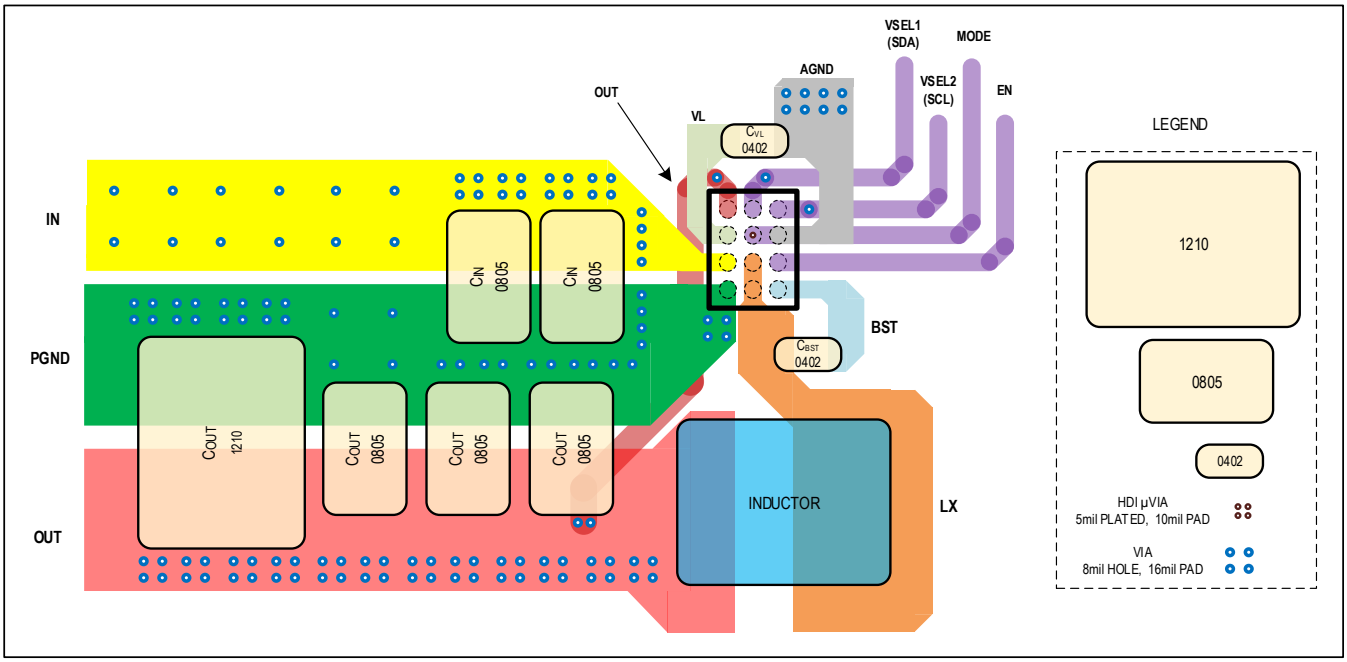


Figure 2. Layout Guidelines

An excellent PCB layout optimizes product performance by lowering switching and conduction losses, smoother power flow, and cleaner control signals. The MAX77726/MAX77727's pinout design separates the power and signal stages, enabling a cleaner layout. Based on this, *Figure 2* shows ADI's recommended PCB layout for the MAX77726/MAX77727. Only the HDI PCB layout is shown here; for non-HDI PCBs, contact Analog Devices for further assistance.

The following are the key points for PCB layout:

- Input and Output Capacitors Should Be Placed Close to the IC Pins: Since the IC operates at high frequencies, this layout minimizes ringing caused by loop inductance and improves transient response. We also recommend placing C_{OUT} close to the IC, as the AC ripple current still passes through C_{OUT}. If C_{OUT} is too far, ACR losses increase due to the longer path.
- Place the BST Capacitor as Close to the IC as Possible: The BST capacitor provides the V_{GS} voltage for the internal high-side (HS) switch. It should be placed as close as possible to the pin to maintain the HS driver's power quality.
- LX Node Arrangement: The LX Node in a Buck circuit has high dv/dt, so it is recommended to use the TOP Layer for the LX path and place PGND underneath it as shielding, which can create a coaxial cable effect to prevent radiation interference.
- OUT Sense: OUT is the output voltage feedback pin, which should be routed to the MLCC (C_{OUT}) and connected back to the IC using a Kelvin connection. It also serves as an active discharge path. Thus, attention must be paid to the path's current-carrying capability.
- VIA Planning: The number and diameter of vias depend on the operating frequency. Due to the skin effect, smaller diameters and more vias are preferred at higher frequencies. This also depends on PCB thickness, layer count, and other factors. Additionally, for reliability, only laser-drilled vias are allowed under the WLP package's IC pins in the vertical direction, rather than mechanical drilling.
- PGND and AGND Arrangement: Connect the PGND bump to the low-impedance ground plane on the PCB with vias placed next to the pin. Do not create PGND islands, as PGND islands risk interrupting hot loops. Connect the AGND and AGND island to the same low-impedance ground plane on the PCB (the same net as PGND).
- Do not Overlook Ceramic Capacitor DC Voltage Derating: Carefully choose capacitor values and case sizes. For more information, refer to the *Output Capacitor Selection* section in the MAX77726/MAX77727 IC data sheet and *Tutorial 5527*.

Register Map

FUNC

I²C Slave Address

The MAX77727 has one slave address. The least significant bit is the read/write\ indicator (1 for read, 0 for write).

• PMIC(SID): 0x44 / 0x45

ADDRESS	NAME	MSB							LSB
PMIC_FUNC									
0x00	PMIC_ID[7:0]	ID[7:0]							
0x01	PMIC_REV[7:0]	PMIC_REV_RSVD_7_4[3:0]				REV[3:0]			
0x02	VOUT[7:0]	HVOUT	VOUT_SPR_6	VOUT[5:0]					
0x03	BCK_CNFG1[7:0]	–	–	FPWM	–	–	–	–	–
0x04	BCK_CNFG2[7:0]	BUCK_DIS	MODE	–	–	–	–	–	–
0x09	STATUS_LATCH[7:0]	–	–	–	–	–	PLIM	TLIM	VIN_UVLO

Register Details

PMIC_ID (0x00)

PMIC ID

BIT	7	6	5	4	3	2	1	0
Field	ID[7:0]							
Reset	0x72							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ID	7:0	ID of MAX77727

PMIC_REV (0x01)

PMIC revision

BIT	7	6	5	4	3	2	1	0
Field	PMIC_REV_RSVD_7_4[3:0]				REV[3:0]			

Reset		
Access Type	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
PMIC_REV_RSVD_7_4	7:4	Spare Bits, No Function
REV	3:0	PMIC Silicon Revision

VOUT (0x02)

Output voltage selection

BIT	7	6	5	4	3	2	1	0
Field	HVOUT	VOUT_SPR_6	VOUT[5:0]					
Reset								
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
HVOUT	7	Buck High/Low Voltage Range Selection	**Value** / **Enumeration** / **Decode** 0x0 / / Low voltage range 0x1 / / High voltage range
VOUT_SPR_6	6	Spare Bit, No Function	
VOUT	5:0	BUCK Output Voltage	**Value** / **HVOUT = 0** / **HVOUT = 1** 0x0 / 1.8 / 5.0 0x1 / 1.8 / 5.0 0x2 / 1.8 / 5.0 0x3 / 1.8 / 5.0 0x4 / 1.8 / 5.0 0x5 / 1.8 / 5.0 0x6 / 1.8 / 5.0 0x7 / 1.8 / 5.0

BITFIELD	BITS	DESCRIPTION	DECODE		
			0x8	1.9	5.25
			0x9	2.0	5.5
			0xA	2.1	5.75
			0xB	2.2	6.0
			0xC	2.3	6.25
			0xD	2.4	6.5
			0xE	2.5	6.75
			0xF	2.6	7.0
			0x10	2.7	7.25
			0x11	2.8	7.5
			0x12	2.9	7.75
			0x13	3.0	8.0
			0x14	3.1	8.25
			0x15	3.2	8.5
			0x16	3.3	8.75
			0x17	3.4	9.0
			0x18	3.5	9.25
			0x19	3.6	9.5
			0x1A	3.7	9.75
			0x1B	3.8	10.0
			0x1C	3.9	10.25
			0x1D	4.0	10.5
			0x1E	4.1	10.75
			0x1F	4.2	11.0
			0x20	4.3	11.25
			0x21	4.4	11.5

BITFIELD	BITS	DESCRIPTION	DECODE		
			0x22	4.5	11.75
			0x23	4.6	12.0
			0x24	4.7	12.25
			0x25	4.8	12.5
			0x26	4.9	12.75
			0x27	4.9	13.0
			0x28	4.9	13.25
			0x29	4.9	13.5
			0x2A	4.9	13.75
			0x2B	4.9	14.0
			0x2C	4.9	14.25
			0x2D	4.9	14.5
			0x2E	4.9	14.75
			0x2F	4.9	15.0
			0x30	4.9	15.0
			0x31	4.9	15.0
			0x32	4.9	15.0
			0x33	4.9	15.0
			0x34	4.9	15.0
			0x35	4.9	15.0
			0x36	4.9	15.0
			0x37	4.9	15.0
			0x38	4.9	15.0
			0x39	4.9	15.0
			0x3A	4.9	15.0
			0x3B	4.9	15.0

BITFIELD	BITS	DESCRIPTION	DECODE
			0x3C 4.9 15.0 0x3D 4.9 15.0 0x3E 4.9 15.0 0x3F 4.9 15.0

BCK_CNFG1 (0x03)

Buck control register 1

BIT	7	6	5	4	3	2	1	0
Field	–	–	FPWM	–	–	–	–	–
Reset	–	–		–	–	–	–	–
Access Type	–	–	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
			Value / Enumeration / Decode 0x0 / / Disable FPWM 0x1 / / Enable FPWM
FPWM	5	Forced PWM Mode Control Bit	

BCK_CNFG2 (0x04)

Buck control register 2

BIT	7	6	5	4	3	2	1	0
Field	BUCK_DIS	MODE	–	–	–	–	–	–
Reset			–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
			Value / Enumeration / Decode 0x0 / / BUCK is enabled 0x1 / / BUCK is disabled
BUCK_DIS	7	Buck Disable Control	

BITFIELD	BITS	DESCRIPTION	DECODE
MODE	6	USM Control Bit	Value: 0x0 — Enumeration: — — Decode: Disable USM Value: 0x1 — Enumeration: — — Decode: Enable USM

STATUS_LATCH (0x09)

Fault latch register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	PLIM	TLIM	VIN_UVLO
Reset	–	–	–	–	–		0x0	0x0
Access Type	–	–	–	–	–	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
PLIM	2	Peak Limit Fault	Value: 0x0 — Enumeration: — — Decode: No fault. Buck I_{LIM} has not been reached IPK. Value: 0x1 — Enumeration: — — Decode: Fault. Buck ILIM has been reached IPK.
TLIM	1	Thermal Fault	Value: 0x0 — Enumeration: — — Decode: No Thermal Protection. Junction temperature is below the thermal limitation (TLIM) threshold. Value: 0x1 — Enumeration: — — Decode: Thermal Protection. Junction temperature is above the thermal limitation (TLIM) threshold.
VIN_UVLO	0	Input UVLO	Value: 0x0 — Enumeration: — — Decode: No Fault. No fault since the last time this bit was read.

BITFIELD	BITS	DESCRIPTION	DECODE		
			0x1		Fault. Fault occured at least once since the last time this bit was read.

Ordering Information

PART NUMBER	TEMP RANGE	PACKAGE	FEATURES
MAX77726AWC+	-40°C to +125°C	12-WLP	VSEL1 and VSEL2 pins to select among four output voltage levels preprogrammed to 5V, 3.3V, 9V, and 15V.
MAX77726AWC+T	-40°C to +125°C	12-WLP	VSEL1 and VSEL2 pins to select among four output voltage levels preprogrammed to 5V, 3.3V, 9V, and 15V.
MAX77727AAWC+	-40°C to +125°C	12-WLP	Output voltage programmable from 1.8V to 15V through I^2C.
MAX77727AAWC+T	-40°C to +125°C	12-WLP	Output voltage programmable from 1.8V to 15V through I^2C.

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/25	Release for Market Intro	—