Data Sheet

MAX74840

30V, Single Supply, Low Bias Current, RRO, 8MHz JFET Op Amp

FEATURES

- Wide gain bandwidth product: 8MHz typical
- High slew rate
  - 23V/µs typical (low to high)
  - −18V/µs typical (high to low)
- Low input bias current: ±15pA maximum at T_A = 25°C
- Low offset voltage: ±10mV maximum at T_A = 25°C
- Low offset voltage drift: ±4µV/°C typical
- Input voltage range includes Pin V−
- Rail-to-rail output
- Electromagnetic interference rejection ratio (EMIRR)
  - 90dB typical at f = 1000MHz and f = 2400MHz

APPLICATIONS

- High output impedance sensor interfaces
- Photodiode sensor interfaces
- Transimpedance amplifiers
- ADC drivers
- Precision filters and signal conditioning

GENERAL DESCRIPTION

The MAX74840 is a single-supply, rail-to-rail output (RRO), junction field effect transistors (JFET) input operational amplifiers (Op Amps).

The input voltage range includes the negative supply and the output swings rail-to-rail. This enables the user to maximize dynamic input range in low voltage, single supply applications without the need for a separate negative voltage power supply for ground sense.

Input EMI filters increase the signal robustness in the face of closely located switching noise sources.

The speed, in terms of bandwidth and slew rate, increases along with a strong output drive to improve settling time performance and enables the devices to drive the inputs of modern single-ended, successive approximation register (SAR) analog-to-digital converters (ADCs).

The MAX74840 is specified for operation over the extended industrial temperature range of −40°C to +125°C, and operate from 5V to 30V, with specifications at ±15V. The MAX74840 is available in an 8-lead MSOP package.

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SPECIFICATIONS

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(Supply voltage (V_{SY}) = ±15V, common-mode voltage (V_{CM}) = output voltage (V_{OUT}) = 0V, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			±0.5	±10	mV
		−40°C < T_A < +125°C		±2		mV
Offset Voltage Match					±1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		±4		µV/°C
Input Bias Current	I_B			±3	±15	pA
		−40°C < T_A < +125°C		±1.5		nA
		V_{CM} = −15V		−15		pA
Input Offset Current	I_{OS}				±15	pA
		−40°C < T_A < +125°C		±0.5		nA
Input Voltage Range	IVR		−15.2		+14	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −15V to +12V	82	98		dB
		−40°C < T_A < +125°C		81		dB
Open-Loop Voltage Gain	A_{VO}	R_L = 10kΩ, V_{OUT} = −14.5V to +14.5V	117	122		dB
		−40°C < T_A < +125°C		109		dB
Input Capacitance	C_{INDM}	Differential mode		0.4		pF
	C_{INCM}	Common mode		3.6		pF
Input Resistance	R_{DIFF}	Differential mode		10^{13}		Ω
	R_{CM}	Common mode		10^{13}		Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	14.95	14.97		V
		−40°C < T_A < +125°C		14.9		V
Output Voltage Low	V_{OL}	I_{SINK} = 1mA		−14.955	−14.935	V
		−40°C < T_A < +125°C		−14.88		V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1V		20		mA
Short-Circuit Current	I_{SC}	Sourcing		42		mA
		Sinking		−51		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1kHz, A_V = 1		0.1		Ω
		f = 1kHz, A_V = 10		0.4		Ω

(Supply voltage (V_{SY}) = ±15V, common-mode voltage (V_{CM}) = output voltage (V_{OUT}) = 0V, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Closed-Loop Output Impedance	Z_{OUT}	f = 1kHz, A_V = 100		3		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4V to ±18V	84	100		dB
		−40°C < T_A < +125°C		81		dB
Supply Current per Amplifier	I_{SY}			0.770	1.05	mA
		−40°C < T_A < +125°C		0.725		mA
DYNAMIC PERFORMANCE						
Slew Rate	SR+	V_{OUT} = ±12.5V, R_L = 2kΩ, C_L = 100pF, A_V = 1		23		V/µs
	SR−	V_{OUT} = ±12.5V, R_L = 2kΩ, C_L = 100pF, A_V = 1		−18		V/µs
Gain Bandwidth Product	GBP	A_V = 100, C_L = 35pF		8		MHz
Unity-Gain Crossover	UGC	A_V = 1		7		MHz
−3dB Bandwidth	−3dB	A_V = 1		15.5		MHz
Phase Margin	Φ_M			53		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 10V step, R_L = 2kΩ, C_L = 15pF, A_V = −1		1.5		µs
Settling Time to 0.01%	t_S	V_{IN} = 10V step, R_L = 2kΩ, C_L = 15pF, A_V = −1		2		µs
EMI REJECTION RATIO						
EMI Rejection Ratio	EMIRR	V_{IN} = 100mV p-p, f = 1000MHz		90		dB
		V_{IN} = 100mV p-p, f = 2400MHz		90		dB
NOISE PERFORMANCE						
Voltage Noise	$e_{N\ p-p}$	0.1Hz to 10Hz		0.75		µV p-p
Voltage Noise Density	e_N	f = 10Hz		30		nV/√Hz
		f = 100Hz		15		nV/√Hz
		f = 1kHz		12.5		nV/√Hz
		f = 10kHz		12		nV/√Hz
Current Noise Density	i_N	f = 1kHz		0.8		fA/√Hz
Total Harmonic Distortion Plus Noise, BW = 80kHz	THD + N	A_V = 1, f = 10Hz to 20kHz, V_{IN} = 7V rms at 1kHz		0.0003		%
Total Harmonic Distortion Plus Noise, BW = 500kHz	THD + N	A_V = 1, f = 10Hz to 20kHz, V_{IN} = 7V rms at 1kHz		0.00035		%

(Supply voltage (V_{SY}) = ±15V, common-mode voltage (V_{CM}) = output voltage (V_{OUT}) = 0V, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MATCHING SPECIFICATIONS						
Maximum Offset Voltage over Temperature				0.5		mV
Offset Voltage Temperature Drift				0.25		µV/°C
Input Bias Current				0.5	5	pA
CROSSTALK						
CROSSTALK	C_S	R_L = 5kΩ, V_{IN} = 20V p-p				
		f = 1kHz		−112		dB
CROSSTALK	C_S	f = 100kHz		−72		dB

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
Supply Voltage	36V
Input Voltage	(V−) −0.3V to (V+) +0.2V
Differential Input Voltage	36V
Input Current (Indefinite)	±10mA
Input Current (Duration < 1sec)	±100mA
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (10sec)	300°C
ESD Rating, Human Body Model (HBM)	4kV

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction-to-case thermal resistance.

Table 3. Thermal Resistance

PACKAGE TYPE[1]	θ_{JA}	θ_{JC}[3]	UNIT
1-Layer JEDEC Board	N/A[2]	115	°C/W
2-Layer JEDEC Board	185	N/A[2]	°C/W

[1] Thermal impedance simulated values are based on a JEDEC thermal test board. See JEDEC JESD51.

[2] N/A means not applicable.

[3] For θ_{JC} test, 100µm thermal interface material (TIM) is used. TIM is assumed to have 3.6W/mK.

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

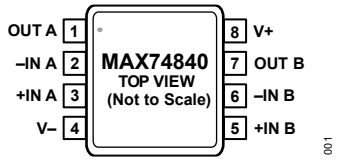

Figure 1. 8-Lead MSOP Pin Configuration

Pin Function Descriptions

Table 4. Pin Descriptions

PIN	NAME	DESCRIPTION
1	OUT A	Output, Channel A.
2	−IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A.
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	−IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

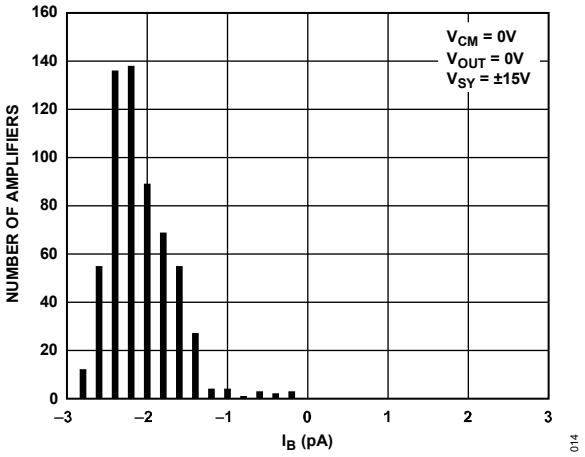

Figure 2. Input Bias Current (I_B) Distribution, V_{SY} = ±15V

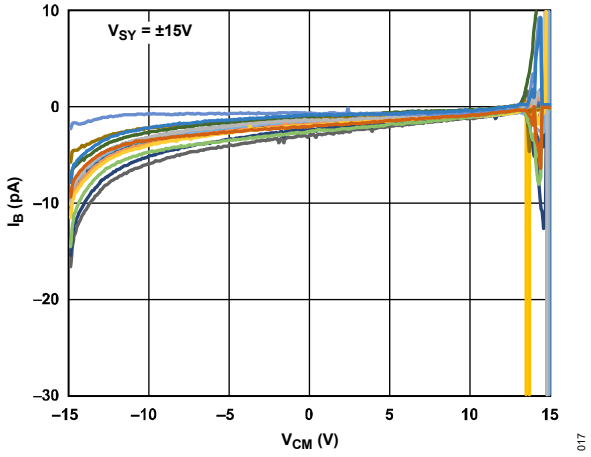

Figure 3. Input Bias Current (I_B) vs. Input Common-Mode Voltage (V_{CM}), V_{SY} = ±15V

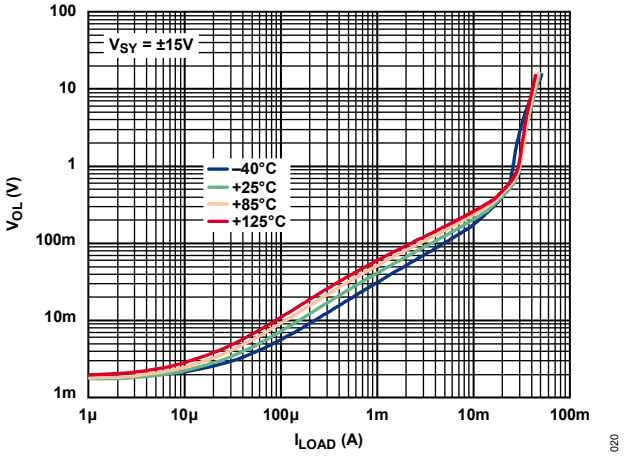

Figure 4. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, V_{SY} = ±15V

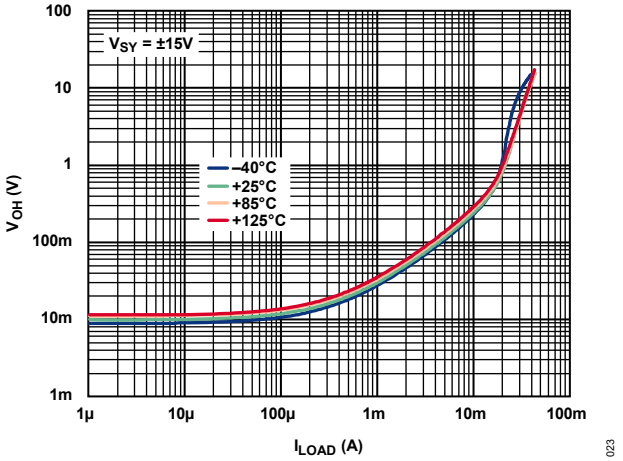

Figure 5. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, V_{SY} = ±15V

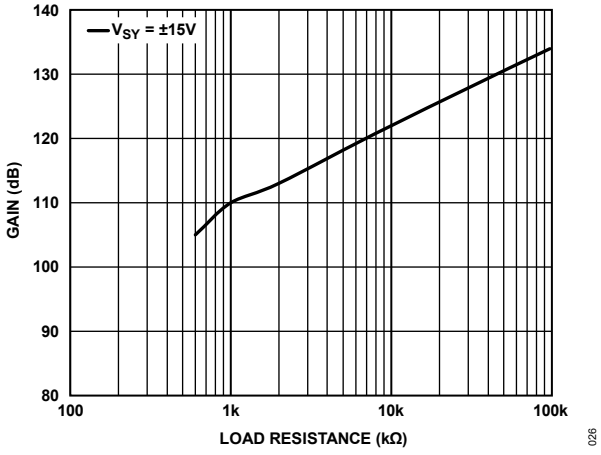

Figure 6. Open-Loop Voltage Gain (A_{VO}) vs. Load Resistance

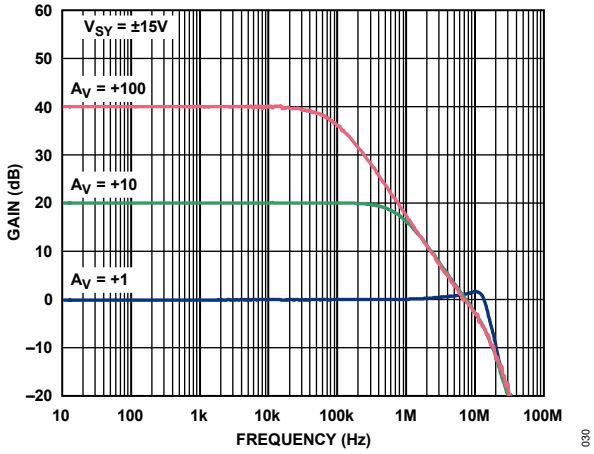

Figure 7. Closed-Loop Gain (A_V) vs. Frequency, V_{SY} = ±15V

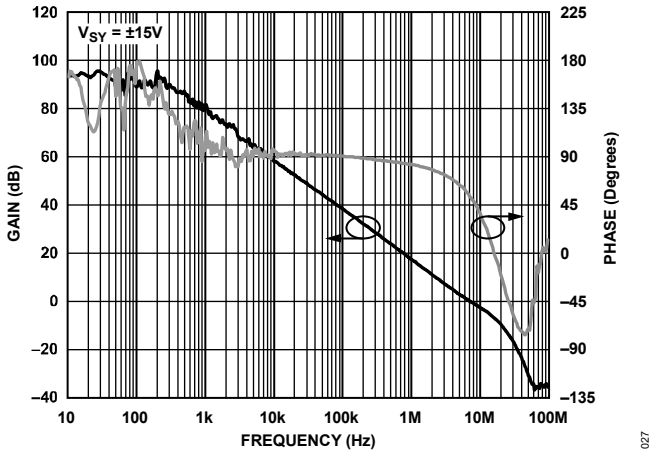

Figure 8. Open-Loop Voltage Gain (A_{VO}) and Phase vs. Frequency, V_{SY} = ±15V

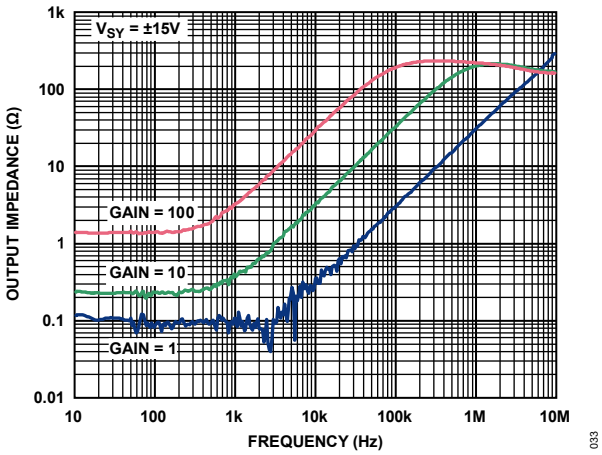

Figure 9. Output Impedance vs. Frequency, V_{SY} = ±15V

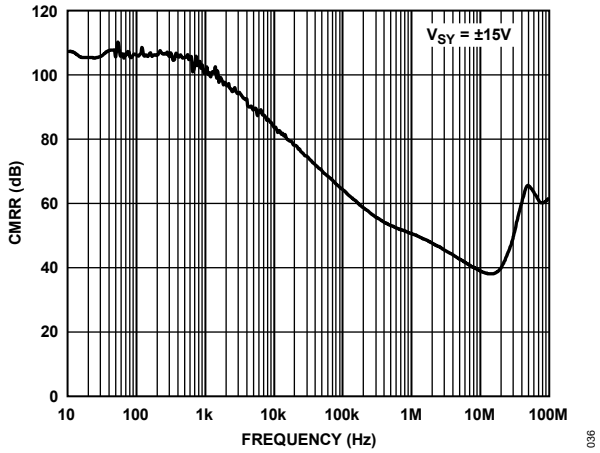

Figure 10. CMRR vs. Frequency, V_{SY} = ±15V

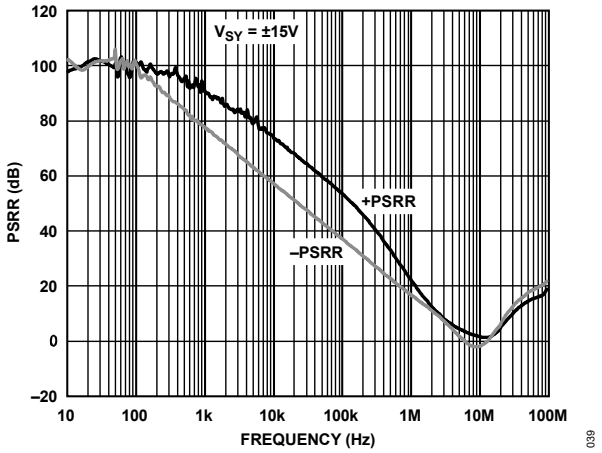

Figure 11. PSRR vs. Frequency, V_{SY} = ±15V

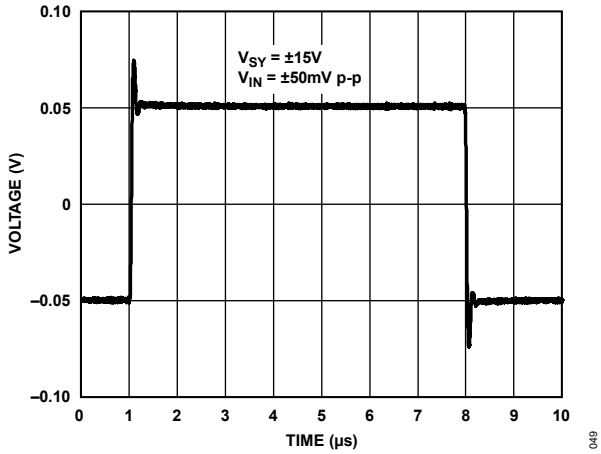

Figure 12. Small Signal Transient Response, V_{SY} = ±15V

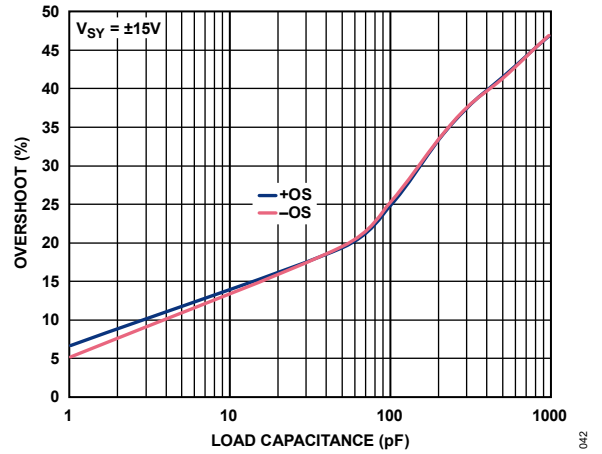

Figure 13. Small Signal Overshoot (OS) vs. Load Capacitance, V_{SY} = ±15V

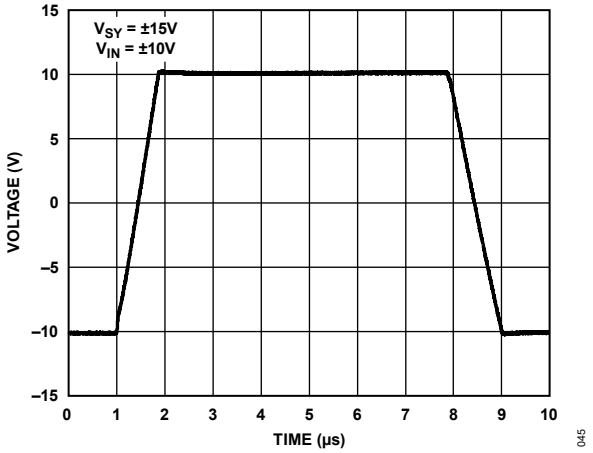

Figure 14. Large Signal Transient Response, V_{SY} = ±15V

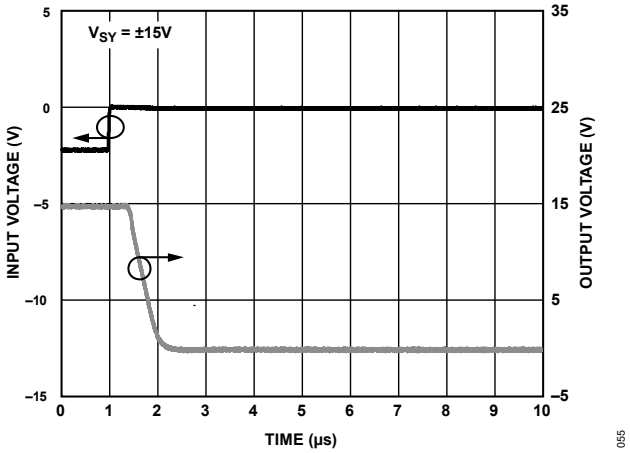

Figure 15. Positive Overload Recovery, A_V = −10, V_{SY} = ±15V

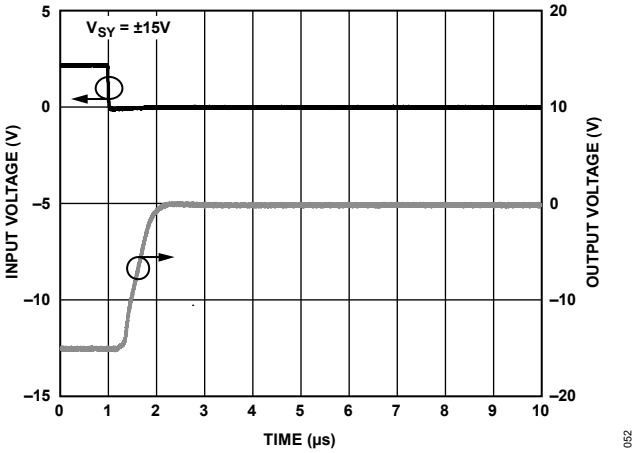

Figure 16. Negative Overload Recovery, A_V = −10, V_{SY} = ±15V

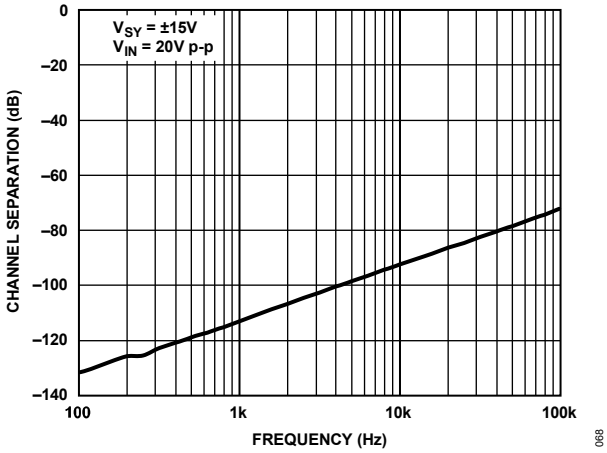

Figure 17. Channel Separation vs. Frequency, V_{SY} = ±15V

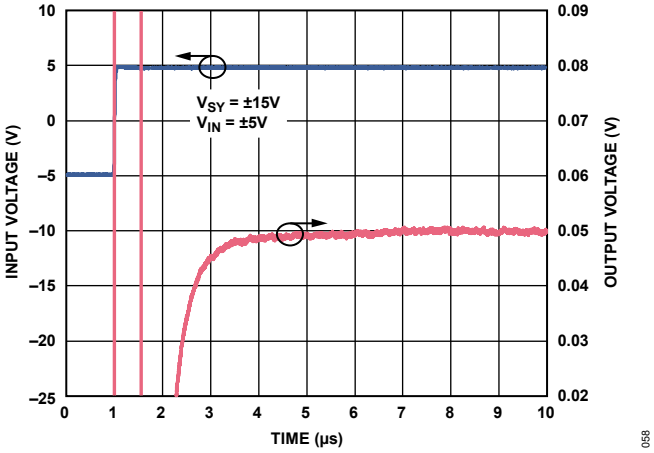

Figure 18. Positive Settling Time, A_V = −10, V_{SY} = ±15V

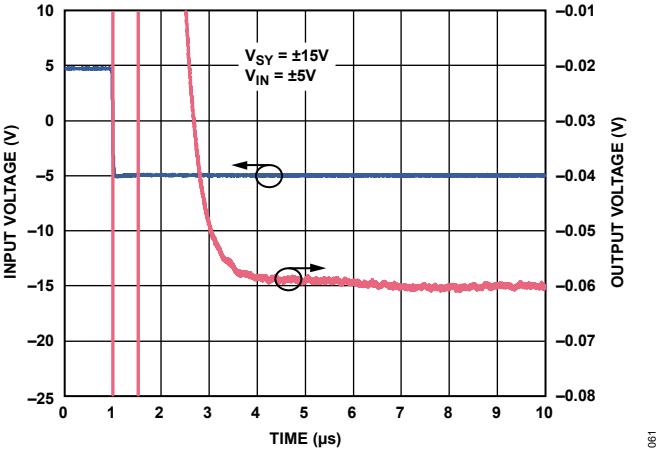

Figure 19. Negative Setting Time, A_V = −10, V_{SY} = ±15V

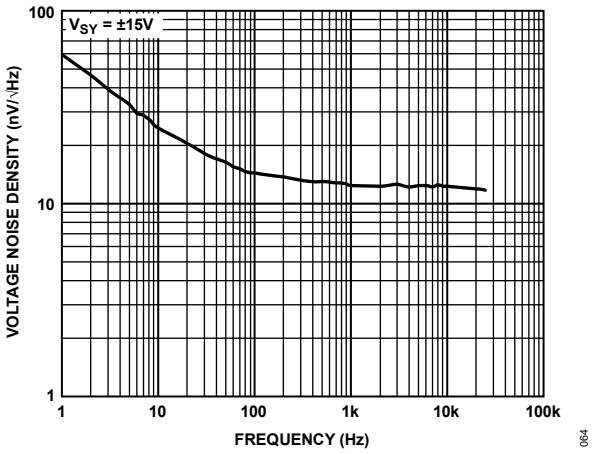

Figure 20. Voltage Noise Density, V_{SY} = ±15V

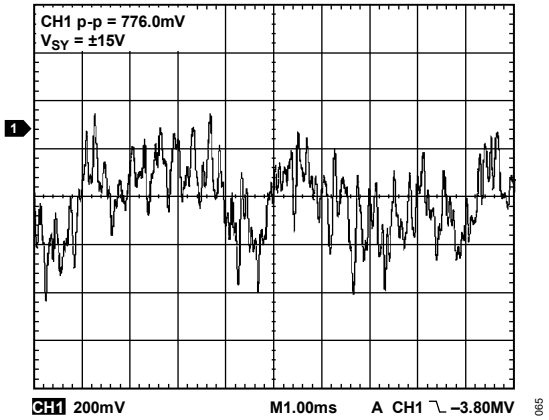

Figure 21. 0.1Hz to 10Hz Noise, V_{SY} = ±15V, Gain = 1Million

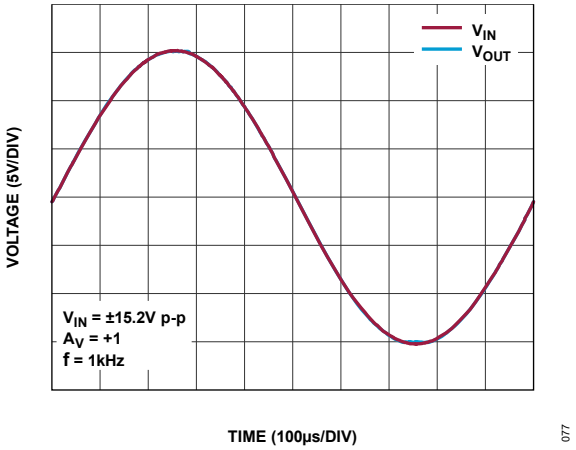

Figure 22. No Phase Reversal

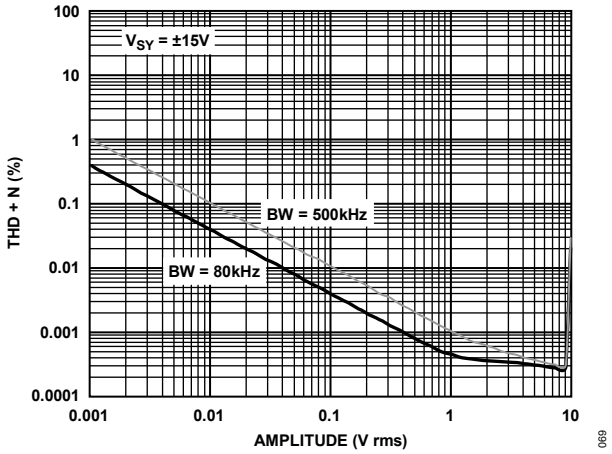

Figure 23. THD + N vs. Amplitude, V_{SY} = ±15V

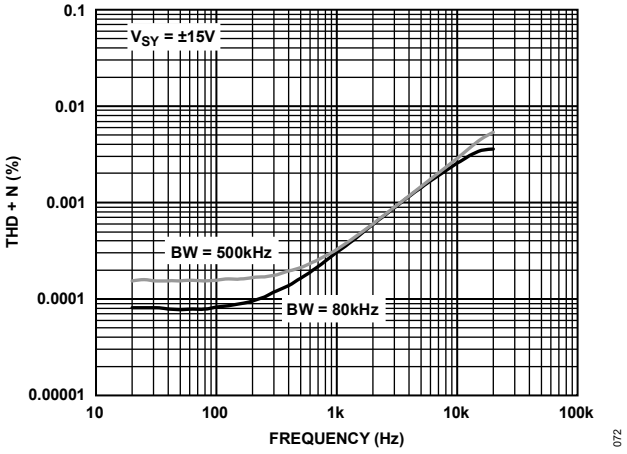

Figure 24. THD + N vs. Frequency, V_{SY} = ±15V

THEORY OF OPERATION

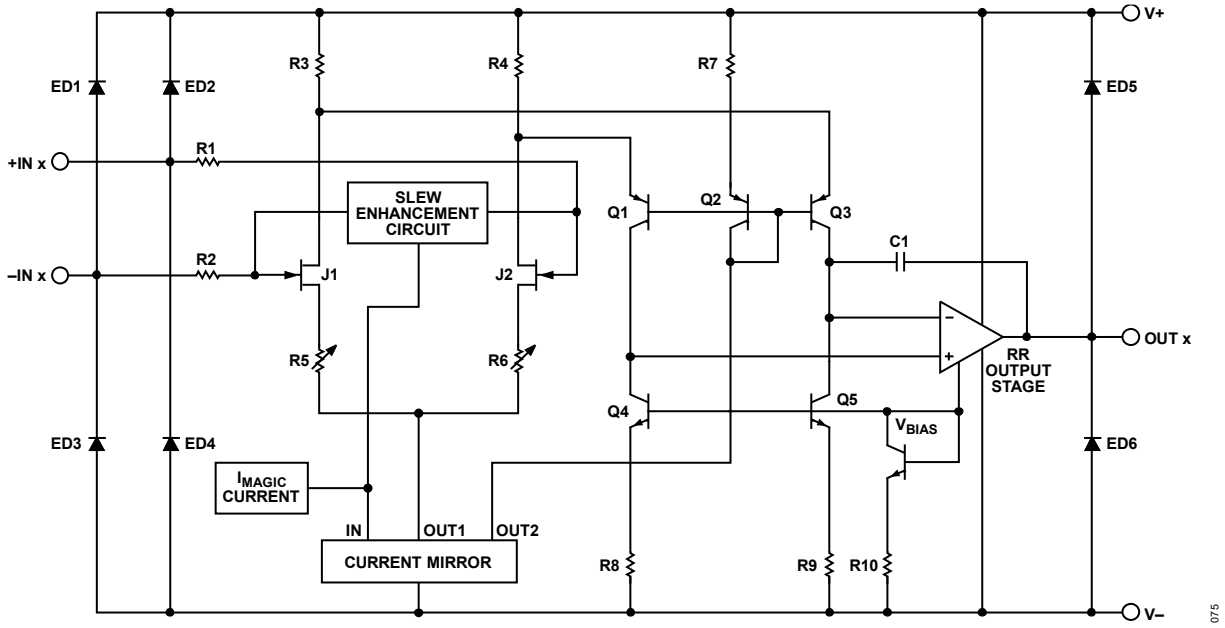

Figure 25. Simplified Circuit Diagram

Input Characteristics

The MAX74840 input stage consists of N-channel JFETs that provide low offset, low noise, and high impedance. The minimum input common-mode voltage extends from −0.2mV below V− to 1V less than V+. Driving the input closer to the positive rail causes loss of amplifier bandwidth and increased common-mode voltage error. *Figure 26* shows the rounding of the output due to the loss of bandwidth. The input and output are superimposed.

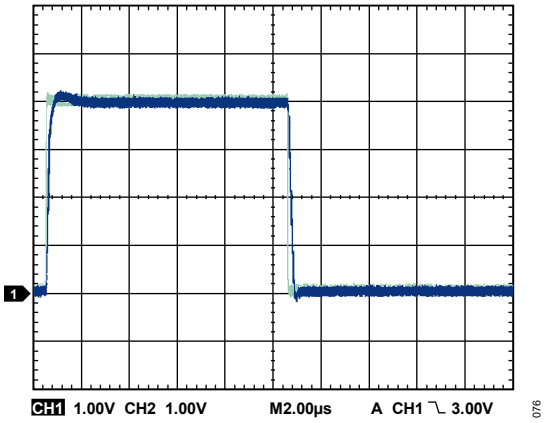

Figure 26. Bandwidth Limiting due to Headroom Requirements

Input Overvoltage Protection

The MAX74840 has internal protective circuitry that allows voltages as high as 0.2V beyond the supplies applied at the input of either terminal without causing damage. Use a current-limiting resistor in series with the input of the MAX74840 if the input voltage exceeds 0.2V beyond the supply rails of the amplifiers. If the overvoltage condition persists for more than a few seconds, damage to the amplifiers can result.

For higher input voltages, determine the resistor value by:

$$\frac{V_{IN} - V_{SY}}{R_S} \leq 10mA \qquad (1)$$

where:

V_{IN} is the input voltage.

V_{SY} is the voltage of either the V+ pin or the V− pin.

R_S is the series resistor.

With a very low input bias current of ±1.5nA maximum up to 125°C, higher resistor values can be used in series with the inputs without introducing large offset errors. A 1kΩ series resistor allows the MAX74840 to withstand 10V of continuous overvoltage and increases the noise by a negligible amount. A 5kΩ resistor protects the inputs from voltages as high as 25V beyond the supplies and adds less than 10µV to the offset voltage of the amplifier.

EMI Rejection Ratio

Figure 27 shows the EMI rejection ratio (EMIRR) vs. the frequency for the MAX74840.

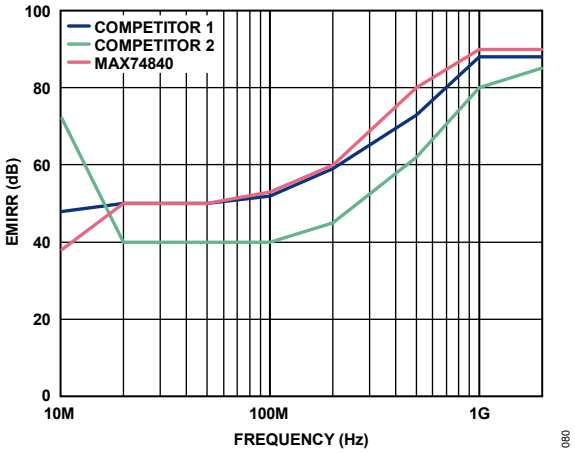

Figure 27. EMIRR vs. Frequency

Output Characteristics

The MAX74840's unique bipolar rail-to-rail output stage swings within 10mV of the supplies with no external resistive load.

The approximate output saturation resistance of the MAX74840 is 24Ω, sourcing or sinking. Use the output impedance to estimate the output saturation voltage when driving heavier loads. As an example, when driving 5mA, the saturation voltage from either rail is approximately 120mV.

If the MAX74840 output drives hard against the output saturation voltage, it recovers within 1.2µs of the input, returning to the linear operating region of the amplifier (see *Figure 15* and *Figure 16*).

APPLICATIONS INFORMATION

Maximum Power Dissipation

The maximum power the MAX74840 can safely dissipate is limited by the associated rise in junction temperature. For plastic packages, the maximum safe junction temperature is 150°C. If this maximum temperature is exceeded, reduce the die temperature to restore proper circuit operation. Leaving the device in the overheated condition for an extended period of time can result in device burnout. To ensure proper operation, it is important to observe the specifications shown in the *Absolute Maximum Ratings* and *Thermal Resistance* sections.

OUTLINE DIMENSIONS

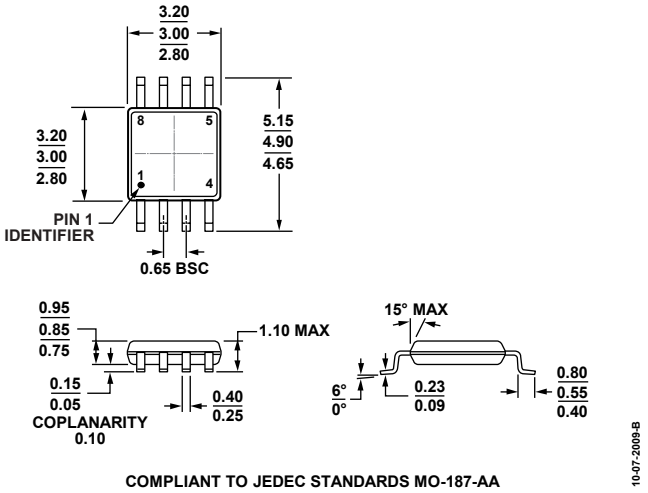

Figure 28.8-Lead Mini Small Outline Package [MSOP] (RM-8) Dimensions shown in millimeters

ORDERING GUIDE

Table 5. Ordering Guide

MODEL[1]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKING QUANTITY	PACKAGE OPTION	MARKING CODE
MAX74840ARMZ	−40°C to +125°C	8-Lead MSOP		RM-8	A6W
MAX74840ARMZ-R7	−40°C to +125°C	8-Lead MSOP	Reel, 1000	RM-8	A6W
MAX74840ARMZ-RL	−40°C to +125°C	8-Lead MSOP	Reel, 3000	RM-8	A6W

[1] Z = RoHS Compliant Part.

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/25	Initial release	—