Data Sheet

MAX74831

24V, 110MHz FastFET Operational Amplifier

FEATURES

- FET input amplifier
- 3pA input bias current
- Low cost
- High speed: 110MHz, −3dB bandwidth (G = +1)
- 180V/µs slew rate (G = +2)
- Low noise
  - 7nV/√Hz (f = 10kHz)
  - 1fA/√Hz (f = 10kHz)
- Wide supply voltage range: 5V to 24V
- Single-supply and rail-to-rail output
- Low offset voltage 3mV maximum
- High common-mode rejection ratio: −100dB
- Excellent distortion specifications
- SFDR −100dBc at 1MHz
- Supply current: 6.6mA per amplifier typical
- No phase reversal

APPLICATIONS

- Photodiode preamplifier (preamp)
- Filters
- Analog-to-digital converter (A/D) drivers
- Level shifting
- Buffering

GENERAL DESCRIPTION

The MAX74831[1] *FastFET*™ amplifier is a voltage feedback amplifier with field-effect transistor (FET) inputs that offers high performance and ease of use. This amplifier is developed in the Analog Devices, Inc., proprietary, complementary bipolar (XFCB) process and allows exceptionally low noise operation (7.0nV/√Hz and 1fA/√Hz) as well as very high input impedance.

The MAX74831 works in a variety of applications with a wide 5V to 24V supply range, single-supply operation, and 110MHz bandwidth. For added versatility, the amplifier also contains rail-to-rail outputs.

Despite the low cost, this amplifier provides excellent overall performance. The amplifier's 0.02% differential gain, 0.02° phase error, and 0.1dB flatness out to 7MHz make it ideal for video applications. Additionally, it offers a high slew rate of 180V/µs, excellent distortion (spurious-free dynamic range (SFDR) of −100dBc at 1MHz), extremely high common-mode rejection ratio (CMRR) of −100dB, and a low input offset voltage of 3mV maximum under warmed up conditions. The MAX74831 operates using a typical supply current of only 6.6mA per amplifier and can deliver up to 30mA of load current.

The MAX74831 is a high performance, high speed, FET input amplifier available in small **8-lead [MSOP] (RM-8)** package. It operates over the industrial temperature range of −40°C to +85°C.

[1] Protected by U. S. Patent No. 6,262,633.

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REVISION HISTORY

8/2026—Revision 0: Initial Version

SPECIFICATIONS

Electrical Characteristics ±12V

At T_A = 25°C, V_S = ±12V, R_L = 1kΩ, unless otherwise noted.

Table 1. Electrical Characteristics ±12V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE					
−3dB Bandwidth	G = +1, V_O = 0.2V p-p	100	110		MHz
	G = +2, V_O = 0.2V p-p		50		MHz
	G = +2, V_O = 2V p-p		40		MHz
Bandwidth For 0.1dB Flatness	G = +2, V_O = 0.2V p-p		7		MHz
Input Overdrive Recovery	G = +1, −12.5V to +12.5V		175		ns
Output Overdrive Recovery	G = −1, −12.5V to +12.5V		170		ns
Slew Rate	G = +2, V_O = 4V step	130	180		V/µs
Settling Time To 0.1%	G = +2, V_O = 2V step		55		ns
	G = +2, V_O = 10V step		250		ns
NOISE/HARMONIC PERFORMANCE					
SFDR	f_C = 1MHz, G = +2, V_O = 2V p-p		−100		dBc
	f_C = 5MHz, G = +2, V_O = 2V p-p		−67		dBc
	f_C = 1MHz, G = +2, V_O = 10V p-p		−85		dBc
Third-Order Intercept	f_C = 10MHz, R_L = 100Ω		24		dBm
Input Voltage Noise	f = 10kHz		7		nV/√Hz
Input Current Noise	f = 10kHz		1		fA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150Ω		0.04		%
Differential Phase Error	NTSC, G = +2, R_L = 150Ω		0.03		Degrees
DC PERFORMANCE					
Input Offset Voltage	V_{CM} = 0V		0.4	3	mV
Input Offset Voltage Drift			1.2	17	µV/°C
Input Bias Current			3	15	pA
	T_{MIN} to T_{MAX}		25		pA
Input Offset Current			2	15	pA
	T_{MIN} to T_{MAX}		2		pA
Open-Loop Gain	V_O = ±10V, R_L = 1kΩ	103	114		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000 || 2.1		GΩ || pF
Differential Input Impedance			1000 || 4.5		GΩ || pF
Input Common-Mode Voltage Range					
FET Input Range		−12 to +8.5	−12.0 to +9.5		V
Common-Mode Rejection Ratio	V_{CM} = −1V to +1V	−85	−100		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1kΩ	−11.8 to +11.8	−11.9 to +11.9		V
	R_L = 350Ω		−11.25 to +11.5		V
Output Current	V_O = 22V p-p, SFDR ≥ −60dBc, f = 500kHz		30		mA
Short-Circuit Current			120		mA

SPECIFICATIONS

Table 1. Electrical Characteristics ±12V (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Capacitive Load Drive	30% overshoot G = +1		25		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current Per Amplifier			6.6	7.4	mA
Power-Supply Rejection Ratio	±PSRR	−84	−93		dB

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
Supply Voltage	26.4V
Power Dissipation	See **Figure 1**
Common-Mode Input Voltage	V_{EE} − 0.5V to V_{CC} + 0.5V
Differential Input Voltage	1.8V
Temperature	
Storage Range	−65°C to +125°C
Operating Range	−40°C to +85°C
Lead (Soldering, 10sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Maximum Power Dissipation

The associated rise in junction temperature (T_J) on the die limits the maximum safe power dissipation in theMAX74831 package. The plastic encapsulating the die locally reaches the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the MAX74831. Exceeding a junction temperature of 175°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The still air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and total power dissipated in the package (P_D) determine the junction temperature of the die. Calculate the junction temperature by:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, then the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = Quiescent\ Power + (Total\ Drive\ Power - Load\ Power) \quad (2)$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L} \quad (3)$$

Consider the RMS output voltages. If R_L is referenced to V_S-, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$.

If the rms signal levels are indeterminate, then consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L} \quad (4)$$

In single-supply operation with R_L referenced to V_S-, worst case is $V_{OUT} = V_S/2$.

ABSOLUTE MAXIMUM RATINGS

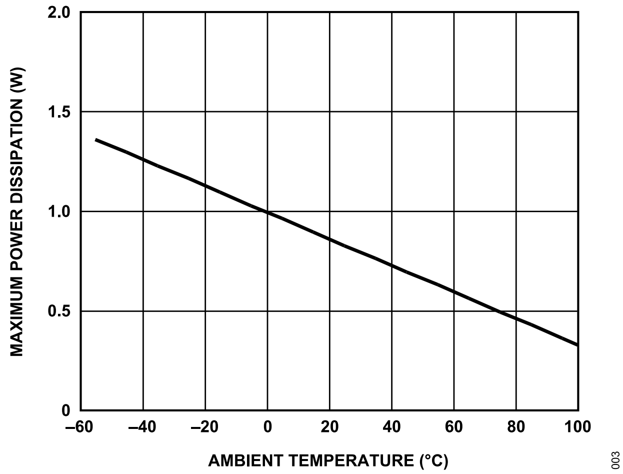

Figure 1. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduce the θ_{JA}.

Figure 1 shows the maximum safe power dissipation in the package vs. the ambient temperature for MSOP (150°C/W) package on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

Output Short-Circuit

Shorting the MAX74831 output to ground or drawing excessive current can cause catastrophic failure.

ESD Caution

	ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

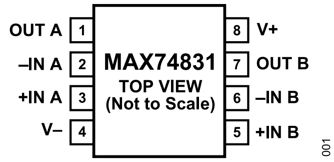

Figure 2. 8-Lead [MSOP]

Table 3. Pin Function Descriptions

PIN NUMBER	MNEMONIC	DESCRIPTION
1	OUT A	Output Channel A.
2	−IN A	Inverting Input Channel A.
3	+IN A	Noninverting Input Channel A.
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input Channel B.
6	−IN B	Inverting Input Channel B.
7	OUT B	Output Channel B.
8	V+	Positive Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

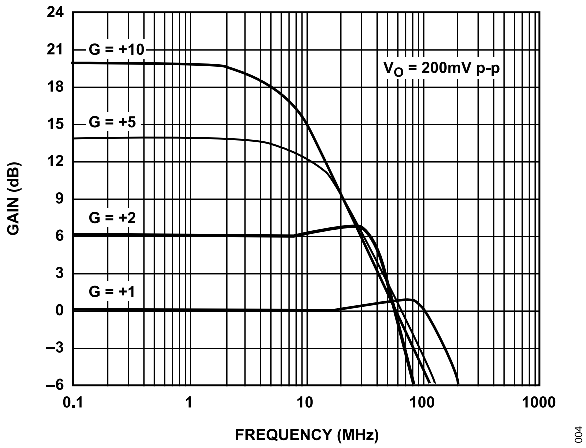

Figure 3. Small Signal Frequency Response for Various Gains

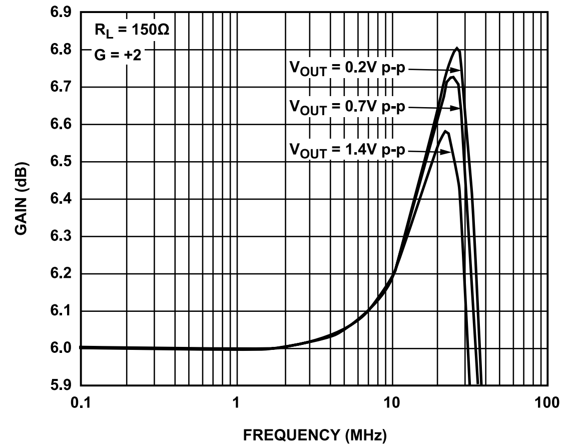

Figure 6. 0.1dB Flatness Frequency Response

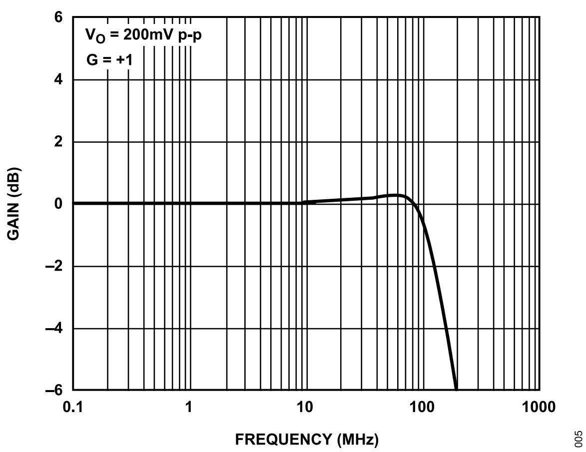

Figure 4. Small Signal Frequency Response

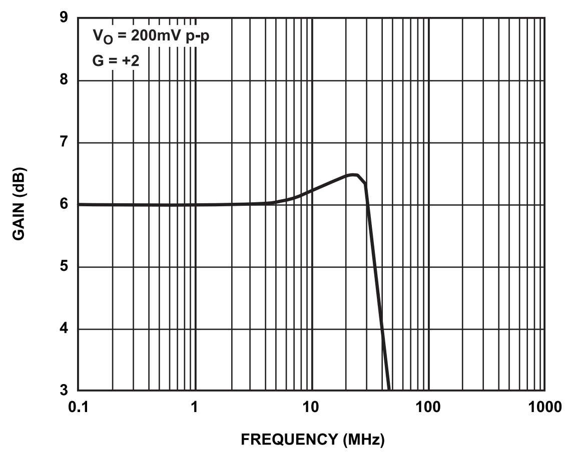

Figure 7. Small Signal Frequency Response

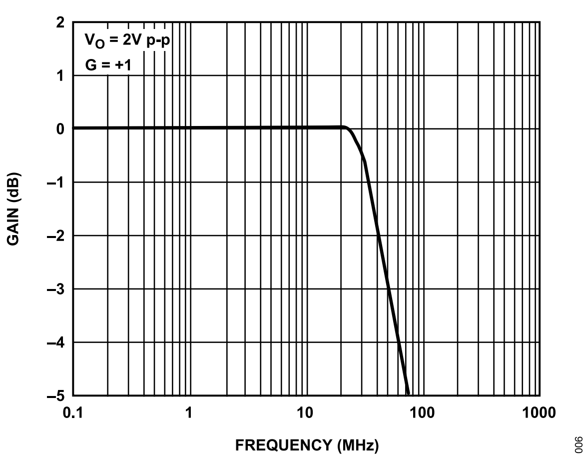

Figure 5. Large Signal Frequency Response

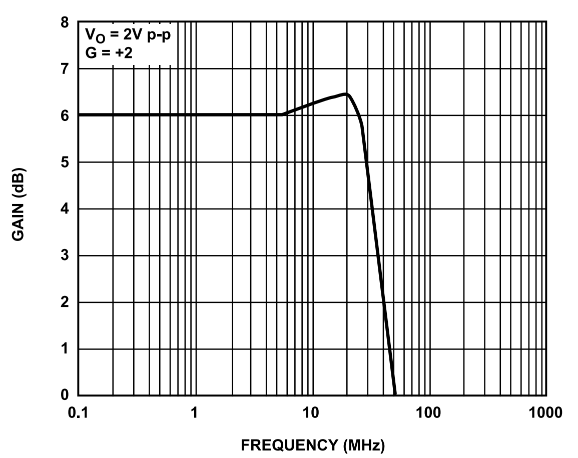

Figure 8. Large Signal Frequency Response

TYPICAL PERFORMANCE CHARACTERISTICS

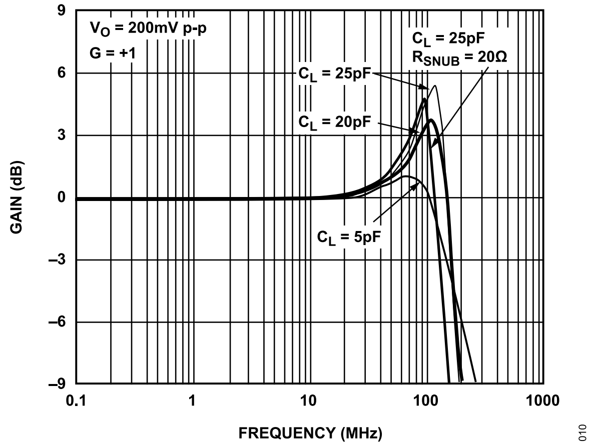

Figure 9. Small Signal Frequency Response for Various C_{LOAD}

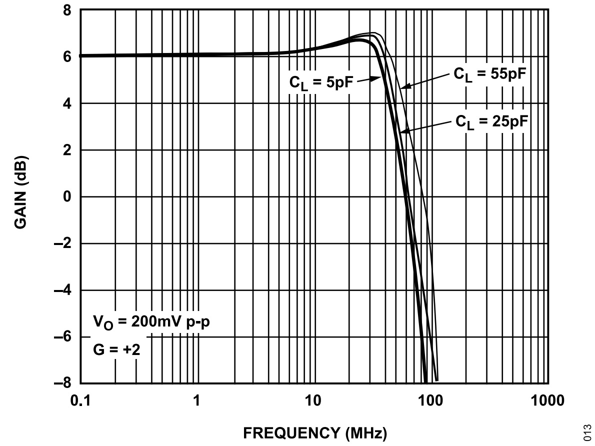

Figure 12. Small Signal Frequency Response for Various C_{LOAD}

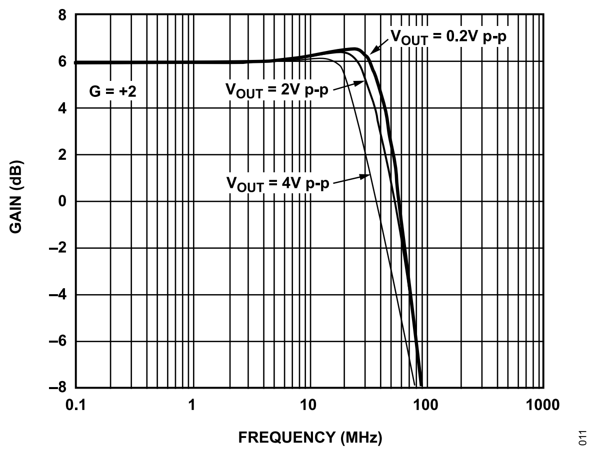

Figure 10. Frequency Response for Various Output Amplitudes

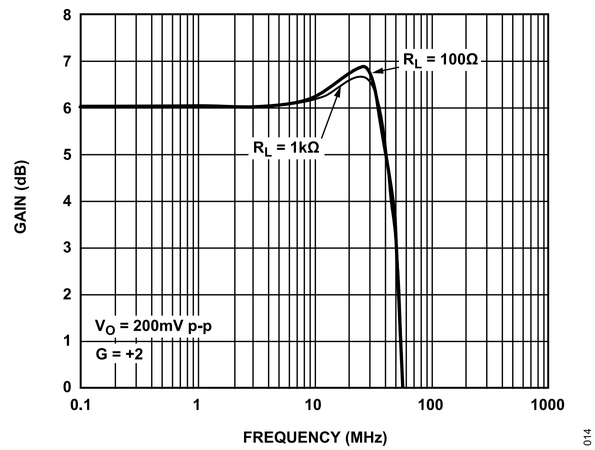

Figure 13. Small Signal Frequency Response for Various R_{LOAD}

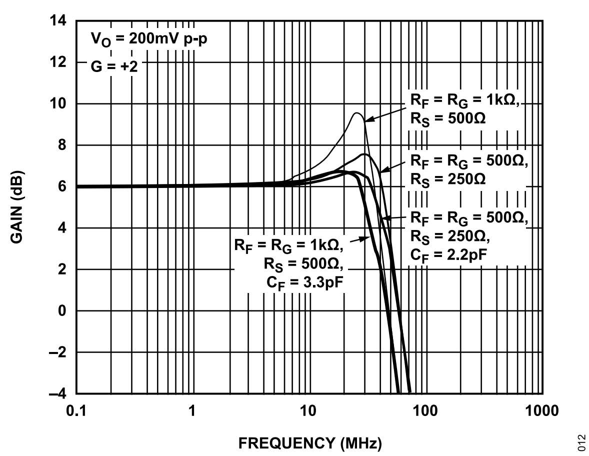

Figure 11. Small Signal Frequency Response for Various R_F/C_F

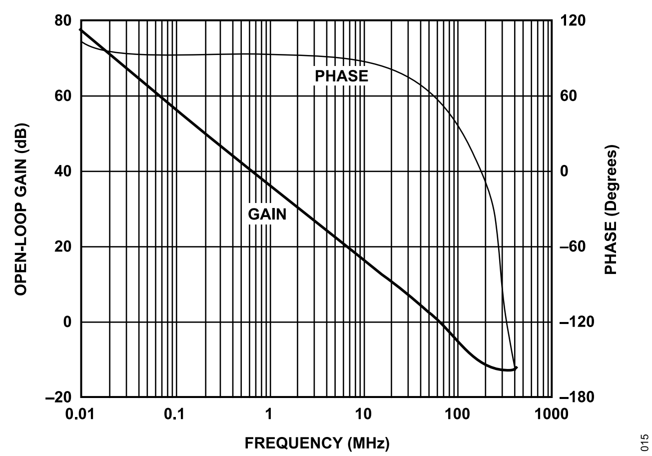

Figure 14. Open-Loop Response

TYPICAL PERFORMANCE CHARACTERISTICS

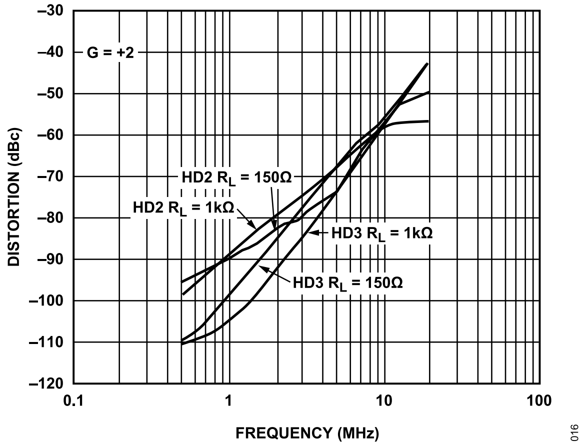

Figure 15. Harmonic Distortion vs. Frequency for Various Loads

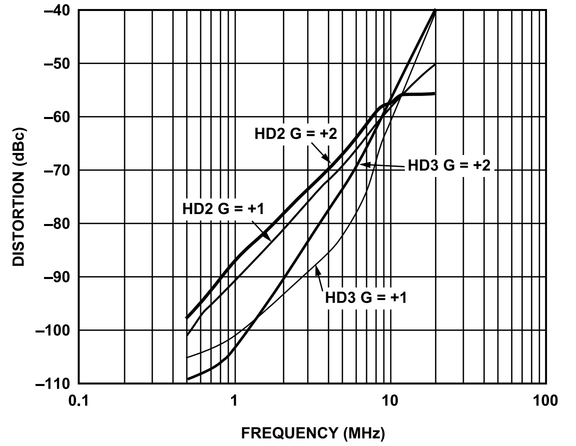

Figure 18. Harmonic Distortion vs. Frequency for Various Gains

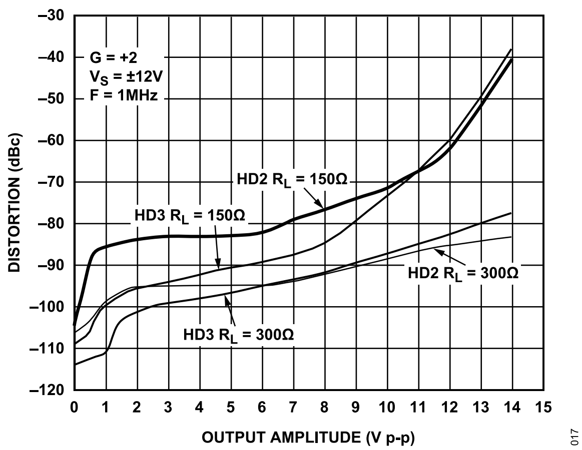

Figure 16. Harmonic Distortion vs. Amplitude for Various Loads V_S = ±12V

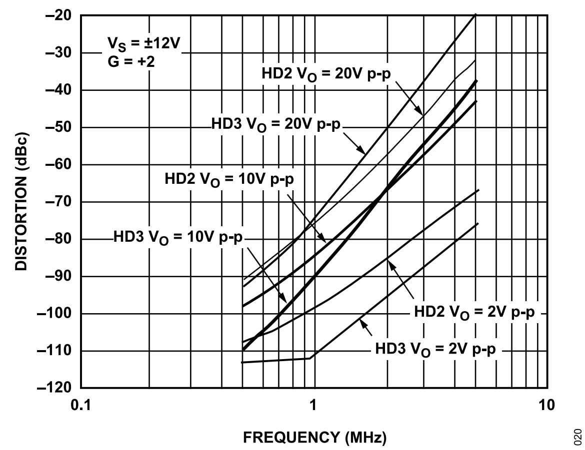

Figure 19. Harmonic Distortion vs. Frequency for Various Amplitudes

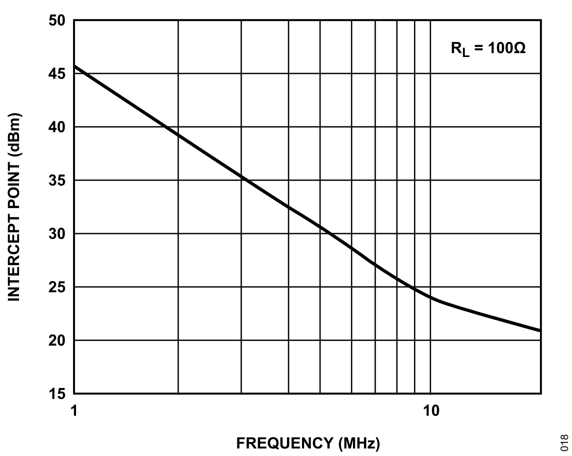

Figure 17. Third-Order Intercept vs. Frequency

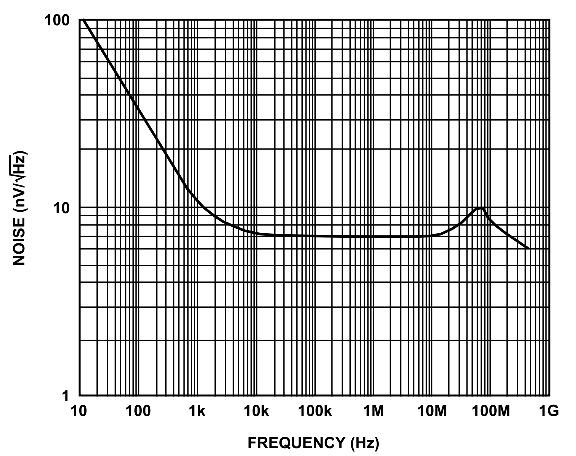

Figure 20. Voltage Noise

TYPICAL PERFORMANCE CHARACTERISTICS

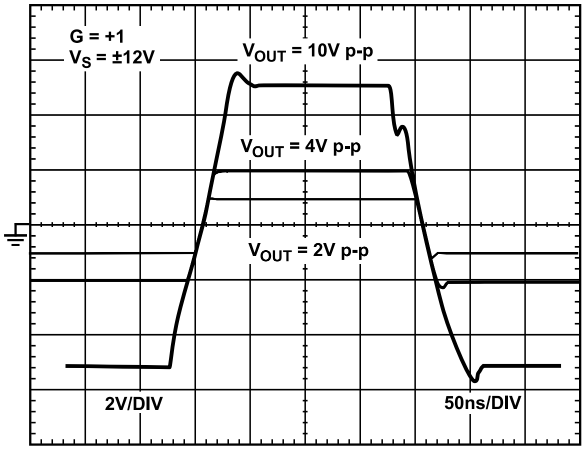

Figure 21. Large Signal Transient Response

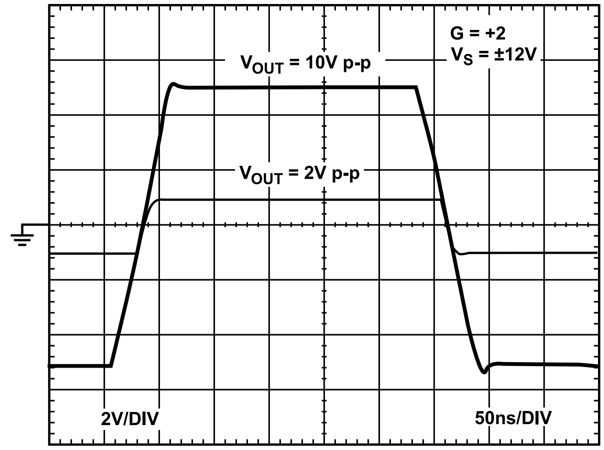

Figure 24. Large Signal Transient Response

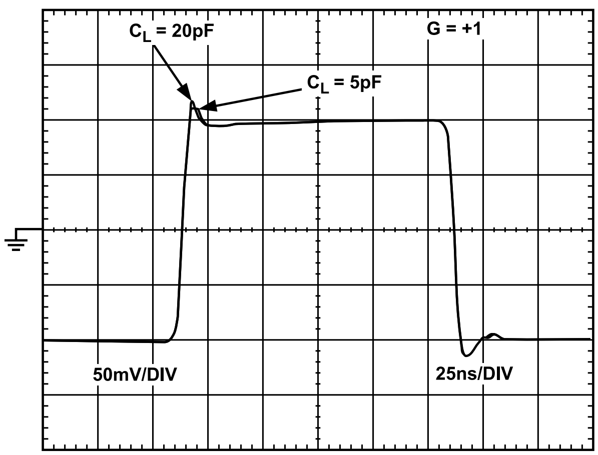

Figure 22. Small Signal Transient Response

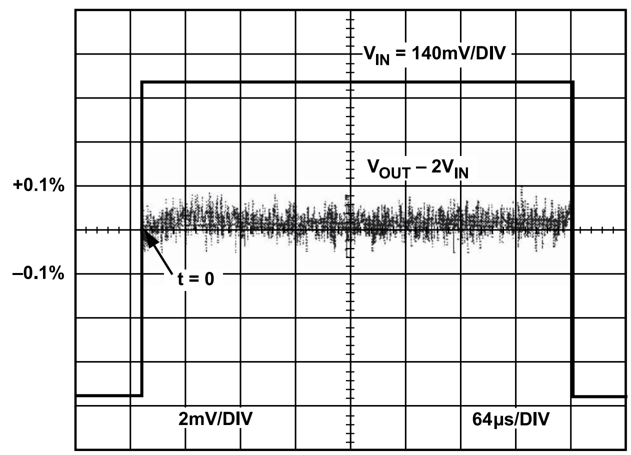

Figure 25. Long-Term Settling Time

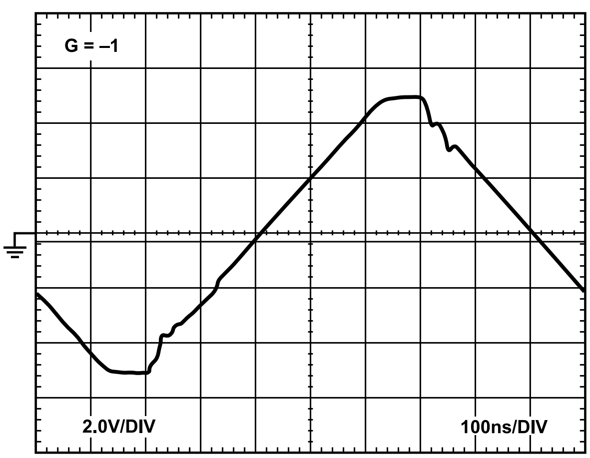

Figure 23. Output Overdrive Recovery

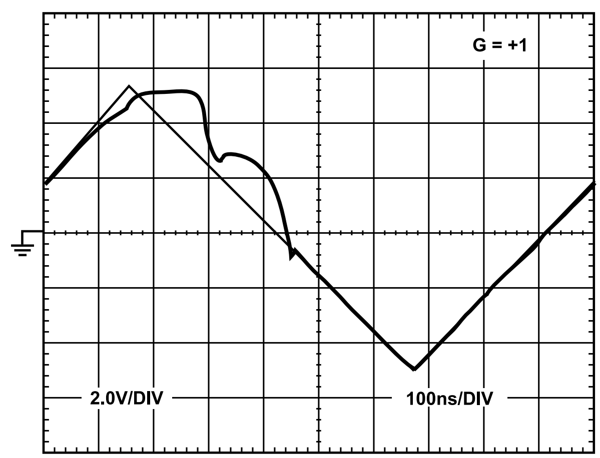

Figure 26. Input Overdrive Recovery

TYPICAL PERFORMANCE CHARACTERISTICS

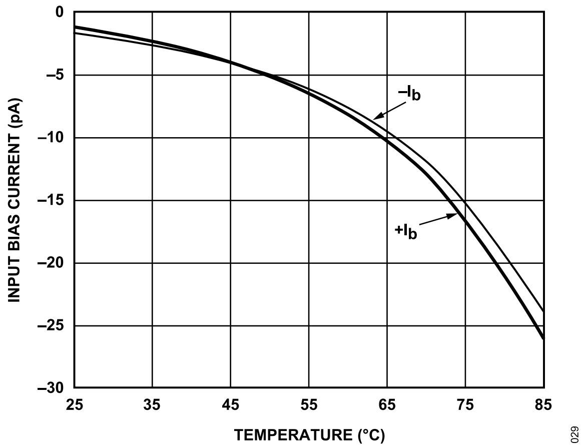

Figure 27. Input Bias Current vs. Temperature

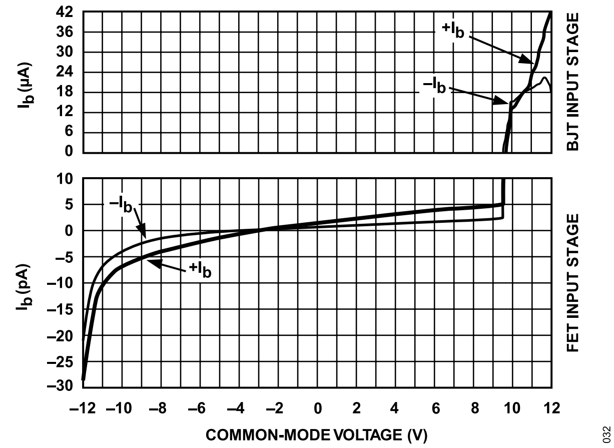

Figure 30. Input Bias Current vs. Common-Mode Voltage Range

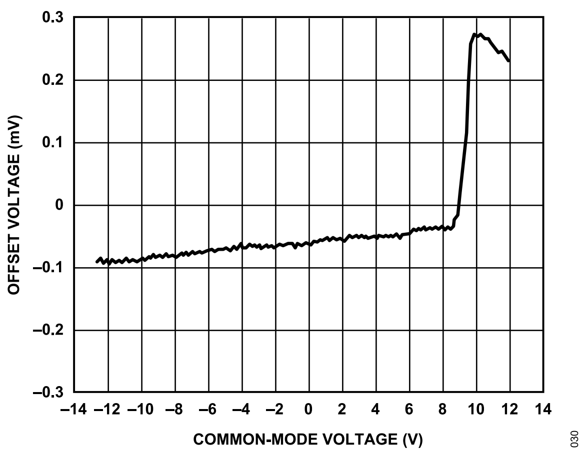

Figure 28. Input Offset Voltage vs. Common-Mode Voltage

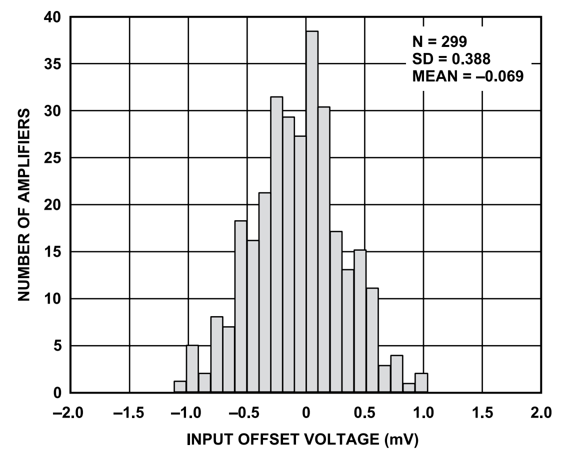

Figure 31. Input Offset Voltage

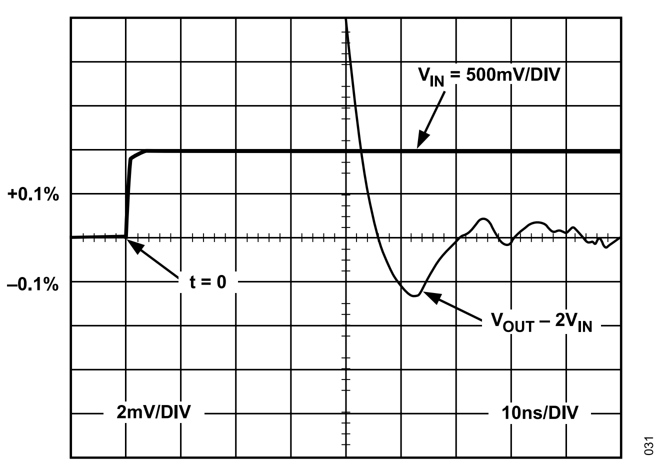

Figure 29. 0.1% Short-Term Settling Time

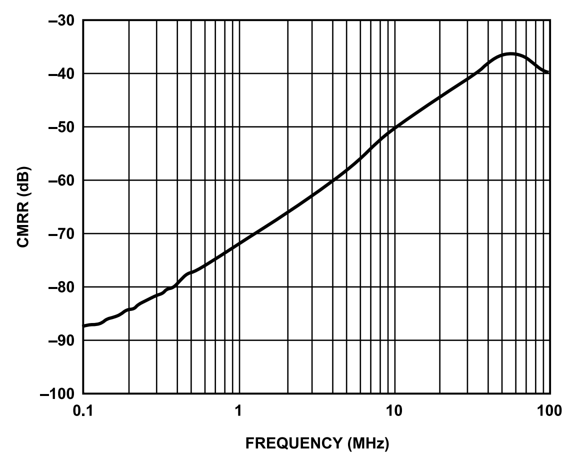

Figure 32. CMRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

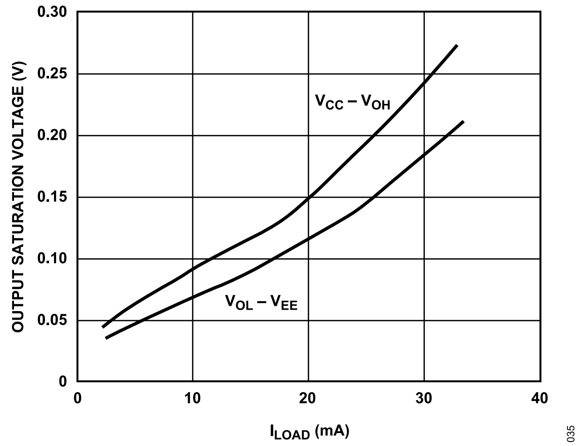

Figure 33. Output Saturation Voltage vs. Output Load Current

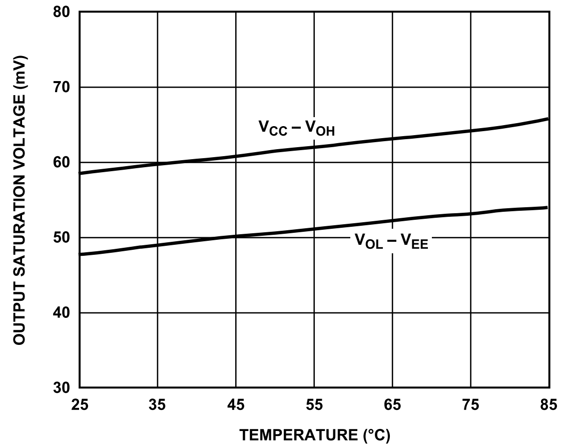

Figure 36. Output Saturation Voltage vs. Temperature

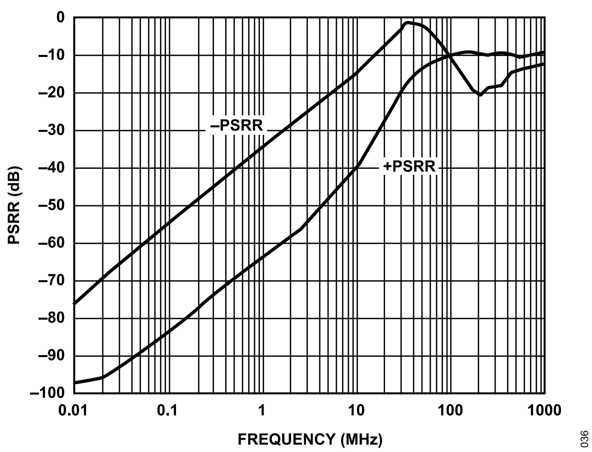

Figure 34. PSRR vs. Frequency

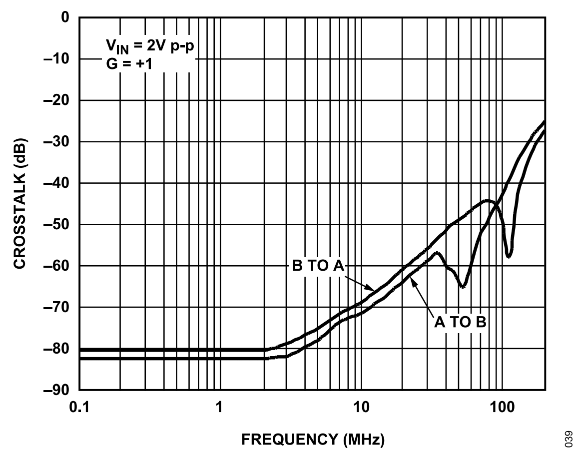

Figure 37. Crosstalk vs. Frequency

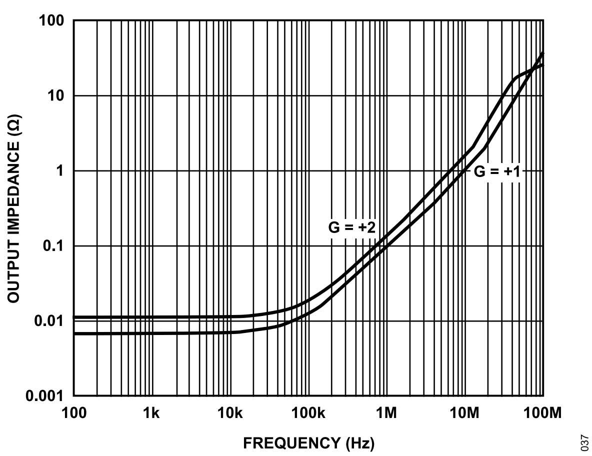

Figure 35. Output Impedance vs. Frequency

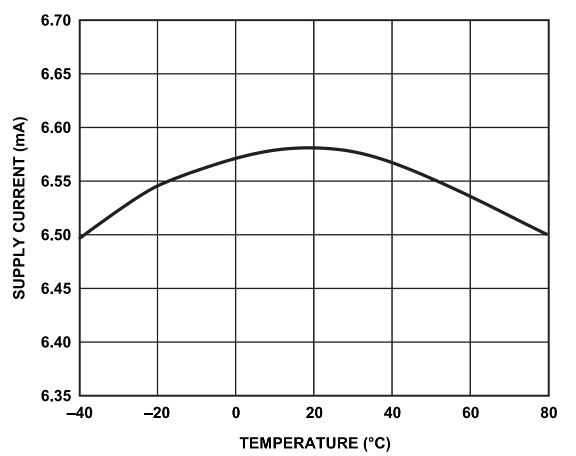

Figure 38. Quiescent Supply Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

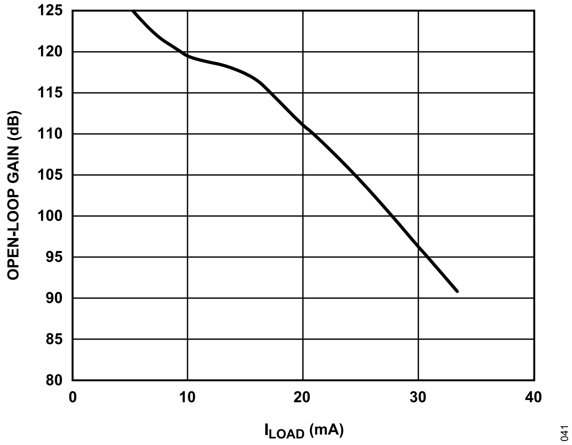

Figure 39. Open-Loop Gain vs. Load Current

THEORY OF OPERATION

The MAX74831 is a voltage feedback operational amplifier (op amp) that combine a laser-trimmed junction field effect transistor (JFET) input stage with the Analog Devices eXtra fast complementary bipolar (XFCB) process, resulting in an outstanding combination of precision and speed. The supply voltage range is from 5V to 24V. The amplifier features a patented rail-to-rail output stage capable of driving within 0.5V of either power supply while sourcing or sinking up to 30mA. Also featured is a single-supply input stage that handles common-mode signals from below the negative supply to within 3V of the positive rail. Operation beyond the JFET input range is possible because of an auxiliary bipolar input stage that functions with input voltages up to the positive supply. The amplifier operates as if it has a rail-to-rail input and exhibit no phase reversal behavior for common-mode voltages within the power supply.

With voltage noise of 7nV/√Hz and −100dBc distortion for 1MHz, 2V p-p signals, the MAX74831 is a great choice for high resolution data-acquisition systems. The low noise, sub-pA input current, precision offset, and high speed makes it superb preamp for fast photodiode applications. The speed and output drive capability of the MAX74831 also makes it useful in video applications.

Input Protection

Back-to-back diodes between the input terminals protect the inputs of the MAX74831 as well as ESD diodes to either power supply. This results in an input stage that draws picoamps of input current that can withstand up to 1500V ESD events human body model (HBM) with no degradation.

Excessive power dissipation through the protection devices destroys or degrades the performance of the amplifier. Differential voltages greater than 0.7V result in an input current of approximately $(|V_+ - V_-|\ 0.7V)/R_I$, where R_I is the resistance in series with the inputs.

For input voltages beyond the positive supply, the input current is approximately $(V_I - V_{CC} - 0.7V)/R_I$. Beyond the negative supply, the input current is about $(V_I - V_{EE} + 0.7V)/R_I$. Use an appropriately sized input resistor (R_I) to limit the input current to 30mA if the amplifier inputs experience sustained differential voltages greater than 0.7V or input voltages beyond the amplifier power supply, as shown in **Figure 40**.

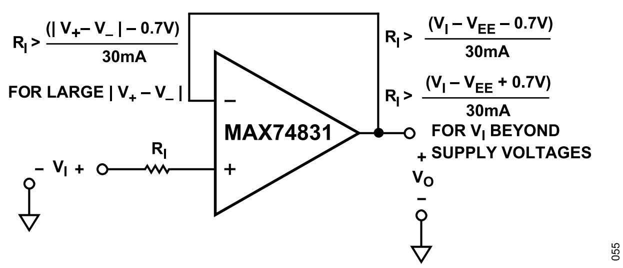

Figure 40. Current-Limiting Resistor

Input and Output Overload Behavior

Figure 41 shows a simplified schematic of the MAX74831 input stage. This includes the cascoded N-channel JFET input pair, the ESD and other protection diodes, and the auxiliary NPN input stage that eliminates any phase inversion behavior. Driving the common-mode input voltage to within approximately 3V of the positive power supply turns off the input JFET's bias current and turns on the NPN pair bias, which takes over control of the amplifier. The NPN differential pair now sets the amplifier's offset, and the input bias current is now in the range of several tens of microamps. **Figure 30** shows this behavior. Normal operation resumes when the common-mode voltage falls below 3V from the positive supply threshold.

The output transistors of the rail-to-rail output stage have circuitry to limit the extent of their saturation when the output is driven beyond its normal range. This helps output recovery time. **Figure 23** shows the output recovery from a 0.5V output overdrive on a ±5V supply.

THEORY OF OPERATION

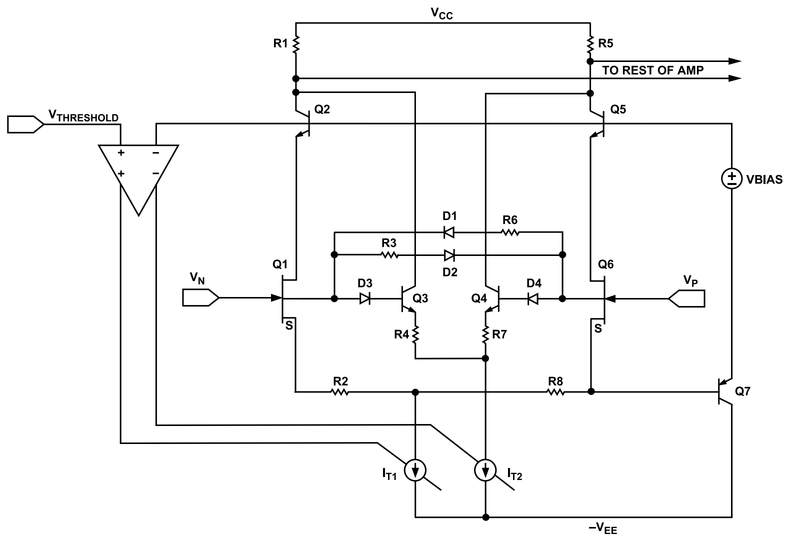

Figure 41. Simplified Input Stage

APPLICATIONS INFORMATION

Output Capacitance

To a lesser extent, parasitic capacitances on the output can cause peaking and ringing of the frequency response. There are two methods to effectively minimize their effect:

1. As shown in **Figure 42**, put a small value resistor (R_S) in series with the output to isolate the load capacitor from the amp's output stage. A good value to choose is 20Ω (see **Figure 9**).
2. Increase the phase margin with higher noise gains or add a pole with a parallel resistor and capacitor from −IN to the output.

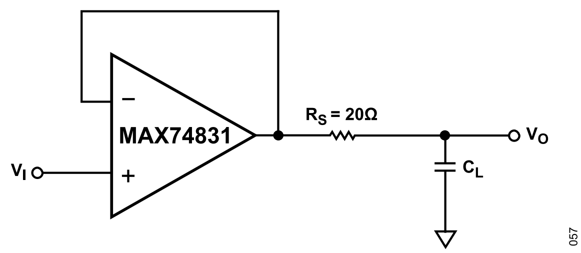

Figure 42. Output Isolation Resistor

OUTLINE DIMENSIONS

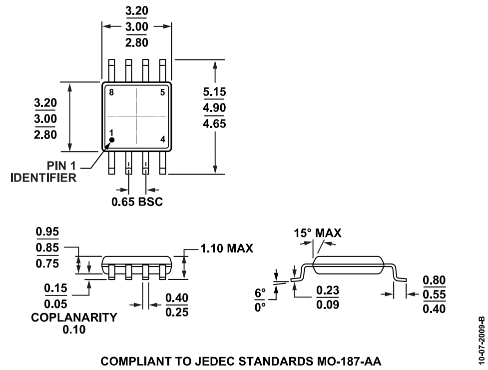

Figure 43. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

Updated: August 06, 2026

Ordering Guide

MODEL[1]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKING QUANTITY	PACKAGE OPTION	MARKING CODE
MAX74831ARMZ	−40°C to +85°C	8-Lead [MSOP]	Tube, 50	RM-8	A70
MAX74831ARMZ-R7	−40°C to +85°C	8-Lead [MSOP]	Reel7, 1000	RM-8	A70
MAX74831ARMZ-RL	−40°C to +85°C	8-Lead [MSOP]	Reel, 3000	RM-8	A70

1 Z = RoHS Compliant Part.