Data Sheet

MAX74810

50V, EMI Enhanced, Zero Drift, Ultralow Noise, Rail-to-Rail Output Operational Amplifiers

FEATURES

- Low offset voltage: 7µV maximum
- Extremely low offset voltage drift: 30nV/°C maximum
- Low voltage noise density: 5.8nV/√Hz typical
  - 117nV p-p typical from 0.1Hz to 10Hz
- Low input bias current: 50pA typical
- Gain-bandwidth product: 2.7MHz
- Single-supply operation: input voltage range includes ground and rail-to-rail output
- Wide range of operating voltages
  - Single-supply operation: 4.5V to 50V
  - Dual-supply operation: ±2.25V to ±25V
- Integrated EMI filters
- Unity-gain stable

APPLICATIONS

- Inductance, capacitance, and resistance (LCR) meter/megohmmeter front-end amplifiers
- Load cell and bridge transducers
- Magnetic force balance scales
- High precision shunt current sensing
- Thermocouple/resistance temperature detector (RTD) sensors
- Programmable logic controller (PLC) input and output amplifiers
- Automotive sensors
- Onboard chargers (OBC) and DC/DC converters
- Battery management systems (BMS)
- Traction inverter

GENERAL DESCRIPTION

The MAX74810 is a dual-channel, zero drift op amp with low noise and power, ground sensing inputs, and rail-to-rail output, optimized for total accuracy over time, temperature, and voltage conditions. The wide operating voltage and temperature ranges, as well as the high open-loop gain and very low DC and AC errors, make the devices suitable for amplifying very small input signals and for accurately reproducing larger signals in a wide variety of applications.

The MAX74810 performance is specified at 5.0V and 50V power supply voltages. These devices operate over the range of 4.5V to 50V, and are excellent for applications using single-ended supplies of 5V, 10V, 12V, and 30V, or for applications using higher single supplies and dual supplies of ±2.5V, ±5V, and ±15V. The MAX74810 uses on-chip filtering to achieve high immunity to electromagnetic interference (EMI).

The MAX74810 is fully specified over the extended industrial temperature range of −40°C to +125°C and is available in an 8-lead MSOP package.

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TABLE OF CONTENTS

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{SY} = 5.0V, V_{CM} = V_{SY}/2V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	Test Conditions/Comments	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = V_{SY}/2		0.7	7	µV
Offset Voltage Drift	TCV_{OS}			2.5		nV/°C
Input Bias Current	I_B			50		pA
		−40°C ≤ T_A ≤ +125°C		2		nA
Input Offset Current	I_{OS}			80		pA
Input Voltage Range	IVR		0		3.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0V to 3.5V		155		dB
Large Signal Voltage Gain	A_V	R_L = 10kΩ, V_{OUT} = 0.5V to 4.5V		145		dB
Input Resistance Differential Mode	R_{INDM}			30		kΩ
Input Resistance Common Mode	R_{INCM}			100		GΩ
Input Capacitance Differential Mode	C_{INDM}			7		pF
Input Capacitance Common Mode	C_{INCM}			35		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10kΩ to V_{SY}/2		4.98		V
Output Voltage Low	V_{OL}	R_L = 10kΩ to V_{SY}/2		20		mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1V		14		mA
Short-Circuit Current Source	I_{SC+}			22		mA
Short-Circuit Current Sink	I_{SC-}			29		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1MHz, A_V = 1		4		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 4.5V to 50V		160		dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0mA		830	900	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR+	R_L = 10kΩ, C_L = 50pF, A_V = 1		1.4		V/µs
	SR−	R_L = 10kΩ, C_L = 50pF, A_V = 1		1.3		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 10mV p-p, R_L = 10kΩ, C_L = 50pF, A_V = 100		2.7		MHz
Phase Margin	Φ_M	V_{IN} = 10mV p-p, R_L = 10kΩ, C_L = 50pF, A_V = 1		64		Degrees

(V_{SY} = 5.0V, V_{CM} = V_{SY}/2V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	Test Conditions/Comments	MIN	TYP	MAX	UNITS
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 10kΩ, C_L = 50pF, A_V = 1		4		µs
Channel Separation	CS	V_{IN} = 1V p-p, f = 10kHz, R_L = 10kΩ, C_L = 50pF		98		dB
EMI Rejection Ratio of +IN/+IN x	EMIRR	V_{IN} = 100mV peak, f = 400MHz		72		dB
		V_{IN} = 100mV peak, f = 900MHz		80		dB
		V_{IN} = 100mV peak, f = 1800MHz		83		dB
		V_{IN} = 100mV peak, f = 2400MHz		85		dB
NOISE PERFORMANCE						
Total Harmonic Distortion Plus Noise BW = 80kHz	THD + N	A_V = 1, f = 1kHz, V_{IN} = 0.6V rms		0.001		%
Peak-to-Peak Voltage Noise	$e_{N\ p-p}$	A_V = 100, f = 0.1Hz to 10Hz		117		nV p-p
Voltage Noise Density	e_N	A_V = 100, f = 1kHz		5.8		nV/√Hz
Peak-to-Peak Current Noise	$i_{N\ p-p}$	A_V = 100, f = 0.1Hz to 10Hz		16		pA p-p
Current Noise Density	i_N	A_V = 100, f = 1kHz		0.8		pA/√Hz

Table 2. Electrical Characteristics

(V_{SY} = 50V, V_{CM} = V_{SY}/2V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	Test Conditions/Comments	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = V_{SY}/2		1.5	7	µV
		−40°C ≤ T_A ≤ +125°C			10	µV
Offset Voltage Drift	TCV_{OS}			6	30	nV/°C
Input Bias Current	I_B			50	200	pA
		−40°C ≤ T_A ≤ +125°C		4.5		nA
Input Offset Current	I_{OS}			80	500	pA
Input Voltage Range	IVR		0		48.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0V to 48.5V	140	144		dB
		−40°C ≤ T_A ≤ +125°C		135		dB
Large Signal Voltage Gain	A_V	R_L = 10kΩ V_{OUT} = 0.5V to 49.5V	135	137		dB
Input Resistance Differential Mode	R_{INDM}			30		kΩ
Input Resistance Common Mode	R_{INCM}			1000		GΩ
Input Capacitance Differential Mode	C_{INDM}			7		pF
Input Capacitance Common Mode	C_{INCM}			35		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10kΩ to V_{SY}/2	49.75	49.8		V
Output Voltage Low	V_{OL}	R_L = 10kΩ to V_{SY}/2		200	250	mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1V		14		mA
Short-Circuit Current Source	I_{SC+}			21		mA
Short-Circuit Current Sink	I_{SC-}			32		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1MHz, A_V = 1		4		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 4.5V to 50V	150	160		dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0mA		830	1100	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR+	R_L = 10kΩ, C_L = 50pF, A_V = 1		1.7		V/µs
	SR−	R_L = 10kΩ, C_L = 50pF, A_V = 1		0.8		V/µs

(V_{SY} = 50V, V_{CM} = V_{SY}/2V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	Test Conditions/Comments	MIN	TYP	MAX	UNITS
Gain Bandwidth Product	GBP	V_{IN} = 10mV p-p, R_L = 10kΩ, CL = 50pF, A_V = 100		2.7		MHz
Phase Margin	Φ_M	V_{IN} = 10mV p-p, R_L = 10kΩ, C_L = 50pF, A_V = 1		64		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 10V step, R_L = 10kΩ, C_L = 50pF, A_V = 1		12		µs
Channel Separation	CS	V_{IN} = 10V p-p, f = 10kHz, R_L = 10kΩ, C_L = 50pF		98		dB
EMI Rejection Ratio of +IN/+IN x	EMIRR	V_{IN} = 100mV peak, f = 400MHz		72		dB
		V_{IN} = 100mV peak, f = 900MHz		80		dB
		V_{IN} = 100mV peak, f = 1800MHz		83		dB
		V_{IN} = 100mV peak, f = 2400MHz		85		dB
NOISE PERFORMANCE						
Total Harmonic Distortion Plus Noise BW = 80kHz	THD + N	A_V = 1, f = 1kHz, V_{IN} = 10V rms		0.0007		%
Peak-to-Peak Voltage Noise	$e_{N\,p-p}$	A_V = 100, f = 0.1Hz to 10Hz		117		nV p-p
Voltage Noise Density	e_N	A_V = 100, f = 1kHz		5.8		nV/√Hz
Peak-to-Peak Current Noise	$i_{N\,p-p}$	A_V = 100, f = 0.1Hz to 10Hz		16		pA p-p
Current Noise Density	i_N	A_V = 100, f = 1kHz		0.8		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 3. Absolute Maximum Ratings

PARAMETER	RATING
Supply Voltage	57V
Input Voltage	(V−) – 0.3V to (V+) + 0.3V
Input Current[1]	±10mA
Input Current (duration < 1 sec)	±100mA
Differential Input Voltage	±5V
Output Short-Circuit Duration to Ground	Indefinite
Temperature Range Storage	−65°C to +150°C
Temperature Range Operating	−40°C to +125°C
Temperature Range Junction	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

1 The input pins have clamp diodes to the power supply pins. Limit the input current to ±10mA or less whenever input signals exceed the power supply rail by 300mV.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages using a standard 4-layer JEDEC board.

Table 4. Thermal Resistance

PACKAGE TYPE	θ_{JA}	θ_{JC}	UNIT
RM-8	194	38	°C/W

Power Sequencing

Apply the op amp supplies simultaneously; if this is not possible, apply the positive power supply first, before the negative power supply.

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

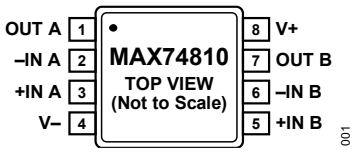

Figure 1. MAX74810 Pin Configuration

Pin Descriptions

Table 5. MAX74810 Pin Function Descriptions

PIN	NAME	DESCRIPTION
1	OUT A	Output, Channel A
2	−IN A	Inverting Input, Channel A
3	+IN A	Noninverting Input, Channel A
4	V−	Negative Supply Voltage
5	+IN B	Noninverting Input, Channel B
6	−IN B	Inverting Input, Channel B
7	OUT B	Output, Channel B
8	V+	Positive Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

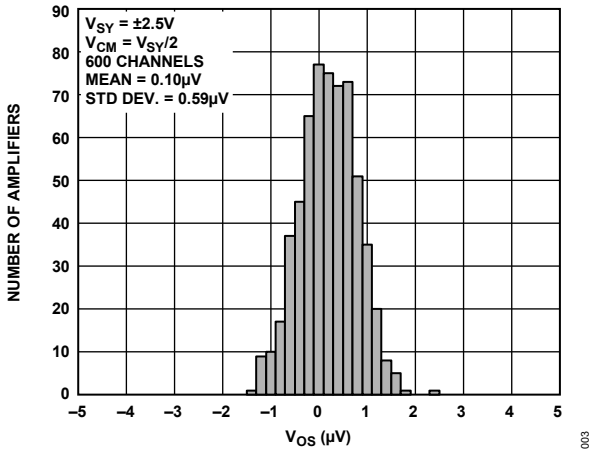

Figure 2. Input Offset Voltage Distribution, V_{SY} = ±2.5V

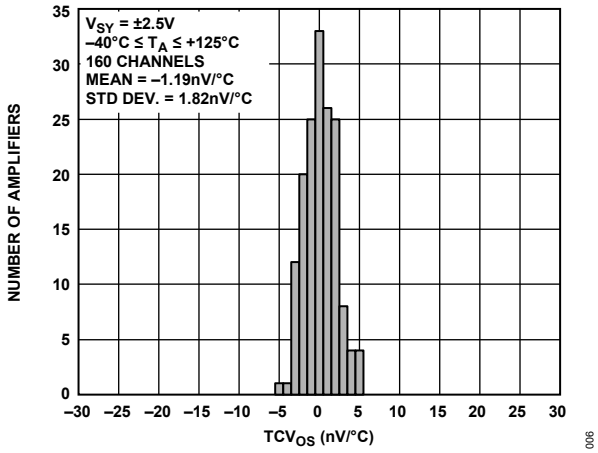

Figure 3. Input Offset Voltage Drift Distribution, V_{SY} = ±2.5V

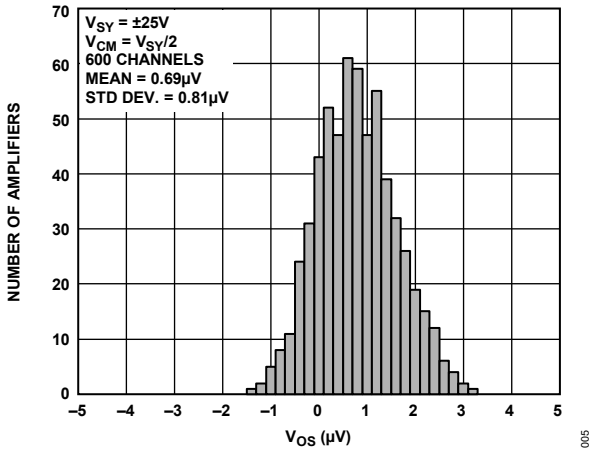

Figure 4. Input Offset Voltage Distribution, V_{SY} = ±25V

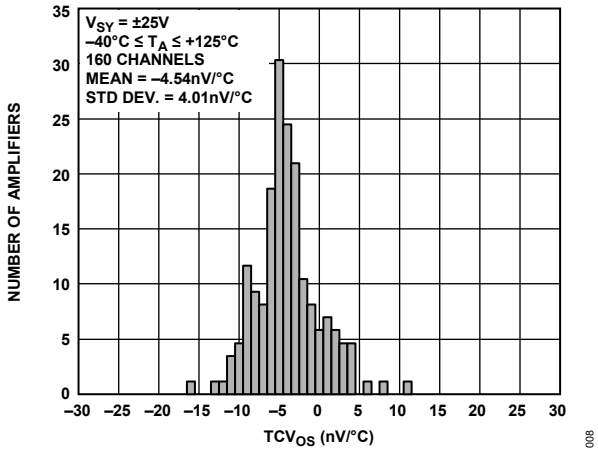

Figure 5. Input Offset Voltage Drift Distribution, V_{SY} = ±25V

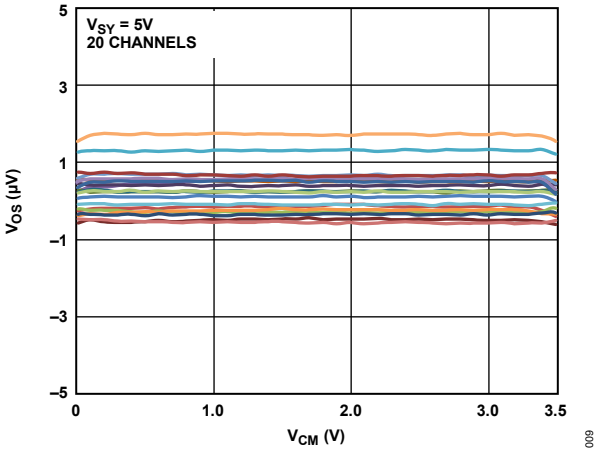

Figure 6. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 5V

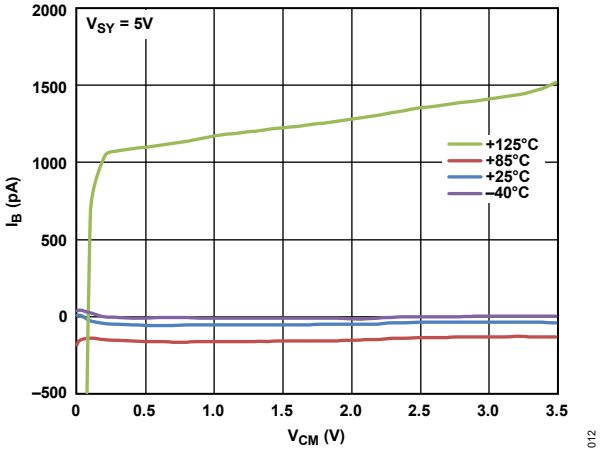

Figure 7. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 5V

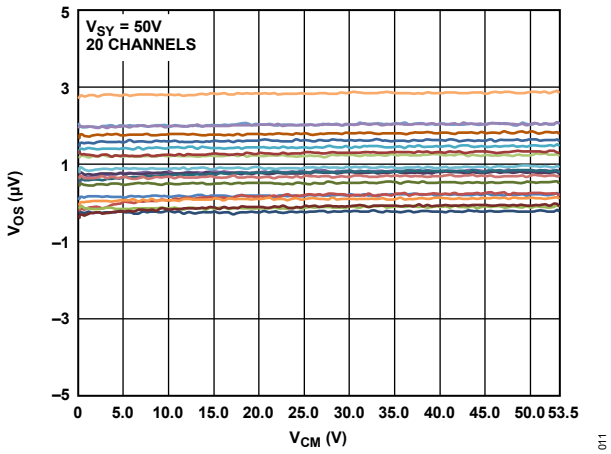

Figure 8. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 50V

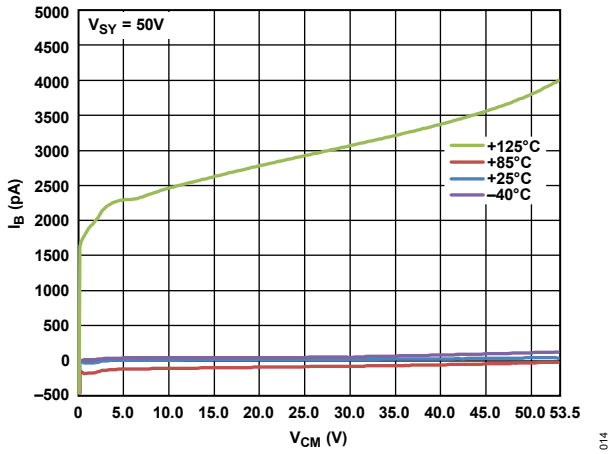

Figure 9. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 50V

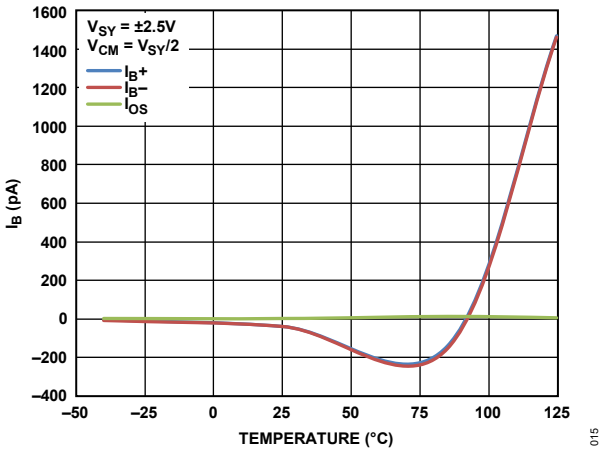

Figure 10. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±2.5V

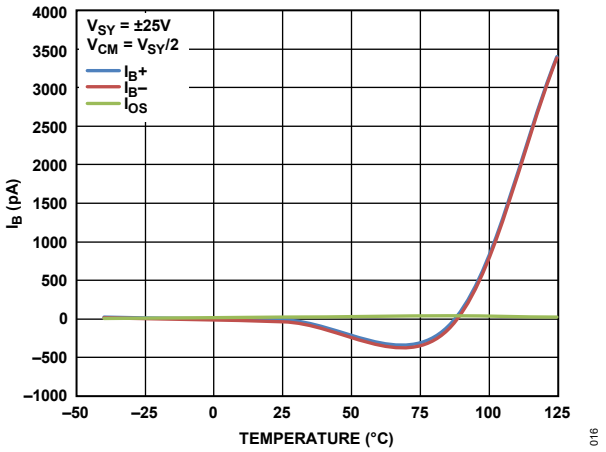

Figure 11. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±25V

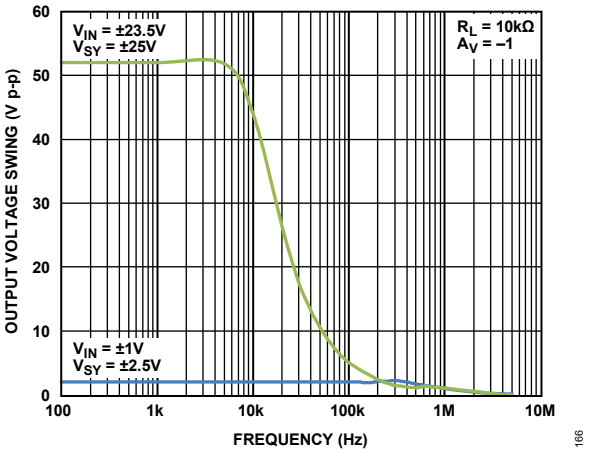

Figure 12. Output Voltage Swing vs. Frequency

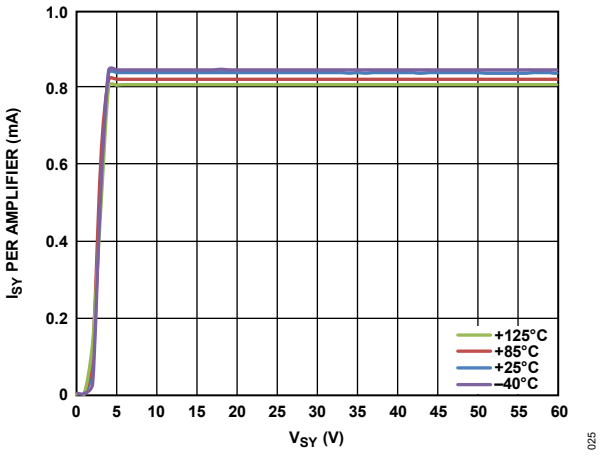

Figure 13. Supply Current (I_{SY}) per Amplifier vs. Supply Voltage (V_{SY})

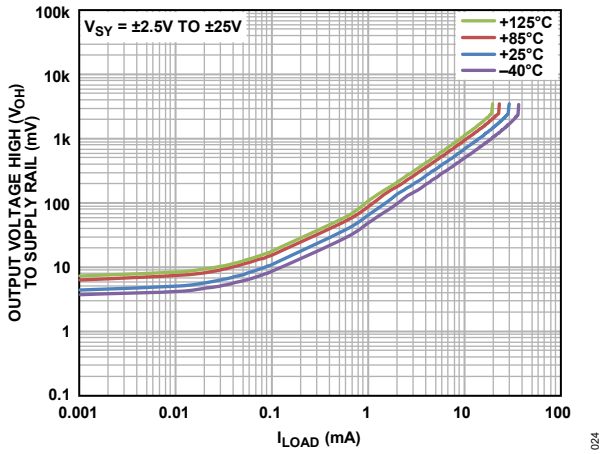

Figure 14. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD})

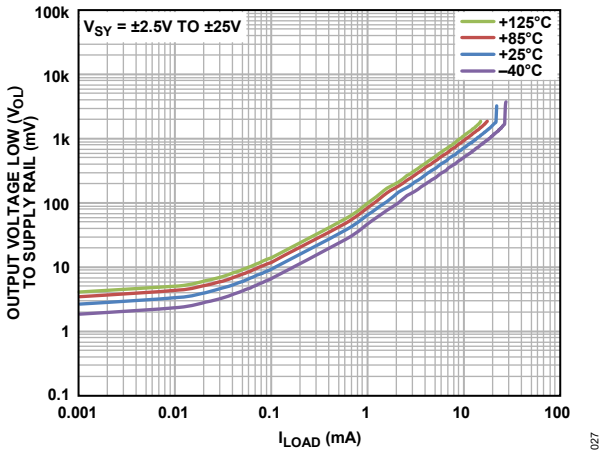

Figure 15. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD})

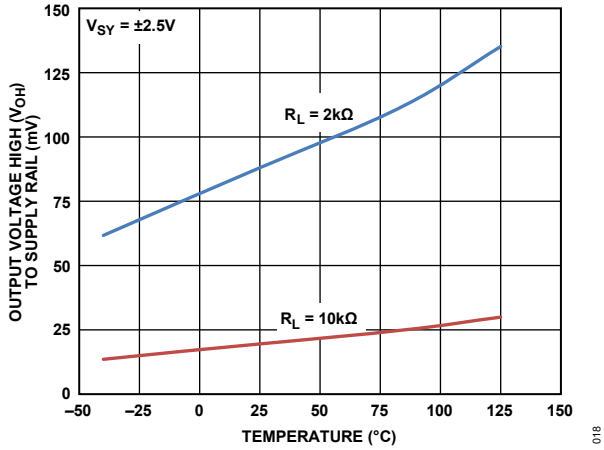

Figure 16. Output Voltage High (V_{OH}) to Supply Rail vs. Temperature, V_{SY} = ±2.5V

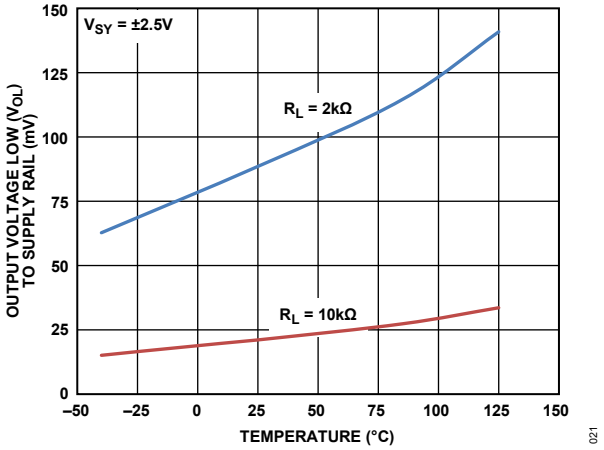

Figure 17. Output Voltage Low (V_{OL}) to Supply Rail vs. Temperature, V_{SY} = ±2.5V

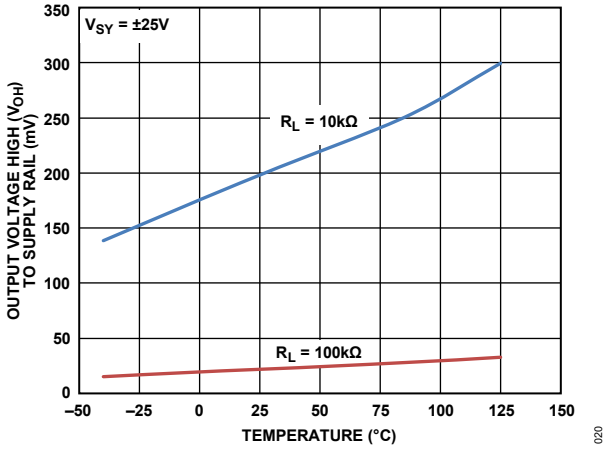

Figure 18. Output Voltage High (V_{OH}) to Supply Rail vs. Temperature, V_{SY} = ±25V

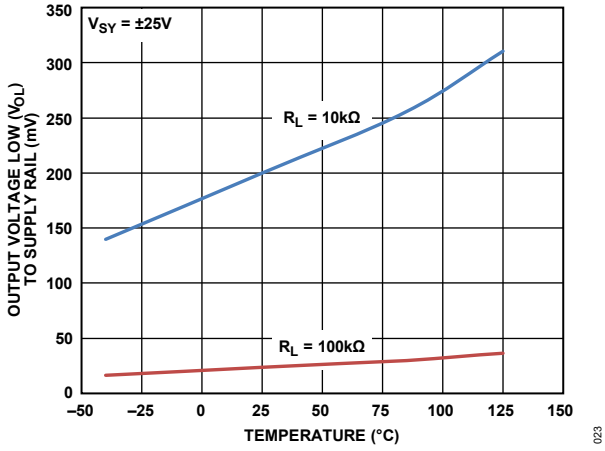

Figure 19. Output Voltage Low (V_{OL}) to Supply Rail vs. Temperature, V_{SY} = ±25V

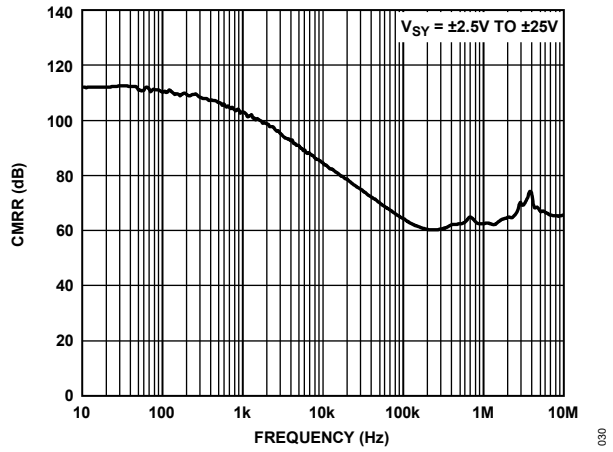

Figure 20. CMRR vs. Frequency

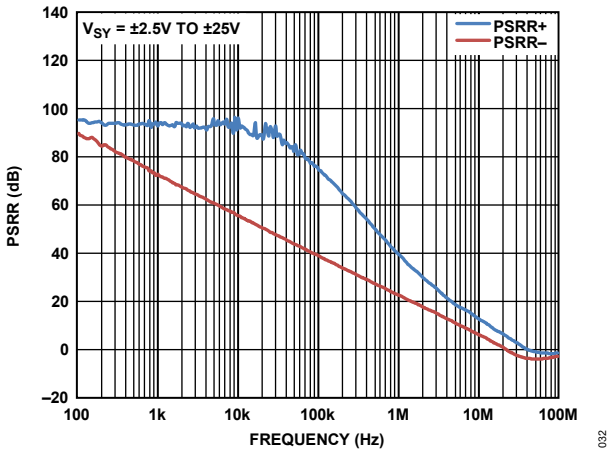

Figure 21. PSRR vs. Frequency

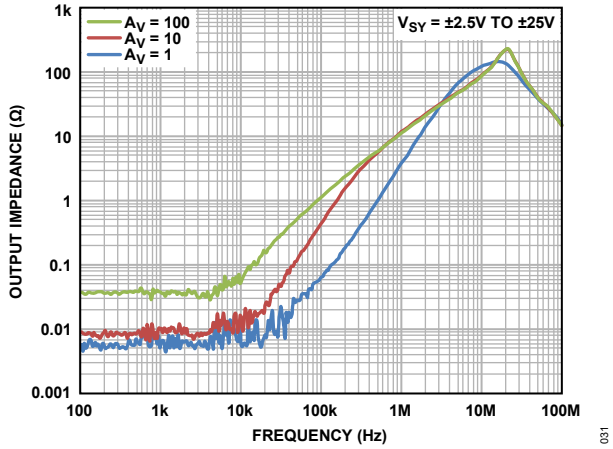

Figure 22. Closed-Loop Output Impedance vs. Frequency

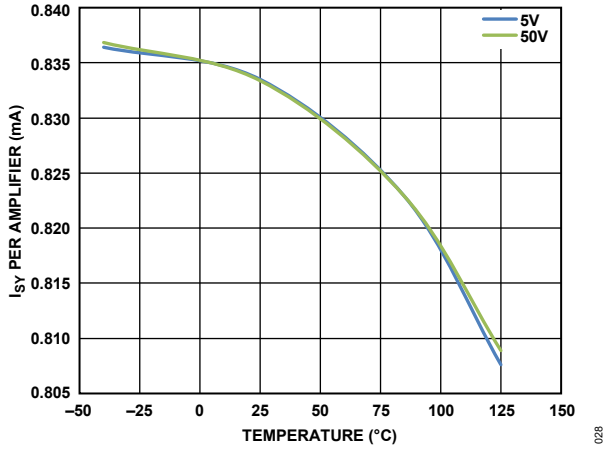

Figure 23. Supply Current (I_{SY}) per Amplifier vs. Temperature

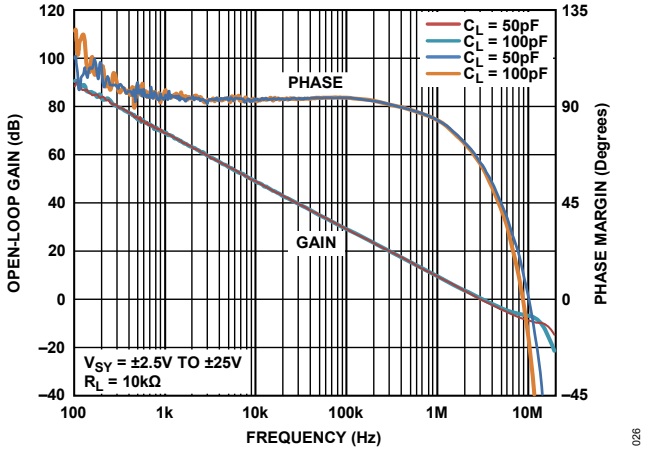

Figure 24. Open-Loop Gain and Phase Margin vs. Frequency

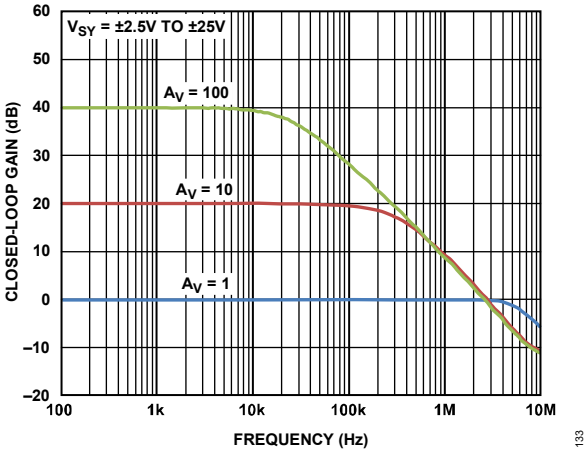

Figure 25. Closed-Loop Gain vs. Frequency

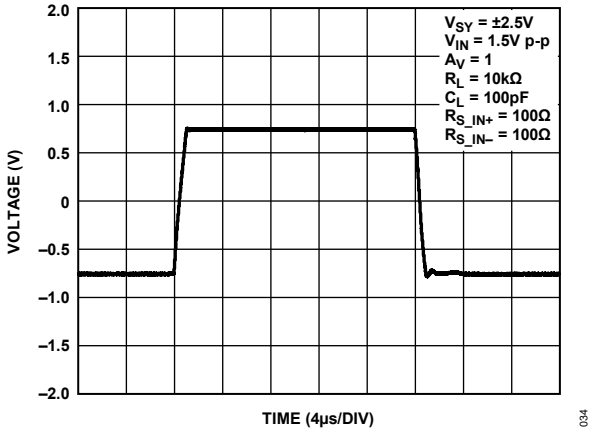

Figure 26. Large Signal Transient Response, V_{SY} = ±2.5V

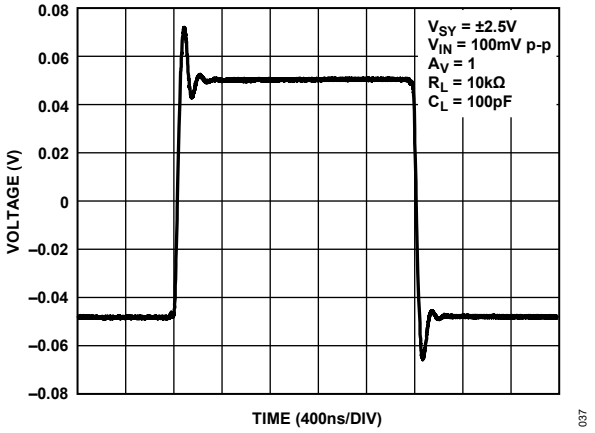

Figure 27. Small Signal Transient Response, V_{SY} = ±2.5V

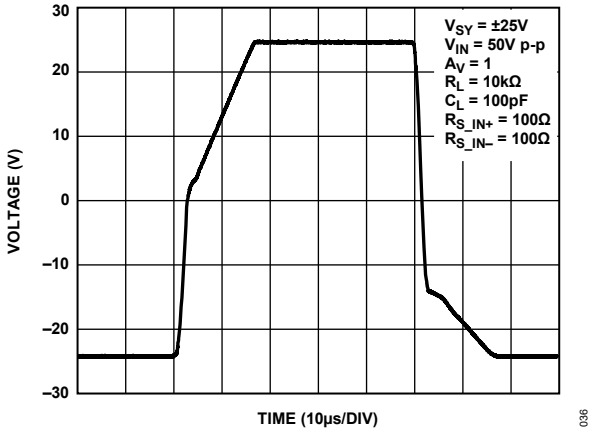

Figure 28. Large Signal Transient Response, V_{SY} = ±25V

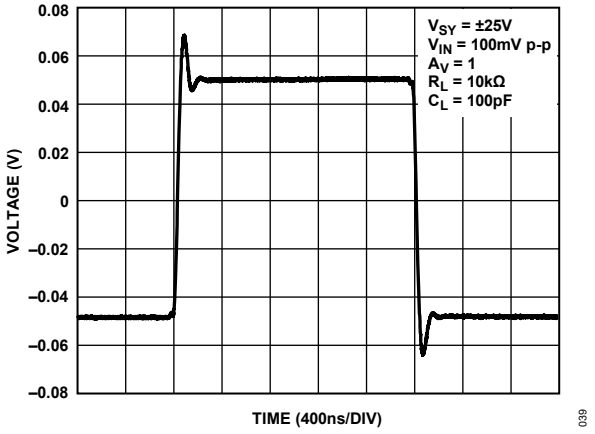

Figure 29. Small Signal Transient Response, V_{SY} = ±25V

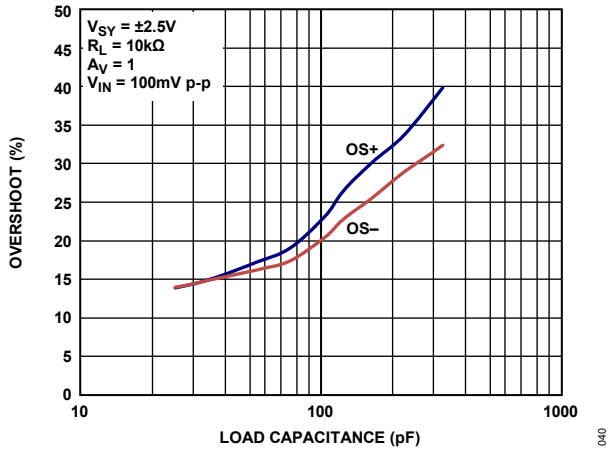

Figure 30. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±2.5V

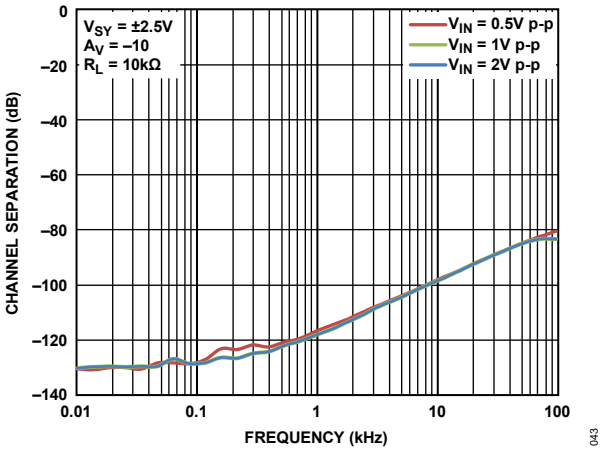

Figure 31. Channel Separation vs. Frequency, V_{SY} = ±2.5V

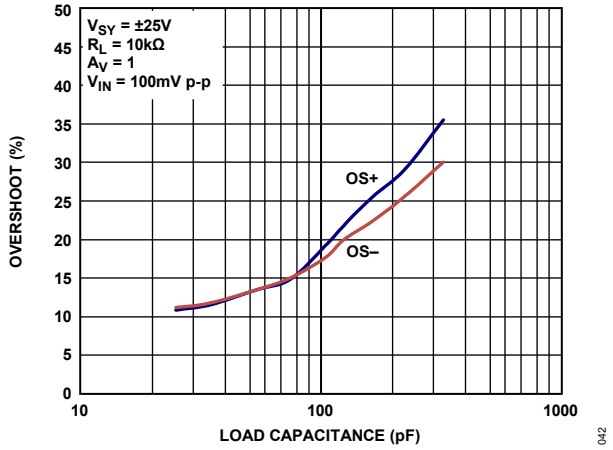

Figure 32. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±25V

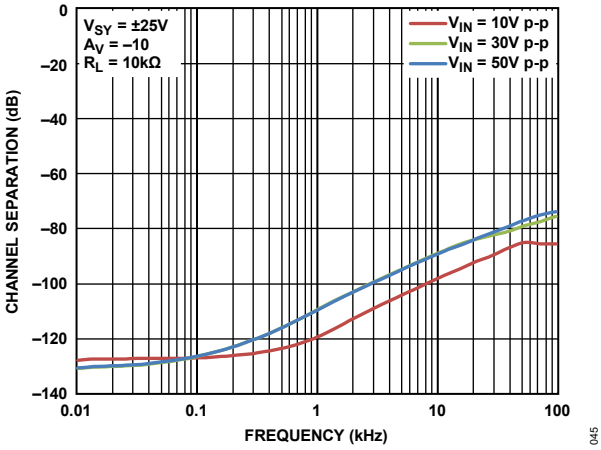

Figure 33. Channel Separation vs. Frequency, V_{SY} = ±25V

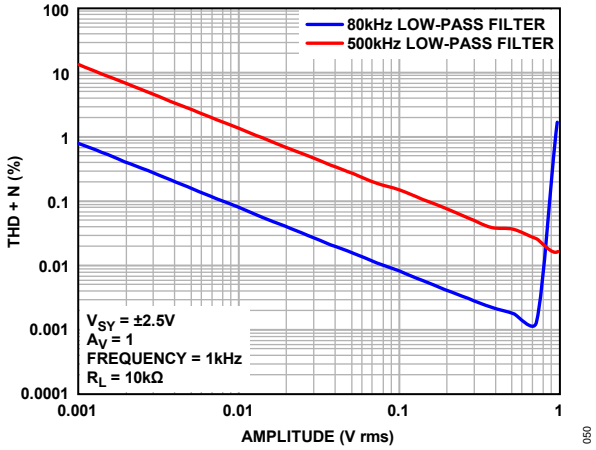

Figure 34. THD + N vs. Amplitude, V_{SY} = ±2.5V

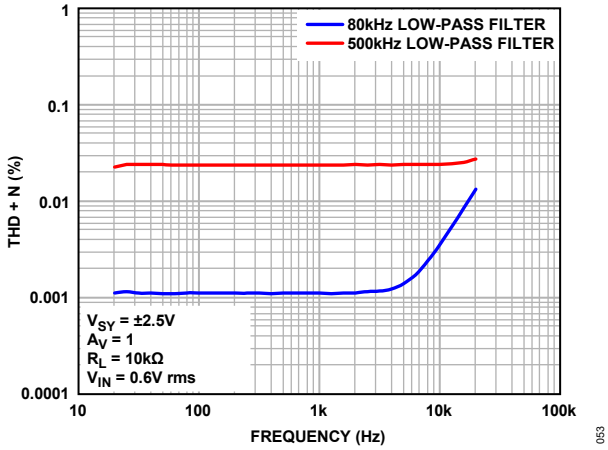

Figure 35. THD + N vs. Frequency, V_{SY} = ±2.5V

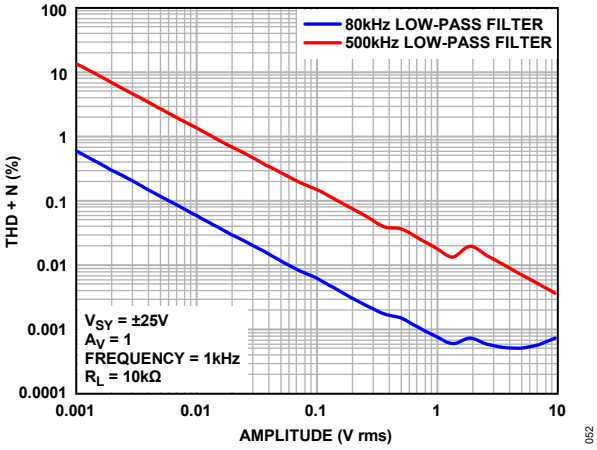

Figure 36. THD + N vs. Amplitude, V_{SY} = ±25V

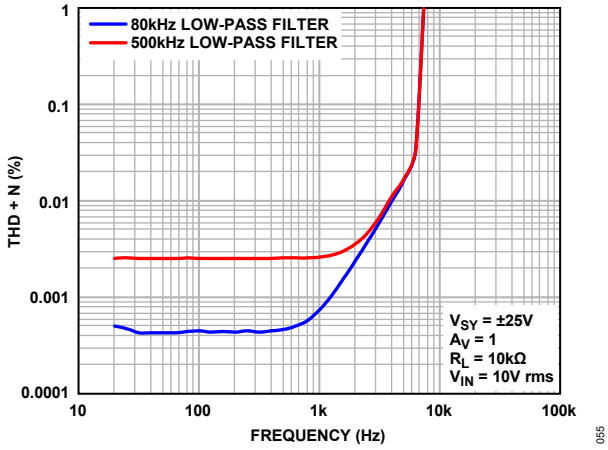

Figure 37. THD + N vs. Frequency, V_{SY} = ±25V

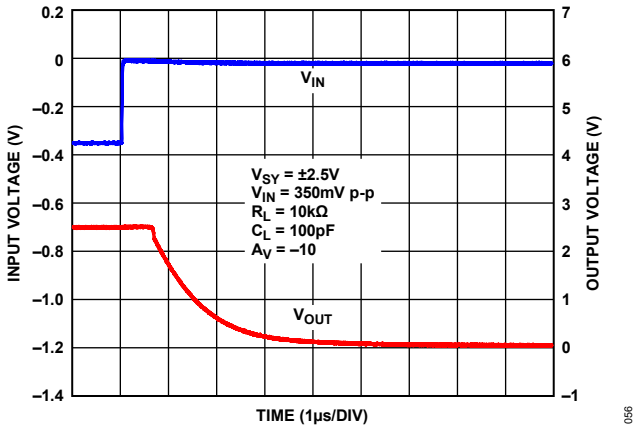

Figure 38. Positive Overload Recovery, V_{SY} = ±2.5V

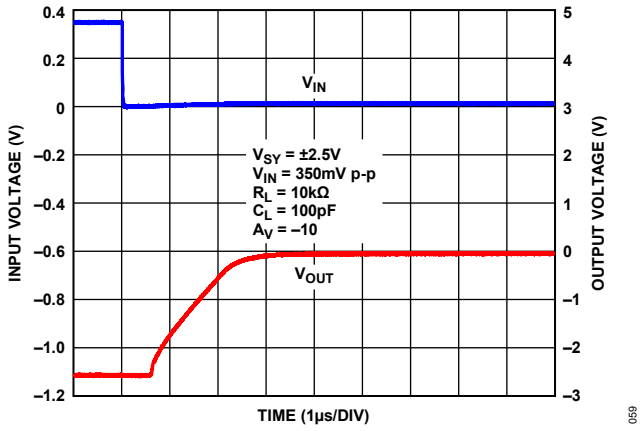

Figure 39. Negative Overload Recovery, V_{SY} = ±2.5V

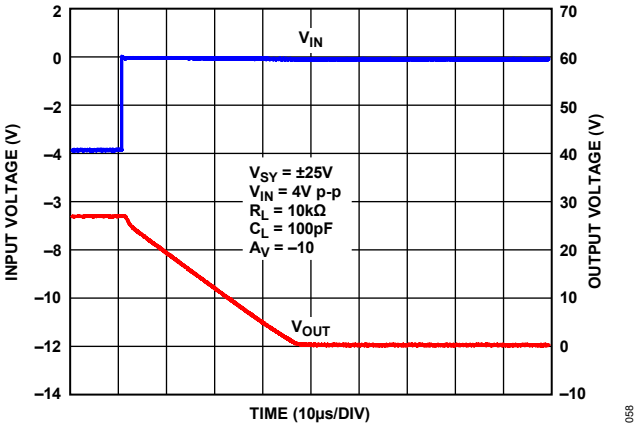

Figure 40. Positive Overload Recovery, V_{SY} = ±25V

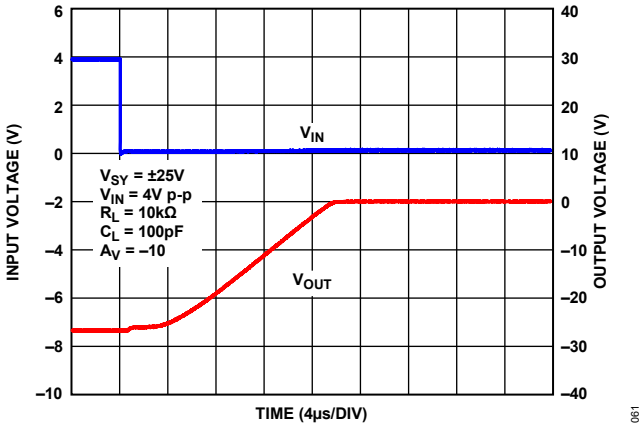

Figure 41. Negative Overload Recovery, V_{SY} = ±25V

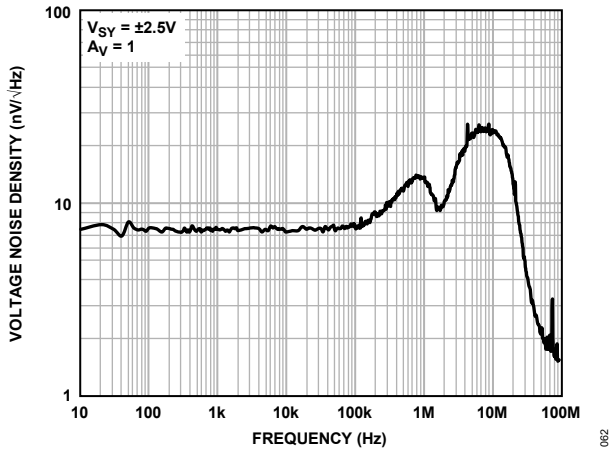

Figure 42. Voltage Noise Density vs. Frequency, V_{SY} = ±2.5V

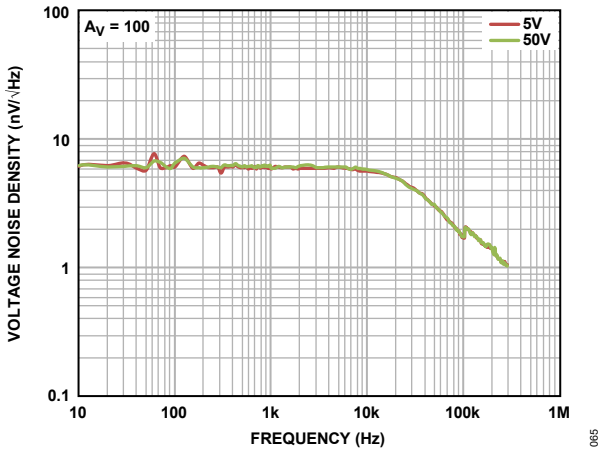

Figure 43. Voltage Noise Density vs. Frequency, A_V = 100

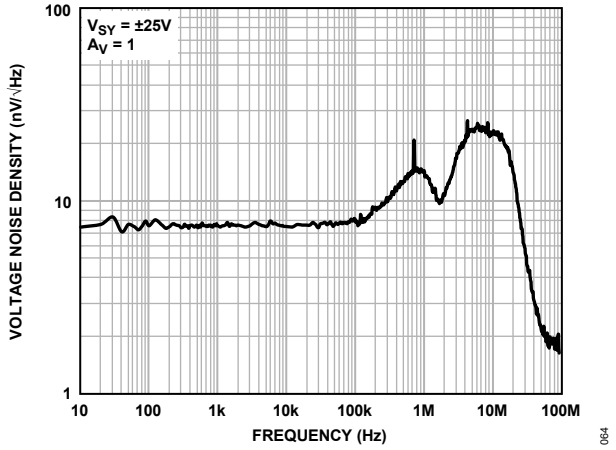

Figure 44. Voltage Noise Density vs. Frequency, V_{SY} = ±25V

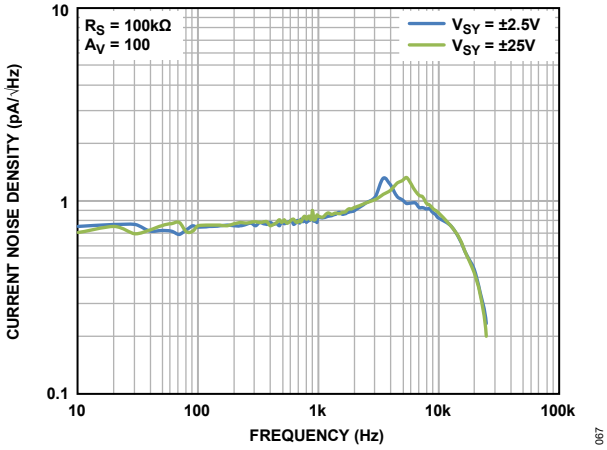

Figure 45. Current Noise Density vs. Frequency

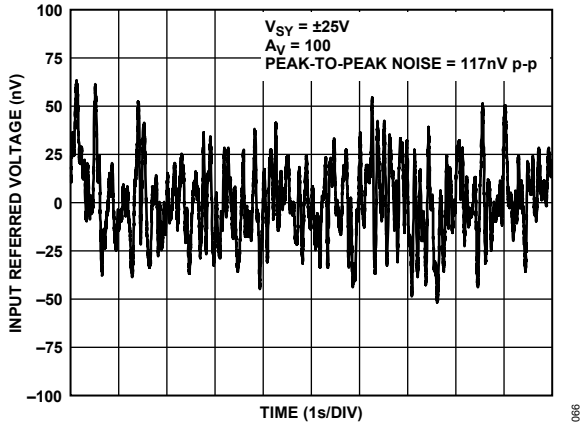

Figure 46. 0.1Hz to 10Hz Noise

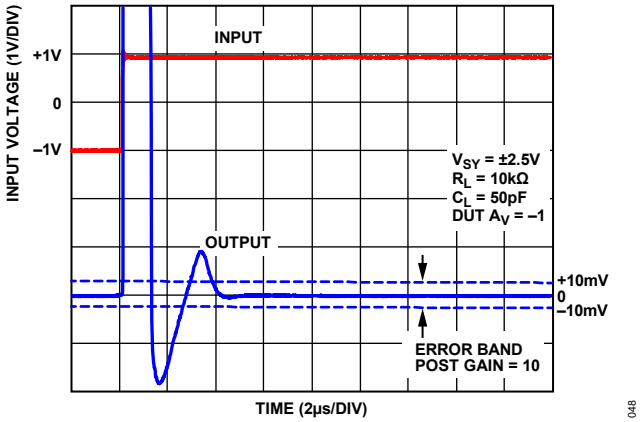

Figure 47. Positive Settling Time to 0.1%, V_{SY} = ±2.5V

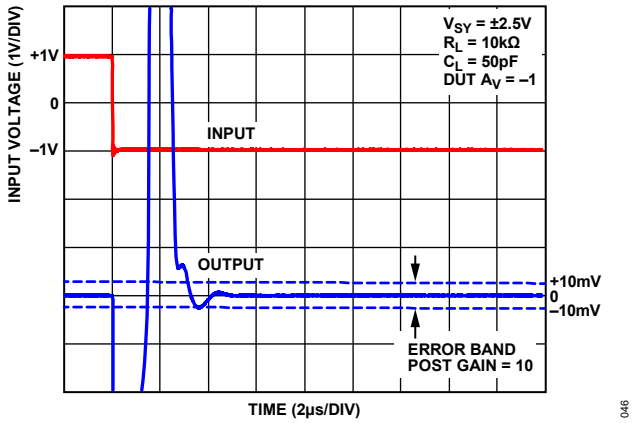

Figure 48. Negative Settling Time to 0.1%, V_{SY} = ±2.5V

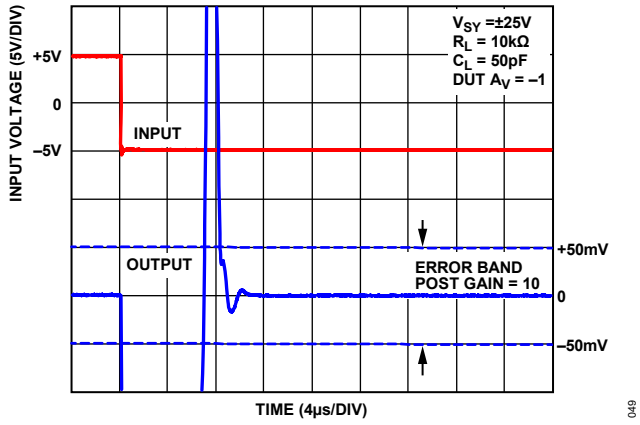

Figure 49. Positive Settling Time to 0.1%, V_{SY} = ±25V

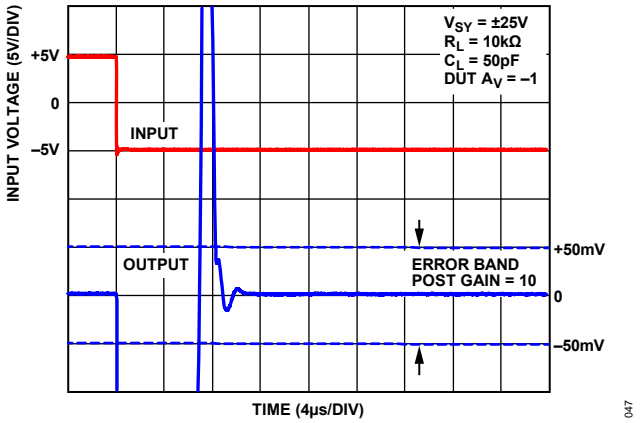

Figure 50. Negative Settling Time to 0.1%, V_{SY} = ±25V

THEORY OF OPERATION

The MAX74810 is a dual, ultralow noise, high voltage, zero drift, rail-to-rail output operational amplifier. It features a chopping technique that offers an ultralow input offset voltage of 7µV and an input offset voltage drift of 30nV/°C maximum. Offset voltage errors due to common-mode voltage swings and power supply variations are also corrected by the chopping technique, resulting in a superb typical CMRR figure of 144dB and a PSRR figure of 160dB at a 50V supply voltage.

The MAX74810 has a wide operating voltage range from ±2.25V (or 4.5V) to ±25V (or 50V). It is a single supply amplifier, where its input voltage range includes the lower supply rail. It also offers low voltage noise density of 5.8nV/√Hz (at f = 1kHz, A_V = 100) and reduced 1/f noise component. These features are ideal for the amplification of low level signals in high precision applications. A few examples of such applications are weigh scales, high precision current sensing, high voltage buffers, and signal conditioning for temperature sensors, among others.

Figure 51 shows the MAX74810 architecture block diagram. The architecture consists of an input EMI filter and clamp circuitry, three gain stages (G_{m1}, G_{m2}, and G_{m3}), input and output chopping networks ($CHOP_{IN}$ and $CHOP_{OUT}$), a clock generator, offset and ripple correction loop circuitry, frequency compensation capacitors (C1, C2, and C3), and thermal shutdown circuitry.

An EMI filter and clamp circuit are implemented at the input front-end to protect the internal circuitry against electrostatic discharge (ESD) stresses and high voltage transients.

$CHOP_{IN}$ and $CHOP_{OUT}$ are controlled by a clock generator and operate at 4.8MHz. The input baseband signal is initially modulated by $CHOP_{IN}$. Next, $CHOP_{OUT}$ demodulates the input signal and modulates the millivolt level input offset voltage and 1/f noise of the input transconductance amplifier, G_{m1}, to the chopping frequency at 4.8MHz. The chopping networks remove the low frequency errors, but, in return, the networks introduce chopping artifacts at the chopping frequency. Therefore, an offset and ripple correction loop, operating at 800kHz, is used. This frequency is the switching frequency of the amplifier. This circuitry reduces chopping artifacts, allowing the MAX74810 to have a high chopping frequency with minimal artifacts.

The thermal shutdown circuit shuts down the circuit when the die is overheated (see the *Thermal Shutdown* section for more information).

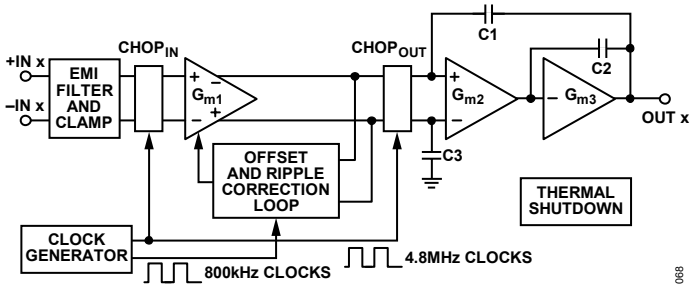

Figure 51. MAX74810 Architecture Block Diagram

On-Chip Input EMI Filter and Clamp Circuit

Figure 52 shows the input EMI filter and clamp circuit. The MAX74810 has internal ESD protection diodes (D1, D2, D3, and D4) connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse-biased during normal operation. This protection scheme allows voltages as high as approximately 300mV beyond the rails to be applied at the input of either terminal without causing permanent damage. See *Table 3* in the *Absolute Maximum Ratings* section for more information.

The EMI filter is composed of two 200Ω input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}), and a differential capacitor (C_{DM}). These RC networks set the −3dB low-pass cutoff frequencies at 50MHz for common-mode signals, and at 33MHz for differential signals. After the EMI filter, back-to-back diodes (D5 and D6) are added to protect internal circuit devices from high voltage input transients. Each diode has about 1V of forward turn-on voltage.

As specified in the *Absolute Maximum Ratings* section (see *Table 3*), the maximum input differential voltage is limited to ±5V. If more than ±5V is applied, a continuous current larger than ±10mA flows through one of the back-to-back diodes. This current compromises long-term reliability and can cause permanent damage to the device.

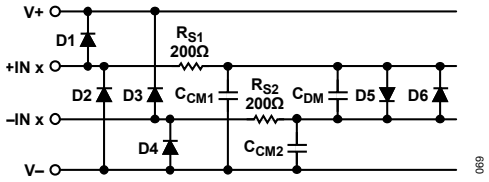

Figure 52. Input EMI Filter and Clamp Circuit

Thermal Shutdown

As soon as the junction temperature reaches 190°C, the thermal shutdown circuitry shuts down the amplifier. Note that either one of the two thermal shutdown circuitries is activated; this activation disables the channel. When the amplifier is disabled, the output becomes open state and the quiescent current of the channel decreases to 0.1mA. When the junction temperature cools down to 160°C, the thermal shutdown circuitry enables the amplifier and the quiescent current increases to its typical value.

When overheating in the die is caused by an undesirable excess amount of output current, the thermal shutdown circuit repeats its function. The junction temperature keeps increasing until it reaches 190°C and one of the channels is disabled. Then, the junction temperature cools down until it reaches 160°C, and the channel is enabled again. The process then repeats.

Input Protection

When the input of the MAX74810 exceeds one of the supply rails by more than 300mV, the ESD diodes mentioned in the *On-Chip Input EMI Filter and Clamp Circuit* section become forward-biased and large amounts of current begin to flow through them. Without current limiting, this excessive fault current causes permanent damage to the device. If the inputs are expected to be subject to overvoltage conditions, insert a resistor in series with each input to limit the input current to ±10 mA maximum. However, consider the resistor thermal noise effect on the entire circuit.

At a ±25V supply voltage, the broadband voltage noise of the MAX74810 is approximately 5.8nV/√Hz (at unity gain), and a 1kΩ resistor has a thermal noise of 4nV/√Hz. Adding a 1kΩ resistor increases the total noise to 7nV/√Hz.

Noise Considerations

1/f Noise

1/f noise, also known as pink noise or flicker noise, is inherent in semiconductor devices and increases as frequency decreases. At a low frequency, 1/f noise is a major noise contributor and causes a significant output voltage offset when amplified by the noise gain of the circuit. However, because the low frequency 1/f noise appears as a slow varying offset to the MAX74810, it is effectively reduced by the chopping technique. This technique allows the MAX74810 to have a much lower noise at DC and low frequency in comparison to standard low noise amplifiers that are susceptible to 1/f noise. *Figure 46* shows the 0.1Hz to 10Hz noise to be only 117nV p-p of noise.

APPLICATIONS INFORMATION

Use of Large Source Resistance

The MAX74810 is designed to work with low value source resistance. Note that the amplifier has an ultralow voltage noise density of 5.8nV/√Hz. A 1kΩ resistor contributes 4nV/√Hz; therefore, placing a 1kΩ resistor at the input increases total noise to 7nV/√Hz. For this reason (noise), it is recommended to avoid using large source resistance.

Unity Gain Follower with Large Source Resistance

When the MAX74810 is configured in a unity-gain follower configuration with a large source resistance and slow power supply ramp rate, the amplifier output may rail to the positive supply.

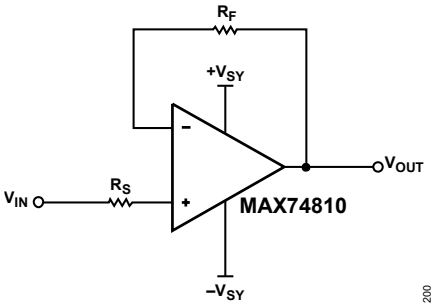

Figure 53. Insert R_F When Large R_S is Used

Workaround

To avoid the amplifier output railing to the positive supply, implement one of the following actions (see *Table 6* and *Figure 53*):

- Reduce the value of the source resistance (R_S).
- Insert a feedback resistor (R_F).

Table 6. Amplifier Output Railing Workaround Recommendations

CONDITION	RECOMMENDATION
$1.5V \le V_{SY} - V_{IN} < 2.5V$	$R_F = 200\Omega$ or $R_F \ge 50R_S$, whichever is greater
$2.5V \le V_{SY} - V_{IN} < 3.5V$	$R_S \le 200\Omega$ or $R_F \ge 2R_S$
$V_{SY} - V_{IN} \ge 3.5V$	$R_S \le 500\Omega$ or $R_F \ge 0.5R_S$

OUTLINE DIMENSIONS

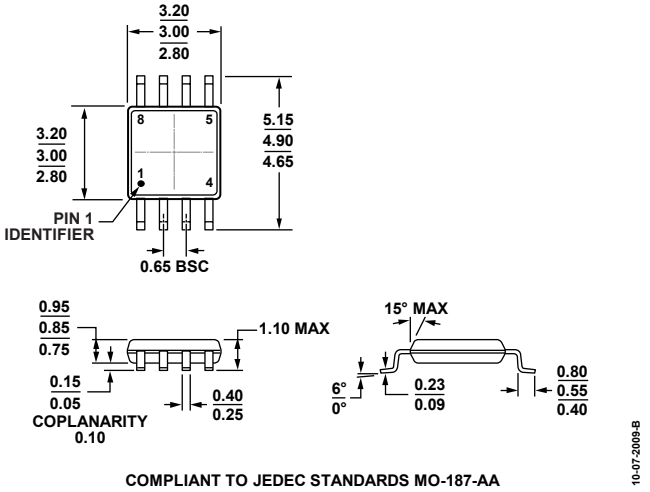

Figure 54. 8-Lead Mini Small Outline Package [MSOP] (RM-8) Dimensions shown in millimeters

ORDERING GUIDE

Table 7. Ordering Guide

MODEL[1]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKING QUANTITY	PACKAGE OPTION	MARKING CODE
MAX74810ARMZ	-40°C to +125°C	8-Lead MSOP	Tube, 50	RM-8	A6R
MAX74810ARMZ-R7	-40°C to +125°C	8-Lead MSOP	Reel, 1000	RM-8	A6R
MAX74810ARMZ-RL	-40°C to +125°C	8-Lead MSOP	Reel, 3000	RM-8	A6R

[1] Z = RoHS compliant part

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	06/25	Initial release	-