# Low-Power, Precision Instrumentation Amplifier with Programmable Gain

**MAX41400**

## General Description

The MAX41400 is a low-power, high-precision instrumentation amplifier with programmable gain through input pins.

Available in a space-saving, 9-bump wafer-level package (WLP) with a 0.4mm bump pitch, it is designed for use in portable medical and industrial sensor applications. The device features internal EMI filters to protect from RF disturbances and EMI. The internal fixed gain can be selected from 10V/V to 250V/V. The gain-setting resistors are located inside the device, thus minimizing gain drift variations over the temperature range.

The MAX41400 features rail-to-rail CMOS inputs and outputs; a 28kHz, -3dB bandwidth at just 65µA (typ) supply current; and 25µV (max) zero-drift input offset voltage over time and temperature. The zero-drift feature eliminates the high 1/f noise typically found in CMOS input amplifiers, making it useful for a wide variety of low-frequency measurement applications.

The MAX41400 operates from a 1.7V to 3.6V power supply voltage and is specified over the -40°C to +125°C automotive temperature range.

## Applications

- Low-Power Sensor Interface
- Pressure, Weight, and Force Sensors
- RTD Temperature Sensors
- Wearable Devices
- EKG Medical Devices
- Insulin and Infusion Pumps

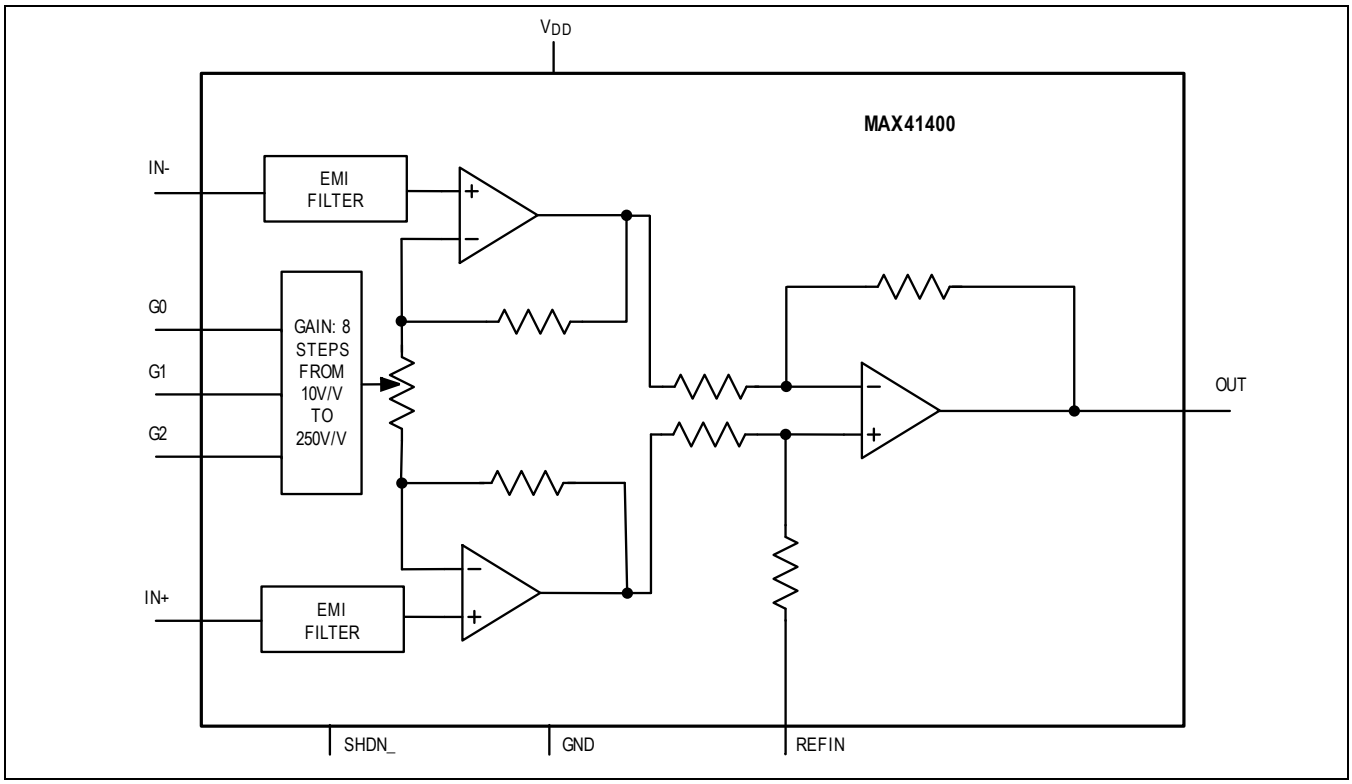
## Benefits and Features

- Supply Voltage Range: 1.7V to 3.6V
- Very Low 25µV (max) Input Offset Voltage
- Low 65µA Quiescent Current
- Rail-to-Rail Inputs and Outputs
- EMIRR
  - >100dB at 1800MHz, 2400MHz
  - >90dB at 900MHz
- 28kHz, -3dB Bandwidth
- On-the-Fly Programmable Gain:
  - 10V/V, 20V/V, 40V/V, 80V/V, 100V/V, 150V/V, 200V/V, and 250V/V
- Power-Saving Shutdown Mode
- Available in Tiny 1.26mm x 1.23mm, 9-Bump WLP and 2.5mm x 2mm, 10-Pin TDFN

***Ordering Information*** ***appears at end of data sheet.***

19-100852; Rev 3; 7/24

## Simplified Block Diagram



## Absolute Maximum Ratings

$V_{DD}$ to GND .....-0.3V to +4V

IN+ to IN-.....-0.3V to $V_{DD}$ + 0.3V

OUT, REF to GND.....-0.3V to $V_{DD}$ + 0.3V

IN+, IN-, G0, G1, G2, SHDN_ to GND.....-0.3V to $V_{DD}$ + 0.3V

Continuous Current into any Input/Output Pin ..... 10mA

Output Short-Circuit Duration to Either $V_{DD}$ or GND .....Continuous

Continuous Power Dissipation (WLP - derate 11.91mW/°C above +70°C).....952.61mW

Continuous Power Dissipation (TDFN - derate 9.80mW/°C above +70°C).....784mW

Operating Temperature Range .....-40°C to +125°C

Junction Temperature .....+150°C

Storage Temperature Range .....-40°C to +150°C

Soldering Temperature (reflow).....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

| **Ultra-Thin WLP** | |
|---|---|
| Package Code | N91F1+1 |
| Outline Number | 21-100443 |
| Land Pattern Number | Refer to Application Note 1891 |
| **Thermal Resistance, Four Layer Board:** | |
| Junction-to-Ambient ($\theta_{JA}$) | 83.98°C/W |
| Junction-to-Case ($\theta_{JC}$) | 24.60°C/W |

| **10 TDFN** | |
|---|---|
| Package Code | T102A2+2C |
| Outline Number | 21-100013 |
| Land Pattern Number | 90-100007 |
| **Thermal Resistance, Four Layer Board:** | |
| Junction-to-Ambient ($\theta_{JA}$) | 102°C/W |
| Junction-to-Case ($\theta_{JC}$) | 2.90°C/W |

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

## Electrical Characteristics

(Global conditions unless otherwise stated: $V_{DD}$ = 1.8V, $V_{IN+}$ = $V_{IN-}$ = $V_{DD}/2$, $V_{REFIN}$ = $V_{DD}/2$, G = 10V/V, $R_{LOAD}$ = 10kΩ to $V_{DD}/2$, $V_{\overline{SHDN}}$ = $V_{DD}$, typical values at +25°C, -40°C ≤ $T_A$ ≤ +125°C)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DC SPECIFICATIONS** | | | | | | | |
| Input Offset Voltage | $V_{OS}$ | -40°C ≤ $T_A$ ≤ +85°C | All gain options | | 1 | 25 | µV |
| | | -40°C ≤ $T_A$ ≤ +125°C | All gain options | | 1 | 35 | |
| Input Offset Drift | $TCV_{OS}$ | | | | 5 | | nV/°C |
| Input Bias Current | $I_B$ | $T_A$ = +25°C | *Note 1* | | 10 | 150 | pA |
| | | -40°C ≤ $T_A$ ≤ +125°C | *Note 1* | | 10 | 300 | |
| Input Offset Current | $I_{OS}$ | *Note 1* | | | 10 | | pA |
| Input Common-Mode Range | $V_{CM}$ | Guaranteed by CMRR | | 0.1 | | VDD - 0.1 | V |
| Input ESD Protections | | HBM, both IN+ and IN- | | | 2 | | kV |
| Common-Mode Rejection Ratio | CMRR | -40°C ≤ $T_A$ ≤ +125°C | Gain = 10, 20 | 106 | 120 | | dB |
| | | | Gain = 40, 80 | 115 | 130 | | |
| | | | Gain = 100, 150 | 120 | 130 | | |
| | | | Gain = 200, 250 | 120 | 130 | | |
| Power-Supply Rejection Ratio | PSRR | 1.7V ≤ $V_{DD}$ ≤ 3.6V | Gain = 10, 20 | 98 | 110 | | dB |
| | | | Gain = 40, 80 | 110 | 120 | | |
| | | | Gain = 100, 150 | 113 | 130 | | |
| | | | Gain = 200, 250 | 113 | 130 | | |
| Range of Gain | G | | | | WLP: 10, 40, 100, 200 TDFN: 10, 20, 40, 80, 100, 150, 200, 250 | | V/V |
| Gain Selection Settling Time | | $V_{OUT}$ to settle within ±100mV | | | 20 | | µs |
| Gain Error | $G_E$ | $T_A$ = +25°C | All gain options | | 0.05 | 0.18 | % |
| | | -40°C ≤ $T_A$ ≤ +125°C | All gain options | | 0.08 | 0.40 | |
| Gain Error Tempco | $TC_{GE}$ | | | | 5 | | ppm/°C |
| Output Voltage Swing High | $V_{OH}$ | $V_{DD}$ - $V_{OUT}$ | $R_{LOAD}$ = 10kΩ to $V_{DD}/2$ | | | 50 | mV |

(Global conditions unless otherwise stated: $V_{DD}$ = 1.8V, $V_{IN+}$ = $V_{IN-}$ = $V_{DD}$/2, $V_{REFIN}$ = $V_{DD}$/2, G = 10V/V, $R_{LOAD}$ = 10kΩ to $V_{DD}$/2, $V_{\overline{SHDN}}$ = $V_{DD}$, typical values at +25°C, -40°C ≤ $T_A$ ≤ +125°C)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output Voltage Swing Low | $V_{OL}$ | $V_{OUT}$ - GND | $R_{LOAD}$ = 10kΩ to $V_{DD}$/2 | | | 25 | mV |
| **INPUT REFERENCE** | | | | | | | |
| Input Reference Voltage Range | $V_{REFIN}$ | | | 0 | | $V_{DD}$ | V |
| **AC SPECIFICATIONS** | | | | | | | |
| Bandwidth, -3dB | | Gain = 10 | | | 28 | | kHz |
| | | Gain = 40 | | | 28 | | |
| | | Gain = 100 | | | 10 | | |
| | | Gain = 200 | | | 5 | | |
| Slew Rate | SR | | | | 0.08 | | V/µs |
| Input Voltage-Noise Density | $V_N$ | f = 10Hz, 1kHz, 10kHz | WLP:<br>G = 10V/V<br>G = 40V/V<br>G = 100V/V<br>G = 200V/V<br>TDFN:<br>G = 20V/V<br>G = 80V/V<br>G = 150V/V<br>G = 250V/V | | WLP:<br>54<br>38<br>41<br>36<br>TDFN:<br>47<br>46<br>43<br>42 | | nV/√Hz |
| Input Voltage Noise | | 0.1Hz to 10Hz, gain = 10 | | | 1.3 | | $\mu V_{P-P}$ |
| EMI Rejection Ratio | EMIRR | $V_{RFPEAK}$ = 100$mV_{PK}$, f = 900MHz, both IN+ and IN- | | | >90 | | dB |
| | | $V_{RFPEAK}$ = 100$mV_{PK}$, f = 1800MHz, 2400MHz, both IN+ and IN- | | | >100 | | |
| Input Current-Noise Density | $I_N$ | f = 1kHz | | | 100 | | fA/√Hz |
| Capacitive Loading Stability | $C_L$ | | | | 100 | | pF |
| **POWER SUPPLY** | | | | | | | |
| Supply Voltage | $V_{DD}$ | Guaranteed by PSRR, -40°C ≤ $T_A$ ≤ +125°C | | 1.7 | | 3.6 | V |
| Supply Current | $I_{DD}$ | | | | 65 | 90 | µA |
| Power-Up Time | $t_{ON}$ | $V_{OUT}$ to settle within 90% | $V_{DD}$ = 0 to 1.8V step | | 100 | | µs |
| Shutdown Supply Current | $I_{SHDN}$ | -40°C ≤ $T_A$ ≤ +85°C | *Note 1* | | 0.1 | 0.3 | µA |
| | | -40°C ≤ TA ≤ +125°C | *Note 1* | | 0.1 | 0.7 | |

(Global conditions unless otherwise stated: $V_{DD}$ = 1.8V, $V_{IN+}$ = $V_{IN-}$ = $V_{DD}$/2, $V_{REFIN}$ = $V_{DD}$/2, G = 10V/V, $R_{LOAD}$ = 10kΩ to $V_{DD}$/2, $V_{\overline{SHDN}}$ = $V_{DD}$, typical values at +25°C, -40°C ≤ $T_A$ ≤ +125°C)

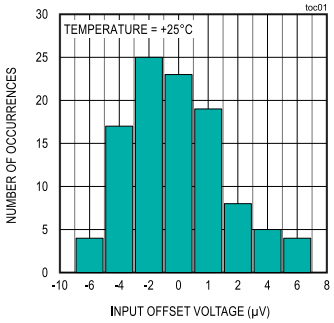
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Turn-On Time | $t_{ONSD}$ | $V_{OUT}$ to settle within 90% | $V_{DD}$ = 1.8V, $V_{\overline{SHDN}}$ = 0 to 1.8V step in <1µs | | 100 | | µs |
| **LOGIC INPUTS DC CHARACTERISTICS** | | | | | | | |
| Input Low Level | $V_{IL}$ | Active level | | | | 0.3 x $V_{DD}$ | V |
| Input High Level | $V_{IH}$ | | | 0.7 x $V_{DD}$ | | | V |
| Input Leakage Current | $I_L$ | | | | | 18 | nA |

**Note 1:** Guaranteed by design and characterization.

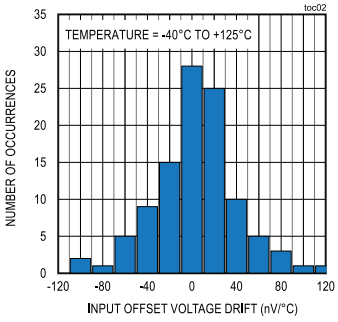
## Typical Operating Characteristics

(Global conditions unless otherwise stated: $V_{DD}$ = 1.8V, $V_{IN+}$ = $V_{IN-}$ = $V_{DD}$/2, $V_{REFIN}$ = $V_{DD}$/2, G = 10V/V, $R_{LOAD}$ = 10kΩ to $V_{DD}$/2, $V_{SHDN\_}$ = $V_{DD}$, typical values at +25°C, -40°C ≤ $T_A$ ≤ +125°C)

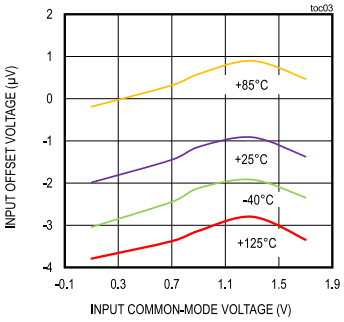
INPUT OFFSET VOLTAGE HISTOGRAM



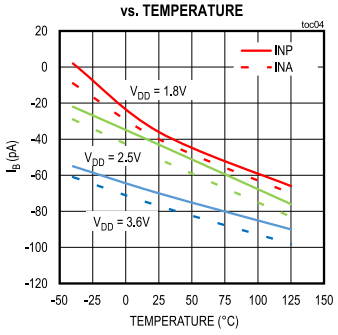

INPUT OFFSET VOLTAGE DRIFT HISTOGRAM



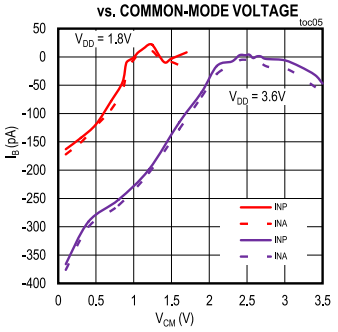

INPUT OFFSET VOLTAGE vs. INPUT COMMON-MODE VOLTAGE



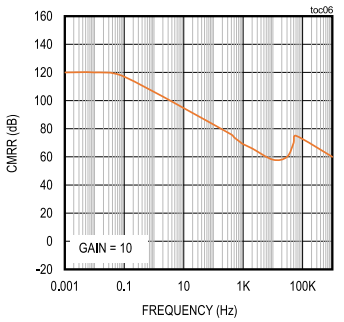

INPUT BIAS CURRENT vs. TEMPERATURE



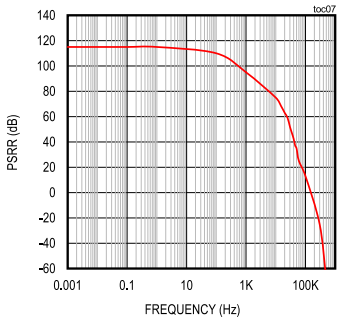

INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



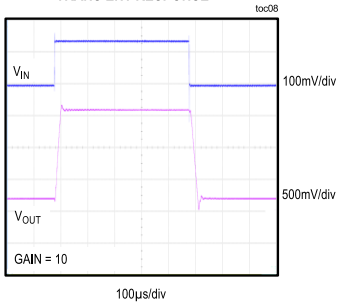

CMRR vs. FREQUENCY



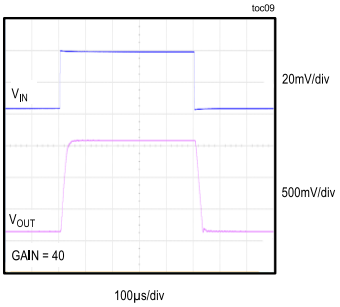

PSRR vs. FREQUENCY



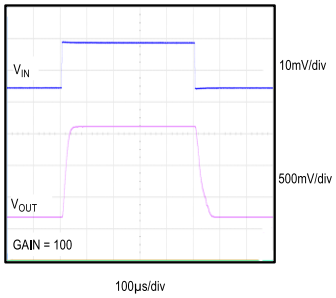

LARGE SIGNAL TRANSIENT RESPONSE



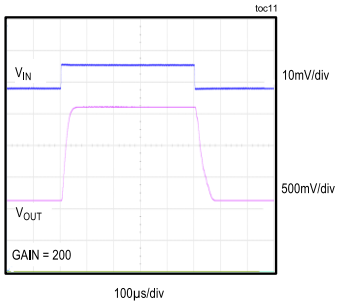

LARGE SIGNAL TRANSIENT RESPONSE



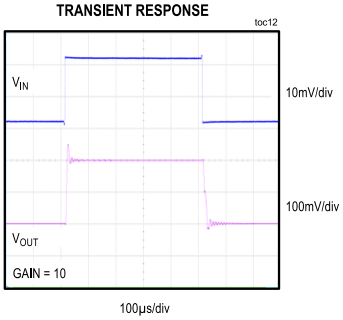
LARGE SIGNAL TRANSIENT RESPONSE



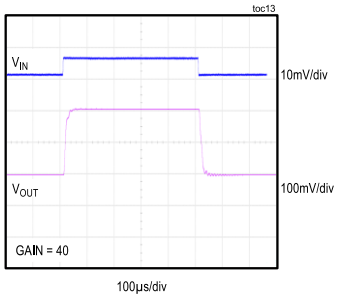

LARGE SIGNAL TRANSIENT RESPONSE



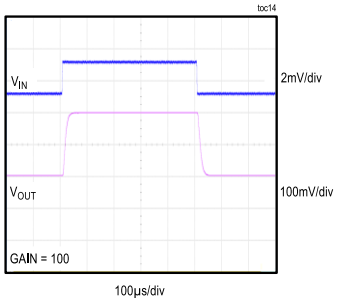

SMALL SIGNAL TRANSIENT RESPONSE



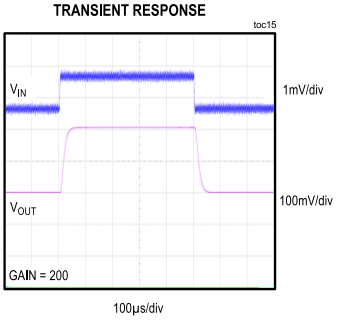

SMALL SIGNAL TRANSIENT RESPONSE



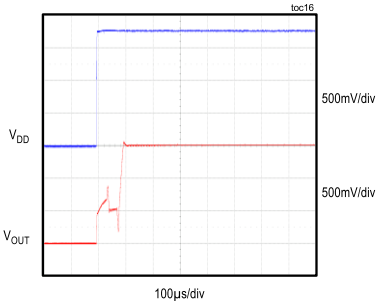

SMALL SIGNAL TRANSIENT RESPONSE



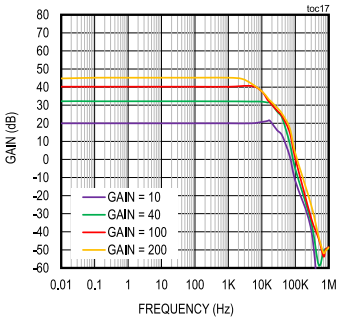

SMALL SIGNAL TRANSIENT RESPONSE



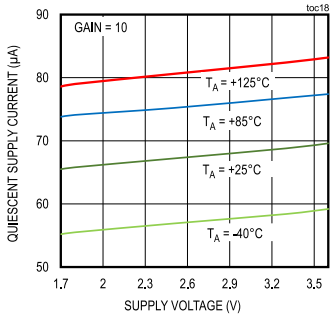

POWER-UP TIME



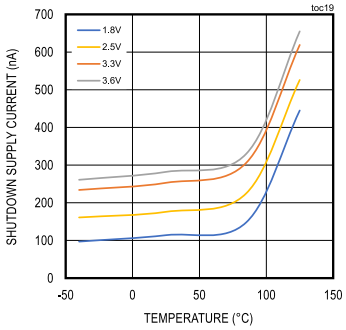

GAIN vs. FREQUENCY



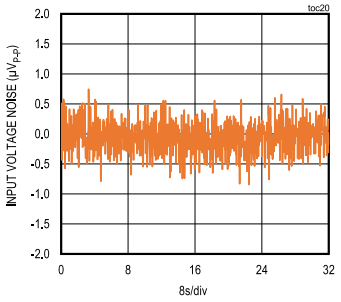

QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



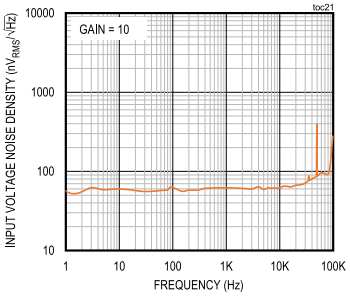

SHUTDOWN CURRENT vs. TEMPERATURE



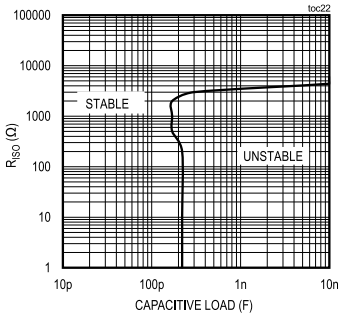

INTEGRATED NOISE (0.1Hz TO 10Hz)



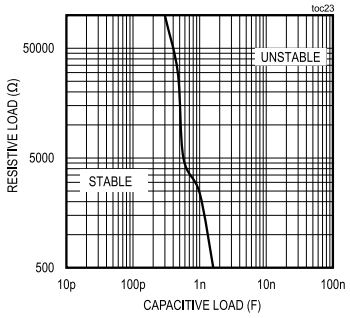

INPUT VOLTAGE NOISE DENSITY vs. FREQUENCY



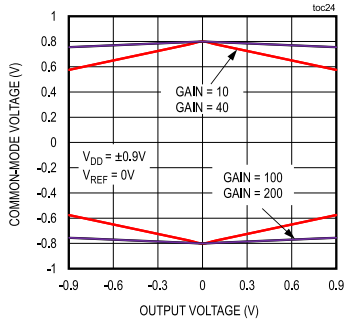
**STABILITY vs. CAPACITIVE LOAD AND ISOLATION RESISTOR**



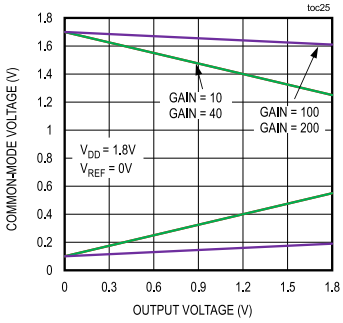

**STABILITY vs. CAPACITIVE LOAD AND RESISTIVE LOAD**



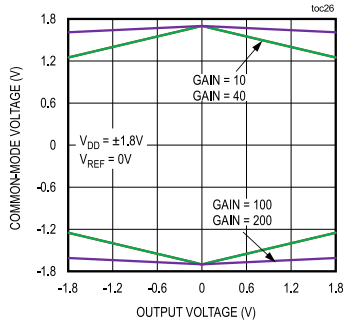

**TYPICAL COMMON-MODE RANGE vs. OUTPUT VOLTAGE**




**TYPICAL COMMON-MODE RANGE vs. OUTPUT VOLTAGE**




**TYPICAL COMMON-MODE RANGE vs. OUTPUT VOLTAGE**

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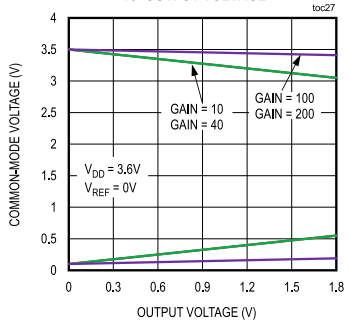
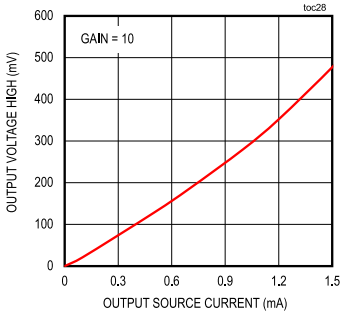
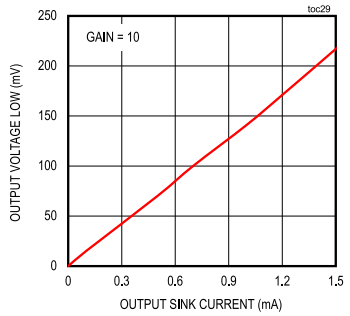


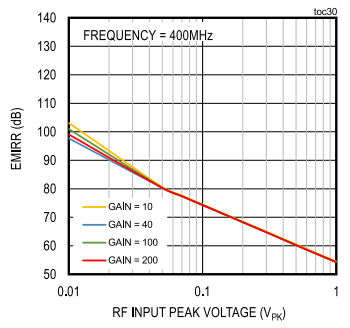

**OUTPUT VOLTAGE HIGH vs. OUTPUT SOURCE CURRENT**



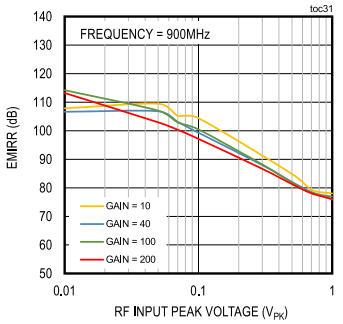

**OUTPUT VOLTAGE LOW vs. OUTPUT SINK CURRENT**



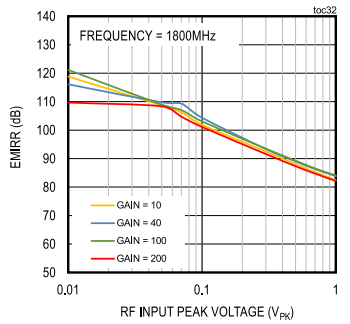

**EMIRR vs. INPUT VOLTAGE**



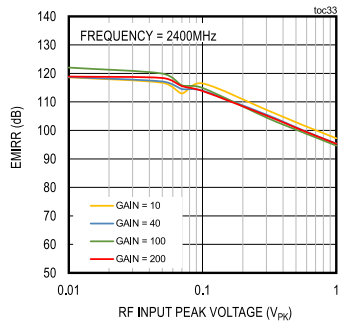

**EMIRR vs. INPUT VOLTAGE**

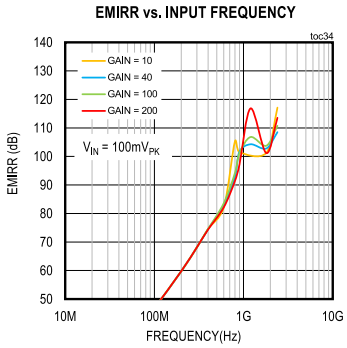



**EMIRR vs. INPUT VOLTAGE**



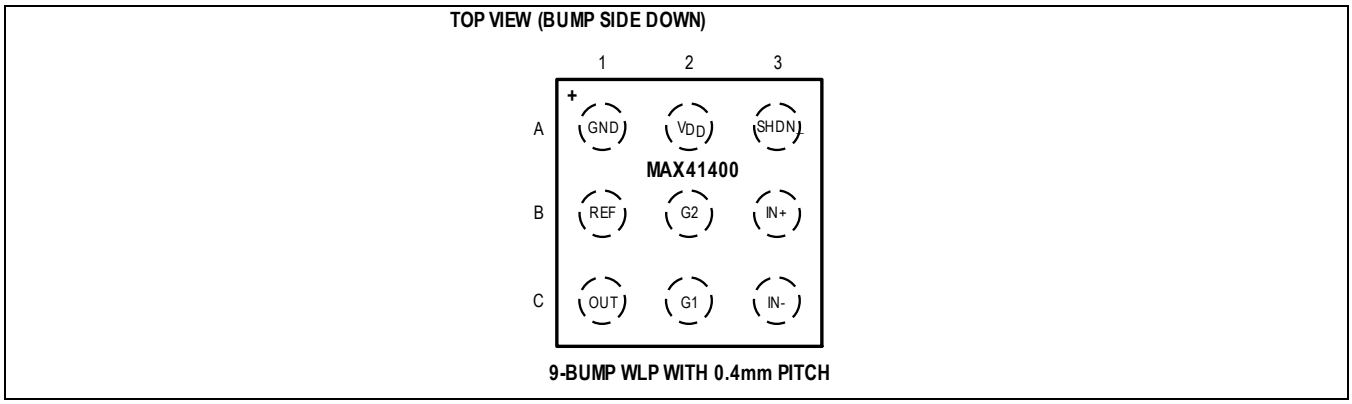

**EMIRR vs. INPUT VOLTAGE**



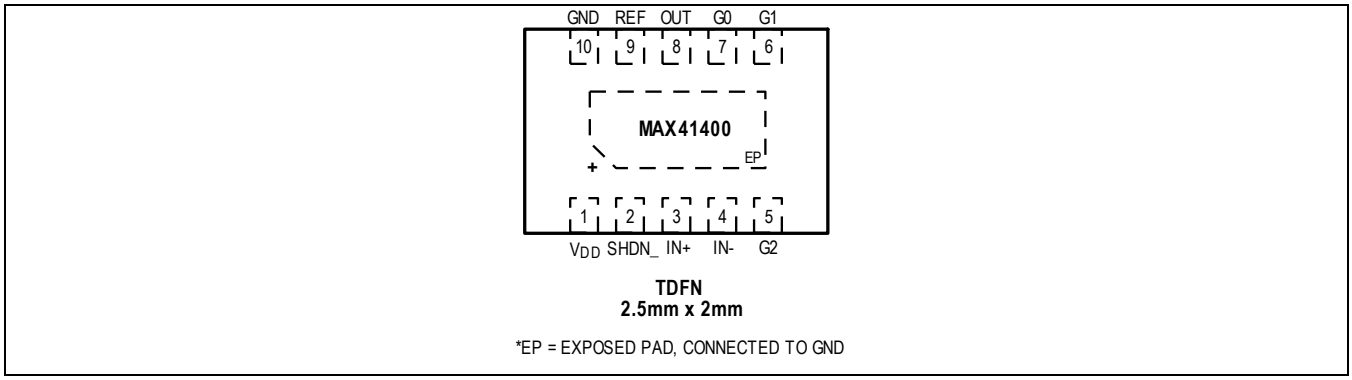

EMIRR vs. INPUT FREQUENCY
toc34
GAIN = 10
GAIN = 40
GAIN = 100
GAIN = 200
$V_{IN}$ = 100m$V_{PK}$
EMIRR (dB)
140
130
120
110
100
90
80
70
60
50
10M
100M
1G
10G
FREQUENCY(Hz)

## Pin Configurations

**WLP**




**TDFN**




## Pin Descriptions

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| WLP | TDFN | | |
| B3 | 3 | IN+ | Noninverting Input |
| A1 | 10 | GND | Ground |
| C3 | 4 | IN- | Inverting Input |
| A2 | 1 | $V_{DD}$ | Positive Supply |
| C1 | 8 | OUT | Output |
| A3 | 2 | SHDN_ | Shutdown (active low) |
| B1 | 9 | REF | Input Reference |
| — | 7 | G0 | Gain Selection Input. Connect to either $V_{DD}$ or GND. The gain selection is based on the appropriate gain selection table in the *Detailed Description*. |
| C2 | 6 | G1 | Gain Selection Input. Connect to either $V_{DD}$ or GND. The gain selection is based on the appropriate gain selection table in the *Detailed Description*. |
| B2 | 5 | G2 | Gain Selection Input. Connect to either $V_{DD}$ or GND. The gain selection is based on the appropriate gain selection table in the *Detailed Description*. |

## Detailed Description

The MAX41400 is a programmable-gain precision instrumentation amplifier based on a traditional three-amplifier topology. The input stage is composed of two operational amplifiers that together provide a high common-mode rejection ratio, low input bias current, and low input offset voltage. The output stage is a conventional differential amplifier that provides an overall common-mode rejection of 130dB (G = +10V/V).

The amplifier has on-chip gain-setting resistors and the gains are selectable through input pins. On-chip trimming of internal gain-setting resistors helps optimize gain error, CMRR, and offset. Since all gain-setting resistors are within the device, this minimizes gain drift variation over the temperature range and saves design time and space.

### Gain-Selection Inputs

Three inputs are used to select the internal gain for the TDFN package option. Each input can be connected to either GND or $V_{DD}$.

The WLP option supports only two inputs that limits gain selection to four options.

## Table 1. Gain Selection (TDFN)

| PACKAGE | G2 | G1 | G0 | GAIN (V/V) |
|---|---|---|---|---|
| TDFN | GND | GND | GND | 10 |
| | GND | GND | $V_{DD}$ | 20 |
| | GND | $V_{DD}$ | GND | 40 |
| | GND | $V_{DD}$ | $V_{DD}$ | 80 |
| | $V_{DD}$ | GND | GND | 100 |
| | $V_{DD}$ | GND | $V_{DD}$ | 150 |
| | $V_{DD}$ | $V_{DD}$ | GND | 200 |
| | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | 250 |

## Table 2. Gain Selection (WLP)

| PACKAGE | G2 | G1 | GAIN (V/V) |
|---|---|---|---|
| WLP | GND | GND | 10 |
| | GND | $V_{DD}$ | 40 |
| | $V_{DD}$ | GND | 100 |
| | $V_{DD}$ | $V_{DD}$ | 200 |

### Input Voltage Range

The common-mode input range for all of these amplifiers is ($V_{SS}$ + 0.1V) to ($V_{DD}$ - 0.1V). Ideally, the instrumentation amplifier responds only to a differential voltage applied to its inputs, IN+ and IN-. If both inputs are at the same voltage, the output is $V_{REF}$. A differential voltage at IN+ ($V_{IN+}$) and IN- ($V_{IN-}$) develops an identical voltage across the gain-setting resistor, causing a current ($I_G$) to flow. This current also flows through the feedback resistors of the two input amplifiers A1 and A2, generating a differential voltage of:

$$V_{OUT2} - V_{OUT1} = I_G \times (R_1 + R_G + R_1)$$

where $V_{OUT1}$ and $V_{OUT2}$ are the output voltages of A1 and A2, $R_G$ is the gain-setting resistor, and $R_1$ is the feedback resistor of the input amplifiers.

$I_G$ is determined by the following equation:

$$I_G = \frac{(V_{IN+} - V_{IN-})}{R_G}$$

The output voltage ($V_{OUT}$) for the instrumentation amplifier is expressed in the following equation:

$$V_{OUT} = (V_{IN+} + V_{IN-}) \times (2 \times \frac{R_1}{R_G} + 1) \times \frac{R_3}{R_2}$$

The common-mode input range is a function of the amplifier's output voltage and the supply voltage. With a power supply of $V_{DD}$, the largest output signal swing can be obtained with REF tied to $V_{DD}/2$. This results in an output-voltage swing of $\pm V_{DD}/2$. An output-voltage swing less than full scale increases the common-mode input range.

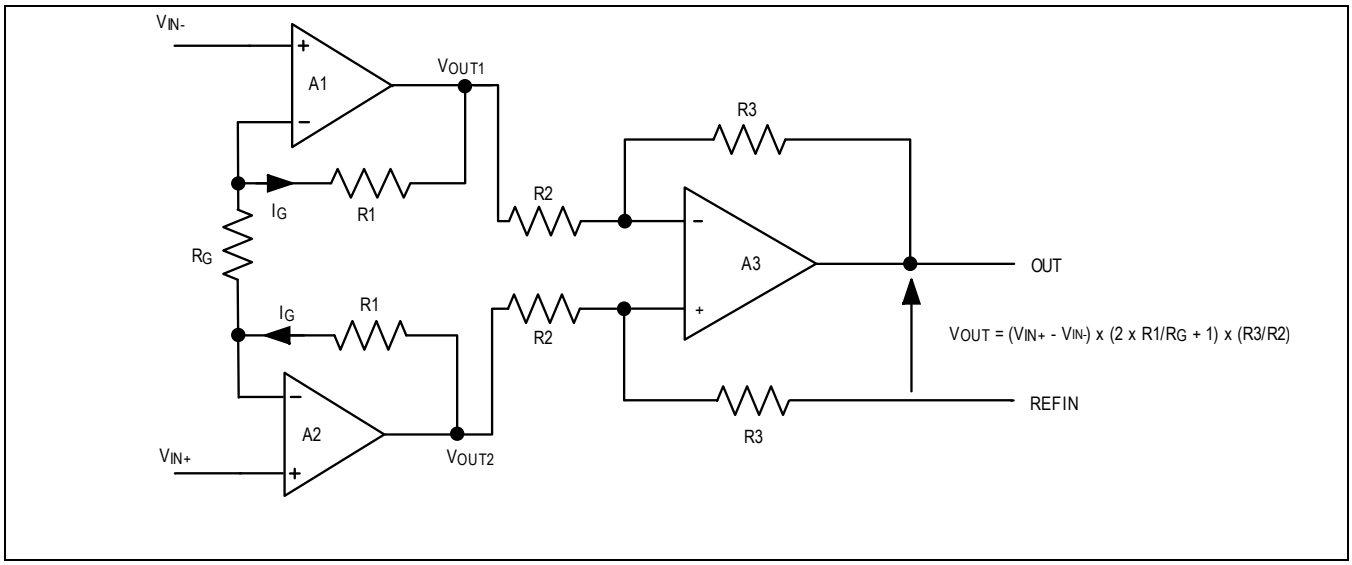



*Figure 1. MAX41400 Internal Configuration*

### Input Stage and Output Stage Gain Setting

When $R_2$ and $R_3$ are not equally set at the output stage, the MAX41400's gain is determined by the gain of both the input stage (A1) and output stage (A2) amplifiers. At a different gain setting, internal $R_1$, $R_G$, $R_2$, and $R_3$ are selected respectively. *Table 3* shows the input and output stage gain settings with respect to the total gain of the MAX41400.

## Table 3. Input Stage and Output Stage Gain

| G2 | G1 | G0 | GAIN1 INPUT STAGE | GAIN2 OUTPUT STAGE | GAIN |
|---|---|---|---|---|---|
| GND | GND | GND | 5 | 2 | 10 |
| GND | GND | $V_{DD}$ | 10 | 2 | 20 |
| GND | $V_{DD}$ | GND | 20 | 2 | 40 |
| GND | $V_{DD}$ | $V_{DD}$ | 8 | 10 | 80 |
| $V_{DD}$ | GND | GND | 10 | 10 | 100 |
| $V_{DD}$ | GND | $V_{DD}$ | 15 | 10 | 150 |
| $V_{DD}$ | $V_{DD}$ | GND | 20 | 10 | 200 |
| $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | 25 | 10 | 250 |

### Input Common-Mode Range vs. Output Voltage Characterization

*Figure 2* illustrates the MAX41400's typical common-mode input voltage range over the output voltage swing at a different gain. Although the common-mode input range for all three amplifiers is ($V_{SS}$ + 0.1V) to ($V_{DD}$ - 0.1V), the common-mode input voltage range of MAX41400 is changed with the amplifier's output voltage and gain setting. The reason is, as the input stage's operational amplifiers A1 and A2 amplify the differential input voltage, the common-mode input voltage range

of the MAX41400 is limited by the output stage differential amplifier's linear input range. For example, with gain = 10, when the output voltage is 0.9V, the MAX41400's common-mode input voltage range is determined by the input range of the output amps (±0.8V) minus the amplified differential input amplitude at the output amps (±0.225V). For a higher gain configuration, the $V_{CM}$ range will increase, since a smaller differential voltage is necessary for the given output voltage.

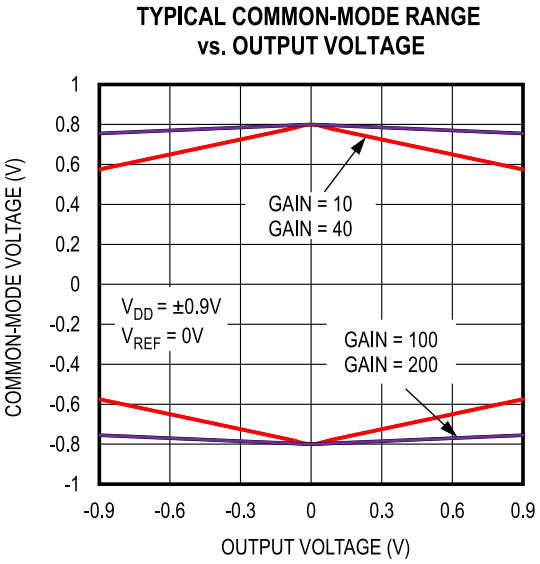



*Figure 2. Common-Mode Input Range over Output Swing*

## Shutdown Mode

The MAX41400 features a low-power shutdown mode. When the shutdown pin ($\overline{SHDN}$) is pulled low, the internal amplifiers are switched off and the supply current drops to 0.1µA, typ. This disables the instrumentation amplifier and puts its output in a high-impedance state. Pulling $\overline{SHDN}$ high enables the instrumentation amplifier.

## External Noise Suppression in EMI Form

The MAX41400 has input EMI filters to prevent effects of radio frequency interference on the output. The EMI filters comprise passive devices that present significantly higher impedance to higher frequency signals.

## Input Offset Voltage

The MAX41400 features a chop structure, which reduces input offset voltage and 1/f noise while reducing the output ripple typically associated with chopping circuits. The output stage resistor bridge is carefully trimmed to reduce the offset introduced by the mismatch of the resistor network.

## External Offset Adjustment

If necessary, external offset can be adjusted by applying a voltage at the REF pin. The voltage applied at the REF pin is required to have a low output impedance (i.e., lower than 10Ω) in order to provide high common-mode rejection.

## Applications Information

### Gain-Selection Input Logic

The MAX41400 features a digitally adjustable gain-selection input (G0,G1,G2), which allows changing the instrumentation amplifier gain without an external gain setting resistor, thus minimizing gain drift variation over the temperature range and saving design time and space.

Input low level ($V_{IL}$) and input high level ($V_{IH}$) determine the threshold for gain-selection input to recognize a valid logic state. With three gain-selection inputs (TDFN) and two gain-selection inputs (WLP) available, the MAX41400 supports eight gain settings (TDFN) and four gain settings (WLP) respectively.

The logic state of the gain-selection input can be achieved by connecting the input pin to either GND or $V_{DD}$ or can be controlled by a microcontroller. Note that the logic threshold is referred to the negative supply rail of the MAX41400 for dual-supply operation.

### Capacitive-Load Stability

The MAX41400 is stable for capacitive loads up to 100pF. Applications that require greater capacitive-load driving capability can use an isolation resistor between the output and the capacitive load to reduce ringing on the output signal. However, this alternative reduces gain accuracy because $R_{ISO}$ forms a potential divider with the load resistor.

### Power Supplies and Layout

The MAX41400 operates either with a single supply from +1.7V to +3.6V with respect to ground or with dual supplies from ±0.85V to ±1.8V. For best performance, bypass each power supply to ground with a separate 0.1µF capacitor.

Good layout technique optimizes performance by decreasing the amount of stray capacitance at the instrumentation amplifier's input. Excess capacitance will produce peaking in the amplifier's frequency response. To decrease stray capacitance, minimize trace lengths by placing external components as close to the instrumentation amplifier as possible.

### Transducer Applications

The MAX41400 can be used in various signal-conditioning circuits for thermocouples, PT100s, strain gauges (displacement sensors), piezoresistive transducers (PRTs), flow sensors, and bioelectrical applications. *Figure 3* shows a simplified example of how to attach four strain gauges (two identical two-element strain gauges) to the inputs of the MAX41400. The bridge contains four resistors, two of which increase and two of which decrease by the same ratio.

With a fully balanced bridge, points A (IN+) and B (IN-) see half of the the excitation voltage ($V_{BRIDGE}$). The low impedance (120Ω to 350Ω) of the strain gauges, however, could cause significant voltage drop contributions by the wires leading to the bridge, which would cause excitation variations. The output voltage ($V_{OUT}$) can be calculated as follows:

$$V_{OUT} = V_{AB} \times G$$

where G is the gain of the MAX41400.

## Typical Application Circuits

### Transducer Application

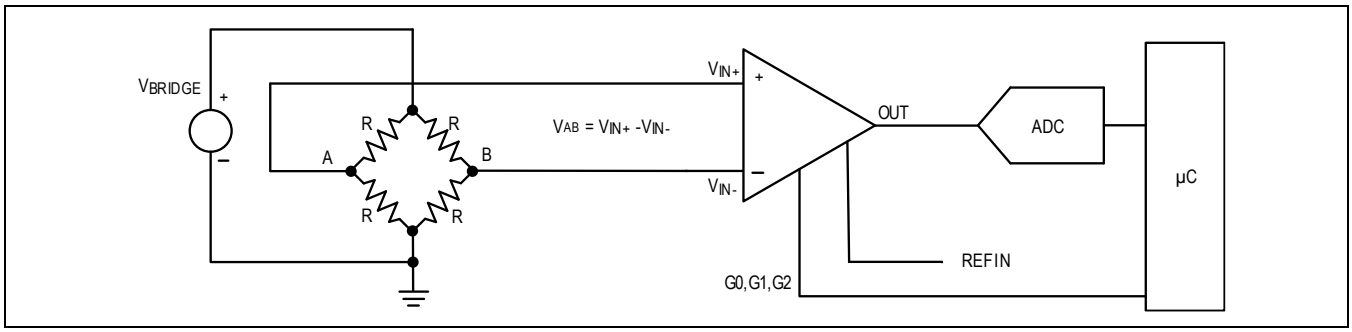



*Figure 3. Strain Gauge Connection to MAX41400*

### PT100 Application

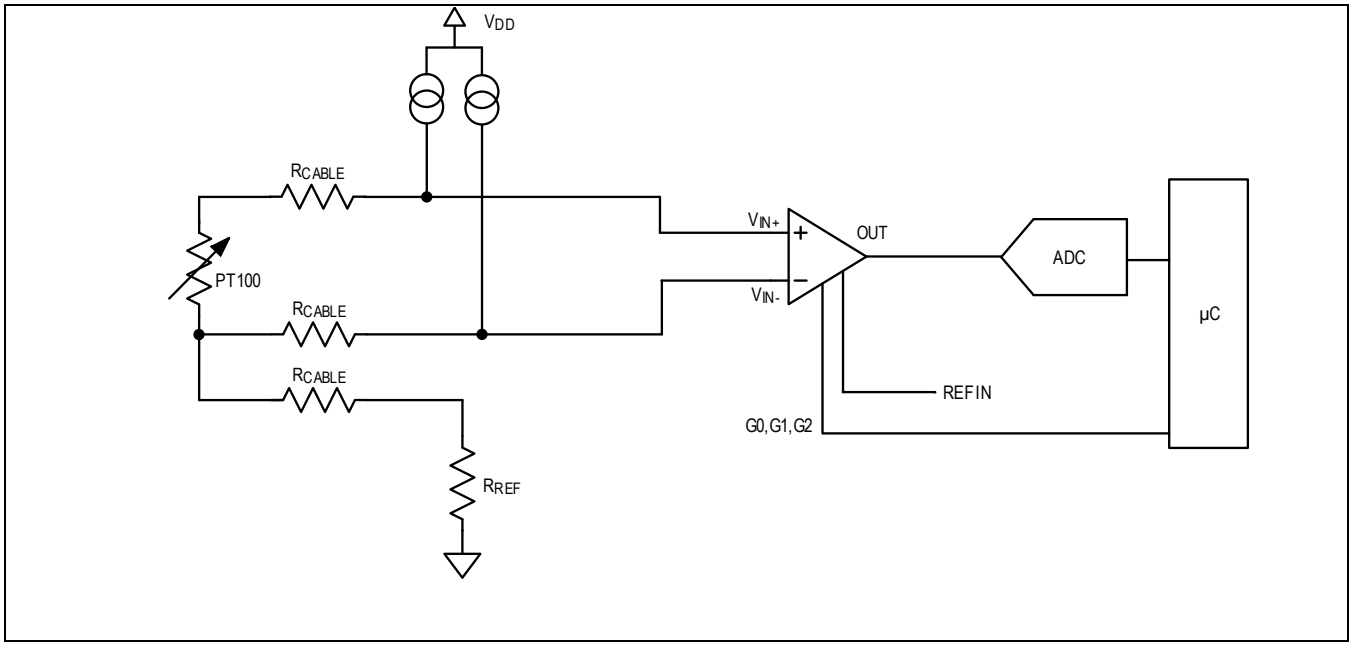



*Figure 4. Three-Wire PT100 Sensing Circuit*

## Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE | TOP MARKING |
|---|---|---|---|
| MAX41400ANL+ | -40°C to +125°C | 9 WLP | +AAS |
| MAX41400ANL+T | -40°C to +125°C | 9 WLP | +AAS |
| MAX41400ATB+ | -40°C to +125°C | 10 TDFN | +AZN |
| MAX41400ATB+T | -40°C to +125°C | 10 TDFN | +AZN |

*+ Denotes a lead(Pb)-free/RoHS-compliant package.*

*T = Tape-and-reel.*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 10/20 | Release for intro | — |
| 1 | 1/21 | Updated Electrical Characteristics table, Typical Operating Characteristics | 8, 11, 12 |
| 2 | 7/21 | Updated Benefits and Features, Electrical Characteristics table, Typical Operating Characteristics | 1, 8, 9, 12 |
| 3 | 7/24 | Added gain test conditions for CMRR and PSRR and updated gain error spec in *Electrical Characteristics* table, updated *Ordering Information* | 4, 17 |