

## 2.5V to 5.5V, 5A Reversible Buck/Boost Regulator for Backup Applications

**MAX38890**

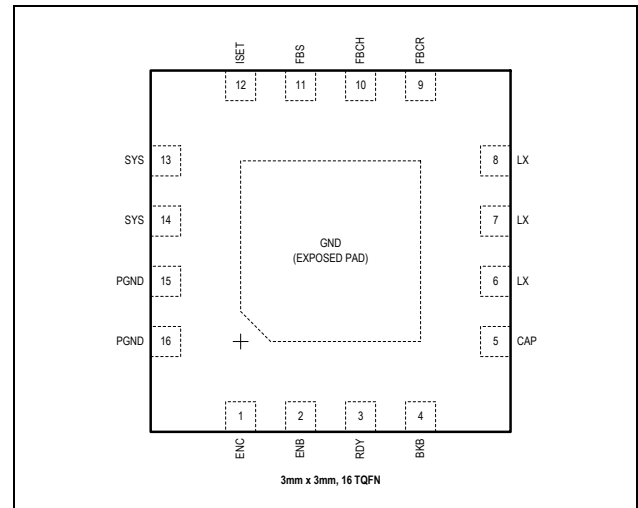
### Product Highlights

- 2.5V to 5.5V System Output Voltage Range
- 0.5V to 5.5V Supercapacitor Voltage Range
- $\pm 1\%$  Threshold Accuracy
- 2.5% Hysteresis between Backup and Charging
- 1A to 5A Peak Inductor Current Limit
  - Peak Inductor Current Is Pin-Programmable over 1A to 5A through External Resistor
- 94% Peak Efficiency, Charging or Discharging Mode
- 4 $\mu$ A Quiescent Current in Ready State
  - After Supercapacitor Is Charged, Draws only 4 $\mu$ A of Quiescent Current
- Ready and Backup State Outputs
  - RDY and BKB Flags Provide Real-Time Status to System
- 3mm x 3mm, 16-Pin TQFN Package

### Key Applications

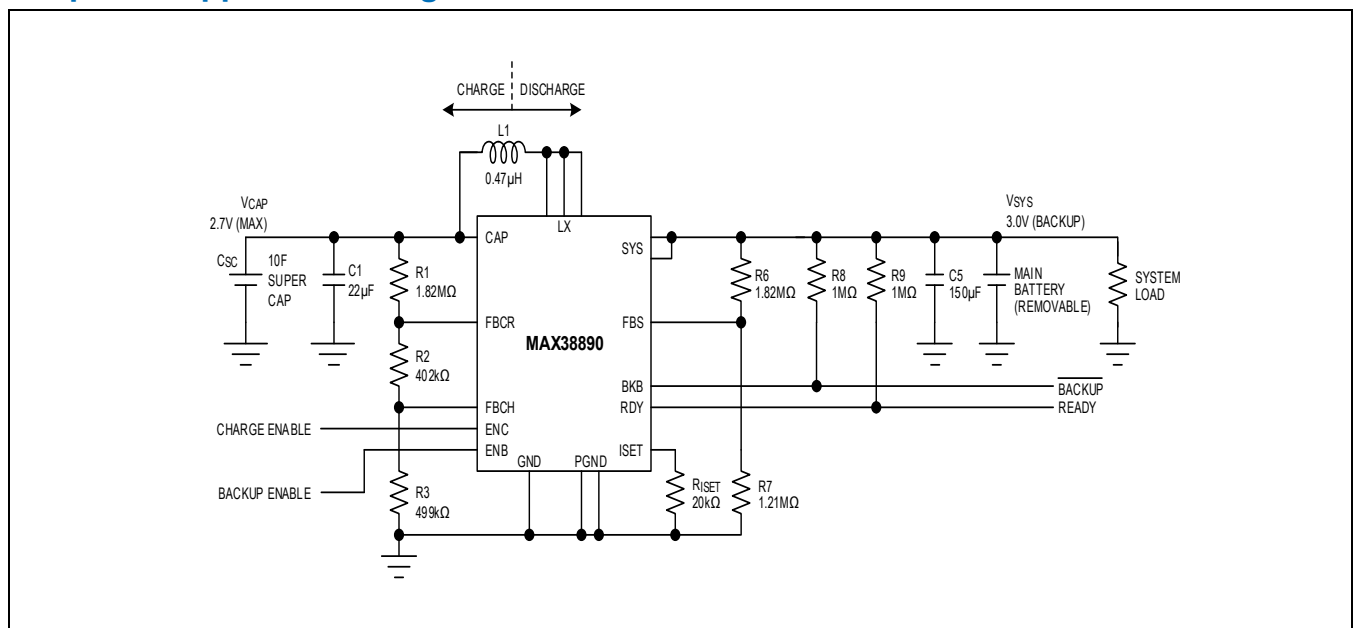
- Handheld Industrial Equipment
- Portable Devices/Computers with Removable Battery
- Industrial Sensor and Actuators
- Aftermarket Automotive Tracking

### Pin Configuration



[Ordering Information](#) appears at end of data sheet.

### Simplified Application Diagram



## Absolute Maximum Ratings

CAP, ENB, ENC, LX to GND ..... -0.3V to +6V  
 SYS, BKB, RDY to GND ..... -0.3V to +6V  
 FBCH, FBCT to GND ..... -0.3V to CAP + 0.3V  
 FBS, ISET to GND ..... -0.3V to SYS + 0.3V  
 PGND to GND ..... -0.3V to +0.3V  
 Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ , TQFN,  
 derate 23.1mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) ..... 1847.6mW

Operating Temperature Range .....  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Storage Temperature Range .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Maximum Junction Temperature .....  $+150^\circ\text{C}$   
 Lead Temperature (soldering, 10s) .....  $+300^\circ\text{C}$   
 Soldering Temperature (reflow) .....  $+260^\circ\text{C}$   
 LX RMS Current .....  $\pm 5.0\text{A}_{\text{RMS}}$   
 Output Short-Circuit Duration ..... Continuous

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

### TQFN

Package Code	T1633+5C
Outline Number	<a href="#">21-0136</a>
Land Pattern Number	<a href="#">90-0032</a>
<b>THERMAL RESISTANCE, FOUR-LAYER BOARD</b>	
Junction to Ambient ( $\theta_{JA}$ )	43.3 $^\circ\text{C}/\text{W}$
Junction to Case ( $\theta_{JC}$ )	4 $^\circ\text{C}/\text{W}$

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

(V<sub>SYS</sub> = 3.7V, V<sub>CAP</sub> = 2.8V, T<sub>J</sub> = -40°C to +125°C (typical values at T<sub>J</sub> = +25°C), circuit of [Figure 1](#), unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYS Voltage Range	V <sub>SYS</sub>	Guaranteed by LX peak backup current and SYS shutdown current		2.5		5.5	V
CAP Voltage Range	V <sub>CAP</sub>	Guaranteed by maximum on-time and CAP shutdown current		0.5		5.5	V
SYS Shutdown Current	I <sub>SYS_SD</sub>	V <sub>SYS</sub> = 5.5V, V <sub>ENC</sub> = V <sub>ENB</sub> = 0V	T <sub>A</sub> = +25°C	0.010		1	μA
			T <sub>A</sub> = +125°C		0.46		
SYS Ready Supply Current	I <sub>SYS_RDY</sub>	V <sub>FBS</sub> = 1.3V, V <sub>FBCH</sub> = 0.515V, V <sub>FBCR</sub> = 0.6V	T <sub>A</sub> = +25°C	4.5		8	μA
			T <sub>A</sub> = +125°C		8		
SYS Backup Supply Current	I <sub>SYS_BU</sub>	V <sub>FBS</sub> = 1.212V, V <sub>FBCH</sub> = 0.5V, V <sub>FBCR</sub> = 0.6V			75	150	μA
CAP Shutdown Current	I <sub>CAP_SD</sub>	V <sub>CAP</sub> = 5.5V, V <sub>ENC</sub> = V <sub>ENB</sub> = 0V	T <sub>A</sub> = +25°C	0.01		1	μA
			T <sub>A</sub> = +125°C		0.2		
System Undervoltage Threshold	V <sub>UVLOF</sub>	V <sub>SYS</sub> falling, 100mV typical hysteresis, V <sub>CAP</sub> = 0V		2.1	2.2	2.3	V
FBS Backup Voltage	V <sub>FBS_BU</sub>	V <sub>FBS</sub> rising, when discharging stops		1.188	1.2	1.212	V
FBS Charging Threshold	V <sub>FBS_CHG</sub>	From V <sub>FBS</sub> backup voltage, when charging begins		2	2.5	3	%
FBCH Threshold	V <sub>TH_FBCH</sub>	V <sub>FBCH</sub> rising, when charging stops; 10mV typical hysteresis		0.495	0.5	0.505	V
FBCR Threshold	V <sub>TH_FBCR</sub>	V <sub>FBCR</sub> rising, when RDY releases; 10mV typical hysteresis		0.495	0.5	0.505	V
ENC Input Threshold	V <sub>IL</sub>	V <sub>FBS</sub> = 1.3V, V <sub>FBCH</sub> = 0.4V, when LX switching	V <sub>ENC</sub> rising	600	850		mV
	V <sub>IH</sub>	V <sub>FBS</sub> = 1.3V, V <sub>FBCH</sub> = 0.4V, when LX switching	V <sub>ENC</sub> falling		950	1200	
ENB Input Threshold	V <sub>IL</sub>	V <sub>FBS</sub> = 1.1V, V <sub>FBCH</sub> = 0.4V, when LX switching	V <sub>ENB</sub> rising	600	850		mV
	V <sub>IH</sub>	V <sub>FBS</sub> = 1.1V, V <sub>FBCH</sub> = 0.4V, when LX switching	V <sub>ENB</sub> falling		950	1200	
ISET Resistor Range	R <sub>ISET</sub>	Guaranteed by LX peak current limits		20		100	kΩ
LX Switching Frequency	F <sub>SW</sub>	V <sub>CAP</sub> = 1.5V, I <sub>SYS</sub> = 1A			1.2		MHz
LX Peak Back-Up Current Limit	I <sub>LX_BU</sub>	Circuit of Figure 1, V <sub>CAP</sub> = 2V, V <sub>SYS</sub> = 2.5V (Note 1)	R <sub>ISET</sub> = 20kΩ	4	5	6	A
	I <sub>LX_BU</sub>	Circuit of Figure 1, V <sub>CAP</sub> = 2V, V <sub>SYS</sub> = 2.5V (Note 1)	R <sub>ISET</sub> = 100kΩ		1		

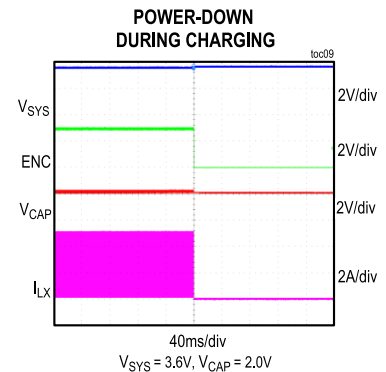
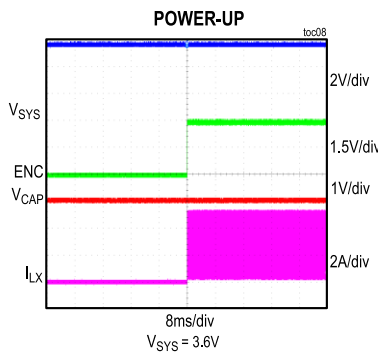
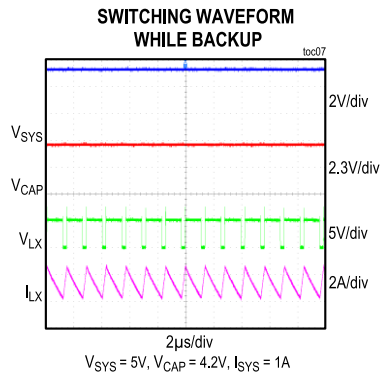
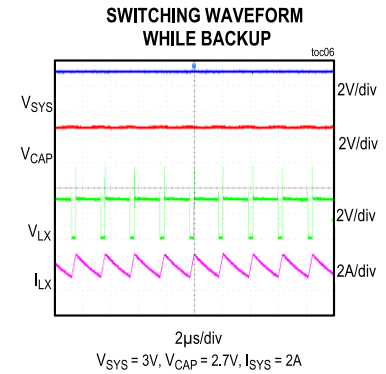
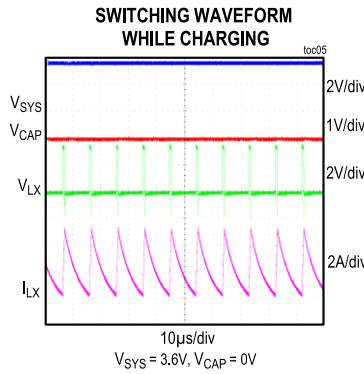
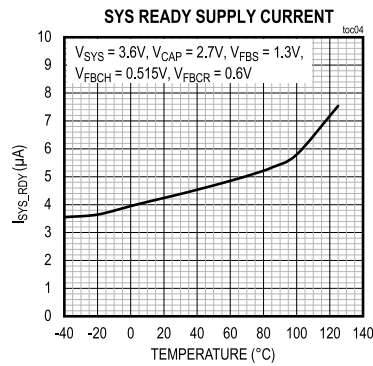
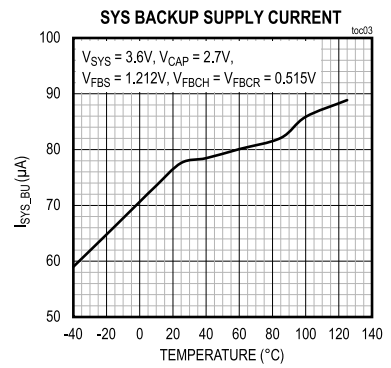
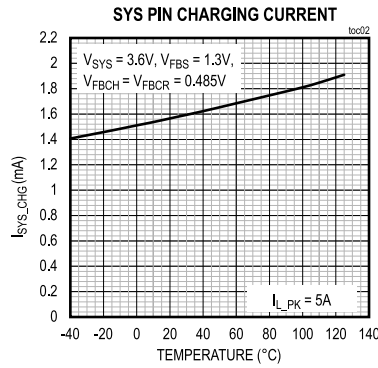
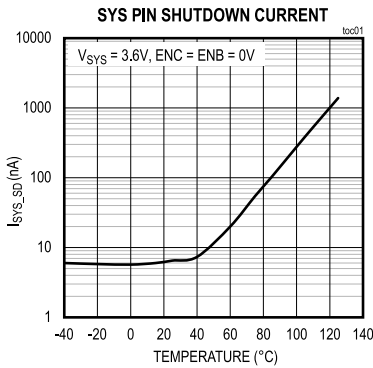
(V<sub>SYS</sub> = 3.7V, V<sub>CAP</sub> = 2.8V, T<sub>J</sub> = -40°C to +125°C (typical values at T<sub>J</sub> = +25°C), circuit of [Figure 1](#), unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX Peak Charge Current Limit (Note 1)	I <sub>LX_CHG</sub>	Circuit of Figure 1, V <sub>SYS</sub> = 3.7V, V <sub>CAP</sub> = 2V	R <sub>ISET</sub> = 20kΩ	4	5	6	A
			R <sub>ISET</sub> = 100kΩ		1		
Feedback Input Bias Current	I <sub>FBS</sub> , I <sub>FBCH</sub> , I <sub>FBCR</sub>	V <sub>FBS</sub> = 1.2V, V <sub>FBCH</sub> = V <sub>FBCR</sub> = 0.5V	T <sub>A</sub> = +25°C	-0.1	0.01	+0.1	μA
			T <sub>A</sub> = +125°C		0.01		
Enable Input Leakage Current	I <sub>ENC</sub> , I <sub>ENB</sub>	0V < V <sub>ENC</sub> , V <sub>ENB</sub> < 5.5V	T <sub>A</sub> = +25°C	-1	0.004	1	μA
			T <sub>A</sub> = +125°C		0.01		
LX Low-Side FET Resistance	R <sub>LOW</sub>	V <sub>LX</sub> switched to 0V			42	84	mΩ
LX High-Side FET Resistance	R <sub>HIGH</sub>	V <sub>LX</sub> switched to V <sub>SYS</sub>			57	114	mΩ
LX Leakage Current	I <sub>LX_LKG</sub>	V <sub>ENC</sub> = V <sub>ENB</sub> = 0V, V <sub>SYS</sub> = 5.5V, V <sub>LX</sub> = 0V to 5.5V	T <sub>A</sub> = +25°C	-1	0.01	1	μA
			T <sub>A</sub> = +125°C		0.26		
Maximum On-Time	t <sub>ON</sub>	Typical Application Circuit, V <sub>SYS</sub> = 2.9V	V <sub>CAP</sub> = 2V	320	400	480	ns
			V <sub>CAP</sub> = 1.2V		570		
Minimum Off-Time	t <sub>OFF</sub>	Backup mode, V <sub>FBS</sub> = 1.164V		80	100	120	ns
Maximum Duty Cycle	Duty <sub>MAX</sub>	V <sub>CAP</sub> = 0.5V		90	95		%
Overtemperature Lockout Threshold	T <sub>OTLO</sub>	T <sub>J</sub> rising, 15°C typical hysteresis			165		°C
Logic Output Leakage High	I <sub>BKB_H</sub>	V <sub>BKB</sub> = 5.5V, V <sub>RDY</sub> = 5.5V	T <sub>A</sub> = +25°C	-1	0.001	+1	μA
	I <sub>RDY_H</sub>	V <sub>BKB</sub> = 5.5V, V <sub>RDY</sub> = 5.5V	T <sub>A</sub> = +125°C		0.01		
Logic Output Voltage Low	V <sub>BKB_L</sub> , V <sub>RDY_L</sub>	I <sub>BKB</sub> = 10mA, I <sub>RDY</sub> = 10mA			0.1	0.4	V
High-Side FET Zero-Crossing	I <sub>ZXP</sub>	Circuit of Figure 1, V <sub>SYS</sub> = 2.9V, V <sub>CAP</sub> = 2V (Note 1)			60		mA
Low-Side FET Zero-Crossing	I <sub>ZXN</sub>	Circuit of Figure 1, V <sub>SYS</sub> = 3.7V, V <sub>CAP</sub> = 2V (Note 1)			180		mA

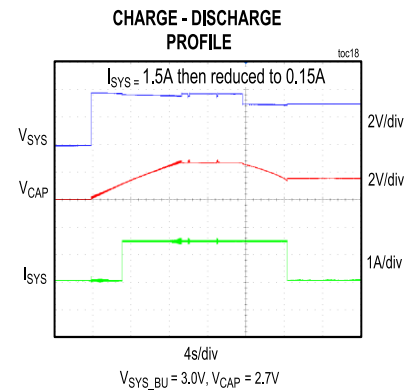
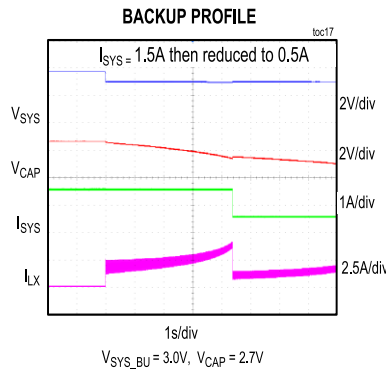
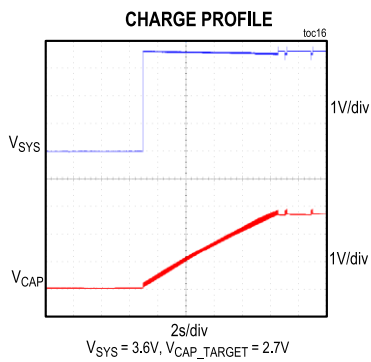
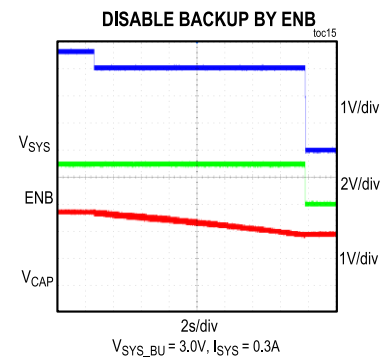
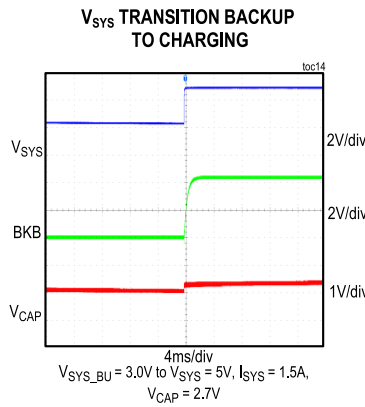
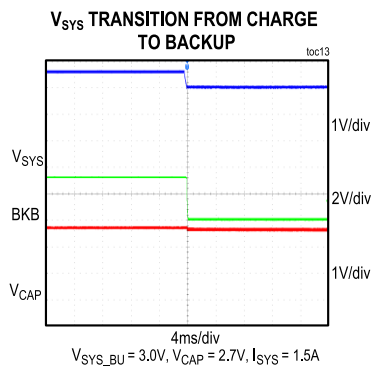
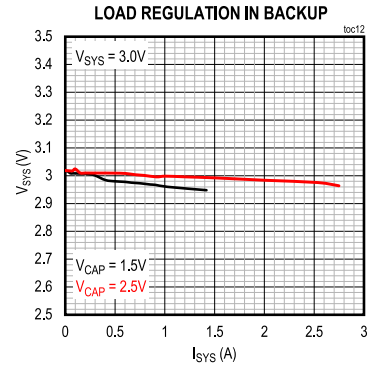
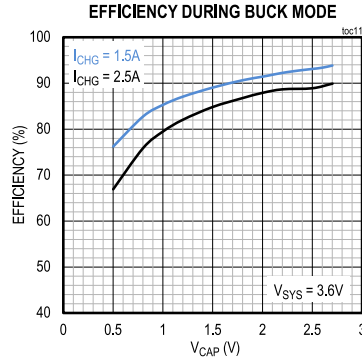
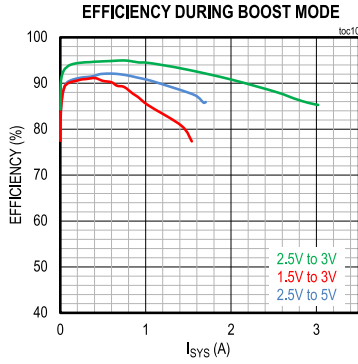
**Note 1:** DC measurement, actual inductor current accuracy in the circuit is affected by the propagation delay time.

Typical Operating Characteristics

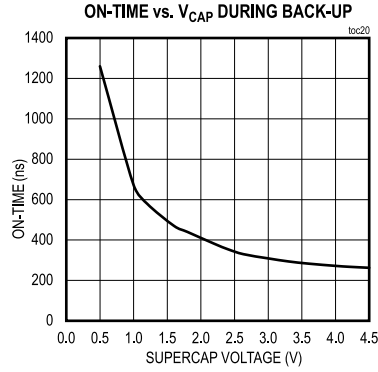
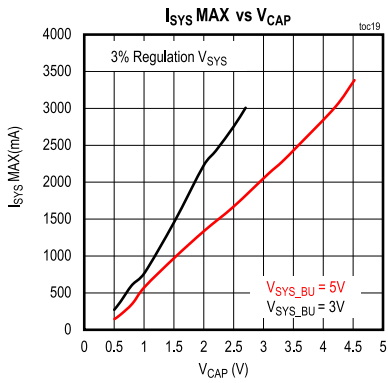
( $V_{SYS} = 3.6V$ ,  $V_{CAP} = 2.7V$ ,  $C_{SYS} = 150\mu F$ ,  $C_{CAP} = 22\mu F + 10F$ ,  $L = 0.47\mu H$ , unless otherwise noted.)



( $V_{SYS} = 3.6V$ ,  $V_{CAP} = 2.7V$ ,  $C_{SYS} = 150\mu F$ ,  $C_{CAP} = 22\mu F + 10F$ ,  $L = 0.47\mu H$ , unless otherwise noted.)

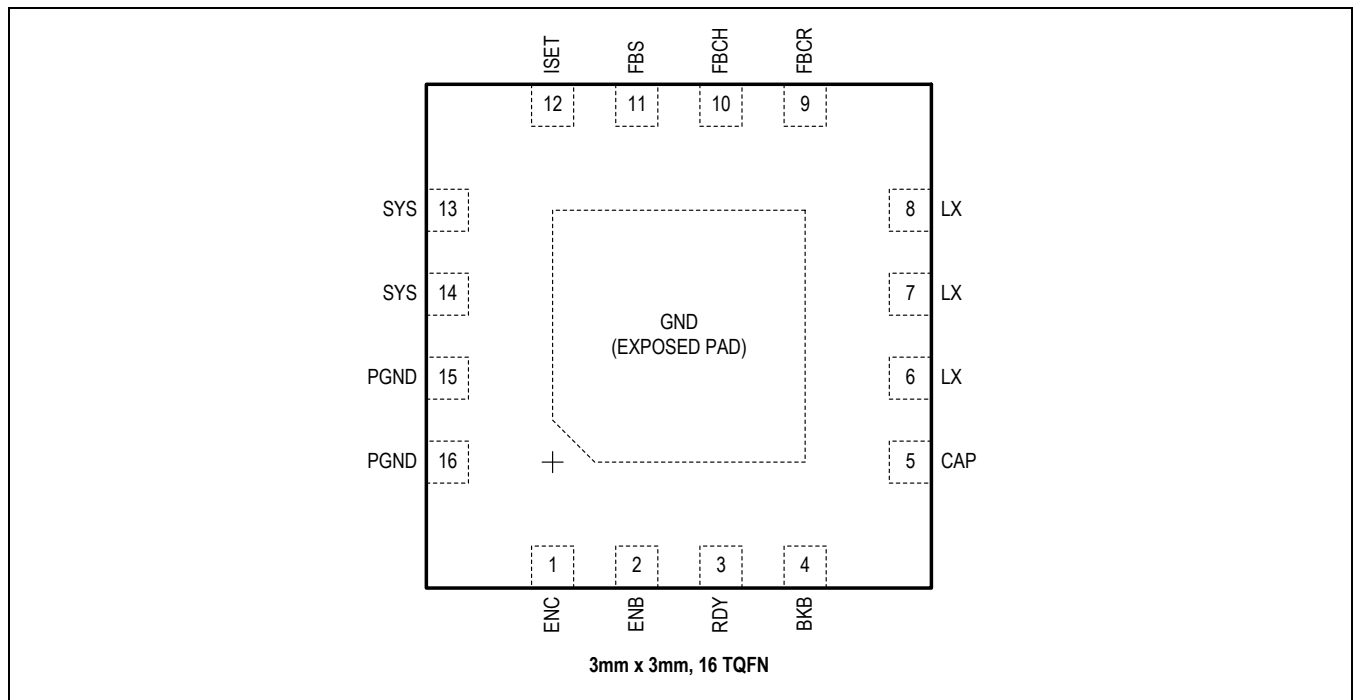


( $V_{SYS} = 3.6V$ ,  $V_{CAP} = 2.7V$ ,  $C_{SYS} = 150\mu F$ ,  $C_{CAP} = 22\mu F + 10F$ ,  $L = 0.47\mu H$ , unless otherwise noted.)



### Pin Configuration

#### 16 TQFN

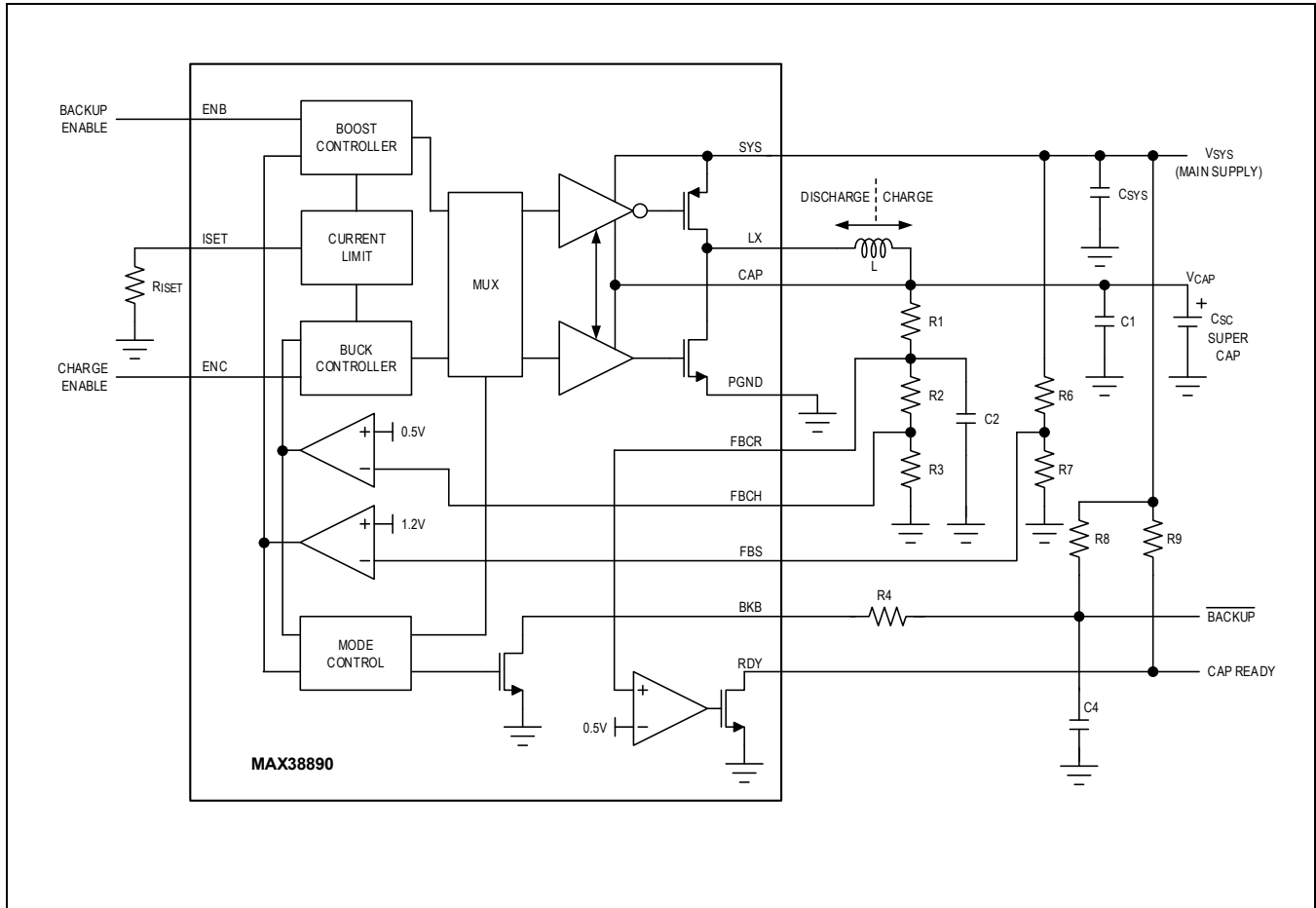


## Pin Descriptions

PIN	NAME	FUNCTION
1	ENC	Charger Enable Input. Drive this pin high to enable charging of the supercapacitor while $V_{SYS}$ is above the charging threshold. Drive this pin low to disable charging. If not driven, tie this pin to the SYS rail.
2	ENB	Backup Enable Input. Drive this pin high to enable system backup when $V_{SYS}$ drops below the backup threshold. Drive this pin low to disable backup. If not driven, tie this pin to the SYS rail.
3	RDY	Ready Status Pin. Connect a pullup resistor from RDY to a logic supply. $V_{RDY}$ will be pulled low when $V_{FBCR}$ is below 0.5V and released when it is above 0.5V. $V_{RDY}$ is pulled low when $V_{ENC}$ and $V_{ENB}$ are both low.
4	BKB	Backup Status Pin. Connect a pullup resistor from BKB to a logic supply. $V_{BKB}$ will be pulled low when $V_{FBS}$ is regulating at 1.2V and released when it is above 1.23V. $V_{BKB}$ is released high when $V_{ENC}$ and $V_{ENB}$ are both low. It is recommended to have an RC filter from BKB to ground as shown in <a href="#">Figure 1</a> for smooth transition of BKB flag.
5	CAP	Supercapacitor. Connect to a supercapacitor rated between 0.8V to 5V. Put a high-frequency capacitor of 22 $\mu$ F close to the CAP pin.
6, 7, 8	LX	Inductor Switching Node. Connect a 0.47 $\mu$ H inductor from LX to CAP. Keep this switching node separated from feedback signal nodes FBS, FBCH, and FBCR as much as possible.
9	FBCR	Supercapacitor Ready Input. RDY will go high when $V_{FBCR}$ reaches 0.5V. It is recommended to place 0.47 $\mu$ F capacitor from FBCR to ground for smooth transition of the RDY flag.
10	FBCH	Supercapacitor Feedback Input. Connect a resistor-divider from CAP to FBCH to GND to set the supercapacitor maximum charging voltage.
11	FBS	System Feedback Input. Connect a resistor-divider from SYS to FBS to GND to set the system backup operating voltage. When $V_{FBS}$ is >102.5% of $V_{FBS\_BU}$ , the supercapacitor will be charged from SYS.
12	ISET	Charge/Discharge Current Select. During charging, the average supercapacitor current ( $I_{CAP\_CHG}$ ) is set to $I_{CAP\_CHG} = 2.5A \times (20k\Omega/R_{ISET})$ . During backup, $V_{SYS}$ is regulated through the boost regulator with a peak inductor current of $I_{LX\_BU} = 5A \times (20k\Omega/R_{ISET})$
13, 14	SYS	System Supply. Connect to the system supply and bypass with 2x47 $\mu$ F and 2x22 $\mu$ F ceramic capacitors to PGND. In addition, place a high-frequency filter capacitor of 1 $\mu$ F close to the part across the SYS and PGND pins.
15, 16	PGND	Power Ground.
EP	GND	Analog Ground. Connect the exposed pad to the ground plane with excellent thermal conduction to ambient temperature to avoid overtemperature.



## Functional Diagram



## Detailed Description

The MAX38890 is a flexible storage capacitor or capacitor bank backup regulator transferring power efficiently between a storage element and a system supply rail.

When the main supply is present and its voltage is above the minimum threshold system supply voltage, the regulator operates in charging mode and charges the storage element with a maximum 5A peak, 2.5A average inductor current. Once the storage element is charged, the circuit draws only 4 $\mu$ A of current while maintaining the storage element in its ready state. The supercapacitor needs to be fully charged to enable backup operation.

When the main supply is removed, the regulator prevents the system from dropping below the set system backup operating voltage, boosting the supercapacitor voltage to a regulated  $V_{SYS}$  by discharging the storage element with a maximum 5A peak inductor current. During this backup mode of operation, the MAX38890 utilizes an adaptive on-time, current-limited, pulse-frequency-modulation (PFM) control scheme. Once the MAX38890 is in backup mode, the BKB flag is low.

The external pins allow various settings such as maximum supercapacitor voltage, system backup voltage ( $V_{SYS}$ ), and peak inductor charge and discharge current.

The MAX38890 implements a True Shutdown™ feature, disconnecting SYS from CAP as well as protecting against a SYS short if  $V_{CAP} > V_{SYS}$ .

Charging and backup can be disabled by keeping the ENC and ENB pins low, respectively. The backup system status can be monitored through two status outputs: the RDY flag that indicates when the supercapacitor is charged and the BKB flag that indicates when backup operation is occurring.

## Application Circuits

The typical application of the MAX38890 is shown in [Figure 1](#).

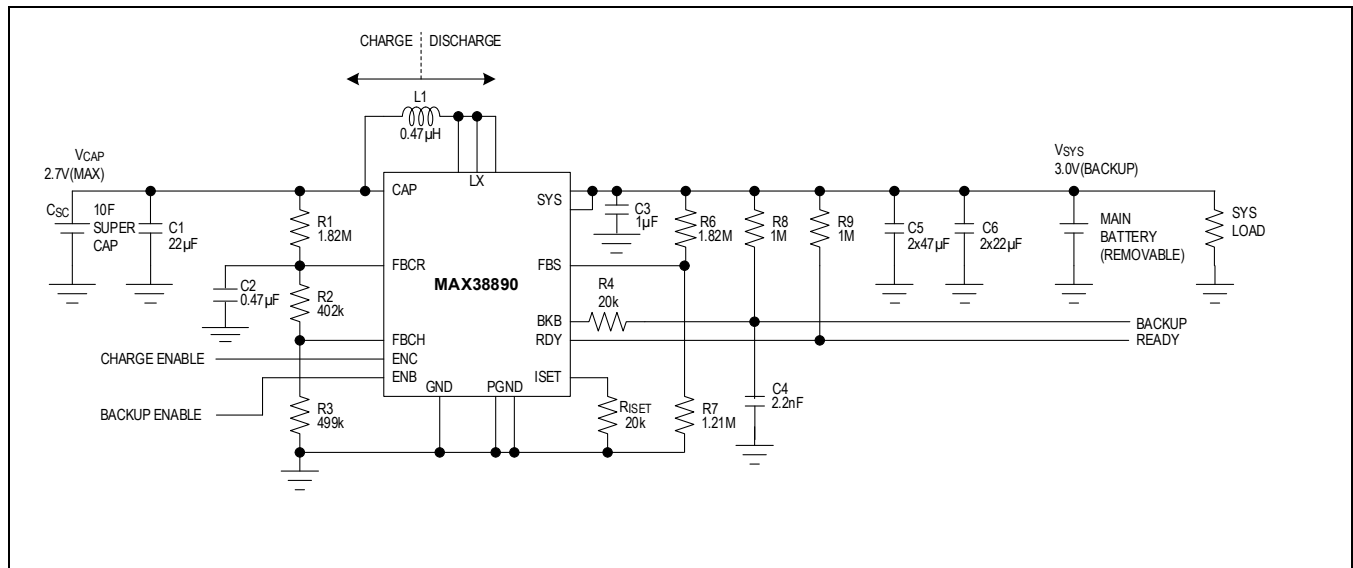


Figure 1. Application Circuit

## Supercapacitor Voltage Configuration

The maximum supercapacitor voltage ( $V_{CAP\_MAX}$ ) during charging is determined by the resistor-divider driving the FBCH pin. When  $V_{FBCH}$  reaches 0.5V, further charging of the supercapacitor is halted. The threshold has a 2.5% (12.5mV) hysteresis. To keep the ready power drawn low, keep the quiescent current in the resistor-divider low by setting the resistor from FBCH to GND to 500k $\Omega$ . The resistance from CAP to FBCH ( $R_1 + R_2$ ) can then be determined by the standard equation:

$$R_1 + R_2 = R_3 \times \left( \frac{V_{CAP\_MAX}}{0.5V} - 1 \right)$$

Selecting  $V_{CAP\_MAX} = 2.7V$  and  $R_3 = 499k\Omega$ :

$$R_1 + R_2 \approx 2.2M\Omega$$

The RDY pin is a flag that goes high when the supercapacitor has crossed a user-defined voltage. Like the FBCH input, the FBCR pin is driven from CAP through a resistor-divider. To save quiescent current, the FBCR and FBCH resistor-dividers can be combined using a three-resistor-divider string, as shown in [Figure 1](#).

Total resistance from CAP to GND ( $R_T$ ) is:

$$R_T = R_1 + R_2 + R_3 = 2.2M\Omega + 499k\Omega \approx 2.7M\Omega$$

RDY goes high when  $V_{FBCR}$  is greater than 0.5V.

Assuming RDY to go high when  $V_{CAP}$  reaches 1.5V:

$$V_{CAP\_RDY} = 1.5V$$

$$R_3 = 499k\Omega$$

$$R_2 = R_T \times \left( \frac{0.5V}{V_{CAP\_RDY}} \right) - R_3 = 2.7M\Omega \times \left( \frac{0.5V}{1.5V} \right) - 499k\Omega = 401k\Omega$$

Selecting  $R_2 = 402\text{k}\Omega$ :

$$R_1 = R_T - R_2 - R_3 = 2.7\text{M}\Omega - 402\text{k}\Omega - 499\text{k}\Omega = 1.8\text{M}\Omega$$

Select  $R_2 = 1.82\text{M}\Omega$  for fine-tuning on the bench.

During backup, the supercapacitor voltage discharges and the boost converter automatically adjusts its duty cycle to regulate  $V_{\text{SYS}}$ . When  $V_{\text{SYS}}$  drops below UVLO threshold ( $V_{\text{UVLOF}}$ ) or  $V_{\text{FBCH}}$  drops to 10% of the FBCH threshold voltage ( $V_{\text{TH\_FBCH}}$ ), the boost regulator stops delivering load current and the supercapacitor voltage is preserved with only the current from the resistor-divider discharging the supercapacitor further.

### System Voltage Configuration

The backup system voltage is determined by a resistor-divider driving the FBS pin. Set the system backup voltage using a resistor-divider from SYS to FBS to GND. When  $V_{\text{FBS}}$  is above 1.23V, the DC-DC regulator draws power from the main battery through the SYS pin to charge the supercapacitor to the maximum voltage set by FBCH and be ready for backup. The peak charging current can be programmed to up to 5A, max. When the main battery is removed and  $V_{\text{FBS}}$  drops to 1.2V, the DC-DC regulator draws power from the supercapacitor and regulates the SYS pin to the programmed backup voltage with the programmed peak inductor current, which is a maximum of 5A.

In order to reduce the current flowing through the resistor-divider, select high-value resistors.

To set system the backup voltage to 3.0V, select the bottom resistor ( $R_7$ ) to 1.21M $\Omega$ . The top resistor value can be calculated by the following equation:

$$R_6 = \left( 3.0 \times \frac{R_7}{1.2} \right) - R_7$$

$$R_6 = \left( 3.0 \times \frac{1.21\text{M}\Omega}{1.2} \right) - 1.21\text{M}\Omega = 1.815\text{M}\Omega$$

Select  $R_6 = 1.82\text{M}\Omega$  for fine-tuning on the bench.

### Charge/Discharge Current Configuration

The MAX38890 current configuration pin, ISET, gives the user the ability to optimize the efficiency around the maximum load requirements of the system during backup. A larger current setting allows the supercapacitor to be discharged to a lower voltage for a given load during backup.

A single resistor sets both the charging and backup current.

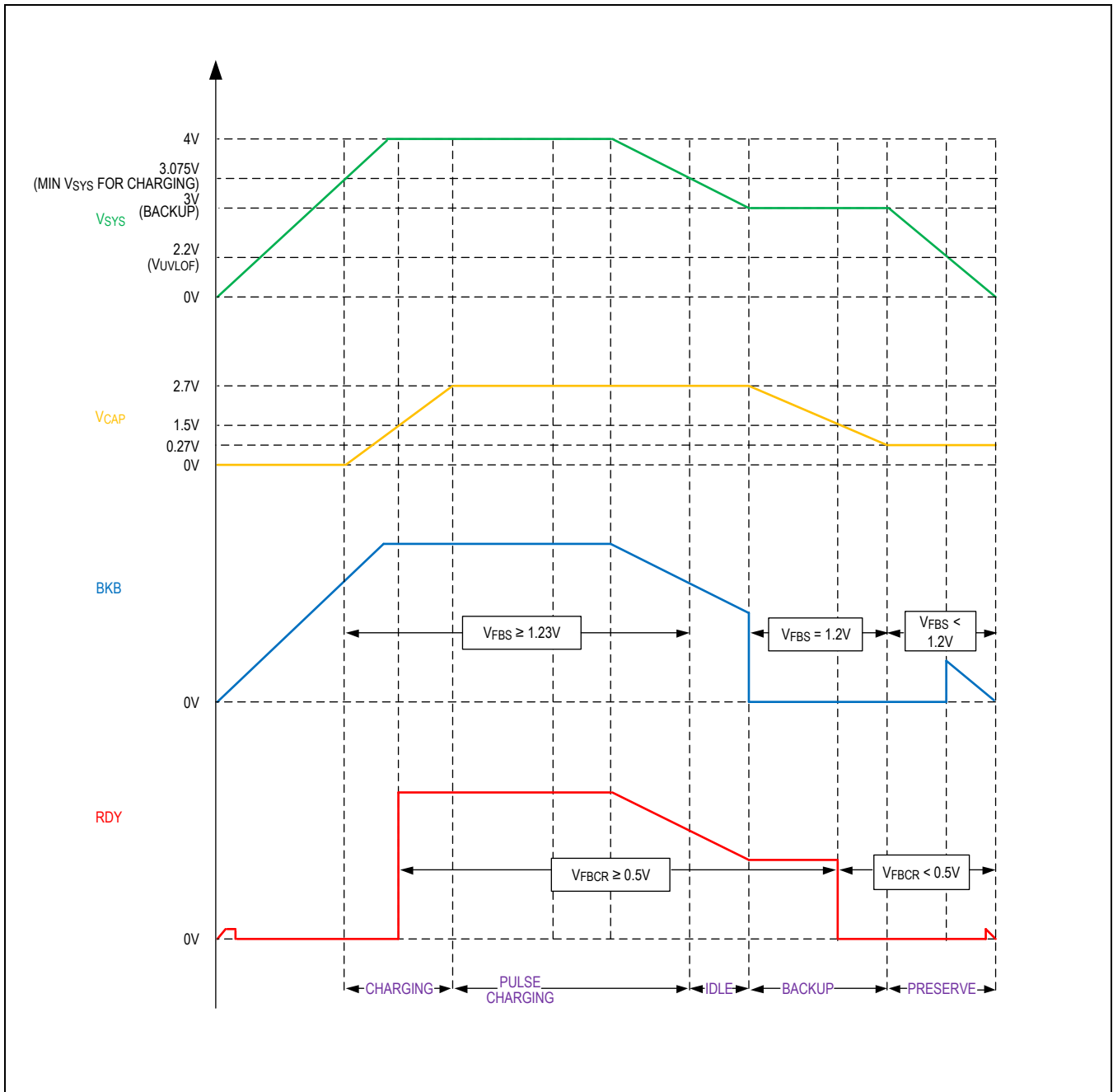


Figure 2. System Waveforms

**Charging**

Supercapacitor charging current and discharging current is determined by the same resistor,  $R_{ISET}$ . The buck regulator operates in forced discontinuous conduction mode (DCM) until the supercapacitor gets fully charged.

Average charging current ( $I_{CAP\_CHG}$ ) is determined by:

$$I_{CAP\_CHG} = 2.5A \times \left( \frac{20k\Omega}{R_{ISET}} \right)$$

where  $R_{ISET}$  can be selected from 100kΩ to 20kΩ, and  $I_{CAP\_CHG}$  varies from 0.5A to 2.5A, respectively. Since charging current is efficiently drawn through a buck regulator, the average charging current from SYS ( $I_{SYS\_CHG}$ ) is:

$$I_{SYS\_CHG} = 2.5A \times \left( \frac{20k\Omega}{R_{ISET}} \right) \times \left( \frac{V_{CAP}}{V_{SYS}} \right) \times \left( \frac{1}{(\text{charging efficiency})} \right)$$

Peak charging current ( $I_{LX\_CHG}$ )

$$I_{LX\_CHG} = 5A \times \left( \frac{20k\Omega}{R_{ISET}} \right)$$

When the supercapacitor voltage reaches its maximum voltage as determined by the FBCH threshold, the forced DCM of the charging stops. After this, only pulse charging takes place.

**Backup**

The peak inductor current limit during backup operation can be set by the same  $R_{ISET}$  resistor using the below equation:

$$I_{LX\_BU} = 5A \times \left( \frac{20k\Omega}{R_{ISET}} \right)$$

where  $R_{ISET}$  can be selected from 100kΩ to 20kΩ, and  $I_{LX\_BU}$  varies from 1A to 5A, respectively.

During backup operation, the MAX38890 regulator regulates the system voltage to the target backup voltage and as a result, the voltage on the supercapacitor reduces from the maximum charged voltage. For a given system load in backup ( $I_{SYS\_BU}$ ), the minimum supercapacitor voltage ( $V_{CAP\_MIN}$ ) needed to support the load can be calculated as:

$$V_{CAP\_MIN} = V_{SYS\_MIN} \times \left[ \frac{I_{SYS\_BU}}{I_{LX\_BU} - (0.5 \times dILX)} \right] \times \left( \frac{1}{(\text{backup efficiency})} \right)$$

For a system backup voltage of 3.0V and 1.5A system load, assuming the system backup is required until the minimum supercapacitor voltage of 1.5V and system efficiency of 75%.

Let us calculate the inductor current ripple based on on-time for a given minimum super capacitor voltage. From the on-time vs. supercapacitor voltage TOC, the voltage across inductor during on-time is given as below:

$$V_L = L \times \left[ \frac{dILX}{Ton} \right] = V_{cap}$$

$$dILX = V_{cap} \times \left[ \frac{Ton}{L} \right] = \frac{1.5 \times 480ns}{470nH} = 1.53A$$

The actual minimum supercapacitor voltage to backup 3V with 1.5A system load is calculated as below:

$$V_{CAP\_MIN} = 3V \times \left[ \frac{1.5A}{5A - (0.5 \times 1.53)} \right] \times \left( \frac{1}{75\%} \right) = 1.42V$$

For a system backup voltage of 5.0V and 0.5A system load, assuming the system backup is required until the minimum supercapacitor voltage of 1.0V and system efficiency of 75%.

The inductor ripple current is calculated as below:

$$dILX = V_{cap} \times \left[ \frac{Ton}{L} \right] = \frac{1.0 \times 636ns}{470nH} = 1.35A$$

The actual minimum supercapacitor voltage to backup 5V with 0.5A system load is calculated as below:

$$V_{CAP\_MIN} = 5V \times \left[ \frac{0.5A}{5A - (0.5 \times 1.35)} \right] \times \left( \frac{1}{75\%} \right) = 0.77V$$

It is not recommended to operate the MAX38890 below the calculated  $V_{CAP\_MIN}$  for a given load. This causes the inductor peak current to hit the current limit which resets the regulator. Once the part is reset, the system supply needs to be reapplied to the SYS rail for the MAX38890 to restart and charge the storage element to its programmed threshold, after which backup operation can be resumed. Refer to the TOC for backup profile of 3V system backup voltage and 1.5A system load.

To avoid the regulator resetting, it is recommended either to reduce the load current before the supercapacitor voltage reaches the  $V_{CAP\_MIN}$  level or the inductor peak current hits the set current limit.

## Applications Information

### Capacitor Selection

Capacitors at the SYS and CAP pins reduce current peaks and increase efficiency. Ceramic capacitors are recommended because they have the lowest equivalent series resistance (ESR), smallest size, and lowest cost. Choose an acceptable dielectric such as X5R where the ambient temperature is less than +85°C or X7R where the ambient temperature is less than +125°C. Due to the ceramic capacitor's capacitance derating at higher DC bias voltages, 2x47µF and 2x22µF ceramic capacitors are recommended at the SYS side and a 22µF ceramic capacitor at the CAP side for most applications. In addition, it is recommended to place a high-frequency filter capacitor of 1µF across the SYS and PGND pins as mentioned in the [PCB Layout Guidelines](#).

### Supercapacitor Selection

When the power source supplying the  $V_{SYS}$  voltage is removed, power to the output is provided by the MAX38890 operating in the backup or boost mode of operation using the supercapacitor as its source. In order to ensure that the supply voltage stays in regulation, the amount of power the supercapacitor can deliver at its minimal voltage should be greater than that required by the system. The MAX38890 presents a constant power load to the supercapacitor where smaller current is pulled out of the supercapacitor near its maximum  $V_{CAP}$  voltage. However, current drawn from the supercapacitor increases as it discharges to maintain constant power at the load. The amount of energy required in backup mode is the product of the constant backup power and time defined as backup time,  $T_{BACKUP}$ .

The amount of energy available in the supercapacitor ( $C_{SC}$ ) is calculated using the following formula:

$$E = \frac{1}{2} \times C_{SC} \times (V_{CAPMAX}^2 - V_{CAPMIN}^2) (J)$$

The amount of energy required to complete the backup equals to:

$$E = V_{SYS} \times I_{SYS} \times T_{BACKUP} (J)$$

where  $I_{SYS}$  is the system load during backup.

Since the energy required at the system side during the backup event comes from the available energy in the supercapacitor, assuming conversion efficiency  $\eta$  and the given  $T_{BACKUP}$ , the required  $C_{SCAP}$  is determined by the following equation:

$$C_{SC} = \frac{2 \times V_{SYS} \times I_{SYS} \times T_{BACKUP}}{[(V_{CAPMAX}^2 - V_{CAPMIN}^2) \times \eta]} (F)$$

For example, in the [Figure 1](#) application circuit, assuming a 1.5A system load and an average efficiency of 75%, the minimum value of the supercapacitor required for a 5s backup time is:

$$C_{SC} = \frac{2 \times 3.0V \times 1.5A \times 5s}{[(2.7V)^2 - (1.5V)^2] \times 0.75} = 12F$$

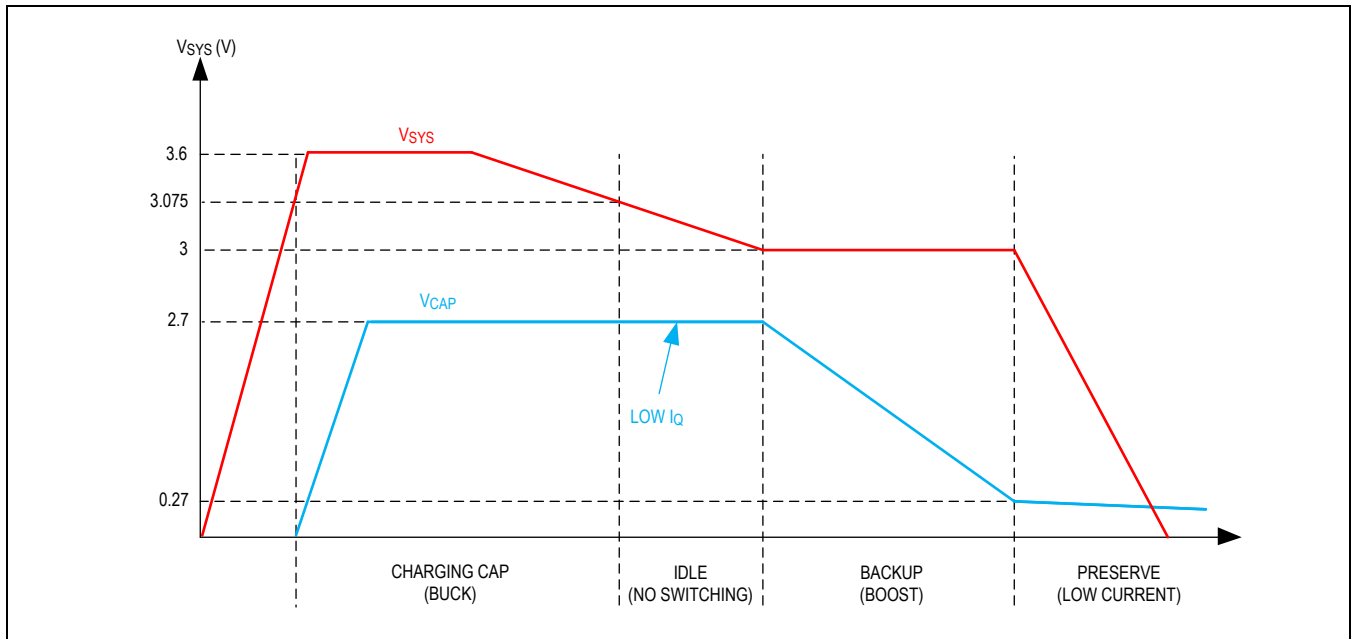


Figure 3. Charging/Discharging Waveforms

### Inductor Selection

The recommended inductor value for the MAX38890 is 0.47 $\mu$ H.

### Status Flags

The MAX38890 has two dedicated pins to report the device status to the host processor. Both of these output pins are open-drain type and require external pullup resistors. The recommended value for the pullup resistors is 1M $\Omega$ . The pins should be pulled up to the SYS rail.

#### BKB Flag

The BKB flag indicates that the converter is in backup mode, and it is low when the part is in backup mode, and  $V_{FBS}$  is regulating at 1.2V. This pin is high when  $V_{FBS}$  is above 1.23V. The BKB is high when  $V_{ENC}$  and  $V_{ENB}$  are both low.

#### RDY Flag

The RDY flag helps the external processor to detect that the supercapacitor is ready to back up the SYS voltage. The RDY flag is high when  $V_{FBCR} > 0.5V$  and low when  $V_{FBCR} < 0.5V$ . The RDY threshold can be set using the external resistor divider from the supercapacitor to GND.

### Enabling the Device

The MAX38890 has dedicated enable pins for both charging and backup modes. Both of the pins can either be driven individually by a digital signal, pulled up, or strapped to the SYS rail.

#### Charger Enable Input (ENC)

Drive this pin high to enable charging of the supercapacitor while  $V_{SYS}$  is above the charging threshold. Drive it low to disable charging and reduce quiescent current. The ENC voltage applied should be more than 950mV.

#### Backup Enable Input (ENB)

Drive this pin high to enable system backup when  $V_{SYS}$  drops below the backup threshold. Drive it low to disable backup and reduce quiescent current. The ENB voltage applied should be more than 950mV.

**PCB Layout Guidelines**

Minimize trace lengths to reduce parasitic capacitance, inductance and resistance, and radiated noise. Keep the main power path from SYS, LX, CAP, and PGND as tight and short as possible. Minimize the surface area used for LX since this is the noisiest node. It is recommended to place a filter capacitor close to the part across the SYS and GND pins to minimize voltage spikes on account of trace inductance, as shown in [Figure 4](#).

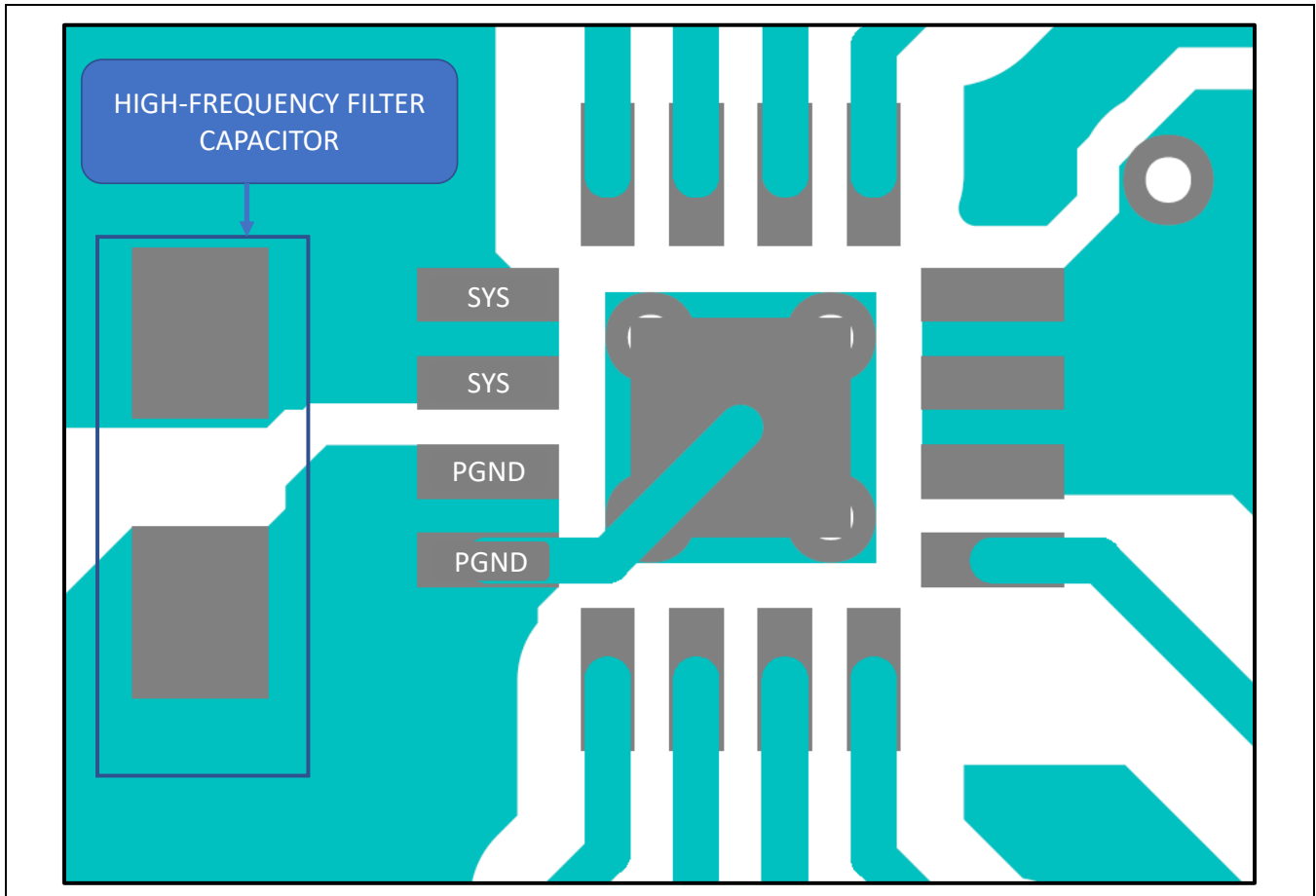


Figure 4. High-Frequency Filter Capacitor

The trace between the feedback resistor dividers should be as short as possible and should be isolated from the noisy power path. Refer to the EV kit layout for best practices.

The PCB layout is important for robust thermal design. The junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout, and pad connections. Using thick PCB copper and having a SYS, LX, CAP, and PGND copper pour enhances the thermal performance. The TQFN package has a large, exposed pad under the package, which creates an excellent thermal path to the PCB. This pad is electrically connected to the analog GND of the controller (AGND). Its PCB pad should have multiple thermal vias connecting the pad to the internal ground plane. The thermal vias should either be capped or have a small diameter in order to minimize solder wicking and voids.

**Ordering Information**

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	FEATURES
MAX38890AATE+	-40°C to +125°C	3mm x 3mm, 16-pin TQFN	Enable input, selectable voltages and currents

+Denotes a lead (Pb)-free/RoHS-compliant package.



**Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/22	Release for Market Intro	—

