MAX32690
ERRATA SHEET

Revision A4 Errata

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Analog Devices may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Analog Devices has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

This errata sheet only applies to components of this revision. These components are branded on the topside of the package with a six-digit code in the form yywwRR, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and RR is the revision of the component. To obtain an errata sheet on other die revisions, visit the Analog Devices website at www.analog.com/MAX32690.

1) SPIXF MAY READ INCORRECT ADDRESSES OF NON-PROGRAM DATA IF BUS IDLE TIMER LIMIT IS 0

Description:

SPIXF will not send a new address, and thus return incorrect values, if there is no idle time between two consecutive reads of non-program data that both generate a cache miss. This issue does not affect SPIXF reads of program data. (18144)

Workaround:

Set SPIXF_BUS_IDLE.busidle to 1 instead of setting SPIXF_BUS_IDLE.busidle to 0. This will have minimal effect on the speed of sequential code execution.

2) BACK-TO-BACK ZEROIZATION ON IDCACHE0 DOES NOT WORK

Description:

Performing back-to-back zeroization operations on the cache does not work as expected. (1854)

Workaround:

Invalidate the cache immediately after the zeroization to properly zeroize the cache.

419-100144, Rev 0; 10/25

3) BACK-TO-BACK ZEROIZATION ON IDCACHEXIP DOES NOT WORK

Description:
Performing back-to-back zeroization operations on the cache does not work as expected. (1868)

Workaround:
Invalidate the cache immediately after the zeroization to properly zeroize the cache.

4) GPIO3[7:0] MAXIMUM VOLTAGE IS V_{DD3A}

Description:
The analog input pins GPIO3[7:0] will source current into the V_{DD3A} supply if the voltage on any of the GPIO3[7:0] pins exceeds V_{DD3A}. (1898)

Workaround:
Ensure the voltage applied to GPIO3[7:0] is less than or equal to V_{DD3A}.

5) UART TRANSMIT FIFO FAILS TO ASSERT HALF-EMPTY INTERRUPT

Description:
The transmit FIFO does not reliably assert the half-empty interrupt. (18117)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

6) CAN PERIPHERAL DOES NOT SUPPORT FD CLOCK RATES

Description:
The CAN peripheral supports the CAN FD protocol but does not support CAN FD clock rates. (18127)

Workaround:
The peripheral should only be used in CAN 2.0b networks.

7) IN TARGET MODE, INCORRECT DATA IS TRANSMITTED IF AN EMPTY SPI FIFO IS WRITTEN DURING AN SPI TRANSACTION

Description:

In target mode, if data is written to an empty transmit FIFO while chip select is active and an SPI transaction is in progress (i.e., SPI clock is provided by the controller), the data written to the FIFO gets transferred but is shifted or incomplete on the SPI bus. (18101)

Workaround:

In target mode, do not let the transmit FIFO become empty during a transaction until all data has been transmitted. Additionally, ensure that the FIFO contains some data prior to the transaction start. In other words, the transmit FIFO should be preloaded prior to chip select becoming active.

8) IN TARGET MODE, SPI FIFO TRANSMITS UNEXPECTED DATA WHEN TX FIFO EMPTY

Description:

After an SPI transmit FIFO is empty, it is expected that the device will transmit 0x00 on subsequent clocks. Instead, when the FIFO empty condition is met, the device will continue to loop through the FIFO and transmit its contents. For example, if the application is sending 8 bytes and the controller attempts to read 10 bytes, the last 2 bytes read are undefined. (18102)

Workaround:

None.

9) 140 WLP PACKAGE REQUIRES EXTERNAL LDO FOR BLUETOOTH LE OPERATION

Description:

Internal coupling in the 140 WLP package prevents proper operation of the Bluetooth® LE peripheral. This issue does not affect any other packages.

Workaround:

If using the BLE peripheral, follow these steps:

1. Drive the BLE_LDO_IN pin with an external source that meets the $V_{BLE\_LDO\_IN}$ (GCR_BTLELDOCTRL.ldotxbyp = 1) electrical specification.
2. Set GCR_BTLELDOCTRL.ldotxbyp = 1 to bypass the internal Bluetooth LE LDO.

10) CACHE LINE FILL BUFFER NOT CLEARED

Description:
The cache line fill buffer is not automatically cleared when the cache is enabled, resulting in stale data. (18114)

Workaround:
Invalidate the cache, enable, then invalidate again to clear the stale data.

11) AES CCM OPERATION MAY FAIL IF SYS_CLK OPERATES AT IPO FREQUENCY

Description:
AES CCM mode operations may produce incorrect results, and/or the CTB_CTRL.done flag does not work correctly if SYS_CLK is equal to or faster than half the IPO frequency during the operation. Generating SYS_CLK using a clock source other than IPO does not require a workaround, as all other clock sources are slower than the IPO. Other AES modes are not affected by this erratum. (18190)

Workaround:
If IPO is the clock source, set GCR_CLKCTRL.sysclk_div to any divisor of four or greater.

12) DEVICE RESETS WHEN EXITING STANDBY OR UPM MODES

Description:
The device performs an unintended system reset upon exiting STANDBY or UPM modes if the low-voltage reset function is enabled (GCR_PFRST.en = 1). (18191)

Workaround:
1. Clear GCR_PFRST.en to 0.
2. Enter UPM or STANDBY mode.
3. After waking from UPM or STANDBY, read GCR_PFBUF until both GCR_PFBUF.pwrgood = 0b1 and GCR_PFBUF.pwrgood_buf = 0b111.
4. Set GCR_PFRST.en to 1.

MAX32690
REV A4 ERRATA

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/25	Initial release	—