Industrial Octal High-Side Switch with Advanced Diagnostics

MAX22915

General Description

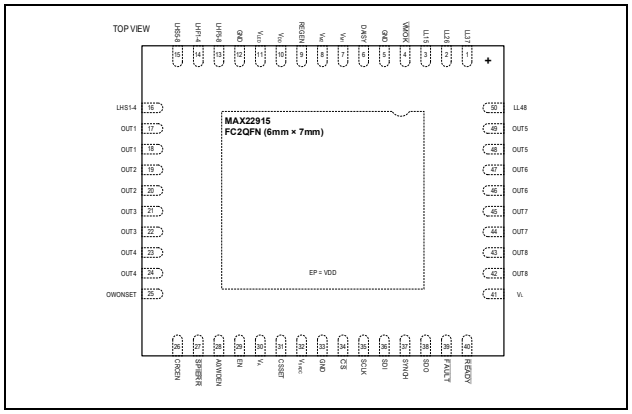
The MAX22915 is an industrial output device with eight high-side switches. Each channel is specified to handle up to 1A (typ) of continuous current with an on-resistance of 120mΩ (typ) and 250mΩ (max) at 125°C.

The MAX22915 has a built-in 7-bit ADC to monitor chip temperature, per-channel output current or V_{DD} supply voltage. It supports continous or on-demand monitoring, with option to average multiple ADC conversions.The MAX22915 provides flexible configurations and global diagnostics, which include undervoltage warnings, thermal condition reportings, and communication errors.

Each channel is equipped with overload, overcurrent and short-to-V_{DD} detections, as well as open-wire detection that can detect an open-wire fault condition when switch is on, off, or toggling at up to 131Hz. Moreover, these diagnotics have enhanced immunity to IEC 61000-4-4 EFT and IEC 61000-4-6 Conducted RF.

The SPI interface has a built-in chip addressing decoder, which allows communication with two MAX22915 utilizing a common chip select ($\overline{CS}$). The 16-LED driver matrix provides indications of per-channel fault and status. Internal active clamps allow for fast turn-off of inductive loads. Integrated ESD and surge protection requires only a single TVS on V_{DD}. The MAX22915 is available in a compact 50-pin 6mm × 7mm flip chip QFN package.

Pin Configuration



Product Highlights

- Robustness with Extensive Diagnostics
  - 7-bit ADC to Monitor Chip Temperature, Per-Channel Output Current or V_{DD} Supply Voltage
  - Per-Channel Open-Wire Detection with Switches On, Off, or Toggling at up to 131Hz
  - Per-Channel Overload, Overcurrent and Short-to-V_{DD} Fault Detection
  - CRC Error Checking on SPI Interface
  - Watchdog Timer on SPI and SYNCH Pin
  - Thermal Shutdown Protection and Adjustable Thermal Warning Reporting
  - 65V Absolute Maximum Supply Range
  - Internal Clamps for Fast Inductive Load Demagnetization
  - UVLO Warning on Supply Voltages
  - Loss of V_{DD} or GND Protection
  - Integrated IEC 61000-4-2 ESD Protection at ±8kV Contact and ±15kV Air-Gap
  - Integrated IEC 61000-4-5 Surge Protection at ±1kV/42Ω Using Single TVS on V_{DD}
  - Enhanced EFT and RF Conducted Immunity on Per-Channel Diagnostics with Switches On, Off, or Toggling at up to 131Hz
  - −40°C to +125°C Operating Temperature Range
- Reduced Power and Heat Dissipation
  - Active Current Limiting at 1A (typ), 1.3A (max)
  - 5mA (typ) Supply Current
  - 250mΩ (max) On-Resistance at +125°C
- Flexibility and Space Saving
  - Selectable $V_{M\_}$ Supply Voltage Monitoring
  - Selectable Open-Wire Detection Thresholds
  - Selectable Output Current Measurement Full-Scale Range
  - SYNCH Input for Simultaneous Update of OUT_
  - LED Driver Matrix for 16 Fault and Status LEDs, powered by 24V, 5V, or 3.3V
  - Flexible Logic Supply Voltage from 2.5V to 5.5V
  - Addressable SPI Reduces Isolation Cost
  - Compact 6mm × 7mm FCQFN Package

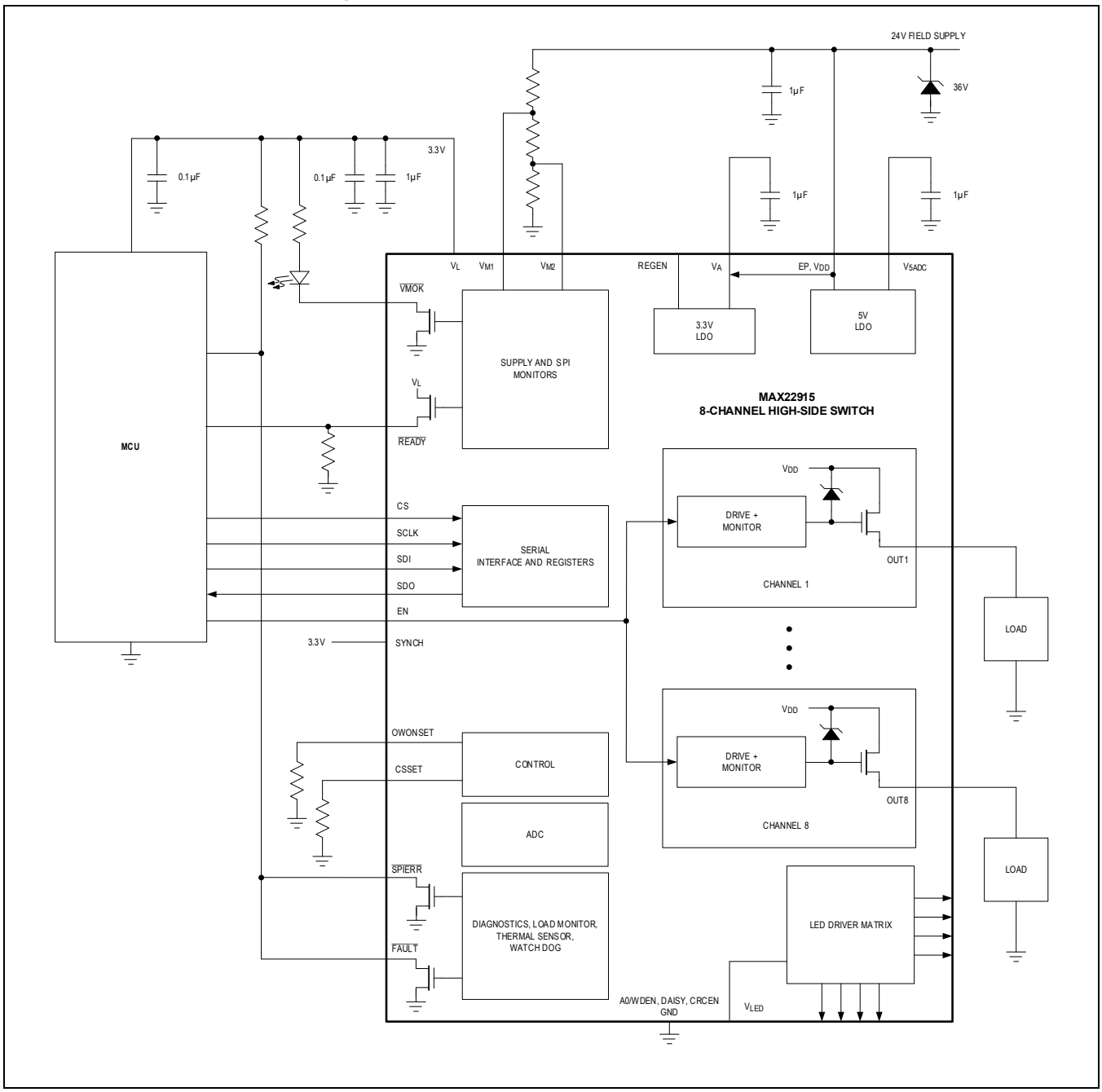
Applications

- Industrial Digital Outputs
- PLC Systems

***Ordering Information* appears at end of data sheet.**

19-102099; Rev. 0; 2/26

Simplified Application Diagram



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Absolute Maximum Ratings

V_{DD} ..... −0.3V to +65V

OUT_ ..... (V_{DD} − 49)V to (V_{DD} + 0.3)V

V_A, V_L, V_{5ADC} ..... −0.3V to +6V

V_{M1}, V_{M2} ..... −0.3V to +6V

V_{LED} ..... −0.3V to +70V

SDO, $\overline{READY}$ ..... −0.3V to (V_L + 0.3)V

REGEN, OWONSET, CSSET ..... −0.3V to (V_{5ADC} + 0.3)V

$\overline{FAULT}$, $\overline{SPIERR}$ ..... −0.3V to +6V

SDI, SCLK, EN, A0/WDEN, SYNCH, CRCEN, DAISY, $\overline{CS}$ ..... −0.3V to +6V

LH_, LL_, $\overline{VMOK}$ ..... −0.3V to (V_{LED} + 0.3)V

OUT_ Load Current ..... Internally Limited

Continuous Power Dissipation (Multilayer Board (T_A = +70°C, derate 40.6mW/°C above +70°C)) 3249.4mW

Operating Temperature Range ..... −40°C to +125°C

Junction Temperature ..... +150°C

Storage Temperature Range ..... −65°C to +150°C

Soldering Temperature ..... +260°C

Note 1: All voltages are relative to GND.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Flip Chip QFN

Package Code	F5067F+1F
Outline Number	*21-100765*
Land Pattern Number	*90-100269*
Thermal Resistance, 4-Layer Board	
Junction-to-Ambient (θ_{JA})	24.62°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1.69°C/W (bottom)

For the latest package outline information and land patterns (footprints), go to Package Index. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to Thermal Characterization of IC Packages.

Electrical Characteristics

(V_{DD} = +10V to +36V, V_{LED} = +3V to +36V, V_A = +3V to +5.5V, V_L = +2.5V to +5.5V, T_A = −40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = V_L = 3.3V, T_A = +25°C.) (*Note 2*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} SUPPLY						
V_{DD} Supply Voltage	V_{DD}		10		36	V
V_{DD} Supply Current	I_{DD}	EN = high, OUT_ turned on, no load, V_A and V_L supplied externally, ADC not converting		5.0	6.5	mA
		EN = low			6.5	
V_{DD} UVLO Threshold Rising	$V_{DD\_UVLO\_R}$	V_{DD} rising			9.6	V
V_{DD} UVLO Threshold Falling	$V_{DD\_UVLO\_F}$	V_{DD} falling, OUT_ turned off, VDD_UVLO bit asserted	7.9			V
V_{DD} UVLO Threshold Hysteresis	$V_{DD\_UVLO\_H}$			0.35		V
V_{DD} POR Threshold Rising	$V_{DD\_POR\_R}$	V_{DD} rising, REGEN open			6.8	V
V_{DD} POR Threshold Falling	$V_{DD\_POR\_F}$	V_{DD} falling, REGEN open	5.6			V
V_{DD} POR Hysteresis	$V_{DD\_POR\_H}$			0.44		V
V_A ANALOG SUPPLY (REGEN = GND)						
V_A Supply Voltage	V_A	V_A supplied externally, REGEN = GND	3.0		5.5	V
V_A Supply Current	I_A	EN = high, OUT_ turned on, no load, no LEDs connected; V_A = 3.3V		1.2	1.5	mA
		EN = high, OUT_ turned on, no load, no LEDs connected; V_A = 5.5V		2.2	2.5	
V_A UVLO Threshold Rising	$V_{A\_UVLO\_R}$	V_{DD} = 24V, V_A rising	2.45		2.9	V
V_A UVLO Threshold Falling	$V_{A\_UVLO\_F}$	V_{DD} = 24V, V_A falling	2.35		2.8	V
V_A UVLO Threshold Hysteresis	$V_{A\_UVLO\_H}$	V_{DD} = 24V		0.1		V
V_L LOGIC SUPPLY						
V_L Supply Voltage	V_L		2.5		5.5	V
V_L Supply Current	I_L	All logic inputs high or low		18	34	µA
V_L POR Threshold Rising	$V_{L\_POR\_R}$	V_L rising	1.89		2.4	V
V_L POR Threshold Falling	$V_{L\_POR\_F}$	V_L falling	1.82		2.36	V
V_L POR Threshold Hysteresis	$V_{L\_POR\_H}$			0.1		V
V_M VOLTAGE MONITOR						
V_{M1} Threshold Rising	V_{M1_R}	V_{M1} rising, $\overline{VMOK}$ turned active low	0.892	0.91	0.93	V
V_{M2} Threshold Falling	V_{M2_F}	V_{M2} falling, $\overline{VMOK}$ turned passive high	0.676	0.69	0.704	V
V_A LINEAR REGULATOR						
Output Voltage	V_{A_OUT}	REGEN open, C_{LOAD} = 1µF, 0mA < I_{A_OUT} < 20mA	3.0	3.3	3.6	V
Current Limit	I_{A_LIM}	REGEN open	25			mA
Short Circuit Current	I_{A_SHRT}	REGEN open, V_{A_OUT} = 0V			60	mA

(V_{DD} = +10V to +36V, V_{LED} = +3V to +36V, V_A = +3V to +5.5V, V_L = +2.5V to +5.5V, T_A = −40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = V_L = 3.3V, T_A = +25°C.) (*Note 2*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Load Regulation		REGEN open, 0mA < I_{A_OUT} < 20mA			0.1		mV/mA
REGEN Threshold Rising	V_{REGEN_R}	REGEN rising				3.25	V
REGEN Threshold Falling	V_{REGEN_F}	REGEN falling		0.2			V
REGEN Leakage Current	I_{REGEN_LKG}	REGEN = GND		−50			µA
V_{5ADC} LINE REGULATOR							
V_{5ADC} Output Voltage	V_{5ADC}			4.8		5.2	V
V_{5ADC} UVLO Threshold	V_{5ADC_UVLO}			4.3		4.6	V
V_{5ADC} UVLO Threshold Hysteresis	V_{5ADC_HYST}				0.4		V
V_{5ADC} Current Limit	V_{CL_5ADC}			2	3.7	4.4	mA
OUT_ SWITCHES							
On Resistance	R_{OUT_LO}	Low R_{OUT} mode	$I_{OUT\_}$ = −600mA, *Note 4*		120	250	mΩ
	R_{OUT_HI}	High R_{OUT} mode	OWON_EN_ = 1, $I_{OUT\_}$ < $I_{OUT\_TH\_R}$		1.5	3.5	Ω
On Resistance Threshold Current Rising	$I_{OUT\_TH\_R}$	On resistance switches from R_{OUT_HI} to R_{OUT_LO}		38	46	55	mA
Current Limit	I_{OUT_LIM}			0.7	1	1.3	A
Cold Lamp Current Limit	I_{OUT_LAMP}			1.2	1.5	1.8	A
Off Leakage Current	I_{OUT_LKG}	OUT_ turned off, OWOFF_EN_ = 0		−10		+10	µA
OFF STATE DIAGNOSTICS (OUT_)							
OUT_ Off State Voltage	V_{OUT_OFF}	OWOFF_EN_ = 1, $I_{OUT\_}$ = 0A		5.7	6.7	7.8	V
Pull-Up Current	I_{PU_OWOFF1}	OWOFF_EN_ = 1, $V_{OUT\_}$ < 5V	OWOFF_CS[1:0] = 00b	10	20	32	µA
	I_{PU_OWOFF2}	OWOFF_EN_ = 1, $V_{OUT\_}$ < 5V	OWOFF_CS[1:0] = 01b	65	100	135	
	I_{PU_OWOFF3}	OWOFF_EN_ = 1, $V_{OUT\_}$ < 5V	OWOFF_CS[1:0] = 10b	230	300	370	
	I_{PU_OWOFF4}	OWOFF_EN_ = 1, $V_{OUT\_}$ < 5V	OWOFF_CS[1:0] = 11b	480	600	720	
Open-Wire Off Threshold	V_{OWOFF_TH}	OWOFF_EN_ = 1		5		5.8	V
Short-to-V_{DD} Threshold	V_{SHTVDD_TH}	SHTVDD_EN_ = 1	SHTVDD_TH[1:0] = 00b	8.2	9	10	V
			SHTVDD_TH[1:0] = 01b	9.1	10	10.9	
			SHTVDD_TH[1:0] = 10b	11	12	13	
			SHTVDD_TH[1:0] = 11b	13	14	15	
ON STATE DIAGNOSTICS (OUT_)							
OWONSET Regulation Voltage	$V_{OWONSET}$				700		mV
	I_{OWON_TH}	$R_{OWONSET}$ = 137kΩ			0.52		mA

(V_{DD} = +10V to +36V, V_{LED} = +3V to +36V, V_A = +3V to +5.5V, V_L = +2.5V to +5.5V, T_A = −40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = V_L = 3.3V, T_A = +25°C.) (*Note 2*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Open-Wire On Threshold		$R_{OWONSET}$ = 82kΩ			0.82		
		$R_{OWONSET}$ = 22kΩ			2.94		
ADC							
ADC Resolution					7		Bit
THERMAL MEASUREMENT							
Measurable Temperature High	T_{SENSE_HI}				+150		°C
Measureble Temperature Low	T_{SENSE_LO}				+85		°C
Thermal Measurement ADC Accuracy	T_{SENSE_PREC}	T_J = +125°C			±3		°C
OUTPUT CURRENT MEASUREMENT							
CSSET Regulation Voltage	V_{CSSET}				800		mV
Current Full Scale Max	I_{CSSET_MAX}	R_{CSSET} = 10kΩ			0.7		A
Current Full Scale Min	I_{CSSET_MIN}	R_{CSSET} = 40kΩ			0.175		A
SUPPLY VOLTAGE MEASUREMENT							
Measurable Supply Voltage High	V_{SENSE_HI}				36		V
Measurable Supply Voltage Low	V_{SENSE_LO}	V_{DD} falling			$V_{DD\_UV\_LO\_F}$		V
		V_{DD} rising			$V_{DD\_UV\_LO\_R}$		
LOGIC INPUTS							
Input Voltage High	V_{IH}			0.7 × V_L			V
Input Voltage Low	V_{IL}					0.3 × V_L	V
Input Threshold Hysteresis	V_{IHYS}				0.11 × V_L		V
Input Pull-Down Resistor	R_{IPD}	EN, CRCEN, SDI, SCLK, A0/WDEN, DAISY			200		kΩ
Input Pull-Up Resistor	R_{IPU}	SYNCH, $\overline{CS}$			200		kΩ
LOGIC OUTPUT (SDO)							
Output Logic High	V_{OH}	I_{LOAD} = −5mA	*Note 4*	V_L − 0.6			V
Output Logic Low	V_{OL}	I_{LOAD} = +5mA	*Note 4*			0.33	V
SDO Output Tristate Leakage Current	I_{SDO_LKG}	$\overline{CS}$ = high		−1		+1	µA
OPEN-DRAIN LOGIC OUTPUTS ($\overline{FAULT}$, $\overline{SPIERR}$, $\overline{READY}$)							
Output High ($\overline{READY}$)	V_{ODH}	I_{LOAD} = −5mA	*Note 4*	V_L − 0.6			V
Output Low ($\overline{SPIERR}$, $\overline{FAULT}$)	V_{ODL}	I_{LOAD} = +5mA	*Note 4*			0.33	V
Leakage Current	I_{OD_LKG}	Open-drain output turned off, V = 5.5V		−1		+1	µA
LED DRIVERS (LH_, LL_, V_{LED})							
LED Supply Voltage	V_{LED}			3.0		V_{DD}	V
LH_ Output Voltage High	V_{LH_OH}	LH_ = on, I_{LOAD} = −5mA, *Note 4*		V_{LED} − 0.3			V

(V_{DD} = +10V to +36V, V_{LED} = +3V to +36V, V_A = +3V to +5.5V, V_L = +2.5V to +5.5V, T_A = −40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = V_L = 3.3V, T_A = +25°C.) (*Note 2*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LH_ Off Leakage Current	I_{LH_LKG}	LH_ = off, $V_{LH\_}$ = 9V				1	µA
LL_ Output Voltage Low	V_{LL_OL}	LL_ = on, I_{LOAD} = +5mA, *Note 4*				0.3	V
LL_ Off Leakage Current	I_{LL_LKG}	LL_ = off, $V_{LL\_}$ = V_{LED}		−1		+1	µA
LED Driver Scan Rate	f_{LED}	Update rate for each LED			1		kHz
PROTECTION							
OUT_ Clamp Voltage	V_{CLAMP}	OUT_ turned off, V_{CLAMP} = V_{DD} – $V_{OUT\_}$, $I_{OUT\_}$ = −500mA	*Note 4*	49	56	63	V
Per-Channel Thermal Shutdown Temperature	T_{J_SHDN}	Junction temperature rising			150		°C
Per-Channel Thermal Shutdown Hysteresis	$T_{J\_SHDN\_H}$				15		°C
Chip Thermal Shutdown Temperature	T_{C_SHDN}	Chip temperature rising			150		°C
Chip Thermal Shutdown Hysteresis	$T_{C\_SHDN\_H}$				10		°C
OUT_ TIMING CHARACTERISTICS							
Propagation Delay, LH	t_{PD_LH}	*Figure 2*	Delay from rising SYNCH edge to OUT_ rising to 90% of V_{DD}, R_{LOAD} = 48Ω		11	30	µs
Propagation Delay, HL	t_{PD_HL}	*Figure 2*	Delay from rising SYNCH edge to OUT_ falling to 10% of V_{DD}, R_{LOAD} = 48Ω		11	30	µs
Rise Time	t_R	*Figure 2*	20% to 80% V_{DD}, R_{LOAD} = 48Ω		6		µs
Fall Time	t_F	*Figure 2*	80% to 20% V_{DD}, R_{LOAD} = 48Ω		6		µs
WATCHDOG TIMING CHARACTERISTICS							
Watchdog Timeout	t_{WD}	WD_TIMEOUT[1:0] = 01b			50		ms
		WD_TIMEOUT[1:0] = 10b			200		
		WD_TIMEOUT[1:0] = 11b			500		
Watchdog Timeout Accuracy	t_{WD_ACC}	Watchdog timer enabled		−30		+30	%
SPI TIMING CHARACTERISTICS							
SCLK Clock Period	t_{CH+CL}	*Figure 1*		100			ns
SCLK Pulse Width High	t_{CH}	*Figure 1*		40			ns
SCLK Pulse Width Low	t_{CL}	*Figure 1*		40			ns
$\overline{CS}$ Fall to SCLK Rise	t_{CSS}	*Figure 1*		40			ns
SDI Hold Time	t_{DH}	*Figure 1*		10			ns
SDI Setup Time	t_{DS}	*Figure 1*		10			ns

(V_{DD} = +10V to +36V, V_{LED} = +3V to +36V, V_A = +3V to +5.5V, V_L = +2.5V to +5.5V, T_A = −40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = V_L = 3.3V, T_A = +25°C.) (*Note 2*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SDO Propagation Delay	t_{DO}	*Figure 1*	C_{LOAD} = 10pF, SCLK falling edge to SDO stable			30	ns
SDO Rise and Fall Times	t_{FT}	*Figure 1*			1		ns
$\overline{CS}$ Hold Time	t_{CSH}	*Figure 1*		40			ns
$\overline{CS}$ Pulse Width High	t_{CSPW}	*Figure 1*	*Note 3*	40			ns
EMC							
ESD	V_{ESD_C}	OUT_ to GND	Contact Discharge per IEC 61000-4-2 (*Note 6*)		±8		kV
	V_{ESD_A}	OUT_ to GND	Airgap Discharge per IEC 61000-4-2 (*Note 6*)		±15		
	V_{ESD}	All other pins	Human Body Model (*Note 5*, *Note 6*)		±2		
Surge	V_{SURGE}	OUT_ to GND with 42Ω, TVS on V_{DD}	Per IEC 61000-4-5 (*Note 6*, *Note 7*)		±1		kV

Note 2: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization.

Note 3: All logic input pins except $\overline{CS}$ and SYNCH have a pull-down resistor. $\overline{CS}$ and SYNCH pins have a pull-up resistor.

Note 4: All currents into the device are positive. All currents out of the device are negative.

Note 5: Bypass V_{DD} to GND with a 1µF capacitor as close as possible to the device for high ESD protection.

Note 6: Not production tested.

Note 7: At typical value of V_{DD} = 24V, with a TVS diode on V_{DD} to GND.

Timing Diagrams

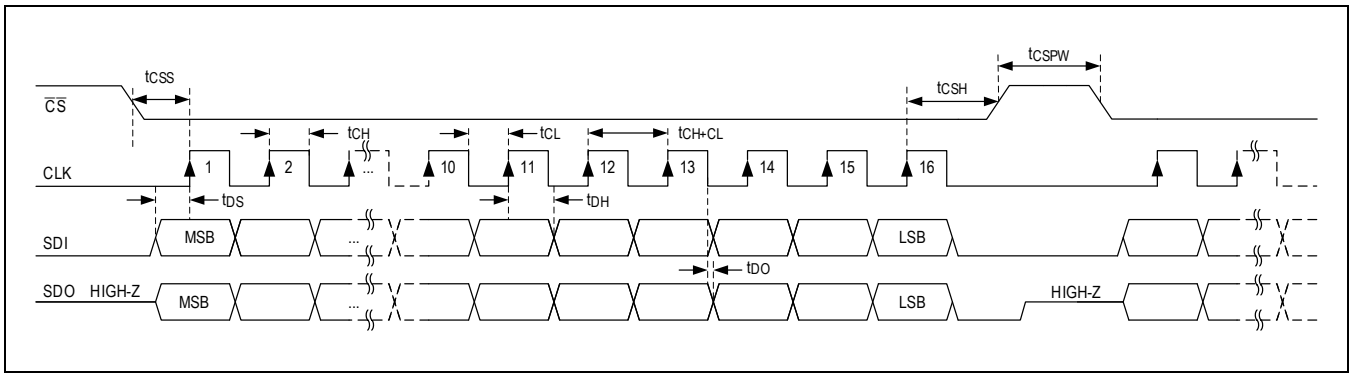


Figure 1. SPI Timing Diagram

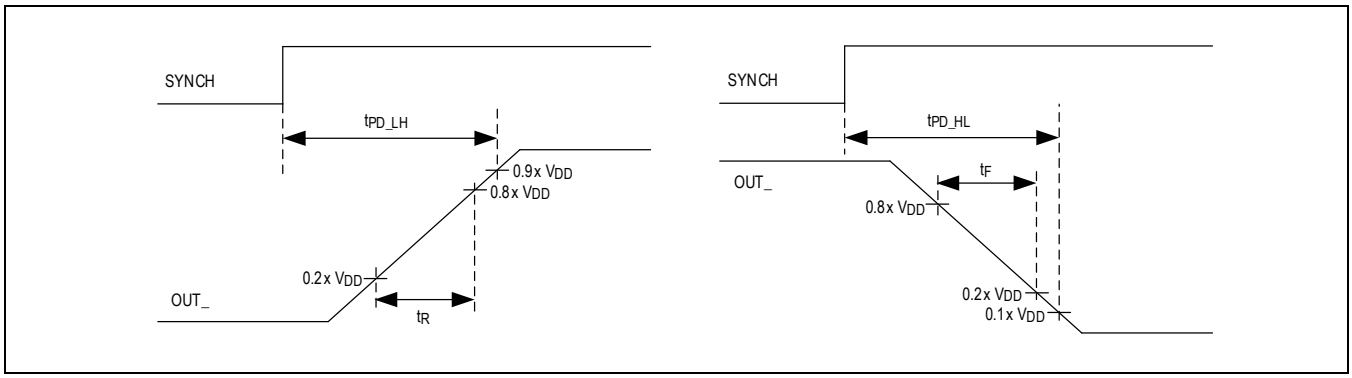
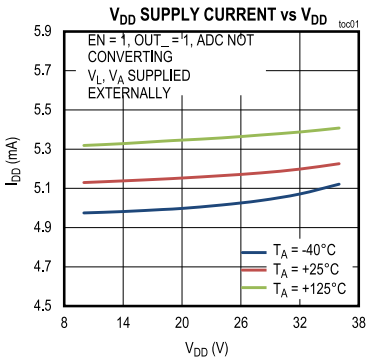
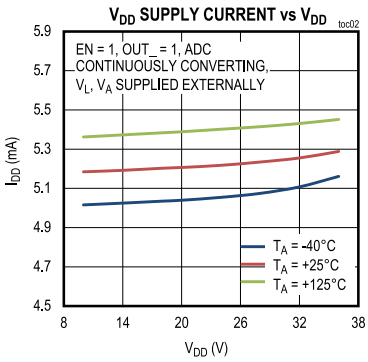


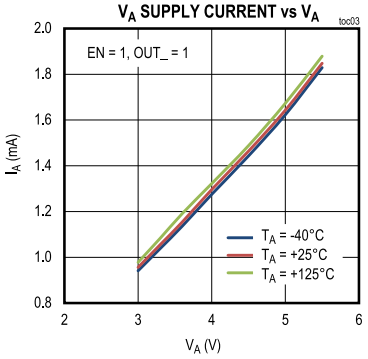
Figure 2. Propagation Delay Timing Characteristics

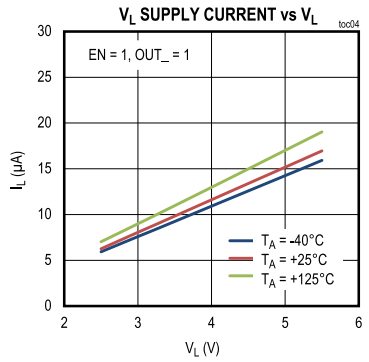
Typical Operating Characteristics

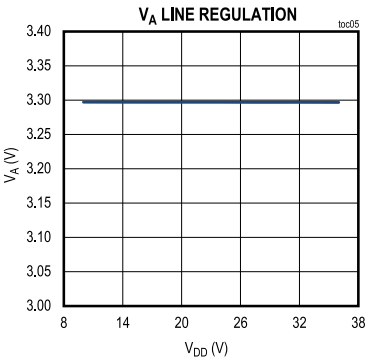
(V_{DD} = +24V, REGEN = open, V_L = +3.3V, T_A = +25°C, unless otherwise noted)

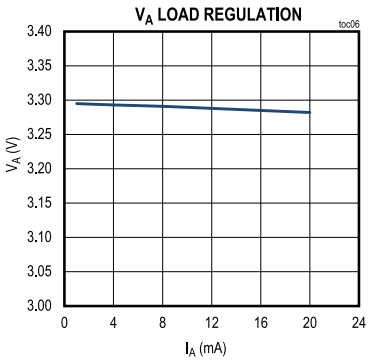


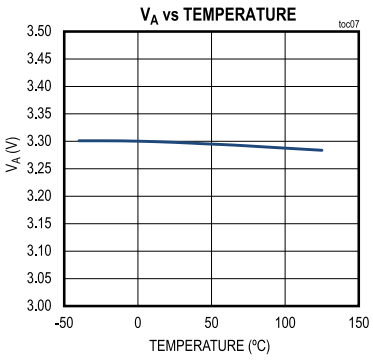


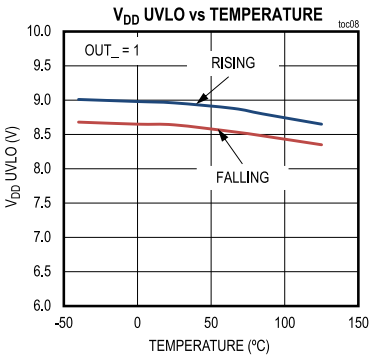


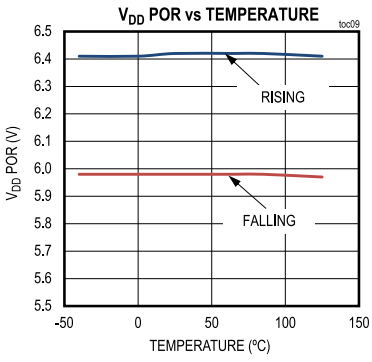


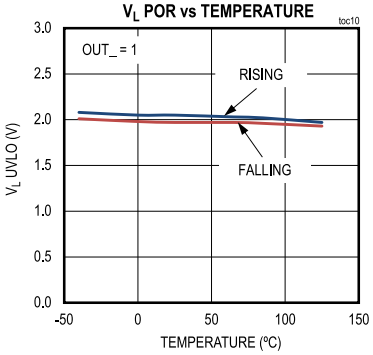


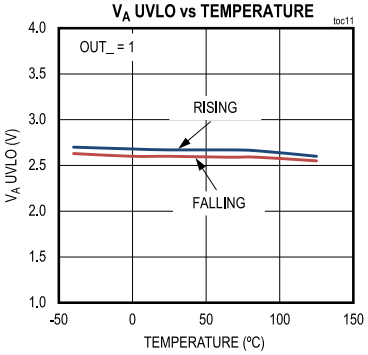


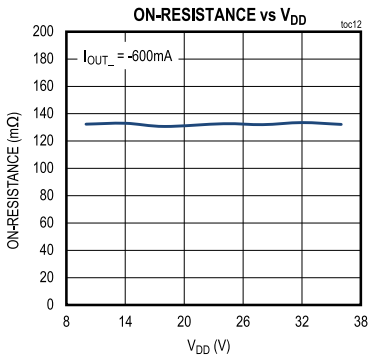


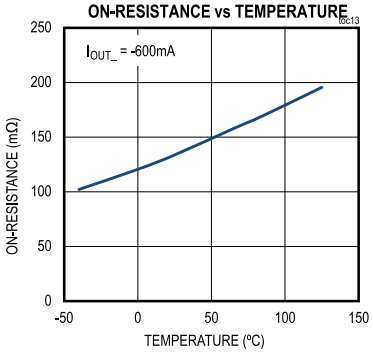


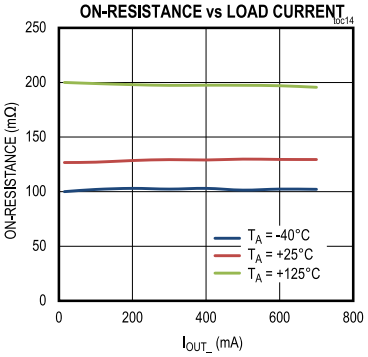


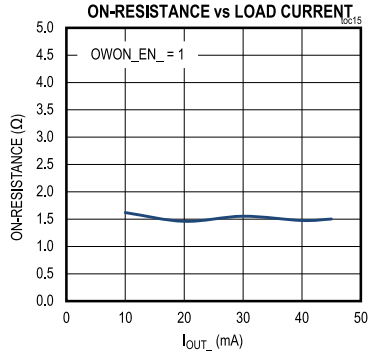

V_L POR vs TEMPERATURE
toc10
OUT_ = 1
RISING
FALLING
V_L UVLO (V)
TEMPERATURE (°C)

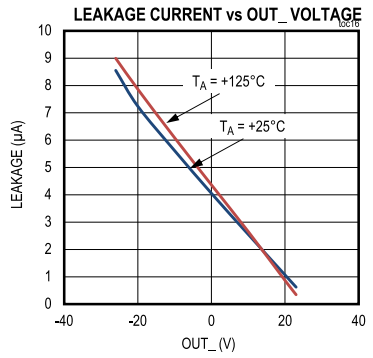

V_A UVLO vs TEMPERATURE
toc11
OUT_ = 1
RISING
FALLING
V_A UVLO (V)
TEMPERATURE (°C)

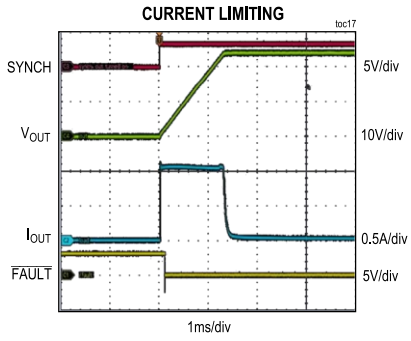

ON-RESISTANCE vs V_DD
toc12
I_OUT_ = -600mA
ON-RESISTANCE (mΩ)
V_DD (V)

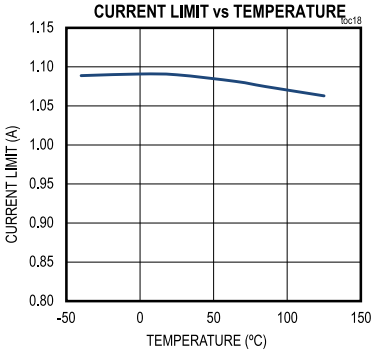

ON-RESISTANCE vs TEMPERATURE
toc13
I_OUT_ = -600mA
ON-RESISTANCE (mΩ)
TEMPERATURE (°C)

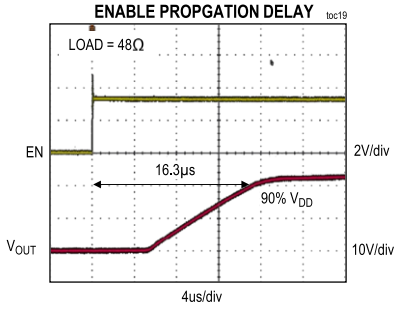

ON-RESISTANCE vs LOAD CURRENT
toc14
T_A = -40°C
T_A = +25°C
T_A = +125°C
ON-RESISTANCE (mΩ)
I_OUT_ (mA)

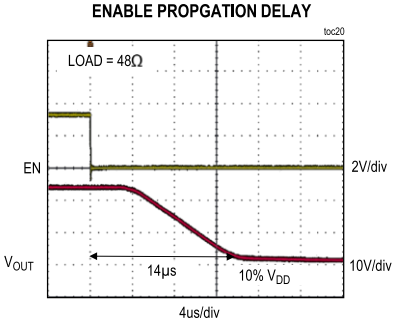

ON-RESISTANCE vs LOAD CURRENT
toc15
OWON_EN_ = 1
ON-RESISTANCE (Ω)
I_OUT_ (mA)

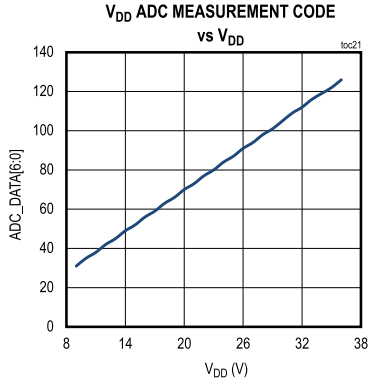

LEAKAGE CURRENT vs OUT_ VOLTAGE
toc16
T_A = +125°C
T_A = +25°C
LEAKAGE (µA)
OUT_ (V)


CURRENT LIMITING
toc17
SYNCH
V_OUT
I_OUT
FAULT
5V/div
10V/div
0.5A/div
5V/div
1ms/div

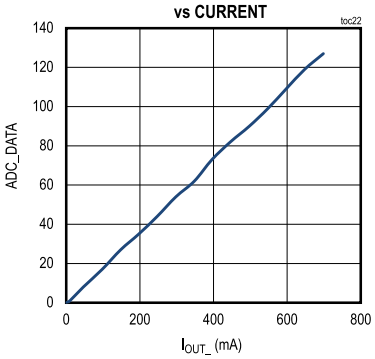

CURRENT LIMIT vs TEMPERATURE
toc18
CURRENT LIMIT (A)
TEMPERATURE (°C)


ENABLE PROPGATION DELAY
toc19
LOAD = 48Ω
EN
V_OUT
16.3µs
90% V_DD
2V/div
10V/div
4us/div

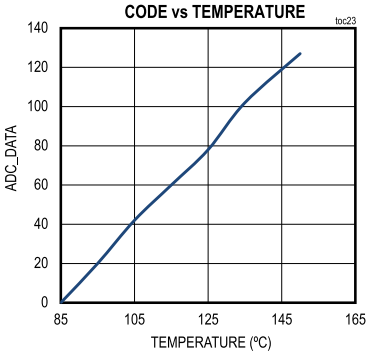

ENABLE PROPGATION DELAY
toc20
LOAD = 48Ω
EN
V_OUT
14µs
10% V_DD
2V/div
10V/div
4us/div


V_DD ADC MEASUREMENT CODE
vs V_DD
toc21
ADC_DATA[6:0]
V_DD (V)

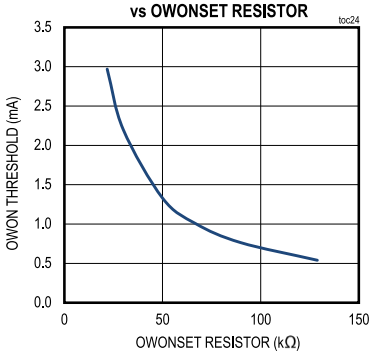
CURRENT ADC MEASUREMETN CODE vs CURRENT



TEMPERATURE ADC MEASUREMENT CODE vs TEMPERATURE

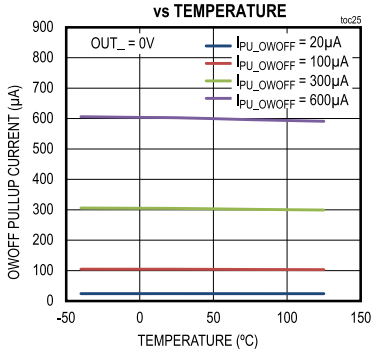


OPEN-WIRE ON THRESHOLD vs OWONSET RESISTOR

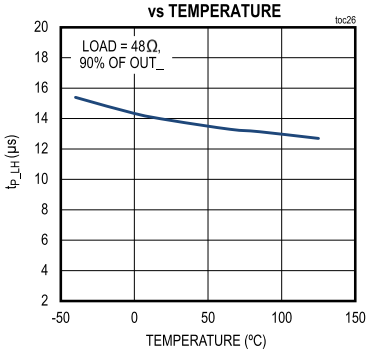


3

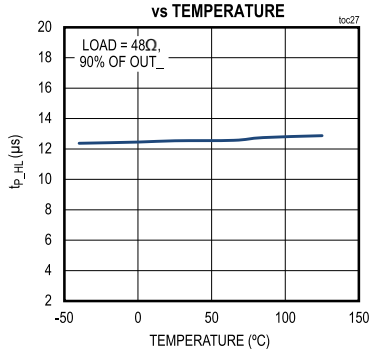
OWOFF PULL-UP CURRENT vs TEMPERATURE



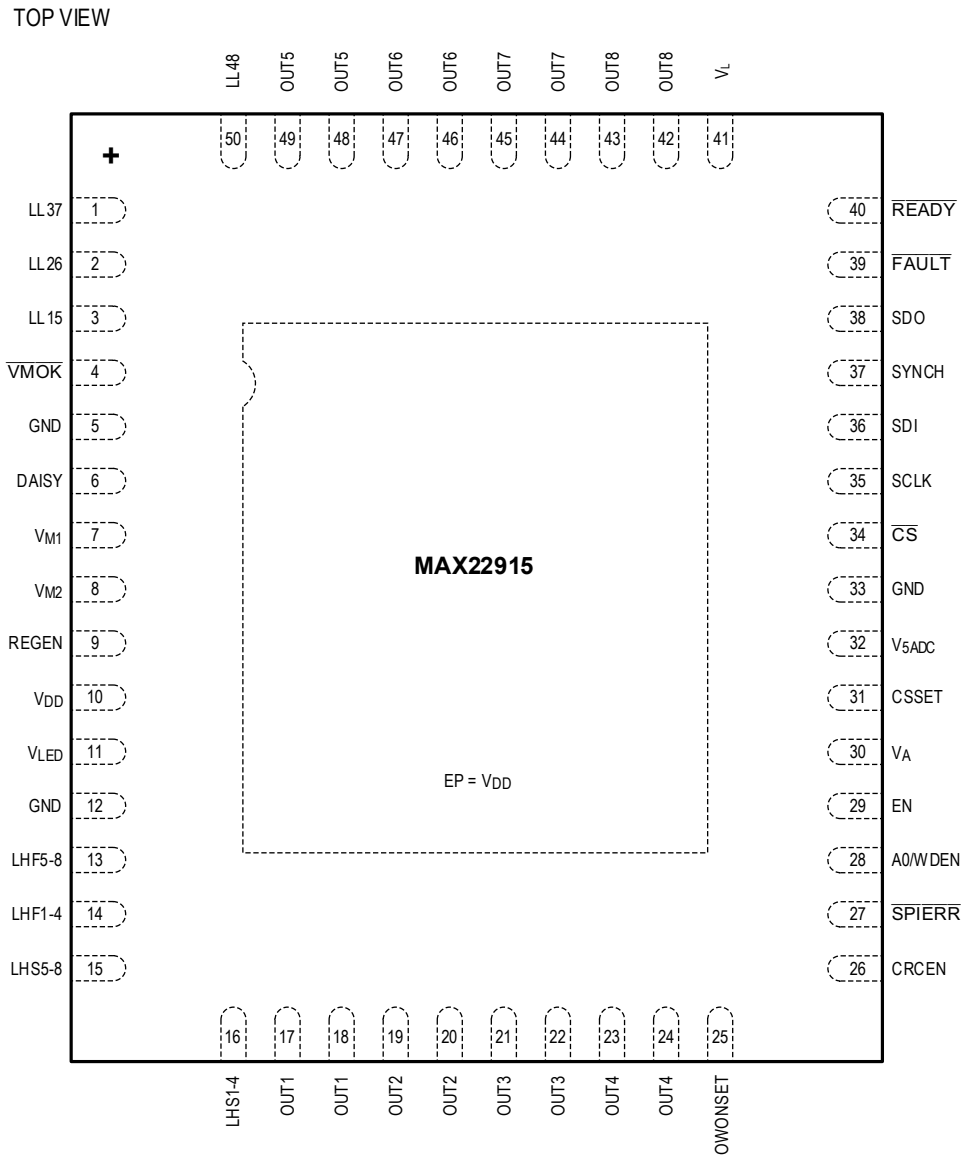
TURN-ON PROPGATION DELAY vs TEMPERATURE



TURN-OFF PROPGATION DELAY vs TEMPERATURE



Pin Configuration



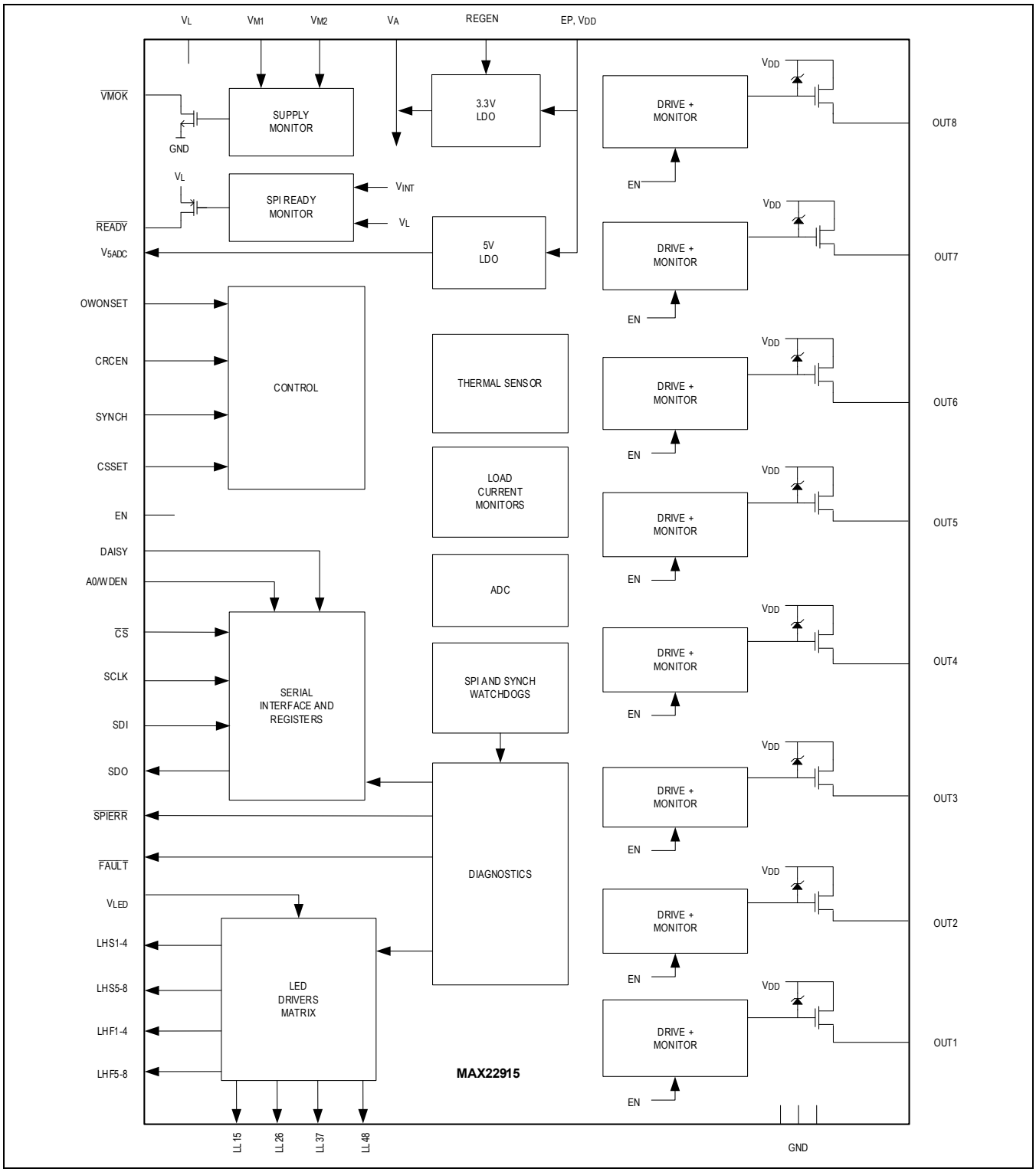
FC2QFN
(6mm × 7mm)

Pin Descriptions

PIN	NAME	FUNCTION	REF SUPPLY	Type
POWER SUPPLIES				
EP, 10	V_{DD}	Supply Voltage, nominally 24V. Connect V_{DD} and EP together. Bypass V_{DD} to GND with a 1µF ceramic capacitor as close to EP as possible.	GND	Supply
30	V_A	Analog Supply Input. Connect an external 3.0V to 5.5V supply to V_A or use the internal linear regulator by leaving REGEN open. Bypass V_A to GND with a 1µF ceramic capacitor.	GND	Supply
9	REGEN	V_A regulator enable input. Connect REGEN to GND to disable V_A regulator. Leave REGEN open to enable V_A regulator, which internally supplies V_A with 3.3V.	GND	Control
5, 12, 33	GND	Ground. Connect all GND pins together.	GND	GND
41	V_L	Logic Supply Input. V_L defines the logic levels on all logic interface pins. Bypass V_L to GND with a 0.1µF ceramic capacitor.	GND	Supply
32	V_{5ADC}	ADC Supply Input. V_{5ADC} supplies the internal ADC. Bypass V_{5ADC} to GND with a 0.1µF ceramic capacitor. Do not use V_{5ADC} to drive external loads.	GND	Supply
4	$\overline{VMOK}$	$\overline{VMOK}$ is an active-low, open-drain logic output that asserts low when V_{M1} input voltage rises above its rising threshold voltage. $\overline{VMOK}$ becomes high-impedance when V_{M2} input voltage falls below its falling threshold voltage. Connect an LED with a pull-up resistor to a voltage between 3.3V and V_{DD}.	GND	Logic
7, 8	V_{M1}, V_{M2}	V_{M1} and V_{M2} are analog voltage inputs used to supervise the supply voltage and determine the state of $\overline{VMOK}$ logic output. Use a voltage divider between the supply voltage and GND to set the threshold voltages for $\overline{VMOK}$.	GND	Analog
SWITCH OUTPUTS				
17, 18	OUT1	High-Side Switch Output 1.	VDD	Power
19, 20	OUT2	High-Side Switch Output 2.	VDD	Power
21, 22	OUT3	High-Side Switch Output 3.	VDD	Power
23, 24	OUT4	High-Side Switch Output 4.	VDD	Power
49, 48	OUT5	High-Side Switch Output 5.	VDD	Power
47, 46	OUT6	High-Side Switch Output 6.	VDD	Power
45, 44	OUT7	High-Side Switch Output 7.	VDD	Power
43, 42	OUT8	High-Side Switch Output 8.	VDD	Power
DIAGNOSTIC SETTINGS				
25	OWONSET	Open-Wire Detection Threshold Current Set. Connect a resistor between OWONSET and GND to define the threshold current for open-wire detection when the OUT_ switches are closed.	VA	Analog
31	CSSET	Current Measurement Full-Scale Range Set. Connect a resistor between CSSET and GND to set the full-scale range of internal ADC current measurement.	VA	Analog
CONTROL INTERFACE				
29	EN	Enable Logic Input. Drive EN high for normal operation. Drive EN low to disable all OUT_ switches. EN has an weak pull-down.	VL	Logic
39	$\overline{FAULT}$	$\overline{FAULT}$ Global Diagnostics Open-Drain Output. The $\overline{FAULT}$ asserts low under conditions defined in the INTERRUPT register. Connect a pull-up resistor to V_L.	VL	Logic
37	SYNCH	SYNCH Input. All eight output switches are updated simultaneously on the rising edge of SYNCH, as determined by the contents of the SET_OUT register. The OUT_ states do not change when SYNCH is held low. When SYNCH is high, the output states change immediately when a new value is written into the SET_OUT register. SYNCH has an weak pull-up.	VL	Logic

26	CRCEN	CRC Enable Select Input. Drive CRCEN high to enable CRC generation and error detection on the serial data. CRCEN has an weak pull-down.	VL	Logic
40	$\overline{\text{READY}}$	$\overline{\text{READY}}$ is an open-drain output that is passive low when the internal chip supply and V_L I/O supply are both higher than their respective UVLO thresholds, which indicates that MAX22915 is ready for SPI communication. When the internal register supply falls below its UVLO threshold, the register contents are lost and $\overline{\text{READY}}$ transitions active-high. Connect a pull-down resistor from $\overline{\text{READY}}$ to GND.	VL	Logic
27	$\overline{\text{SPIERR}}$	SPI Error Open-Drain Output. The $\overline{\text{SPIERR}}$ asserts low when an error occurs during an SPI transaction. Connect a pull-up resistor to V_L.	VL	Logic
SERIAL INTERFACE				
36	SDI	Serial Data Input. SPI MOSI data from controller. SDI has a weak pull-down.	VL	Logic
38	SDO	Serial Data Output. SPI MISO data output to controller.	VL	Logic
35	SCLK	Serial Clock Input from SPI Controller. SCLK has a weak pull-down.	VL	Logic
34	$\overline{\text{CS}}$	Chip Select Input from Controller. $\overline{\text{CS}}$ has a weak pull-up.	VL	Logic
28	A0/WDEN	Chip Address for Addressable SPI or SPI Watchdog Enable Input for Daisy-Chained SPI Mode. A0/WDEN has a weak pull-down.	VL	Logic
6	DAISY	Daisy-Chain Enable Select Input. Drive DAISY high to enable daisy-chained SPI mode. DAISY has a weak pull-down.	VL	Logic
LED DRIVER MATRIX				
11	V_{LED}	Supply for LED Drivers. Apply supply voltage of 3.0V to V_{DD}.	GND	Supply
3	LL15	OUTs 1, 5 Status/Fault LED Cathode Output (Open-Drain Low-Side). Connect a resistor in series to set the LED current.	VLED	Logic
2	LL26	OUTs 2, 6 Status/Fault LED Cathode Output (Open-Drain Low-Side). Connect a resistor in series to set the LED current.	VLED	Logic
1	LL37	OUTs 3, 7 Status/Fault LED Cathode Output (Open-Drain Low-Side). Connect a resistor in series to set the LED current.	VLED	Logic
50	LL48	OUTs 4, 8 Status/Fault LED Cathode Output (Open-Drain Low-Side). Connect a resistor in series to set the LED current.	VLED	Logic
16	LHS1-4	OUTs 1-4 Status LED Anode Outputs (Open-Drain High-Side). Connect a resistor in series to set the LED current.	VLED	Logic
15	LHS5-8	OUTs 5-8 Status LED Anode Outputs (Open-Drain High-Side). Connect a resistor in series to set the LED current.	VLED	Logic
14	LHF1-4	OUTs 1-4 Fault LED Anode Connections (Open-Drain High-Side). Connect a resistor in series to set the LED current.	VLED	Logic
13	LHF5-8	OUTs 5-8 Fault LED Anode Connections (Open-Drain High-Side). Connect a resistor in series to set the LED current.	VLED	Logic

Functional Diagram



Detailed Description

The MAX22915 is an octal high-side switch with 250mΩ (max) on-resistance at T_A = +125°C. Per-channel diagnostics can be enabled through SPI to indicate open-wire with switches on, off or toggling up to 131Hz, overload, overcurrent, short-to-V_{DD}, as well as global diagnostics including supply undervoltage warning, chip temperature reporting, and communication error. An internal 7-bit ADC can be used to monitor chip temperature, supply voltage, or load current at each switch output. Active clamping limits the negative OUT_ voltage to (V_{DD} − V_{CLAMP}) and allows for freewheeling currents to demagnetize the inductive loads quickly. A watchdog timer monitors SPI and SYNCH activity and automatically turns the OUT_ switches off in case of missing SPI activity.

Synchronization

On the rising edge of the SYNCH logic input, all OUT_switches change to the new state previously programmed into the SET_OUT register. If SYNCH is held high, the OUT_ switches change state immediately when the SET_OUT register is written to (transparent mode).

When EN pin is low, all OUT_ are off independent of the SYNCH pin state and the SET_OUT register value.

Power-Up and Undervoltage Lockout

When the V_{DD}, V_{5ADC}, V_A, or V_L supply voltages are under their respective UVLO thresholds, all OUT_ switches are off and the open-wire detect current sources are turned off.

When both V_L and the internal supply voltage to the registers rise above their UVLO thresholds, the MAX22915 is ready for communication and the $\overline{\text{READY}}$ pin becomes passive low to indicate that the device is ready to communicate through the SPI interface.

In addressable SPI mode (DAISY = low), at power-up, the POR bit in the GLOBAL_ERR register is set to 1 and the $\overline{\text{FAULT}}$ output is set active-low. The POR bit and the $\overline{\text{FAULT}}$ pin are only cleared once the GLOBAL_ERR register is read. The POR bit = 1 signals that the register contents are in power-on-reset state and any custom configuration requires reprogramming.

When V_{DD} rises above the $V_{DD\_UVLO\_R}$ threshold, the OUT_ switches can operate normally. When V_{DD} falls below the $V_{DD\_UVLO\_F}$ threshold, the VDD_UVLO bit and $\overline{\text{FAULT}}$ pin are asserted, and all OUT_ switches are turned off. The register contents are lost when both V_A and V_{DD} drop below their undervoltage lockout thresholds.

When V_{M1} rises above its rising threshold, the $\overline{\text{VMOK}}$ pin is asserted low. When V_{M2} falls below its falling threshold, the $\overline{\text{VMOK}}$ pin is reset, as shown in *Figure 3*, the $\overline{\text{VM\_OK}}$ bit and $\overline{\text{FAULT}}$ pin are asserted, but the OUT_ switches continue to operate normally.

In daisy-chained SPI mode (DAISY = high), the $\overline{\text{READY}}$ and $\overline{\text{VMOK}}$ pins are active, but the $\overline{\text{FAULT}}$ pin does not signal supply undervoltage conditions.

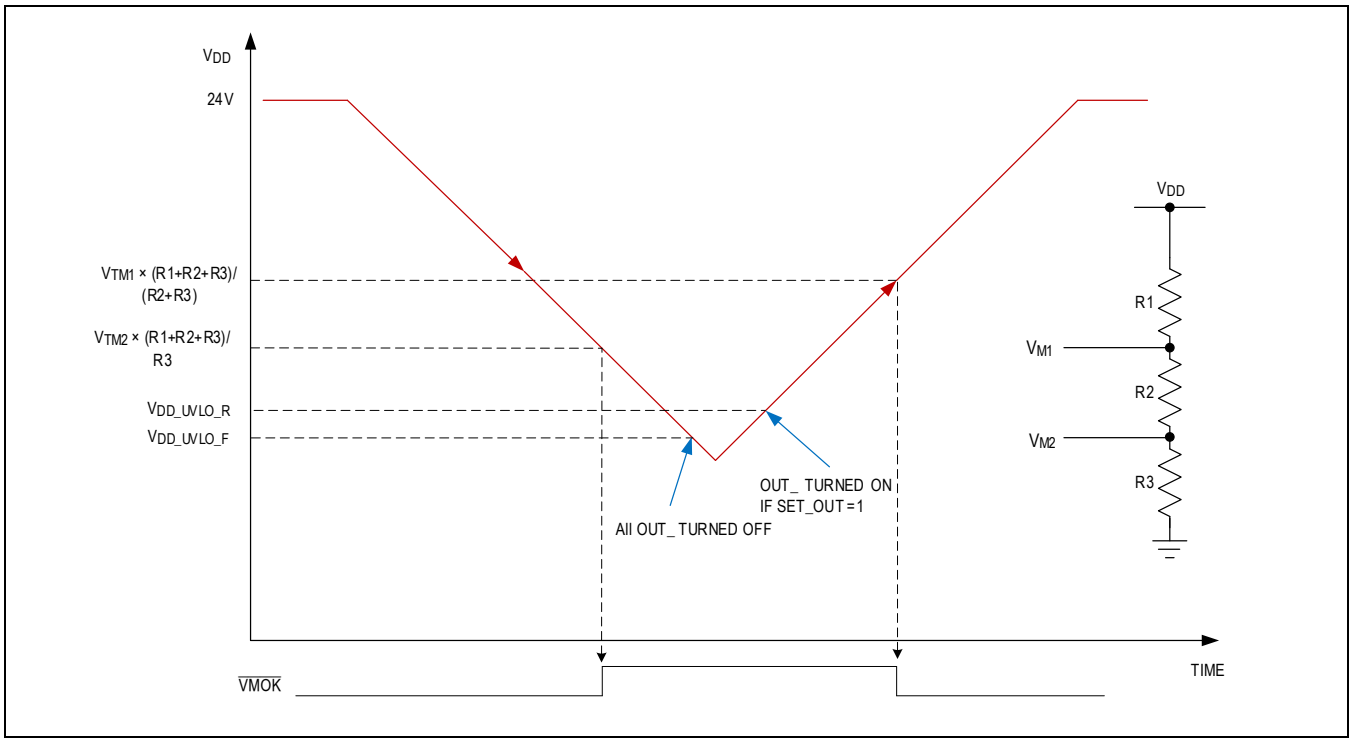


Figure 3. V_{DD} Monitoring

Current Limiting

Each high-side switch features active current limiting. When the load current exceeds 1A (typ), 0.7A (min), it is limited by the high-side switch. If the load tries to draw higher current, the voltage across the high-side switch increases, hence the temperature increases in accordance with its power dissipation, until thermal overload fault occurs and channel is turned off.

When an OUT_ channel shows an overcurrent, the CL_ bit is set in the CL_FLT register.

Channel Thermal Management

Every channel's temperature is constantly monitored. If the temperature of a driver rises above the thermal shutdown threshold of 150°C (typ), that channel is automatically turned off for protection. After the temperature drops by 15°C (typ), the driver turns on again.

When a driver turns off due to thermal shutdown, the per-channel overload bit, OVL_ in the OVL_FLT register, the OVL_FAULT bit in the INTERRUPT register, and the $\overline{FAULT}$ pin indicating this fault, are asserted, if not masked. For more details, see the Register Map section.

Chip Thermal Warning

The chip temperature warning is enabled through the THERM_WARN_EN bit in ADC_CONFIG1 register, and the temperature warning threshold is set through THERM_WARN_TH register between 85°C (typ) and 150°C (typ). When the chip temperature rises above the set threshold, the THERM_ERR bit in the INTERRUPT register and the $\overline{FAULT}$ pin are asserted. For more details, see the *Chip Temperature Measurement* section.

Chip Thermal Protection

When the chip temperature rises above the thermal shutdown threshold of 150°C (typ), the chip enters shutdown protection and all overloaded OUT_ switches are kept off until chip temperature drops below 140°C (typ). The THERM_SHTD bit in the GLOBAL_ERR register, THERM_ERR bit in the INTERRUPT register, and the $\overline{FAULT}$ pin are asserted.

If the chip temperature rises further above 165°C (typ) due to a short, an overload on the V_A regulator, or LED matrix, the internal V_A linear regulator, all OUT_ switches, and the LED matrix are shutdown to prevent part damage. In this condition,

the THERM_SHTD and THERM_ERR bits are already set, $\overline{FAULT}$ pin already asserted, and in daisy-chained SPI mode the F_ bits in SDO are all set to 1. The register contents are not lost in thermal shutdown if V_{DD} supply is present.

When the chip temperature then falls by the hysteresis amount, the V_A regulator turns on, LED matrix and OUT_ switches are restored to normal operation.

High On-Resistance

When the open-wire detection in switch on-state is enabled through OWON_ENABLE register and the output current is below 46mA (typ), the channel on-resistance is 1.5Ω (typ). When the output current rises above 38mA (min), the channel on-resistance goes back to normal operating mode at 0.12Ω (typ). This feature provides enhanced immunity to conducted RF noises.

Lamp Load Turn-On

Incandescent lamps initially draw high currents while their filament is cold, and this turn-on current reduces as the filament heats up. The MAX22915 has a scheme that automatically detects the presence of a lamps load. When a lamp load is detected, the overcurrent and overload faults are masked for a duration of 200ms (typ). The lamp load detection can be disabled through LAMP_DIS bit in CONFIG3 register.

Diagnostics

Table 1 lists the per-channel diagnostics made available by the MAX22915 and the state of the high-side switch for which diagnostics are determined. *Table 2* summarizes the global diagnostics.

Table 1. Per-Channel Diagnostics

PER-CHANNEL DIAGNOSTIC	SWITCH STATE	ENABLE	INTERRUPT MASK
Overload	Closed	By default	By OVL_M
Overcurrent	Closed	Per-channel	By CL_M
Open-Wire On	Closed	Per-channel	By OWON_M
Open-Wire Off	Open	Per-channel	By OWOFF_M
Short to V_{DD}	Open	Per-channel	By SHTVDD_M

Table 2. Global Diagnostics

GLOBAL DIAGNOSTICS	FUNCTION	ENABLED	FAULT INTERRUPT MASK
THERM_SHTD	Chip thermal shutdown	Always on	None
THERM_ERR	Chip thermal warning and thermal shutdown	Thermal warning enabled by THERM_WARN_EN Thermal shutdown always on	None
THERM_WARM	Chip thermal warning	By THERM_WARN_EN	None
POR	Undervoltage on the internal supply to registers	Always on	None
VA_UVLO	V_A in undervoltage	Always on	SUPPLY_ERR_M
$\overline{VM\_OK}$	Low V_{M1}, V_{M2} warning	Always on	VMOK_M
VDD_UVLO	V_{DD} in undervoltage, all OUT_ switches off	Always on	SUPPLY_ERR_M
SUPPLY_ERR	V_{DD}, V_A in undervoltage, low V_{M1}, V_{M2}	Always on	SUPLLY_ERR_M
WD_ERR	SPI has no/incomplete activity for the timeout period	By WD_TIMEOUT[1:0] (DAISY = low) By A0/WDEN (DAISY = high)	COM_ERR_M
SYNCH_ERR	SYNCH pin stuck low for the timeout period	By SYNCH_WD_EN	COM_ERR_M
COM_ERR	SPI CRC or communication error	By CRCEN pin	COM_ERR_M

For more details on these diagnostic bits, see the Register Map section.

Diagnostic Filtering

Open-wire detection in switch off-state and short-to-V_{DD} detection, in conjunction with reactive loads, can take many milliseconds to settle to stable conditions after a change of high-side switch state. During this time, diagnostic detection does not generate reliable results. Therefore after the OUT_ switching-off instant, a blanking period selected by OW_BLANK_TM[4:0] bits in the CONFIG3 register configures the time period during which these diagnostics are not evaluated. After this blanking time, a filter is engaged for 64µs (typ), after which the open-wire off and short-to-V_{DD} diagnostics are determined and updated as per-channel diagnostics in the OWOFF_FLT and SHTVDD_FLT registers. In addition the OWOFF_FAULT and SHTVDD_FAULT bits in the INTERRUPT register, the fault LEDs (FLEDs) if FLED_SET = 0, and the diagnostic bits in the SDO data (if read) are updated. For the overload and overcurrent diagnostics, a 64µs (typ) filter time is employed and there is no blanking time.

When an OUT_ switch changes its on/off state, the diagnostic results of the previous state is cleared internally, the diagnostic bits are auto-cleared if FLATCH_EN in CONFIG1 register is set to 0. If FLATCH_EN is set to 1, the diagnostic bits are cleared by an SPI read command.

Diagnostic Bit Behavior

The per-channel diagnostic bits (OVL_, CL_, OWOFF_, OWON_, and SHTVDD_) can be configured to be latched or real-time through the FLATCH_EN bit in the CONFIG1 register. When latched diagnostics are enabled (FLATCH_EN = 1), the diagnostic bits are set to 1 when a fault is detected, and remains at 1 even if the fault disappears. This bit is only reset to 0 when the cause of the fault has disappeared AND the relevant fault register is read through SPI in addressable SPI mode. If the case of the fault has not disappeared, the real-time fault keeps the diagnostic bit at 1.

In daisy-chained SPI mode, the $\overline{\text{FAULT}}$ pin and F_ bits in SDO are cleared on the following SPI cycle if fault condition is removed.

The per-channel faults in each of the five error registers are logically OR'ed together to produce the fault bits in the INTERRUPT register. *Figure 4* shows this on the basis of overload diagnostics.

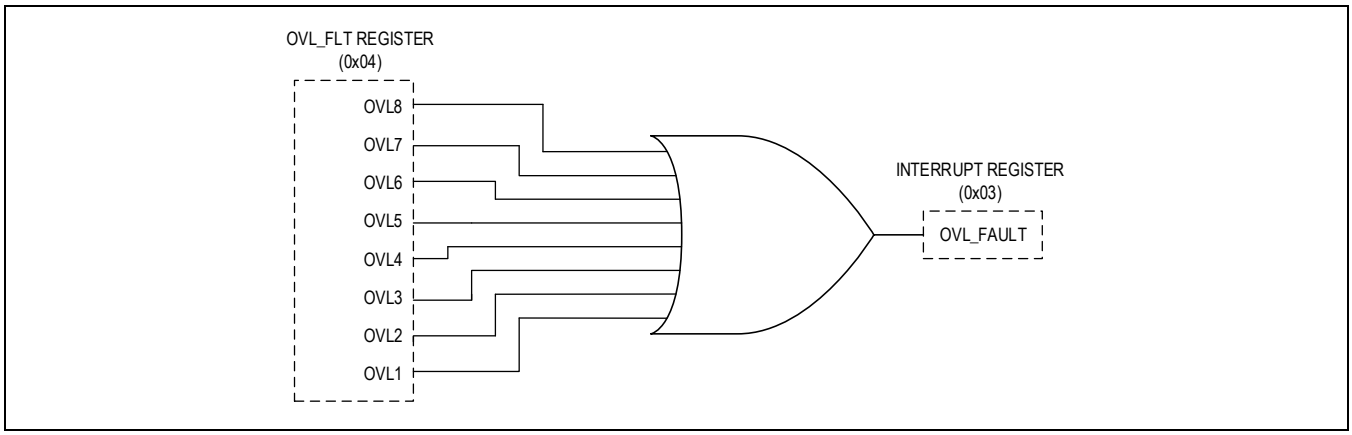


Figure 4. Overload Interrupt Diagnostic Scheme

$\overline{\text{FAULT}}$ Pin Signaling

The $\overline{\text{FAULT}}$ pin is an open-drain logic output that transitions active low when a fault condition is detected. The source of faults are the 8 bits in the INTERRUPT register: per-channel faults and global faults, as shown in *Figure 5*. The source of $\overline{\text{FAULT}}$ can be masked through the MASK register. In addressable SPI mode, the diagnostics can be latched (FLATCH_EN = 1), in which case the $\overline{\text{FAULT}}$ pin can only be cleared by reading both the INTERRUPT register and the corresponding fault register(s), whose fault is latched in the INTERRUPT register. In this case, the $\overline{\text{FAULT}}$ pin cannot be cleared by only reading the INTERRUPT register. If FLATCH_EN = 0, then the diagnostic bits, the INTERRUPT register bits and the $\overline{\text{FAULT}}$ pin are not latched, so are real time.

In daisy-chained SPI mode, the $\overline{\text{FAULT}}$ pin is latched, and cleared on the next SPI cycle if the cause of the fault has disappeared.

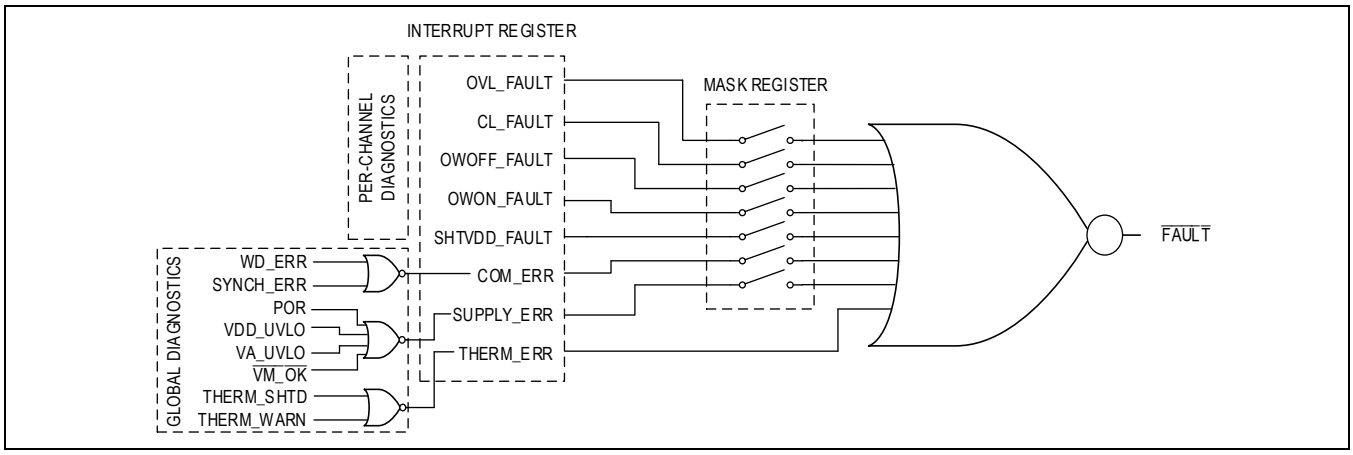


Figure 5. $\overline{FAULT}$ Signaling Scheme

Short-to-V_{DD} Detection

The MAX22915 can detect shorts-to-V_{DD}, if enabled through SPI. This diagnostic only works when an OUT_ switch is off. If the OUT_ voltage is higher than the threshold voltage set by the SHTVDD_TH[1:0] bits in CONFIG2 register, the SHTVDD_FAULT bit in the INTERRUPT register is asserted, and SHTVDD_ bit in the SHTVDD_FLT register is set to 1, as well as the $\overline{FAULT}$ output pin driven low (if not masked).

The SHTVDD_TH[1:0] bits set the short-to-V_{DD} threshold to 9V, 10V, 12V, or 14V when V_{DD} is above 16V (typ). For V_{DD} below 16V (typ), the short-to-V_{DD} threshold is always set to 9V regardless of the SHTVDD_TH[1:0] bits.

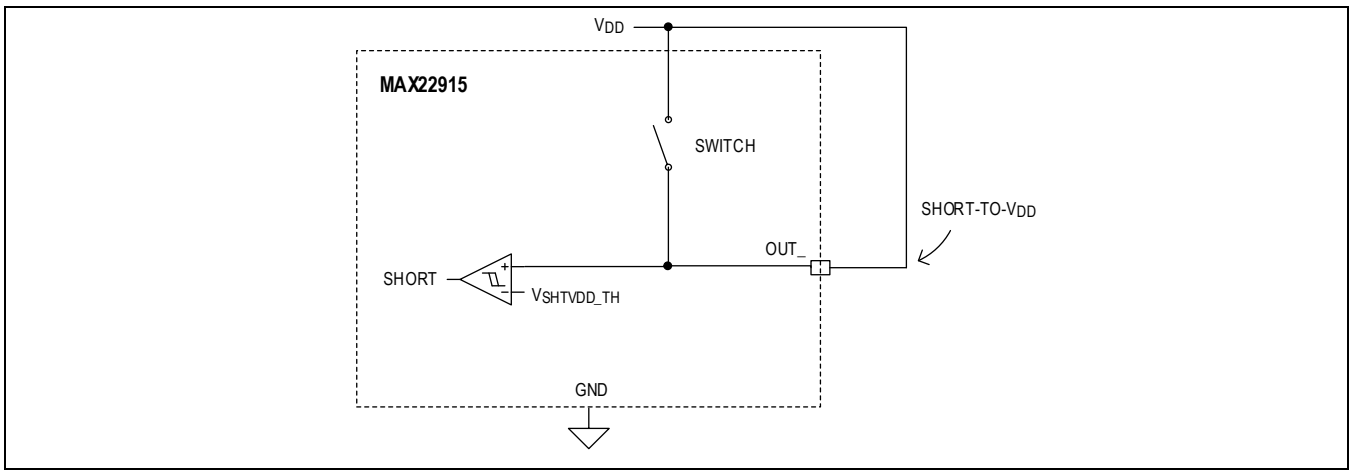


Figure 6. Short-to-V_{DD} Detection Scheme

Open-Wire Detection

Monitoring of an open-wire load condition can be enabled on a per-channel basis through SPI serial configuration. Open-wire detection can be selected for either, or both, of the cases with a high-side switch in the on and/or off state. Moreover, the MAX22915 provides enhanced conducted RF immunity to open-wire detection for high-side switch toggling between on and off states up to 131Hz.

Open-Wire Detection with Switch On

Open-wire detection can be enabled on any OUT_ switch through the OWON_EN_ bits in the OWON_ENABLE register. When the high-side switch is closed, the load current flowing out of the high-side switch is monitored. If this current drops below the threshold value set through the resistor connected to the OWONSET pin, an open-wire fault is reported in OWON_FLT register. The OWONSET resistor selects a load current threshold in the range of 0.44mA (typ) to 2.4mA (typ) using the following equation:

Load current threshold (mA) = 57.52 × $R_{OWONSET}$ (kΩ)^ -0.961.

The time for open-wire on fault diagnostic, from the OUT_ switch is turned on, is divided into a user-configurable channel on-delay and an open-wire on detection time, as shown in *Figure 7*.

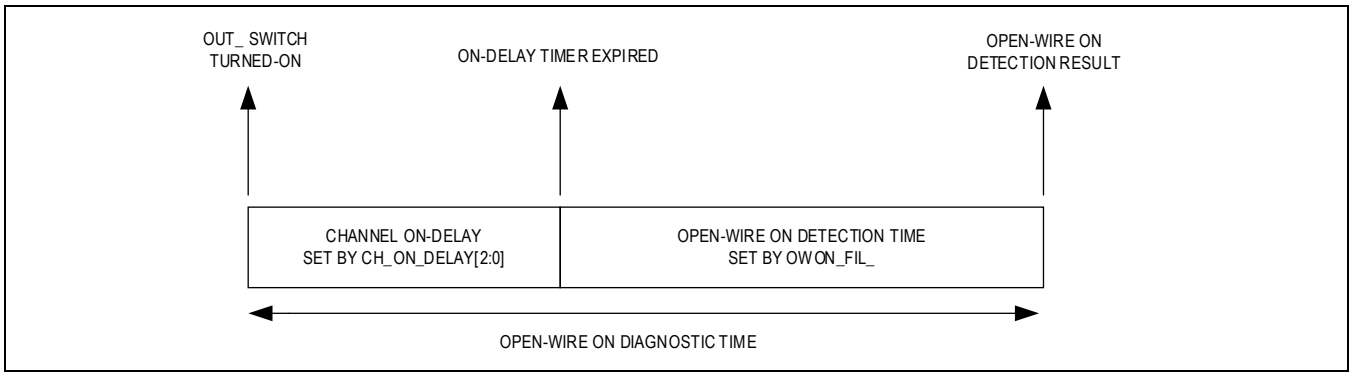


Figure 7. Open-Wire ON Fault Diagnostic Time

The channel on-delay timer can be configured by the CH_ON_DELAY[2:0] bits in the ADC_CONFIG3 register between 0.5ms (typ) and 100ms (typ). Once this timer has expired and open-wire on is enabled, the channel is considered fully turned on, and open-wire on detection starts the diagnostics and provides the result after a time interval set by OWON detection time. The per-channel open-wire on detection time can be configured by the OWON_FIL_ bit in OWON_FILTER register:

- Set OWON_FIL_ = 0 to set the open-wire on detection time to 3ms (default).
- Set OWON_FIL_ = 1 to set the open-wire on detection time to 1ms.

If the channel load current comes back after the open-wire on detection completes is below 46mA (typ), the on-resistance of the switch increases to 1.5Ω (typ) and the open-wire on detection is reset and restarted.

For example, if the channel on-delay timer has been set to its minimum value at 0.5ms (typ), and the open-wire on detection time has been set to 3ms (typ) by default, the total time interval rquired to report an open-wire on fault on an OUT_ switch starting from its turning-on is 0.5ms + 3ms + 3ms = 6.5ms.

If required, the open-wire on diagnoistic time can be reduced. Set FAST_DET_MODE bit in CONFIG3 register to 1 to halve the open-wire on detection time. Note that this mode option is applied to all OUT_ switches. Therefore assuming FAST_DET_MODE option is enabled, the open-wire diagnostic time in the previous example is changed:

- Open-wire on diagnostics time is 0.5ms + 3ms + 3ms = 6.5m with FAST_DET_MODE = 0.
- Open-wire on diagnostics time is 0.5ms + 3ms = 3.5ms with FAST_DET_MODE = 1.

Table 3 shows the timing parameters with the related fields and registers. *Table 4* shows the possible combinations based on the value assumed by the parameters.

Table 3. Open-Wire On Timing Parameters

PARAMETER NAME	DESCRIPTION
Channel On-Delay Timer	Time interval required to consider OUT_ switch fully enabled starting from its turning-on. It can be set by the user by means of the field CH_ON_DELAY[2:0].
Open-Wire On Detection Time	Time required to provide the result of the open-wire on detection result starting from when the OUT_ switch is fully enabled. It can be set per-channel by means of the register OWON_FILTER.
Output FET Mode Option	Option which allows to halve the open-wire on detection time. Set FAST_DET_MODE = 1 to enable this option.
Open-Wire On Diagnostics Time	Channel On-Delay Timer + Open-wire On Detection Time.

Table 4. Open-Wire On Timers

OPEN-WIRE ON FILTER TIME OWON_FIL_, ms	FAST_DET_MODE	OPEN-WIRE ON DETECTION TIME (ms)	OPEN-WIRE ON DIAGNOSTICS TIME (ms)
0b, 3ms	0b	6	6.5
1b, 1ms	0b	2	2.5
0b, 3ms	1b	3	3.5
1b, 1ms	1b	1	1.5

Note that for each case the channel on-delay timer is assumed equal to its minimum value at 0.5ms (typ). This is configured by default by setting CH_ON_DELAY[2:0] bits to 000b.

Figure 8 shows the relationship between the OUT_ switch status and the open-wire on fault state. If the OUT_ switch is always on and the FAST_DET_MODE option is disabled, assuming the channel on-delay timer has expired, the load current is instantly compared with the set threshold. After the open-wire on detection time, the OWON_ bit in the OWON_FLT register updates according to the load current condition.

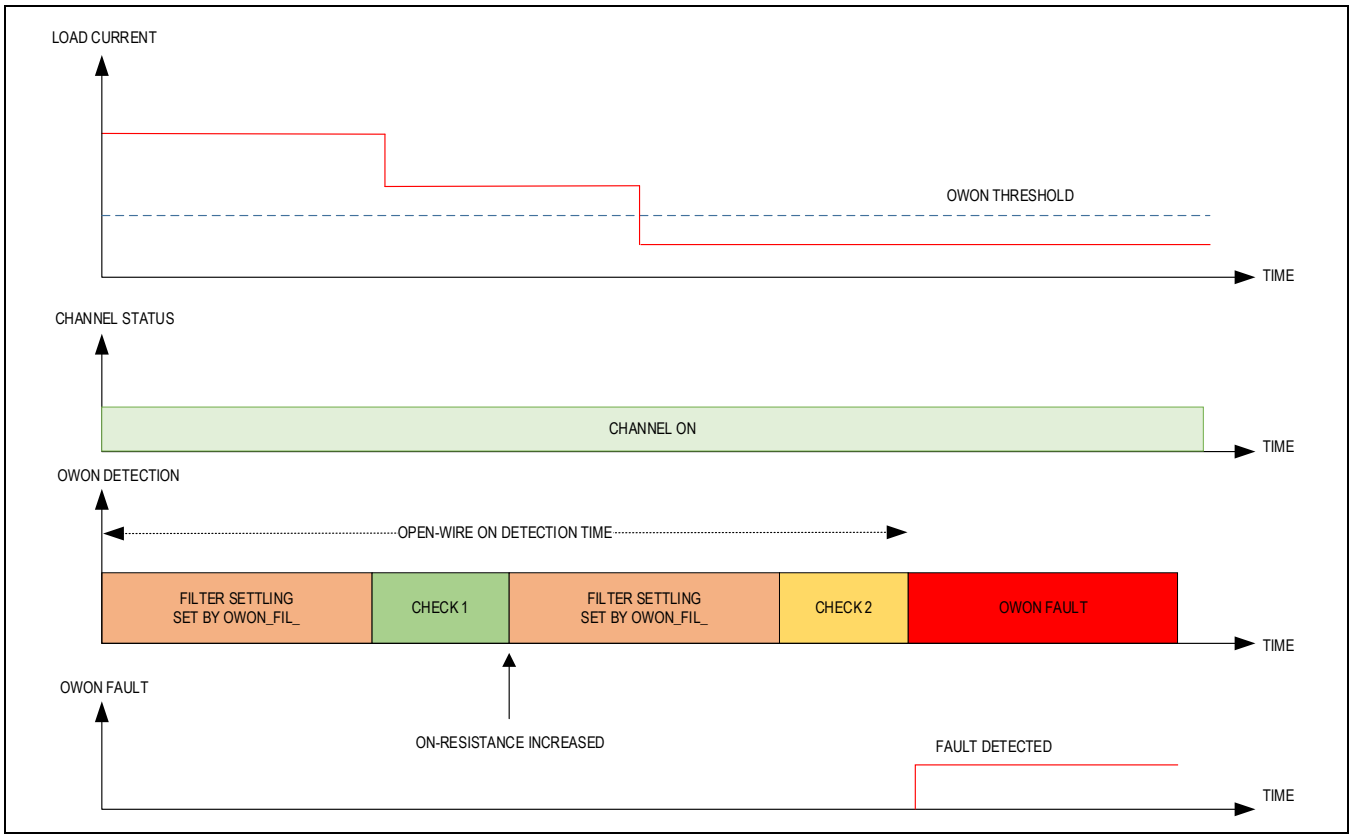


Figure 8. Open-Wire On Detection with Fast Detection Mode Disabled

Figure 9 shows the condition in which the OUT_ switch is initially turned on, and the FAST_DET_MODE option is enabled, the open-wire on detection time is halved when the OUT_ switch is turned on next time.

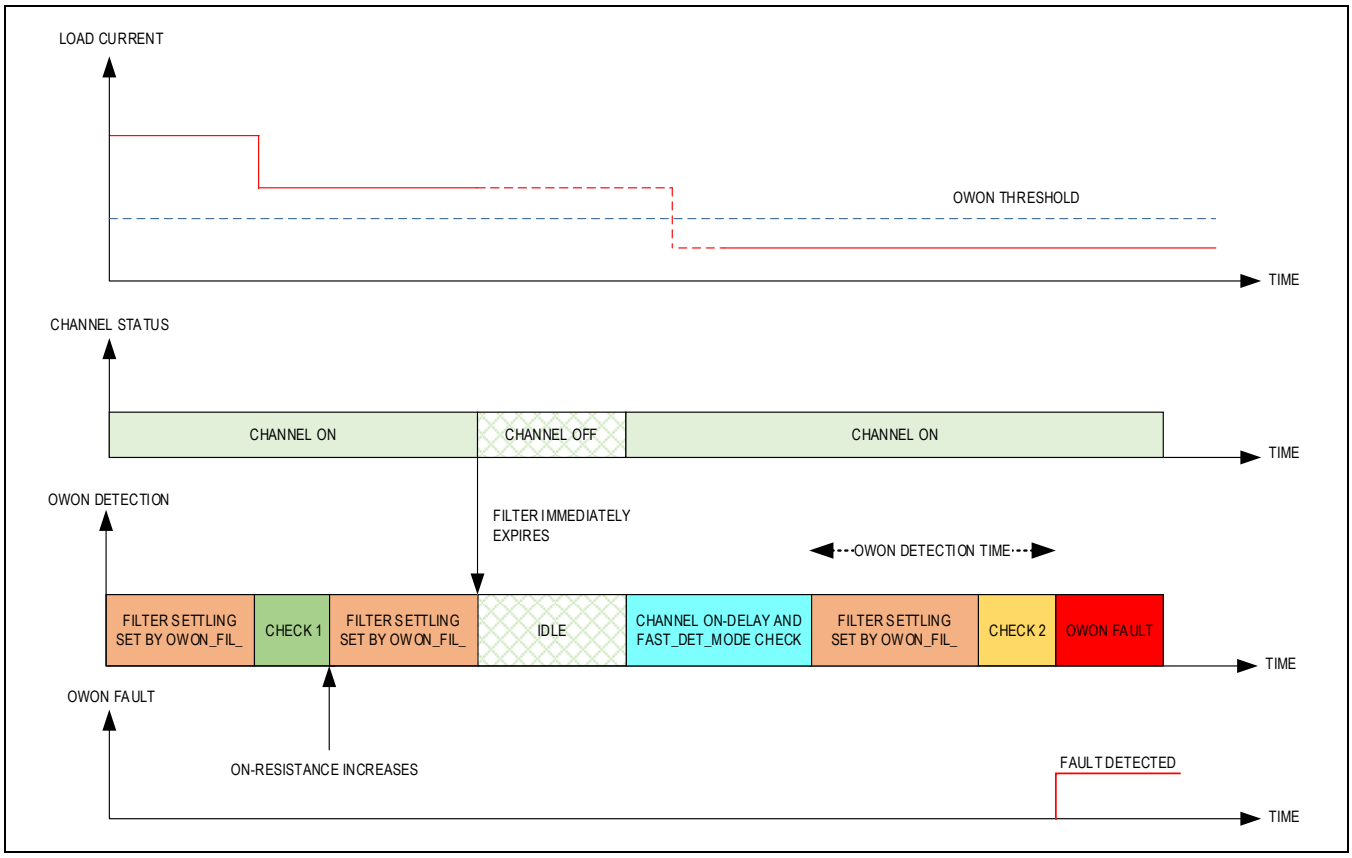


Figure 9. Open-Wire On Detection with FAST DETECTION MODE Enabled

Open-Wire Detection with Switch Off

Monitoring of an open-wire condition in the switch off-state can be enabled on individual channels through the OWOFF_EN_ bits in the OWOFF_ENABLE register. When the high-side switch is off, a weak current source/sink, I_{PU_OWOFF}, is enabled that pulls OUT_ to 7V (typ) during an open-wire fault when a load is missing. If the OUT_ voltage is above 5V (min), an open-wire off fault is asserted in OWOFF_FLT register, as well as OWOFF_FAULT bit in INTERRUPT register and the $\overline{FAULT}$ pin. The I_{PU_OWOFF} current source is configured through the OWOFF_CS[1:0] bits in the CONFIG2 register. For more details, see *Figure 10*.

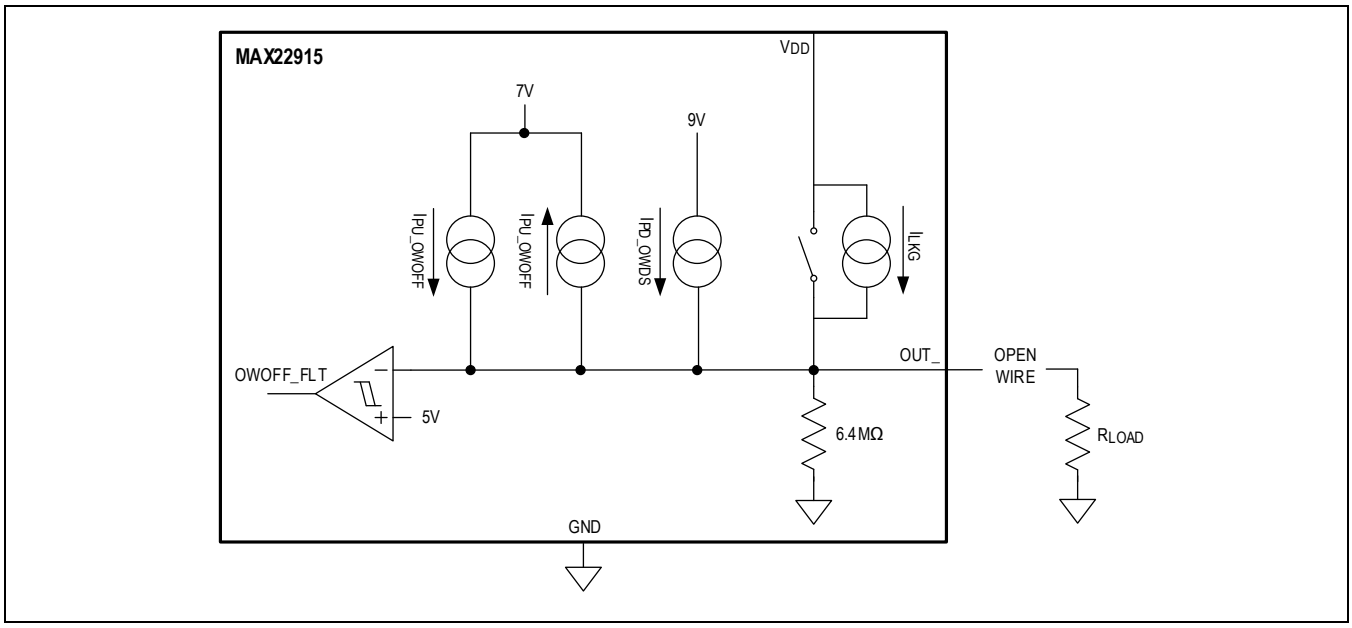


Figure 10. Open-Wire Off Detection Scheme

An additional pull-down current sink, I_{PD_OWDS}, can be enabled to assist discharging of capacitance on OUT_ to allow for faster open-wire off detection after switch is turned off. The pull-down current source can by turned on by setting the OWOFF_DS[1:0] bits in the CONFIG1 register, and it is automatically turned off when OUT_ voltage falls below 9V (typ). Both current sources are enabled only when open-wire off detection is enabled.

Open-Wire Detection with Switch Toggling

The MAX22915 supports open-wire diagnostic when OUT_ switches are toggling at up to 131Hz. In switch on-state, the minimum open-wire diagnostic time is limited by channel on-delay timer and open-wire on detection time. For more details on timing analysis, see the *Open-Wire Detection with Switch On* section. Use these following options to reduce the diagnostic time:

- Enable FAST_DET_MODE to halve open-wire on detection time.
- Set shorter channel on-delay timer through CH_ON_DELAY[2:0] bits.
- Set shorter open-wire on detection time through OWON_FIL_ bit.

In switch off-state, the minimum open-wire diagnostic time is limited by the rate at which OUT_ switch discharges. Use these following options to accelerate the discharging of capacitive loads:

- Set higher pull-up current through OWOFF_CS[1:0] bits.
- Set higher pull-down current through OWOFF_DS[1:0] bits.

Blanking Time for Open-Wire with Switch Off and Short-to-V_{DD}

After the channel is turned off, assume the open-wire off and short-to-V_{DD} diagnostics are enabled, both faults are not asserted until a blanking time, specified by the OW_BLANK_TM[7:3] bits in the CONFIG3 register, expires. This allows user to delay these faults from reporting before OUT_ switches discharge and become stable. *Figure 11* shows the blanking time for open-wire off detection after channel is turned off.

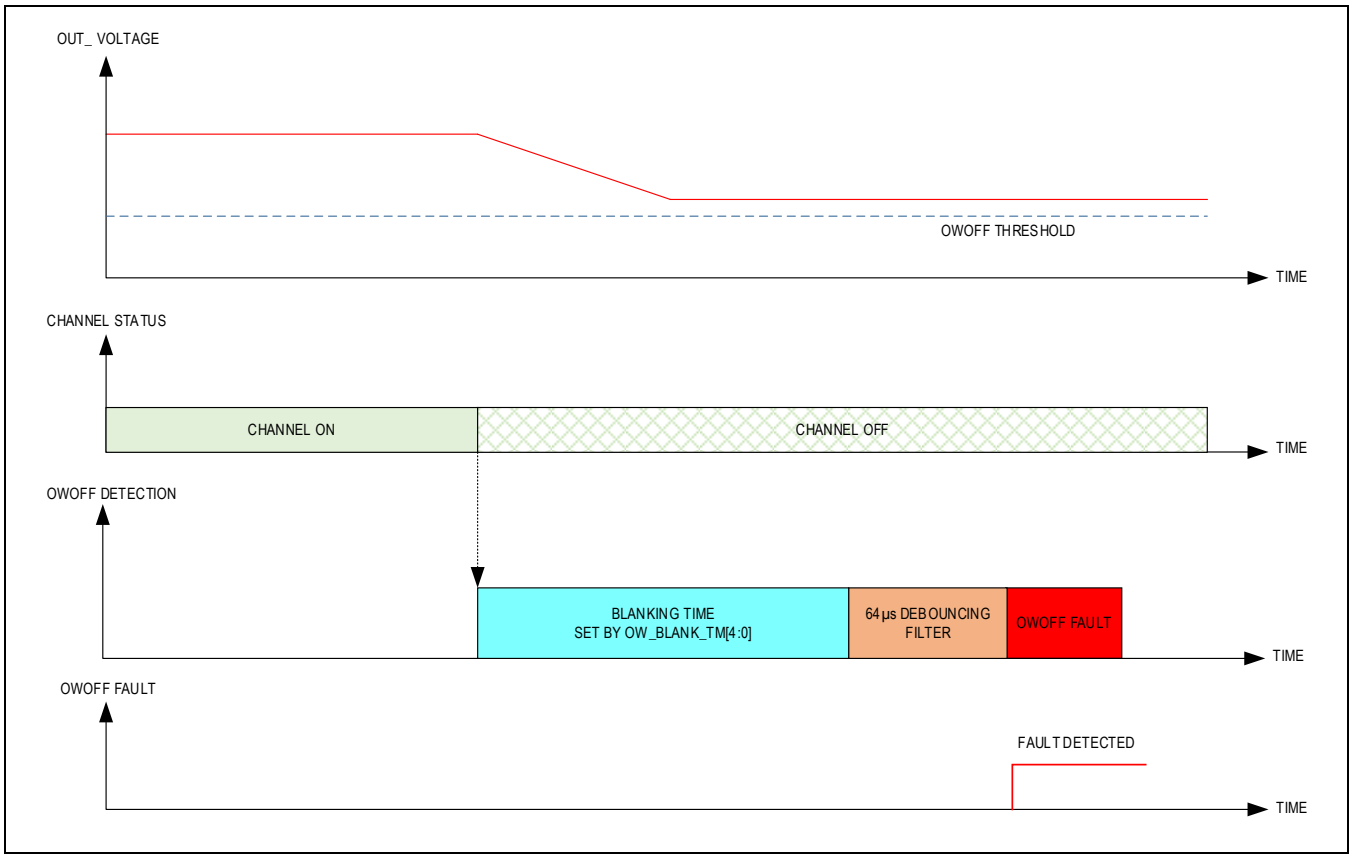


Figure 11. Open-Wire Off Fault Blanking Time

The OW_BLANK_TM_EN bit in CONFIG3 register is used to enable the blanking function. If the blanking time is not enabled, open-wire off and short-to-V_{DD} faults are asserted shortly after the debouncing filter time of 64µs (typ).

Watchdog

The MAX22915 provides two watchdog timers to allow monitoring activity on the SPI interface and on SYNCH pin. In daisy-chained SPI mode, drive A0/WDEN to enable the watchdog for SPI. In addressable SPI mode, the watchdog timer is enabled through the WD_TIMEOUT[1:0] bits, monitors and expects clock activities on the SCLK and $\overline{CS}$ inputs. At least one valid SPI cycle must be detected in the watchdog timeout period. This means that the SCLK input must have a multiple of 8 clock cycles during a $\overline{CS}$ low period.

The SYNCH pin watchdog can be enabled by SYNCH_WD_EN bit and monitors the SYNCH pin whether or not stuck low. At least one 1µs (typ) SYNCH high period must be detected in the 50ms (typ) watchdog timeout period, to avoid SYNCH pin watchdog error. When SYNCH pin watchdog is enabled, watchdog for SPI is always enabled. For more details on selecting timeout period, see the Register Map section.

In daisy-chained SPI mode, the SPI watchdog timeout is 50ms (typ) and SYNCH pin watchdog is disabled.

If the watchdog criterion is not met, all OUT_ switches are automatically turned off and the $\overline{FAULT}$ pin is asserted. In addressable SPI mode, the WD_ERR, SYNCH_ERR, and COM_ERR bits are set to 1, and all registers, except the INTERRUPT, OVL_FLT, CL_FLT, OWOFF_FLT, OWON_FLT, SHTVDD_FLT, GLOBAL_ERR, and MASK registers, are reset and all status and fault LEDs are turned off. When all bits at SYNCH_WD_EN and WD_TIMEOUT[1:0] are set to 1, the MAX22915 instantly times out and resets to the same state as seen under a watchdog fault, with the exeception of asserting WD_ERR, SYNCH_ERR, COM_ERR bits, and $\overline{FAULT}$ pin.

LED Driving Matrix

The 4x4 LED driver crossbar matrix offers an efficient configuration for driving up to 16 LEDs. The LEDs can either be turned on/off by the SPI controller by setting the SET_SLED and/or SET_FLED register bits in addressable SPI mode, or can be controlled by the MAX22915 autonomously to indicate per-channel status and fault conditions, which depends on

the setting of bits SLED_SET and FLED_SET in the CONFIG1 register. If controlled internally (SLED_SET= 0 or FLED_SET= 0), a channel's status LED automatically turns on when the corresponding OUT_ switch is on and there is no fault condition. If diagnostics detection is enabled on any OUT_ switch and a fault is detected, its associated fault LED (FLED) turns on and its associated status LED (SLED) is automatically turns off. This means that for any OUT_ channel, its SLED and FLED never turn on simultaneously. If FLED_SET = 0, diagnostics that are enabled (SHTVDD_FAULT, OWON_FAULT, OWOFF_FAULT, CL_, or OVL_) result in FLEDs turning on when a fault is detected. Only overcurrent detection can be masked from driving the FLEDs through the LED_CL bit in the CONFIG2 register.

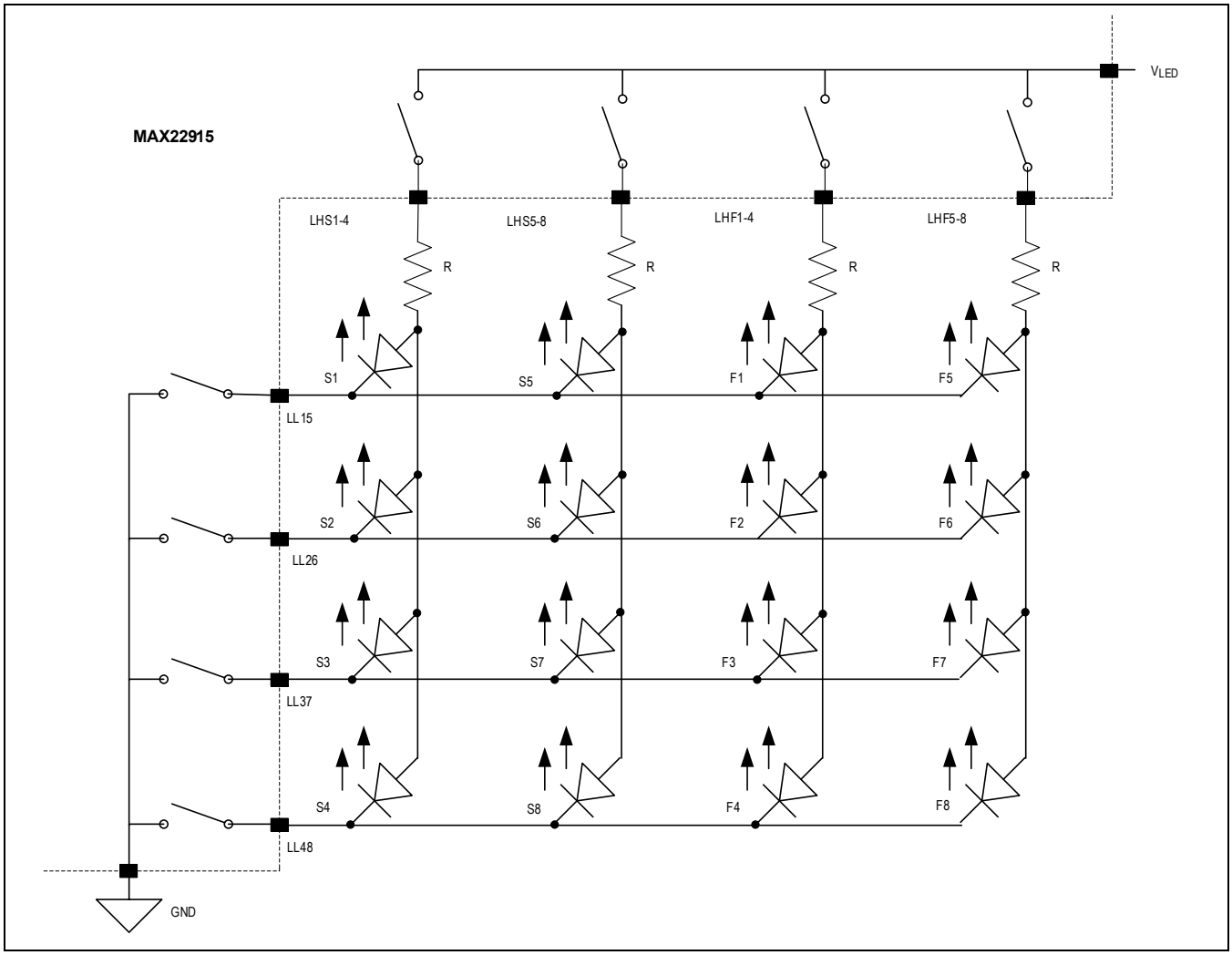


Figure 12. LED Matrix Scheme

When a lamp load is detected during OUT_ switch turns on, overload and overcurrent faults are masked, and its SLED turns on and its FLED stays off for 200ms (typ).

If the FLEDs are controlled internally, they are always filtered, both in daisy-chained and addressable SPI modes. When controlled internally, the FLED minimum on-time can be configured through the FLED_STRETCH[1:0] bits in the CONFIG1 register. For FLED stretching in a single fault condition, see *Figure 13*. When the fault occurs, the FLED stretching counter starts and the output FLED turns on until the counter reaches the stretching time set by the FLED_STRETCH[1:0] bits. If the fault occurs again within the stretching time, the FLED stretching counter is reset and restarted. If the fault condition does not disappear at the end of FLED stretching time, the FLED stays on. For FLED streching in multiple faults condition, see *Figure 14*.

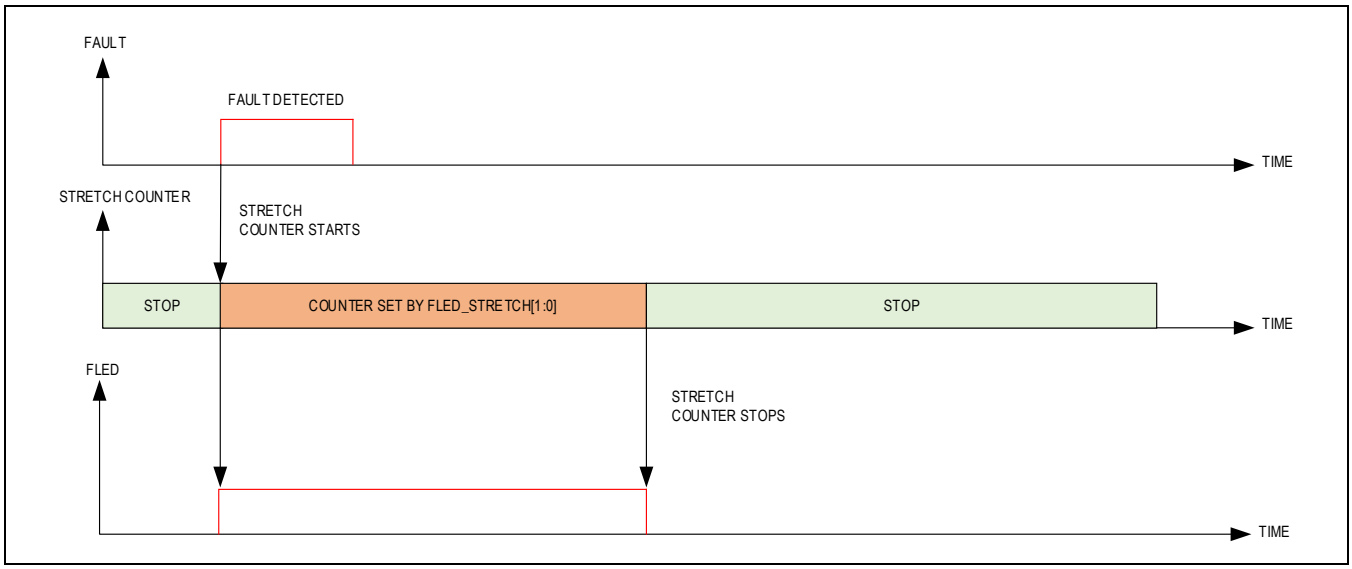


Figure 13. Single FLED Stretching

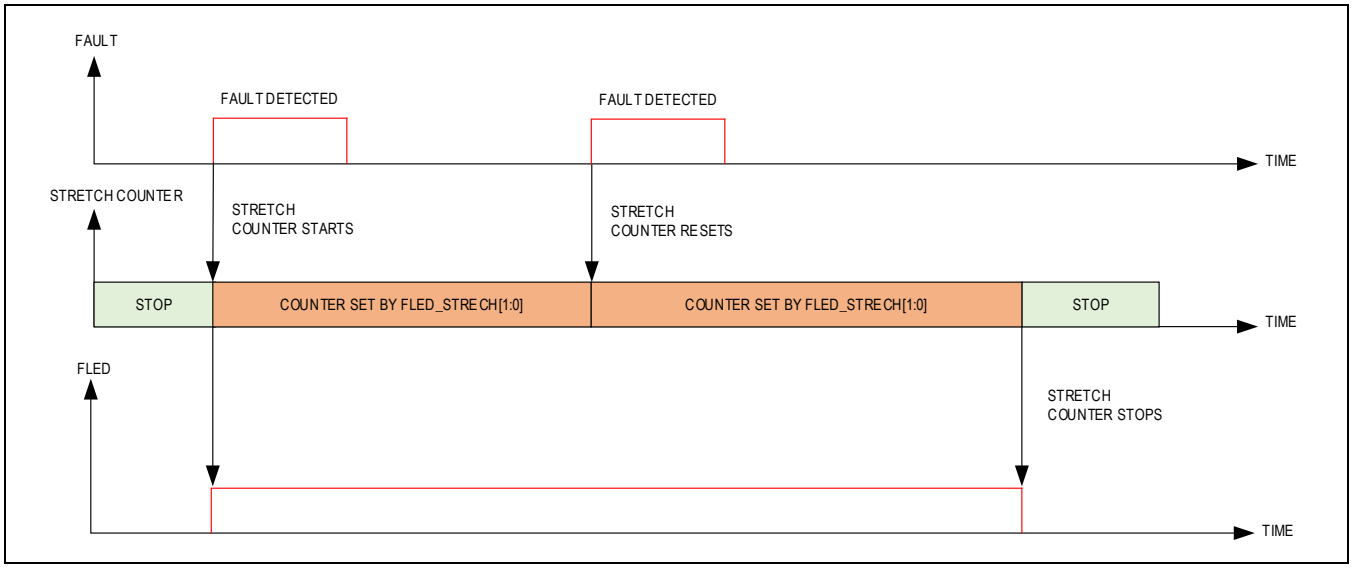


Figure 14. Multiple FLED Stretchings

The SLEDs are real-time when controlled internally. The LED matrix is powered by the V_{LED} supply input, which can be in the range from 3.0V (min) up to the V_{DD} field supply voltage.

If daisy-chained SPI mode is selected (DAISY = high), the LED matrix is always controlled autonomously by the MAX22915. Only overload faults are signaled at FLEDs and they are stretched by 2s. For every current limiting resistor, R, each of the four LEDs in a column string is pulsed for a quarter of the time, so that current only flows through one LED and its resistor at one time. Thus the resistors, R, determine the current through one LED during the pulse. Each LED is pulsed on at a rate of 1kHz (typ) and is on for 25% of the 1ms period. Thus the average current flowing through a LED that is turned on, is about $0.25 \times (V_{LED} - V_F)/R$, where V_F is the forward voltage of the LED. Choose the resistor value R according to the LED's current/light intensity requirements.

Monitoring of Load Currents, V_{DD} Supply, and Chip Temperature

The MAX22915 features an internal 7-bit ADC to monitor the load current at each channel, V_{DD} supply voltage, or chip temperature. The ADC is available in on-demand or continuous mode operation, with an option to average multiple current or temperature measurements.

Monitoring and Operating Modes

The MAX22915 internal ADC monitors three different variables using a scheduling process with a multiplexer. For more details on the channel scheduler, see *Figure 15* and for more details on the multiplexer, see *Figure 18*. A total of 10 channels are monitored and measured, if enabled and selected, including load current measurement at Channel 0 to Channel 7 corresponding to OUT1 to OUT8, V_{DD} measurement at Channel 8, and chip temperature measurement at Channel 9. Each of these channel has its own operating modes and configuration settings, as shown in *Table 5*.

Table 5. ADC Measurement Channels and Modes

CHANNEL	MEASUREMENT	MODE	CONFIGURATION
Channel 0	Load current at OUT1	Continous, on-demand, single	Average up to 128 samples, per-channel enable, channel turn-on delay
Channel 1	Load current at OUT2		
Channel 2	Load current at OUT3		
Channel 3	Load current at OUT4		
Channel 4	Load current at OUT5		
Channel 5	Load current at OUT6		
Channel 6	Load current at OUT7		
Channel 7	Load current at OUT8		
Channel 8	V_{DD} supply voltage	Continuous, on-demand	N/A*
Channel 9	Chip temperature	Continuous, on-demand	Average up to 128 samples

(*)N/A means not applicable.

The channel scheduler (*Figure 15*) is equipped with an internal pointer and iteratively checks each channel. If the channel checked is the current sense (Channel 0 to Channel 7), the ADC only proceed to measure if all the following criterion are met:

- The channel is turned on for an interval greater than the channel on-delay timer defined by the CH_ON_DELAY[2:0] bits in ADC_CONFIG3 register. The channel is considered fully enabled.
- Its CURR_MEAS_EN_ bit is set to 1 in CURR_MEAS_ENABLE register.
- Operating mode is set.

If the channel checked is the voltage sense (Channel 8), the ADC measures V_{DD} supply voltage if VDD_ON_DEMAND bit or VDD_CONT bit is set to 1. If the channel checked is the temperature sense (Channel 9), the ADC measures the die temperature if TEMP_ON_DEMAND or TEMP_CONT bit is set to 1.

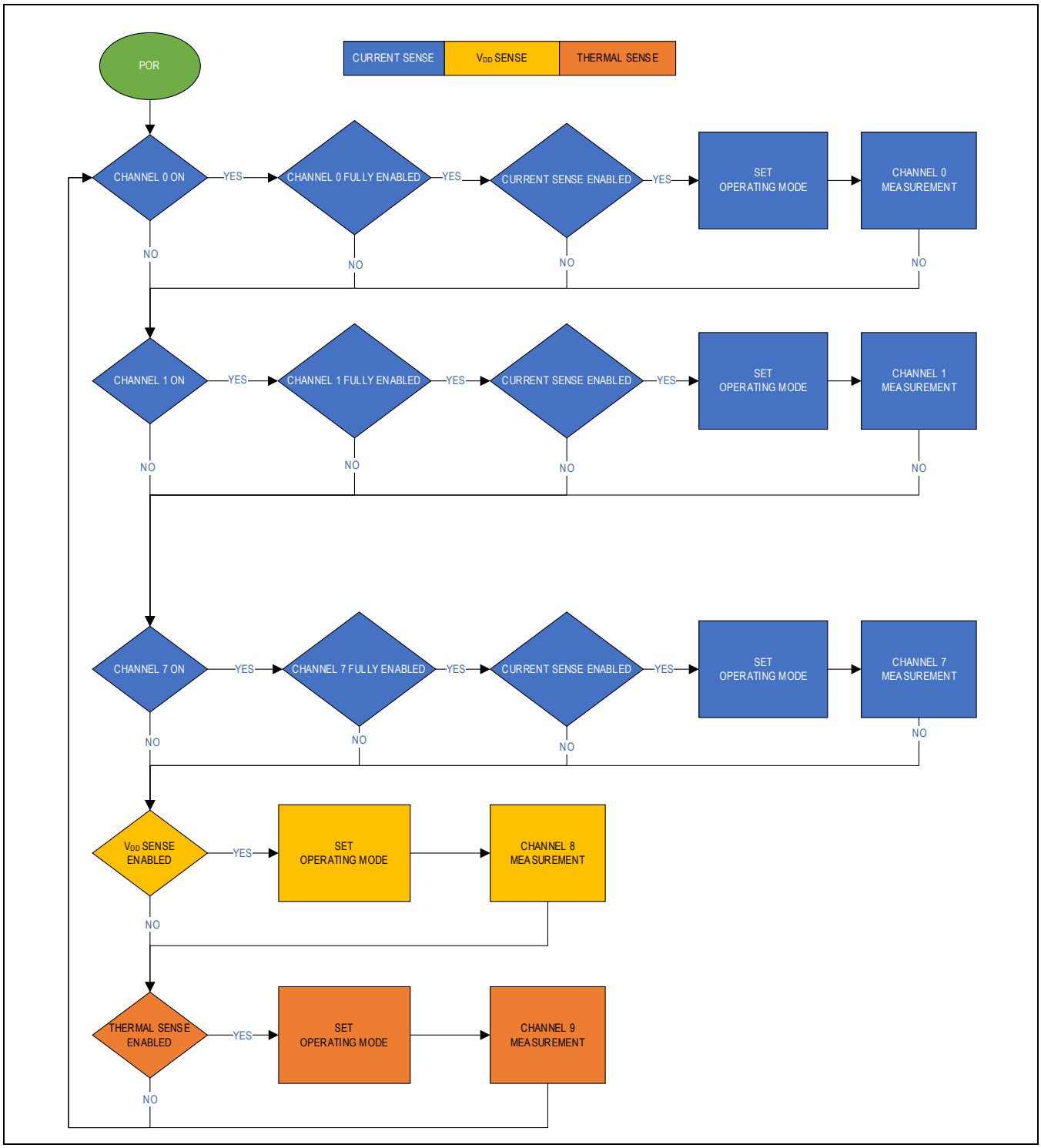


Figure 15. ADC Measurement Scheduler

Independent of the channel to be measured, the actual measurement is always preceded by the operating mode setting. To provide flexible monitoring, three operating modes can be set among continuous mode, on-demand mode, and single mode (current sense only). *Table 6* shows each measurement and its available option modes.

Table 6. ADC Operating Modes

MEASUREMENT	CONTINUOUS MODE	ON-DEMAND MODE	SINGLE MODE
Load Current	The scheduler sequentially checks each high-side switch and ADC measures the load current, if it is fully enabled. This is enabled by setting CURR_CONT bit to 1 in ADC_CONFIG2 register.	The scheduler sequentially checks each high-side switch and ADC makes a single measurement of the load current, if it is fully enabled. This is enabled by setting CURR_ON_DEMAND bit to 1 in ADC_CONFIG2 register. The current sense is selected by setting CH_READ_SEL[3:0] bits in register ADC_CONFIG3, to required channel.	The scheduler sequentially checks each channel and ADC measures only once, if it is fully enabled. This is enabled by setting CURR_SINGLE bit to 1 in ADC_CONFIG2 register. After single mode is enabled, each fully enabled channel is measured only once, until the next time it turns on.
V_{DD} Supply Voltage	The ADC measures the V_{DD} supply voltage each time the scheduler checks Channel 8. This is enabled by setting VDD_CONT bit to 1 in ADC_CONFIG1 register.	The ADC makes a single measurement of the V_{DD} supply voltage. This is enabled by setting VDD_ON_DEMAND bit to 1 in ADC_CONFIG2 register. The voltage sense is selected by setting CH_READ_SEL[3:0] bits to 0x8 in ADC_CONFIG3 register.	Not available.
Chip Temperature	The ADC measures the die temperature each time the scheduler checks Channel 9 and the temperature timer is expired. This is enabled by setting TEMP_CONT bit to 1 in ADC_CONFIG1 register. Temperature timer is fixed at 100ms (typ), much slower than the scheduler to avoid measuring temperature in every scheduler iteration cycle.	The ADC makes a single measurement of the die temperature. This is enabled by setting TEMP_ON_DEMAND bit to 1 in ADC_CONFIG1 register. The temperature sense is selected by setting CH_READ_SEL[3:0] bits to 0x9 in ADC_CONFIG3 register.	Not available.

Load Current Measurement

The MAX22915 integrates enhanced diagnostics features, which allow to monitor the load current at each of eight channels by means of three different operating modes among continuous mode, on-demand mode, and single mode. Moreover, current monitoring has an option to average up to 128 samples.

To perform a load current measurement, do the following procedures:

- Write to SET_OUT to turn on the channel.
- Write to CURR_MEAS_ENABLE register to enable the current sense on the channel.
- Write to CURR_AVG[2:0] bits to set the averaging function of measurement.
- Write to CURR_CONT, or CURR_ON_DEMAND, or CURR_SINGLE to select an operating mode. Do not select multiple operating modes at the same time.
- Write to CH_READ_SEL[3:0] to move the measurement result of the channel to ADC_DATA register.
- Read ADC_DATA register with RDY = 1 indicating a conversion is performed.

The resistor at CSSET sets the full-scale range of the current measurement. The LSB of current sense is 5.5mA (typ) and full-scale range is 700mA (typ) with R_{CSSET} = 10kΩ. The equation to calculate the load current is:

I_{OUT} (mA) = 700(mA)/2^7 × ADC_DATA.

V_{DD} Supply Voltage Measurement

The MAX22915 integrates enhanced diagnostics features, which allow to monitor the V_{DD} supply voltage by means of two different operating modes between continuous and on-demand mode.

To perform a voltage sense, do the following procedures:

- Write to VDD_CONT, or VDD_ON_DEMAND, to select an operating mode. Do not select both operating modes at the same time.
- Write 0x8 to CH_READ_SEL[3:0] to move V_{DD} measurement result to ADC_DATA register.
- Read ADC_DATA register with RDY = 1 indicating a conversion is performed.

The LSB of voltage sense is 0.29V (typ) and full-scale range is 36V (typ). When V_{DD} supply voltage falls below its UVLO threshold, the function is disabled. The equation to calculate the V_{DD} supply voltage is:

V_{DD} (V) = 36(V)/2^7 × ADC_DATA.

Chip Temperature Measurement

The MAX22915 has a 7-bit thermometer that allows measurement of the die temperature through SPI interface. The temperature sense range is between 85°C (typ) to 150°C (typ) and the resolution is 0.5°C (typ). The same thermometer is used for thermal warning reporting through the THERM_WARN bit in the GLOBAL_ERR register when the chip temperature exceeds the threshold set by the THERM_WARN_TH register.

The MAX22915 integrates enhanced diagnostics features, which allow to monitor the chip temperature by means of two different operating modes between continuous and on-demand mode.

To perform a temperature sense, do the following procedures:

- Write to TEMP_CONT, or TEMP_ON_DEMAND, to select an operating mode. Do not select both operating modes at the same time.
- Write to TEMP_AVG to set the averaging function of measurement.
- Write 0x9 to CH_READ_SEL[3:0] to move temperature measurement result to ADC_DATA register.
- Read ADC_DATA register with RDY = 1 indicating a conversion is performed.

The LSB of temperature sense is 0.5°C (typ) and full-scale range is between 85°C to 150°C. The equation to calculate the chip temperature is:

T_J (°C) = 85°C + (150°C − 85°C)/2^7 × ADC_DATA.

Regardless of the operating mode, a thermal warning threshold can be enabled with THERM_WARN_EN = 1 and specified with which the measured chip temperature is compared to THERM_WARM_TH register. If the measured chip temperature is higher than the user-defined threshold, the THERM_WARN bit in the GLOBAL_ERR register, the THERM_ERR bit in the INTERRUPT regsiter, and $\overline{\text{FAULT}}$ pin are asserted.

ADC Conversion Timing

The MAX22915 internal ADC conversion time consists of a channel scheduling delay and the ADC conversion time. For the voltage and temperature sense conversion time, see *Figure 16* and for the current sense conversion time, see *Figure 17*. The scheduling delay is the same for all current sense, voltage sense, and temperature sense. The current sense conversion time contains an additional initialization delay set by OWON_FIL_ bit, as shown in *Figure 17*. Moreover, for load current measurement, before the channel is considered fully enabled when the channel on-delay timer expires after the channel is turned on, the scheduler does not move forward to make a conversion. It is required to wait until the conversion is completed before performing an SPI read on ADC_DATA register. The RDY bit is set to 1 to indicate when the conversion is performed and data are ready.

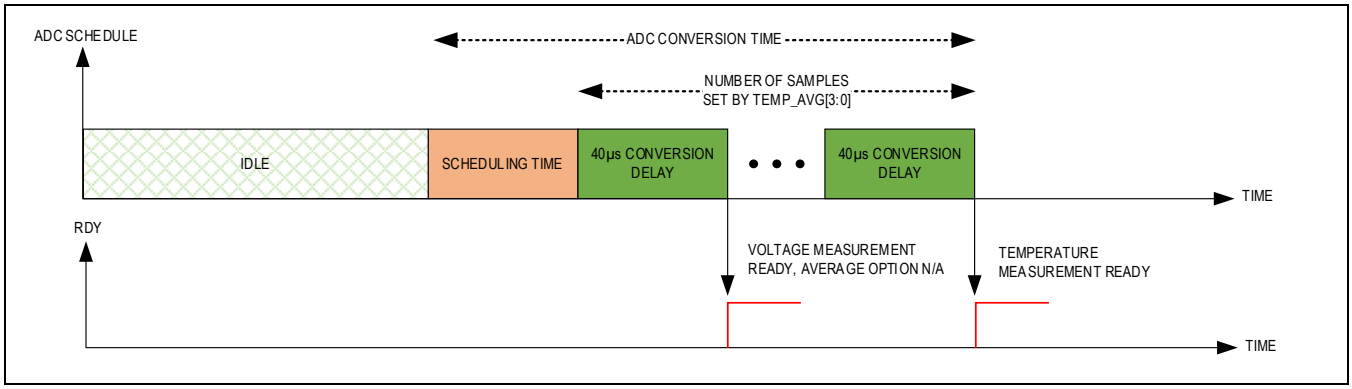


Figure 16. ADC Voltage and Temperature Sense Conversion Time

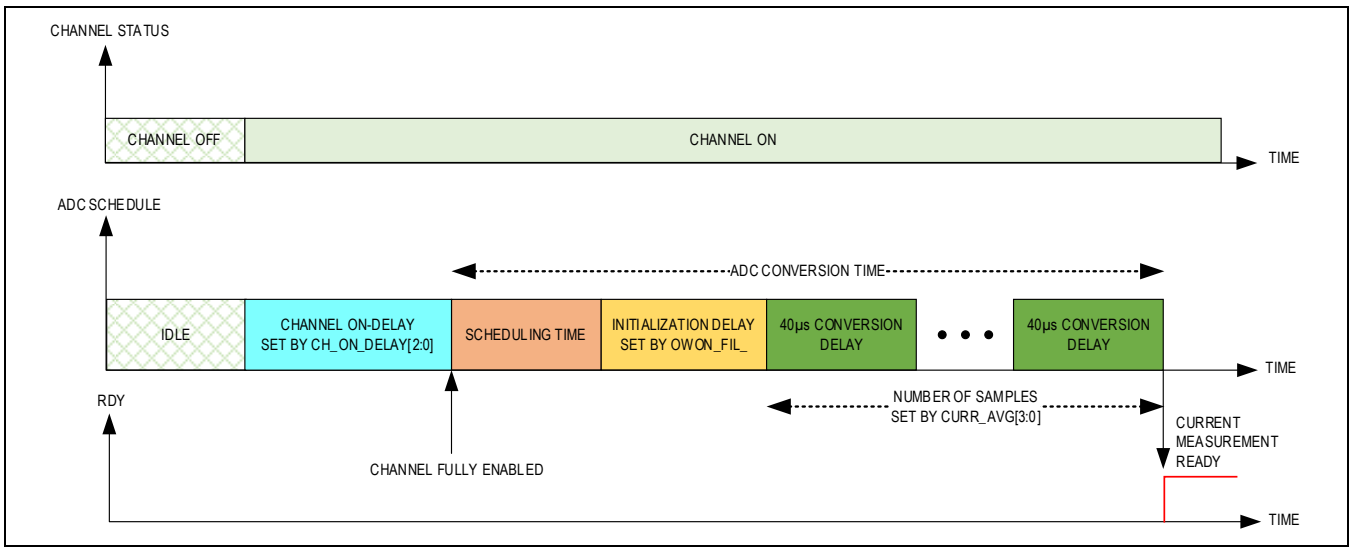


Figure 17. ADC Current Sense Conversion Time

The channel scheduler is equipped with an internal pointer, which sequentially addresses from Channels 0 to Channel 9 and determines whether a measurement is requested and the channel is ready for a conversion. The worst-case scenario is when the channel scheduler is servicing the subsequent channel when user requests a measurement. In this case, the internal pointer has to complete addressing all channels before it returns back and executes the request. The round-trip duration for the internal pointer is 5µs (max), assuming no channel is requesting a measurement.

For example, in continuous-mode current measurement with 64 samples averaged, the total time interval required to wait before reading load current measurement data, after output switch turned-on, is:

0.5ms + 5µs + 3ms + 2.56ms = 6.065ms.

where:

- Channel on-delay timer of 0.5ms (typ) by default.
- Scheduling time of 5µs (max).
- Initialization delay of 3ms (typ) by default.
- Conversion time of 2.56ms (typ) = 64 × 40µs.

Reading Diagnostics Data

ADC_DATA register is used to read measurement results of the channel. To ensure the measurement result is up-to-date, RDY bit in ADC_DATA register is used to indicate a conversion is successful made and data are ready to be read. The RDY bit is cleared after an SPI read. The channel to be read is selected by setting CH_READ_SEL[3:0] bits in the ADC_CONFIG3 register. *Figure 18* shows the way RDY bit and measurement result is moved into ADC_DATA register.

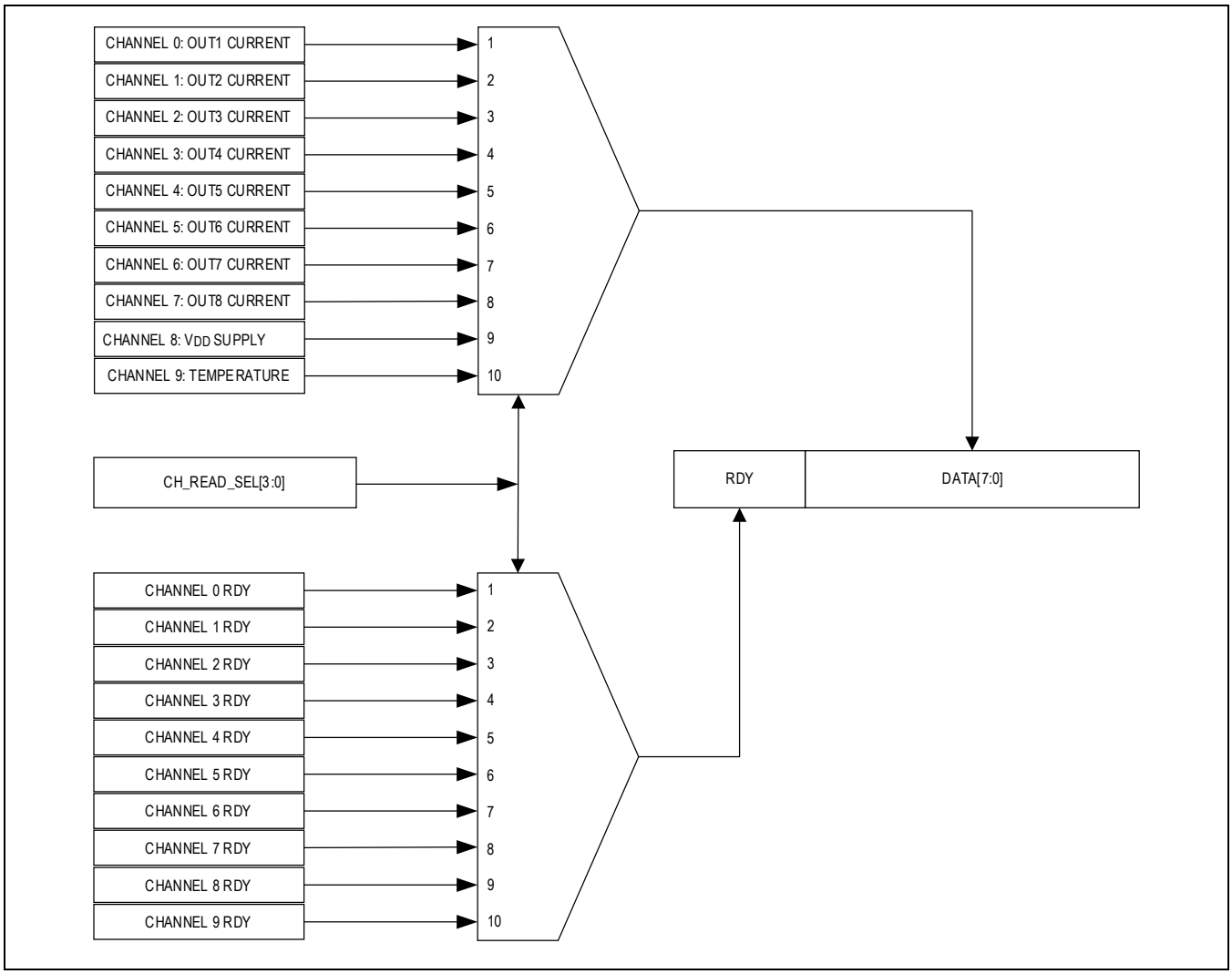


Figure 18. SELECT ADC_DATA

Each channel has its own RDY bit. This bit goes high after a new measurement of the channel is performed. When the CH_READ_SEL[3:0] bits select a channel, both its RDY bit and measurement data are transferred onto ADC_DATA register. The channel RDY bit is cleared after ADC_DATA register is read through SPI. *Figure 19* shows an example using Channel 0.

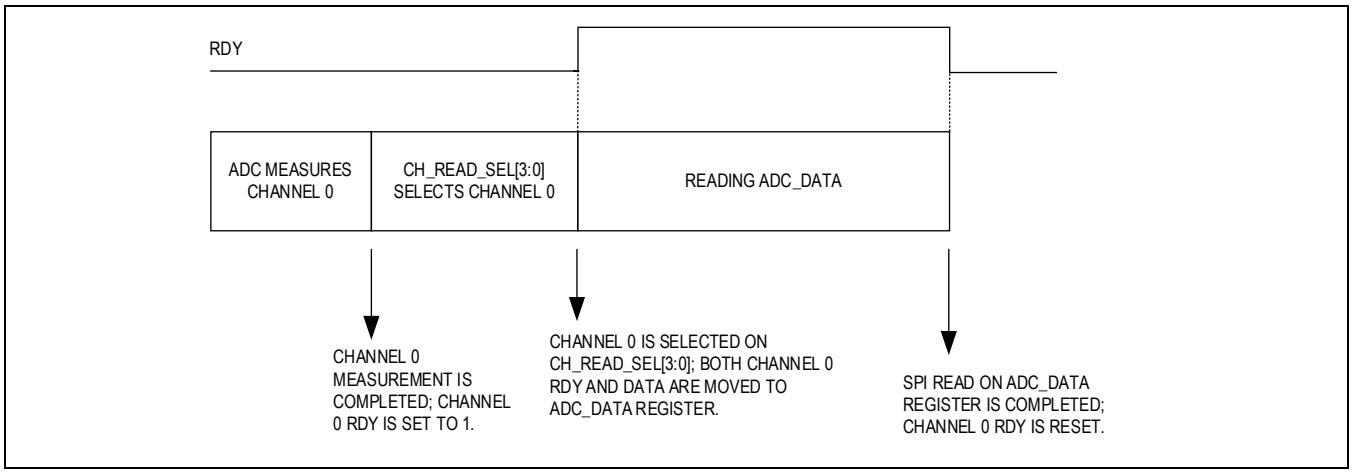


Figure 19. Reading ADC Data

Serial Interface

The MAX22915 communicates with the host controller through a high-speed SPI serial interface. The interface has three logic inputs: clock (SCLK), chip select ($\overline{CS}$), serial data in (SDI), and one data out (SDO). The SDO is three-stated when $\overline{CS}$ is high. The maximum SPI clock rate is 10MHz. The SPI interface logic complies with SPI clock polarity CPOL = 0 and clock phase CPHA = 0.

The MAX22915 SPI can either be operated in addressable SPI mode (Daisy = low) or in daisy-chain mode (DAISY = high). Addressable SPI allows direct communication with up to two MAX22915 on a shared SPI using a single, shared $\overline{CS}$ signal. Addressable SPI offers direct chip access and getting global diagnostics in the same SPI cycle. Addressable SPI supports both single cycle and burst mode read/write operation.

Daisy-chained SPI is enabled by driving DAISY = high. In daisy-chain mode, the first SDO byte provides the channel diagnostics based only on driver overload. Daisy-chain mode provides limited features such as reduced diagnostics and configuration.

Since the power-on default configuration is different in between daisy-chained SPI mode and addressable SPI mode, the MAX22915 does not support dynamic switching between two modes during operation.

Addressable SPI Chip Addressing (A0/WDEN)

In addressable SPI mode, a SPI controller can communicate with up to two MAX22915 devices on a shared, non daisy-chained SPI bus with one single shared $\overline{CS}$ through chip addressing. Each chip on the shared SPI is assigned an individual chip address through the logic input pin A0/WDEN, as shown in *Table 7*.

Table 7. SPI Device Address Selection

A0/WDEN	DEVICE ADDRESS
LOW	0
HIGH	1

The SPI controller addresses a specific chip by sending the appropriate A0 logic in the first bit of the SPI read/write command. The MAX22915 monitors the SPI-address in each SPI read/write cycle and responds when the address matches the programmed address for that IC.

Addressable SPI In-Band Diagnostic Fault Signaling

In every addressable SPI cycle, the MAX22915 returns seven bits in SDO within the first eight SPI clock cycles. These seven bits include ADC conversion ready (RDY), short-to-V_{DD} (SHTVDD_FAULT), open-wire on (OWON_FAULT), open-wire off (OWOFF_FAULT), chip thermal warning (THERM_ERR), output overload (OVL_FAULT) and global faults (GLOBAL_FAULT). The global fault bit, GLOBAL_FAULT, is the logic OR of the COM_ERR, SUPPLY_ERR, and THERM_ERR bits in the INTERRUPT register. These seven diagnostic bits allow for fast identification of the specific channel in fault or global fault condition.

During an SPI write cycle, the second SDO byte returns eight fault bits, one bit associated with each OUT_ channel. These bits are the logic OR of the per-channel diagnostic bits including overload, current limit, short-to-V_{DD}, open-wire on and open-wire off faults.

Single-Cycle Addressable SPI Read

Figure 20 shows the SPI read command in addressable SPI mode (DAISY = low).

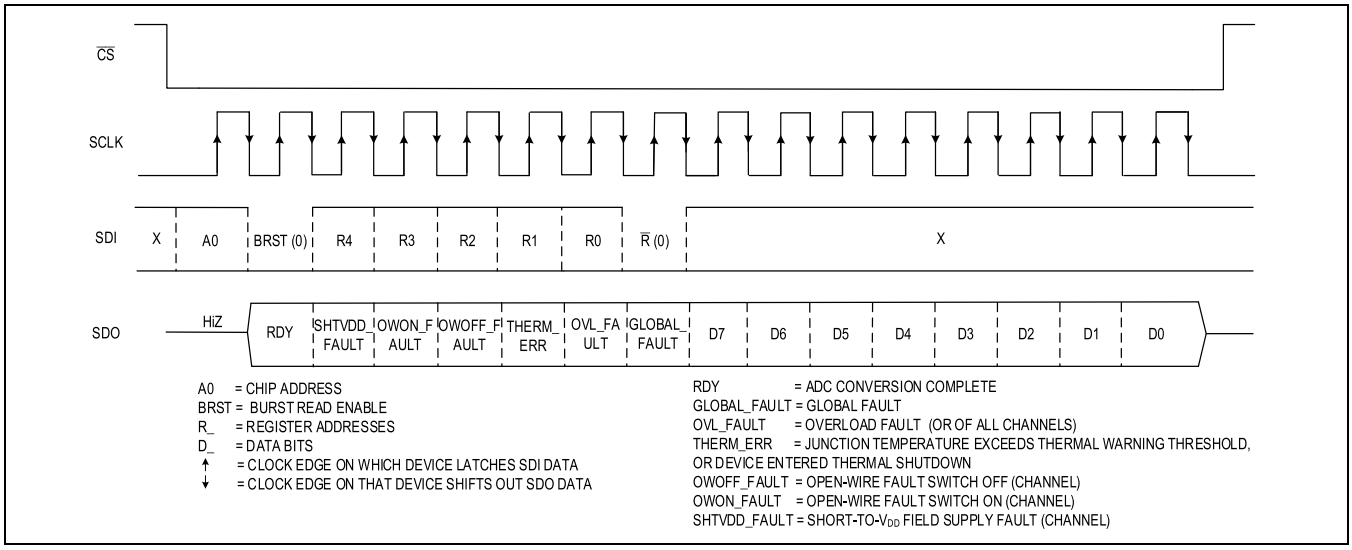


Figure 20. Addressable SPI Single Cycle Read Command

Single-Cycle Addressable SPI Write

Figure 21 shows the SPI write command in SPI addressable mode (DAISY = low).

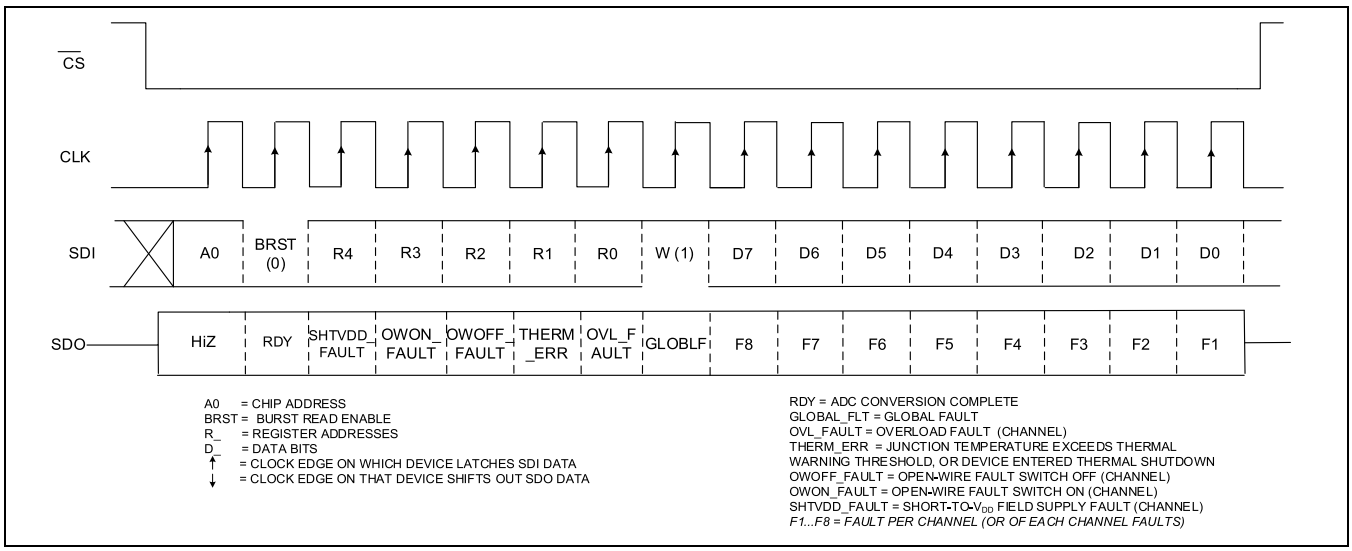


Figure 21. Addressable SPI Single Cycle Write Command

The F_ bits in the second byte of SDO write cycle are the per-channel fault bits. These are the logic OR of the channel fault bits in the OVL_FLT, CL_FLT, OWOFF_FLT, OWON_FLT, and SHTVDD_FLT registers. If only one OUT_ channel has diagnostic fault(s), then an SPI Write command provides full diagnostic information: the channel and all the faults. The only reason to subsequently read the diagnostic registers is to reset the diagnostic bits.

SPI Burst Write

In addressable SPI mode (DAISY = low), burst SPI writing is supported. This allows efficient writing of registers that are commonly accessed: SET_OUT, SET_FLED, and SET_SLED. Burst SPI uses one SPI cycle and one register address

to write to multiple consecutive registers. A burst write is enabled through the BRST bit in the SDI command byte. If the BRST bit is set, the MAX22915 expects an SPI write cycle writing to 2 or 3 registers. The chip-select input ($\overline{CS}$) must be held low during the entire burst write cycle. The SPI clock continues clocking throughout the burst cycle. Only the initial register address (0x00) is specified in the SDI command byte, followed by two or three bytes of data. The burst length is defined by the number of SCLK clocks in the SPI cycle: for a 2-register burst write, 24 clocks are required if CRC is not used, and 32 clocks are required with CRC enabled. For a 3-register burst write, 32 SPI clocks are required without CRC enabled, and 40 clocks with CRC enabled. The burst cycle ends when the $\overline{CS}$ is driven high.

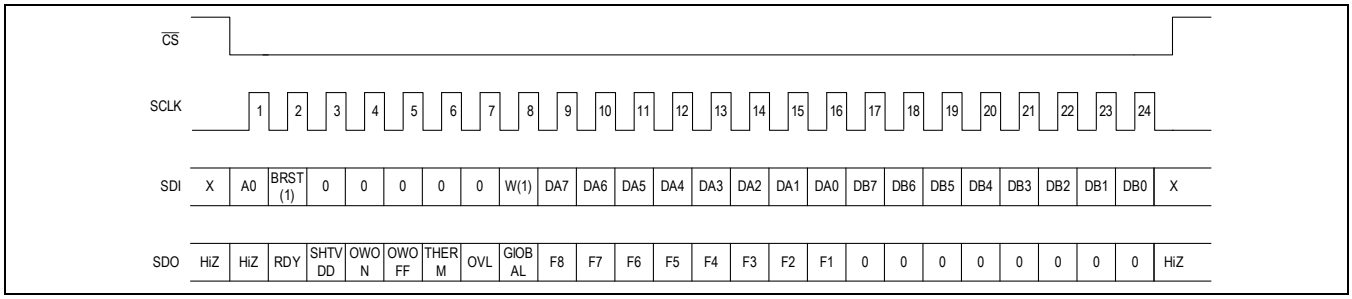


Figure 22. Addressable SPI Two Bytes Burst Write Command

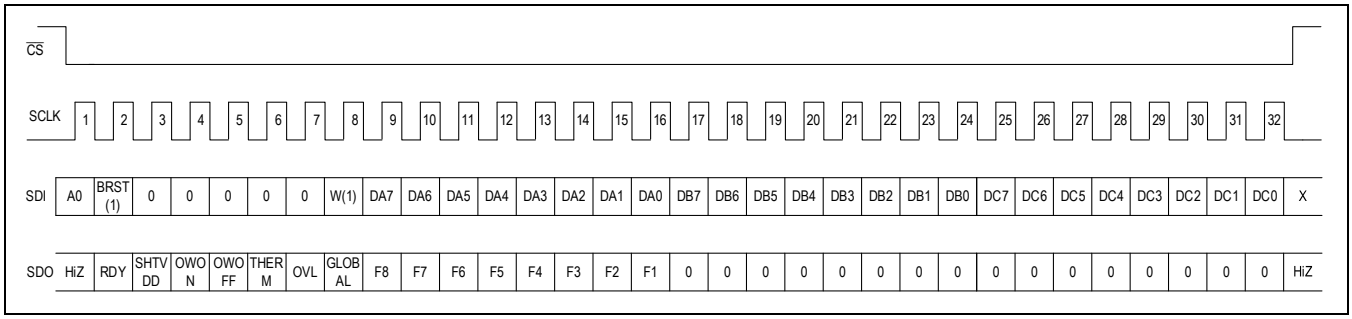


Figure 23. Addressable SPI Three Bytes Burst Write Command

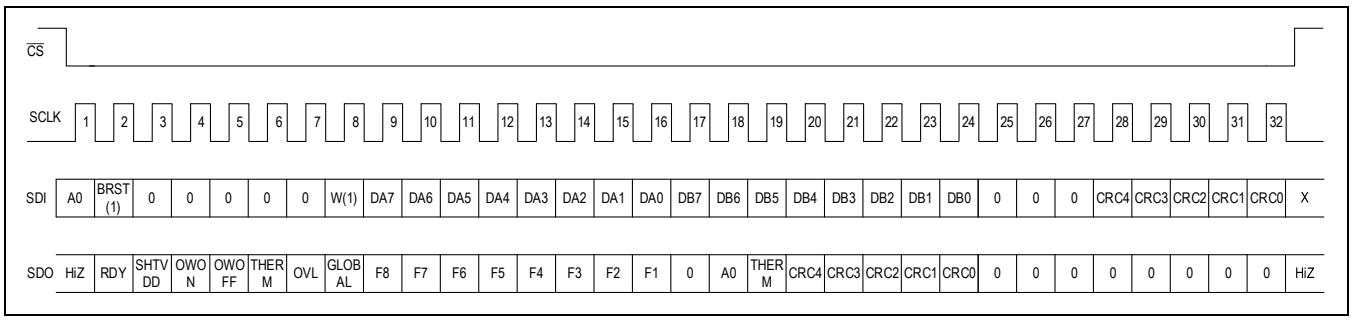


*Figure 24. Addressable SPI Two Bytes Burst Write Command with CRC**

(*)CRC_ bits are calcuated on all the data sent before CRC_ bits.

SPI Burst Read

In addressable SPI mode (DAISY = low), burst SPI reading is supported. Burst SPI reading allows efficient reading of multiple registers in one SPI cycle. The MAX22915 only supports burst reading of the diagnostic registers OVL_FLT, CL_FLT, OWOFF_FLT, OWON_FLT, SHTVDD_FLT, and GLOBAL_ERR.

Set the BRST bit in the SDI command byte to signal a burst SPI cycle. The first register address must be 0x04 (OVL_FLT register) and it must end with the register 0x09 (GLOBAL_ERR register). Total of six consecutive registers can be read within one burst read cycle. If the burst read command ends before the GLOBAL_ERR register, a communication error is signaled on $\overline{SPIERR}$ pin.

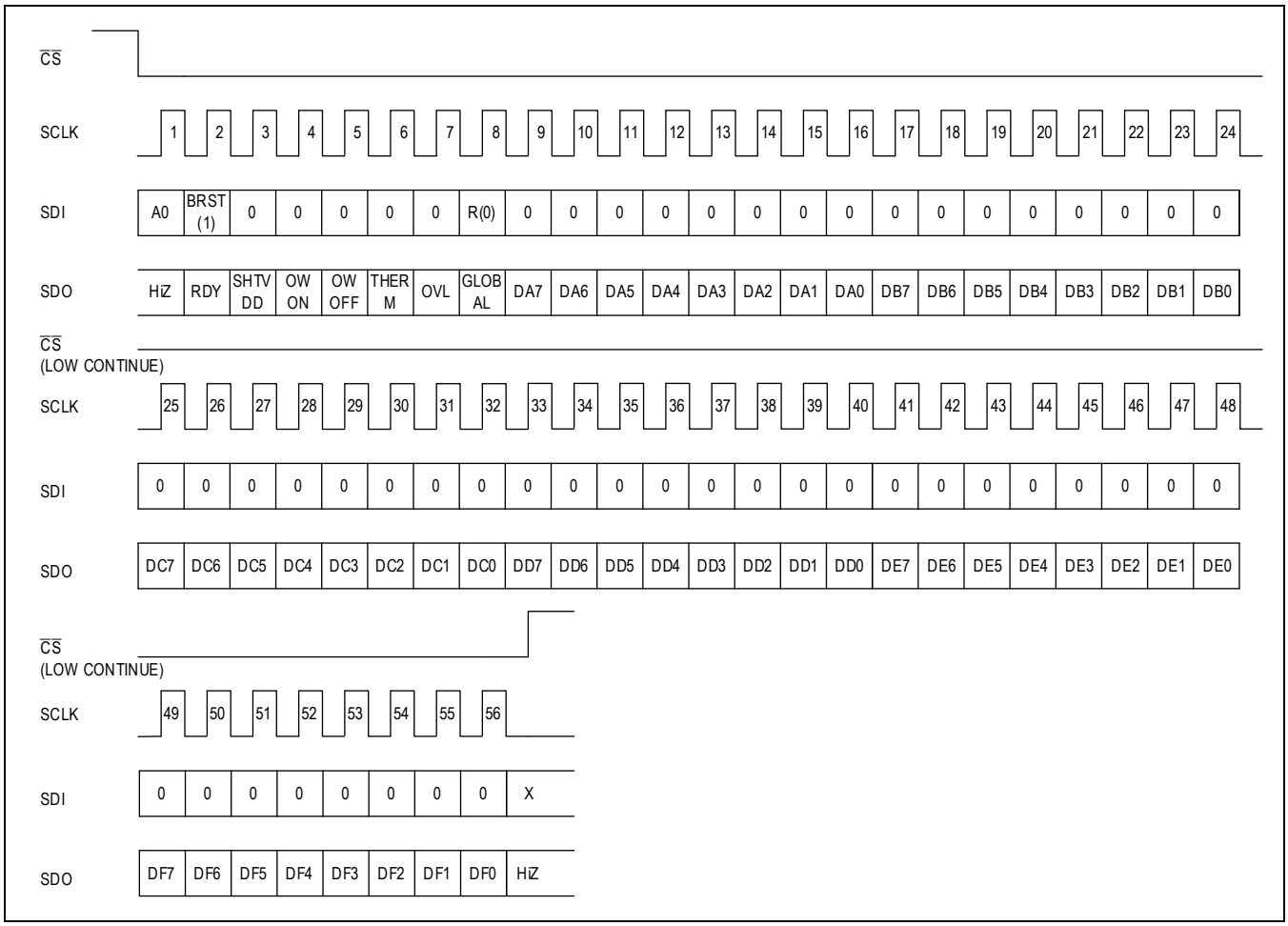


Figure 25. Addressable SPI Burst Read Command

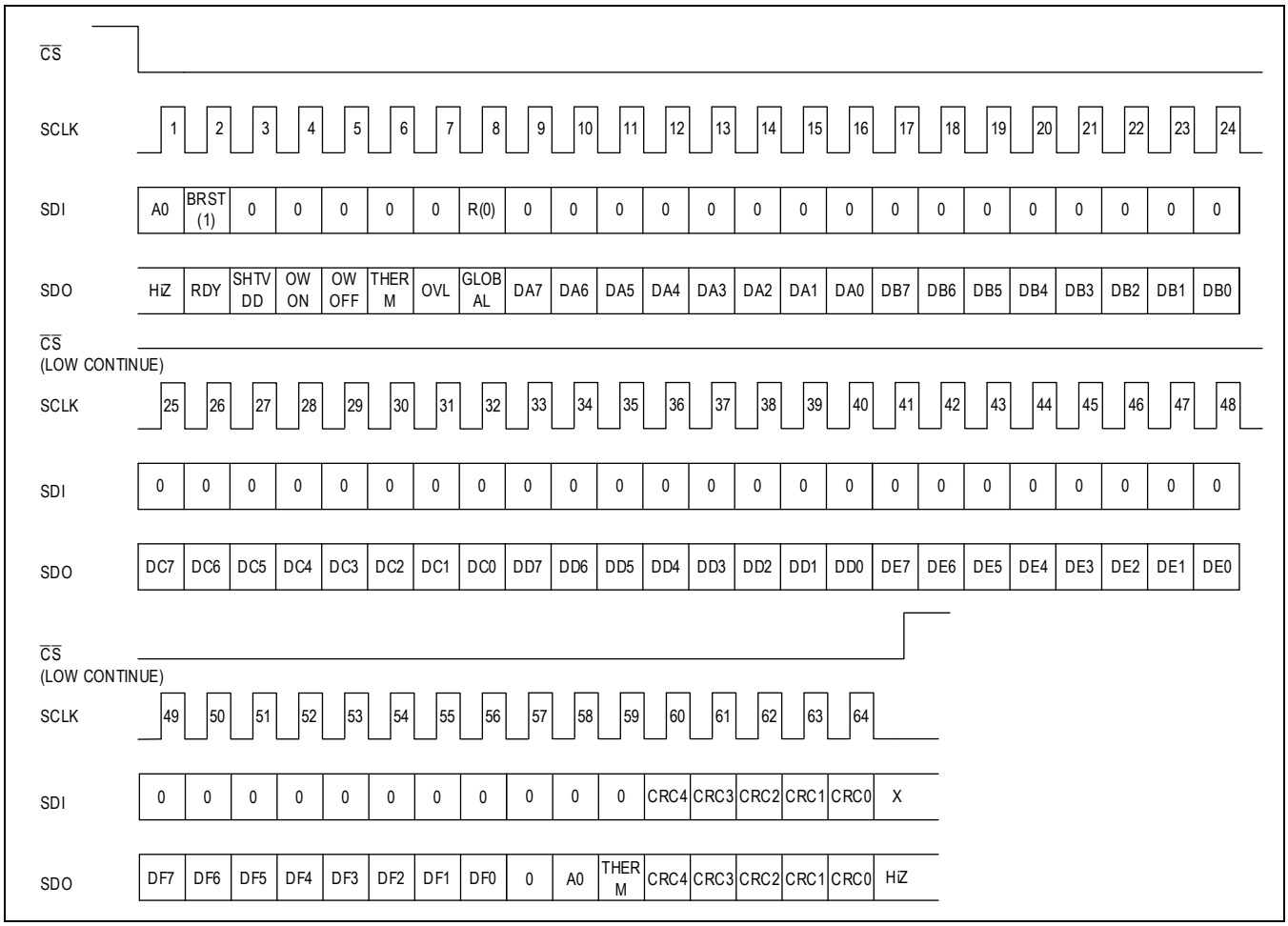


*Figure 26. Addressed SPI Burst Read Command with CRC**

(*) CRC_ bits are calcuated on all the data sent before CRC_ bits.

Daisy-Chained SPI

Daisy-chained SPI mode (DAISY = high) allows communication with multiple MAX22915 devices with one $\overline{CS}$ signal in one SPI cycle. In daisy-chained SPI mode, register access is not possible. Switching between daisy-chained and addressable mode is not supported. Daisy-chained SPI only allows turning the OUT_ switches on/off and reading per-channel overload diagnostics as well as chip thermal shutdown.

Figure 28 shows a daisy-chained SPI command frame without CRC enabled (CRCEN = low), based on only one device in the SPI chain. *Figure 29* shows the command sequence with three MAX22915 devices in the daisy chain.

The ON_ bits turn the OUT_ switches on or off. The F_ bits are per-channel diagnostics and are the same as the OVL_ bits in the OVL_FLT register. The F_ bits are latched and are, therefore, only cleared on the following SPI cycle if the overload fault has disappeared before the following SPI cycle. The F_ bits are not asserted when a lamp load is detected. In chip thermal shutdown, all F_ bits are set to 1.

Daisy-chained SPI mode also supports CRC error detection, which lengthens the SPI cycle to 16 SCLK cycles per each MAX22915.

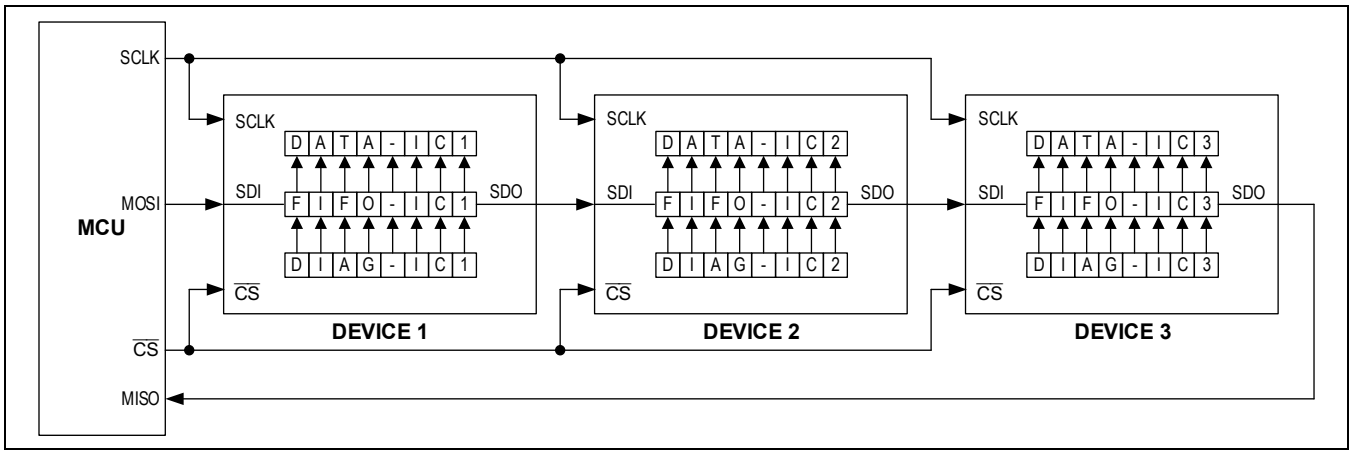


Figure 27. Daisy-Chaining Diagram of Three MAX22915 Devices

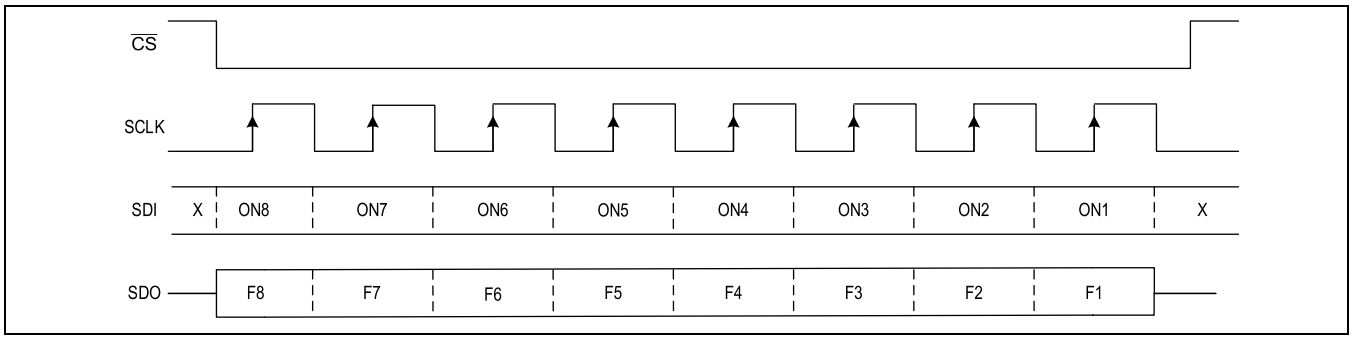


Figure 28. Single Daisy-Chain SPI Command

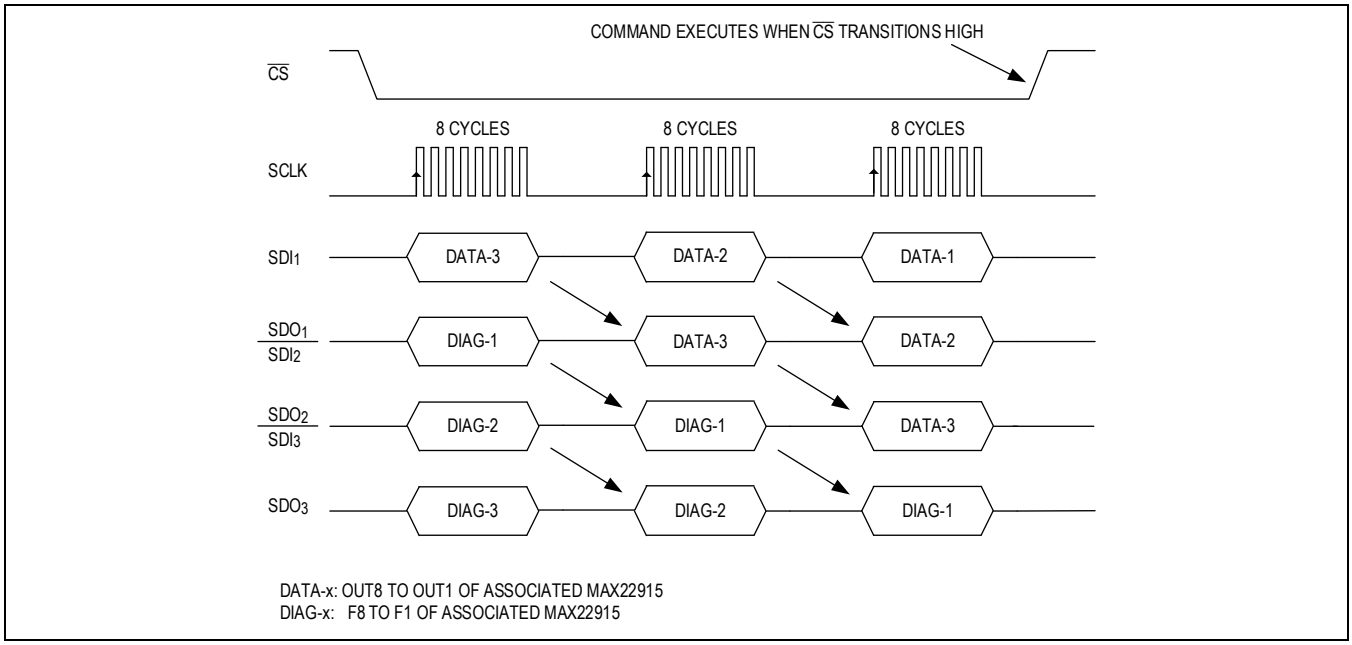


Figure 29. Command Sequence in Daisy-Chain Mode

Checking of Clocks on the Serial Interface

In both addressable and daisy-chained SPI modes, the MAX22915 checks that the number of clock cycles in one SPI cycle (from $\overline{CS}$ falling to rising edge) is a multiple of 8, with 8 clocks minimum for daisy-chained SPI mode and 16 clocks minimum for addressable SPI mode. The expected number of clocks is scaled according to CRCEN pin and burst mode settings. If the number of clock cycles differs from the expected, the SPI command is not executed, and an SPI error is signaled at $\overline{SPIERR}$ pin.

CRC Error Detection on the Serial Interface

CRC error detection of the serial data can be enabled to minimize incorrect operation/misinformation due to data corruption of the SDI/SDO signals. If CRC error detection is enabled, the MAX22915:

- Performs error detection on the SDI data that it receives from the controller.
- And calculates a CRC on the SDO data and appends a check byte to the SDO diagnostics/status data that it sends to the controller.

This ensures that both the data that it receives from the controller (setting/configuration) and the data that it sends to the controller (diagnostics/status) have a low possibility of undetected errors.

Connect the CRCEN pin to high to enable the CRC error detection. A CRC Frame Check Sequence (FCS) is then sent along with each serial transaction. The 5-bit FCS is based on the generator polynomial $X^5 + X^4 + X^2 + 1$ with CRC starting value = 0b11111.

When CRC error detection is enabled, the MAX22915 expects a check byte appended to the SDI data. The check byte has the format, as shown in *Figure 30*.

Table 8. Valid Data Length

DAISY	CRCEN	R/W BIT	BURST BIT	VALID DATA LENGTH (*)
0	0	1	0	16
0	0	1	1	24 or 32
0	1	1	0	24
0	1	1	1	32 or 40
0	0	0	0	16
0	0	0	1	56
0	1	0	0	24
1	0	x	x	8x N (**)
1	1	x	x	16x N (**)

(*) This is the number of SCLK rising edges between $\overline{CS}$ falling and rising edges.

(**) N is an integer number of daisy-chained MAX22915 devices.

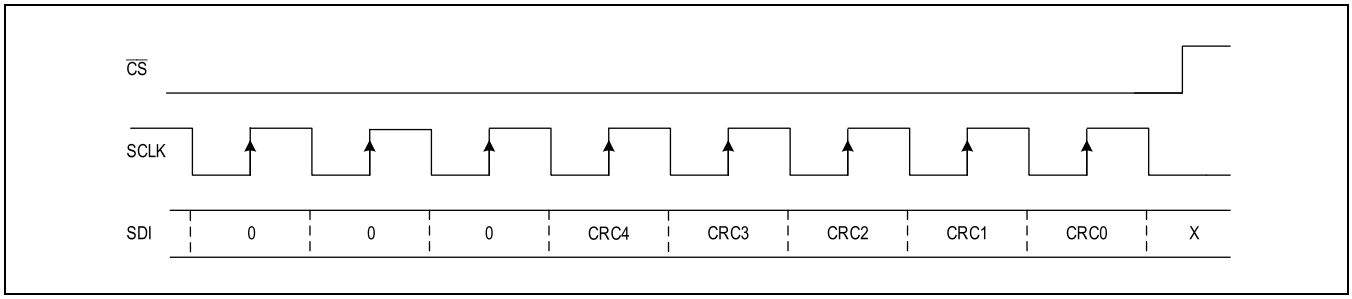


Figure 30. Fcs Byte Expected from the SPI Controller on SDI

The 5 FCS bits (CRC_) are calculated on all the data sent in one SPI command including the three 0 in the MSBs of the check byte. Therefore, the CRC is calculated from 8 + 3 bits up to 56 + 3 bits in case of burst command. CRC0 is the LSB of the FCS.

The MAX22915 verifies the received FCS. If no error is detected, the MAX22915 sets the OUT_ output switches and/or change configuration per the SDI data. If a CRC error is detected, then the MAX22915 does not change the OUT_ outputs or its configuration. Instead, the MAX22915 sets the $\overline{SPIERR}$ logic output low (that is, the open-drain $\overline{SPIERR}$ NMOS output transistor is turned on).

The check byte that the MAX22915 appends to the SDO data has the format, as shown in *Figure 31* and *Figure 32* when the DAISY pin is low.

The A0 is the logic level for the A0/WDEN pin while THERM bit reflects whether a chip thermal shutdown event has occurred. CRC_ are the CRC bits that the MAX22915 calculate on the SDO data, including the 0b0, A0, and THERM bits. This allows the controller to check for errors on the SDO data received from the MAX22915.

The COMERR bit in the FCS byte corresponds to the COM_ERR bit in the INTERRUPT register and is set when either a SPI or SYNCH pin watchdog event has occurred. The VERR bit in the FCS byte corresponds to the SUPPLY_ERR bit in the INTERRUPT register. The THERM bit in the FCS byte is set when the chip thermal shutdown takes place.

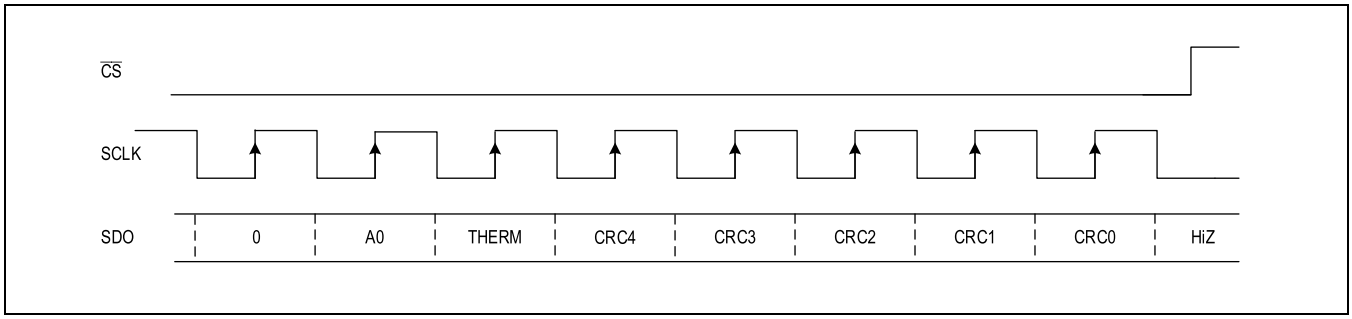


Figure 31. FCS Byte Sent by the MAX22915 to SPI Controller in Addressable SPI Mode

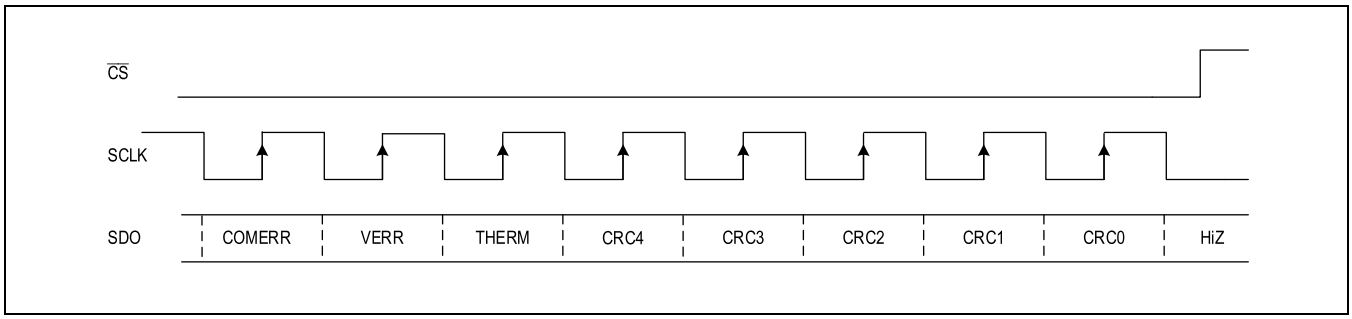


Figure 32. FCS Byte Sent by the MAX22915 to SPI Controller in Daisy-Chained SPI Mode

Register Map

Register Summary: Access Permission: R/W means read and write. R means read only. (MAX22915)

MAX22915 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x00	SET_OUT	[7:0]	ON8	ON7	ON6	ON5	ON4	ON3	ON2	ON1	0x00	R/W
0x01	SET_FLED	[7:0]	FLED8	FLED7	FLED6	FLED5	FLED4	FLED3	FLED2	FLED1	0x00	R/W
0x02	SET_SLED	[7:0]	SLED8	SLED7	SLED6	SLED5	SLED4	SLED3	SLED2	SLED1	0x00	R/W
0x03	INTERRUPT	[7:0]	COM_ERR	SUPPLY_ERR	THERM_ERR	SHTVDD_FAULT	OWON_FAULT	OWOFF_FAULT	CL_FAULT	OVL_FAULT	0x00	R
0x04	OVL_FLT	[7:0]	OVL8	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	0x00	R
0x05	CL_FLT	[7:0]	CL8	CL7	CL6	CL5	CL4	CL3	CL2	CL1	0x00	R
0x06	OWOFF_FLT	[7:0]	OWOFF8	OWOFF7	OWOFF6	OWOFF5	OWOFF4	OWOFF3	OWOFF2	OWOFF1	0x00	R
0x07	OWON_FLT	[7:0]	OWON8	OWON7	OWON6	OWON5	OWON4	OWON3	OWON2	OWON1	0x00	R
0x08	SHTVDD_FLT	[7:0]	SHTVDD8	SHTVDD7	SHTVDD6	SHTVDD5	SHTVDD4	SHTVDD3	SHTVDD2	SHTVDD1	0x00	R
0x09	GLOBAL_ERR	[7:0]	WD_ERR	SYNCH_ERR	THERM_SHTD	VDD_UVLO	THERM_WARN	VM_OK	VA_UVLO	POR	0x01	R
0x0A	OWOFF_ENABLE	[7:0]	OWOFF_EN8	OWOFF_EN7	OWOFF_EN6	OWOFF_EN5	OWOFF_EN4	OWOFF_EN3	OWOFF_EN2	OWOFF_EN1	0x00	R/W
0x0B	OWON_ENABLE	[7:0]	OWON_EN8	OWON_EN7	OWON_EN6	OWON_EN5	OWON_EN4	OWON_EN3	OWON_EN2	OWON_EN1	0x00	R/W
0x0C	SHTVDD_ENABLE	[7:0]	SHTVDD_EN8	SHTVDD_EN7	SHTVDD_EN6	SHTVDD_EN5	SHTVDD_EN4	SHTVDD_EN3	SHTVDD_EN2	SHTVDD_EN1	0x00	R/W
0x0D	CONFIG1	[7:0]	RESERVED	FLATCH_EN	OWOFF_DS		FLED_STRETCH		SLED_SET	FLED_SET	0x43	R/W
0x0E	CONFIG2	[7:0]	SYNC_WD_EN	WD_TIMEOUT		OWOFF_CS		SHTVDD_TH		LED_CL_M	0x00	R/W
0x0F	MASK	[7:0]	COM_ERR_M	SUPPLY_ERR_M	VMOK_M	SHTVDD_M	OWON_M	OWOFF_M	CL_M	OVL_M	0xBE	R/W
0x10	CONFIG3	[7:0]	OW_BLANK_TM					OW_BLANK_TM_EN	FAST_DET_MODE	LAMP_DIS	0x00	R/W
0x11	THERM_WARN_TH	[7:0]	RESERVED	THERM_WARN_TH							0x00	R/W
0x12	CURR_MEAS_ENABLE	[7:0]	CURR_MEAS_EN8	CURR_MEAS_EN7	CURR_MEAS_EN6	CURR_MEAS_EN5	CURR_MEAS_EN4	CURR_MEAS_EN3	CURR_MEAS_EN2	CURR_MEAS_EN1	0x00	R/W
0x13	ADC_CONFIG1	[7:0]	RESERVED	TEMP_AVG			THERM_WARN_EN	TEMP_CONT	TEMP_ON_DEMAND	VDD_CONT	0x00	R/W
0x14	ADC_CONFIG2	[7:0]	RESERVED	CURR_AVG			CURR_SINGLE	CURR_CONT	CURR_ON_DEMAND	VDD_ON_DEMAND	0x00	R/W
0x15	ADC_CONFIG3	[7:0]	CH_ON_DELAY			RESERVED	CH_READ_SEL				0x00	R/W

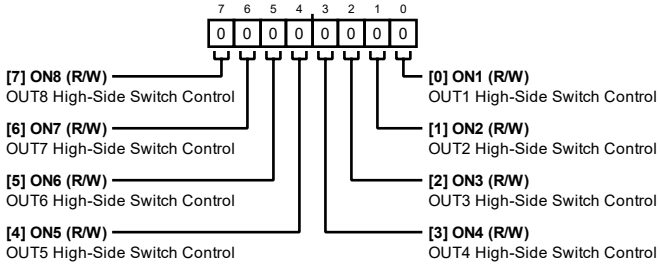
Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x16	*ADC_DATA*	[7:0]	RDY	DATA							0x00	R
0x17	*OWON_FILTER*	[7:0]	OWON_FIL8	OWON_FIL7	OWON_FIL6	OWON_FIL5	OWON_FIL4	OWON_FIL3	OWON_FIL2	OWON_FIL1	0x00	R/W

Register Details: Access Permission: R/W means read and write. R means read only. (MAX22915)

High-Side Switch Control Register

Address: 0x00, Reset: 0x00, Name: SET_OUT

This register turns ON or OFF each high-side switch.



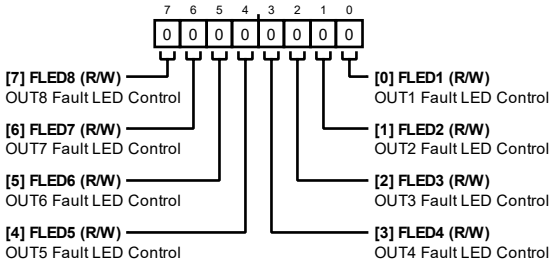
Bit Descriptions for SET_OUT

Bits	Bit Name	Settings	Description	Reset	Access
7	ON8		OUT8 High-Side Switch Control. Set ON8 = 1 to close OUT8 high-side switch. Set ON8 = 0 to open OUT8 high-side switch.	0x0	R/W
6	ON7		OUT7 High-Side Switch Control. Set ON7 = 1 to close OUT7 high-side switch. Set ON7 = 0 to open OUT7 high-side switch.	0x0	R/W
5	ON6		OUT6 High-Side Switch Control. Set ON6 = 1 to close OUT6 high-side switch. Set ON6 = 0 to open OUT6 high-side switch.	0x0	R/W
4	ON5		OUT5 High-Side Switch Control. Set ON5 = 1 to close OUT5 high-side switch. Set ON5 = 0 to open OUT5 high-side switch.	0x0	R/W
3	ON4		OUT4 High-Side Switch Control. Set ON4 = 1 to close OUT4 high-side switch. Set ON4 = 0 to open OUT4 high-side switch.	0x0	R/W
2	ON3		OUT3 High-Side Switch Control. Set ON3 = 1 to close OUT3 high-side switch. Set ON3 = 0 to open OUT3 high-side switch.	0x0	R/W
1	ON2		OUT2 High-Side Switch Control. Set ON2 = 1 to close OUT2 high-side switch. Set ON2 = 0 to open OUT2 high-side switch.	0x0	R/W
0	ON1		OUT1 High-Side Switch Control. Set ON1 = 1 to close OUT1 high-side switch. Set ON1 = 0 to open OUT1 high-side switch.	0x0	R/W

Fault LED Control Register

Address: 0x01, Reset: 0x00, Name: SET_FLED

This register turns ON or OFF each fault LED. The FLED_ bit operates if FLED_SET bit is set in CONFIG1 register. The fault LED is controlled automatically by MAX22915 if FLED_SET bit is not set in CONFIG1 register.



Bit Descriptions for SET_FLED

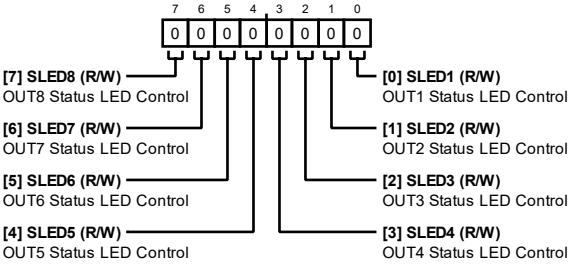
Bits	Bit Name	Settings	Description	Reset	Access
7	FLED8		OUT8 Fault LED Control. Set FLED8 = 1 to turn on OUT8 fault LED. Set FLED8 = 0 to turn off OUT8 fault LED.	0x0	R/W

Bits	Bit Name	Settings	Description	Reset	Access
6	FLED7		OUT7 Fault LED Control. Set FLED7 = 1 to turn on OUT7 fault LED. Set FLED7 = 0 to turn off OUT7 fault LED.	0x0	R/W
5	FLED6		OUT6 Fault LED Control. Set FLED6 = 1 to turn on OUT6 fault LED. Set FLED6 = 0 to turn off OUT6 fault LED.	0x0	R/W
4	FLED5		OUT5 Fault LED Control. Set FLED5 = 1 to turn on OUT5 fault LED. Set FLED5 = 0 to turn off OUT5 fault LED.	0x0	R/W
3	FLED4		OUT4 Fault LED Control. Set FLED4 = 1 to turn on OUT4 fault LED. Set FLED4 = 0 to turn off OUT4 fault LED.	0x0	R/W
2	FLED3		OUT3 Fault LED Control. Set FLED3 = 1 to turn on OUT3 fault LED. Set FLED3 = 0 to turn off OUT3 fault LED.	0x0	R/W
1	FLED2		OUT2 Fault LED Control. Set FLED2 = 1 to turn on OUT2 fault LED. Set FLED2 = 0 to turn off OUT2 fault LED.	0x0	R/W
0	FLED1		OUT1 Fault LED Control. Set FLED1 = 1 to turn on OUT1 fault LED. Set FLED1 = 0 to turn off OUT1 fault LED.	0x0	R/W

Status LED Control Register

Address: 0x02, Reset: 0x00, Name: SET_SLED

This register turns ON or OFF each status LED. The SLED_ bit operates if SLED_SET bit is set in CONFIG1 register. The status LED is controlled automatically by MAX22915 if SLED_SET bit is not set in CONFIG1 register.



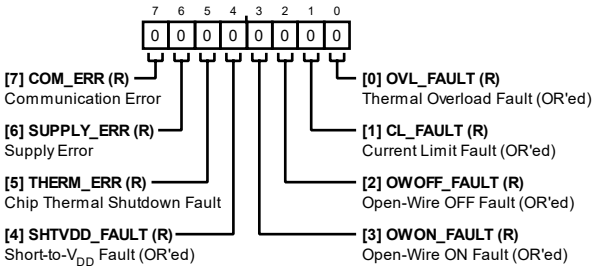
Bit Descriptions for SET_SLED

Bits	Bit Name	Settings	Description	Reset	Access
7	SLED8		OUT8 Status LED Control. Set SLED8 = 1 to turn on OUT8 status LED. Set SLED8 = 0 to turn off OUT8 status LED.	0x0	R/W
6	SLED7		OUT7 Status LED Control. Set SLED7 = 1 to turn on OUT7 status LED. Set SLED7 = 0 to turn off OUT7 status LED.	0x0	R/W
5	SLED6		OUT6 Status LED Control. Set SLED6 = 1 to turn on OUT6 status LED. Set SLED6 = 0 to turn off OUT6 status LED.	0x0	R/W
4	SLED5		OUT5 Status LED Control. Set SLED5 = 1 to turn on OUT5 status LED. Set SLED5 = 0 to turn off OUT5 status LED.	0x0	R/W
3	SLED4		OUT4 Status LED Control. Set SLED4 = 1 to turn on OUT4 status LED. Set SLED4 = 0 to turn off OUT4 status LED.	0x0	R/W
2	SLED3		OUT3 Status LED Control. Set SLED3 = 1 to turn on OUT3 status LED. Set SLED3 = 0 to turn off OUT3 status LED.	0x0	R/W
1	SLED2		OUT2 Status LED Control. Set SLED2 = 1 to turn on OUT2 status LED. Set SLED2 = 0 to turn off OUT2 status LED.	0x0	R/W
0	SLED1		OUT1 Status LED Control. Set SLED1 = 1 to turn on OUT1 status LED. Set SLED1 = 0 to turn off OUT1 status LED.	0x0	R/W

Interrupt Register

Address: 0x03, Reset: 0x00, Name: INTERRUPT

This read-only register contains global diagnostic faults.



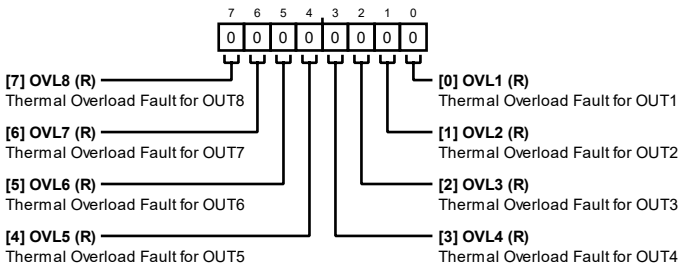
Bit Descriptions for INTERRUPT

Bits	Bit Name	Settings	Description	Reset	Access
7	COM_ERR		Communication Error. COM_ERR bit is set when a watchdog timeout for SPI interface or SYNCH pin is detected. If fault is latched (FLATCH_EN=1), COM_ERR bit is cleared when GLOBAL_ERR register is read and fault conditions have disappeared.	0x0	R
6	SUPPLY_ERR		Supply Error. SUPPLY_ERR bit is logic OR of POR, VDD_UVLO, VA_UVLO and $\overline{VM\_OK}$ bits. If fault is latched (FLATCH_EN = 1), SUPPLY_ERR bit is cleared when GlOBAL_ERR register is read and fault conditions have disappeared.	0x0	R
5	THERM_ERR		Chip Thermal Shutdown Fault. THERM_ERR bit is set after MAX22915 enters chip thermal shutdown or junction temperature rises above thermal warning threshold set by THERM_WARN_TH bits in THERM_WARN_TH register and THERM_WARN_EN bit in ADC_CONFIG1 is set.	0x0	R
4	SHTVDD_FAULT		Short-to-V_{DD} Fault (OR'ed). SHTVDD_FAULT bit is set when a short-to-V_{DD} condition occurs on any OUT_ in OFF state. The per-channel fault can be identified using SHTVDD_ bits in SHTVDD_FLT register.	0x0	R
3	OWON_FAULT		Open-Wire ON Fault (OR'ed). OWOFF_FAULT bit is set when an open-wire condition occurs on any OUT_ in ON state. The per-channel fault can be identified using OWON_ bits in OWON_FLT register.	0x0	R
2	OWOFF_FAULT		Open-Wire OFF Fault (OR'ed). OWOFF_FAULT bit is set when an open-wire condition occurs on any OUT_ in OFF state. The per-channel fault can be identified using OWOFF_ bits in OWOFF_FLT register.	0x0	R
1	CL_FAULT		Current Limit Fault (OR'ed). CL_FAULT bit is set when a current limit condition occurs on any OUT_ in ON state. The per-channel fault can be identified using CL_ bits in CL_FLT register.	0x0	R
0	OVL_FAULT		Thermal Overload Fault (OR'ed). OVL_FAULT bit is set when an overload condition occurs on any OUT_ in ON state. The per-channel fault can be identified using OVL_ bits in OVL_FLT register.	0x0	R

Thermal Overload Fault Register

Address: 0x04, Reset: 0x00, Name: OVL_FLT

This read-only register contains per-channel thermal overload fault. All bits can be configured to be real-time or latched (clear-on-read), depending on FLATCH_EN bit. When bits are configured to be latched (FLATCH_EN = 1), they are reset when this register is read and overload faults have disappeared. If OVL_M bit is set in MASK register, overload fault asserts the OVL_ bit but is not signaled on $\overline{FAULT}$ pin.



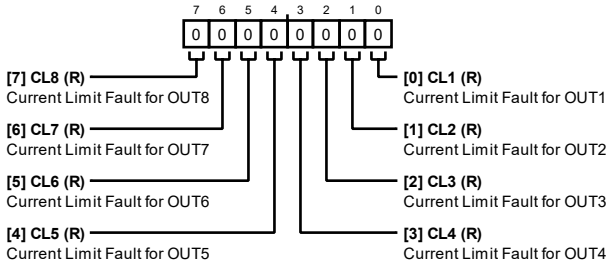
Bit Descriptions for OVL_FLT

Bits	Bit Name	Settings	Description	Reset	Access
7	OVL8		Thermal Overload Fault for OUT8. OVL8 bit is set when a thermal overload is detected on OUT8.	0x0	R
6	OVL7		Thermal Overload Fault for OUT7. OVL7 bit is set when a thermal overload is detected on OUT7.	0x0	R
5	OVL6		Thermal Overload Fault for OUT6. OVL6 bit is set when a thermal overload is detected on OUT6.	0x0	R
4	OVL5		Thermal Overload Fault for OUT5. OVL5 bit is set when a thermal overload is detected on OUT5.	0x0	R
3	OVL4		Thermal Overload Fault for OUT4. OVL4 bit is set when a thermal overload is detected on OUT4.	0x0	R
2	OVL3		Thermal Overload Fault for OUT3. OVL3 bit is set when a thermal overload is detected on OUT3.	0x0	R
1	OVL2		Thermal Overload Fault for OUT2. OVL2 bit is set when a thermal overload is detected on OUT2.	0x0	R
0	OVL1		Thermal Overload Fault for OUT1. OVL1 bit is set when a thermal overload is detected on OUT1.	0x0	R

Current Limit Fault Register

Address: 0x05, Reset: 0x00, Name: CL_FLT

This read-only register contains per-channel current limit fault. All bits can be configured to be real-time or latched (clear-on-read), depending on FLATCH_EN bit. When bits are configured to be latched (FLATCH_EN = 1), they are reset when this register is read and current limit faults have disappeared. If CL_M bit is set in MASK register, current limit fault asserts the CL_ bit but is not signaled on $\overline{FAULT}$ pin.



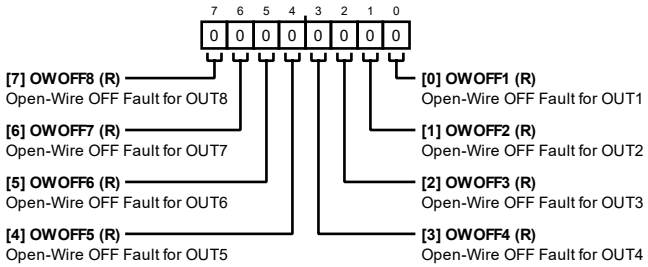
Bit Descriptions for CL_FLT

Bits	Bit Name	Settings	Description	Reset	Access
7	CL8		Current Limit Fault for OUT8. CL8 bit is set when a current limit is detected on OUT8 in ON state.	0x0	R
6	CL7		Current Limit Fault for OUT7. CL7 bit is set when a current limit is detected on OUT7 in ON state.	0x0	R
5	CL6		Current Limit Fault for OUT6. CL6 bit is set when a current limit is detected on OUT6 in ON state.	0x0	R
4	CL5		Current Limit Fault for OUT5. CL5 bit is set when a current limit is detected on OUT5 in ON state.	0x0	R
3	CL4		Current Limit Fault for OUT4. CL4 bit is set when a current limit is detected on OUT4 in ON state.	0x0	R
2	CL3		Current Limit Fault for OUT3. CL3 bit is set when a current limit is detected on OUT3 in ON state.	0x0	R
1	CL2		Current Limit Fault for OUT2. CL2 bit is set when a current limit is detected on OUT2 in ON state.	0x0	R
0	CL1		Current Limit Fault for OUT1. CL1 bit is set when a current limit is detected on OUT1 in ON state.	0x0	R

Open-Wire OFF Fault Register

Address: 0x06, Reset: 0x00, Name: OWOFF_FLT

This read-only register contains per-channel open-wire fault when high-side switch is in OFF state. All bits can be configured to be real-time or latched (clear-on-read), depending on FLATCH_EN bit. When bits are configured to be latched (FLATCH_EN = 1), they are reset when this register is read and open-wire OFF faults have disappeared. If OWOFF_M bit is set in MASK register, open-wire OFF fault asserts the OWOFF_ bit but is not signaled on $\overline{FAULT}$ pin.



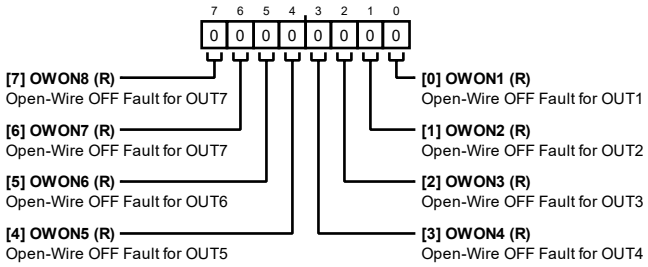
Bit Descriptions for OWOFF_FLT

Bits	Bit Name	Settings	Description	Reset	Access
7	OWOFF8		Open-Wire OFF Fault for OUT8. OWOFF8 bit is set when an open-wire fault is detected on OUT8 in OFF state.	0x0	R
6	OWOFF7		Open-Wire OFF Fault for OUT7. OWOFF7 bit is set when an open-wire fault is detected on OUT7 in OFF state.	0x0	R
5	OWOFF6		Open-Wire OFF Fault for OUT6. OWOFF6 bit is set when an open-wire fault is detected on OUT6 in OFF state.	0x0	R
4	OWOFF5		Open-Wire OFF Fault for OUT5. OWOFF5 bit is set when an open-wire fault is detected on OUT5 in OFF state.	0x0	R
3	OWOFF4		Open-Wire OFF Fault for OUT4. OWOFF4 bit is set when an open-wire fault is detected on OUT4 in OFF state.	0x0	R
2	OWOFF3		Open-Wire OFF Fault for OUT3. OWOFF3 bit is set when an open-wire fault is detected on OUT3 in OFF state.	0x0	R
1	OWOFF2		Open-Wire OFF Fault for OUT2. OWOFF2 bit is set when an open-wire fault is detected on OUT2 in OFF state.	0x0	R
0	OWOFF1		Open-Wire OFF Fault for OUT1. OWOFF1 bit is set when an open-wire fault is detected on OUT1 in OFF state.	0x0	R

Open-Wire ON Fault Register

Address: 0x07, Reset: 0x00, Name: OWON_FLT

This read-only register contains per-channel open-wire fault when high-side switch is in ON state. All bits can be configured to be real-time or latched (clear-on-read), depending on FLATCH_EN bit. When bits are configured to be latched (FLATCH_EN=1), they are reset when this register is read and open-wire ON faults have disappeared. If OWON_M bit is set in MASK register, open-wire ON fault asserts the OWON_ bit but is not signaled on $\overline{FAULT}$ pin.



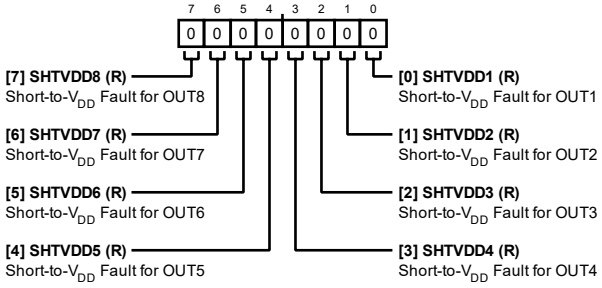
Bit Descriptions for OWON_FLT

Bits	Bit Name	Settings	Description	Reset	Access
7	OWON8		Open-Wire OFF Fault for OUT7. OWON8 bit is set when an open-wire fault is detected on OUT8 in ON state.	0x0	R
6	OWON7		Open-Wire OFF Fault for OUT7. OWON7 bit is set when an open-wire fault is detected on OUT7 in ON state.	0x0	R
5	OWON6		Open-Wire OFF Fault for OUT6. OWON6 bit is set when an open-wire fault is detected on OUT6 in ON state.	0x0	R
4	OWON5		Open-Wire OFF Fault for OUT5. OWON5 bit is set when an open-wire fault is detected on OUT5 in ON state.	0x0	R
3	OWON4		Open-Wire OFF Fault for OUT4. OWON4 bit is set when an open-wire fault is detected on OUT4 in ON state.	0x0	R
2	OWON3		Open-Wire OFF Fault for OUT3. OWON3 bit is set when an open-wire fault is detected on OUT3 in ON state.	0x0	R
1	OWON2		Open-Wire OFF Fault for OUT2. OWON2 bit is set when an open-wire fault is detected on OUT2 in ON state.	0x0	R
0	OWON1		Open-Wire OFF Fault for OUT1. OWON1 bit is set when an open-wire fault is detected on OUT1 in ON state.	0x0	R

Short-to-V_{DD} Fault Register

Address: 0x08, Reset: 0x00, Name: SHTVDD_FLT

This read-only register contains per-channel short-to-V_{DD} fault when high-side switch is in OFF state. All bits can be configured to be real-time or latched (clear-on-read), depending on FLATCH_EN bit. When bits are configured to be latched (FLATCH_EN = 1), they are reset when this register is read and short-to-V_{DD} faults have disappeared. If SHTVDD_M bit is set in MASK register, short-to-V_{DD} fault asserts the SHTVDD_ bit but is not signaled on $\overline{FAULT}$ pin.



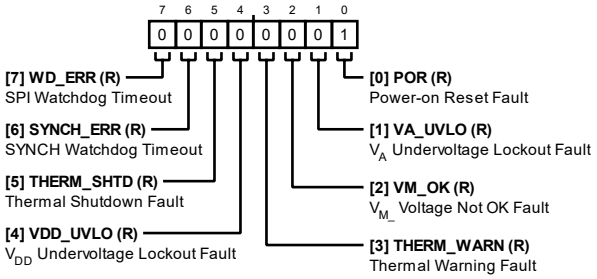
Bit Descriptions for SHTVDD_FLT

Bits	Bit Name	Settings	Description	Reset	Access
7	SHTVDD8		Short-to-V_{DD} Fault for OUT8. SHTVDD8 bit is set when a short-to-V_{DD} fault is detected on OUT8 in OFF state.	0x0	R
6	SHTVDD7		Short-to-V_{DD} Fault for OUT7. SHTVDD7 bit is set when a short-to-V_{DD} fault is detected on OUT7 in OFF state.	0x0	R
5	SHTVDD6		Short-to-V_{DD} Fault for OUT6. SHTVDD6 bit is set when a short-to-V_{DD} fault is detected on OUT6 in OFF state.	0x0	R
4	SHTVDD5		Short-to-V_{DD} Fault for OUT5. SHTVDD5 bit is set when a short-to-V_{DD} fault is detected on OUT5 in OFF state.	0x0	R
3	SHTVDD4		Short-to-V_{DD} Fault for OUT4. SHTVDD4 bit is set when a short-to-V_{DD} fault is detected on OUT4 in OFF state.	0x0	R
2	SHTVDD3		Short-to-V_{DD} Fault for OUT3. SHTVDD3 bit is set when a short-to-V_{DD} fault is detected on OUT3 in OFF state.	0x0	R
1	SHTVDD2		Short-to-V_{DD} Fault for OUT2. SHTVDD2 bit is set when a short-to-V_{DD} fault is detected on OUT2 in OFF state.	0x0	R
0	SHTVDD1		Short-to-V_{DD} Fault for OUT1. SHTVDD1 bit is set when a short-to-V_{DD} fault is detected on OUT1 in OFF state.	0x0	R

Global Error Register

Address: 0x09, Reset: 0x01, Name: GLOBAL_ERR

This read-only registers contains global faults including watchdog timeout, supply voltage errors, thermal warning and thermal shutdown faults.



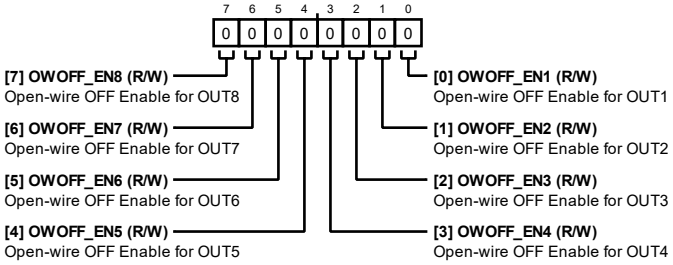
Bit Descriptions for GLOBAL_ERR

Bits	Bit Name	Settings	Description	Reset	Access
7	WD_ERR		SPI Watchdog Timeout. WD_ERR bit is set when a watchdog timeout for SPI is enabled via WD_TIMEOUT bits, and detected. This bit is mapped to COM_ERR bit in INTERRUPT register. If COM_ERR_M bit is set in MASK register, SPI watchdog timeout asserts WD_ERR and COM_ERR bits but is not signaled on $\overline{FAULT}$ pin.	0x0	R
6	SYNCH_ERR		SYNCH Watchdog Timeout. SYNCH_ERR bit is set when a watchdog timeout for SYNCH pin is enabled via SYNCH_WD_EN bit, and detected. This bit is mapped to COM_ERR bit in INTERRUPT register. If COM_ERR_M bit is set in MASK register, SYNCH watchdog timeout asserts SYNCH_ERR and COM_ERR bits but is not signaled on $\overline{FAULT}$ pin.	0x0	R
5	THERM_SHTD		Thermal Shutdown Fault. THERM_SHTD bit is set after MAX22915 enters a chip thermal shutdown. This bit is mapped to THERM_ERR bit in INTERRUPT register. THERM_SHTD bit is cleared by reading GLOBAL_ERR register when junction temperature falls below thermal shutdown threshold.	0x0	R
4	VDD_UVLO		V_{DD} Undervoltage Lockout Fault. VDD_UVLO bit is set when V_{DD} voltage falls below VDD_UVLO threshold. VDD_UVLO bit is cleared by reading GLOBAL_ERR register when V_{DD} voltage rises above VDD_UVLO threshold. If SUPPLY_ERR_M bit is set in MASK register, V_{DD} falling below VDD_UVLO threshold asserts VDD_UVLO and SUPPLY_ERR bits (or VERR bit in SDO signal if daisy-chain mode with CRC operation is selected) but is not signaled on $\overline{FAULT}$ pin.	0x0	R
3	THERM_WARN		Thermal Warning Fault. THERM_WARN bit is set when junction temperature rises above thermal warning threshold set in THERM_WARN_TH register and THERM_WARN_EN bit is set in ADC_CONFIG1 register. THERM_WARN bit is cleared by reading GLOBAL_ERR register when junction temperature falls below thermal warning threshold.	0x0	R
2	VM_OK		$V_{M\_}$ Voltage Not OK Fault. $\overline{VM\_OK}$ bit is set when V_{M2} voltage falls below V_{M2} falling threshold. $\overline{VM\_OK}$ bit is cleared by reading GLOBAL_ERR register when V_{M1} voltage rises above V_{M1} rising threshold. If VMOK_M bit is set in MASK register, V_{M2} falling below V_{M2} falling threshold asserts $\overline{VM\_OK}$ and SUPPLY_ERR bits but is not signaled on $\overline{FAULT}$ pin.	0x0	R
1	VA_UVLO		V_A Undervoltage Lockout Fault. VA_UVLO bit is set when V_A voltage falls below VA_UVLO threshold. VA_UVLO bit is cleared by reading GLOBAL_ERR register when V_A voltage rises above VA_UVLO threshold. If SUPPLY_ERR_M bit is set in MASK register, V_A falling below VA_UVLO threshold asserts VA_UVLO and SUPPLY_ERR bits but is not signaled on $\overline{FAULT}$ pin.	0x0	R
0	POR		Power-on Reset Fault. POR bit is set on initial power-up and after internal voltage to registers falls to a level where register contents are lost. After internal voltage is restored, POR bit is cleared by reading GLOBAL_ERR register.	0x1	R

Open-Wire OFF Fault Enable Register

Address: 0x0A, Reset: 0x00, Name: OWOFF_ENABLE

This register enables per-channel open-wire fault diagnostics when high-side switch is in OFF state. If OWOFF_EN_ = 0, pull-up current source is disabled on corresponding channel.



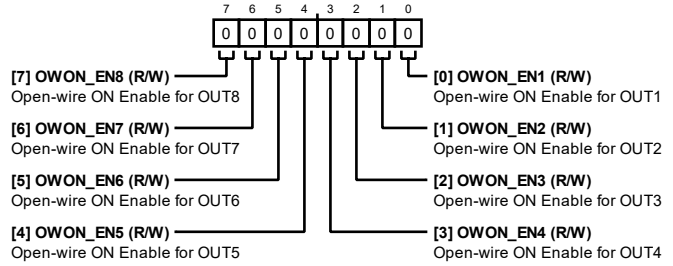
Bit Descriptions for OWOFF_ENABLE

Bits	Bit Name	Settings	Description	Reset	Access
7	OWOFF_EN8		Open-wire OFF Enable for OUT8. Set OWOFF_EN8 = 1 to enable open-wire detection on OUT8 in OFF state. Set OWOFF_EN8 = 0 to disable open-wire detection on OUT8 in OFF state.	0x0	R/W
6	OWOFF_EN7		Open-wire OFF Enable for OUT7. Set OWOFF_EN7 = 1 to enable open-wire detection on OUT7 in OFF state. Set OWOFF_EN7 = 0 to disable open-wire detection on OUT7 in OFF state.	0x0	R/W
5	OWOFF_EN6		Open-wire OFF Enable for OUT6. Set OWOFF_EN6 = 1 to enable open-wire detection on OUT6 in OFF state. Set OWOFF_EN6 = 0 to disable open-wire detection on OUT6 in OFF state.	0x0	R/W
4	OWOFF_EN5		Open-wire OFF Enable for OUT5. Set OWOFF_EN5 = 1 to enable open-wire detection on OUT5 in OFF state. Set OWOFF_EN5 = 0 to disable open-wire detection on OUT5 in OFF state.	0x0	R/W
3	OWOFF_EN4		Open-wire OFF Enable for OUT4. Set OWOFF_EN4 = 1 to enable open-wire detection on OUT4 in OFF state. Set OWOFF_EN4 = 0 to disable open-wire detection on OUT4 in OFF state.	0x0	R/W
2	OWOFF_EN3		Open-wire OFF Enable for OUT3. Set OWOFF_EN3 = 1 to enable open-wire detection on OUT3 in OFF state. Set OWOFF_EN3 = 0 to disable open-wire detection on OUT3 in OFF state.	0x0	R/W
1	OWOFF_EN2		Open-wire OFF Enable for OUT2. Set OWOFF_EN2 = 1 to enable open-wire detection on OUT2 in OFF state. Set OWOFF_EN2 = 0 to disable open-wire detection on OUT2 in OFF state.	0x0	R/W
0	OWOFF_EN1		Open-wire OFF Enable for OUT1. Set OWOFF_EN1 = 1 to enable open-wire detection on OUT1 in OFF state. Set OWOFF_EN1 = 0 to disable open-wire detection on OUT1 in OFF state.	0x0	R/W

Open-Wire ON Fault Enable Register

Address: 0x0B, Reset: 0x00, Name: OWON_ENABLE

This register enables per-channel open-wire fault diagnostics when high-side switch is in ON state.



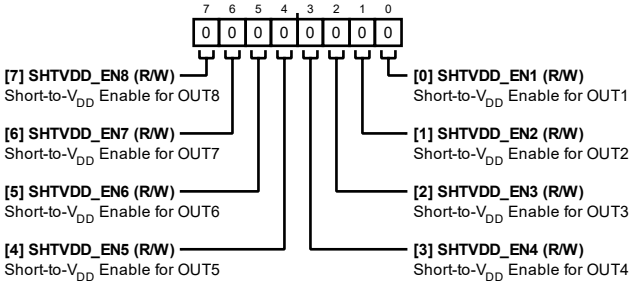
Bit Descriptions for OWON_ENABLE

Bits	Bit Name	Settings	Description	Reset	Access
7	OWON_EN8		Open-wire ON Enable for OUT8. Set OWON_EN8 = 1 to enable open-wire detection on OUT8 in ON state. Set OWON_EN8 = 0 to disable open-wire detection on OUT8 in ON state.	0x0	R/W
6	OWON_EN7		Open-wire ON Enable for OUT7. Set OWON_EN7 = 1 to enable open-wire detection on OUT7 in ON state. Set OWON_EN7 = 0 to disable open-wire detection on OUT7 in ON state.	0x0	R/W
5	OWON_EN6		Open-wire ON Enable for OUT6. Set OWON_EN6 = 1 to enable open-wire detection on OUT6 in ON state. Set OWON_EN6 = 0 to disable open-wire detection on OUT6 in ON state.	0x0	R/W
4	OWON_EN5		Open-wire ON Enable for OUT5. Set OWON_EN5 = 1 to enable open-wire detection on OUT5 in ON state. Set OWON_EN5 = 0 to disable open-wire detection on OUT5 in ON state.	0x0	R/W
3	OWON_EN4		Open-wire ON Enable for OUT4. Set OWON_EN4 = 1 to enable open-wire detection on OUT4 in ON state. Set OWON_EN4 = 0 to disable open-wire detection on OUT4 in ON state.	0x0	R/W
2	OWON_EN3		Open-wire ON Enable for OUT3. Set OWON_EN3 = 1 to enable open-wire detection on OUT3 in ON state. Set OWON_EN3 = 0 to disable open-wire detection on OUT3 in ON state.	0x0	R/W
1	OWON_EN2		Open-wire ON Enable for OUT2. Set OWON_EN2 = 1 to enable open-wire detection on OUT2 in ON state. Set OWON_EN2 = 0 to disable open-wire detection on OUT2 in ON state.	0x0	R/W
0	OWON_EN1		Open-wire ON Enable for OUT1. Set OWON_EN1 = 1 to enable open-wire detection on OUT1 in ON state. Set OWON_EN1 = 0 to disable open-wire detection on OUT1 in ON state.	0x0	R/W

Short-to-V_{DD} Fault Enable Register

Address: 0x0C, Reset: 0x00, Name: SHTVDD_ENABLE

This register enables per-channel short-to-V_{DD} fault diagnostics when high-side switch is in OFF state.



Bit Descriptions for SHTVDD_ENABLE

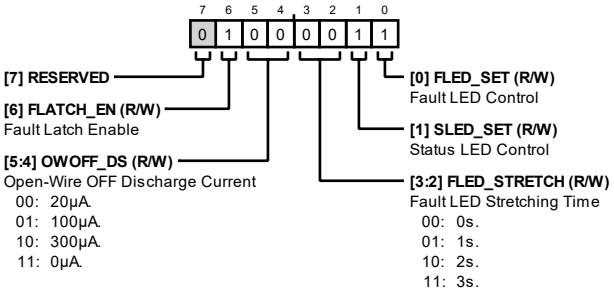
Bits	Bit Name	Settings	Description	Reset	Access
7	SHTVDD_EN8		Short-to-V_{DD} Enable for OUT8. Set SHTVDD_EN8 = 1 to enable short-to-V_{DD} detection on OUT8 in OFF state. Set SHTVDD_EN8 = 0 to disable short-to-V_{DD} detection on OUT8 in OFF state.	0x0	R/W
6	SHTVDD_EN7		Short-to-V_{DD} Enable for OUT7. Set SHTVDD_EN7 = 1 to enable short-to-V_{DD} detection on OUT7 in OFF state. Set SHTVDD_EN7 = 0 to disable short-to-V_{DD} detection on OUT7 in OFF state.	0x0	R/W
5	SHTVDD_EN6		Short-to-V_{DD} Enable for OUT6. Set SHTVDD_EN6 = 1 to enable short-to-V_{DD} detection on OUT6 in OFF state. Set SHTVDD_EN6 = 0 to disable short-to-V_{DD} detection on OUT6 in OFF state.	0x0	R/W

Bits	Bit Name	Settings	Description	Reset	Access
4	SHTVDD_EN5		Short-to-V_{DD} Enable for OUT5. Set SHTVDD_EN5 = 1 to enable short-to-V_{DD} detection on OUT5 in OFF state. Set SHTVDD_EN5 = 0 to disable short-to-V_{DD} detection on OUT5 in OFF state.	0x0	R/W
3	SHTVDD_EN4		Short-to-V_{DD} Enable for OUT4. Set SHTVDD_EN4 = 1 to enable short-to-V_{DD} detection on OUT4 in OFF state. Set SHTVDD_EN4 = 0 to disable short-to-V_{DD} detection on OUT4 in OFF state.	0x0	R/W
2	SHTVDD_EN3		Short-to-V_{DD} Enable for OUT3. Set SHTVDD_EN3 = 1 to enable short-to-V_{DD} detection on OUT3 in OFF state. Set SHTVDD_EN3 = 0 to disable short-to-V_{DD} detection on OUT3 in OFF state.	0x0	R/W
1	SHTVDD_EN2		Short-to-V_{DD} Enable for OUT2. Set SHTVDD_EN2 = 1 to enable short-to-V_{DD} detection on OUT2 in OFF state. Set SHTVDD_EN2 = 0 to disable short-to-V_{DD} detection on OUT2 in OFF state.	0x0	R/W
0	SHTVDD_EN1		Short-to-V_{DD} Enable for OUT1. Set SHTVDD_EN1 = 1 to enable short-to-V_{DD} detection on OUT1 in OFF state. Set SHTVDD_EN1 = 0 to disable short-to-V_{DD} detection on OUT1 in OFF state.	0x0	R/W

Global Configuration Register 1

Address: 0x0D, Reset: 0x43, Name: CONFIG1

This register configures latching behavior of diagnostics faults, open-wire off discharge current source, and control of status and fault LEDs.



Bit Descriptions for CONFIG1

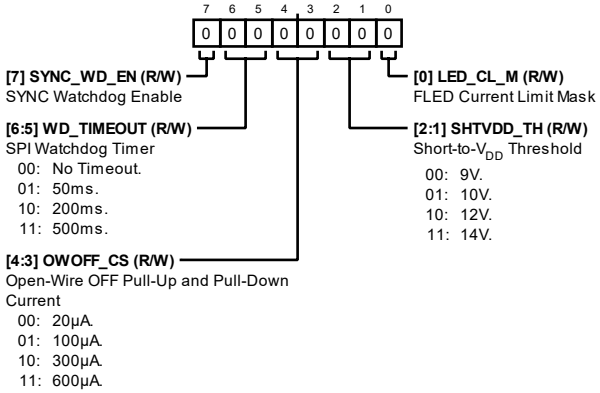
Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
6	FLATCH_EN		Fault Latch Enable. Set FLATCH_EN = 1 to enable latching of diagnostic faults in OVL_FLT, CL_FLT, OWOFF_FLT, OWON_FLT and SHTVDD_FLT registers. Set FLATCH_EN = 0 to disable the latching of these diagnostic faults.	0x1	R/W
[5:4]	OWOFF_DS		Open-Wire OFF Discharge Current. OWOFF_DS bits set pull-down current on OUT_ to discharge voltage when open-wire OFF detection is enabled. If OUT_ voltage falls below 9V (typ), this current source is disabled.	0x0	R/W
		00	20µA.		
		01	100µA.		
		10	300µA.		
		11	0µA.		
[3:2]	FLED_STRETCH		Fault LED Stretching Time. FLED_STRETCH bits set minimum on-time for fault LEDs, if controlled by MAX22915 (FLED_SET = 0), upon per-channel fault occurs. In such case, fault LEDs have a minimum on-time defined by FLED_STRETCH bits and turn off when fault conditions disappear or fault LED stretching time expires, whichever lasts longer. When DAISY pin is high, minimum on-time for fault LEDs is configured to 2s.	0x0	R/W
		00	0s.		
		01	1s.		

Bits	Bit Name	Settings	Description	Reset	Access
		10	2s.		
		11	3s.		
1	SLED_SET		Status LED Control. Set SLED_SET = 1 for status LEDs to be controlled by SET_SLED register. If SLED_SET = 0, status LEDs are controlled autonomously by MAX22915. When DAISY pin is high, status LEDs are always controlled by MAX22915.	0x1	R/W
0	FLED_SET		Fault LED Control. Set FLED_SET = 1 for fault LEDs to be controlled by SET_FLED register. If FLED_SET = 0, fault LEDs are controlled by internal per-channel fault diagnostics including SHTVDD_, OWON_, OWOFF_, CL_, and OVL_ (if enabled). When DAISY pin is high, fault LEDs are always controlled by overload diagnostics OVL_.	0x1	R/W

Global Configuration Register 2

Address: 0x0E, Reset: 0x00, Name: CONFIG2

This register configures watchdog timer, open-wire off pull-up and pull-down current source, short-to-V_{DD} threshold and current limit fault reflected on fault LEDs.



Bit Descriptions for CONFIG2

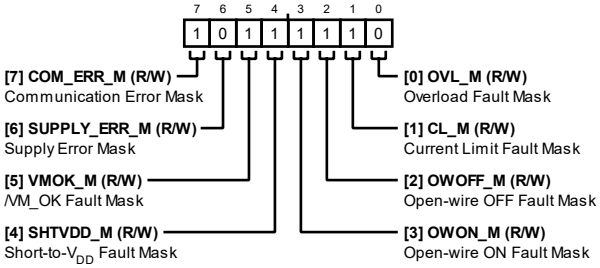
Bits	Bit Name	Settings	Description	Reset	Access
7	SYNC_WD_EN		SYNC Watchdog Enable. SYNC_WD_EN bit enables the 50ms watchdog timer for SYNCH. When DAISY pin is high, SPI and SYNCH watchdog timeouts are both configured to 1.2s. When WD_TIMEOUT is set to 11b and SYNC_WD_EN is set to 1, timeout fault instantly takes place.	0x0	R/W
[6:5]	WD_TIMEOUT		SPI Watchdog Timer. WD_TIMEOUT bits enable and set watchdog timer for SPI. When DAISY pin is high, SPI and SYNCH watchdog timeouts are both configured to 1.2s.	0x0	R/W
		00	No Timeout.		
		01	50ms.		
		10	200ms.		
		11	500ms.		
[4:3]	OWOFF_CS		Open-Wire OFF Pull-Up and Pull-Down Current. OWOFF_CS bits set pull-up and pull-down current on OUT_ when open-wire OFF detection is enabled.	0x0	R/W
		00	20µA.		
		01	100µA.		
		10	300µA.		
		11	600µA.		
[2:1]	SHTVDD_TH		Short-to-V_{DD} Threshold. SHTVDD_TH bits set threshold voltage for short-to-V_{DD} detection on OUT_ in OFF state.	0x0	R/W
		00	9V.		

Bits	Bit Name	Settings	Description	Reset	Access
		01	10V.		
		10	12V.		
		11	14V.		
0	LED_CL_M		FLED Current Limit Mask. Set LED_CL_M = 1 to mask fault LEDs signaling current limit fault on OUT_, when fault LEDs are controlled internally (FLED_SET = 0).	0x0	R/W

Fault Mask Register

Address: 0x0F, Reset: 0xBE, Name: MASK

This register masks or unmasks diagnostic faults from signaling on $\overline{FAULT}$ pin. Disabling mask (setting bits = 0) enables fault sources to assert $\overline{FAULT}$ pin. Enabling mask (setting bit = 1) disables fault sources to assert $\overline{FAULT}$ pin. Mask bits do not prevent diagnostic faults from setting INTERRUPT register as well as corresponding fault registers.



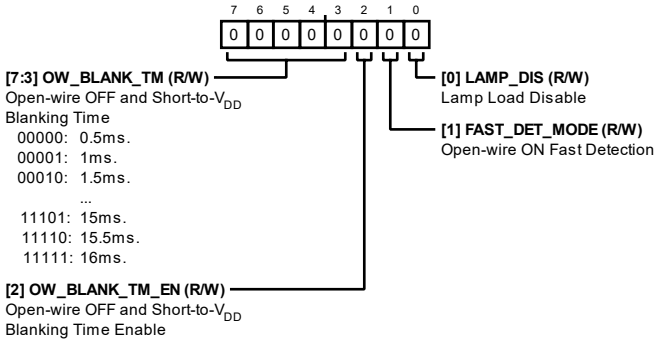
Bit Descriptions for MASK

Bits	Bit Name	Settings	Description	Reset	Access
7	COM_ERR_M		Communication Error Mask. Set COM_ERR_M = 1 to disable SPI or SYNCH watchdog timeouts being signaled on $\overline{FAULT}$ pin. Independent of COM_ERR_M bit setting, SPI or SYNCH watchdog timeouts always assert COM_ERR in INTERRUPT register.	0x1	R/W
6	SUPPLY_ERR_M		Supply Error Mask. Set SUPPLY_ERR_M = 1 to disable supply errors and warnings being signaled on $\overline{FAULT}$ pin. Independent of SUPPLY_ERR_M bit setting, supply errors and warnings always assert SUPPLY_ERR in INTERRUPT register.	0x0	R/W
5	VMOK_M		/VM_OK Fault Mask. Set VMOK_M = 1 to disable $V_{M\_}$ not OK condition being signaled in SUPPLY_ERR in INTERRUPT register.	0x1	R/W
4	SHTVDD_M		Short-to-V_{DD} Fault Mask. Set SHTVDD_M = 1 to disable per-channel short-to-V_{DD} conditions being signaled on $\overline{FAULT}$ pin. Independent of SHTVDD_M bit setting, short-to-V_{DD} conditions always assert SHTVDD_ bits.	0x1	R/W
3	OWON_M		Open-wire ON Fault Mask. Set OWON_M = 1 to disable per-channel open-wire on conditions being signaled on $\overline{FAULT}$ pin. Independent of OWON_M bit setting, open-wire on conditions always assert OWON_ bits.	0x1	R/W
2	OWOFF_M		Open-wire OFF Fault Mask. Set OWOFF_M = 1 to disable per-channel open-wire off conditions being signaled on $\overline{FAULT}$ pin. Independent of OWOFF_M bit setting, open-wire off conditions always assert OWOFF_ bits.	0x1	R/W
1	CL_M		Current Limit Fault Mask. Set CL_M = 1 to disable per-channel current limit conditions being signaled on $\overline{FAULT}$ pin. Independent of CL_M bit setting, current limit conditions always assert CL_ bits.	0x1	R/W
0	OVL_M		Overload Fault Mask. Set OVL_M = 1 to disable per-channel overload conditions being signaled on $\overline{FAULT}$ pin. Independent of OVL_M bit setting, overload conditions always assert OVL_ bits.	0x0	R/W

Global Configuration Register 3

Address: 0x10, Reset: 0x00, Name: CONFIG3

This register configures open-wire OFF and short-to-V_{DD} blanking time, open-wire ON detection time, and lamp load turn-on feature.



Bit Descriptions for CONFIG3

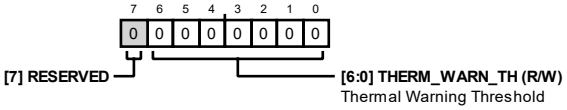
Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	OW_BLANK_TM		Open-wire OFF and Short-to-V_{DD} Blanking Time. OW_BLANK_TM bits set blanking time on open-wire and short-to-V_{DD} diagnostics on OUT_ in OFF state.	0x0	R/W
		00000	0.5ms.		
		00001	1ms.		
		00010	1.5ms.		
		00011	2ms.		
		00100	2.5ms.		
		00101	3ms.		
		00110	3.5ms.		
		00111	4ms.		
		01000	4.5ms.		
		01001	5ms.		
		01010	5.5ms.		
		01011	6ms.		
		01100	6.5ms.		
		01101	7ms.		
		01110	7.5ms.		
		01111	8ms.		
		10000	8.5ms.		
		10001	9ms.		
		10010	9.5ms.		
		10011	10ms.		
		10100	10.5ms.		
		10101	11ms.		
		10110	11.5ms.		
		10111	12ms.		
		11000	12.5ms.		
		11001	13ms.		
		11010	13.5ms.		
		11011	14ms.		
		11100	14.5ms.		
		11101	15ms.		
		11110	15.5ms.		
		11111	16ms.		

Bits	Bit Name	Settings	Description	Reset	Access
2	OW_BLANK_TM_EN		Open-wire OFF and Short-to-V_{DD} Blanking Time Enable. Set OW_BLANK_TM_EN = 1 to enable blanking time, set by OW_BLANK_TM bits, on open-wire and short-to-V_{DD} diagnostics on OUT_ in OFF state.	0x0	R/W
1	FAST_DET_MODE		Open-wire ON Fast Detection. Reduce the open-wire detection time on OUT_ in ON state. Set FAST_DET_MODE = 1 for open-wire ON detection when OUT_ are toggling at more than 75Hz.	0x0	R/W
0	LAMP_DIS		Lamp Load Disable. Set LAMP_DIS = 0 to enable the lamp load turn-on feature, allowing for 1.5A inrush current and 200ms (typ) of overload and current limit fault blanking time.	0x0	R/W

Thermal Warning Threshold Register

Address: 0x11, Reset: 0x00, Name: THERM_WARN_TH

This register configures threshold temperature for thermal warning fault.



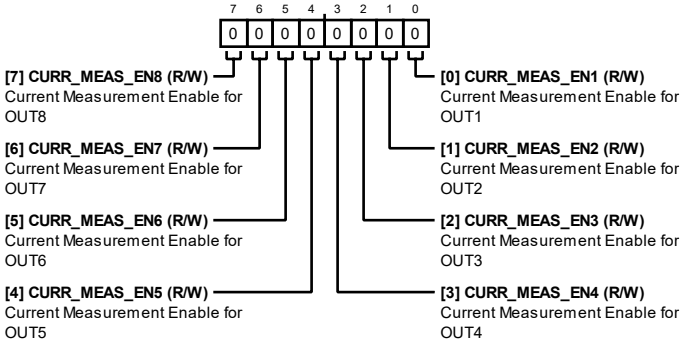
Bit Descriptions for THERM_WARN_TH

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
[6:0]	THERM_WARN_TH		Thermal Warning Threshold. THERM_WARN_TH bits set the threshold temperature = 85°C + dec (THERM_WARN_TH[6:0]) × 0.5°C for thermal warning fault.	0x0	R/W

Current Measurement Enable Register

Address: 0x12, Reset: 0x00, Name: CURR_MEAS_ENABLE

This register enables current measurement for selected switch in ON state.



Bit Descriptions for CURR_MEAS_ENABLE

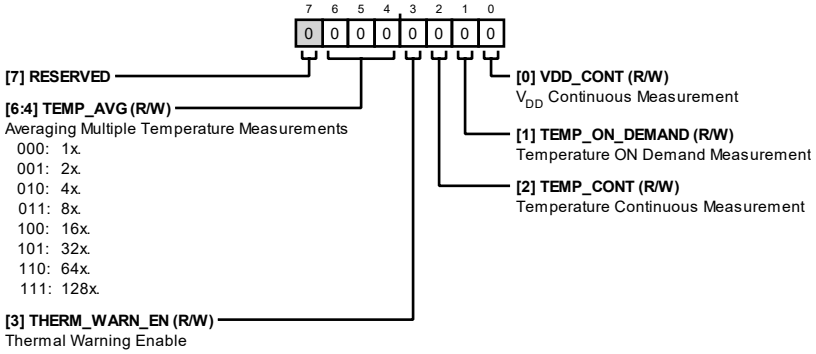
Bits	Bit Name	Settings	Description	Reset	Access
7	CURR_MEAS_EN8		Current Measurement Enable for OUT8. Set CURR_MEAS_EN8 = 1 to enable current measurement on OUT8 in ON state. Set CURR_MEAS_EN8 = 0 to disable.	0x0	R/W
6	CURR_MEAS_EN7		Current Measurement Enable for OUT7. Set CURR_MEAS_EN7 = 1 to enable current measurement on OUT7 in ON state. Set CURR_MEAS_EN7 = 0 to disable.	0x0	R/W

Bits	Bit Name	Settings	Description	Reset	Access
5	CURR_MEAS_EN6		Current Measurement Enable for OUT6. Set CURR_MEAS_EN6 = 1 to enable current measurement on OUT6 in ON state. Set CURR_MEAS_EN6 = 0 to disable.	0x0	R/W
4	CURR_MEAS_EN5		Current Measurement Enable for OUT5. Set CURR_MEAS_EN5 = 1 to enable current measurement on OUT5 in ON state. Set CURR_MEAS_EN5 = 0 to disable.	0x0	R/W
3	CURR_MEAS_EN4		Current Measurement Enable for OUT4. Set CURR_MEAS_EN4 = 1 to enable current measurement on OUT4 in ON state. Set CURR_MEAS_EN4 = 0 to disable.	0x0	R/W
2	CURR_MEAS_EN3		Current Measurement Enable for OUT3. Set CURR_MEAS_EN3 = 1 to enable current measurement on OUT3 in ON state. Set CURR_MEAS_EN3 = 0 to disable.	0x0	R/W
1	CURR_MEAS_EN2		Current Measurement Enable for OUT2. Set CURR_MEAS_EN2 = 1 to enable current measurement on OUT2 in ON state. Set CURR_MEAS_EN2 = 0 to disable.	0x0	R/W
0	CURR_MEAS_EN1		Current Measurement Enable for OUT1. Set CURR_MEAS_EN1 = 1 to enable current measurement on OUT1 in ON state. Set CURR_MEAS_EN1 = 0 to disable.	0x0	R/W

ADC Configuration Register 1

Address: 0x13, Reset: 0x00, Name: ADC_CONFIG1

This register configures temperature and V_{DD} measurement modes, averaging multiple temperature measurements, and enabling or disabling thermal warning.



Bit Descriptions for ADC_CONFIG1

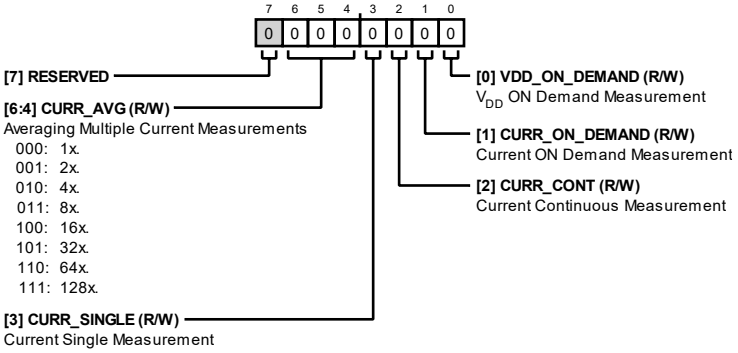
Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
[6:4]	TEMP_AVG		Averaging Multiple Temperature Measurements. TEMP_AVG bits set the number of temperature measurements with which to calculate average temperature.	0x0	R/W
		000	1x.		
		001	2x.		
		010	4x.		
		011	8x.		
		100	16x.		
		101	32x.		
		110	64x.		
		111	128x.		
3	THERM_WARN_EN		Thermal Warning Enable. Set THERM_WARN_EN = 1 to enable thermal warning detection on junction temperature. If temperature rises above threshold set by THERM_WARN_TH bits, THERM_WARN is asserted in GLOBAL_ERR register.	0x0	R/W

Bits	Bit Name	Settings	Description	Reset	Access
2	TEMP_CONT		Temperature Continuous Measurement. Set TEMP_CONT = 1 to enable temperature continuous measurement. Do not set both TEMP_CONT and TEMP_ON_DEMAND to 1 simultaneously.	0x0	R/W
1	TEMP_ON_DEMAND		Temperature ON Demand Measurement. Set TEMP_ON_DEMAND = 1 to enable temperature ON demand measurement. This bit is automatically cleared when temperature measurement is completed. Do not set both TEMP_ON_DEMAND and TEMP_CONT to 1 simultaneously.	0x0	R/W
0	VDD_CONT		V_{DD} Continuous Measurement. Set VDD_CONT = 1 to enable V_{DD} continuous measurement. Do not set both VDD_CONT and VDD_ON_DEMAND to 1 simultaneously.	0x0	R/W

ADC Configuration Register 2

Address: 0x14, Reset: 0x00, Name: ADC_CONFIG2

This register configures current and V_{DD} measurement modes, and averaging multiple current and V_{DD} measurements.



Bit Descriptions for ADC_CONFIG2

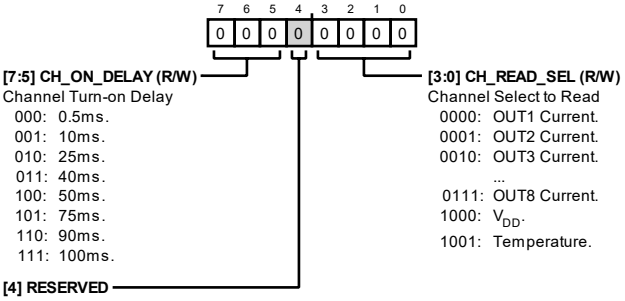
Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
[6:4]	CURR_AVG		Averaging Multiple Current Measurements. CURR_AVG bits set the number of current measurements on selected OUT_ in ON state, with which to calculate average current.	0x0	R/W
		000	1x.		
		001	2x.		
		010	4x.		
		011	8x.		
		100	16x.		
		101	32x.		
		110	64x.		
		111	128x.		
3	CURR_SINGLE		Current Single Measurement. Set CURR_SINGLE = 1 to enable a single current measurement on selected OUT_ in ON state. This bit is automatically cleared when current measurement is completed.	0x0	R/W
2	CURR_CONT		Current Continuous Measurement. Set CURR_CONT = 1 to enable current continuous measurement on selected OUT_ in ON state.	0x0	R/W
1	CURR_ON_DEMAND		Current ON Demand Measurement. Set CURR_ON_DEMAND = 1 to enable current ON demand measurement on selected OUT_ in ON state. This bit is automatically cleared when current measurement is completed.	0x0	R/W

Bits	Bit Name	Settings	Description	Reset	Access
0	VDD_ON_DEMAND		V_{DD} ON Demand Measurement. Set VDD_ON_DEMAND = 1 to enable V_{DD} ON demand measurement. This bit is automatically cleared when supply voltage measurement is completed. Do not set both VDD_ON_DEMAND and VDD_CONT to 1 simultaneously.	0x0	R/W

ADC Configuration Register 3

Address: 0x15, Reset: 0x00, Name: ADC_CONFIG3

This register configures channel turn-on delay before ADC measurement takes place and data (per-channel output current, V_{DD} voltage, or chip temperature) to be read through ADC Data register.



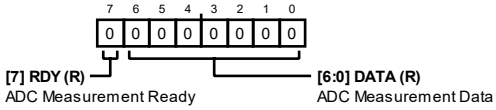
Bit Descriptions for ADC_CONFIG3

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	CH_ON_DELAY		Channel Turn-on Delay. CH_ON_DELAY bits set time interval to be waited, starting from OUT_ initial turning-on, to be considered fully enabled and available for an ADC measurement.	0x0	R/W
		000	0.5ms.		
		001	10ms.		
		010	25ms.		
		011	40ms.		
		100	50ms.		
		101	75ms.		
		110	90ms.		
		111	100ms.		
4	RESERVED		Reserved.	0x0	R
[3:0]	CH_READ_SEL		Channel Select to Read. CH_READ_SEL bits select channel to be read in ADC_DATA register.	0x0	R/W
		0000	OUT1 Current.		
		0001	OUT2 Current.		
		0010	OUT3 Current.		
		0011	OUT4 Current.		
		0100	OUT5 Current.		
		0101	OUT6 Current.		
		0110	OUT7 Current.		
		0111	OUT8 Current.		
		1000	V_{DD}.		
		1001	Temperature.		

ADC Data Register

Address: 0x16, Reset: 0x00, Name: ADC_DATA

This read-only register contains ADC measurement data.



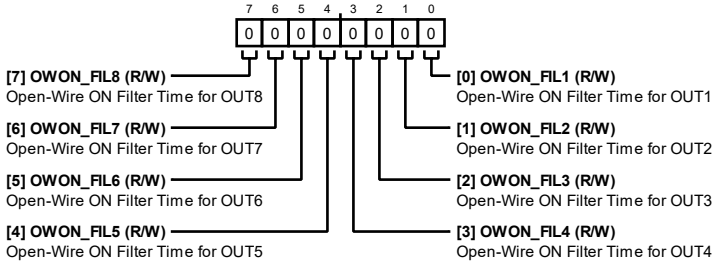
Bit Descriptions for ADC_DATA

Bits	Bit Name	Settings	Description	Reset	Access
7	RDY		ADC Measurement Ready. RDY is set when a new measurement data on selected channel is available and stored in DATA bits. RDY is cleared when ADC_DATA register is read.	0x0	R
[6:0]	DATA		ADC Measurement Data.	0x0	R

Open-Wire ON Filter Time Register

Address: 0x17, Reset: 0x00, Name: OWON_FILTER

This register configures open-wire ON filter time for each OUT_.



Bit Descriptions for OWON_FILTER

Bits	Bit Name	Settings	Description	Reset	Access
7	OWON_FIL8		Open-Wire ON Filter Time for OUT8. Set OWON_FIL8 = 0 to set 3ms as filter time on current sense and open-wire detection on OUT8 in ON state, for enhanced EMC immunity. Set OWON_FIL8 = 1 to set 1ms as filter time.	0x0	R/W
6	OWON_FIL7		Open-Wire ON Filter Time for OUT7. Set OWON_FIL7 = 0 to set 3ms as filter time on current sense and open-wire detection on OUT7 in ON state, for enhanced EMC immunity. Set OWON_FIL7 = 1 to set 1ms as filter time.	0x0	R/W
5	OWON_FIL6		Open-Wire ON Filter Time for OUT6. Set OWON_FIL6 = 0 to set 3ms as filter time on current sense and open-wire detection on OUT6 in ON state, for enhanced EMC immunity. Set OWON_FIL6 = 1 to set 1ms as filter time.	0x0	R/W
4	OWON_FIL5		Open-Wire ON Filter Time for OUT5. Set OWON_FIL5 = 0 to set 3ms as filter time on current sense and open-wire detection on OUT5 in ON state, for enhanced EMC immunity. Set OWON_FIL5 = 1 to set 1ms as filter time.	0x0	R/W
3	OWON_FIL4		Open-Wire ON Filter Time for OUT4. Set OWON_FIL4 = 0 to set 3ms as filter time on current sense and open-wire detection on OUT4 in ON state, for enhanced EMC immunity. Set OWON_FIL4 = 1 to set 1ms as filter time.	0x0	R/W
2	OWON_FIL3		Open-Wire ON Filter Time for OUT3. Set OWON_FIL3 = 0 to set 3ms as filter time on current sense and open-wire detection on OUT3 in ON state, for enhanced EMC immunity. Set OWON_FIL3 = 1 to set 1ms as filter time.	0x0	R/W
1	OWON_FIL2		Open-Wire ON Filter Time for OUT2. Set OWON_FIL2 = 0 to set 3ms as filter time on current sense and open-wire detection on OUT2 in ON state, for enhanced EMC immunity. Set OWON_FIL2 = 1 to set 1ms as filter time.	0x0	R/W
0	OWON_FIL1		Open-Wire ON Filter Time for OUT1. Set OWON_FIL1 = 0 to set 3ms as filter time on current sense and open-wire detection on OUT1 in ON state, for enhanced EMC immunity. Set OWON_FIL1 = 1 to set 1ms as filter time.	0x0	R/W

Applications Information

Inductive Load Turn-off Energy Clamping

During turn-off of inductive loads, the free-wheel energy is clamped by the internal V_{CL} clamps. This energy must be limited to 150mJ (max) at T_J = +125°C at $I_{OUT\_}$ = −600mA (max) per-channel, all channels switching simultaneously.

Surge Protection

The MAX22915 is tolerant of ±1kV (1.2/50µs) surges coupled through a 42Ω/0.5µF CDN onto the OUT_ pins relative to GND when the V_{DD} pin is protected by a single TVS. Suitable TVS are SMCJ36A, SMC30J40A, or SM30T39AY. Ensure that the peak clamping voltage of the V_{DD} TVS is below 65V (max).

Loss of V_{DD} or Loss of GND Protection

The MAX22915 is protected in case of a loss of V_{DD} or a loss of GND fault. If the V_{DD} or GND connection is lost, all high-side switches are disabled, and all OUT_ pins go to a high-impedance state, regardless of the state of ON_ in the SET_OUT register. The current from the OUT_ pin in the event of a loss of GND is ±10µA (max), which is well below the level defined by IEC 61131-2, ensuring a logic state 0. Very low OUT_ leakage current allows MAX22915 to be compatible with the Type 1, Type 2, and Type 3 digital input (DI) devices.

RF Conducted Immunity

The MAX22915 provides enhanced IEC 61000-4-6 conducted RF immunity for open-wire on and off, as well as short-to-V_{DD} detections when switch is open, closed, or toggling at up to 131Hz. To ensure that the OUT_ pins do not produce wrong logic conditions while being off, connect a 10nF capacitor at each OUT_ to GND. Set open-wire on filter time to 3ms for robust open-wire on detection.

To enable fast diagnostics while the switch is toggling at up to 131Hz, enable the open-wire on fast detection by setting the FAST_DET_MODE bit in CONFIG3 register. Enable extra pull-down current to discharge OUT_ voltage, for open-wire off and short-to-V_{DD} detection, by setting OWOFFD_ bits in CONFIG1 register. For more details, see the *Open-Wire Detection with Switch Toggling* section.

Reverse Currents into OUT_

If currents flow into the OUT_ pins, the device heats up due to internal currents that flow through the device from V_{DD} to GND. The internal currents are proportional to the reverse current into OUT_. The maximum allowed reverse OUT_ current depends on V_{DD}, the ambient temperature and the thermal resistance. At 25°C ambient temperature, the reverse current into one OUT_ must be limited to 1A (max) at V_{DD} = 36V and 1.5A (max) at V_{DD} = 24V. Driving higher currents into OUT_ can thermally destroy the device.

Typical Application Circuit

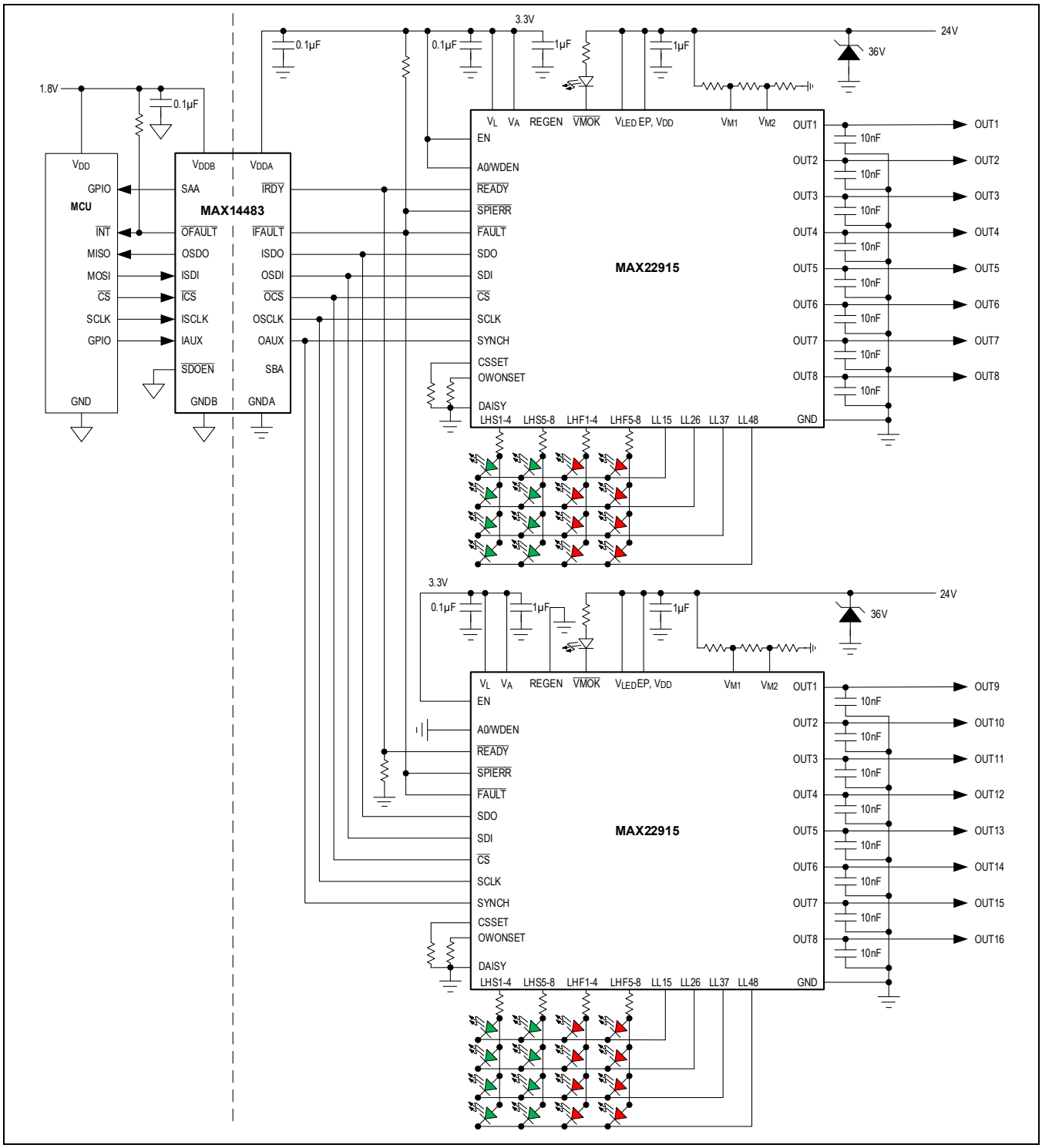


Figure 33. 16-Channel Isolated DO Application Using a 6-Channel Digital Isolator

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING	LEAD PITCH (mm)
MAX22915AFG+	−40°C to +125°C	50-FC2QFN	MAX22915AFG	0.4
MAX22915AFG+T	−40°C to +125°C	50-FC2QFN	MAX22915AFG	0.4

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/26	Initial release	—

NOTES