![ANALOG DEVICES]

IO-Link Device Transceiver with Integrated Cortex-M0 and Analog Front End

MAX22522

Product Highlights

- Enable Smallest Sensors and Actuators
  - Cortex-M0 with 64kB RAM and SWD
  - IO-Link State Machine
  - High Performance IO-Link Transceiver
  - High Speed Comparator
  - 6-bit DAC
  - Three 256-Tap 10kΩ Variable Resistors
  - 60kΩ 64-Tap Variable Resistor
  - 13-Bit ADC
  - 10 GPIOs Configurable as I^2C, SPI, SWD
  - Integrated Temperature Sensor
  - Integrated Oscillator with PLL for IO-Link
- Highly Flexible and Configurable
  - 7V to 36V Supply
  - COM1, COM2, and COM3 Data Rates
  - Programmable 50mA to 250mA C/Q Current Limit Threshold
  - 5V and 1.8V Linear Regulators with Controller
  - WLP Package (4.42mm × 2.64mm)
- Robust 24V IO Interface
  - Reverse Polarity and Overvoltage Protection
  - Internal Monitoring Enables Enhanced Diagnostics
  - Fast Demag of 200mA/1.2H Inductive Loads
  - ±4kV IEC 61000-4-2 Contact ESD Protection
  - ±6kV IEC 61000-4-2 Air-Gap ESD Protection
  - ±1.2kV/500Ω Surge Protection on C/Q and V_{24}

General Description

The MAX22522 is a mixed signal IO-Link device transceiver incorporating an ARM® Cortex-M0 with an IO-Link data link state machine. This state machine autonomously manages all time critical tasks for IO-Link communication at the COM1, COM2, and COM3 data rates. The integrated state machine manages all IO-Link M-sequence types, as well as full ISDU transfers.

The MAX22522 integrates programmable analog components including a 13-bit ADC, an integrated comparator, and four programmable resistors, which allow the MAX22522 to be used for signal generation and conditioning for end-of-line calibration for sensors and actuators.

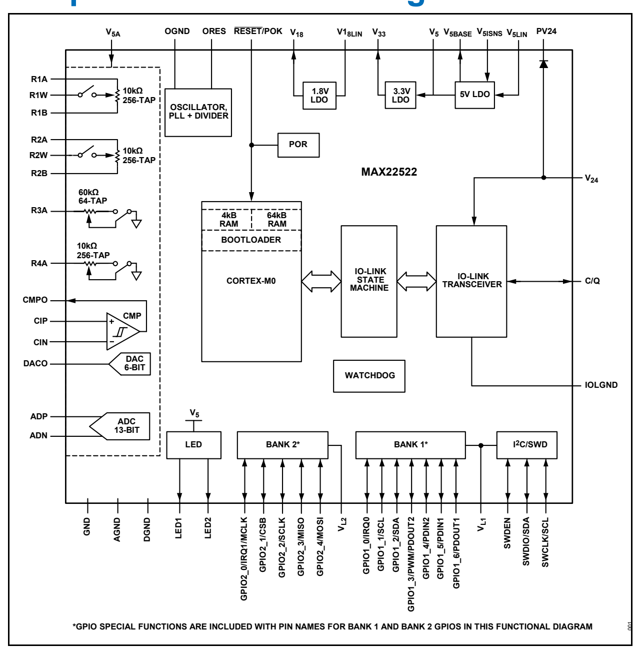
Low-noise 5V, 3.3V, and 1.8V linear regulators provide low-noise supplies for analog signal sensing. Optionally, an external NPN transistor may also be used to shunt regulator heat off-chip.

The 24V C/Q driver can be configured to operate in high-side (PNP), low-side (NPN), or push-pull (PP) modes. The C/Q current limit threshold is programmable from 50mA to 250mA.

An integrated comparator, a 6-bit DAC, a 13-bit ADC, and high-resolution variable resistors are included for signal conditioning for analog sensing circuitry.

The MAX22522 is available in a 60-bump WLP package (4.42mm × 2.64mm) and operates over the −40°C to +125°C temperature range.

Simplified Functional Diagram



Ordering Information appears at end of data sheet.

19-102072; Rev 0; 11/25

© 2025 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Product Highlights 1
General Description 1
Simplified Functional Diagram 1
Absolute Maximum Ratings 4
Package Information 4
Electrical Characteristics 5
Timing Diagrams 17
Typical Operating Characteristics 18
Pin Configurations 24
Pin Descriptions 24
Detailed Description 27
- Power 27
- Power-Up Sequencing 27
- PV24 Protected Supply 27
- V_5 Linear Regulator 27
- V_{33} Linear Regulator 28
- V_{18} Linear Regulator 28
- 24V Interface (V_{24}, C/Q, IOLGND) 28
- Variable Resistors (R1, R2) 28
- Variable Resistors (R3, R4) 28
- General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) 29
  - GPIO Alternate Functions 29
- High Speed Comparator and DAC (CMP, DAC) 30
- Analog-to-Digital Converter (ADC) 30
- Clock Control 31
- Timers and System Watchdog 31
  - SysTick Timer 31
- IO-Link Data Link Layer 31
  - SIO Mode 31
  - Wake-Up and Establish COM 31
  - Process Data Transfers 31
  - Process Data Output (PDOut) 31
  - Process Data Input (PDIn) 32
  - ISDU Transmission 32
- LED1, LED2: Status and Diagnostic Indicators 32

Applications Information 33
- Power Dissipation and Thermal Considerations 33

EMC Protection 33
Layout and Grounding 34
Ordering Information 34
Chip Information 34
Revision History 35

Absolute Maximum Ratings

(All voltages referenced to GND unless otherwise noted.).......

V_{24} (Continuous).. −36V to +36V

V_{24} (Peak, 100µs).. −52V to +60V

PV24 (Continuous)... −0.3V to +36V

PV24 (Peak, 100µs) MAX (−0.3V, V_{24} − 52V) to MIN (+52V, V_{24} + 52V)

V_{24} to PV24 .... −48V to +48V

C/Q (Continuous) MAX (−36V, V_{24} − 36V) to MIN (+36V, V_{24} + 36V)

C/Q (Peak, 100µs) MAX (−52V, V_{24} − 60V) to MIN (+52V, V_{24} + 60V)

GND, AGND, DGND, IOLGND .... −0.3V to +0.3V

V_{5LIN} (Continuous) .... MAX (−0.3V, V_{5BASE} − 0.3V) to +36V

V_{5LIN} (Peak, 100µs) .... MAX (−0.3V, V_{5BASE} − 0.3V) to +52V

V_{5ISNS} .... MAX (−0.3V, V_{5LIN} − 2V) to +36V

V_{5BASE} ....−0.3V to MIN (+18V, V_{5LIN} + 0.3V)

V_5, V_{5A} .... −0.3V to +6V

V_{33} ....−0.3V to (V_5 + 0.3V)

V_{18LIN}......................................MAX (−0.3V, V_{18} − 0.3V) to +6V

V_{18} .... −0.3V to +2V

V_{L1}, V_{L2} .... −0.3V to +6V

$\overline{\text{RESET}}$/POK ....−0.3V to +6V

ORES..−0.3V to (V_{18} + 0.3V)

R1A, R1B, R1W, R2A, R2B, R2W, R3A, R4A (Note 1) .. −0.3V to (V_{5A} + 0.3V)

CMPO ....−0.3V to (V_5 + 0.3V)

CIP, CIN, DACY..................................... −0.3V to (V_{5A} + 0.3V)

ADP, ADN...−0.3V to (V_{18} + 0.3V)

LED1, LED2...−0.3V to +6V

GPIO1_x ....−0.3V to (V_{L1} + 0.3V)

GPIO2_x ....−0.3V to (V_{L2} + 0.3V)

SWDEN, SWDIO/SDA, SWCLK/SCL.......−0.3V to (V_{L1} + 0.3V)

Continuous Current into V_{24}, C/Q, IOLGND ....±0.5A

Continuous Current into Variable Resistor, Rx............. ±2.5mA

Continuous Current into Any Other Pin .... ±50mA

Continuous Power Dissipation (T_A = +70°C, derates at 25.46mW/°C above +70°C)....................................... 2037mW

Operating Temperature Range..................... −40°C to +125°C

Maximum Junction Temperature.................................+150°C

Storage Temperature Range........................ −40°C to +150°C

Bump Reflow Temperature..+260°C

Note 1: Ensure that sink/source current does not exceed the maximum rating at any voltage.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	W602B4+1
Outline Number	*21-100691*
Land Pattern Number	Refer to the Application Note 1891*: Wafer-Level Packaging (WLP) and Its Applications*
Thermal Resistance, 4-Layer Board:	
Junction-to-Ambient (θ_{JA})	39.27°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to www.analog.com/en/resources/packaging-quality-symbols-footprints/package-index. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to www.analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.

Electrical Characteristics

(V_{24} = 7V to 36V, V_{5LIN} = V_5 to 36V, V_5 = 4.5V to 5.5V, V_{18LIN} = V_{18} to 5.5V, V_{18} = 1.71V to 1.89V, V_{L1} = 2.5V to 5.5V, V_{L2} = 1.62V to 5.5V, GND = DGND = OGND = AGND = IOLGND = 0V, and T_A = −40°C to +125°C, ORES connected to 10kΩ to GND. GPIO1_x, SWDEN at V_{L1} or GND. GPIO2_x at V_{L2} or GND. $\overline{\text{RESET}}$/POK pull-up to 3.3V. Typical values are at V_{24} = 24V, V_{L1} = V_{L2} = 3.3V, V_{5LIN} = V_5 = V_{5A} = 5V, V_{18LIN} = V_{18} = 1.8V, and T_A = +25°C (See Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{24} SUPPLY						
V_{24} Supply Voltage	V_{24}		7		36	V
V_{24} Undervoltage Error Threshold	$V_{24\_ERR\_R}$	V_{24} rising (See Note 3, Note 4)	6.6		6.9	V
V_{24} Undervoltage Error Threshold	$V_{24\_ERR\_F}$	V_{24} falling (See Note 3, Note 4)	6.1		6.5	V
V_{24} Undervoltage Warning Threshold	$V_{24\_WRN\_R}$	V_{24} rising (Note 4)	16	16.9	18	V
	$V_{24\_WRN\_F}$	V_{24} falling (Note 4)	15.5	16.5	17.5	
V_{24} Supply Current	I_{24_DIS}	No load on C/Q, V_5, and V_{18} powered externally, and the microcontroller is halted (See Note 5) / Registers in a default state, C/Q disabled, PLL off, and 921kHz precise oscillator off		0.03	0.11	mA
	$I_{24\_ACT\_H}$	No load on C/Q, V_5, and V_{18} powered externally, and the microcontroller is halted (See Note 5) / Registers in a default state except: C/Q in push-pull and high, PLL on, 921kHz precise oscillator on	0.3	0.437	0.7	
	$I_{24\_ACT\_L}$	No load on C/Q, V_5, and V_{18} powered externally, and the microcontroller is halted (See Note 5) / Registers in a default state except: C/Q in push-pull and low, PLL on, 921kHz precise oscillator on	0.3	0.419	0.7	
V_{24} Clamp Voltage	V_{24_CLAMP}	(V_{24} – GND), I_{LOAD} = 1mA	42	48.2	53	V
LOGIC SUPPLY (V_{L1}, V_{L2})						
V_{L1} Supply Voltage	V_{L1}		2.5		5.5	V
V_{L2} Supply Voltage	V_{L2}	(Note 6)	1.62		5.5	V
V_{L1} Supply Current	I_{L1}	All logic inputs are at GND or V_{L1}, no load on any logic outputs			60	µA
V_{L2} Supply Current	I_{L2}	All logic inputs are at GND or V_{L2}, no load on any logic outputs			70	µA
5V SUPPLY (V_5)						
V_5 Supply Voltage	V_5	V_5 externally supplied, V_{5LIN} = V_5	4.5		5.5	V
V_5 Undervoltage Lockout Threshold	$V_{5\_UVLO\_R}$	V_5 rising (See Note 4)	3.5		4.5	V
	$V_{5\_UVLO\_F}$	V_5 falling (See Note 4)	3.5		4.5	
V_5 Undervoltage Lockout Threshold Hysteresis	$V_{5\_UVLO\_HYST}$			140		mV

(V_{24} = 7V to 36V, V_{5LIN} = V_5 to 36V, V_5 = 4.5V to 5.5V, V_{18LIN} = V_{18} to 5.5V, V_{18} = 1.71V to 1.89V, V_{L1} = 2.5V to 5.5V, V_{L2} = 1.62V to 5.5V, GND = DGND = OGND = AGND = IOLGND = 0V, and T_A = −40°C to +125°C, ORES connected to 10kΩ to GND. GPIO1_x, SWDEN at V_{L1} or GND. GPIO2_x at V_{L2} or GND. $\overline{\text{RESET}}$/POK pull-up to 3.3V. Typical values are at V_{24} = 24V, V_{L1} = V_{L2} = 3.3V, V_{5LIN} = V_5 = V_{5A} = 5V, V_{18LIN} = V_{18} = 1.8V, and T_A = +25°C (See Note 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_5 Supply Current	I_{5_DIS}	No load on C/Q, V_5, and V_{18} powered externally, and the microcontroller halted (See Note 5)	Registers in default state, C/Q disabled, PLL off, and IO-Link oscillator off	0.1		0.27	mA
	$I_{5\_ACT\_H}$	No load on C/Q, V_5, and V_{18} powered externally, and the microcontroller halted (See Note 5)	Registers in default state except: C/Q in push-pull and high, PLL on, 921kHz precise oscillator on	0.25		0.57	
	$I_{5\_ACT\_L}$	No load on C/Q, V_5, and V_{18} powered externally, and the microcontroller halted (See Note 5)	Registers in default state except: C/Q in push-pull and low, PLL on, 921kHz precise oscillator on	0.25		0.57	
1.8V SUPPLY (V_{18})							
V_{18} Supply Voltage	V_{18}	V_{18LIN} = V_{18}, V_{18} externally supplied		1.71		1.89	V
V_{18} Undervoltage Lockout Threshold	$V_{18\_UVLO\_R}$	V_{18} rising (See Note 4)		1.66		1.76	V
	$V_{18\_UVLO\_F}$	V_{18} falling (See Note 4)		1.62		1.72	
V_{18} Undervoltage Lockout Threshold Hysteresis					35		mV
V_{18} Supply Current	I_{18_SLEEP}	V_5 and V_{18} powered externally, f_{HCLK} = 18MHz, sleep mode	PLL off		0.9		mA
			PLL on		2.1		
	I_{18_DIS}	V_5 and V_{18} powered externally, f_{HCLK} = 18MHz, microcontroller halted (See Note 5)	Registers in a default state, PLL off, and 921kHz precise oscillator off	2.8		4.6	
	I_{18_ACT}	V_5 and V_{18} powered externally, f_{HCLK} = 36MHz, microcontroller halted (See Note 5)	Registers in a default state, PLL on, and 921kHz precise oscillator on	4.5	6.7	9	
		V_5 and V_{18} powered externally, f_{HCLK} = 18MHz, executing code from RAM	PLL off		5.4		
			PLL on		6.6		
V_{5A} SUPPLY (V_{5A})							

(V_{24} = 7V to 36V, V_{5LIN} = V_5 to 36V, V_5 = 4.5V to 5.5V, V_{18LIN} = V_{18} to 5.5V, V_{18} = 1.71V to 1.89V, V_{L1} = 2.5V to 5.5V, V_{L2} = 1.62V to 5.5V, GND = DGND = OGND = AGND = IOLGND = 0V, and T_A = −40°C to +125°C, ORES connected to 10kΩ to GND. GPIO1_x, SWDEN at V_{L1} or GND. GPIO2_x at V_{L2} or GND. $\overline{RESET}$/POK pull-up to 3.3V. Typical values are at V_{24} = 24V, V_{L1} = V_{L2} = 3.3V, V_{5LIN} = V_5 = V_{5A} = 5V, V_{18LIN} = V_{18} = 1.8V, and T_A = +25°C (See *Note 2*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{5A} Supply Voltage	V_{5A}		4.5		5.5	V
V_{5A} Supply Current	I_{5A_DIS}	Digipots, comparators, and DACs disabled			4.5	μA
	I_{5A_ACT}	Digipots, comparators, and DACs enabled, Digipots and DAC set at mid-code, comparators fast mode enabled			60	
ACTIVE DIODE (PV24)						
Active Diode On-Resistance	R_{ACT}	I_{LOAD} = 10mA		3.1	7	Ω
Active Diode Current Limit	I_{ACTMAX}	I_{LOSS} < 1%	110		430	mA
5V LINEAR REGULATOR (V_5, V_{5LIN}, V_{5BASE}, V_{5ISNS})						
V_{5LIN} Input Supply Voltage	V_{5LIN}		6		36	V
V_{5LIN} Supply Current	I_{5LIN_DIS}	V_5 = V_{5LIN}, V_5 regulator is disabled	10		60	μA
	I_{5LIN_ACT}	V_5 = 36V, no load	50		350	
V_5 Output Voltage	V_{5_OUT}	7V ≤ V_{5LIN} ≤ 36V	4.8		5.2	V
V_5 Load Regulation	ΔV_{5_LDR}	V_{5LIN} = 24V, 1mA ≤ I_{LOAD} ≤ 50mA		2	5	%
V_5 Line Regulation	ΔV_{5_LNR}	6V ≤ V_{5LIN} ≤ 36V, I_{LOAD} = 1mA	−0.2		+0.2	mV/V
V_5 Current limit	I_{5_SHORT}		52		250	mA
V_{5LIN} to V_5 Enable Voltage Threshold	$V_{THR\_V5LIN\_R}$	(V_{5LIN} – V_5) rising	0.2	0.43	0.7	V
	$V_{THR\_V5LIN\_F}$	(V_{5LIN} – V_5) falling	0.17	0.41	0.67	
V_{5LIN} to V_5 Enable Voltage Threshold Hysteresis	$V_{THR\_V5LIN\_HYST}$			20		mV
V_{5LIN} to V_5 Enable Voltage Threshold	$V_{THR\_V5LIN\_F}$	(V_{5LIN} – V_5) falling	2.2			μF
3.3V LINEAR REGULATOR (V_{33})						
V_{33} Output Voltage	V_{33}		3.2		3.45	V
V_{33} Load Regulation	ΔV_{33_LDR}	V_5 = 5V, 1mA ≤ I_{LOAD} ≤ 50mA	0	1.0	5	%
V_{33} Line Regulation	ΔV_{33_LNR}	4.5V ≤ V_5 ≤ 5.5V, I_{LOAD} = 1mA	−1		+1	mV/V
V_{33} Current Limit	I_{33_SHORT}		68		208	mA
V_{33} Load Capacitance	C_{33}	Required capacitance for stability, ±20% tolerance allowed	2.2			μF
1.8V LINEAR REGULATOR (V_{18})						
V_{18LIN} Input Supply Voltage	V_{18LIN}		2.7		5.5	V
V_{18} Output Voltage	V_{18_OUT}	2.7V ≤ V_{18LIN} ≤ 5.5V	1.74		1.86	V
V_{18} Load Regulation	ΔV_{18_LDR}	V_{18LIN} = 5V, 1mA ≤ I_{LOAD} ≤ 50mA		1	4	%
V_{18} Line Regulation	ΔV_{18_LNR}	2.7V ≤ V_{18LIN} ≤ 5.5V, I_{LOAD} = 1mA	−0.6		+0.6	mV/V
V_{18} Current Limit	I_{V18_SHORT}		68		208	mA
V_{18LIN} to V_{18} Enable Voltage Threshold	$V_{THR\_V18LIN\_R}$	(V_{18LIN} – V_{18}) rising	0.15		0.7	V

(V_{24} = 7V to 36V, V_{5LIN} = V_5 to 36V, V_5 = 4.5V to 5.5V, V_{18LIN} = V_{18} to 5.5V, V_{18} = 1.71V to 1.89V, V_{L1} = 2.5V to 5.5V, V_{L2} = 1.62V to 5.5V, GND = DGND = OGND = AGND = IOLGND = 0V, and T_A = −40°C to +125°C, ORES connected to 10kΩ to GND. GPIO1_x, SWDEN at V_{L1} or GND. GPIO2_x at V_{L2} or GND. $\overline{\text{RESET}}$/POK pull-up to 3.3V. Typical values are at V_{24} = 24V, V_{L1} = V_{L2} = 3.3V, V_{5LIN} = V_5 = V_{5A} = 5V, V_{18LIN} = V_{18} = 1.8V, and T_A = +25°C (See Note 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
18MHz RAW OSCILLATOR							
Raw Oscillator Frequency	f_{CLK_INT}	(See Note 7)		17.51	18.432	19.35	MHz
921kHz PRECISION REFERENCE OSCILLATOR							
Reference Oscillator Supply Current	I_{POSC_REF}			230		550	µA
Internal Reference Oscillator Frequency	f_{POSC_REF}	10kΩ ±0.1% resistance between ORES and OGND		912.5	921.6	931.0	kHz
Internal Reference Oscillator Precision	PRE_{POSC_REF}	10kΩ ±0.1% resistance between ORES and OGND		−1.00		+1.00	%
External Oscillator Required Resistance	R_{ORES}	±0.1% tolerance			10		kΩ
PHASE-LOCKED LOOP (PLL)							
PLL Supply Current	I_{PLL}	PLL_{MULT} = 80, PLL current sourced from V_{18}			0.8	1.6	mA
PLL Multiplying factor	PLL_{MULT}				80		
C/Q DRIVER							
C/Q Driver High-Side On-Resistance	R_{CQOH}	High-side enabled, CQ_CL= 11, I_{LOAD} = 150mA (See Note 8)			0.97	2	Ω
C/Q Driver Low-Side On-Resistance	R_{CQOL}	Low-side enabled, CQ_CL= 11, I_{SINK} = 150mA (See Note 8)			1.7	3.4	Ω
C/Q Driver Current Limit	I_{CQ_CL}	V_{CQ} = (V_{24} – 3V) or 3V	CQ_CL[1:0] = 00	53	60	65	mA
			CQ_CL[1:0] = 01	106	120	130	
			CQ_CL[1:0] = 10	209	240	255	
			CQ_CL[1:0] = 11	259	287	317	
C/Q Driver Short Circuit Protection	I_{CQ_FAULT}	Relative to the typical programmed current limit			25		%
C/Q Reverse Current	$I_{REV\_CQ\_H}$	V_{24} = 24V, C/Q enabled, and high impedance or pull-up enabled	V_{CQ} = V_{24} + 5V	0.25		0.7	mA
	$I_{REV\_CQ\_L}$	V_{24} = 24V, C/Q enabled, and high impedance or pull-down enabled	V_{CQ} = −5V	−0.025		−0.005	
C/Q Input Current (High Impedance)	I_{CQ_HZ}	V_{24} = 24V, C/Q enabled, push-pull, high impedance, no pull-up or pull-down enabled	0.1V ≤ V_{CQ} ≤ (V_{24} − 0.1V)	−19		+19	µA
C/Q Leakage Current	I_{CQ_LKG}	V_{24} = 24V, C/Q disabled, no pull-up or pull-down enabled	(V_{24} − 36V) ≤ V_{CQ} ≤ 36V	−44		+55	µA
C/Q Clamp Voltage	V_{CQ_CLAMP}	V_{24} − V_{CQ}, I_{LOAD} = −1mA		42	48.2	53	V
		V_{CQ} − GND, I_{LOAD} = 1mA		42	48.2	53	

(V_{24} = 7V to 36V, V_{5LIN} = V_5 to 36V, V_5 = 4.5V to 5.5V, V_{18LIN} = V_{18} to 5.5V, V_{18} = 1.71V to 1.89V, V_{L1} = 2.5V to 5.5V, V_{L2} = 1.62V to 5.5V, GND = DGND = OGND = AGND = IOLGND = 0V, and T_A = −40°C to +125°C, ORES connected to 10kΩ to GND. GPIO1_x, SWDEN at V_{L1} or GND. GPIO2_x at V_{L2} or GND. $\overline{RESET}$/POK pull-up to 3.3V. Typical values are at V_{24} = 24V, V_{L1} = V_{L2} = 3.3V, V_{5LIN} = V_5 = V_{5A} = 5V, V_{18LIN} = V_{18} = 1.8V, and T_A = +25°C (See *Note 2*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
C/Q Rise Time	t_{CQ_RISE}	Push-pull or PNP mode, V_{24} = 30V, CQ_CL[1:0] = 11	CQ_SLEW[1:0] = 00	0.11		0.23	µs
			CQ_SLEW[1:0] = 01	0.24		0.48	
			CQ_SLEW[1:0] = 10	0.36		0.75	
			CQ_SLEW[1:0] = 11	2.5		6.3	
C/Q Fall Time	t_{CQ_FALL}	Push-pull or NPN mode, V_{24} = 30V, CQ_CL[1:0] = 11	CQ_SLEW[1:0] = 00	0.13		0.27	µs
			CQ_SLEW[1:0] = 01	0.26		0.52	
			CQ_SLEW[1:0] = 10	0.38		0.79	
			CQ_SLEW[1:0] = 11	1.8		5	
C/Q Driver Propagation Delay	t_{CQ_PLH}	Push-pull, V_{24} = 30V, CQ_CL[1:0] = 11	CQ_SLEW[1:0] = 00	0.15		0.70	µs
	t_{CQ_PHL}	Push-pull, V_{24} = 30V, CQ_CL[1:0] = 11	CQ_SLEW[1:0] = 00	0.15		0.90	
C/Q Skew	t_{CQ_SKEW}	Push-pull, V_{24} = 30V, CQ_CL[1:0] = 11	CQ_SLEW[1:0] = 00	−0.50		+0.50	µs
C/Q PULL-UP/PULL-DOWN							
C/Q Weak Pull-Up	I_{CQPUW}	C/Q disabled, weak pull-up enabled	V_{CQ} = 5V	−200		−130	µA
C/Q Weak Pull-Down	I_{CQPDW}	C/Q disabled, weak pull-down enabled	V_{CQ} = (V_{24} − 5V)	+150		+200	µA
C/Q 2mA Pull-Up	I_{CQPU2}	C/Q disabled, 2mA pull-up enabled	V_{CQ} = 5V	−2.4		−1.9	mA
C/Q 2mA Pull-Down	I_{CQPD2}	C/Q disabled, 2mA pull-down enabled	V_{CQ} = (V_{24} − 5V)	1.9		2.4	mA
C/Q RECEIVER							
C/Q Input Voltage Range	V_{CQ_IN}	For valid C/Q reception		V_{24} − 36V		36	V
C/Q Input Threshold High	V_{CQ_TH}	V_{24} ≥ 18V		11.3		12.2	V
		V_{24} < 18V		62		68	$\%V_{24}$
C/Q Input Threshold Low	V_{CQ_TL}	V_{24} ≥ 18V		9.4		10.3	V
		V_{24} < 18V		52		58	$\%V_{24}$
C/Q Input Capacitance	C_{IN_CQ}				72		pF
C/Q Receiver Propagation Delay	t_{CQIN_PLH}	RX_FILTER = 0		0.16		0.58	µs
		RX_FILTER = 1		0.5		1.8	
	t_{CQIN_PHL}	RX_FILTER = 0		0.21		0.66	
		RX_FILTER = 1		0.5		1.8	

(V_{24} = 7V to 36V, V_{5LIN} = V_5 to 36V, V_5 = 4.5V to 5.5V, V_{18LIN} = V_{18} to 5.5V, V_{18} = 1.71V to 1.89V, V_{L1} = 2.5V to 5.5V, V_{L2} = 1.62V to 5.5V, GND = DGND = OGND = AGND = IOLGND = 0V, and T_A = −40°C to +125°C, ORES connected to 10kΩ to GND. GPIO1_x, SWDEN at V_{L1} or GND. GPIO2_x at V_{L2} or GND. $\overline{RESET}$/POK pull-up to 3.3V. Typical values are at V_{24} = 24V, V_{L1} = V_{L2} = 3.3V, V_{5LIN} = V_5 = V_{5A} = 5V, V_{18LIN} = V_{18} = 1.8V, and T_A = +25°C (See Note 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
C/Q Receiver Skew	t_{CQIN_SKEW}	RX_FILTER = 0		−0.3		+0.3	µs
		RX_FILTER = 1		−1		+1	
ANALOG-TO-DIGITAL CONVERTER (ADC)							
ADC Resolution	N_{BIT_ADC}				12 + sign		bit
ADC Input Voltage Range	V_{ADC}	(V_{ADP} − V_{ADN})		−1.27		+1.27	V
		V_{ADP}, V_{ADN} to ground		0		V_{18}	
ADC Internal Reference	V_{ADC_REF}			1.235	1.25	1.27	V
ADC INL	INL_{ADC}	f_{CONV} = 500ksps		−10		+10	LSB
ADC DNL	DNL_{ADC}	f_{CONV} = 500ksps		−3.5		+3.5	LSB
ADC Gain Error		V_{FS} = 2.5V		−0.8		+0.8	$\%V_{FS}$
ADC Offset Error		ADC output with V_{ADP} = V_{ADN} = 0V		−8		+8	LSB
Conversion Time	t_{ADC}	ADC clock is HCLK			33		Clock cycles
ADP, ADN Input Leakage	I_{ADP}, I_{ADN}	$V_{ADP, ADN}$ = 1.8V		−1		+1	µA
ADC INPUT MUX AND BUFFER							
ADC Buffer Input Range	V_{BUFIN}	GPIO1_3 – GPIO1_6, when configured as ADC inputs		0		V_{5A}	V
ADC Buffer Output Range	V_{BUFOUT}			0.01		1.4	V
ADC Buffer Offset	V_{BUF_OS}	Buffer input = 0.01V to 1.5V		−4		+4	mV
ADC -3dB Buffer Bandwidth	V_{BUF_BW}				1.5		MHz
ADC Buffer Internal Voltage Reference	V_{BUF_REF}			712		725	mV
ANALOG COMPARATORS AND DIGITAL-TO-ANALOG CONVERTERs (DACs) (CIP, CIN, CMPO, DACY) (CMP_IN_HIGH = 1, CMP_IN_LOW = 1)							
Comparator Common Mode Range	V_{CM_CMP}			0		V_{5A}	V
Comparator Offset	V_{OS_CMP}	CIP_ rising	Input = 0V	−20	0	+15	mV
			Input = V_{5A}	−15	0	+15	
			Input = V_{5A} / 2	−12	0	+12	
Comparator Hysteresis	$V_{OS\_CMP\_HYST}$	Input = 0V to V_{5A}			25		mV
Comparator Response Time	t_{CMP}	CIP_ Threshold = 2.5V, CIP_ from 2.4V to 2.6V	CMP_FILT_EN = 0, CMP_SLOW_EN = 0	30		120	ns
			CMP_FILT_EN = 0, CMP_SLOW_EN = 1	120		810	
			CMP_FILT_EN = 1, CMP_SLOW_EN = 0	0.75		1.65	µs
			CMP_FILT_EN = 1, CMP_SLOW_EN = 1	0.9		2.2	

(V_{24} = 7V to 36V, V_{5LIN} = V_5 to 36V, V_5 = 4.5V to 5.5V, V_{18LIN} = V_{18} to 5.5V, V_{18} = 1.71V to 1.89V, V_{L1} = 2.5V to 5.5V, V_{L2} = 1.62V to 5.5V, GND = DGND = OGND = AGND = IOLGND = 0V, and T_A = −40°C to +125°C, ORES connected to 10kΩ to GND. GPIO1_x, SWDEN at V_{L1} or GND. GPIO2_x at V_{L2} or GND. $\overline{\text{RESET}}$/POK pull-up to 3.3V. Typical values are at V_{24} = 24V, V_{L1} = V_{L2} = 3.3V, V_{5LIN} = V_5 = V_{5A} = 5V, V_{18LIN} = V_{18} = 1.8V, and T_A = +25°C (See Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Comparator Input Leakage	I_{CMP_LKG}	$V_{CIP, CIN}$ = 0V to 5.5V	−1		+1	μA
Comparator Output High	V_{CMPO_H}	I_{LOAD} = 5mA	V_{5A} − 0.15		V_{5A}	V
Comparator Output Low	V_{CMPO_L}	I_{LOAD} = −5mA			0.1	V
DAC Full Scale	$V_{DAC\_}$			100		%V_{5A}
DAC Resolution	N_{DAC}			6		BIT
DAC INL	INL_{DAC}		−0.35		+0.35	LSB
DAC DNL			−0.2		+0.2	LSB
DAC Monotonicity		Guaranteed by DNL test				
DAC Output Resistance	R_{DAC}			273		kΩ
VARIABLE RESISTORS (R1, R2, R3, R4) (See Note 9)						
R1, R2 Resistor Value	R_{R1}, R_{R2}		8.2	10.9	13.6	kΩ
R1W, R2W Wiper Resistance	R_{R1W}, R_{R2W}	0V < V_{R1W}, $V_{R2W\_}$ ≤ V_{5A}, I_{TEST} = 200μA; T_A = 25°C	35	52	65	Ω
		0V < V_{R1W}, $V_{R2W\_}$ ≤ V_{5A}, I_{TEST} = 200μA; −40°C ≤ T_A ≤ 125°C	15	55	120	Ω
R1, R2 Off-Current	$I_{OFF\_R1\_}$ $I_{OFF\_R2\_}$	R1, R2 disabled, 0V ≤ $V_{R1\_}$, $V_{R2\_}$ ≤ V_{5A}	−1		+1	μA
R1, R2 Bandwidth	BW_{R1}, BW_{R2}	R1A/R2A connected to 2.5V_{DC}, drive R1W/R2W with a 1.2kΩ resistor, R1B/R2B is unconnected, Rx_POS = 0x80 (See Figure 1)		0.866		MHz
R1, R2 INL	$INL_{R1, R2}$		−3.5		+1	LSB
R1, R2 DNL	DNL_{R1}, DNL_{R2}		−1.2		+1.2	LSB
R1A, R1B, R2A, R2B Capacitance	$C_{R1\_}$, $C_{R2\_}$	R1/R2 disabled, V_{RxA} = V_{RxB} = V_{RxW} = 0V		14		pF
R1W, R2W Off-Capacitance	C_{R1W}, C_{R2W}	R1/R2 disabled, V_{RxA} = V_{RxB} = V_{RxW} = 0V		10		pF
R1A, R1B, R2A, R2B On-Capacitance	C_{R1_ON}, C_{R2_ON}	R1, R2 enabled, set to minimum resistance, V_{RxW} = 0V		14		pF
R3 Resistor Value	R_{R3}	I_{TEST} = 100μA or V_{TEST} = 0.5V	47	63	79	kΩ
R3 Steps	N_{R3}			63		

(V_{24} = 7V to 36V, V_{5LIN} = V_5 to 36V, V_5 = 4.5V to 5.5V, V_{18LIN} = V_{18} to 5.5V, V_{18} = 1.71V to 1.89V, V_{L1} = 2.5V to 5.5V, V_{L2} = 1.62V to 5.5V, GND = DGND = OGND = AGND = IOLGND = 0V, and T_A = −40°C to +125°C, ORES connected to 10kΩ to GND. GPIO1_x, SWDEN at V_{L1} or GND. GPIO2_x at V_{L2} or GND. $\overline{\text{RESET}}$/POK pull-up to 3.3V. Typical values are at V_{24} = 24V, V_{L1} = V_{L2} = 3.3V, V_{5LIN} = V_5 = V_{5A} = 5V, V_{18LIN} = V_{18} = 1.8V, and T_A = +25°C (See Note 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
R3 Maximum Current	I_{R3}	(See Note 8)			2		mA
R3 Leakage Current	I_{OFFR3}	R3 disabled, V_{R3} = 0V to V_{5A}		−1		+1	µA
R3 INL	INL_{R3}	From 0 to 63		−0.25		+0.25	LSB
R3 DNL				−0.08		+0.08	LSB
R3 Capacitance	C_{R3}	R3 disabled, V_{R3} = 0V			7		pF
R4 Resistor Value	R_{R4_0}	V_{TEST} = 0.5V	R4_POS = 0x00	8.5	11.1	14.5	kΩ
	R_{R4_8}	V_{TEST} = 0.5V	R4_POS = 0x08	8	10.7	14	
	R_{R4_255}	V_{TEST} = 0.5V	R4_POS = 0xFF	0.07	0.11	0.16	
R4 Steps					256		
R4A Off-Current	I_{OFF_R4A}	R4 disabled, 0V to V_{5A}		−1		+1	µA
R4 INL	INL_{R4}			−0.8		+0.8	LSB
R4 DNL				−0.5		+0.5	LSB
R_{4A} Capacitance	C_{R4A}	R4 disabled, V_{R4A} = 0V			21		pF
LED OUTPUT (LED1, LED2)							
LED_ Output Voltage Low	V_{LED_OL}	I_{LOAD} = −5mA				0.2	V
LED_ High Impedance Leakage Current	I_{LED_OL}	0V ≤ V_{LEDx} ≤ 5.5V		−1		+1	µA
$\overline{\text{RESET}}$/POK							
$\overline{\text{RESET}}$/POK Input Voltage High	V_{RST_IH}			1.7			V
$\overline{\text{RESET}}$/POK Input Voltage Low	V_{RST_IL}					1.3	V
$\overline{\text{RESET}}$/POK Output Voltage Low	V_{POK_LOW}	I_{LOAD} = −5mA				0.1	V
$\overline{\text{RESET}}$/POK High Impedance Leakage Current	I_{RST_OD}	0V ≤ V_{RESET_POK} ≤ 5.5V		−1		+1	µA
BANK 1 GPIOs (GPIO1_0 – GPIO1_6)							
GPIO1_x Input Voltage High	$V_{GPIO1IH}$	Not in I²C mode		0.70 × V_{L1}			V
GPIO1_x Input Voltage Low	$V_{GPIO1IL}$	Not in I²C mode				0.28 × V_{L1}	V
GPIO1_2 I²C Mode SDA Input Voltage High	V_{SDA_IH}	GPIO1_2 configured in I²C mode		1.8			V
GPIO1_2 I²C Mode SDA Input Voltage Low	V_{SDA_IL}	GPIO1_2 configured in I²C mode				1	V
GPIO1_x Output Voltage High	V_{GPIO1_OH}	I_{LOAD} = 5mA		V_{L1} − 0.26			V
GPIO1_x Output Voltage Low	V_{GPIO1_OL}	I_{LOAD} = −5mA				0.2	V
GPIO1_x Pull-Up Resistance	R_{GPIO1_PU}	V_{GPIO1_x} = 0V, pull-up enabled		230		470	kΩ

(V_{24} = 7V to 36V, V_{5LIN} = V_5 to 36V, V_5 = 4.5V to 5.5V, V_{18LIN} = V_{18} to 5.5V, V_{18} = 1.71V to 1.89V, V_{L1} = 2.5V to 5.5V, V_{L2} = 1.62V to 5.5V, GND = DGND = OGND = AGND = IOLGND = 0V, and T_A = −40°C to +125°C, ORES connected to 10kΩ to GND. GPIO1_x, SWDEN at V_{L1} or GND. GPIO2_x at V_{L2} or GND. $\overline{\text{RESET}}$/POK pull-up to 3.3V. Typical values are at V_{24} = 24V, V_{L1} = V_{L2} = 3.3V, V_{5LIN} = V_5 = V_{5A} = 5V, V_{18LIN} = V_{18} = 1.8V, and T_A = +25°C (See Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GPIO1_x Pull-Down Resistance	R_{GPIO1_PD}	V_{GPIO1_x} = V_{L1}, pull-down enabled	230		430	kΩ
GPIO1_x Leakage Current	I_{GPIO1_LKG}	GPIO1_x is high impedance, no pull-up or pull-down enabled	−1		+1	µA
GPIO1_x Input Capacitance	C_{GPIO1_IN}			2		pF
GPIO1_x Analog Input Capacitance	C_{GPIO1_AN}	GPIO1_x is configured as analog input		2		pF
GPIO2_0 PIN (GPIO2_0/IRQ1/MCLK)						
GPIO2_0 Input Voltage High	V_{GPIO20_IH}	GPIO2_0 is not configured as MCLK input	0.70 × V_{L2}			V
GPIO2_0 Input Voltage Low	V_{GPIO20_IL}	GPIO2_0 is not configured as MCLK input			0.28 × V_{L2}	V
MCLK Input Voltage High	V_{MCLK_IH}	GPIO2_0 is configured as MCLK input, V_{L2} ≥ 2.5V	1.6			V
MCLK Input Voltage Low	V_{MCLK_IL}	GPIO2_0 is configured as MCLK input, V_{L2} ≥ 2.5V			0.4	V
GPIO2_0 Output Voltage High	V_{GPIO20_OH}	I_{LOAD} = 5mA, V_{L2} ≥ 2.5V	V_{L2} − 0.35			V
GPIO2_0 Output Voltage Low	V_{GPIO20_OL}	I_{LOAD} = −5mA, V_{L2} ≥ 2.5V			0.32	V
GPIO2_0 Pull-Up Resistance	R_{GPIO20_PU}	V_{GPIO2_0} = 0V, pull-up enabled	240		440	kΩ
GPIO2_0 Pull-Down Resistance	R_{GPIO20_PD}	V_{GPIO2_0} = V_{L2}, pull-down enabled	230		430	kΩ
GPIO2_0 Leakage Current	I_{GPIO20_LKG}	GPIO2_0 is high impedance, no pull-up or pull-down enabled	−1		+1	µA
GPIO2_0 Input Capacitance	C_{GPIO20_IN}			2		pF
BANK 2 GPIOs (GPIO2_1 to GPIO2_4)						
GPIO2_x Input Voltage High	V_{GPIO2_IH}		0.82 × V_{L2}			V
GPIO2_x Input Voltage Low	V_{GPIO2_IL}				0.18 × V_{L2}	V
GPIO2_x Output Voltage High	V_{GPIO2_OH}	I_{LOAD} = 5mA	V_{L2} − 0.35			V
GPIO2_x Output Voltage Low	V_{GPIO2_OL}	I_{LOAD} = -5mA			0.32	V
GPIO2_x Pull-Up Resistance	R_{GPIO2_PU}	V_{GPIO2_x} = 0V, pull-up enabled	200		470	kΩ
GPIO2_x Pull-Down Resistance	R_{GPIO2_PD}	V_{GPIO2_x} = V_{L2}, pull-down enabled	200		450	kΩ
GPIO2_x Leakage Current	I_{GPIO2_LKG}	GPIO2_x is high impedance, no pull-up or pull-down enabled	−1		+1	µA
GPIO2_x Input Capacitance	C_{GPIO2_IN}			2		pF
SERIAL WIRE DEBUG (SWD) INTERFACE (SWDEN, SWDIO/SDA, SWCLK/SCL)						

(V_{24} = 7V to 36V, V_{5LIN} = V_5 to 36V, V_5 = 4.5V to 5.5V, V_{18LIN} = V_{18} to 5.5V, V_{18} = 1.71V to 1.89V, V_{L1} = 2.5V to 5.5V, V_{L2} = 1.62V to 5.5V, GND = DGND = OGND = AGND = IOLGND = 0V, and T_A = −40°C to +125°C, ORES connected to 10kΩ to GND. GPIO1_x, SWDEN at V_{L1} or GND. GPIO2_x at V_{L2} or GND. $\overline{RESET}$/POK pull-up to 3.3V. Typical values are at V_{24} = 24V, V_{L1} = V_{L2} = 3.3V, V_{5LIN} = V_5 = V_{5A} = 5V, V_{18LIN} = V_{18} = 1.8V, and T_A = +25°C (See Note 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage High	V_{SWD_IH}			1.6			V
Input Voltage Low	V_{SWD_IL}					1.1	V
Output Voltage High	V_{SWD_H}	I_{LOAD} = 5mA		V_{L1} − 0.15			V
Output Voltage Low	V_{SWD_L}	I_{LOAD} = −5mA				0.15	V
SWDEN Pull-Down Resistance	I_{SWD_EN}			80		170	kΩ
SWDIO/SDA Leakage Current	I_{SWD_LKG}			−1		+1	µA
THERMAL PROTECTION							
C/Q Driver Shutdown Temperature	T_{SHUT_DRV}	Driver temperature rising			+160		°C
C/Q Driver Shutdown Temperature Hysteresis	$T_{SHUT\_DRV\_HYST}$				12		°C
IC Thermal Warning Temperature	T_{WRN}				+135		°C
IC Thermal Warning Temperature Hysteresis	T_{WRN_HYST}				14		°C
IC Thermal Shutdown Temperature	T_{SHUT_IC}				+170		°C
IC Thermal Shutdown Temperature Hysteresis	$T_{SHUT\_IC\_HYST}$				14		°C
INTERNAL THERMAL SENSOR							
Thermal Sensor Precision					±13		°C
Thermal Sensor Slope					2.0		mV/°C
Thermal Sensor Voltage	V_{TS_PTAT}	T_{DIE} = 25°C		565	590	620	mV
EMC TOLERANCE							
Electrostatic discharge (ESD) Protection (V_{24}, C/Q, to GND)		IEC 61000-4-2 Contact Discharge			±4		kV
ESD Protection (V_{24}, C/Q, to GND)		IEC 61000-4-2 Air-Gap			±6		kV
ESD Protection		Human Body Model	V_{24}, C/Q to GND		±2		kV
			All other Pins		±2		
Surge Protection (V_{24}, C/Q, to GND)		500Ω 8µs/20µs surge to GND			±1.2		kV
AC ELECTRICAL CHARACTERISTICS							
SWD TIMING							
Clock Frequency	f_{CLK_SWD}					10	MHz
Data Output Delay	t_{DO}				35		ns
Data Hold Time	t_{HD}			10			ns
Data Setup Time	t_{SU}			10			ns

(V_{24} = 7V to 36V, V_{5LIN} = V_5 to 36V, V_5 = 4.5V to 5.5V, V_{18LIN} = V_{18} to 5.5V, V_{18} = 1.71V to 1.89V, V_{L1} = 2.5V to 5.5V, V_{L2} = 1.62V to 5.5V, GND = DGND = OGND = AGND = IOLGND = 0V, and T_A = −40°C to +125°C, ORES connected to 10kΩ to GND. GPIO1_x, SWDEN at V_{L1} or GND. GPIO2_x at V_{L2} or GND. $\overline{\text{RESET}}$/POK pull-up to 3.3V. Typical values are at V_{24} = 24V, V_{L1} = V_{L2} = 3.3V, V_{5LIN} = V_5 = V_{5A} = 5V, V_{18LIN} = V_{18} = 1.8V, and T_A = +25°C (See Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C HOST CONTROLLER TIMING (See Figure 2), (GPIO1_1, GPIO1_2 CONFIGURED FOR I²C FUNCTIONALITY)						
SCL Clock Frequency	$1/t_{SCL}$				1	MHz
Data to Clock Delay in Start Condition	$t_{DC:STA}$			t_{SCL} × 0.4		ns
Data to Clock Delay in Repeated Start Condition	$t_{DC:STA}$			t_{SCL} × 0.4		ns
Clock to Data Delay in Repeated Start Condition	$t_{CD:STA}$			t_{SCL} × 0.2		ns
Low Period of SCL Clock	t_{LOW}			50		%
High Period of SCL Clock	t_{HIGH}			50		%
Data Hold Time	$t_{HD:DAT}$			0		ns
Data Setup Time	$t_{SU:DAT}$		55			ns
Data Output Delay	t_{DLY_DO}			1	3	ns
Setup Time for Stop	t_{CD_STP}			t_{SCL} × 0.4		ns
SPI HOST CONTROLLER TIMING (See Figure 3) (GPIO2_0 to GPIO2_4 CONFIGURED FOR SPI FUNCTIONALITY)						
SCLK Clock Frequency	$1/t_{SCLK}$	(See Note 10)			$f_{HCLK}/4$	MHz
SCLK Pulse Width High	t_{CH}			0.5 × t_{SCLK}		ns
SCLK Pulse Width Low	t_{CL}			0.5 × t_{SCLK}		ns
$\overline{\text{CS}}$ Fall to SCLK Rise Time	t_{CSS}	(See Note 11, Note 12)		(CS_SETTLE_TIM + 1) x t_{SYS} + 0.5 × t_{SCLK}		ns
MISO Setup Time	t_{DS}	V_{L2} = 1.62V	40			ns
		V_{L2} = 3.3V to 5.5V	12			
MISO Hold Time	t_{DH}	V_{L2} = 1.62V	0			ns
		V_{L2} = 3.3V to 5.5V	17			
MOSI Output Delay	t_{DO}	V_{L2} = 1.62V		1		ns
		V_{L2} = 3.3V to 5.5V		1		
SCLK to $\overline{\text{CS}}$ Rise	t_{CSH}			0.5 × t_{SCLK}		ns
I²C DEVICE TIMING						
SCL Clock Frequency	f_{SCL}	(See Note 13)			1	MHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		0.3			µs

(V_{24} = 7V to 36V, V_{5LIN} = V_5 to 36V, V_5 = 4.5V to 5.5V, V_{18LIN} = V_{18} to 5.5V, V_{18} = 1.71V to 1.89V, V_{L1} = 2.5V to 5.5V, V_{L2} = 1.62V to 5.5V, GND = DGND = OGND = AGND = IOLGND = 0V, and T_A = −40°C to +125°C, ORES connected to 10kΩ to GND. GPIO1_x, SWDEN at V_{L1} or GND. GPIO2_x at V_{L2} or GND. $\overline{RESET}$/POK pull-up to 3.3V. Typical values are at V_{24} = 24V, V_{L1} = V_{L2} = 3.3V, V_{5LIN} = V_5 = V_{5A} = 5V, V_{18LIN} = V_{18} = 1.8V, and T_A = +25°C (See Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for Repeated Start	$t_{SU:STA}$		0.25			µs
Hold Time for Repeated Start	$t_{HD:STA}$		0.25			µs
Low Period of SCL Clock	t_{LOW}		0.35			µs
High Period of SCL Clock	t_{HIGH}		0.25			µs
Data Hold Time	$t_{HD:DAT}$	(See Note 14, Note 15)	0		0.4	µs
Data Setup Time	$t_{SU:DAT}$	(See Note 14, Note 15)	80			ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Width Suppressed by Input Filter	t_{SP}	(See Note 16)			50	ns

Note 2: All devices are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed by design.

Note 3: The C/Q driver is disabled when V_{24} falls below the undervoltage error threshold ($V_{24\_ERR\_R}$, $V_{24\_ERR\_F}$).

Note 4: The undervoltage rising threshold is guaranteed to be higher than the undervoltage falling threshold.

Note 5: The microcontroller is halted when all of the internal peripherals are disabled. The internal clock is on and switching when the microcontroller is halted.

Note 6: MCLK performance degrades when V_{L2} < 2.5V.

Note 7: The 18MHz raw oscillator should not be used for clocking when using IO-Link communication.

Note 8: Not production tested. Guaranteed by design.

Note 9: Resistance can be adjusted to within 1LSB of the typical value using the recommended numerical correction. For more details, request the MAX22522 user guide.

Note 10: The SCLK period is a function of the CLK_DIV bits setting in the SPI1_SCLK_CONFIG0 register.

Note 11: The $\overline{CS}$ to SCLK time is a function of the CS_SETTLE_TIM bits setting in the SPI1_SCLK_CONFIG0 register.

Note 12: t_{SYS} is based on the microcontroller's HCLK. For more details, see the Clock Control section.

Note 13: The SCL clock frequency, f_{SCL}, must meet the minimum clock low time plus the rise/fall times.

Note 14: The maximum data hold time, t_{HD_DAT}, has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 15: This device internally provides a hold time of at least 100ns for the SDA signal (see the minimum VIH of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 16: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Timing Diagrams

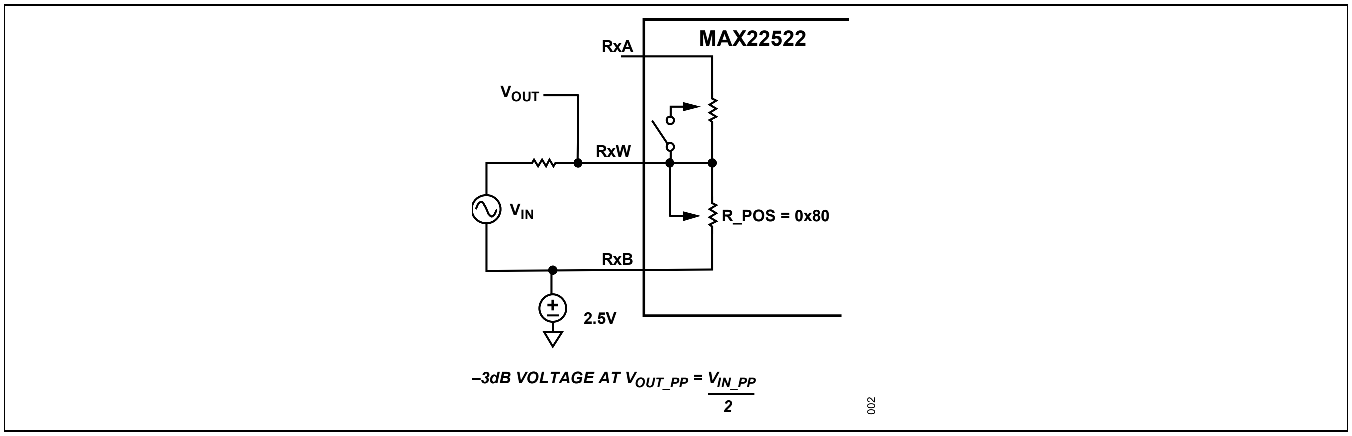


Figure 1. R1, R2 Bandwidth Measurement Circuit

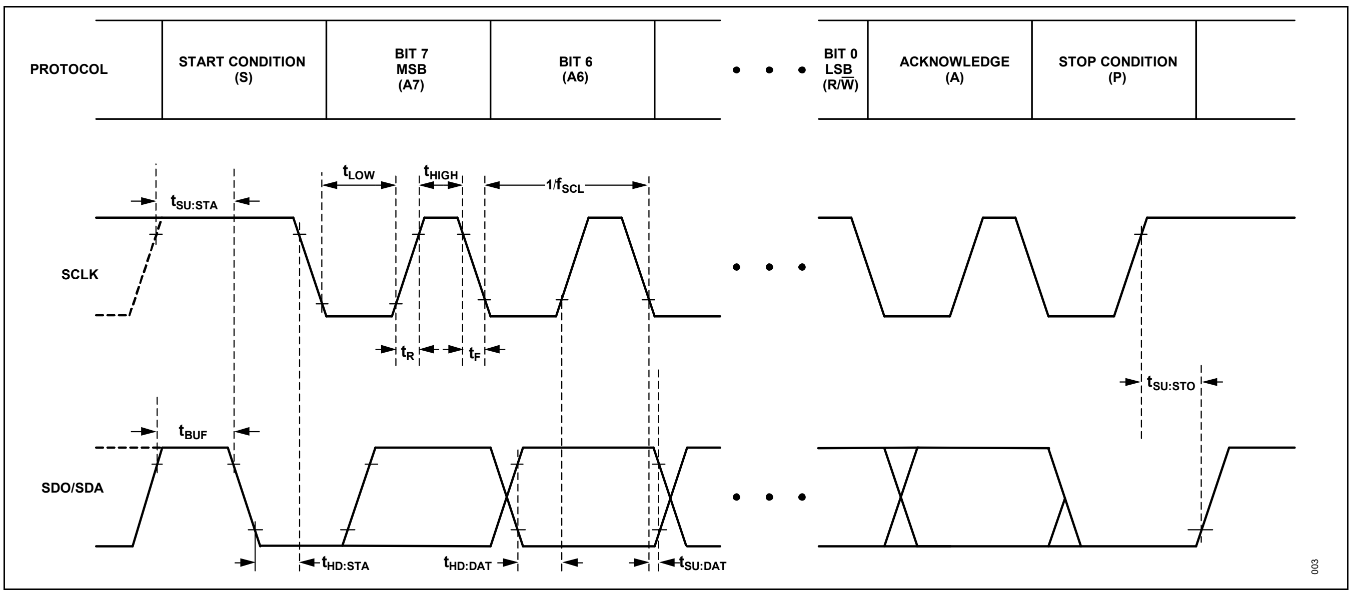


Figure 2. I²C Timing Diagram

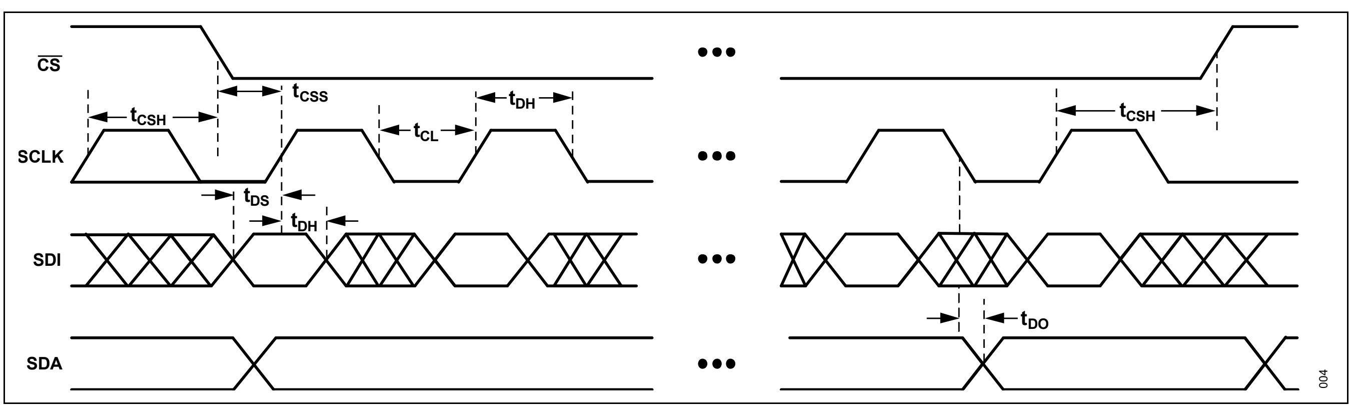
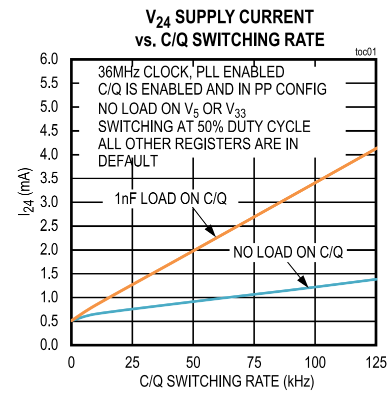
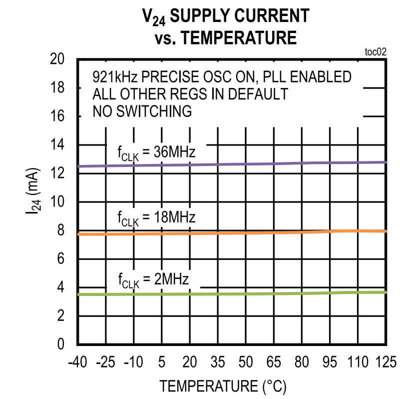


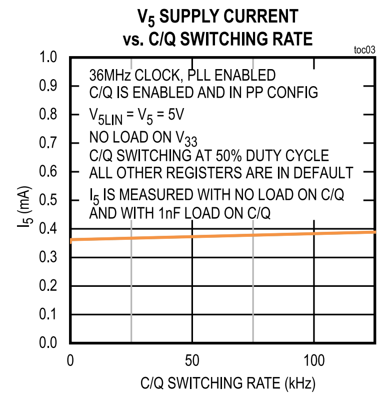
Figure 3. SPI Timing Diagram

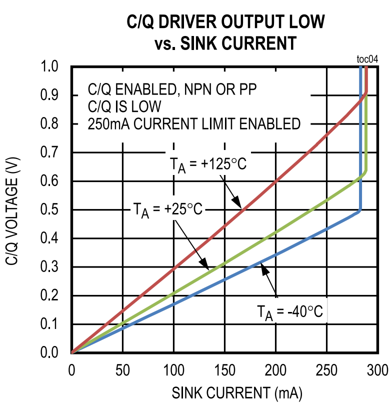
Typical Operating Characteristics

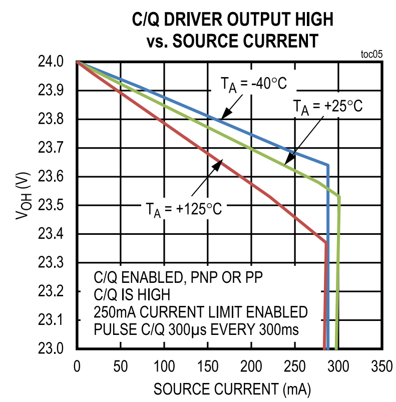
V_{24} = 24V, V_{5LIN} = PV24, V_{18LIN} = V33, V_{L1} = V_{L2} = V_{33}, 36MHz clock, T_A = 25°C, unless otherwise noted.

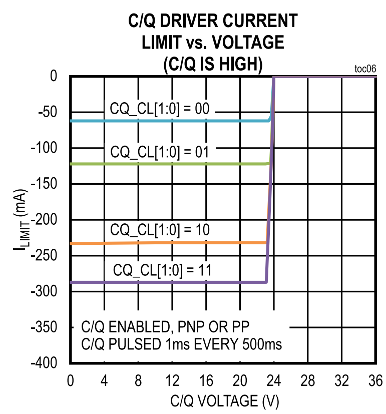


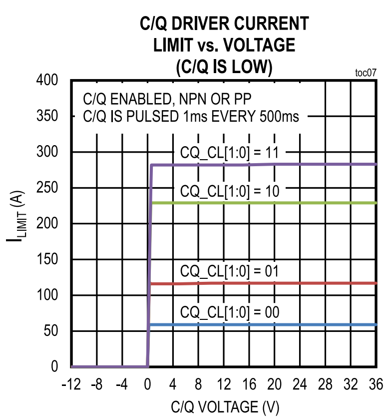


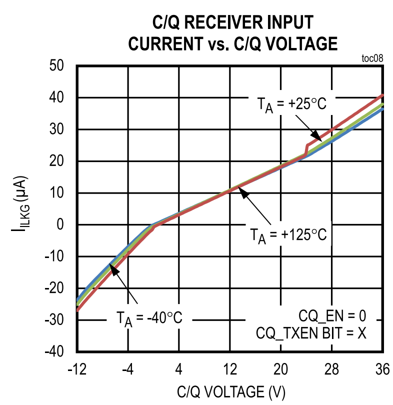


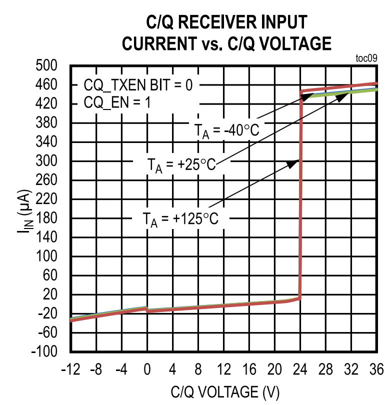






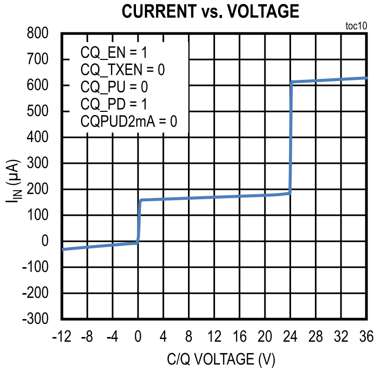




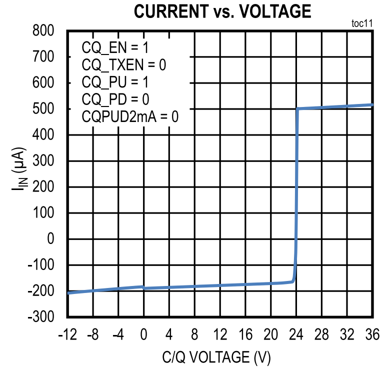


V_{24} = 24V, V_{5LIN} = PV24, V_{18LIN} = V33, V_{L1} = V_{L2} = V_{33}, 36MHz clock, T_A = 25°C, unless otherwise noted.

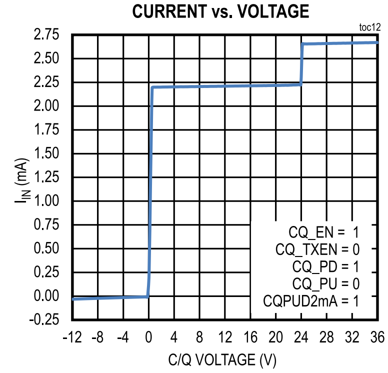
C/Q WEAK PULL-DOWN CURRENT vs. VOLTAGE



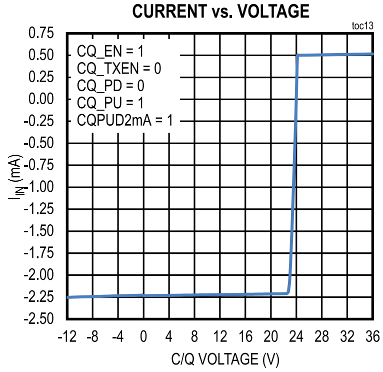
C/Q WEAK PULL-UP CURRENT vs. VOLTAGE



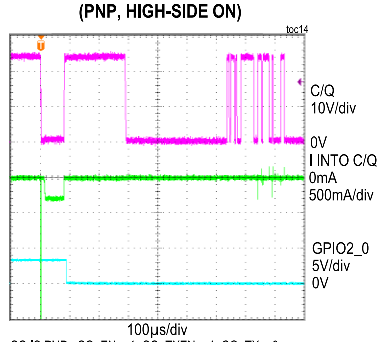
C/Q 2mA PULL-DOWN CURRENT vs. VOLTAGE



C/Q 2mA PULL-UP CURRENT vs. VOLTAGE

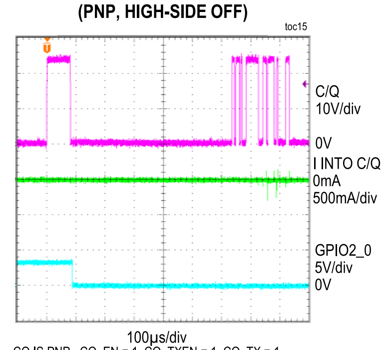


WAKE-UP DETECTION (PNP, HIGH-SIDE ON)



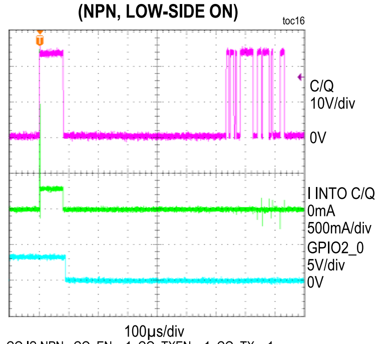
CQ IS PNP, CQ_EN = 1, CQ_TXEN = 1, CQ_TX = 0
COM3 DATA RATE, 250mA CURRENT LIMIT
GPIO2_0 ASSERTS LOW WHEN WU_INT = 1

WAKE-UP DETECTION (PNP, HIGH-SIDE OFF)



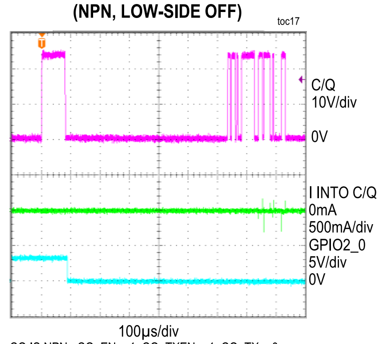
CQ IS PNP, CQ_EN = 1, CQ_TXEN = 1, CQ_TX = 1
COM3 DATA RATE, 250mA CURRENT LIMIT
GPIO2_0 ASSERTS LOW WHEN WU_INT = 1

WAKE-UP DETECTION (NPN, LOW-SIDE ON)



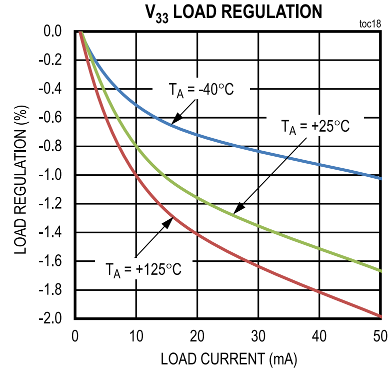
CQ IS NPN, CQ_EN = 1, CQ_TXEN = 1, CQ_TX = 1
COM3 DATA RATE, 250mA CURRENT LIMIT
GPIO2_0 ASSERTS LOW WHEN WU_INT = 1

WAKE-UP DETECTION (NPN, LOW-SIDE OFF)



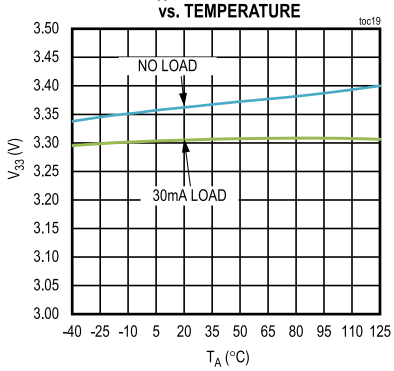
CQ IS NPN, CQ_EN = 1, CQ_TXEN = 1, CQ_TX = 0
COM3 DATA RATE, 250mA CURRENT LIMIT
GPIO2_0 ASSERTS LOW WHEN WU_INT = 1

V_{33} LOAD REGULATION

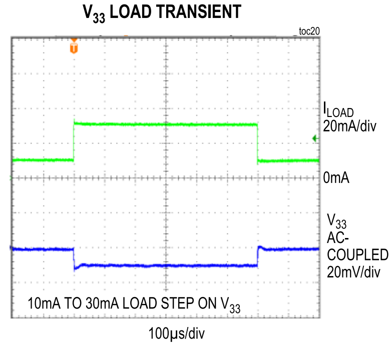


V_{24} = 24V, V_{5LIN} = PV24, V_{18LIN} = V33, V_{L1} = V_{L2} = V_{33}, 36MHz clock, T_A = 25°C, unless otherwise noted.

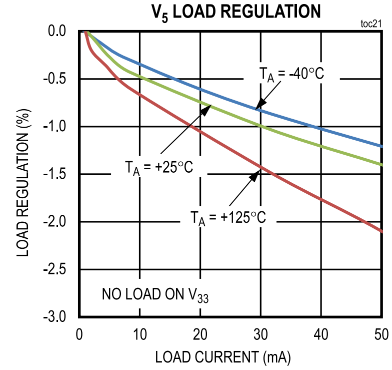
V_{33} OUTPUT VOLTAGE vs. TEMPERATURE



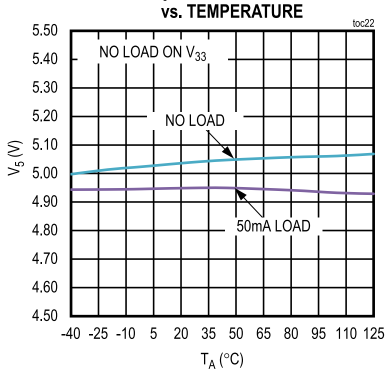
V_{33} LOAD TRANSIENT



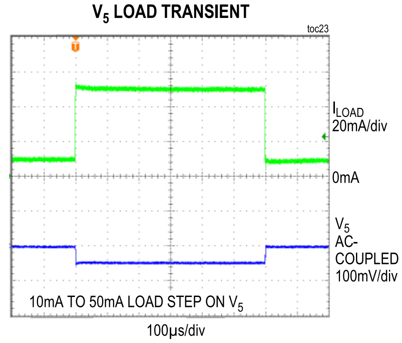
V_5 LOAD REGULATION



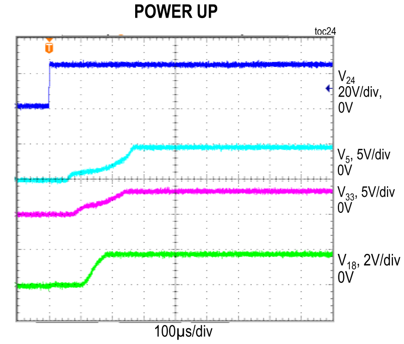
V_5 OUTPUT VOLTAGE vs. TEMPERATURE



V_5 LOAD TRANSIENT

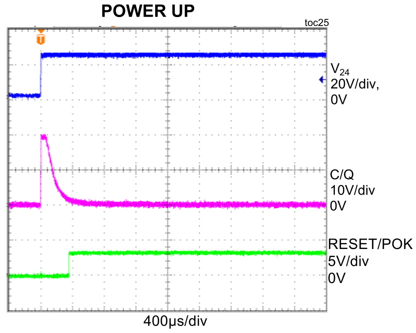


POWER UP



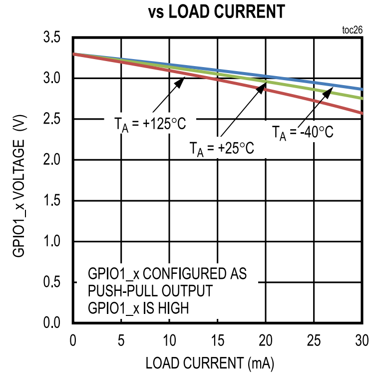
ALL REGISTERS ARE IN DEFAULT STATE

POWER UP

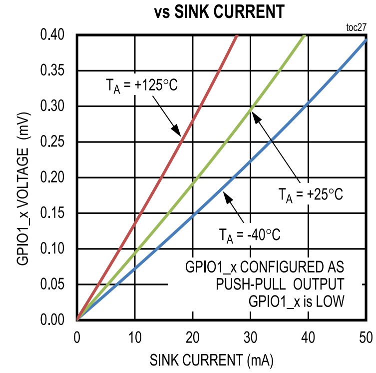


ALL REGISTERS IN DEFAULT STATE
RESET/POK PULLED UP TO V_{33} WITH 10kΩ

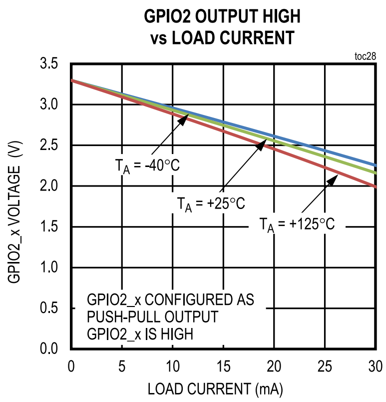
GPIO1 OUTPUT HIGH vs LOAD CURRENT

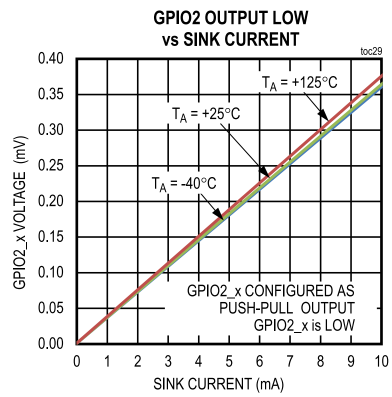


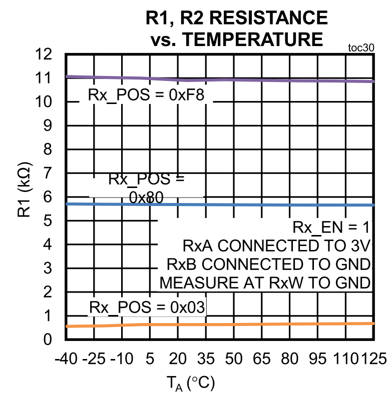
GPIO1 OUTPUT LOW vs SINK CURRENT

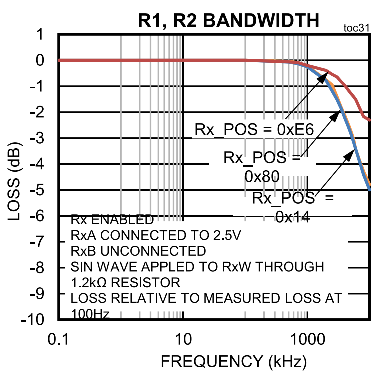


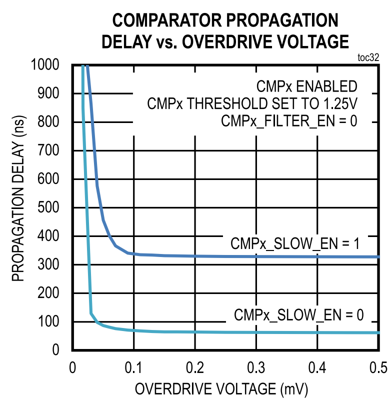
V_{24} = 24V, V_{5LIN} = PV24, V_{18LIN} = V33, V_{L1} = V_{L2} = V_{33}, 36MHz clock, T_A = 25°C, unless otherwise noted.

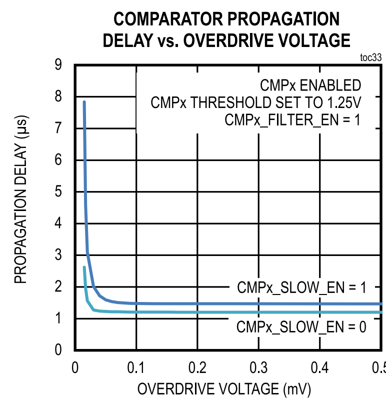


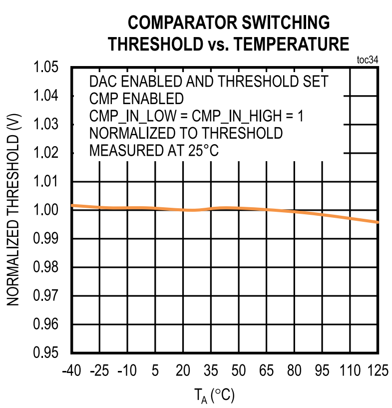


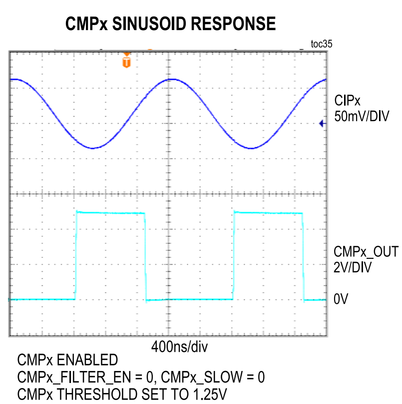


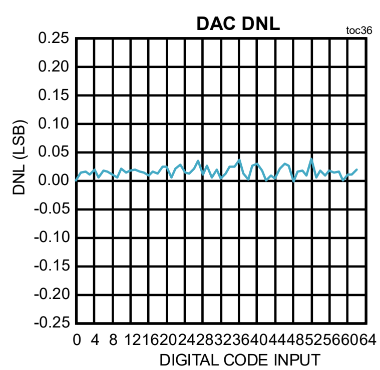




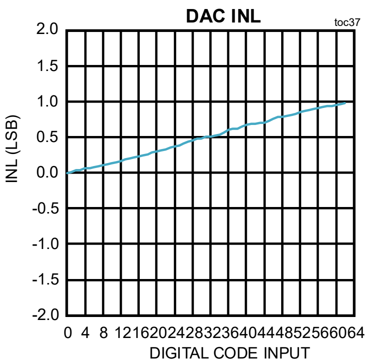


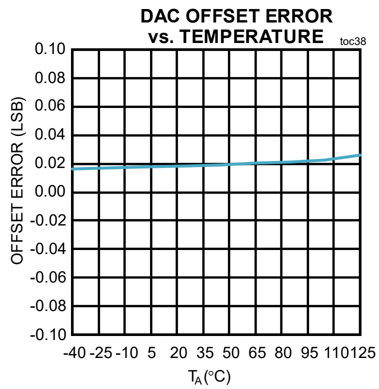


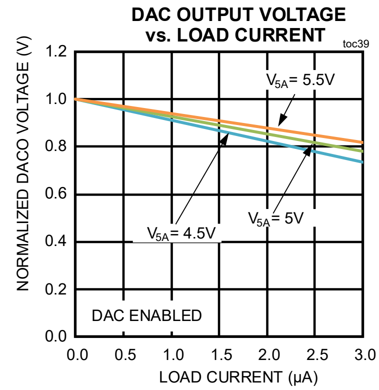


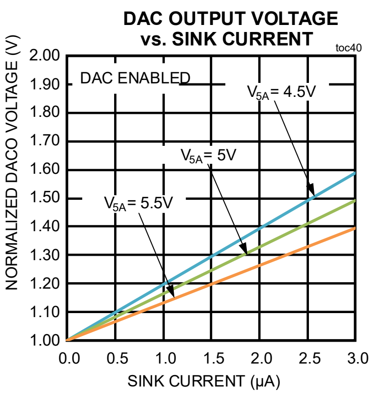


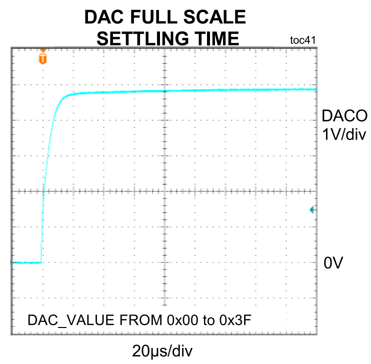
V_{24} = 24V, V_{5LIN} = PV24, V_{18LIN} = V33, V_{L1} = V_{L2} = V_{33}, 36MHz clock, T_A = 25°C, unless otherwise noted.

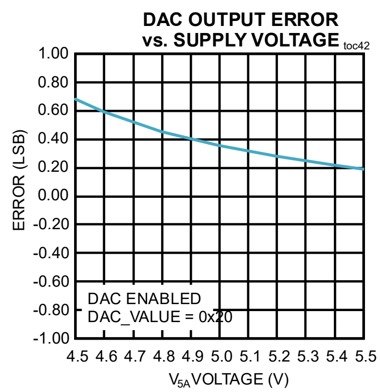


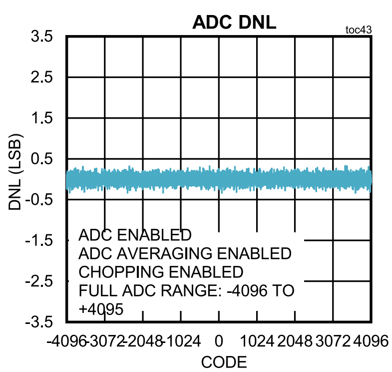


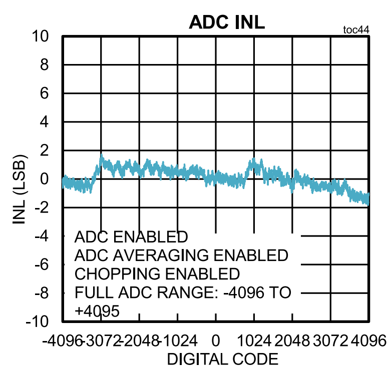


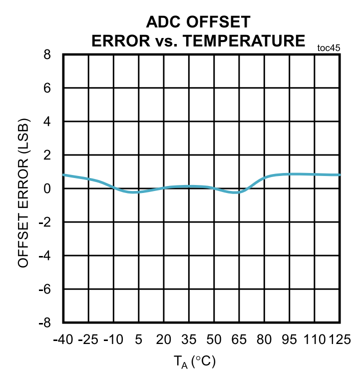




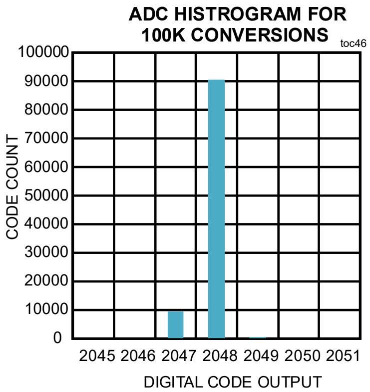


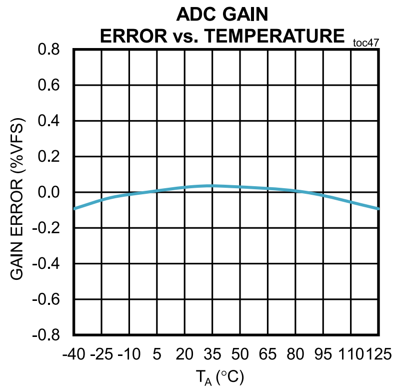






V_{24} = 24V, V_{5LIN} = PV24, V_{18LIN} = V33, V_{L1} = V_{L2} = V_{33}, 36MHz clock, T_A = 25°C, unless otherwise noted.





Pin Configurations

MAX22522
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10
A	GND	ADP	ADN	CMPO	GPIO2_4	GPIO2_2	SWCLK/ SCL	SWDIO/ SDA	GPIO2_0	IOLGND
B	CIP	CIN	DACO	VL2	GPIO2_3	GPIO2_1	SWDEN	VL1	LED2	IOLGND
C	R3A	R2W	R2B	DGND	GPIO1_6	GPIO1_5	GPIO1_4	GPIO1_0	LED1	C/Q
D	R2A	R1W	R1B	GND	GND	GND	IOLGND	V5ISNS	V24	V24
E	R1A	AGND	V5A	AGND	GPIO1_3	GPIO1_2	V33	V18LIN	V5LIN	PV24
F	GND	R4A	OGND	ORES	GPIO1_1	$\overline{\text{RESET}}$/ POK	V18	V5	V5BASE	PV24

WLP
(4.418mm x 2.638mm)

Pin Descriptions

PIN	NAME	FUNCTION
POWER		
D9, D10	V_{24}	Supply Voltage Input. Connect V_{24} to the L+ terminal of the IO-Link connector, or to an external supply. Bypass V_{24} to GND with a 10nF (typ) capacitor as close to the device as possible.
E10, F10	PV24	Active Diode Output. Bypass PV24 with external 1µF (typ) capacitor as close to the device as possible.
E9	V_{5LIN}	5V Linear Regulator Input. Connect V_{5LIN} to PV24 or to an external supply between 6V and 36V. Bypass V_{5LIN} to GND with a 1µF (typ) capacitor. Connect V_{5LIN} to V_5 to disable the 5V linear regulator. V_5 must be connected to an external 5V supply, when the regulator is disabled.
D8	V_{5ISNS}	5V Linear Regulator Current Sense Input. Connect the collector of the transistor to V_{5ISNS} when an external NPN is used. Leave V_{ISNS} unconnected when not using an external NPN. For more details, see the *V5 Linear Regulator* section.
F9	V_{5BASE}	5V Linear Regulator Output. Connect the base of the transistor to V_{5BASE} when an external NPN is used. Connect V_{5BASE} directly to V_5 when an external NPN is not used. For more details, see the *V5 Linear Regulator* section.
F8	V_5	5V Supply Input/5V Linear Regulator Feedback Input. Bypass V_5 to GND with a 2.2µF (typ) capacitor as close to the device as possible when not using an external NPN. Bypass V5 to GND with a 4.7µF (min) capacitor when using an external NPN. For more details, see the *V5 Linear Regulator* section.
E8	V_{18LIN}	1.8V Linear Regulator Input. Connect V_{18LIN} to V_{33} or to external power supply from 2.7V to 5.5V. Bypass V_{18LIN} to GND with a 1µF (typ) capacitor as close to the device as possible. Connect V_{18LIN} to V_{18} to disable the 1.8V linear regulator.
F7	V_{18}	1.8V Supply Input/Linear Regulator Output. Bypass V_{18} to GND with a 2.2µF (typ) capacitor as close to the device as possible. Connect V_{18} to V_{18LIN} to disable the 1.8V linear regulator. Connect an external 1.8V to V_{18} when the regulator is disabled.
E7	V_{33}	3.3V Linear Regulator Output. Bypass V_{33} to GND 2.2µF (typ) capacitor as close to the device as possible.
E3	V_{5A}	5V Analog Supply Input. Bypass V_{5A} to GND with a 100nF (typ) capacitor as close to the device as possible. Connect a 5V supply to V_{5A}.
E2, E4	AGND	Analog Ground. For more details, see the *Layout and Grounding* section.
B8	V_{L1}	Logic I/O Bank 1 Supply Input. Bypass V_{L1} to GND with a 100nF (typ) capacitor as close to the device as possible. Connect V_{L1} to a power supply from 2.2V to 5.5V.
B4	V_{L2}	Logic I/O Bank 2 Supply Input. X. Bypass V_{L2} to GND with a 100nF (typ) capacitor to GND as close to the device as possible. Connect V_{L2} to a supply from 1.65V to 5.5V.
C4	DGND	Digital Ground. For more details, see the *Layout and Grounding* section.

A1, D4, D5, D6, F1	GND	Ground. For more details, see the Layout and Grounding section.
24V INTERFACE		
C10	C/Q	IO-Link Transceiver Input/Output. C/Q is used for IO-Link communication.
A10, B10, D7	IOLGND	IO-Link Power Ground. For more details, see the Layout and Grounding section.
921kHz PRECISION OSCILLATOR		
F4	ORES	921kHz Precision Oscillator Resistor. Connect a high accuracy (±0.1%) 10kΩ resistor between ORES and OGND.
F3	OGND	Internal Oscillator Ground. For more details, see the Layout and Grounding section.
LEDs (LED1, LED2) AND $\overline{\text{RESET}}$/POK		
C9	LED1	Open-drain LED Output 1.
B9	LED2	Open-drain LED Output 2.
F6	$\overline{\text{RESET}}$/POK	Dual Function Active-Low Reset Input and Open-Drain Power-OK (POK) Output. $\overline{\text{RESET}}$/POK asserts low when V_5 or V_{18} fall below their undervoltage lockout (UVLO) threshold. $\overline{\text{RESET}}$/POK asserts high after V_5 and V_{18} exceed their UVLO thresholds. Drive $\overline{\text{RESET}}$/POK low to reset the device. Connect $\overline{\text{RESET}}$/POK to V_{L1} or V_{L2} through a 10kΩ resistor.
VARIABLE RESISTORS (R1, R2, R3, R4)		
E1	R1A	R1 Variable Resistor Side A.
D3	R1B	R1 Variable Resistor Side B.
D2	R1W	R1 Variable Resistor Wiper.
D1	R2A	R2 Variable Resistor Side A.
C3	R2B	R2 Variable Resistor Side B.
C2	R2W	R2 Variable Resistor Wiper.
C1	R3A	R3 Variable Resistor.
F2	R4A	R4 Variable Resistor.
COMPARATOR AND DAC		
A4	CMPO	Comparator Output.
B1	CIP	Comparator Positive Input.
B3	DACO	DAC Output.
B2	CIN	Comparator Negative Input.
ADC		
A2	ADP	ADC Positive Input.
A3	ADN	ADC Negative Input.
BANK1 GPIOs (GPIO1_0 – GPIO1_6)		
C8	GPIO1_0	Bank 1 GPIO 0. GPIO1_0 can be configured as a digital input, digital output, or as an interrupt input (IRQ0). For more details, see the General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) section.
F5	GPIO1_1	Bank 1 GPIO 1. GPIO1_1 can be configured as a digital input, digital output, or as the SCL output of the I^2C host controller. For more details, see the General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) section.
E6	GPIO1_2	Bank 1 GPIO 2. GPIO1_2 can be configured as a digital input, digital output, or as the SDA signal of the I^2C host controller. For more details, see the General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) section.
E5	GPIO1_3	Bank 1 GPIO 3. GPIO1_3 can be configured as a digital input, digital output, an ADC input, a PWM output, or to indicate a PDOUT bit (PDOUT2). For more details, see the General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) section.
C7	GPIO1_4	Bank 1 GPIO 4. GPIO1_4 can be configured as a digital input, digital output, an ADC input, or as a logic input for the PDIN data (PDIN2). For more details, see the General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) section.

C6	GPIO1_5	Bank 1 GPIO 5. GPIO1_5 can be configured as a digital input, digital output, an ADC input, or as a logic input for the PDIN data (PDIN1). For more details, see the General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) section.
C5	GPIO1_6	Bank 1 GPIO 6. GPIO1_6 can be configured as a digital input, digital output, an ADC input, a PWM output, or to indicate a PDOUT bit (PDOUT1). For more details, see the General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) section.
BANK2 GPIOs (GPIO2_0 – GPIO2_4)		
A9	GPIO2_0	Bank 2 GPIO 0. GPIO2_0 can be configured as a digital input, digital output, an interrupt input (IRQ1), an external clock input (MLCK), or as an active-low chip select (CS1) output when bank 2 GPIOs are configured as an SPI host controller. For more details, see the General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) section. When configured as an MCLK input, connect an external clock from 1.843MHz to 14.74MHz to GPIO2_0. Request the User Guide for more information.
B6	GPIO2_1	Bank 2 GPIO 1. GPIO2_1 can be configured as a digital input, digital output, or as an active-low chip select (CS0) output when bank 2 GPIOs are configured as an SPI host controller. For more details, see the General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) section.
A6	GPIO2_2	Bank 2 GPIO 2. GPIO2_2 can be configured as a digital input, digital output, or as the SCLK clock output when bank 2 GPIOs are configured as an SPI host controller. For more details, see the General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) section.
B5	GPIO2_3	Bank 2 GPIO 3. GPIO2_3 can be configured as a digital input, digital output, or as a serial data MISO when bank 2 GPIOs are configured as an SPI host controller. For more details, see the General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) section.
A5	GPIO2_4	Bank 2 GPIO 3. GPIO2_3 can be configured as a digital input, digital output, or as a serial data MOSI when bank 2 GPIOs are configured as an SPI host controller. For more details, see the General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x) section.
SWD DEBUG INTERFACE (SWEN, SWD, SWSCL)		
B7	SWDEN	SWD or I²C Debug Interface Enable. Drive SWDEN high to enable the SWD debug interface. Drive SWDEN low to enable the I²C debug interface. For more details, request the MAX22522 the user guide.
A7	SWCLK/SCL	Debug Interface Clock Input. SWCLK/SCL is the serial debug clock input when SWDEN is high (SWD interface is enabled). SWCLK/SCL is the I²C SCL clock input if SWDEN is low. For more details, request the MAX22522 the user guide.
A8	SWDIO/SDA	Debug Interface Data Line. SWDIO/SDA is the serial debug data line when SWDEN is high. SWDIO/SDA is the I²C SDA data line when SWDEN is low. For more details, request the MAX22522 the user guide.

Detailed Description

Power

The MAX22522 requires three supplies for normal operation: a 24V supply (V_{24}) for IO-Link communication, a 5V supply (V_5 and V_{5A}) to power the integrated analog components, and a 1.8V supply (V_{18}). The Cortex-M0, analog peripherals, and internal oscillators are powered from the V_5 and V_{18} supplies.

An internal active diode provides a protected supply output, PV24. PV24 can drive loads up to 100mA (typ).

Additionally, three linear regulators (5V, 3.3V, and 1.8V) allow for a flexible supply structure from the V_{24} supply.

Power-Up Sequencing

The MAX22522 initially uses an internal supply and reference circuitry to turn-on the linear regulators and active diode for PV24 when the V_{24} supply rises. When the V_{18} and V_5 voltages exceed their respective undervoltage lockout (UVLO) thresholds, the internal 18MHz raw oscillator is enabled. Once the internal supplies and the oscillator are stabilized, the MAX22522 drives $\overline{\text{RESET}}$/POK high and the Cortex-M0 begins its boot-up sequence.

If the V_{18} or V_5 voltage falls below the UVLO threshold at any time during power-up, the start-up procedure is restarted.

PV24 Protected Supply

The MAX22522 generates a reverse-voltage protected and hot-plug safe supply from V_{24}, PV24. PV24 powers on at a controlled rate and can support capacitive loads up to 1µF (typ). PV24 can drive loads up to 100mA (typ) during normal operation.

Connect PV24 to V_{5LIN} to power the 5V and 3.3V linear regulators. If V_{18LIN} = V_{33}, then PV24 also powers the 1.8V linear regulator. Optionally, PV24 can be connected to the input of an external regulator, as shown in *Figure 4*.

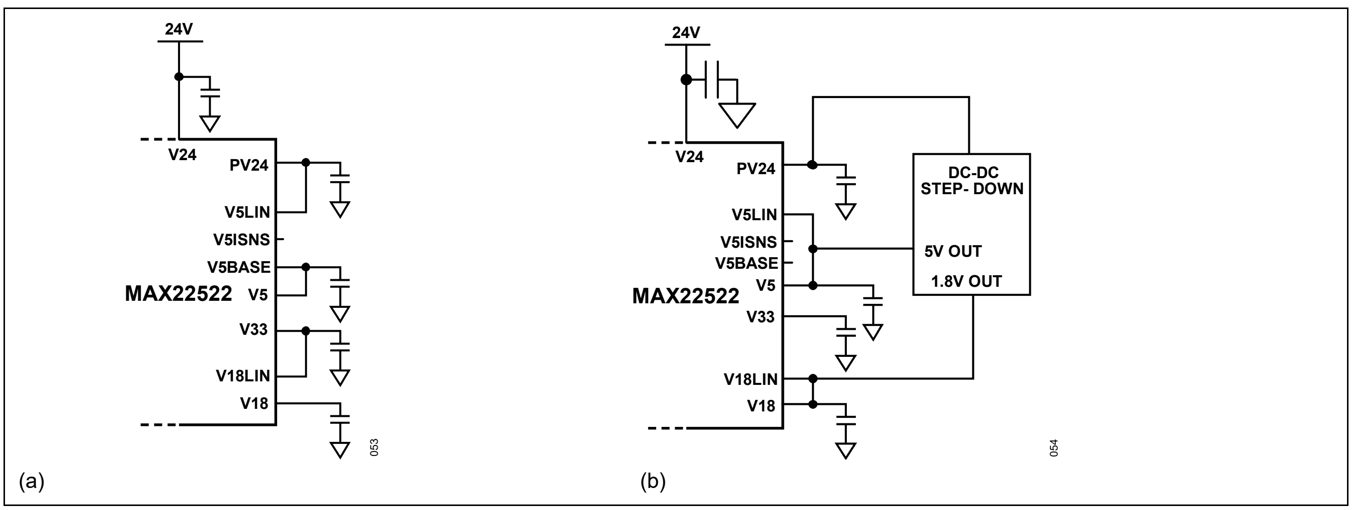


Figure 4. PV24 Power Scheme (a) PV24 Powered Directly with Internal Regulators (b) PV24 Powered by External DC-DC Regulator

V_5 Linear Regulator

The V_5 regulator is capable of driving external loads up to 50mA (typ), including device and V_{33} LDO current consumption. To drive larger loads, or to reduce power dissipation within the MAX22522, use an external pass transistor to generate the required 5V.

Bypass V_5 to GND with a 4.7µF (min) capacitor when using an external transistor. Connect V_{5BASE} to the base of the transistor to regulate the voltage and connect V_5 to the emitter. Additionally, connect a 4.7kΩ resistor between V_{5BASE} and the emitter of the transistor when using the is configuration. For more details, see *Figure 5*.

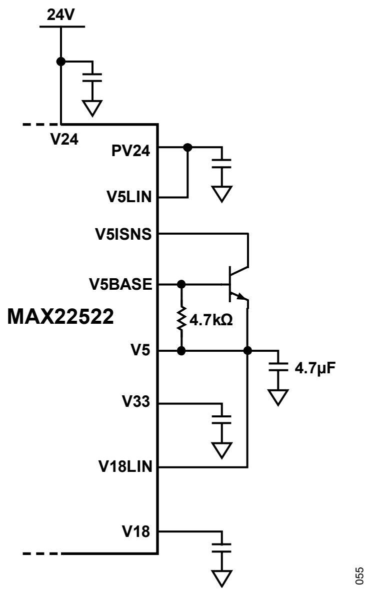


Figure 5. V_5 Regulator Configuration with an External NPN Transistor

Connect V_{5LIN} to V_5 and connect V_5 to an external supply to disable the internal V_5 linear regulator. V_5 is the supply input for the internal analog and digital functions and must be supplied externally when the linear regulator is disabled. Ensure that V_5 is present for normal operation.

V_{33} Linear Regulator

The V_{33} linear regulator is powered from V_5 and can drive loads up to 50mA (typ). Bypass V_{33} to ground with at least 2.2µF (typ) for normal operation.

V_{18} Linear Regulator

The V_{18} regulator is capable of driving external loads up to 50mA (typ). Connect V_{18LIN} to V_{33}, V_5, or to an external supply from 2.7V to 5.5V to power the 1.8V internal regulator. Bypass V_{18} to ground with at least 2.2µF (typ) for normal operation.

Connect V_{18LIN} to V_{18} to disable the internal 1.8V linear regulator. Connect an external 1.8V supply to V_{18} when the internal regulator is disabled. Ensure that V_{18} is present for normal operation.

24V Interface (V_{24}, C/Q, IOLGND)

The MAX22522 features an IO-Link transceiver interface capable of operating with voltages up to 36V. This industrial standard interface includes the C/Q input/output, the V_{24} supply, and the IO-Link ground (IOLGND).

The C/Q switching driver is programmable for high-side (PNP), low-side (NPN), or push-pull (PP) functionality, and operates over all of the COM1, COM2, and COM3 IO-Link data rates. Additionally, C/Q features a programmable current limit (50mA to 250mA), programmable rising and falling slew rates, and an integrated 2mA pull-up/pull-down that can be enabled/disabled.

Variable Resistors (R1, R2)

The MAX22522 features two low-capacitance variable resistors, R1 and R2, that can be used in either potentiometer or rheostat modes. The 8-bit data in the R1 and R2 registers is decoded to one of 256 resistance settings each for R1 and R2.

R1 and R2 have an end-to-end impedance of 10kΩ (typ) and operate up to 5V. Ensure that the current into R1 and R2 does not exceed 2mA.

Variable Resistors (R3, R4)

The MAX22522 features two variable resistors, R3 and R4, that are referenced to ground.

The 6-bit data in the R3 register is decoded to one of 64 settings for the R3 resistor. Resistance is linearly distributed between 1LSB to 63LSB. R3 has an end-to-end impedance of 60kΩ and is capable of operating up to 5V. Ensure that the current into R3A does not exceed 2mA. A code of 0x00 in the R3 register disables the variable resistor.

The 8-bit data in the R4 register is decoded to one of 256 settings for the R4 resistor. Resistance is linearly distributed between 1LSB to 255LSB. R4 has an end-to-end impedance of 10kΩ and is capable of operating up to 5V. Ensure that the current into R4A does not exceed 2mA.

General-Purpose Inputs/Outputs (GPIO1_x, GPIO2_x)

The MAX22522 integrates 12 GPIO pins divided into two groups, or banks: Bank 1 and Bank 2. Bank 1 includes seven GPIOs (GPIO1_0 to GPIO1_6) powered by V_{L1}. Bank 2 includes five GPIOs (GPIO2_0 to GPIO2_4) powered by V_{L2}.

All GPIOs can be configured as outputs (open-drain or push-pull) or inputs, and feature pull-up/-downs that can be enabled or disabled. Additionally, each GPIO can be programmed with an individual alternate functionality.

Figure 6 shows the GPIO pin logic. This logic applies to all GPIO pins in both Bank 1 and Bank 2.

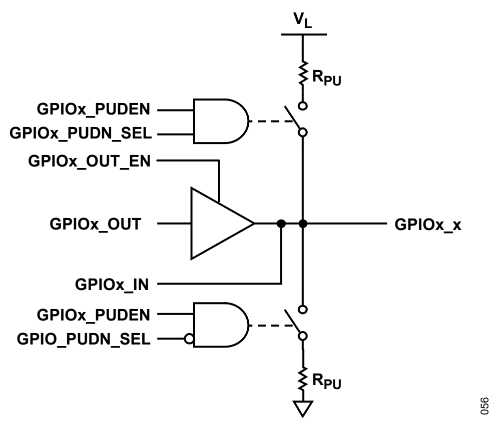


Figure 6. GPIO Logic Circuit

GPIO Alternate Functions

All GPIOs in Bank 1 and Bank 2 are configurable as standard I/Os. Additionally, each GPIO can be configured for specialized, or alternate functionality. Alternate functions are enabled by setting bits in the GPIO1_ALT_FUNC and/or GPIO2_ALT_FUNC registers.

Table 1 shows the alternate functions for each GPIO in Bank 1. *Table 2* shows the alternate functions for each GPIO in Bank 2. Alternate functions automatically set the direction and output value of a given GPIO.

Table 1. Bank 1 GPIO Alternate Functions

BANK 1 GPIO	ALTERNATE FUNCTION	DESCRIPTION
GPIO1_0	IRQ0	IRQ0 input.
GPIO1_1	SCL	I^2C clock line when configured as I^2C host controller.
GPIO1_2	SDA	I^2C data line when configured as I^2C host controller.
GPIO1_3	PWM(1)	PWM output.
	PDOUT2(2)	PDOut bit. For more details, refer to the MAX22522 user guide.
GPIO1_4	PDIN2	PDIn bit. For more details, refer to the MAX22522 user guide.
GPIO1_5	PDIN1	PDIn bit. For more details, refer to the MAX22522 user guide.
GPIO1_6	PDOUT1	PDOut bit. For more details, refer to the MAX22522 user guide.

(#) This is the level of precedence assigned to the bit when multiple alternate functions are enabled simultaneously. For example, when both (1) and (2) functions are enabled in the register, the pin operates with the (1) function only.

Table 2. Bank 2 GPIO Alternate Functions

BANK1 GPIO	ALTERNATE FUNCTION	DESCRIPTION
GPIO2_0	IRQ1(1)	IRQ1 input.
	MCLK(2)	MCLK clock output.
	CS1	Chip select output 1 when configured for SPI host controller functionality. For more details, refer to the MAX22522 user guide.
GPIO2_1	CS0	Chip select output 0 when configured for SPI host controller functionality. For more details, refer to the MAX22522 user guide.
GPIO2_2	SCLK	SPI clock output when configured for SPI host controller functionality. For more details, refer to the MAX22522 user guide.
GPIO2_3	MISO	Serial data output when configured for SPI host controller functionality. For more details, refer to the MAX22522 user guide.
GPIO2_4	MOSI	Serial data input when configured for SPI host controller functionality. For more details, refer to the MAX22522 user guide.

(#) This is the level of precedence assigned to the bit when multiple alternate functions are enabled simultaneously. For example, when both (1) and (2) functions are enabled in the register, the pin operates with the (1) function only.

Note that the MAX22522 enables the first function in the table of each GPIO, when multiple functions are selected. For example, if both PWM and PDOUT2 are enabled for GPIO1_3, it operates as a PWM output.

Some alternate functions depend on other configurations and settings in other registers. For example, the MCLK function on GPIO2_0 is enabled and configured using the clock control register. This functionality also disables any other functions for this GPIO. For more details, refer to theMAX22522 user guide and Register Table.

High Speed Comparator and DAC (CMP, DAC)

The MAX22522 features a high speed, rail-to-rail, 5V tolerant comparator, CMP, and analog-to-digital converter (DAC). Enable and configure the comparator and DAC by writing to the CMP and DAC registers, as shown in the MAX22522 user guide and Register Table. CMP and DAC are powered by the V_{5A} supply and are referenced to AGND.

Analog-to-Digital Converter (ADC)

The MAX22522 features an integrated 13-bit (12-bit-plus-sign) SAR ADC. The ADC can directly sample signals on the ADP and ADN pins, GPIO1_3 to GPIO1_6 I/Os, an internal reference, or an internal PTAT thermal sensor using an internal buffer (*Figure 7*).

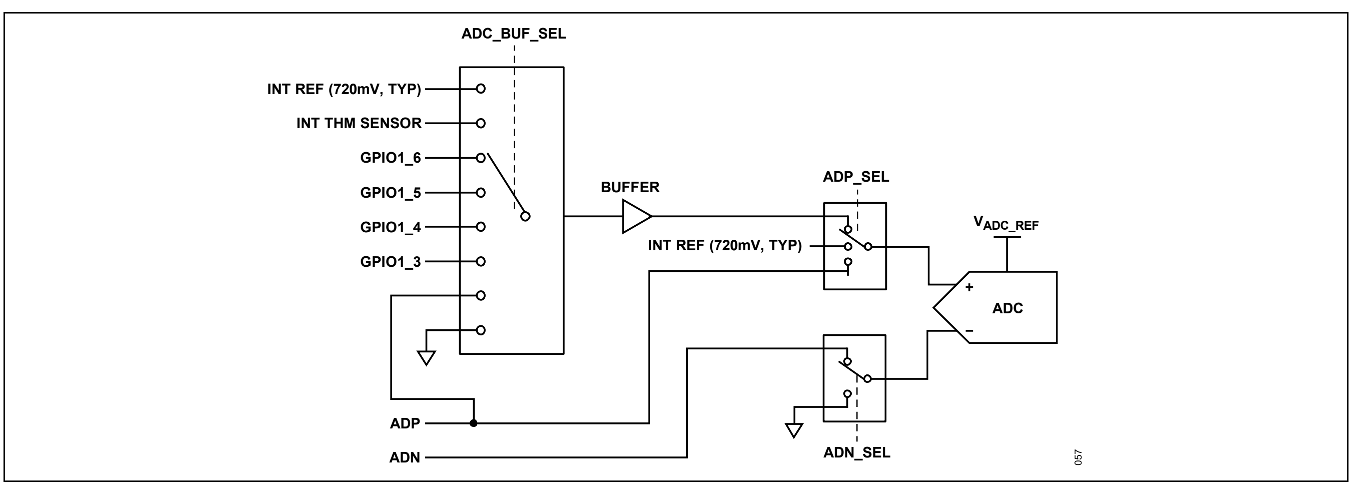


Figure 7. ADC Input Structure

The ADC and ADC buffer input are powered by the V_{5A} supply. The ADC is referenced to the internal 1.25V (typ) V_{ADC_REF} voltage. Ensure that the voltages on the ADC inputs do not exceed the *Absolute Maximum Ratings* for each pin. ADP and ADN analog inputs can range from 0V to 1.8V (typ) references to DGND, however signal inputs at the multiplexer have a 5V tolerance.

Clock Control

The MAX22522 can generate all of the required clock references internally. An internal 18MHz (typ) raw oscillator is implemented for power-up and watchdog functions. An internal 921.6kHz precise oscillator is available after power-up for IO-Link communication. An external clock may be connected by configuring GPIO2_0 as the MCLK input. See *Figure 8*.

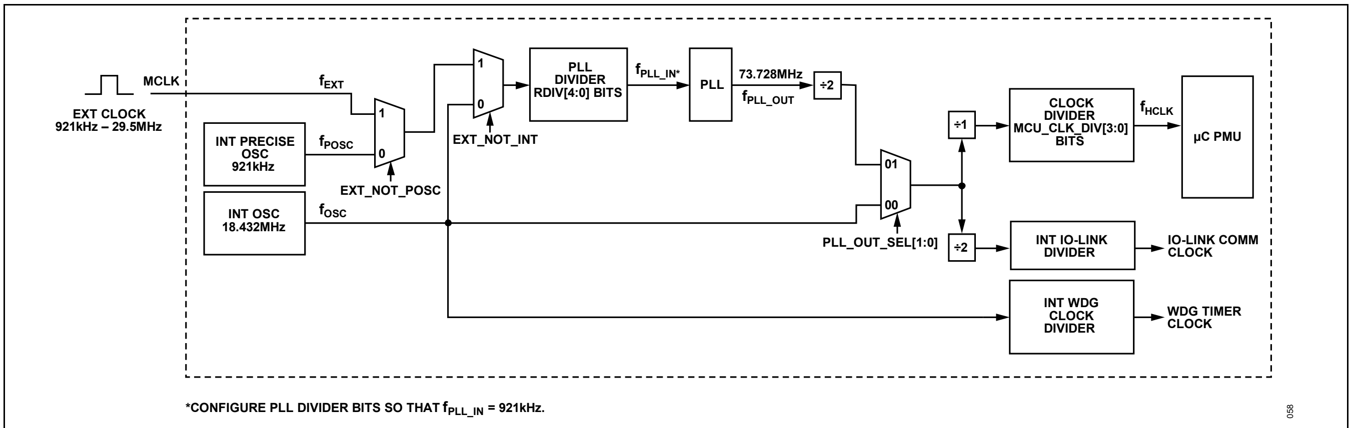


Figure 8. Clock Configuration

The clock control configuration registers should be programmed as soon as the initialization sequence is complete, as shown in the Register Map and MAX22522 user guide, as part of the application program.

Timers and System Watchdog

The MAX22522 features a system watchdog counter, a standard Cortex-M0 SysTick timer, and an additional enhanced timer used to count external events or generate a PWM/TOGGLE output signal (single-cycle or continuous).

SysTick Timer

The MAX22522 includes a SysTick timer, standard in an ARM Cortex-M0. For more details on this timer, refer to the ARM website.

IO-Link Data Link Layer

The MAX22522 integrates a fully functional IO-Link device data link layer state machine capable of handling both cyclic and acyclic data transmission types, as shown in the IO-Link standard version 1.1.4.

SIO Mode

The transceiver is configured to operate in SIO mode when powered up, and following a hardware or software reset. In SIO mode, the C/Q driver is controlled bits in the TX_CTRL register. C/Q is configurable for low-side (NPN), high-side (PNP), or push-pull (PP) operation and features a programmable current limit and slew rate.

Wake-Up and Establish COM

The transceiver features an integrated IO-Link establish communication sequencer to autonomously manages the IO-Link communication sequence when a valid wake-up pulse is detected.

Process Data Transfers

Process Data Output (PDOut)

The MAX22522 features a process data out (PDOut) buffer architecture that supports up to 32-byte IO-Link PDOut data with buffering for reliable data transfer. The integrated IO-Link state machine autonomously executes the tasks supporting Process Data Output from the IO-Link master.

Process Data Input (PDIn)

The MAX22522 features a process data in (PDIn) buffer that supports up to 32-byte IO-Link PDIn data. The integrated IO-Link state machine manages all real-time tasks related to Process Data Input from the PDIn buffer to the IO-Link master.

ISDU Transmission

The integrated state machine manages the real-time tasks to support ISDU data transfer in both IN (that is, from the IO-Link device to the IO-Link master) and OUT (that is, from the IO-Link master to the device) directions. The MAX22522 integrates a 256-bytes ISDU buffer for both IN and OUT directions.

LED1, LED2: Status and Diagnostic Indicators

The MAX22522 integrates two open-drain outputs for controlling LEDs (LED1 and LED2). These pins can be used as indicators of active SDCI communication and are controlled by setting bits in the LED1CTRMSB, LED1CTRLSB, LED2CTRMSB, and LED2CTRLSB registers.

Applications Information

Power Dissipation and Thermal Considerations

Total power dissipation depends on the quiescent power generated in the device, the power dissipated in the C/Q driver, and the power generated by the internal linear regulators (V_5, V_{33}, and V_{18}). If other peripherals are not driving large loads, power dissipation for those can typically be neglected.

Total power dissipation for the device is calculated using the following equation:

$$P_{TOTAL} = P_{CQ} + P_{V24} + P_{PU} + P_{PD}$$

where P_{CQ} is the power dissipated in the C/Q driver, P_{V24} is the quiescent power dissipated by the device, and P_{PU} and P_{PD} are the power dissipated in the C/Q pull-up/pull-down current sources/sinks, respectively.

Ensure that the total power dissipation is less than the limits listed in the *Absolute Maximum Ratings* section.

When using the internal regulators (V_{5LIN} = PV24 and $V_{18LIN} = V_{33}$), use the following equations to calculate the power dissipation due to the C/Q driver:

$$P_{CQ} = [I_{CQ}(max)]^2 \times R_{ON}$$

where R_{ON} driver on-resistance.

Calculate the quiescent power dissipation in the device using the following equation:

$$P_{V24} = I_{24}(max) \times V_{24}(max)$$

If the 2mA current sinks/sources are enabled, calculate their associated power dissipation as:

$$P_{PD} = I_{PD}(max) \times V_{CQ}(max)$$

$$P_{PU} = I_{PU}(max) \times [V_{24} - V_{CQ}](max)$$

Note that most of the power is dissipated in the linear regulators. Calculate the power dissipated in the linear regulators as follows:

Assuming PV24 is used to power the V_5 linear regulator, calculate the power dissipation in the 5V linear regulator, V_5, using the following equation:

$$P_{V5} = (V_{24} - V_5) \times I_{V5\_LOAD}$$

where I_{V5_LOAD} includes the I_{V33_LOAD} current sourced from V_{33}.

When using an external source to supply V_5 ($V_{5LIN} = V_5$ = external 5V), the power dissipation for the V_5 regulator is calculated as $P_{V5} = V_5 \times I_{V5\_LOAD}$.

Calculate power dissipated in the 3.3V linear regulator, V_{33}, using the following equation:

$$P_{V33} = 1.7V \times I_{V33\_LOAD}$$

where I_{V33_LOAD} includes the I_{V18_LOAD} current sourced from V_{18}.

Assuming that $V_{18LIN} = V_{33}$, calculate the power dissipated in the 1.8V linear regulator, V_{18}, using the following equation:

$$P_{V18} = 1.5V \times I_{V18\_LOAD}$$

Alternately, when using an external source to supply V_{18} ($V_{18LIN} = V_{18}$ = external 1.8V), the power dissipation for the V_{18} regulator is calculated as $P_{V18} = V_{18} \times I_{V18\_LOAD}$.

EMC Protection

The MAX22522 features integrated surge protection of ±1.2kV/500Ω for 1.2µs/50µs surge on the V_{24}, C/Q, and IOLGND pins.

External TVS diodes are required to meet higher levels of surge and ESD protection. When using external TVS, ensure that the TVS diode peak clamping voltage is within the absolute maximum voltage ratings.

Layout and Grounding

Layout for the MAX22522 is important to ensure that all functions operate with minimal interference.

The MAX22522 features five ground pins: ground (GND), analog ground (AGND), digital ground (DGND), the precision oscillator return/ground (OGND), and IO-Link ground (IOLGND). For the best performance, use a star ground layout.

V_{24}, C/Q, and IOLGND pins are connected directly to the IO-Link connector. For EMC purposes, keep the IOLGND separated from other ground to ensure that all IO-Link and field-related currents return to IOLGND. Connect all bypass capacitors and other components from V_{24} and C/Q directly to the IOLGND. Connect the IOLGND to the GND ground layer at one point.

Bypass all supply pins for the IC (V_5, V_{33}, V_{18}, V_{L1}, V_{L2}, and PV24) to the GND pin and connect directly to a ground plane. Bypass capacitors must be placed as close to the IC as possible.

The V_{5A} supply, variable resistors, and comparators are all referenced to the analog ground (AGND). Bypass V_{5A} to AGND as close to the device as possible.

The ADC and internal digital circuitry are referenced to the digital ground (DGND). Bank 1 and Bank 2 GPIOs are referenced to GND.

Connect the OGND return directly to the GND ground plane and be as close to the OGND bump as possible.

For best analog-front-end performance, the AGND and DGND islands should only connect to the GND ground plane at one point. This is typically the same point where the IOLGND is connected to GND.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	PITCH (mm)
MAX22522AWU+	−40°C to +125°C	60 WLP	0.4
MAX22522AWU+T	−40°C to +125°C	60 WLP	0.4

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/25	Initial release	—

NOTES

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners. All Analog Devices products contained herein are subject to release and availability.