*Click **here** to ask an associate for production status of specific part numbers.*

MAX22211

36V, 3.8A Two H-Bridge for Dual Brushed or Single Stepper Motor Drive

General Description

The MAX22211 is a dual 36V, 3.8A_{MAX} H-bridge. It can be used to drive two brushed DC motors or a single stepper motor. The H-bridge FETs have very low impedance resulting in high driving efficiency and low heat generation. The typical total R_{ON} (high-side + low-side) is 0.25Ω. Each H-bridge can be individually pulse-width modulation (PWM)-controlled using three logic inputs (DIN1, DIN2, EN).

The MAX22211 features an accurate current drive regulation (CDR) which can be used to limit the start-up current of a brushed DC motor or to control the phase current for stepper operation. The bridge output current is sensed by a non-dissipative integrated current sensing (ICS) and it is then compared with user configurable threshold (I_{TRIP}). When the bridge current exceeds the I_{TRIP} threshold, the device enforces the decay for a fixed OFF-time (t_{OFF}). Four different Decay methods are supported (Slow Decay, Fast Decay, and two Mixed Decay modes). The non-dissipative ICS eliminates bulky external power resistors which are normally required for this function resulting in a dramatic space and power saving compared with mainstream applications using external sense resistors.

The internally measured current of the two full bridges are mirrored on pins ISENA and ISENB. By connecting external resistors to these pins to GND, voltages proportional to the motor currents are generated. The voltage across these external resistors can be used as inputs to analog-to-digital converters (ADCs) of an external motor controller if the motion control algorithm requires the load current or torque information.

In addition, two open-drain output pins (CDRA, CDRB) are asserted every time the internal current regulation takes control of the driver. This allows the external controller to monitor the activity of the internal current loop.

The maximum user configurable current regulation threshold (I_{TRIP_MAX}) can be set up to 3.8A and is limited by the Overcurrent Protection (OCP). The I_{TRIP} current thresholds can be set independently for the two full bridges by connecting external resistors from pins REFA and REFB to GND. Because of thermal considerations, the recommended maximum RMS current for standard four-layer PCBs is 2A_{RMS} per H-bridge.

The MAX22211 features OCP, thermal shutdown (TSD), and undervoltage lockout (UVLO) protection. An open-drain active low $\overline{FAULT}$ pin is activated every time a fault condition is detected. During TSD and UVLO events, the driver is three-stated until normal operations are restored.

The MAX22211 is available in a small TQFN32 5mm x 5mm package or a TSSOP28 4.4mm x 9.7mm package.

Applications

- Stepper-Motor Driver
- Brushed DC Motor Driver
- Solenoid Driver
- Latched Valves

Benefits and Features

- Two H-Bridges with +36V Maximum Operating Voltage
  - Total R_{ON} (High-Side + Low-Side): 250mΩ Typical (T_A = 25°C)
- Current Ratings per H-Bridge (Typical at T_A = 25°C)
  - I_{TRIP_MAX} = 3.8A (Maximum Current Setting for Internal Current Drive Regulation)
  - I_{RMS} = 2A_{RMS} (Recommended Maximum RMS Current per Full Bridge)
- Integrated Current Drive Regulation
  - ICS Eliminates Bulky External Resistors and Improves Efficiency
  - Current Drive Regulation Monitor Output Pins (CDRA, CDRB)
  - Four Decay Modes Supported (Slow Decay, Fast Decay, and two Mixed Decays)
  - Half Full Scale (HFS) Pin to Improve Current Control Accuracy in the Low Current Range
- Current Sense Output (Current Monitor)
- Fault Indicator Pin ($\overline{FAULT}$)
- Low-Power Mode (Sleep Mode)
- Protections
  - OCP for Each Individual Channel
  - UVLO
  - TSD T_J = 165°C
- TQFN32 5mm x 5mm Package and TSSOP28 4.4mm x 9.7mm Package

***Ordering Information** appears at end of data sheet.*

19-101537; Rev 1; 11/23

© 2023 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.

One Analog Way, Wilmington, MA 01887 U.S.A. | Tel: 781.329.4700 | © 2023 Analog Devices, Inc. All rights reserved.

Simplified Block Diagram

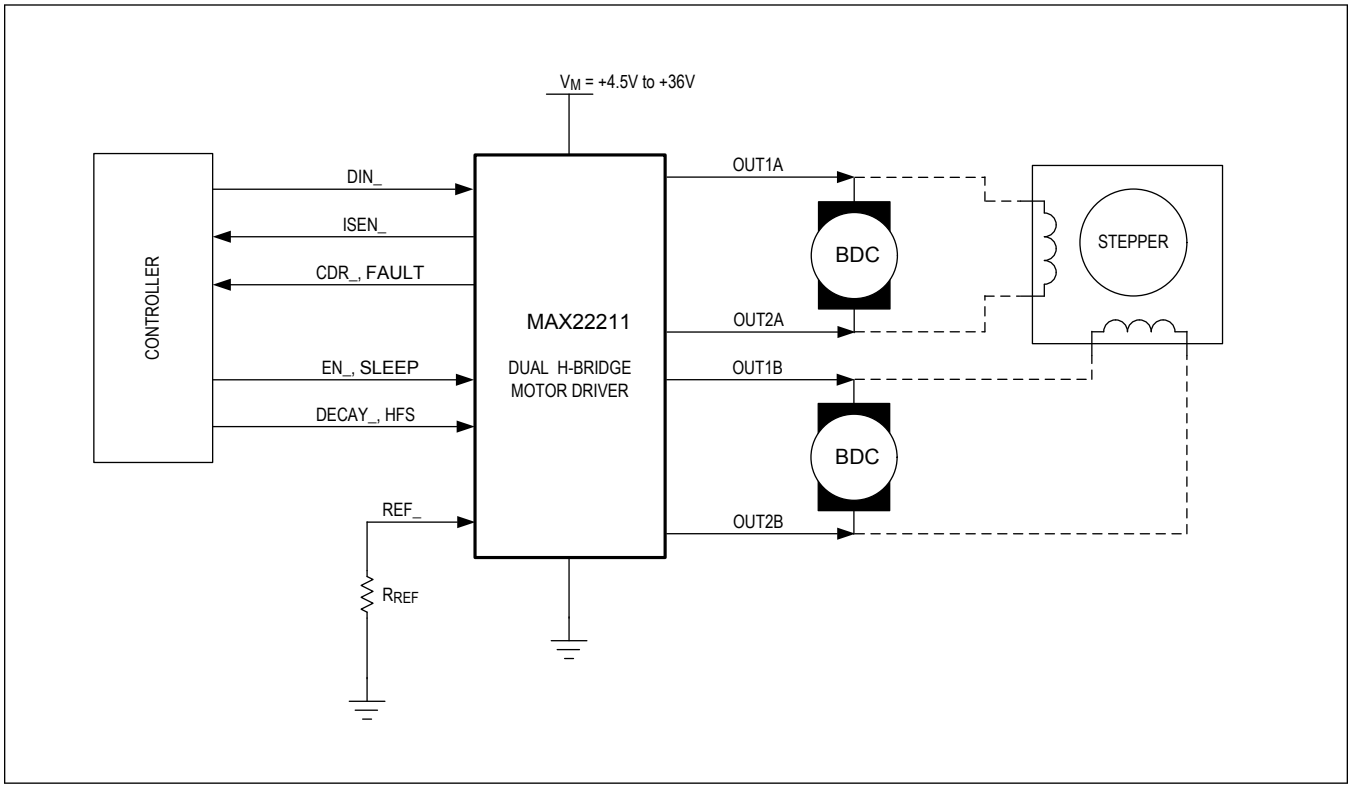


TABLE OF CONTENTS

General Description . . . 1
Applications . . . 1
Benefits and Features . . . 1
Simplified Block Diagram . . . 2
Absolute Maximum Ratings . . . 6
Package Information . . . 6
32-Pin TQFN—5mm x 5mm . . . 6
28-Pin TSSOP—4.4mm x 9.7mm . . . 6
Electrical Characteristics . . . 6
Typical Operating Characteristics . . . 10
Pin Configurations . . . 11
TQFN Pin Configuration . . . 11
TSSOP Pin Configuration . . . 12
Pin Description . . . 12
Functional Diagrams . . . 14
Diagram . . . 14
Detailed Description . . . 15
Sleep Mode (SLEEP Pin) . . . 15
PWM Control . . . 15
Current Sense Output (ISEN) - Current Monitor . . . 15
Current Drive Regulation . . . 18
Setting the Current Regulation Threshold – I_{TRIP} . . . 18
CDR Open-Drain Output . . . 19
Setting the Decay Mode . . . 20
Fault Protection . . . 21
Overcurrent Protection . . . 21
Thermal-Shutdown Protection . . . 21
Undervoltage-Lockout Protection . . . 21
Typical Application Circuits . . . 22
Application Diagram . . . 22
Ordering Information . . . 23
Revision History . . . 24

LIST OF FIGURES

Figure 1. ISEN Current 17
Figure 2. CDR Monitor Timing Diagram 20

LIST OF TABLES

Table 1. MAX22211 Truth Table 15
Table 2. HFS Truth Table 18
Table 3. Decay Mode Truth Table 20

Absolute Maximum Ratings

V_M to GND ..... -0.3V to +42V
V_{DD} to GND..... -0.3V to min (+2.2V, V_M + 0.3V)
PGND to GND ..... -0.3V to +0.3V
OUT_..... -0.3V to (V_M + 0.3)V
V_{CP} to GND..... (V_M - 0.3V) to min (+42V, V_M + 6V)
C_{P2} to GND ..... -0.3V to min (+42V, V_M + 0.3V)
C_{P1} to GND ..... (V_M - 0.3V) to min (+42V, V_M + 6V)
FAULT to GND ..... -0.3V to +6V
CDR_ to GND..... -0.3V to +6V
REF_ to GND ..... -0.3V to min (+2.2V, V_{DD} + 0.3V)
ISEN_ to GND..... -0.3V to min (+2.2V, V_{DD} + 0.3V)
DIN_ to GND..... -0.3V to +6V
EN_ to GND ..... -0.3V to +6V
HFS to GND..... -0.3V to +6V
DECAY_ to GND..... -0.3V to +6V
SLEEP to GND ..... -0.3V to min (+42V, V_M + 0.3V)
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +160°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32-Pin TQFN—5mm x 5mm

Package Code	T3255-8C
Outline Number	21-0140
Land Pattern Number	90-0013
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	47°C/W
Junction to Case (θ_{JC})	1.7°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	1.7°C/W

28-Pin TSSOP—4.4mm x 9.7mm

Package Code	U28E+5C
Outline Number	21-0108
Land Pattern Number	90-0147
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	24.65°C/W
Junction to Case (θ_{JC})	1.52°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_M = +4.5V to +36V, $R_{REF_}$ = from 12kΩ to 72kΩ, typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply-Voltage Range	V_M		4.5		36	V

Electrical Characteristics (continued)

(V_M = +4.5V to +36V, $R_{REF_}$ = from 12kΩ to 72kΩ, typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sleep-Mode Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic low		4	11	µA
Quiescent Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic high		2	4	mA
1.8V Regulator Output Voltage	V_{VDD}	V_M = +4.5V, I_{LOAD} = internal consumption	1.74	1.8	1.86	V
V_{DD} Current Limit	$I_{V18(LIM)}$		20			mA
V_{DD} UVLO Rising	$UVLOV18_R$	V_{DD} rising	1.59	1.65	1.69	V
V_{DD} UVLO Falling	$UVLOV18_F$	V_{DD} falling	1.535	1.58	1.635	V
Charge-Pump Voltage	V_{CP}			V_M + 2.7		V
LOGIC LEVEL INPUTS/OUTPUTS						
Input Voltage Level—High	V_{IH}		1.2			V
Input Voltage Level—Low	V_{IL}				0.65	V
Input Hysteresis	V_{HYS}			110		mV
Pull-Down Current	I_{PD}	To GND	16	34	50	µA
Open-Drain Output Logic-Low Voltage	V_{OL}	I_{LOAD} = 5mA			0.2	V
Open-Drain Output Logic-High Leakage Current	I_{OH}	V_{PIN} = 3.3V	-1		+1	µA
$\overline{SLEEP}$ Voltage Level High	$V_{IH(\overline{SLEEP})}$		0.9			V
$\overline{SLEEP}$ Voltage Level Low	$V_{IL(\overline{SLEEP})}$				0.6	V
$\overline{SLEEP}$ Pull-Down Input Resistance	$R_{PD(\overline{SLEEP})}$		0.8	1.5		MΩ
OUTPUT SPECIFICATIONS						
Output On-Resistance Low-Side	$R_{ON(LS)}$	HFS = logic low		0.125	0.22	Ω
		HFS = logic high		0.22	0.42	
Output On-Resistance High-Side	$R_{ON(HS)}$			0.125	0.22	Ω
Output Leakage	I_{LEAK}	Driver off	-5		+5	µA
Dead Time	t_{DEAD}			100		ns
Output Slew Rate	SR			200		V/µs
PROTECTION CIRCUITS						
Overcurrent Protection Threshold	I_{OCP}		3.8			A
Overcurrent Protection Blanking Time	t_{OCP}		1	2.2	3.2	µs
Autoretry OCP Time	t_{RETRY}			3		ms

Electrical Characteristics (continued)

(V_M = +4.5V to +36V, $R_{REF_}$ = from 12kΩ to 72kΩ, typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Threshold on V_M	V_{UVLO}	V_M rising	3.85	4	4.15	V
UVLO Threshold on V_M Hysteresis	$UVLO_{HYS}$			0.12		V
Thermal Protection Threshold Temperature	TSD			+165		°C
Thermal Protection Temperature Hysteresis	TSD_{HYS}			20		°C
CURRENT REGULATION						
REF Output Voltage	V_{REF}		0.882	0.9	0.918	V
I_{TRIP} Current Regulation Constant	K_{IFS}	HFS = logic low		36		KV
		HFS = logic high		18.4		
Current Trip Regulation Accuracy	DITRIP1	HFS = logic low, I_{OUT} = 1.1A to 3A, GBD	-5	0.4	5	%
		HFS = logic high, I_{OUT} = 0.55A to 1.5A, GBD	-5	0.4	5	
	DITRIP2	HFS = logic low, I_{OUT} = 0.5A to 1.1A, GBD	-10	0.5	10	
		HFS = logic high, I_{OUT} = 0.25A to 0.55A, GBD	-10	0.5	10	
Fixed OFF – Time Internal	t_{OFF}		16	20	24	µs
PWM Blanking Time	t_{BLK}		1.4	2.8	4	µs
CURRENT-SENSE MONITOR						
ISEN_ Voltage Range	ISEN	Voltage range at ISEN_ pins	0		1.1	V
Current-Monitor Scaling Factor	K_{ISEN}	HFS = logic low. See the I_{SEN} output-current equation in the *Current Sense Output (ISEN) - Current monitor* section.		7500		A/A
		HFS = logic high. See the I_{SEN} output-current equation in the *Current Sense Output (ISEN) - Current monitor* section.		3840		
Current-Monitor Accuracy	$DKISEN_1$	(*Note 1*) HFS = logic low, I_{OUT} = 0.7A to 3A	-5	0.4	+5	%
		HFS = logic high, I_{OUT} = 0.35A to 1.5A	-5	0.4	+5	
	$DKISEN_2$	HFS = logic low, I_{OUT} = 0.4A to 0.7A	-10	0.6	+10	
		HFS = logic high, I_{OUT} = 0.2A to 0.35A	-10	0.6	+10	
Current-Sense Output -3dB Small-Signal Bandwidth	BW			400		KHz

Electrical Characteristics (continued)

(V_M = +4.5V to +36V, $R_{REF_}$ = from 12kΩ to 72kΩ, typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. *Note 1*.)

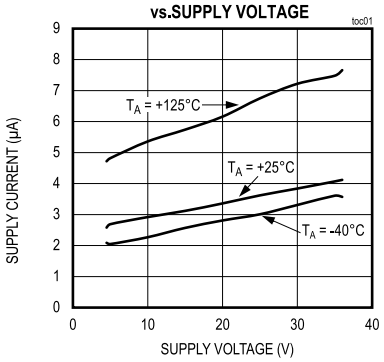
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FUNCTIONAL TIMING						
Sleep Time	t_{SLEEP}	$\overline{SLEEP}$ = logic 1 to logic 0 for OUT_ to become three-state			150	µs
Wake-Up Time from Sleep	t_{WAKE}	$\overline{SLEEP}$ = logic 0 to logic 1 to resume normal operation			3	ms
Enable Time	t_{EN}	Time from EN_ pin rising edge to driver on			0.4	µs
Disable Time	t_{DIS}	Time from EN_ pin falling edge to driver off			0.6	µs

Note 1: Guaranteed by design, not production tested.

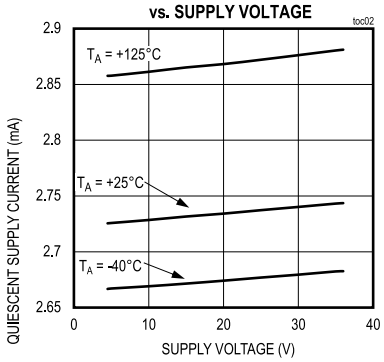
Typical Operating Characteristics

(V_M = +4.5V to +36V; T_A = 25°C unless otherwise noted.)

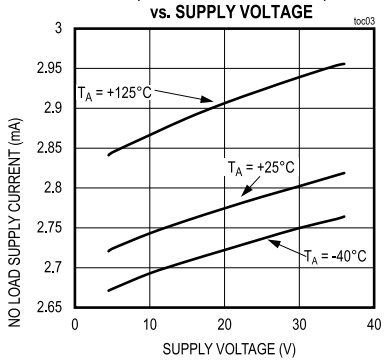
SHUTDOWN SUPPLY CURRENT vs.SUPPLY VOLTAGE



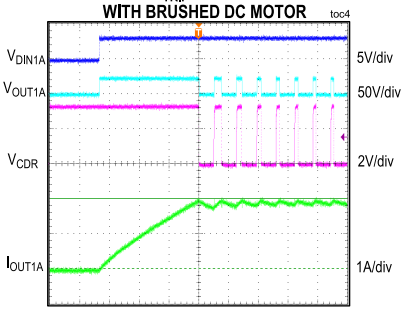
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



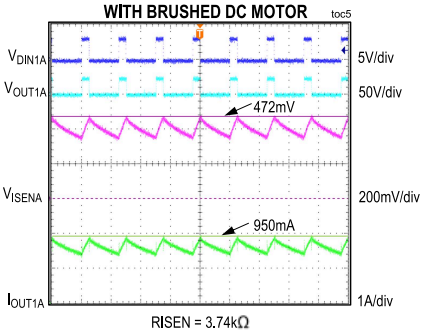
NO LOAD SWITCHING SUPPLY CURRENT (20kHz, 50% DUTY CYCLE) vs. SUPPLY VOLTAGE



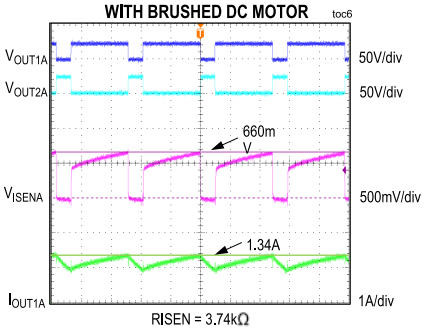
INRUSH CURRENT LIMIT 2.0A I_{TRIP} THRESHOLD WITH BRUSHED DC MOTOR



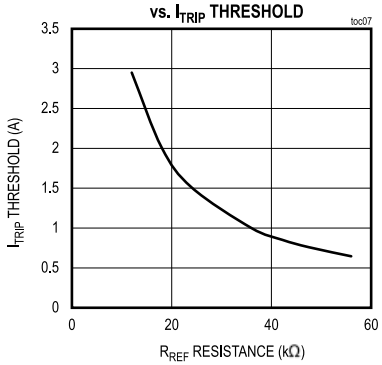
LOAD CURRENT AND ISEN VOLTAGE AT 20kHz SLOW DECAY PWM INPUT WITH BRUSHED DC MOTOR



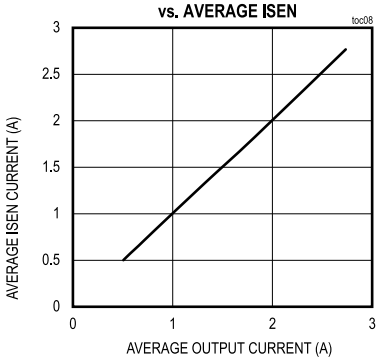
LOAD CURRENT AND ISEN VOLTAGE AT 20kHz FAST DECAY PWM INPUT WITH BRUSHED DC MOTOR



R_{REF} RESISTANCE vs. I_{TRIP} THRESHOLD

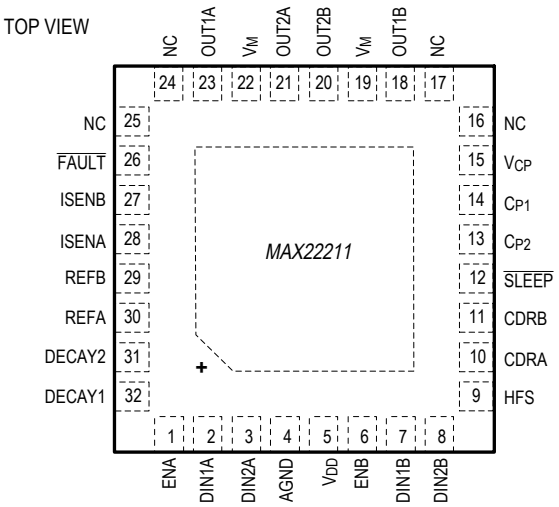


AVERAGE OUTPUT CURRENT vs. AVERAGE ISEN



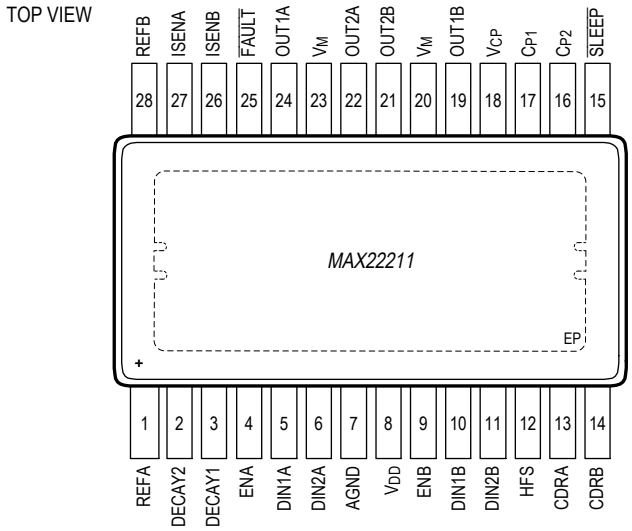
Pin Configurations

TQFN Pin Configuration



TQFN
5mm x 5mm

TSSOP Pin Configuration



TSSOP28
4.4x9.7mm

Pin Description

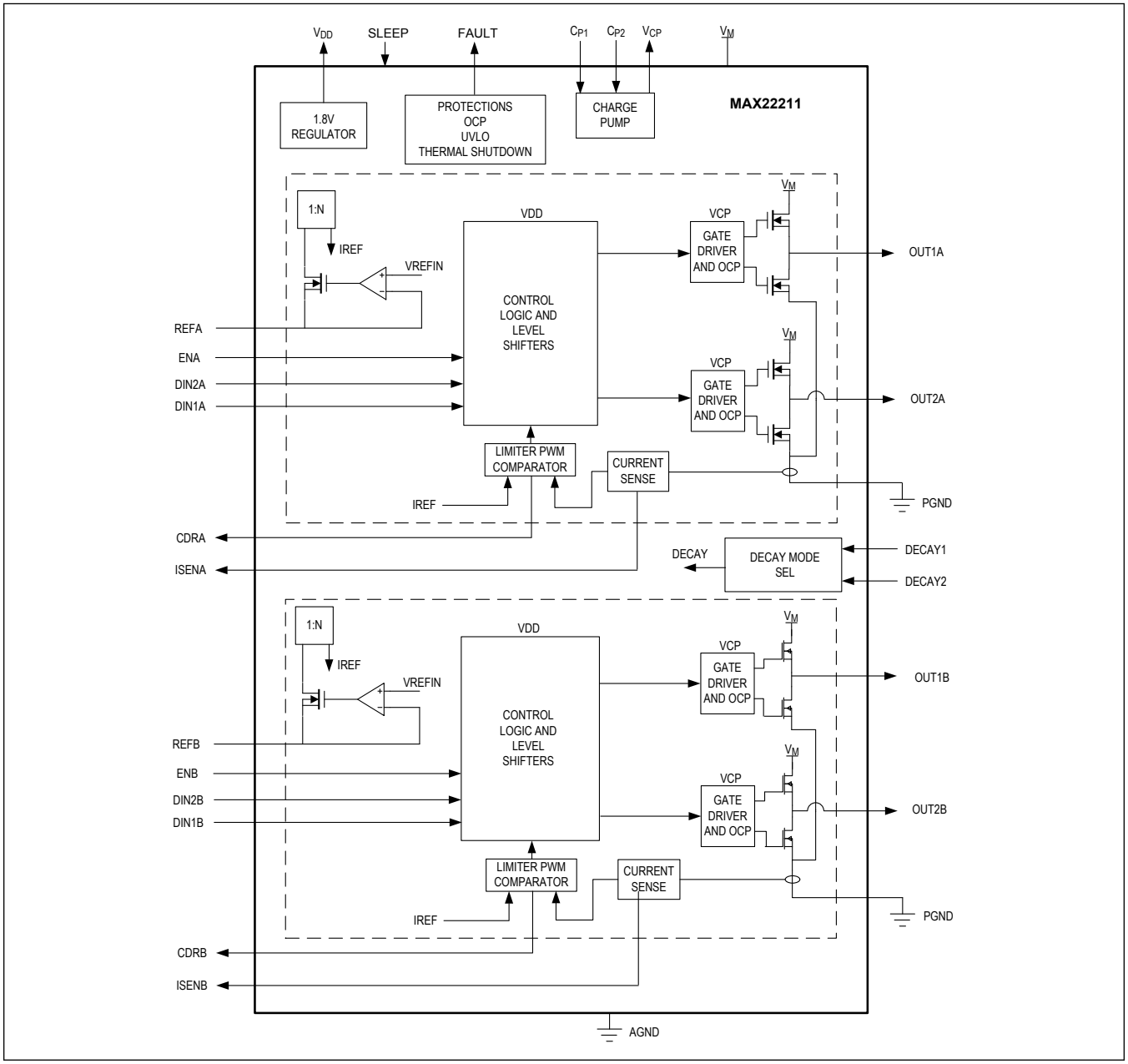
PIN		NAME	FUNCTION	TYPE
TQFN	TSSOP			
30	1	REFA	Programmable Current Analog Input. Connect a resistor from REFA to GND to set the current regulation threshold for Full Bridge A	Analog Input
29	28	REFB	Programmable Current Analog Input. Connect a resistor from REFB to GND to set the current regulation threshold for Full Bridge B	Analog Input
26	25	$\overline{\text{FAULT}}$	Active-Low, Open-Drain, Output Fault Indicator. $\overline{\text{FAULT}}$ goes low to indicate that one or more of the protection mechanisms has been activated. Connect a pull-up resistor from $\overline{\text{FAULT}}$ to the microcontroller supply voltage.	Open Drain Output
10, 11	13, 14	CDR_	Open-Drain Output. Current Drive Regulator Monitor Output.	Open Drain Output
4	7	AGND	Analog Ground. Connect to ground plane.	GND
19, 22	20, 23	V_M	Supply Voltage Input. Connect a V_M-rated 1µF (minimum) surface-mounted device capacitor from V_M to GND close to the device, and a 10µF (minimum) electrolytic bypass capacitor from V_M to GND. Higher values can be considered depending on application requirements.	Supply

Pin Description (continued)

PIN		NAME	FUNCTION	TYPE
TQFN	TSSOP			
5	8	V_{DD}	1.8V Linear Regulator Output. Bypass V_{DD} with a 2.2µF capacitor connected close to the device.	Output
23, 21, 18, 20	24, 22, 19, 21	OUT1 to OUT4, respectively	Driver Outputs	Output
27, 28	26, 27	ISEN_	Current Sense Output Monitor.	Output
2, 3, 7, 8	5, 6, 10, 11	DIN_	CMOS PWM Input	Logic Input
1, 6	4, 9	EN_	Logic Input Pin. Enable Pin	Logic Input
15	18	V_{CP}	Charge-Pump Output. Connect a 1µF capacitor between V_{CP} and V_M as close as possible to the device.	Output
14	17	C_{P1}	Charge-Pump Flying Capacitor Pin 1. Connect a 22nF capacitor between CP1 and CP2, as close as possible to the device.	Output
13	16	C_{P2}	Charge-Pump Flying Capacitor Pin 2. Connect a 22nF capacitor between CP1 and CP2, as close as possible to the device.	Output
12	15	$\overline{SLEEP}$	Active-Low Sleep Pin	Logic Input
31, 32	2, 3	DECAY_	Logic Input. Set the Decay Mode.	Logic Input
9	12	HFS	Set Output Current Full Scale. HFS = 0 coefficient is 100%. HFS = 1 coefficient is 50%.	Logic Input
16, 17, 24, 25	—	NC	No Connection. Not internally connected.	
EP	EP	PGND	Power GND. Connect to ground plane. The thermal exposed pad (EP) is also the electrical power GND pin and must be properly connected to GND.	GND

Functional Diagrams

Diagram



Detailed Description

The MAX22211 is a dual 36V, 3.8A_{MAX} H-bridge. It can be used to drive two brushed DC motors or a Single Stepper Motor. The H-bridge FETs have very low impedance resulting in high driving efficiency and lower heat generation. The typical total R_{ON} (high-side + low-side) is 0.25Ω. Each H-bridge can be individually PWM-controlled using three logic inputs (DIN1, DIN2, EN).

The MAX22211 features an accurate CDR which can be used to limit the start-up current of a brushed DC motor or to control the phase current for stepper operation. The bridge output current is sensed by a non-dissipative ICS and it is then compared with user configurable threshold (I_{TRIP}). When the bridge current exceeds the I_{TRIP} threshold, the device enforces the decay for a fixed OFF-time (t_{OFF}). Four different Decay methods are supported (Slow Decay, Fast Decay, and two Mixed Decay modes). The non-dissipative ICS eliminates bulky external power resistors which are normally required for this function resulting in a dramatic space and power saving compared with mainstream applications using external sense resistors.

The internally measured current of the two full bridges are mirrored on pins ISENA and ISENB. By connecting external resistors to these pins to GND, voltages proportional to the motor currents are generated. The voltage across these external resistors can be used as inputs to ADCs of an external motor controller if the motion control algorithm requires the load current or torque information.

In addition, two open-drain output pins (CDRA, CDRB) are asserted every time the internal current regulation takes control of the driver. This allows the external controller to monitor the activity of the internal current loop.

The maximum user configurable current regulation threshold (I_{TRIP_MAX}) can be set up to 3.8A and is limited by the OCP. The I_{TRIP} current thresholds can be set independently for the two full bridges by connecting external resistors from pins REFA and REFB to GND. Due to thermal considerations, the recommended maximum RMS current for standard four-layer PCBs is 2A_{RMS} per H-bridge.

The MAX22211 features OCP, TSD, and UVLO protection. An open-drain active low $\overline{FAULT}$ pin is activated every time a fault condition is detected. During TSD and UVLO events, the driver is three-stated until normal operations are restored.

The MAX22211 is available in a small TQFN32 5mm x 5mm package or a TSSOP28 4.4mm x 9.7mm package.

Sleep Mode ($\overline{SLEEP}$ Pin)

The $\overline{SLEEP}$ pin can be driven low to place the device into the lowest power-consumption mode possible, with all outputs three-stated, the internal circuits biased off, and the charge pump disabled. A pull-down resistor should be connected between $\overline{SLEEP}$ and GND to ensure the part is disabled whenever this pin is not actively driven. Driving the $\overline{SLEEP}$ pin high wakes up the device and returns it to normal mode. t_{WAKE} is 3ms (max).

PWM Control

When the bridge current is below the programmed threshold (i.e., $I_{BRIDGE} < I_{TRIP}$), each H-bridge is controlled by three logic inputs (DIN1_, DIN2_, EN_). The PWM techniques can be used to vary the output duty cycle and implement motor control. Table 1 shows the control Truth Table.

Table 1. MAX22211 Truth Table

EN_	DIN1_	DIN2_	OUT1_	OUT2_	DESCRIPTION
0	X	X	High-Z	High-Z	H-bridge disabled. High impedance (HiZ)
1	0	0	L	L	Brake Low; Slow Decay
1	1	0	H	L	Reverse (Current from OUT1_ to OUT2_)
1	0	1	L	H	Forward (Current from OUT2_ to OUT1_)
1	1	1	H	H	Brake High; Slow Decay

Current Sense Output (ISEN) - Current Monitor

Currents proportional to the phase currents are mirrored to pins ISENA and ISENB for the A and B H-bridges, respectively. The current is sensed when one of the two low-side FETs sink the output current, and it is therefore

meaningful during both the Energizing (t_{ON}) phase and the Brake (Slow Decay) phase. In Fast Decay the current is not monitored and ISEN_ outputs a zero current.

The following equation shows the relationship between the current sourced at ISEN and the output current.

$$I_{ISEN}(A) = \frac{I_{OUT}(A)}{K_{ISEN}}$$

Equation - ISEN Output Current

in which K_{ISEN} represents the current scaling factor between the output current and its replica at pin ISEN. The K_{ISEN} is typically 7500 A/A (with HFS logic low). For example, if the instantaneous output current is 2A, the current sourced at ISEN is 266µA.

Figure 1 shows an idealized behavior of the ISEN current when Slow or Fast Decay are used. Blanking times, delays, and rise/fall edges have been ignored.

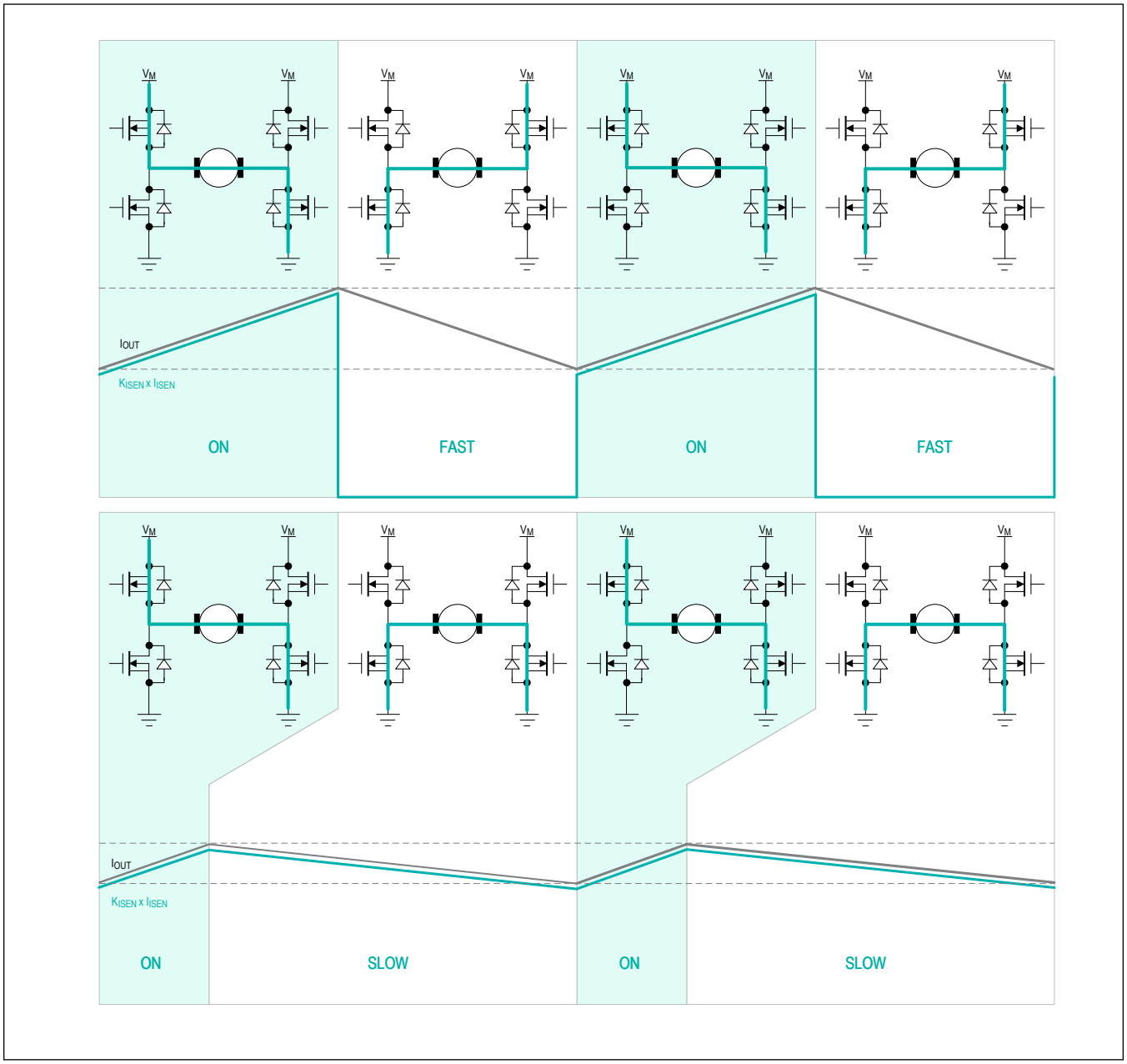


Figure 1. ISEN Current

By connecting an external signal resistor, R_{ISEN}, between the ISEN_ pin and GND, a voltage proportional to the motor current is generated. The voltage across the R_{ISEN} resistor can be input into the ADC of an external controller in applications in which the motor control algorithm requires the current/torque information. The system designer can choose a R_{ISEN} value so that the peak voltage meets the ADC full-scale requirement. The following equation shows the design formula to calculate R_{ISEN} once the ADC full-scale voltage (V_{FS}) and the maximum operating current (I_{MAX}) are known.

$$R_{ISEN}(\Omega) = K_{ISEN} \times \frac{V_{FS}(V)}{I_{MAX}(A)}$$

Equation - RISEN Setting

For example, if the ADC operates up to 1V FS and the maximum operating output current is 2A, then R_{ISEN} would be 7500 x 1V/2A = 3.75KΩ.

The R_{ISEN} value also sets the output impedance of the Current Sense Output circuit (ISEN output impedance). Normally, the input impedance of the ADC is much higher than R_{ISEN} enabling a direct connection to the ISEN pin without attenuation. In case a low input impedance ADC is used, a pre-amplifier (buffer) could be required.

The Current Sense Output circuit bandwidth and step response performances (see Specifications) ensure that the current monitor tracks the driver current in PWM motor drive applications.

Current Drive Regulation

The MAX22211 features embedded CDR. The embedded CDR provides an accurate control of the current flowing into the motor windings. The bridge current is sensed by non-dissipative ICS and it is then compared with the threshold current (I_{TRIP}). As soon as the bridge current exceeds the threshold, the device enforces slow decay for a fixed OFF-time (t_{OFF}). Once t_{OFF} has elapsed, the driver is re-enabled for the next PWM cycle. During current regulation, the PWM duty cycle and frequency depend on the supply voltage, motor inductance, and motor speed and load conditions.

Setting the Current Regulation Threshold – I_{TRIP}

Connect resistors from REFA and REFB to GND to set the current regulation thresholds for Full Bridge A and Full Bridge B, respectively (I_{TRIPA}, I_{TRIPB}) .

The following equation shows the typical I_{TRIP} current as a function of the $R_{REF_}$ shunt resistor connected to pin REF_.

$$I_{TRIP} = \frac{K_{IFS}(kV)}{R_{REF}(K\Omega)} \times HFS(\%)$$

The proportionality constant K_{IFS} is typically 36kV when HFS is logic low and 18.4kV when HFS is logic high. The external resistor R_{REF} can range between 9.5kΩ and 72kΩ.

The HFS depends on the status of the Logic Input pin HFS. When HFS is set logic low, the scalar coefficient is 100% and the power FETs $R_{DS(ON)}$ is set to a minimum 0.25Ω (high-side + low-side). When the HFS is set logic high, the scalar coefficient is 50% and the power FETs have higher $R_{DS(ON)}$ of 0.375Ω (high-side + low-side). This setting is recommended for applications in which the maximum current does not exceed 1.9A and high accuracy at low current is desirable.

The Table 2 summarizes the HFS settings.

Table 2. HFS Truth Table

HFS	I_{TRIP} (%)	MAXIMUM OUTPUT CURRENT	TYPICAL $R_{DS(ON)}$ (HIGH-SIDE + LOW-SIDE)	NOTES
0	100%	3.8A	0.25Ω	Optimized efficiency and extended operating range up to $3.8A_{MAX}$
1	50%	1.9A	0.375Ω	Reduced operating range up to $1.9A_{MAX}$. Improved current accuracy control in the bottom end of the current range

Thermal constraints and limitations must be carefully considered when setting the I_{TRIP} current threshold. These constraints depend on the PCB layout, ground plane thickness, number of layers, air ventilation, heat sinks, number of thermal vias, maximum ambient temperature, etc. A maximum of $2A_{RMS}$ is recommended per H-bridge RMS current when using a standard four-layer board with no forced air or heatsinks. With a proper thermal designed board, a higher peak current can be delivered when the burst duration is significantly shorter than the PCB thermal time constant. For example, using our evaluation board without forced air and with two H-bridges operating simultaneously the device was able to deliver up to 3.8A per H-bridge for a 100ms long burst at room temperature.

CDR Open-Drain Output

This pin is an active-low open-drain output, which is asserted during the fixed decay time interval (t_{OFF}) enforced by the current drive regulation loop. This way, an external controller can monitor if the integrated current loop has taken control of the driver overwriting the status of the PWM logic inputs (DIN1, DIN2). The CDR signal can be used by the external controller for several reasons and provides information about the actual load during current regulation.

In the use case in which the PWM logic inputs are permanently held in Forward or Reverse mode and motor control is entirely entrusted to the internal Current Drive Regulation loop, the CDR pin outputs a PWM logic signal which is a replica of the PWM voltage applied to the load. By processing this signal and comparing its duty cycle with the expected one, a stall detection algorithm can be implemented. The CDR output can also be used as a trigger signal for an external ADC when sampling the ISEN current.

A pullup resistor must be connected from the CDR pins to the controller voltage supply.

The timing diagram in Figure 2 shows the behavior of this function when the motor spins in forward direction with DIN2 held firmly high (Case A) or when DIN2 is toggling (Cases B and C), respectively. The CDR output is asserted only when the decay mode is forced by the internal Current Regulation loop. Note that any PWM transition by the current drive regulation loop resets the fixed off time of the CDR circuit. In Case B, the actual Decay Interval is longer than t_{OFF}, whereas in Case C, the actual Decay Off interval is shorter.

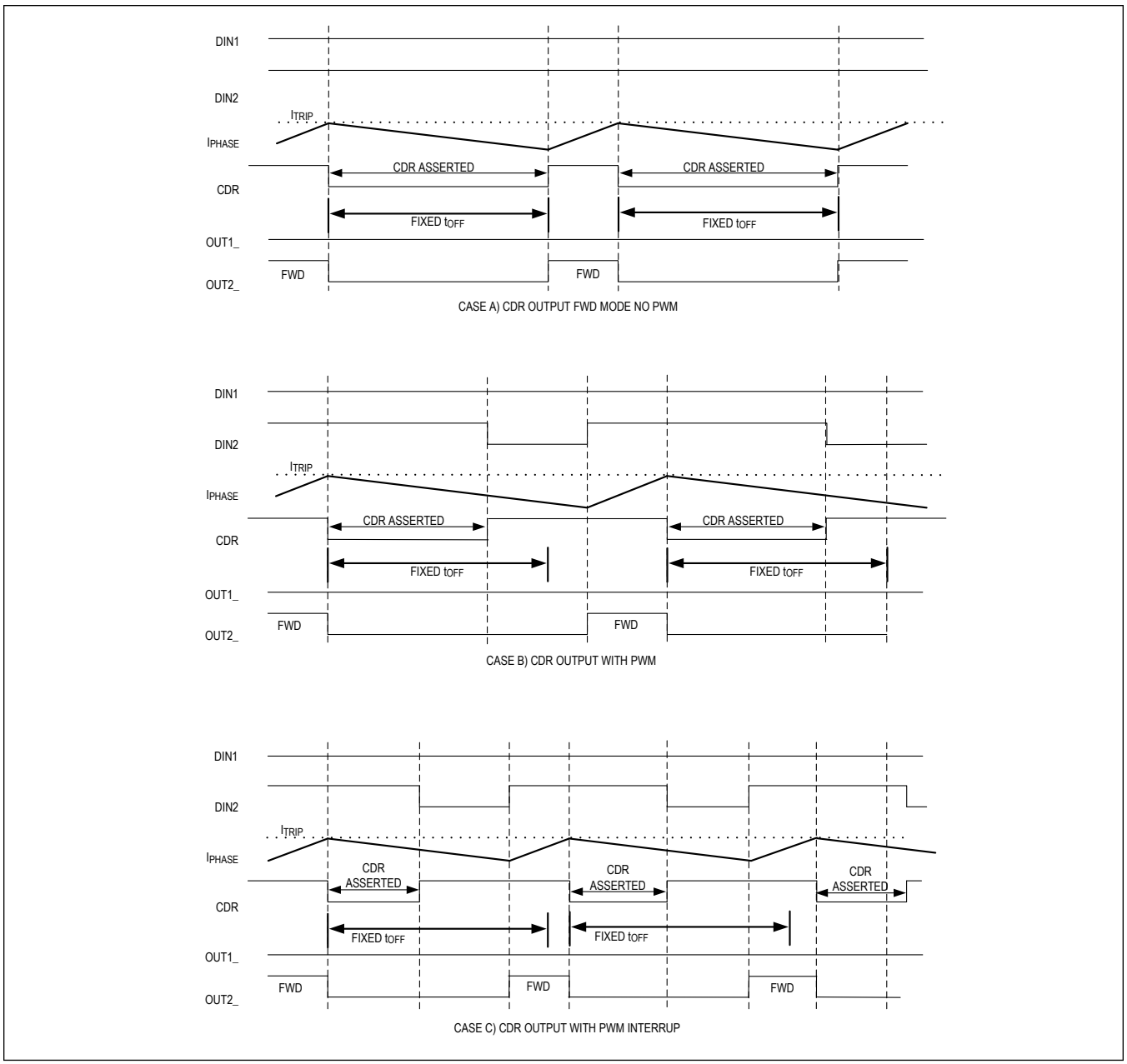


Figure 2. CDR Monitor Timing Diagram

Setting the Decay Mode

Two logic input pins allow to set the Decay Mode during t_{OFF}. The MAX22211 supports slow, fast, and two different mixed decay modes.

Table 3 shows the Truth Table for the Decay Mode selection.

Table 3. Decay Mode Truth Table

DECAY2	DECAY1	DECAY MODE
0	0	Slow

Table 3. Decay Mode Truth Table (continued)

0	1	Mixed 30% Fast/70% Slow
1	0	Mixed 60% Fast/40% Slow
1	1	Fast

Fault Protection

Overcurrent Protection

Overcurrent protection protects the device against short circuits to the rails (supply voltage and ground) and between the outputs (OUT1_ and OUT2_). The OCP threshold is set at 3.8A minimum. If the output current is greater than the OCP threshold for longer than the Overcurrent Protection Blanking Time (t_{OCP}), then an OCP event is detected.

When an OCP event is detected, the H-bridge is immediately disabled, and a fault indication is output on pin $\overline{FAULT}$. The H-bridge is kept in HiZ mode for 3ms (see t_{RETRY} specification). After that, the H-bridge is re-enabled according to the current state of the inputs. If the short circuit is still present, this cycle repeats otherwise normal operation resumes. Prolonged operation in a short-circuit failure mode is not recommended. Prolonged OCP events can affect the device reliability.

Thermal-Shutdown Protection

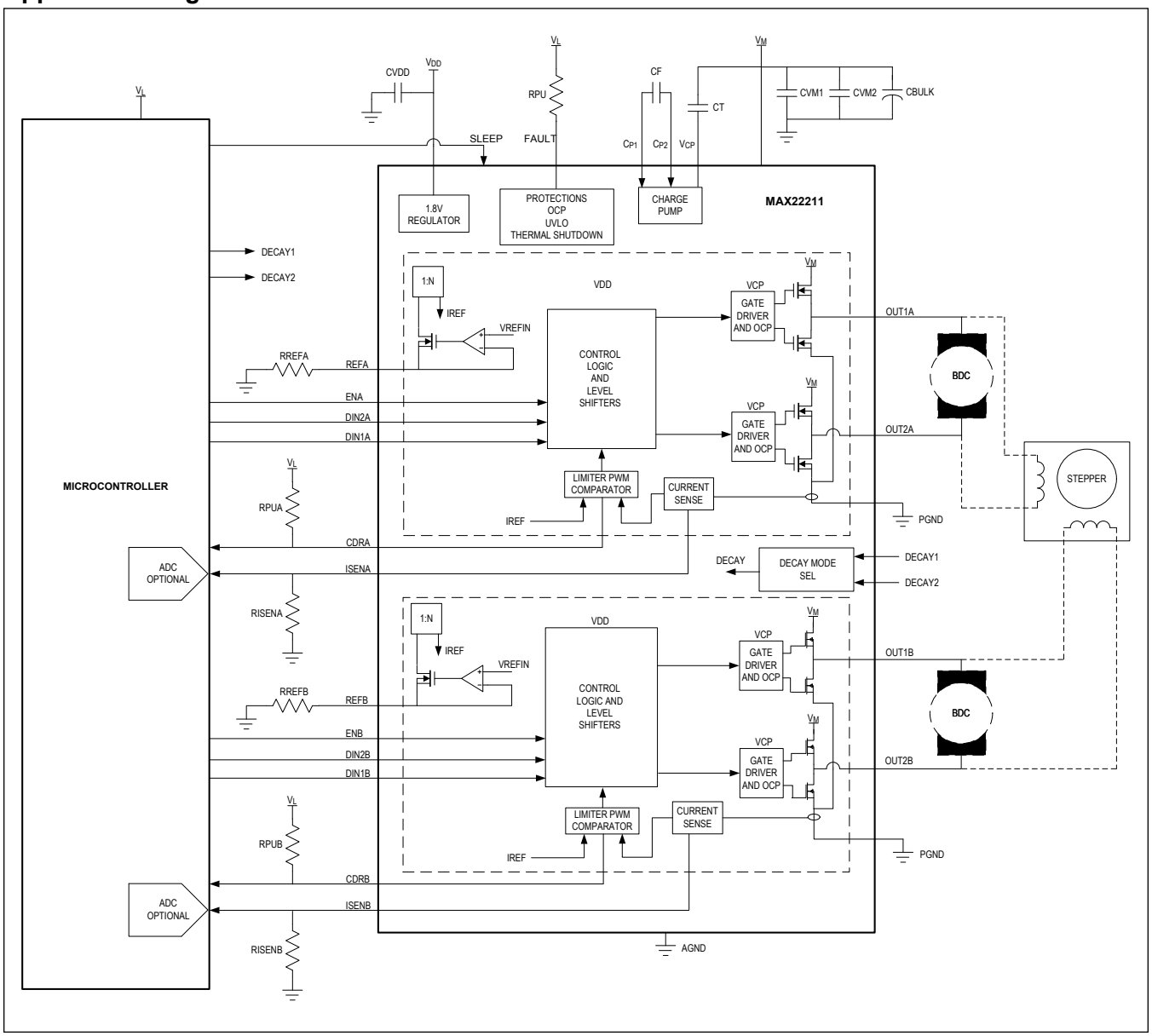
If the die temperature exceeds T_{SD} = +165°C (typ), all output pins (OUT1–OUT4) are three-stated and the $\overline{FAULT}$ pin is driven low. The $\overline{FAULT}$ pin remains low and the outputs are placed in three-state mode until the die temperature falls by the hysteresis amount of 20°C (typ), after which the $\overline{FAULT}$ pin is driven high and the outputs are re-enabled.

Undervoltage-Lockout Protection

When the V_M supply voltage is below the UVLO threshold, all OUT_ outputs are three-stated and the $\overline{FAULT}$ pin is driven low. The OUT_ outputs automatically return to their current state (defined by EN_ and DIN_) when the V_M supply voltage exceeds the OVLO threshold (max) and $\overline{FAULT}$ is driven high.

Typical Application Circuits

Application Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX22211ATJ+T	-40°C to +125°C	32 TQFN - 5mm x 5mm
MAX22211AUI+T	-40°C to +125°C	28 TSSOP - 4.4mm x 9.7mm

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/23	Release for Market Intro	—
1	11/23	Updated *Absolute Maximum Ratings*, *Package Information*, *Electrical Characteristics*, *Pin Configurations*, *Detailed Description*, and *Ordering Information* sections	6, 7, 8, 9, 11, 12, 14, 21, 23

ANALOG DEVICES
www.analog.com

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.