MAX20362

High Peak Load PMIC for Low-Power-Density Batteries

FEATURES

- Low-Power Energy Buffering and with One Inductor
  - Ultra-Low 2.8µA I_Q
  - 5mA to 50mA Input-Current Limit, 1mA Steps
  - 128mA Max BBOUT Current
  - Flexible V_{CAP} Storage Voltages from 1.6V to 9.5V
  - Adjustable V_{BBOUT} from 1.5V to 5.5V, 50mV Steps
  - Ultra-Fast DVS with PPG AFE Interoperability
    - Up to 70% LED Power Savings in PPG Systems
- Small, Flexible Solution
  - I^2C MCU Interface
  - Proprietary Digital Interface to ADI PPG AFEs
  - Tiny Inductor Options
    - 0603 (balance efficiency/size)
    - 0402 (smallest size)
  - 2.53mm x 1.69mm, 24-Bump 0.4mm Pitch WLP

APPLICATIONS

- Fitness/Wellness Heart Rate Trackers
- Medical Vital Signs Patches

***Ordering Information* appears at end of data sheet.**

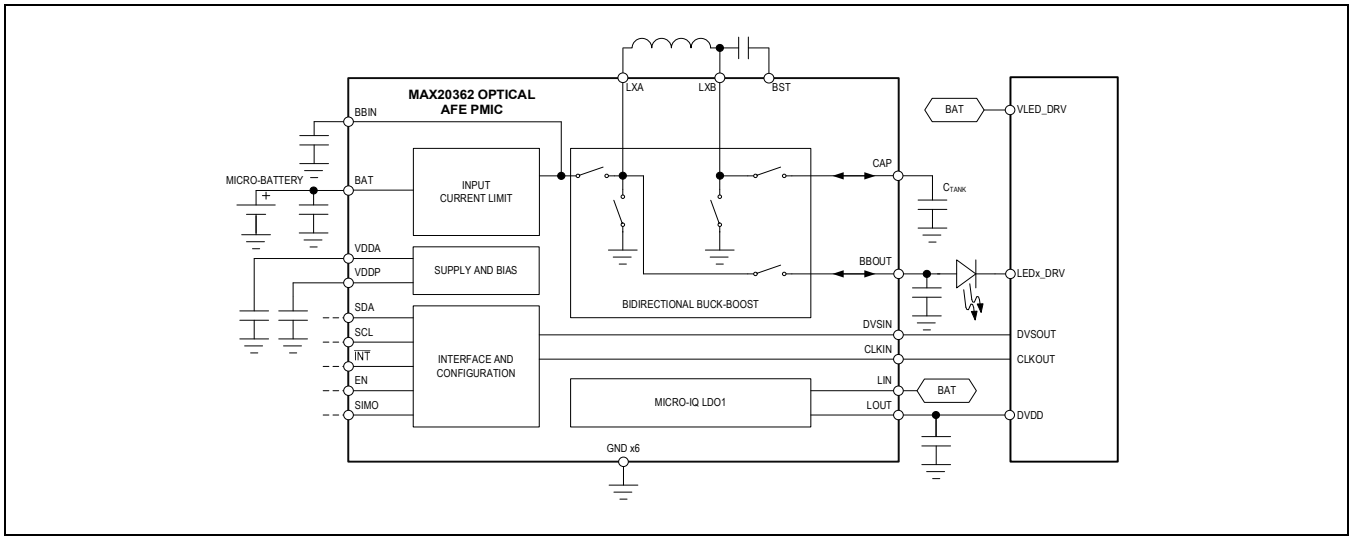
GENERAL DESCRIPTION

The MAX20362 is a power management IC (PMIC) designed to facilitate the power requirements of high peak-load currents in wearable medical and wellness devices using low-power-density batteries. One such application is the delivery of high peak LED currents in photoplethysmography (PPG) subsystems in instances where low-power-density batteries are in use. The device features low quiescent current (2.8µA typ), a high-efficiency multidirectional buck-boost converter, and a low quiescent current (0.75µA typ) fast transient response LDO.

The buck-boost converter operates over a wide input/output voltage range and features a capacitor/supercapacitor charging mode which uses a precise switch-mode input-current limiter to prevent battery current overdraw in systems with weak batteries. The buffer capacitance is then used to supply high peak loads on the BBOUT node, thereby protecting the battery from large peak currents.

The low I_Q LDO is optimized for fast transient response to preserve the highly sensitive PPG analog front end (AFE) signal-to-noise ratio (SNR).

SIMPLIFIED APPLICATION DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 1. Absolute Maximum Ratings

PARAMETER	RATING
SDA, SCL, DVSIN, CLKIN, SIMO, LIN, EN, BAT, BBOUT, LXA	-0.3V to +6.0V
$\overline{INT}$, CAP	-0.3V to +12.0V
BBIN	-0.3V to Min (+6.0, V_{BAT} + 0.3)V
V_{DDP}, V_{DDA}	-0.3V to 2.2V
LXB	-0.3V to Min (+12, V_{CAP} + 0.3)V
BST	Max (V_{LXB} – 0.3, V_{DDP} – 0.3)V to V_{LXB} + 2.2V
LOUT	-0.3V to V_{LIN} + 0.3V
GND to GND	-0.3V to +0.3V
Continuous Current into LIN, LOUT, BBOUT	±250mA
Continuous Current into CAP, LXA, LXB (10% utilization for 100k hours)	±1.6A
Continuous Current into Any Other Terminal	±100mA
Continuous Power Dissipation (Multilayer Board, T_A = +70°C) (derate 33.11mW/°C above +70°C)	2649mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Table 2. Thermal Resistance

Package Type	Θ_{JA}	Unit
W241L2+1	30.2	°C/W

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only Human body model (HBM) per ANSI/ESDA/JEDEC JS-001 Field induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002. International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2. Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings for

Table 3. MAX20362

ESD Model	Withstand Threshold (V)	Class
HBM	±2500	2

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SPECIFICATIONS

Table 4. Electrical Characteristics

(V_{BAT} = 1.85V to +5.5V , T_A = -40°C to +85°C, unless otherwise noted, typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{BBOUT} = 5V, V_{CAP} = 5V, V_{LIN} = 3.7V, V_{LOUT} = 1.8V, C_{CAP_EFF} = >8µF, C_{BAT_EFF} = 1µF, C_{BBIN_EFF} = See the *BBIN Capacitor Selection* section, C_{LIN_EFF} = 1µF, C_{LOUT_EFF} = 1µF, C_{BBOUT_EFF} = See the *BBOUT Capacitor Selection* section, $L_{LXA, LXB}$ = 2.2µH, limits are 100% production tested at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
CURRENT CONSUMPTION							
Shutdown Supply Current	I_{SHDN}	Shutdown	EN = 0		0.1	2	µA
			EN = 1, disabled by register		1.9		
BAT Input Current	I_{Q_BAT}	LDO enabled			2.65		µA
		Buck-boost enabled			2.8		
		Buck-boost enabled and LDO enabled			3.6		
BUCK-BOOST CONVERTER							
Input Voltage Range	V_{BBIN}			1.85		5.5	V
Battery Startup Input Voltage	V_{BAT_STUP}			2.1			V
Output Voltage Range	V_{BBOUT}	50mV step resolution		1.5		5.5	V
CAP Voltage Range	V_{CAP}	BBstStepCap = 00b = 500mV step resolution		2.500		9.500	V
		BBstStepCap = 01b = 250mV step resolution		1.600		5.350	
		BBstStepCap = 10b = 125mV step resolution		1.650		3.025	
Quiescent Supply Current	I_{Q_BB}	I_{BBOUT} = 0µA, BBstVSetCap = 5V, BBstVSet = 5V	Normal operating mode		0.9		µA
	$I_{Q\_BB\_FAST}$	I_{BBOUT} = 0µA, BBstVSetCap = 5V, BBstVSet = 5V	FAST mode		150		
	$I_{Q\_BB\_FPWM}$	I_{BBOUT} = 0µA, BBstVSetCap = 5V, BBstVSet = 5V, current from BAT	FPWM mode		1		mA

(V_{BAT} = 1.85V to +5.5V , T_A = -40°C to +85°C, unless otherwise noted, typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{BBOUT} = 5V, V_{CAP} = 5V, V_{LIN} = 3.7V, V_{LOUT} = 1.8V, C_{CAP_EFF} = >8µF, C_{BAT_EFF} = 1µF, C_{BBIN_EFF} = See the *BBIN Capacitor Selection* section, C_{LIN_EFF} = 1µF, C_{LOUT_EFF} = 1µF, C_{BBOUT_EFF} = See the *BBOUT Capacitor Selection* section, $L_{LXA, LXB}$ = 2.2µH, limits are 100% production tested at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
	$I_{Q\_CAP\_FPWM}$	I_{BBOUT} = 0µA, BBstVSetCap = 5V, BBstVSet = 5V, current from CAP	FPWM mode		8		
Input Current Limit Range	I_{BBLIM}	1mA steps		5		50	mA
Input Current Limit Drop Set Range	V_{BBLIM_DROP}	V_{BBIN} rising	BBIngenDrp = 00b		55		mV
			BBIngenDrp = 01b		100		
			BBIngenDrp = 10b		150		
			BBIngenDrp = 11b		200		
Input Current Limit Max Drop Threshold	$I_{BBLIM\_DRP\_MAX}$	V_{BBIN} falling			360		mV
Input Current Limit Accuracy	I_{BBLIM_ACC}	BBIngenDrp = 00b, BBIN V_{RIPPLE} < 30mV				15	%
		BBIN V_{RIPPLE} < 30mV				25	
Average BBOUT Output Voltage Accuracy	V_{BBOUT_ACC}	I_{BBOUT} = 10mA, C_{BBOUT_EFF} ≥ 5µF	BBstFast = 1	-0.5		+2.7	%
			BBstFast = 0	-1.5		+2	
Average CAP Output Voltage Accuracy	V_{CAP_ACC}	C_{CAP_EFF} ≥ 10µF	BBstFast = 1	-1.5		+1.5	%
			BBstFast = 0	-2		+2	
BBOUT Line Regulation Error	$V_{LINEREG\_BBOUT}$	I_{OUT} = 1mA		-1		+1	%/V
BBOUT Line Transient Response	V_{LINE_TRAN}	V_{BAT} from 3.4V to 2.9V, I_{BBOUT} = 1mA			20		mV
BBOUT Load Regulation Error	$V_{LOADREG\_BBOUT}$	V_{CAP} > 3.7V, I_{OUT} = 128mA			-2.5		%
BBOUT Load Transient Response	V_{LOAD_TRAN}	V_{BBOUT} = 5V, I_{BBOUT} = 10µA to 100mA			40		mV
BBOUT Maximum Output Current	I_{BBOUT_MAX}	V_{CAP} > 1.5V	Load reg ≤ -7.5%	128			mA

(V_{BAT} = 1.85V to +5.5V , T_A = -40°C to +85°C, unless otherwise noted, typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{BBOUT} = 5V, V_{CAP} = 5V, V_{LIN} = 3.7V, V_{LOUT} = 1.8V, C_{CAP_EFF} = >8µF, C_{BAT_EFF} = 1µF, C_{BBIN_EFF} = See the *BBIN Capacitor Selection* section, C_{LIN_EFF} = 1µF, C_{LOUT_EFF} = 1µF, C_{BBOUT_EFF} = See the *BBOUT Capacitor Selection* section, $L_{LXA, LXB}$ = 2.2µH, limits are 100% production tested at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Startup Time	t_{STUP}	C_{CAP_EFF} = 22µF, I_{BBLIM} = 5mA, V_{BBOUT} from 0 to 5.5V, V_{CAP} from 0 to 9.5V, time from EN rising to BBstOnInt			300		ms
Nominal Rising DVS Valley Inductor Current Limit Range	I_{VLYLIM_P}	50mA steps	BBHalfBW = 1	0		550	mA
			BBHalfBW = 0	0		1100	
Nominal Falling DVS Inductor Current Limit Range	$I_{VLY\_LIM\_N}$	50mA steps		0		1550	mA
Soft-Start Current	I_{BB_SS}					I_{BBLim}	mA
Output UVLO Threshold	V_{BBOUT_UVLO}	Rising edge		1.05	1.13	1.25	V
		Falling edge		1.00	1.10	1.20	
VDDA UVLO Threshold	$V_{DDA\_UVLO\_R}$	Rising edge		1.685	1.710	1.735	V
	$V_{DDA\_UVLO\_F}$	Falling edge		1.650	1.675	1.700	
CAP UVLO Threshold	$V_{CAP\_UVLO\_R}$	Rising edge		1.05	1.13	1.25	V
	$V_{CAP\_UVLO\_F}$	Falling edge		1.00	1.10	1.20	
CAP MIN Threshold	$V_{CAP\_MIN\_R}$	Rising edge		1.50	1.56	1.60	V
	$V_{CAP\_MIN\_F}$	Falling edge		1.45	1.50	1.55	
CAP OVLO Threshold	$V_{CAP\_OVLO\_R}$	Rising edge	BBstOvloSel = 00b	2.45	2.50	2.55	V
			BBstOvloSel = 01b	4.90	5.00	5.10	
			BBstOvloSel = 10b	6.17	6.30	6.43	
			BBstOvloSel = 11b	9.80	10.00	10.20	
CAP OVLO Hysteresis	$V_{CAP\_OVLO\_H}$				2		%
LXA Leakage Current	I_{LK_BBLXA}					2.5	µA
LXB Leakage Current	I_{LK_BBLXB}					2.5	µA
BST Leakage Current	I_{LK_BST}					2.5	µA
Passive Discharge Resistance	R_{PSV_CAP}				2.5		kΩ
	R_{PSV_BBOUT}				1.3		
Active Discharge Current BBOUT	I_{ACTD_BBOUT}	V_{BBOUT} = 2.5V			20		mA

(V_{BAT} = 1.85V to +5.5V , T_A = -40°C to +85°C, unless otherwise noted, typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{BBOUT} = 5V, V_{CAP} = 5V, V_{LIN} = 3.7V, V_{LOUT} = 1.8V, C_{CAP_EFF} = >8µF, C_{BAT_EFF} = 1µF, C_{BBIN_EFF} = See the *BBIN Capacitor Selection* section, C_{LIN_EFF} = 1µF, C_{LOUT_EFF} = 1µF, C_{BBOUT_EFF} = See the *BBOUT Capacitor Selection* section, $L_{LXA, LXB}$ = 2.2µH, limits are 100% production tested at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Active Discharge Current CAP	I_{ACTD_CAP}	V_{CAP} = 2.5V		20		mA
BBOUT Pulldown Current	$I_{PD\_BBOUT\_E}$	BBOUT enabled, BBstFast = 0		40		nA
CAP Pulldown Current	$I_{PD\_CAP\_E}$	BBOUT enabled, BBstFast = 0		40		nA
Thermal Shutdown Threshold	T_{SHDN_BB}			140		°C
FAST TRANSIENT RESPONSE LDO						
Input Operating Voltage	V_{LIN}		1.71		5.50	V
Quiescent Supply Current	I_{Q_LDO}	V_{LIN} ≥ max (LDOVset + 0.1V, 1.8V), T_A = 25°C		0.75	1.50	µA
		V_{LIN} ≥ max (LDOVset + 0.1V, 1.8V), T_A = -40°C to +85°C		0.94	11	
Quiescent Supply Current in Dropout	$I_{Q\_L\_DRP}$	I_{LOUT} = 0µA, V_{LIN} = 2.4V, LDOVSet = 2.5V		392	740	µA
		I_{LOUT} = 0µA, V_{LIN} = 1.7V, LDOVSet = 1.8V		374	562	
Quiescent Supply Current at LIN Clip Threshold	$I_{Q\_L\_DRP\_TH}$	I_{LOUT} = 0µA, LDOVSet = 1.8V		30		µA
		I_{LOUT} = 0µA, LDOVSet = 2.5V		30		
Output Leakage	I_{LK_LOUT}	V_{LOUT} = GND, LDO disabled			6	µA
Maximum Output Current	I_{LOUT_MAX}	V_{LIN} > 1.8V	100			mA
		V_{LIN} ≤ 1.8V	50			
Output Voltage Range	V_{LOUT}	100mV step resolution	0.9		4.0	V
Output Voltage Accuracy	V_{LDO_ACC}	V_{LIN} = (V_{LOUT} + 0.5V) or higher, I_{LOUT} = 1mA	-2.4		+2.4	%
Dropout Voltage	V_{DRP_L}	V_{LIN} = 1.7V, I_{LOUT} = 100mA, LDOVSet = 1.8V			100	mV
Line Regulation Error	$V_{LINE\_REG\_L}$	V_{LIN} = (V_{LOUT} + 0.5V) to 5.5V, I_{LOUT} = 1mA	-0.005		+0.005	%/V

(V_{BAT} = 1.85V to +5.5V , T_A = -40°C to +85°C, unless otherwise noted, typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{BBOUT} = 5V, V_{CAP} = 5V, V_{LIN} = 3.7V, V_{LOUT} = 1.8V, C_{CAP_EFF} = >8µF, C_{BAT_EFF} = 1µF, C_{BBIN_EFF} = See the *BBIN Capacitor Selection* section, C_{LIN_EFF} = 1µF, C_{LOUT_EFF} = 1µF, C_{BBOUT_EFF} = See the *BBOUT Capacitor Selection* section, $L_{LXA, LXB}$ = 2.2µH, limits are 100% production tested at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Load Regulation Error	$V_{LOAD\_REG\_L}$	I_{LOUT} = 100µA to 100mA, V_{LIN} = (V_{LOUT} + 0.5V) to 5.5V		0.0004	0.0008	%/mA
Line Transient	$V_{LINE\_TRAN\_L}$	V_{LIN} = 1.9V to 5V, 200ns rise time, LDOVSet = 1.8V, I_{LOAD} = 1mA		±35		mV
		V_{LIN} = 1.9V to 5V, 1µs rise time, LDOVSet = 1.8V, I_{LOAD} = 1mA		±25		
		V_{LIN} = 1.9V to 5V, 10µs rise time, LDOVSet = 1.8V, I_{LOAD} = 1mA		±5		
Load Transient	$V_{LOAD\_TRAN\_L}$	I_{LOUT} = 0mA to 5mA, 200ns rise time, C_{LDO_EFF} = 1µF, LDOVSet = 1.8V		18		mV
		I_{LOUT} = 0mA to 100mA, 200ns rise time, C_{LDO_EFF} = 1µF, LDOVSet = 1.8V		105		
Load Transient Recovery Time	$t_{LOAD\_TRAN\_L}$	I_{LOUT} = 0mA to 5mA, 200ns rise time, C_{LDO_EFF} = 1µF, LDOVSet = 1.8V		37		µs
		I_{LOUT} = 0mA to 100mA, 200ns rise time, C_{LDO_EFF} = 1µF, LDOVSet = 1.8V		12		
Passive Discharge Resistance	R_{PSV_L}		7	10	13	kΩ
Active Discharge Current	I_{ACTD_L}	V_{LIN} = 3.7V	10	16	22	mA
Turn-On Time	t_{ON_L}	V_{LIN} = 4.5V, LDOVSet = 4V, I_{LOUT} = 0mA, time from enable to 90% of final value		8.3	11.5	ms
Startup Current	I_{STUP_L}	V_{LIN} = 4.5V, LDOVSet = 4V, C_{LDO_EFF} = 1µF		5.2	10	mA
Soft-Start Output Slew Rate	V_{SS_SLEW}			5.2		V/ms
Short-Circuit Current Protection Threshold	I_{SHRT_L}	V_{LIN} = 2.7V, V_{LOUT} = GND	125	250	545	mA
Thermal Shutdown Temperature	T_{SHDN_L}			130		°C

(V_{BAT} = 1.85V to +5.5V , T_A = -40°C to +85°C, unless otherwise noted, typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{BBOUT} = 5V, V_{CAP} = 5V, V_{LIN} = 3.7V, V_{LOUT} = 1.8V, C_{CAP_EFF} = >8µF, C_{BAT_EFF} = 1µF, C_{BBIN_EFF} = See the *BBIN Capacitor Selection* section, C_{LIN_EFF} = 1µF, C_{LOUT_EFF} = 1µF, C_{BBOUT_EFF} = See the *BBOUT Capacitor Selection* section, $L_{LXA, LXB}$ = 2.2µH, limits are 100% production tested at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Thermal Shutdown Temperature Hysteresis	$T_{SHDN\_HYS\_L}$			20		°C
Output Noise	V_{NOISE_L}	10Hz to 100kHz, V_{LIN} = 5V LDOVSet = 3.3V		120		µVRMS
		10Hz to 100kHz, V_{LIN} = 5V LDOVSet = 2.5V		100		
		10Hz to 100kHz, V_{LIN} = 5V LDOVSet = 1.2V		65		
		10Hz to 100kHz, V_{LIN} = 5V LDOVSet = 0.9V		50		
DIGITAL INTERFACE						
SDA, SCL, $\overline{INT}$, EN, DVSIN, CLKIN, SIMO Input Leakage Current	I_{LK_IO}		-1		+1	µA
SDA, SCL, EN, DVSIN, CLKIN, SIMO Input Logic High	V_{IO_IH}		1.4			V
SDA, SCL, EN, DVSIN, CLKIN, SIMO Input Logic Low	V_{IO_IL}				0.4	V
$\overline{INT}$ Output Logic Low	$V_{IO\_OL\_INT}$	I_{OL} = 4mA			0.4	V
SDA Output Logic Low	$V_{IO\_OL\_SDA}$	I_{OL} = 20mA			0.4	V
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		0.5			µs
START Condition Repeated Hold Time	t_{HD_STA}		0.26			µs
Low Period of SCL Clock	t_{LOW}		0.5			µs
High Period of SCL Clock	t_{HIGH}		0.26			µs

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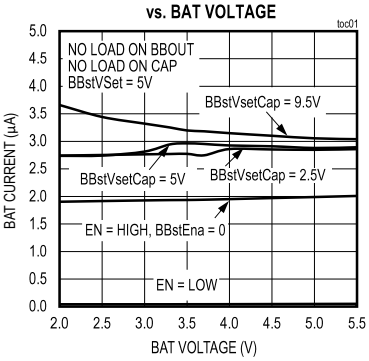
PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Setup Time for a Repeated START Condition	t_{SU_STA}		0.26			µs
Data-Hold Time	t_{HD_DAT}		0			µs
Data-Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}		50			ns
DATA Valid Time	t_{VD_DAT}				450	ns
DATA Valid ACK Time	t_{VD_ACK}				450	ns
DVS Interface						
CLKIN Frequency	f_{CLKIN}				20	MHz
DVSIN Setup Time	t_{DS}		10			ns
DVSIN Hold Time	t_{DH}		20			ns
CLKIN Pulse-Width Low	t_{LOW_SPI}		20			ns
CLKIN Pulse-Width High	t_{HIGH_SPI}		20			ns

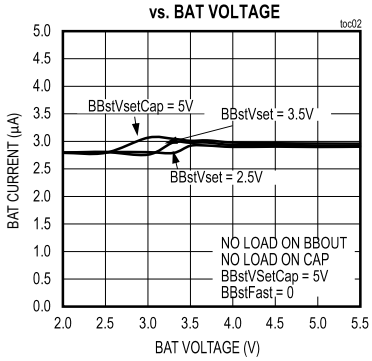
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{BAT} = 3.7V, C_{BBIN} = C_{BBOUT} = 22µF, V_{BBOUT} = 5V, BBstVSetCap = 5V, BBIngenDrop = 55mV, L = 2.2µH)

BAT QUIESCENT SUPPLY CURRENT vs. BAT VOLTAGE



BAT QUIESCENT SUPPLY CURRENT vs. BAT VOLTAGE



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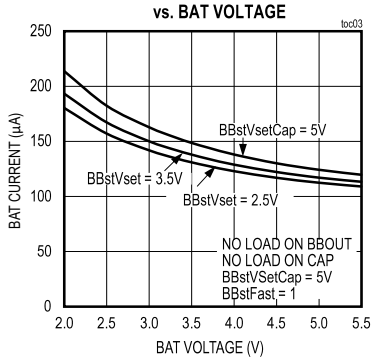
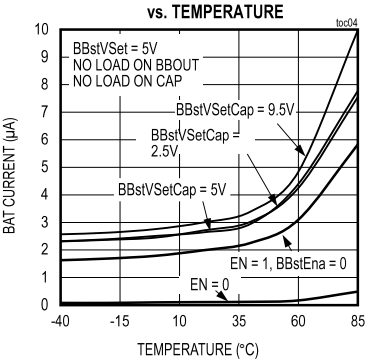
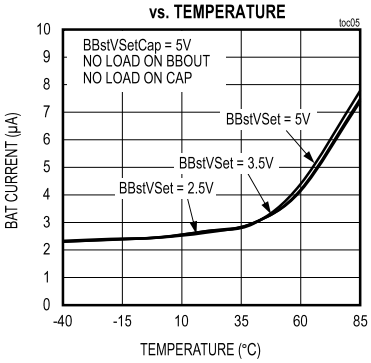


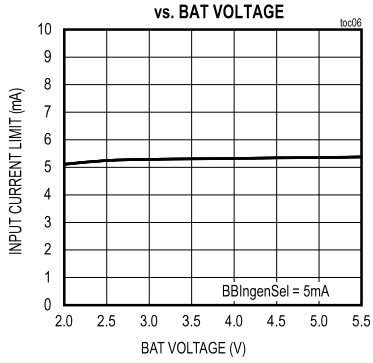
BAT SUPPLY CURRENT vs. TEMPERATURE



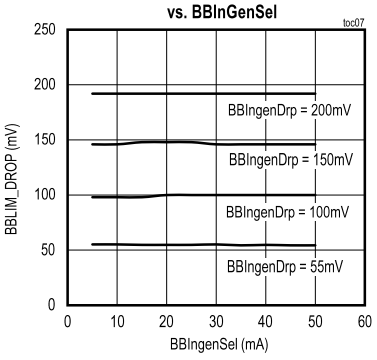
BAT SUPPLY CURRENT vs. TEMPERATURE



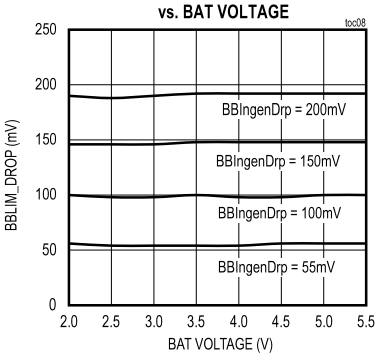
INPUT CURRENT LIMIT vs. BAT VOLTAGE



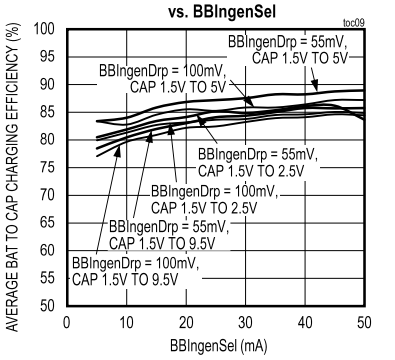
INPUT LIMITER REGULATED VOLTAGE DROP vs. BBInGenSel



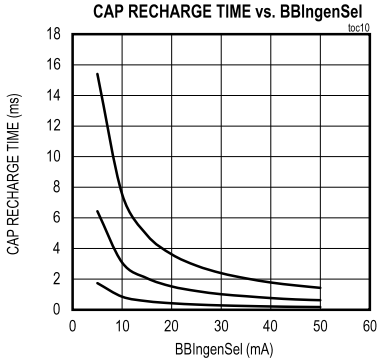
INPUT LIMITER REGULATED VOLTAGE DROP vs. BAT VOLTAGE



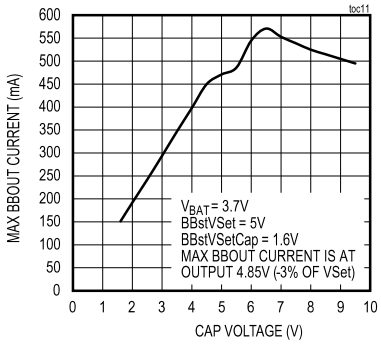
AVERAGE BAT TO CAP CHARGING EFFICIENCY vs. BBIngenSel



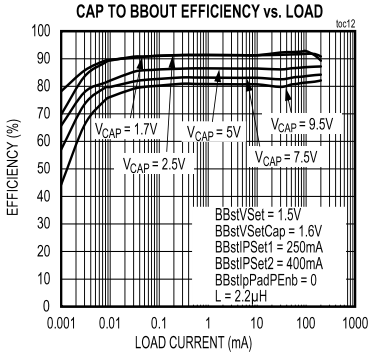
CAP RECHARGE TIME vs. BBIngenSel



MAX BBOUT CURRENT vs. CAP VOLTAGE



CAP TO BBOUT EFFICIENCY vs. LOAD



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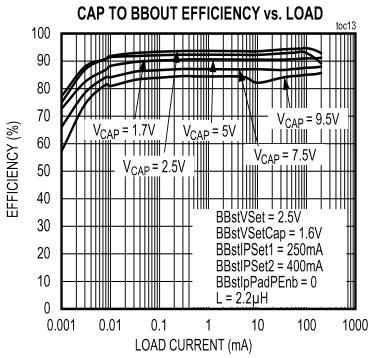
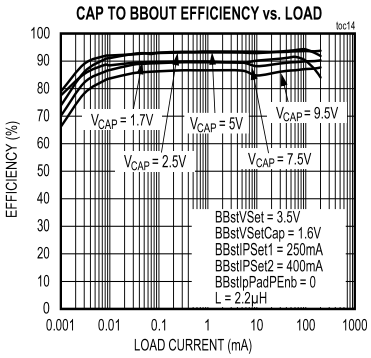
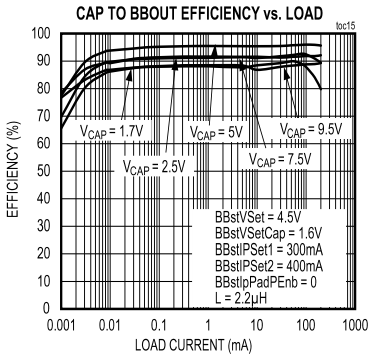


CAP TO BBOUT EFFICIENCY vs. LOAD



CAP TO BBOUT EFFICIENCY vs. LOAD



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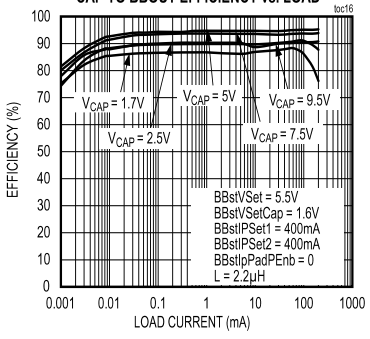
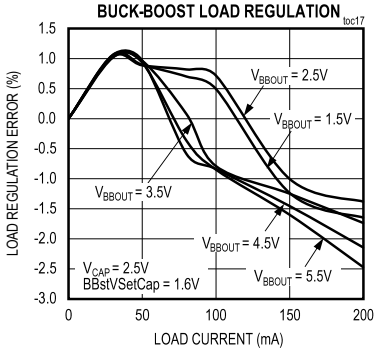


BUCK-BOOST LOAD REGULATION



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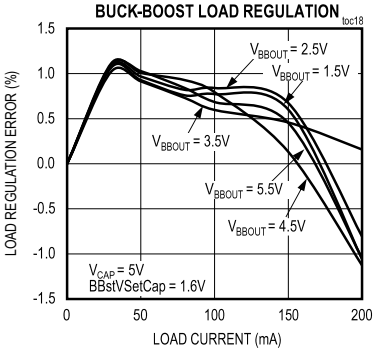
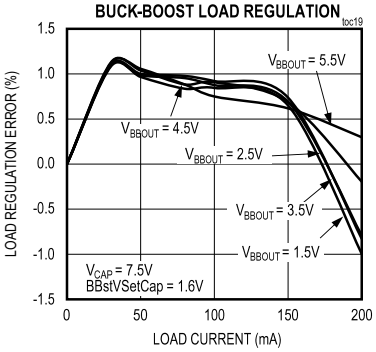
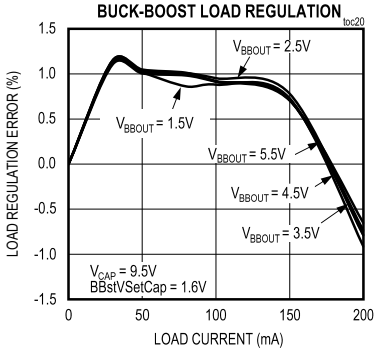


BUCK-BOOST LOAD REGULATION



BUCK-BOOST LOAD REGULATION



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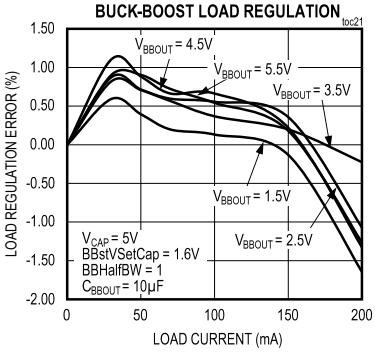
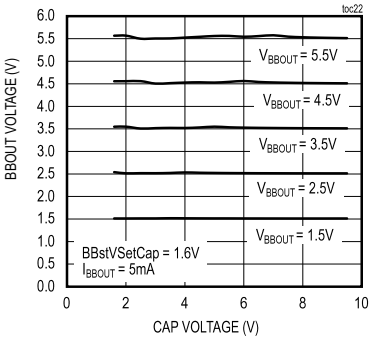
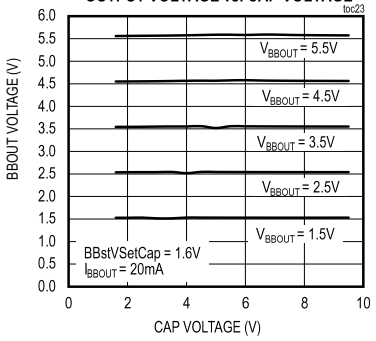


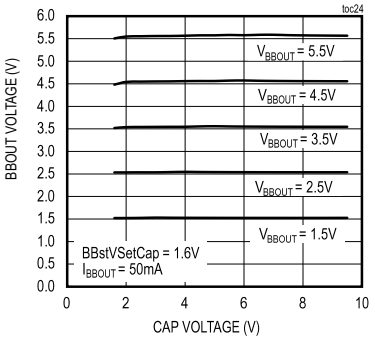
OUTPUT VOLTAGE vs. CAP VOLTAGE



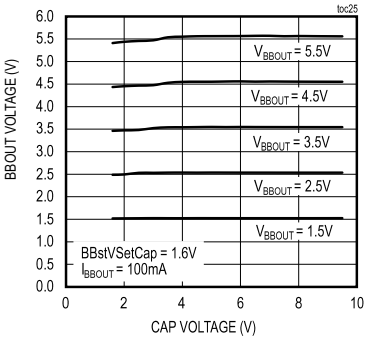
OUTPUT VOLTAGE vs. CAP VOLTAGE



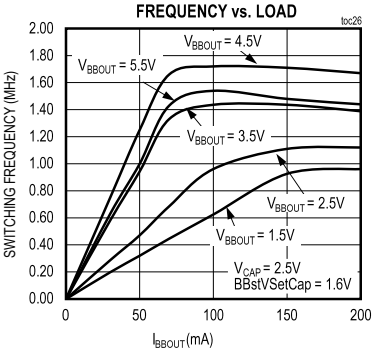
OUTPUT VOLTAGE vs. CAP VOLTAGE



OUTPUT VOLTAGE vs. CAP VOLTAGE



BUCK-BOOST SWITCHING FREQUENCY vs. LOAD



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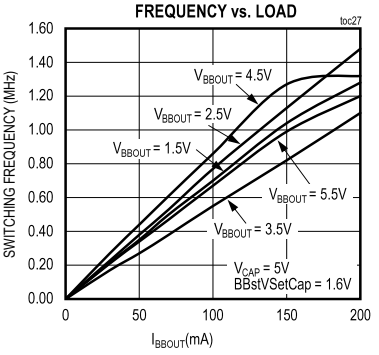

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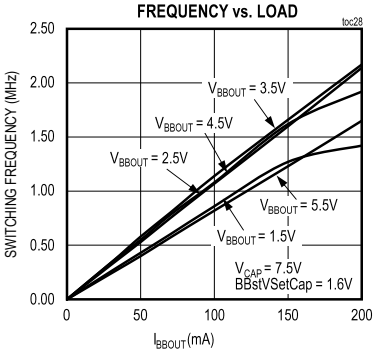

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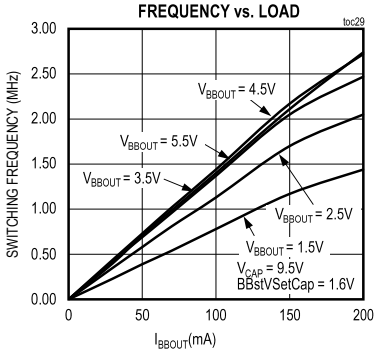
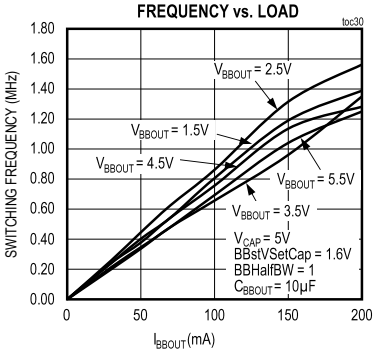
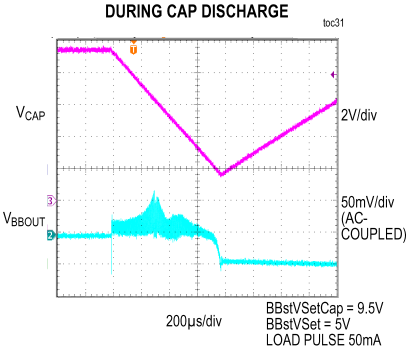


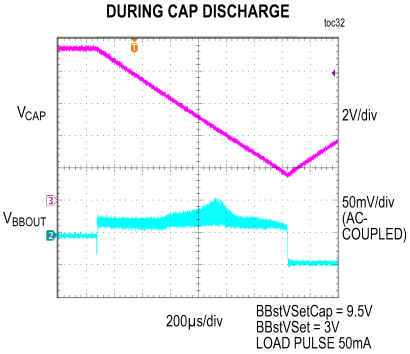
BUCK-BOOST SWITCHING FREQUENCY vs. LOAD



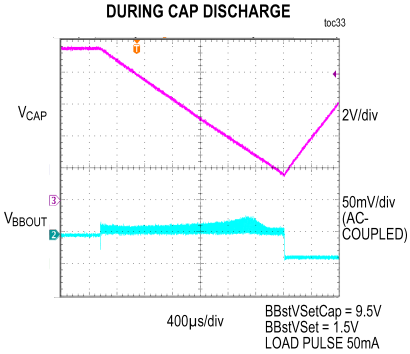
LOAD REGULATION AND RIPPLE DURING CAP DISCHARGE



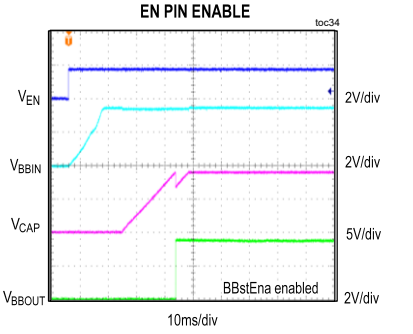
LOAD REGULATION AND RIPPLE DURING CAP DISCHARGE



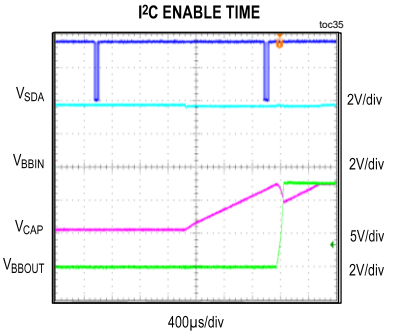
LOAD REGULATION AND RIPPLE DURING CAP DISCHARGE



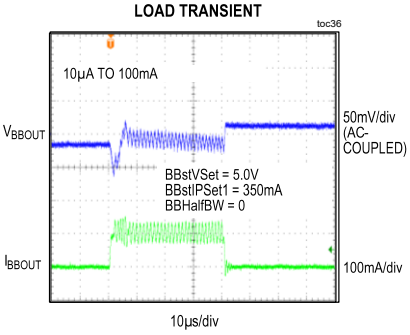
EN PIN ENABLE



I²C ENABLE TIME



LOAD TRANSIENT



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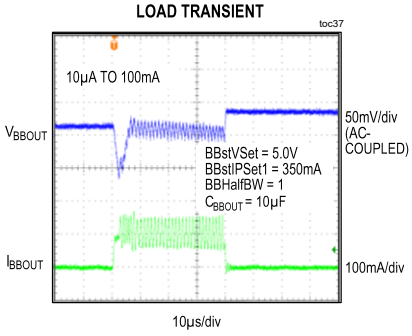
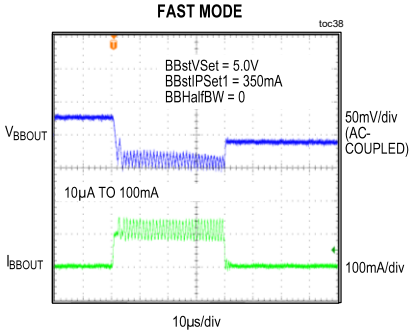
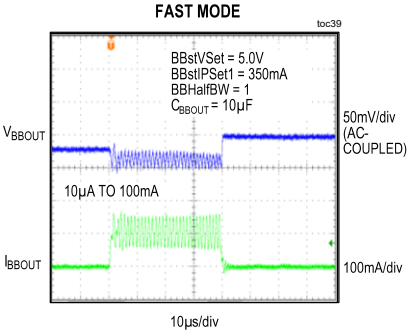


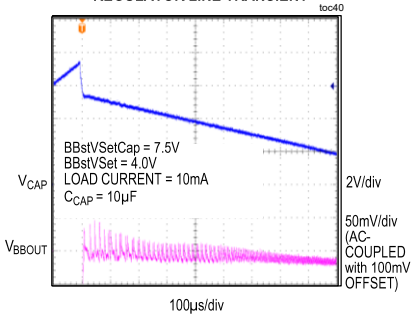
LOAD TRANSIENT WITH FAST MODE



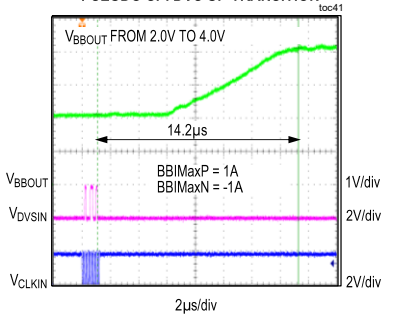
LOAD TRANSIENT WITH FAST MODE



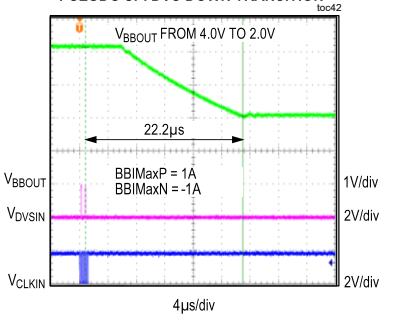
CAP TO BBOUT BUCK-BOOST REGULATOR LINE TRANSIENT



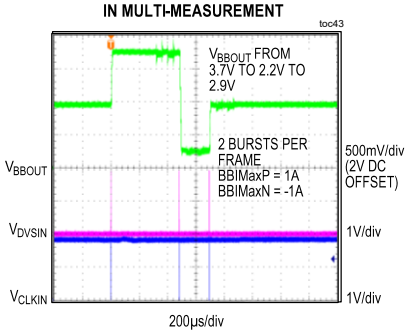
PSEUDO-SPI DVS UP TRANSITION



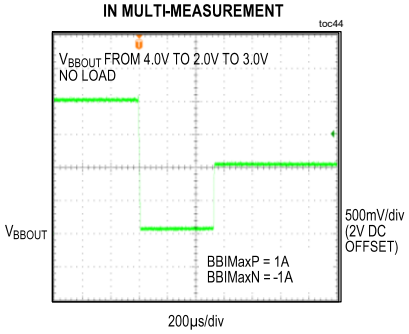
PSEUDO-SPI DVS DOWN TRANSITION



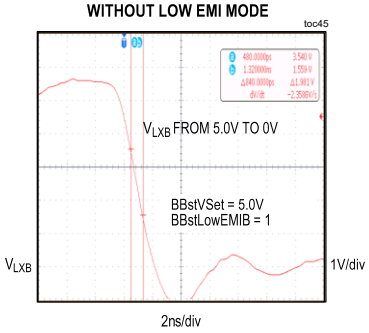
PSEUDO-SPI DVS TRANSITIONS IN MULTI-MEASUREMENT



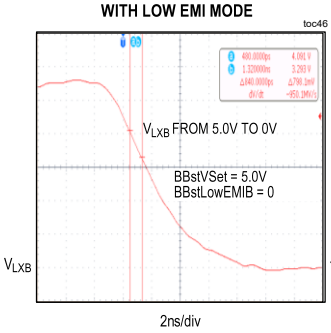
ROUND-ROBIN DVS TRANSITIONS IN MULTI-MEASUREMENT



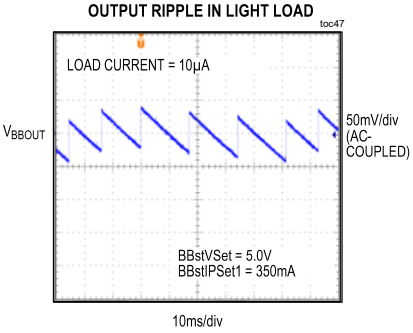
LXB DOWN TRANSITION WITHOUT LOW EMI MODE



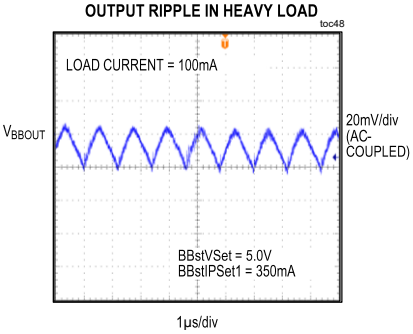
LXB DOWN TRANSITION WITH LOW EMI MODE



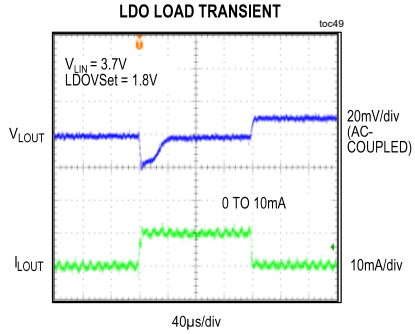
OUTPUT RIPPLE IN LIGHT LOAD



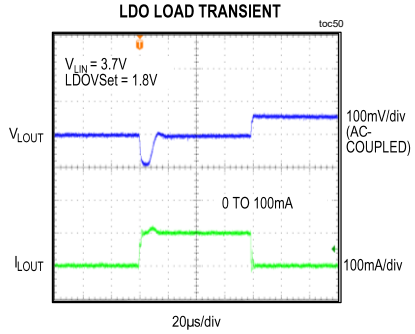
OUTPUT RIPPLE IN HEAVY LOAD



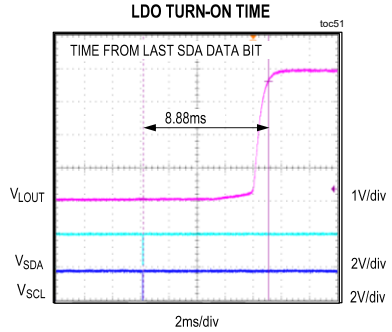
LDO LOAD TRANSIENT



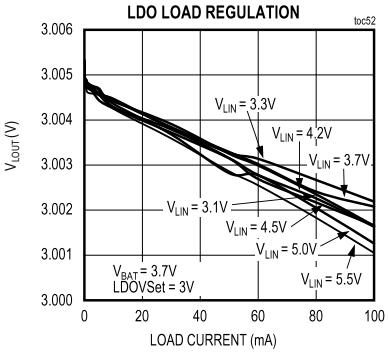
LDO LOAD TRANSIENT



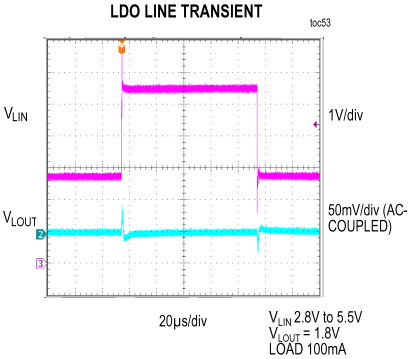
LDO TURN-ON TIME



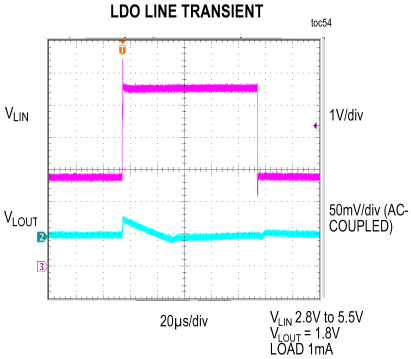
LDO LOAD REGULATION



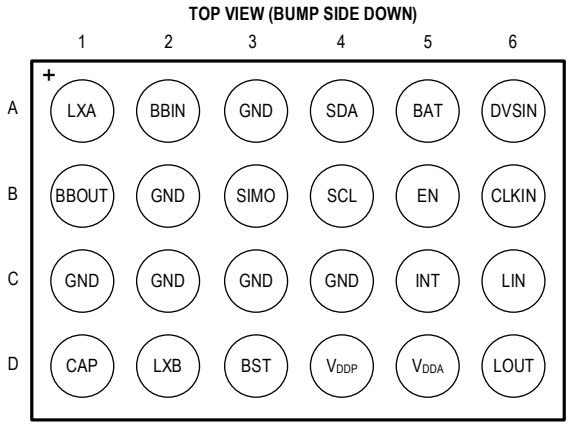
LDO LINE TRANSIENT



LDO LINE TRANSIENT



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



24-BUMP 0.4mm-PITCH WLP
(2.56mm x 1.72mm)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
A1	LXA	Buck-boost regulator switching node A. Connect to LXB through a 1µH or 2.2µH inductor (set BBL2P2Sel accordingly). See the *Inductor Selection* guide for more information.
A2	BBIN	Current-limited buck-boost input. Bypass with a capacitor to GND. See the *BBIN Capacitor Selection* section for guidance on capacitor selection for this node.
A3, B2, C1, C2, C3, C4	GND	Ground. Connect all ground bumps and bypass capacitances together with a low-impedance plane.
A4	SDA	I^2C serial data input/output.
A5	BAT	Battery input. Bypass with a 1µF capacitor to GND.
A6	DVSIN	Dedicated DVS interface data input. Connect to compatible PPG AFE. Connect to ground if unused.
B1	BBOUT	Buck-boost regulator output. The BBOUT node must be bypassed with sufficient capacitance to guarantee proper operation. See the *BBOUT Capacitor Selection* section for capacitance requirements.
B3	SIMO	SIMO digital input. If pulled high, the arbiter gives inductor preference to BBOUT for optimal regulation. If tied low, the BBSimoSel bit controls the arbitration mode. See the *BBIN to CAP and CAP to BBOUT Buck-Boost Interoperation* section for more information. The SIMO pin should not be changed in pseudo-SPI or round-robin DVS mode.
B4	SCL	I^2C Serial Clock Input.

B5	EN	Active-high enable input. For the lowest shutdown current, pull EN low. If shutdown current is unimportant, BBstEna in register 0x01 can be used. The EN pin takes precedence over the BBstEna setting. When EN is low, all registers are reset.
B6	CLKIN	Dedicated DVS interface clock input. Connect to compatible PPG AFE. Connect to ground if unused.
C5	$\overline{INT}$	Active-low, open-drain interrupt output. Pull-up to logic supply through ≥1kΩ resistor.
C6	LIN	LDO Input. Bypass with a 1µF capacitor to GND. To take advantage of the input current limit function, LIN can be connected to BBIN. If this approach is taken, a current limit of 10mA or higher must be selected to ensure proper startup of the LDO. The user is responsible to ensure that the loading on the LDO does not prevent recharge of the CAP node. If LDO is not used, connect LIN and LOUT to ground.
D1	CAP	Storage capacitor output. Connect capacitor between this node and GND. Ensure the capacitance is sized appropriately for the application. See the *CAP Node Tank Capacitance Selection* section for more details on sizing the storage capacitor.
D2	LXB	Buck-boost regulator switching node B. Connect to LXA through a 1µH or 2.2µH inductor (set BBL2P2Sel accordingly). See the *Inductor Selection* guide for more information.
D3	BST	Bootstrap node. Connect a 100nF capacitor between BST and LXB.
D4	V_{DDP}	Internal 1.8V supply bypass node. Connect 1µF between this node and GND. This output is not intended to power any external circuitry.
D5	V_{DDA}	Internal analog 1.8V supply output. Connect 1µF between this node and GND. This output is not intended to power any external circuitry.
D6	LOUT	LDO Output. Bypass with 1µF of capacitance to GND.

THEORY OF OPERATION

System design constraints, such as physical size and battery self-discharge limits, often force designers to select batteries for their systems that are not capable of providing the instantaneous power required for some peak loads. In such cases, the first instinct is to place a large capacitance in parallel with the battery to filter some peak currents, but the current in that case is filtered only by the RC low-pass filter (LPF) formed by the battery impedance and the bypass capacitance. In many cases, this makes placing a parallel capacitance impractical due to the size/amount of capacitance required.

Often, the next instinct for designers is to place the storage capacitance on the output of a current-limited supply (either a linear or switching current limiter). In this case, the theory is that peak loads can be handled by the capacitor, allowing it to droop during the loading event. The capacitor is subsequently recharged, but the battery is protected from high currents by the current limiter. This case presents the designer with a conundrum: either the load being supplied must be tolerant of large voltage ranges and droop during a loading event, or the designer must drastically oversize the capacitor to minimize the supply droop. However, system constraints often make this a suboptimal solution.

The MAX20362 architecture resolves this issue by elegantly utilizing a single inductor to provide current-limited charging of an isolated tank capacitance and to subsequently delivering the charge stored on that tank capacitance to a low-noise, regulated output. By isolating the capacitor from the load, the MAX20362 can charge the tank capacitance up to 9.5V, taking advantage of the fact that the energy stored on a capacitor goes with the square of the voltage ($E = \frac{1}{2} C \times V^2$). Therefore, the system designer can place a smaller capacitance to store the same amount of energy. Additionally, by isolating the tank capacitance from the output, droop on the supply during loading events is eliminated, as the tank capacitance may be drawn down while the BBOUT output voltage remains steady. This means that the tank capacitance can be sized minimally without sacrificing system performance. The low minimum CAP voltage of 1.5V ensures that the device can extract maximal stored energy from the capacitor.

In PPG systems, placing the capacitor at a separate node from the load also allows the MAX20362 to dynamically scale the output voltage at BBOUT by recovering the charge from the BBOUT capacitor and placing it back on the CAP tank capacitance. This allows for the quick scaling of the voltage at the anode of PPG LEDs to minimize headroom and improve system efficiency. See the *Optical DVS* section for more information.

Switching Converter Architectural Description

Conceptually, there are two switching DC-DC regulators implemented in the MAX20362. The first converter, as shown in *Figure 1*, is used to provide input current-limited charging from the battery to the CAP node. The second converter as shown in *Figure 2*, regulates the output voltage at BBOUT from the reservoir capacitance at the CAP node. At a high level, it is useful to first consider these regulators and their operation independently, then to consider the interaction between the two regulators. The independent operation of the converter which is used to charge the CAP node is described in the *Input Current Limiter and BBIN to CAP Buck-Boost Converter* section, followed by a description of the *CAP to BBOUT Buck-Boost Converter* section. Finally, the joint operation of these converters is described in the *BBIN to CAP and CAP to BBOUT Buck-Boost Interoperation* section. Passive component selection and recommendations are covered in the *Applications Information* section.

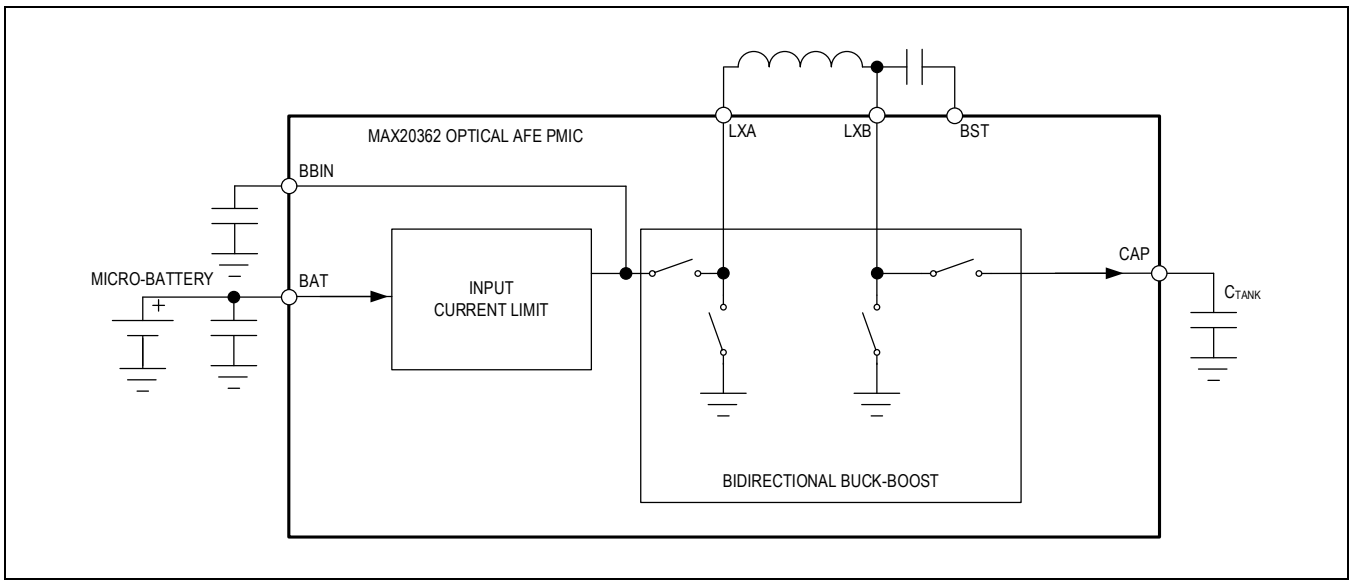


Figure 1. BBIN to CAP Buck-Boost Converter

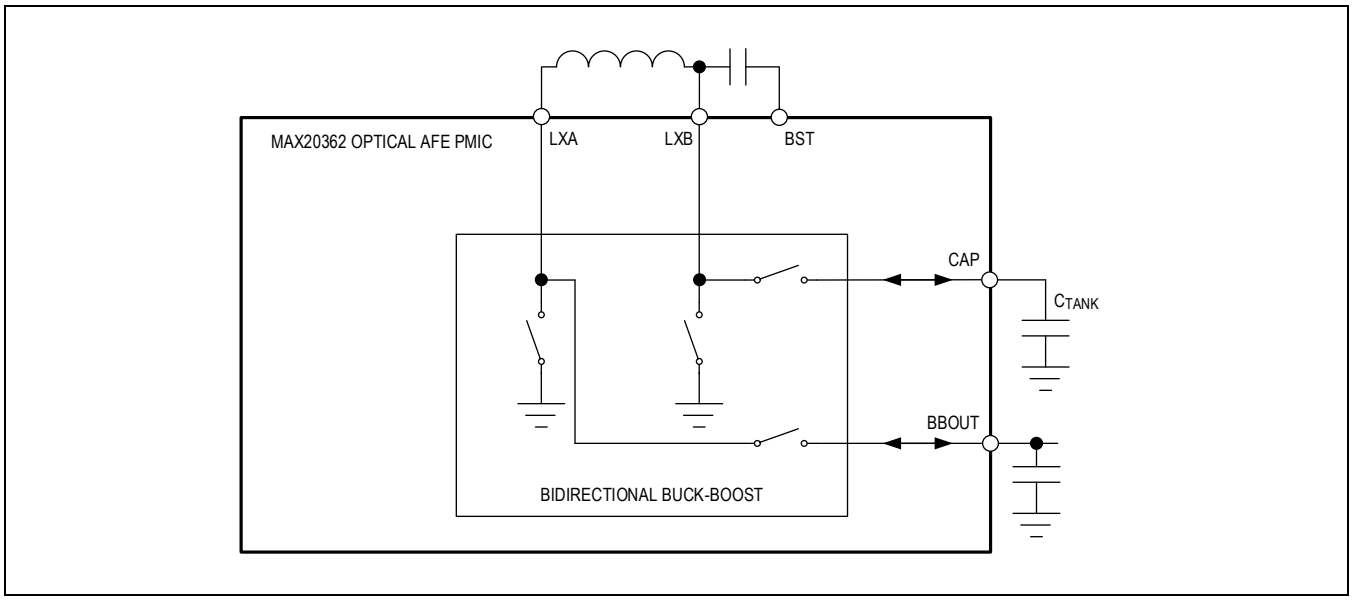


Figure 2. CAP to BBOUT Buck-Boost Converter

Input Current Limiter and BBIN to CAP Buck-Boost Converter

Figure 3 illustrates the basic structure of the MAX20362 BAT to CAP input current-limited switching regulator. The arrows, labeled 1-4 depict the inductor current flow in each switching phase of the buck-boost regulator and are described in detail in the *Switching Phases* section. During regulation, the buck-boost limits the input by modulating its switching frequency, as described in the *Input Current Limiting* section. The buck-boost charges the CAP capacitance to the voltage set by BBstStepCap and BBstVSetCap, allowing the user a wide range of flexibility and high output voltage regulation accuracy. The voltage at CAP can be set in a range from 1.6V to 9.5V with varying resolution depending on the range. See the BBstStepCap and BBstVSetCap register descriptions for more details.

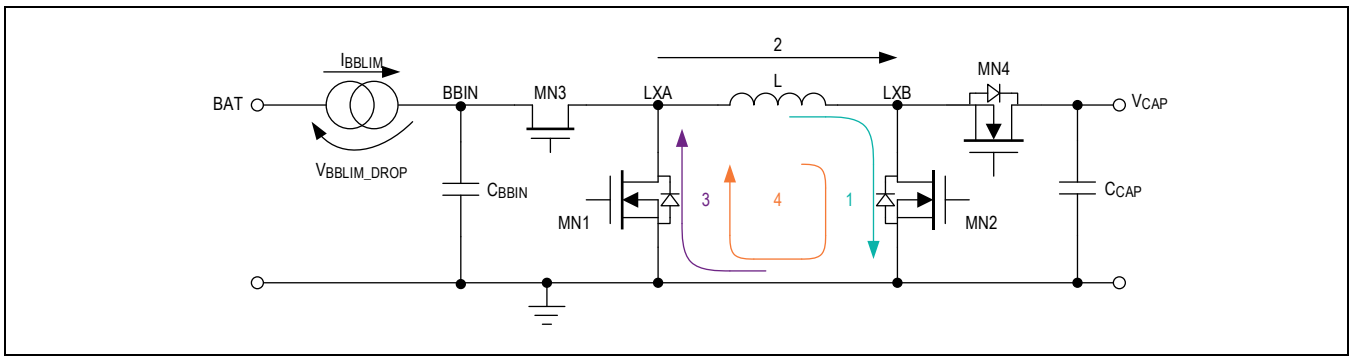


Figure 3. The Buck-Boost Regulator and Switching Phases

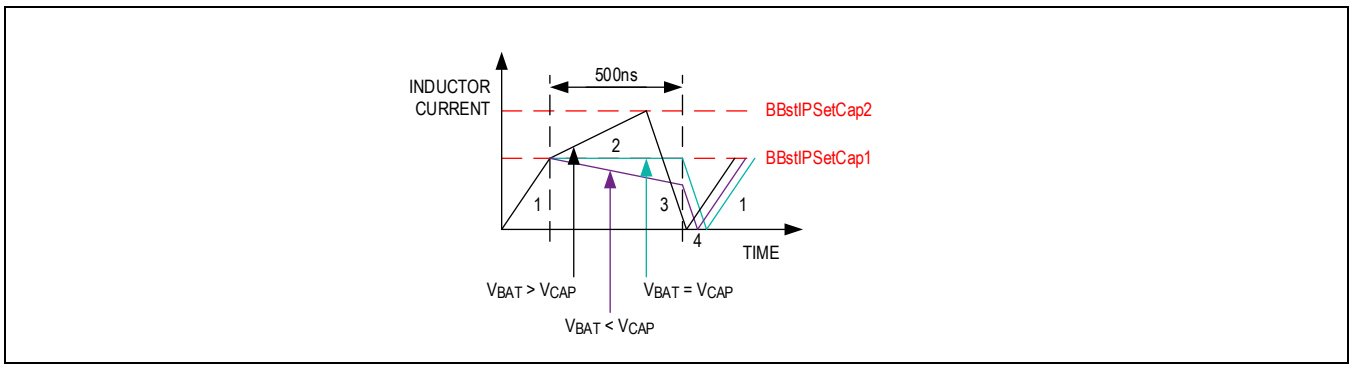


Figure 4. Buck-Boost Inductor Current in Buck-Boost Mode

Switching Phases

Depending on the input and output voltage conditions, the buck-boost executes different sequences of switching phases to generate the desired output voltage. Only two switches are turned on during each phase.

- Phase 1: MN2 on, MN3 on. Inductor charges.
- Phase 2: MN3 on, MN4 on. Inductor charges when $V_{BAT} > V_{CAP}$, discharges when $V_{BAT} < V_{CAP}$.
- Phase 3: MN1 on, MN4 on. Inductor discharges.
- Phase 4: MN1 on, MN2 on. Freewheeling.

Buck, Buck-Boost, and Boost Conditions

The regulator operates in buck mode when the input voltage is substantially greater than the output voltage and in buck-boost mode when the input voltage and output voltage are very close. To minimize discontinuities in the output-voltage ripple during transitions between buck, buck-boost, and boost modes, the switching sequence remains always the same between the modes. First, the inductor charges in phase 1 up to BBstIPSetCap1. The buck-boost then transitions to phase 2. If $V_{BAT} > V_{CAP}$, BBstIPSetCap1 is gradually reduced to 0, and the inductor charges until either the current reaches BBstIPSetCap2 or after a 500ns delay. When the inductor current reaches zero-crossing, the regulator freewheels in phase 4 until the next charge phase. When operating in continuous conduction mode (CCM), the buck-boost enters phase 4 for approximately 30ns. *Figure 4* shows the inductor current in each mode.

Inductor Peak Current Limit

The buck-boost regulator monitors the maximum and minimum values of the inductor current. Peak currents are set in the BBstISetCap register. BBstIPSetCap1 controls the peak current when $V_{BBIN} < V_{CAP}$ and begins the timeout period for phase 2. BBstIPSetCap2 sets a secondary current limit in buck-boost mode that is reached when $V_{BBIN} > V_{CAP}$. The total inductor current limit when $V_{BBIN} > V_{CAP}$ can be as high as BBstIPSetCap1+BBstIPSetCap2. The buck-boost regulator transitions from phase 2 to phase 3 if the inductor current reaches BBstIPSet2 or if the 500ns timeout has elapsed. As the buck-boost enters boost mode, eventually there comes a point where the inductor current reaches 0 before the 500ns timer expires. In this case, phase 3 is skipped to maintain high efficiency.

It is recommended to keep the default BBstIPSetCap1/2 settings (350mA) for optimal efficiency. If the decision is made to adjust these values, the minimum BBstIPSetCap2 should never be lower than 200mA to avoid unwanted behavior.

Input Current Limiting

The MAX20362 BAT to CAP buck-boost must protect the battery from excessive currents of downstream loads. In this architecture, large loads are serviced from the CAP node, but charging the CAP capacitance itself results in large currents with a regular switching converter. This device features an input current-limiting scheme that protects the battery while quickly and efficiently charging the CAP node capacitance. The input current limitation is accomplished using the circuit of *Figure 5*. A linear current generator, sitting between BAT and BBIN, actively limits the current to a value between 5mA and 50mA, set by BBIngenSel in 1mA steps. The buck-boost input current is controlled by modulating the switching frequency of the buck-boost based on the voltage drop between BAT and BBIN. As the capacitance at BBIN discharges, a comparator watches the difference between BAT and BBIN. When the difference exceeds the programmable threshold (50mV, 100mV, 150mV, or 200mV) set by BBIngenDrp, the comparator signals the buck-boost to stop switching activity. When the difference is below the programmable threshold, the comparator signals the buck-boost to initiate a new switching cycle (assuming V_{CAP} is not already at regulation value). In this way, not only is the average current from the battery limited, but even the large peak currents taken by the inductor are filtered by the input current generator. This allows for very precise control over the maximum current drawn from the battery, which protects the battery from damage and prevents other components powered by the battery from experiencing unwanted undervoltage conditions. To maintain the highest efficiency, it is recommended that the BBIngenDrp setting be kept at the lowest setting.

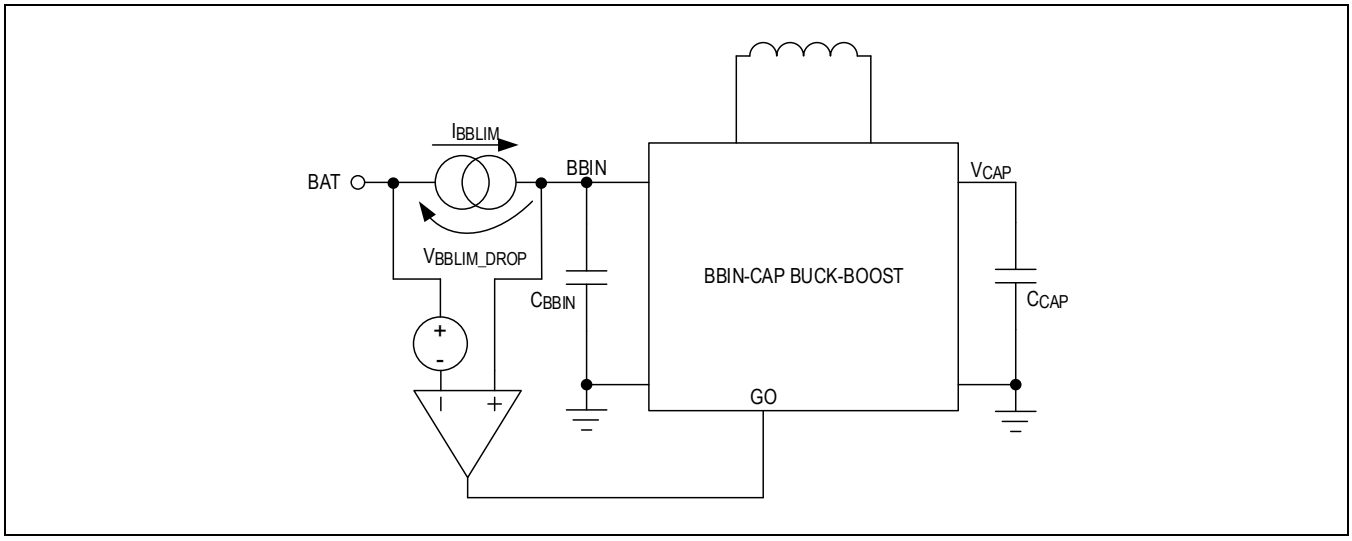


Figure 5. Input Current Limiter Topology

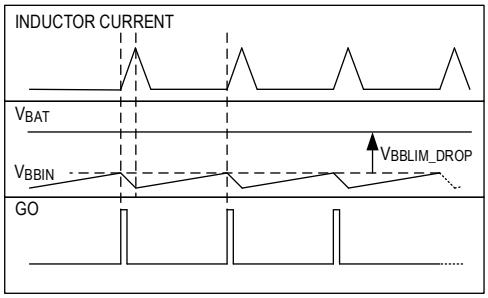


Figure 6. Input Current Limit Operation

CAP to BBOUT Buck-Boost Converter

The MAX20362 is an ultra-low quiescent current, non-inverting buck-boost converter with 128mA output current capability. The converter employs a control algorithm that seamlessly transitions between buck, buck-boost, and boost modes, minimizing discontinuities and subharmonics in the output-voltage ripple. The low 1.5V input voltage allows the device to maximize the energy extracted from the CAP storage element. The CAP to BBOUT converter has been designed to minimize the noise impact of voltage ripple on sensitive downstream subsystems such as PPG LEDs.

The ultra-fast dynamic voltage scaling (DVS) capability allows the device to transition quickly between output voltages and enable in-frame scaling of LED supply voltage when used in conjunction with capable PPG AFEs. Additionally, the low output ripple and fast, predictable transient response maximizes the SNR of high-performance optical PPG AFEs.

Figure 7 illustrates the basic structure of the MAX20362 switching regulator with arrows depicting the inductor current flow in each switching phase.

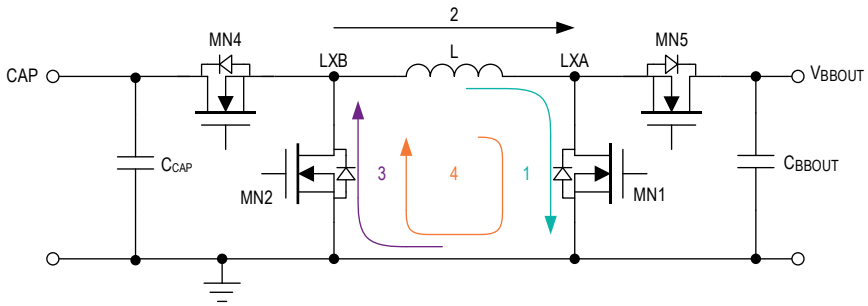


Figure 7. Buck-Boost Regulator and Switching Phases

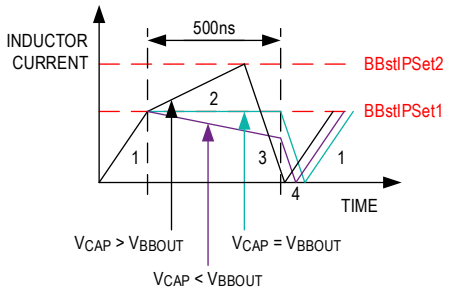


Figure 8. Buck-Boost Inductor Current in Buck-Boost Mode

Switching Phases

Depending on the buck-boost configurations, the topology enters different sequences of phases to generate the desired output voltage. Only two switches are turned on during each phase.

- Phase 1: MN4 on, MN1 on. Inductor charges.
- Phase 2: MN4 on, MN5 on. Inductor charges when $V_{CAP} > V_{BBOUT}$, discharges when $V_{CAP} < V_{BBOUT}$.
- Phase 3: MN2 on, MN5 on. Inductor discharges.
- Phase 4: MN1 on, MN2 on. Freewheeling.

Buck, Buck-Boost, and Boost Conditions

The regulator operates in buck mode when the input voltage is substantially greater than the output voltage and in buck-boost mode when the input voltage and output voltage are very close. To minimize discontinuities in the output-voltage ripple during transitions between buck, buck-boost, and boost modes, the switching sequence remains always the same between the modes. First, the inductor charges in phase 1 up to BBstIPSet1. The buck-boost then transitions to phase 2. If $V_{CAP} > V_{BBOUT}$, BBstIPSet1 is gradually reduced to 0, and the inductor charges until either the current reaches BBstIPSet2 or after a 500ns delay. When the inductor current reaches the valley-current crossing threshold or falls below 0, the regulator freewheels in phase 4 until the next charge phase. When operating in continuous conduction mode (CCM), the buck-boost enters phase 4 for approximately 30ns. *Figure 9* shows the inductor current in each mode.

Inductor Peak and Valley Currents

The buck-boost regulator monitors the maximum and minimum values of the inductor current. If BBstIPAdptDis = 1, the peak currents are fixed to the values in BBstISet and the valley current is fixed to 0mA. If BBstAdptDis = 0, the peak and valley currents are allowed to change based on load requirements.

Peak currents are set in the BBstISet register. BBstIPSet1 controls the peak current when $V_{CAP} < V_{BBOUT}$ and begins the timeout period for phase 2. BBstIPSet2 sets a secondary current limit in buck-boost mode when $V_{CAP} > V_{BBOUT}$. The buck-boost regulator transitions from phase 2 to phase 3 if the inductor current reaches BBstIPSet2 or if the 500ns timeout has elapsed. The MAX20362 gradually reduces BBstIPSet1 such that, when BBstIPSet2 is reached, the BBstIPSet1 is 0. Minimizing the settings of BBstIPSet1 and BBstIPSet2 reduces output ripple but decreases efficiency. Care must be taken to optimize the peak current settings to maintain a low output ripple while maximizing efficiency. The Minimum BBstIPSet2 should never be set lower than 200mA to avoid unwanted behavior. *Figure 9* is a graphical guide for selecting combinations of BBstIPSet1 and BBstIPSet2 to balance efficiency for specific BBstVSet values.

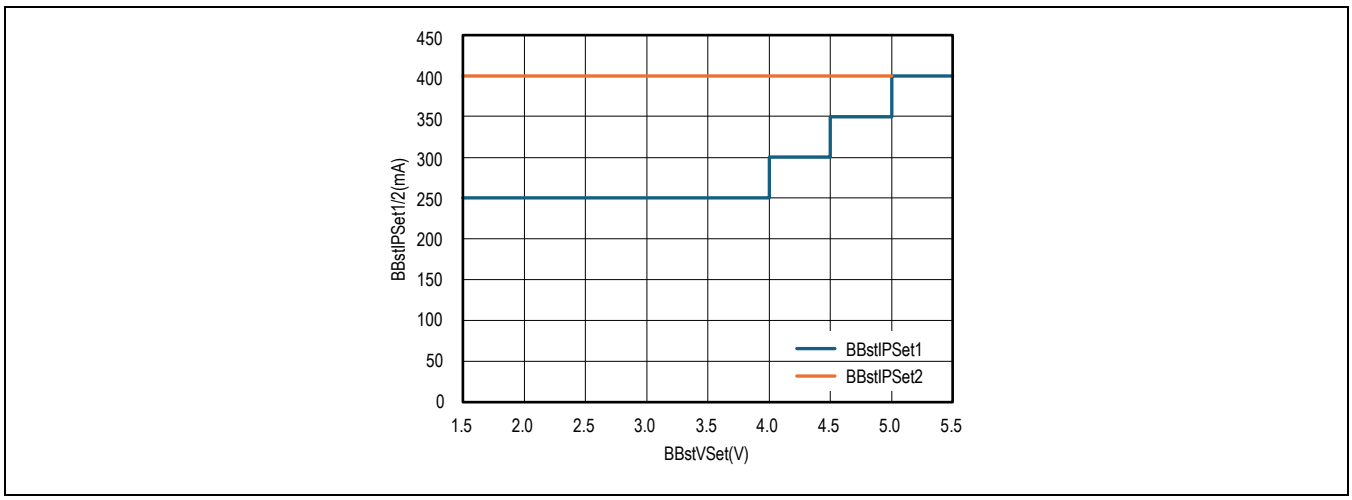


Figure 9. Recommended BBstIPSet1 and BBstIPSet2 Settings

Optical DVS

The MAX20362 utilizes DVS to rapidly change the output voltage on demand. DVS can significantly reduce the power consumption of PPG systems that use LEDs with highly variable forward voltage drops.

Buck-Boost Operation During Fast Dynamic Voltage Scaling Operations

DVS voltage transitions can be positive (output voltage increasing) or negative (output voltage decreasing). To accomplish a positive transition, the buck-boost follows the same switching sequence as described in the *CAP to BBOUT Buck-Boost Converter*, *Switching Phases*, *Buck, Buck-Boost, and Boost Conditions*, and *Inductor Peak and Valley Currents* sections, but it regulates the inductor current at a fixed valley current, as shown in *Figure 10*. The valley current regulated can be adjusted using the BBIMaxP register to values from 0 to 1.1A in 50mA steps. Higher settings lead to increased transition speeds but may result in more ohmic losses during the transition. The speed of the transition should be set by $I = C\frac{dV}{dt}$ to ensure that, for a given BBOUT capacitance, the voltage transition rate is fast enough for the voltage to reach the target within the time required by the application.

Negative DVS transitions force the inductor current in the opposite direction, regulating a reverse current from BBOUT to CAP based on the BBIMaxN setting, as shown in *Figure 11*. By reversing the current in this way, much of the energy pulled from BBOUT during the downward transitions is recovered and can be used for future regulation and DVS positive transitions on BBOUT. This greatly improves the efficiency of the system during DVS events. Similar to a positive transition, BBIMaxP must be set to ensure that the transition occurs within the time allotted by the application. Special care must also be taken to ensure that a negative DVS transition does not overfill the CAP capacitor. An OVLO circuit exists on CAP, which disallows further charging if a negative DVS transition overfills the capacitance. This means that the negative DVS transition is stopped even if the transition to the new regulation voltage has not been completed.

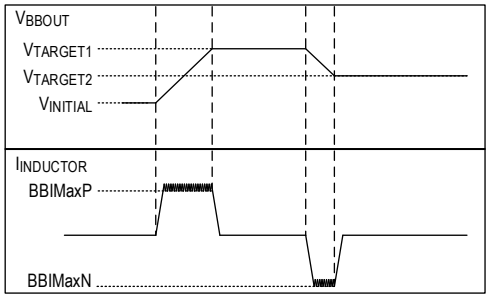


Figure 10. Positive and Negative DVS Transitions

Dynamic Voltage Scaling (DVS) Modes

The MAX20362 features three different DVS control modes:

- I²C: In I²C mode, a dedicated register (BBstVset, register 0x02) in the regmap can be written with the voltage value required.
- Pseudo-SPI: Two dedicated pins (CLKIN, DVSIN) are used to implement a serial digital interface for passing the DVS voltages and additional information. This mode requires the use of a compatible AFE device that features DVS capability and a pseudo-SPI controller, such as the Analog Devices MAX86181.
- Round-Robin: Up to 20 FPWM and voltage values are pre-programmed through the I²C interface. These values are cycled through in succession at each rising/falling edge of the CLKIN pin. This control mode can be utilized with Analog Devices AFEs that feature multiple interrupt output pins, such as the MAX86180, and the ability to set the interrupt to trigger on changes in the 'FIFO Data Ready' status bit.

Table 5. DVS Mode

DVSSource	RREna	MODE
0	0	I²C DVS
1	0	Pseudo-SPI
X	1	Round-Robin

X = Don't care.

I²C Based DVS Control

If the RREna and DVSSource bits are set to zero, the DVS output voltage is set directly through I²C using bits 6-0 of register 0x02, BBstVset, and can be used to dynamically program the output voltage value. Use bits 6-0 of register 0x1E to read back the BBstVset value. Bit 7 of register 0x02, BBstFpwm, enables the FPWM feature, whereas bit 4 of register 0x01, BbstFast, enables the FAST feature. Note that I²C is the only mode where both of these two features can be enabled together. Bit FpwmFast of register 0x6E selects the feature for status check (0 = Fast, 1 = FPWM), and bit 7 of register 0x1E, BB_LOWBP, reads back the feature status (0 = disabled, 1 = enabled). For example, if FpwmFast = 1 and BBstFpwm = 1, then BB_LOWBP reads back 1 regardless of the BBstFast value. On the other hand, if FpwmFast = 1, BBstFpwm = 0, and BBstFast = 1, then BB_LOWBP reads back 0 even the FAST feature is enabled. Note that bit FpwmFast has no effect on setting high-performance feature in I²C mode.

In round-robin and in pseudo-SPI, only FPWM or FAST can be enabled. To choose which one, use read-write bit FpwmFast (register 0x06E, bit 0) (0 = Fast, 1 = FPWM). BB_LOWBP reads back 1 if either of the high-performance features is enabled. In round-robin mode, use each RRLowPBxx bit to disable/enable the high-performance feature for that cycle. If RRLowPBxx = 0, neither FPWM nor FAST is enabled. If RRLowPBxx = 1, FPWM or FAST is enabled

according to FpwmFast bit, and BB_LOWPB reads back 1. In pseudo-SPI mode, the serial communication protocol includes a bit (for example, bit DVS_MODE_SEL in MAX86181) that has the same function as RRLowPBxx. If DVS_MODE_SEL in MAX86181 is low, neither FPWM nor FAST is enabled. If DVS_MODE_SEL in MAX86181 is high, FPWM or FAST is enabled according to FpwmFast bit.

The BBstVSet register (0x02) features write protection that can be enabled or disabled by writing 0xAA or 0x55 to the LockUnlock register (0x51). For this write operation to take effect, the BBLck bit in register 0x50 must be 0; otherwise, the operation on LockUnlock is ignored. The BBstVSet register (0x02) is locked by default.

DVS Target Mode/Pseudo-SPI

When used with a compatible Analog Devices AFE, such as the MAX86181, the MAX20362 output voltage is controlled by a proprietary serial digital interface on the CLKIN and DVSIN pins. To enable this mode, the register bit DVSSource should be set to 1. Once enabled, 300µs is required until the device is ready to receive a new DVS command from the AFE controller. The default V_{BBOUT} in pseudo-SPI mode is 1.5 V.

In DVS target mode, the MAX20362 acts only as a target. All DVS values are programmed in the corresponding controller AFE. Register 0x19 (CommInt) contains the relevant interrupt bits for DVS target mode, indicating controller requests completion, interface timeout expiration, and parity error.

For additional information on the operation of DVS target mode, refer to the data sheet of the relevant DVS controller AFE device, such as MAX86181.

DVS Round-Robin Interface

The DVS round-robin mode allows the user to pre-program multiple DVS output voltages, which are cycled through on the rising/falling edge of the CLKIN signal (see the RRClkPolarity bit in the register map). This mode enables fast DVS output capability on Analog Devices AFEs that do not feature the DVS controller function.

To utilize round-robin mode:

- The user first programs up to 20 DVS voltage values into registers 0x20–0x33.
- If fewer than 20 registers are utilized, write register 0x55, RRSize to define which register location is the last one utilized.
- Configure RRWrap bit, in register 0x54, RRWrap, to determine if the round-robin pointer either remains on the final voltage register or return to location zero after reaching the final voltage value.
- Configure the RRTimeoutRes bit, register 0x55 to determine the device behavior after a timeout.
- Configure the RRClkPolarity bit for high/low-going edge triggering.
- Finally, enable the round-robin mode by writing 1 on the bit RREna (register 0x54, bit 1).

BBIN to CAP and CAP to BBOUT Buck-Boost Interoperation

The two buck-boost converters on MAX20362 share a single inductor. As such, these devices must cooperate to ensure non-overlap in the inductor utilization. There are multiple conditions to consider, but the built-in arbitration state machine simplifies the design for the end user and allows the system designer to focus on higher-level implementation.

Inductor Arbitration

To maintain low noise and keep ripple as consistent as possible on the BBOUT output, it is desirable to give preferential use of the inductor to the CAP to BBOUT converter. To achieve this preferential servicing of BBOUT, the arbiter first looks at requests from CAP and BBOUT for use of the inductor. BBOUT gets preferential access to the inductor, and once BBOUT has been serviced, a timeout must expire before CAP can be serviced. In this way, BBOUT

has free rein to request service during heavy loading intervals without needing to wait for the servicing of the BBIN to CAP buck-boost. One exception to this rule is that if CAP reaches the V_{CAP_MIN} threshold, the arbiter recognizes that BBOUT can no longer be sufficiently supported by CAP, and the CAP node gets equal access to the inductor for service.

Care must be taken to ensure that the BBIN to CAP converter has sufficient time to recharge the CAP node before subsequent BBOUT loading events.

If this behavior of the arbiter is undesirable, the SIMO pin can be pulled low and BBSimoSel set to 0. In this condition, the arbiter always serves BBOUT and CAP on a first-come, first-serve basis. Note that due to delays in the servicing of BBOUT, the voltage ripple does not have a fixed tone and may increase in amplitude.

Soft-Start

The soft-start behavior of MAX20362 requires cooperation of the two buck-boost converters. Since BBOUT is supported by CAP, the CAP node must be ramped first. Once it has been charged, the BBOUT node is charged from CAP. Since charging BBOUT discharges CAP, the CAP node must then be recharged before the startup sequence is complete. *Figure 11* graphically illustrates the startup sequence.

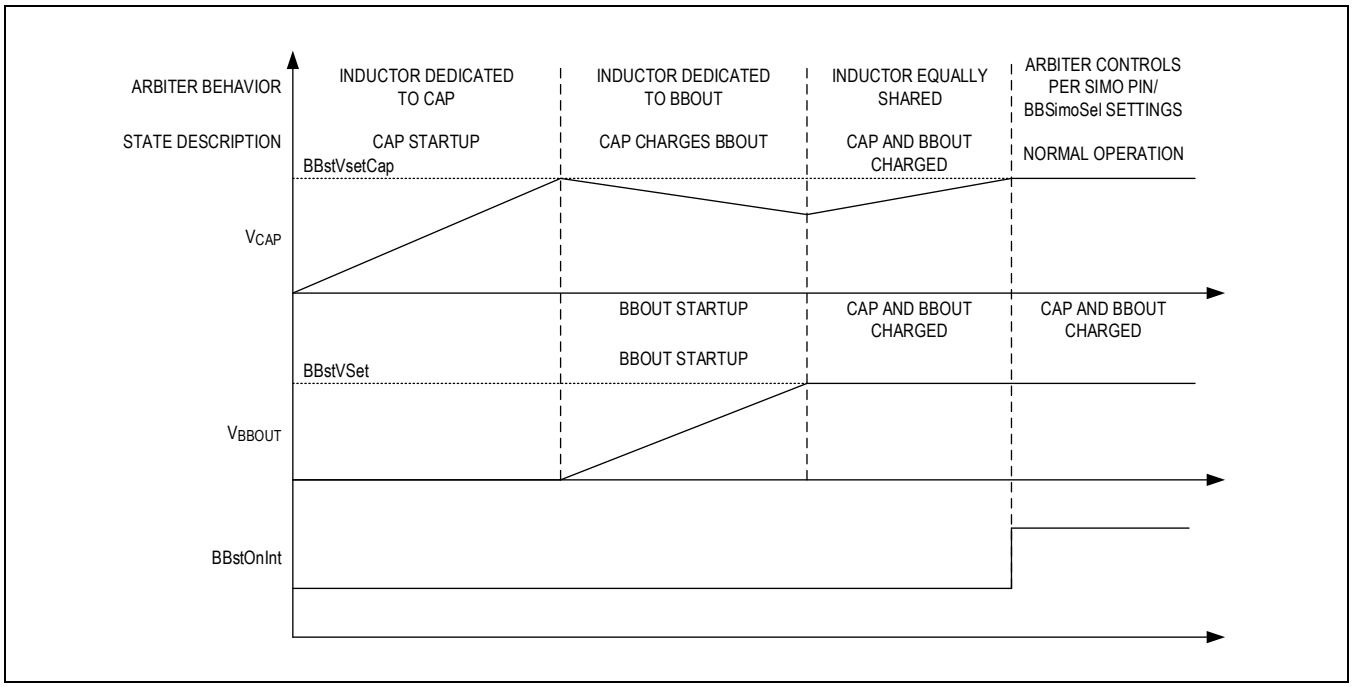


Figure 11. MAX20362 Startup Sequence

Fast Transient Response LDO

The LDO on the MAX20362 is designed to operate with a minimum of 1µF of effective capacitance on the output. Capacitance derating with DC voltage bias and other factors should be taken into consideration when selecting the capacitor. The LDOVSet cannot be changed when the LDO is enabled. LDOVSet voltage change is only effective after toggling LDOEna bit. *Figure 12* shows the recommended LOUT minimum and maximum effective capacitance.

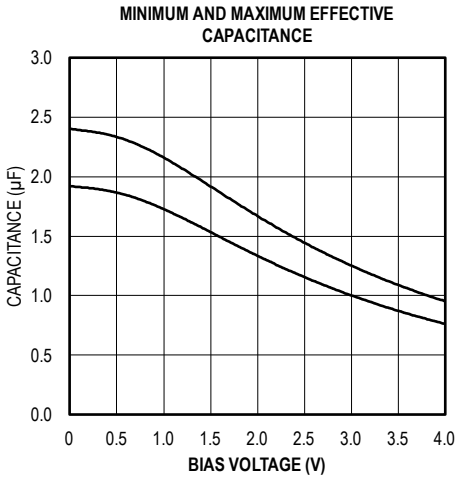


Figure 12. LOUT Recommended Minimum and Maximum Capacitance

APPLICATIONS INFORMATION

Component Selection Guide

The MAX20362 is designed to be compatible with small case-size ceramic capacitors and small case-size inductors. In general, system designers should take care to observe the steep DC bias, AC bias, and temperature derating of small case-size capacitors. Inductor selection should be done with care. Ferrite core inductors are often appealing due to their small physical size and apparently sufficient inductance, but in reality, the DC current derating of the inductance and the excessive core losses make these terrible selections. A good metal alloy core inductor is recommended.

Inductor Selection

Inductor selection for the MAX20362 should be optimized for the intended application. A 2.2µH is recommended for full-range operation, and a 1µH can be used for V_{CAP} less than 5.5V. Aside from the inductor value, physical size, DC resistance (DCR), maximum average current, and saturation current are the primary factors to consider. The maximum average inductor current is obtained using the following equation:

$$I_{L\_MAX} = \max[-BBIMaxN, BBIMaxP + (0.5 \times \max[BBstIPSet1, BBstIPSet2])]$$

The average inductor current calculated above dictates the required maximum average current for temperature rise on the inductor. In order to determine the required inductor saturation current, the peak current must be calculated. The peak current for this converter can be calculated as:

$$I_{L\_PEAK} = \max[-BBIMaxN, BBIMaxP + \max[BBstIPSet1, BBstIPSet2]]$$

where BBstIPSet1 and BBstIPSet2 are the peak current setting described in register 0x03. BBIMaxN is the negative valley current described in register 0x04. BBIMaxP is the positive valley current described in register 0x05. When selecting an inductor, one primary factor in achieving high efficiency is the DCR of the inductor. For maximum efficiency, select an inductor with the lowest DCR possible in the required package size. Another factor to consider is magnetic losses. Generally, magnetic losses are lower in inductors with a larger physical size and/or higher saturation current ratings. In most cases, ferrite core inductors should be avoided, as they tend to exhibit poor AC characteristics, especially in discontinuous conduction mode (DCM).

Table 6. Recommended Inductor

PART NUMBER	MANUFACTURER	VALUE	SIZE (IMPERIAL)	V_{CAP}
DFE201610E-2R2M	Murata	2.2µH	0806	All range
DFE201210U-1R0M = P2	Murata	1µH	0805	<5.5V
PLEA67BBA1R0M-1PT00	TDK	1µH	0402	<5.5V

BBIN Capacitor Selection

The MAX20362 is designed to be compatible with small case-size ceramic capacitors. As such, the device has low capacitance requirements to accommodate the steep voltage derating of 0603, 0402, and 0201 (imperial) capacitors. *Figure 13* shows the minimum capacitance required at BBIN.

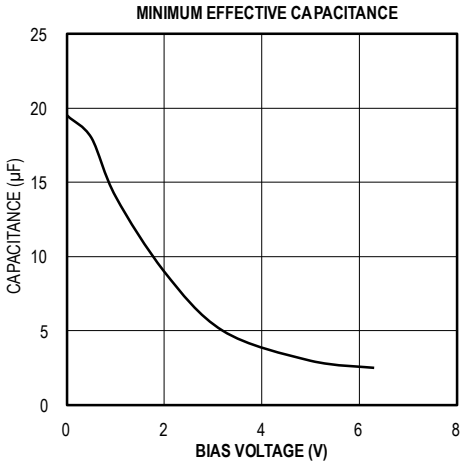


Figure 13. BBIN Required Minimum Capacitance

Table 7. Recommended BBIN Capacitor

PART NUMBER	MANUFACTURER	VALUE	SIZE (IMPERIAL)
GRM155R60J226ME11D	Murata	22µF	0402

BBOUT Capacitor Selection

The MAX20362 is designed to be compatible with small case-size ceramic capacitors. As such, the device has low capacitance requirements to accommodate the steep voltage derating of 0603, 0402, and 0201 (imperial) capacitors. *Figure 14* presents the minimum capacitance required at BBOUT with BBHalfBW = 0. When BBHalfBW = 1, the capacitance may be reduced to half of that shown in *Figure 14*, with the tradeoff of a worse load transient response.

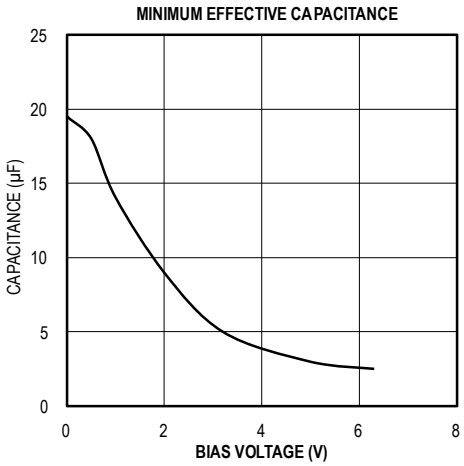


Figure 14. Buck-Boost Required Minimum Output Capacitance

Table 8. Recommended BBOUT Capacitor

PART NUMBER	MANUFACTURER	VALUE	SIZE (IMPERIAL)
GRM155R60J226ME11D	Murata	22µF	0402

CAP Node Tank Capacitance Selection

The MAX20362 is designed to extract nearly all of the energy from the CAP capacitance. Knowing the energy of pulses on the BBOUT node allows the designer to size the CAP capacitance. Design with the following formula in mind:

$$E_{STORED} = \frac{1}{2} C_{DERATED} \times V^2$$

where $C_{DERATED}$ is the derated capacitance at the maximum DC voltage. Design with a 20% margin above the actual energy needed. For example, if BBOUT supports two 100mA pulses of 100µs each, and the buck-boost regulates at 4V for each pulse, the total energy needed on BBOUT is 100mA x 100µs x 2 pulses x 4V = 80µJ. With a 20% margin, this becomes 96µJ. Assume that the capacitor charges to 9.5V and discharges to 1.5V. The energy stored in an ideal capacitor in such a case is:

$$\frac{1}{2} \times C \times \left(9.5^2 - 1.5^2\right) = 89.125C \times J$$

The minimum capacitance needed in this example is the following amount of derated capacitance:

$$\frac{96\mu J}{89.125} = 1.078\mu F$$

Keep in mind that the CAP capacitance recharge is limited by the input current limit. BBOUT pulses must be spaced such that the average load on BBOUT is less than the average input power, plus ~20% margin for efficiency and other factors.

I²C Interface

The MAX20362 contains an I²C-compatible interface for data communication with a host controller (SCL and SDA). The MAX20362 can support I²C frequencies up to 1MHz. SCL and SDA require pull-up resistors connected to a positive supply.

Peripheral Address

In the MAX20362, the peripheral address is configured at the factory by the i2c_2nd_sid OTP bit to be either 0b1101000 (0x68) plus the Read/Write bit or 0b1101100 (0x6C) plus the Read/Write bit. For versions with the 7-bit peripheral address 0x68, set the Read/Write bit high to configure the MAX20362 to read mode (0xD1) or set the Read/Write bit low to configure the MAX20362 to write mode (0xD0). For versions with the 7-bit peripheral address 0x6C, set the Read/Write bit high to configure the MAX20362 to read mode (0xD8) or set the Read/Write bit low to configure the MAX20362 to write mode (0xD9). See i2c_2nd_sid in *Table 9* for the peripheral address corresponding to a given part number. The address is the first byte of information sent to the MAX20362 after the START condition.

Start, Stop, and Repeated Start Conditions

When writing to the MAX20362 using I²C, the controller sends a START condition (S) followed by the MAX20362 I²C write address. After the address, the controller sends the register address of the register to be programmed. The controller then ends communication by issuing a STOP condition (P) to relinquish control of the bus or a REPEATED START condition (Sr) to communicate to another I²C peripheral. See *Figure 15*.

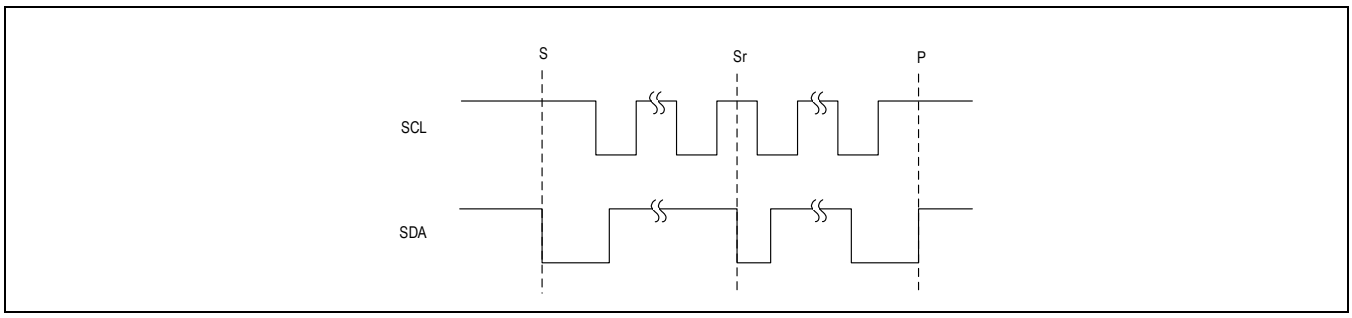


Figure 15. I²C START, STOP, and REPEATED START Conditions

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on the SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *Start, Stop, and Repeated Start Conditions* section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the controller sends an address and two data bytes to the peripheral device (see *Figure 16*).
The following procedure describes the single byte write operation:

- The controller sends a START condition.
- The controller sends the 7-bit peripheral address plus a write bit (low).
- The addressed peripheral asserts an ACK on the data line.
- The controller sends the 8-bit register address.
- The peripheral asserts an ACK on the data line.
- The controller sends 8 data bits.
- The peripheral asserts an ACK on the data line.
- The controller generates a STOP condition.

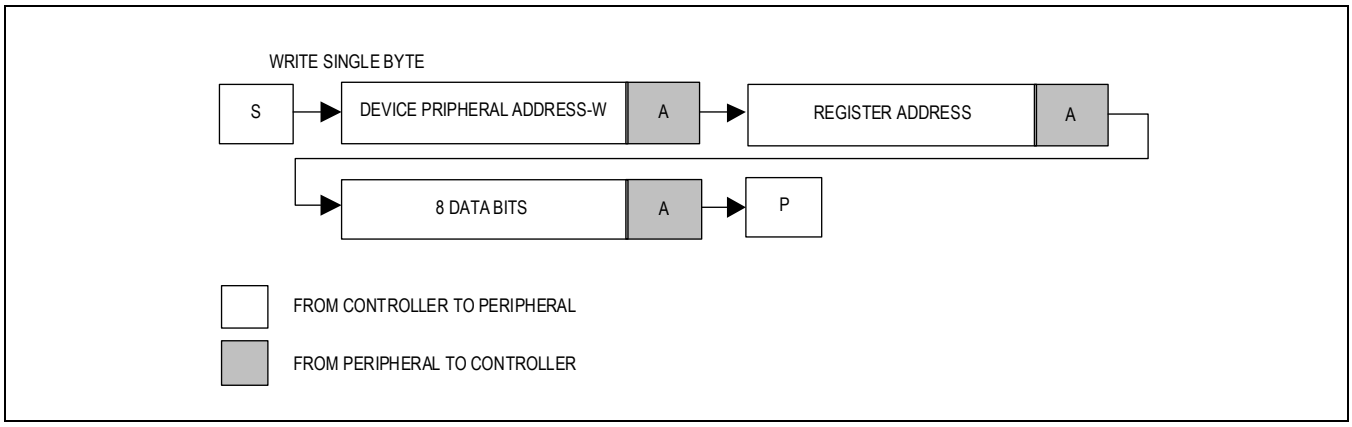


Figure 16. Single Byte Write Sequence

Burst Write

In this operation, the controller sends an address and multiple data bytes to the peripheral device (see *Figure 17*). The peripheral device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

- The controller sends a START condition.
- The controller sends the 7-bit peripheral address plus a write bit (low).
- The addressed peripheral asserts an ACK on the data line.
- The controller sends the 8-bit register address.
- The peripheral asserts an ACK on the data line.
- The controller sends 8 data bits.
- The peripheral asserts an ACK on the data line.
- Repeat 6 and 7 N-1 times.
- The controller generates a STOP condition.

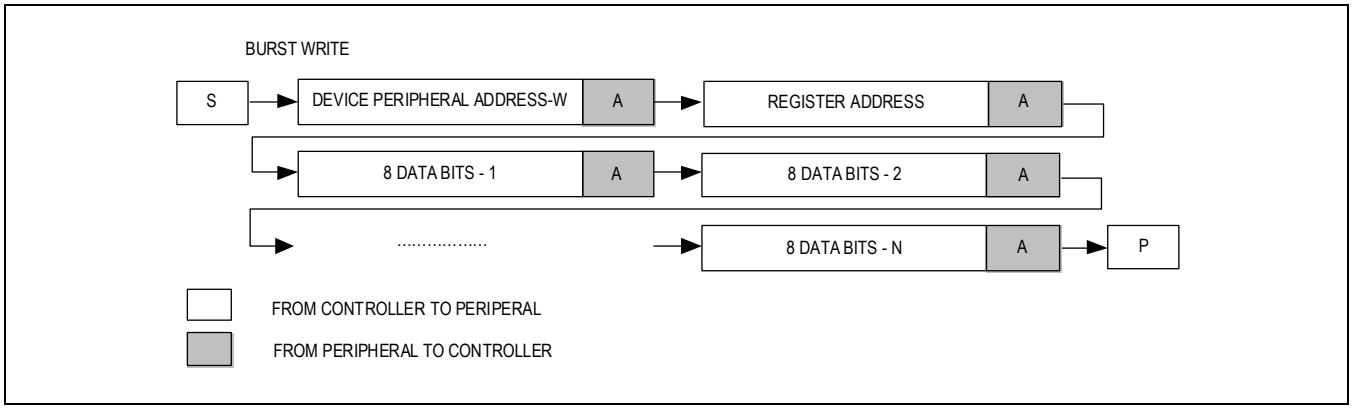


Figure 17. Burst Write Sequence

Single-Byte Read

In this operation, the controller sends an address plus two data bytes and receives one data byte from the peripheral device (see *Figure 18*). The following procedure describes the single byte read operation:

- The controller sends a START condition.
- The controller sends the 7-bit peripheral address plus a write bit (low).
- The addressed peripheral asserts an ACK on the data line.
- The controller sends the 8-bit register address.
- The peripheral asserts an ACK on the data line.
- The controller sends a REPEATED START condition.
- The controller sends the 7-bit peripheral address plus a read bit (high).
- The addressed peripheral asserts an ACK on the data line.
- The peripheral sends 8 data bits.
- The controller asserts a NACK on the data line.
- The controller generates a STOP condition.

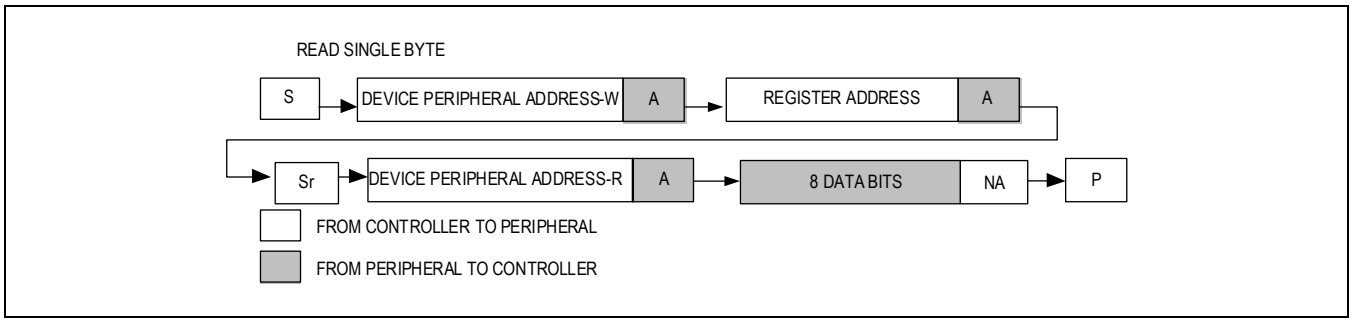


Figure 18. Read Byte Sequence

Burst Read

In this operation, the controller sends an address plus two data bytes and receives multiple data bytes from the peripheral device (see *Figure 19*). The following procedure describes the burst byte read operation:

- The controller sends a START condition.
- The controller sends the 7-bit peripheral address plus a write bit (low).
- The addressed peripheral asserts an ACK on the data line.
- The controller sends the 8-bit register address.
- The peripheral asserts an ACK on the data line.
- The controller sends a REPEATED START condition.
- The controller sends the 7-bit peripheral address plus a read bit (high).
- The peripheral asserts an ACK on the data line.
- The peripheral sends 8 data bits.
- The controller asserts an ACK on the data line.
- Repeat 9 and 10 N-2 times.
- The peripheral sends the last 8 data bits.
- The controller asserts a NACK on the data line.
- The controller generates a STOP condition.

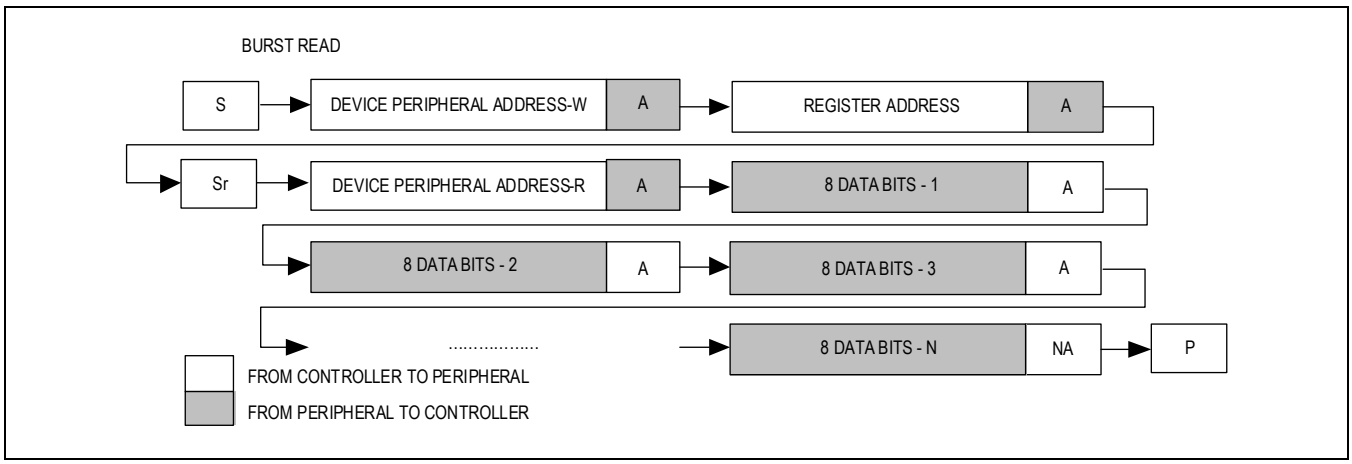


Figure 19. Burst Read Sequence

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the controller and the MAX20362 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see *Figure 20*). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

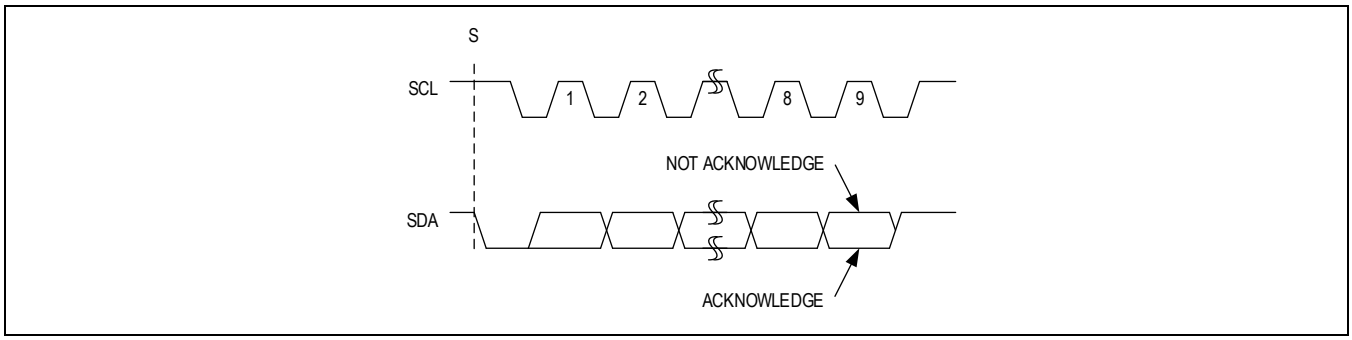


Figure 20. Acknowledge Bits

REGISTER MAP

MAX20362

ADDRESS	NAME	MSB							LSB
USER									
0x00	ChipID[7:0]	ChipID[7:0]							
0x01	BBstCfg0[7:0]	BBHalfBW	BBstLowEMIB	BBstEna	BBstFast	–	BBFHighSh	BBstActDsc	BBstPsvDsc
0x02	BBstVSet[7:0]	BBstFpwm	BBstVSet[6:0]						
0x03	BBstISet[7:0]	BBstIPSet2[3:0]				BBstIPSet1[3:0]			
0x04	BBstIMaxN[7:0]	–	–	–	BBIMaxN[4:0]				
0x05	BBstIMaxP[7:0]	–	–	–	BBIMaxP[4:0]				
0x06	BBstIPwpMaxP[7:0]	–	–	–	BBIPwpMaxP[4:0]				
0x08	BBstCfg1[7:0]	–	–	BBstTmoSel[1:0]		BBL2P2SeI	BBstIpPadPEnb	BBstOvloSel[1:0]	
0x09	BBstCfg2[7:0]	–	–	BBstTankTmoSel[1:0]		BBstTmoSelLg[2:0]			BBSimoSel
0x0A	BBstVSetCap[7:0]	BBstActDscCap	BBstPsvDscCap	BBstStepCap[1:0]		BBstVsetCap[3:0]			
0x0B	BBstISetCap[7:0]	BBstIPSetCap2[3:0]				BBstIPSetCap1[3:0]			
0x0C	BBIngenCfg0[7:0]	BBIngenDrp[1:0]		BBIngenSel[5:0]					
0x10	Status[7:0]	BBCapOvloSts	BBCapUvloSts	BBstOnSts	BBstOffSts	VddaUvloSts	BBoutUvloSts	BstSts	ThmFltSts
0x12	IngenSts[7:0]	–	–	–	OutTmoSts	DrpMinSts	TnkTmoSts	SimoPinSts	BBDrpMaxSts
0x13	LDOStatus[7:0]	–	–	–	–	LDODivSts	LDOShrSts	LDOThmSts	LDOClpSts
0x14	Int[7:0]	BBCapOvloInt	BBCapUvloInt	BBstOnInt	BBstOffInt	VddaUvloInt	BBoutUvloInt	BstFltInt	ThmFltInt
0x15	CommInt[7:0]	–	–	ChgModDone	RRTimeout	RRInc	SPIDone	SPITimeout	SPIParErr
0x16	IngenInt[7:0]	–	–	–	OutTmoInt	BootTmoInt	TnkTmoInt	SimoPinInt	BBDrpMaxInt
0x17	LDOInt[7:0]	–	–	–	–	LDODivInt	LDOShrInt	LDOThmInt	LDOClpInt
0x18	Mask[7:0]	BBCapOvloMsk	BBCapUvloMsk	BBstOnMsk	BBstOffMsk	VddaUvloMsk	BBoutUvloMsk	BstFltMsk	ThmFltMsk

ADDRESS	NAME	MSB							LSB
0x19	CommMsk[7:0]	–	–	ChgModDoneMsk	RRTimeoutMsk	RRIncMsk	SPIDoneMsk	SPITimeoutMsk	SPIParErrMsk
0x1A	IngenMsk[7:0]	–	–	–	OutTmoMsk	BootTmoMsk	TnkTmoMsk	SimoPinMsk	BBDrpMaxMsk
0x1B	LDOMsk[7:0]	–	–	–	–	LDODivMsk	LDOShrMsk	LDOThmMsk	LDOClpMsk
0x1C	BBstIMaxPRb[7:0]	–	–	–	BBIMaxPRb[4:0]				
0x1D	BBFsmState[7:0]	–	–	BBCtrlState[5:0]					
0x1E	BBVset[7:0]	BB_LOWPB	BB_VSET[6:0]						
0x1F	RRpoint[7:0]	–	–	–	RRPointer[4:0]				
0x20	RRVset00[7:0]	RRLowPB00	RRVset00[6:0]						
0x21	RRVset01[7:0]	RRLowPB01	RRVset01[6:0]						
0x22	RRVset02[7:0]	RRLowPB02	RRVset02[6:0]						
0x23	RRVset03[7:0]	RRLowPB03	RRVset03[6:0]						
0x24	RRVset04[7:0]	RRLowPB04	RRVset04[6:0]						
0x25	RRVset05[7:0]	RRLowPB05	RRVset05[6:0]						
0x26	RRVset06[7:0]	RRLowPB06	RRVset06[6:0]						
0x27	RRVset07[7:0]	RRLowPB07	RRVset07[6:0]						
0x28	RRVset08[7:0]	RRLowPB08	RRVset08[6:0]						
0x29	RRVset09[7:0]	RRLowPB09	RRVset09[6:0]						
0x2A	RRVset0A[7:0]	RRLowPB0A	RRVset0A[6:0]						
0x2B	RRVset0B[7:0]	RRLowPB0B	RRVset0B[6:0]						
0x2C	RRVset0C[7:0]	RRLowPB0C	RRVset0C[6:0]						

ADDRESS	NAME	MSB							LSB
0x2D	RRVset0D[7:0]	RRLowPB0D	RRVset0D[6:0]						
0x2E	RRVset0E[7:0]	RRLowPB0E	RRVset0E[6:0]						
0x2F	RRVset0F[7:0]	RRLowPB0F	RRVset0F[6:0]						
0x30	RRVset10[7:0]	RRLowPB10	RRVset10[6:0]						
0x31	RRVset11[7:0]	RRLowPB11	RRVset11[6:0]						
0x32	RRVset12[7:0]	RRLowPB12	RRVset12[6:0]						
0x33	RRVset13[7:0]	RRLowPB13	RRVset13[6:0]						
0x40	LDOCfg[7:0]	–	–	LDOBBstSupp	LDOPropMd	LDOLowIq	LDOAct	LDOPsv	LDOEna
0x41	LDOVSet[7:0]	–	–	–	LDOVSet[4:0]				
0x50	LockMsk[7:0]	–	–	–	–	–	–	–	BBLck
0x51	LockUnlock[7:0]	PASSWD[7:0]							
0x54	DVSCfg[7:0]	–	–	–	–	I2CLkptDis	RRWrap	RREna	DVSSource
0x55	RRCfg1[7:0]	–	RRClkPolarity	RRTimeoutRes	RRSize[4:0]				
0x56	RRCfg2[7:0]	–	–	–	–	–	RRTimeoutLength[2:0]		
0x57	SPICfg[7:0]	–	–	–	–	–	–	–	SPITimeoutEna
0x6E	ConfOtp[7:0]	BGDscSkip	SSpcEna	SSpcFullScale[1:0]		SSpcFunc	SSpcSize[1:0]		FpwmFast
0x6F	FuncDef[7:0]	–	–	–	–	–	–	LtchOffFlt	LtchOffThm

Register Details

ChipID (0x0)

BIT	7	6	5	4	3	2	1	0
Field	ChipID[7:0]							
Reset	0x00							

Access Type	Read Only

BITFIELD	BITS	DESCRIPTION
ChipID	7:0	ChipID[7:0] indicates the version of the device in use.

BBstCfg0 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	BBHalfBW	BBstLowEMIB	BBstEna	BBstFast	–	BBFHighSh	BBstActDsc	BBstPsvDsc
Reset		0b00	0b0	0b0	–	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BBHalfBW	7	Buck-Boost Half Bandwidth Mode Bit is latched internally and can only be changed when BBstEna = 0.	0: Full bandwidth operation (full capacitance required) 1: Half bandwidth operation (capacitance requirement reduced by half)
BBstLowEMIB	6	Buck-Boost Low EMI Mode Disable Changes the rise/fall time of LXA/LXB. Slowing the LXA/LXB slope and increasing rise/fall times can reduce EMI at the cost of efficiency. Bit is latched internally and can only be changed when BBstEna = 0.	0: Increase rise/fall time on LXA/LXB by 4x 1: Nominal slopes
BBstEna	5	Buck-Boost Enable	0: Buck-boost disabled 1: Buck-boost enabled
BBstFast	4	Buck-Boost Pretrigger Mode Setting Increases the quiescent current of the buck-boost to improve output regulation during load transients.	0: Normal, low quiescent current operation 1: Fast response mode enabled. Quiescent current increased to 150µA (typ).
BBFHighSh	2	Buck-Boost f_{HIGH} Threshold Selects the switching frequency threshold f_{HIGH}. If the buck-boost switching frequency exceeds the f_{HIGH} rising threshold, all the blocks are kept ON (I_Q is higher) until the frequency reaches the f_{HIGH} falling threshold. A small voltage glitch on V_{OUT} can sometimes be observed at the crossing of the f_{HIGH} crossover. Bit is latched internally and can only be changed when BBstEna = 0.	0: 50kHz rising/25kHz falling 1: 100kHz rising/50kHz falling
BBstActDsc	1	Buck-Boost Output Active Discharge Control	0: Buck-boost not actively discharged 1: Buck-boost actively discharged for 50ms when disabled
BBstPsvDsc	0	Buck-Boost Output Passive Discharge Control	0: Buck-boost not passively discharged 1: Buck-boost passively discharged when disabled

BBstVSet (0x2)

BIT	7	6	5	4	3	2	1	0

Field	BBstFpwm	BBstVSet[6:0]
Reset	0b0	0b0000000
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BBstFpwm	7	FPWM control - only valid when I²C mode is enabled for DVS (DVSSource = 0). FPWM mode gives the best load regulation and voltage ripple but requires a high quiescent and therefore leads to poor efficiency at light loads. Recommended to use only for loads ≥70mA.	0: FPWM is disabled 1: FPWM is enabled
BBstVSet	6:0	Buck-Boost Output Voltage Setting 1.5V to 5.5V, Linear Scale, 50mV increments	0000000: 1.50V 0000001: 1.55V ...: ... ≥1010000: 5.50V

BBstISet (0x3)

BIT	7	6	5	4	3	2	1	0
Field	BBstIPSet2[3:0]				BBstIPSet1[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
BBstIPSet2	7:4	Buck-Boost Nominal Maximum Peak Current Setting 2. Sets the extra peak current in the inductor from CAP to BBOUT relative to IPSET1 when V_{CAP} > V_{BBOUT}. From 100mA to 475mA, 25mA steps. Suggested settings for optimal efficiency: 400mA Note1: The values are increased by ~+30% when BBL2P2Sel = 0 is set. Note2: The actual peak current in the inductor is higher than the setting here due to delays in the peak current comparator and the power stage. See the buck-boost operation section for a description of the peak current settings.	0000: 100mA 0001: 125mA ...: ... 1111: 475mA
BBstIPSet1	3:0	Buck-Boost Nominal Maximum Peak Buck-Boost Nominal Peak Current Setting 1 Sets the nominal peak current in the inductor from CAP to BBOUT when charging inductor between V_{CAP} and GND. Suggested values to get optimal efficiency: BBstVSet ≤ 4V: IPSET1 = 250mA 4V < BBstVSet ≤ 4.5V: IPSET1 = 300mA	0000: 100mA 0001: 125mA ...: ... 1111: 475mA

BITFIELD	BITS	DESCRIPTION	DECODE
		4.5V < BBstVSet ≤ 5V: IPSET1 = 350mA BBstVSet > 5V: IPSET1 = 400mA Note1: The values are increased by ~+30% when BBL2P2Sel = 0 is set. Note2: The actual peak current in the inductor is larger than this setting due to delays in the peak current comparator and the power stage. Note 3: Real peak current is automatically reduced when $V_{CAP} > V_{BBOUT}$. BBstVSet ≤ 4V: IPSET1 = 200mA 4V < BBstVSet ≤ 4.5V: IPSET1 = 250mA 4.5V < BBstVSet ≤ 5V: IPSET1 = 300mA BBstVSet >5V: IPSET1 = 350mA See the buck-boost operation section for a description of the peak current settings.	

BBstIMaxN (0x4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BBIMaxN[4:0]				
Reset	–	–	–	0b000000				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
BBIMaxN	4:0	Maximum absolute inductor negative valley current limit setting when FPWM is enabled. Bit is latched internally and can only be changed when BBstEna = 0 Settings from 0mA to -1.55A, -50mA steps	00000: 0mA 00001: -50mA ...: ... 11110: -1.50A 11111: -1.55A

BBstIMaxP (0x5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BBIMaxP[4:0]				
Reset	–	–	–	0b000000				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
BBIMaxP	4:0	Maximum inductor positive valley current limit setting. Bit is latched internally and can only be changed when BBstEna = 0 Settings from 0 to 1.1A, 50mA steps	00000: 0mA 00001: 50mA ... ≥10110: 1.1A

BITFIELD	BITS	DESCRIPTION	DECODE
		00000 = 0mA 00001 = 50mA ..... ≥10110 = 1.1A The value is clamped to 550mA (code 0xB) when BBHalfBW (address 0x01, bit 7) is 1, and to 1.1A (code 0x16) when BBHalfBW = 0.	

BBstIPwpMaxP (0x6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BBIPwpMaxP[4:0]				
Reset	–	–	–	0b000000				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
BBIPwpMaxP	4:0	Start-up positive inductor valley current limit. Latched internally, it can only be changed when BBstEna = 0. Settings from 0 to 1.1A, 50mA steps 00000 = 0mA 00001 = 50mA ..... ≥10110 = 1.1A The value is clamped to 550mA (code 0xB) when BBHalfBW (address 0x01, bit 7) is 1, and to 1.1A (code 0x16) when BBHalfBW = 0.	00000: 0mA 00001: 50mA 00010: 100mA ...: ... ≥10110: 1.1A

BBstCfg1 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstTmoSel[1:0]		BBL2P2Sel	BBstIpPadPEnb	BBstOvloSel[1:0]	
Reset	–	–			0b0	0b0		
Access Type	–	–	Write, Read		Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
BBstTmoSel	5:4	SIMO "short" timeout, selected when SIMO configuration is 0 (equal priority). Bit is latched internally and can only be changed when BBstEna = 0.	00: 1µs 01: 6µs 10: 11µs 11: 16µs

BITFIELD	BITS	DESCRIPTION	DECODE
BBL2P2Sel	3	Inductance selection bit. Note: BBL2P2Sel = 1 shows worse load regulation in continuous conduction mode. This setting is latched internally when BBstEna = 1 and can therefore only be changed when BBstEna = 0. BBL2P2Sel = 0 : Use it for 1µH inductor BBL2P2Sel = 1 : Use it for 2.2µH inductor	0: 1µH inductor 1: 2.2µH inductor
BBstIpPadPEnb	2	Adaptive Peak/Valley Current Adjustment Disable 0 = Enabled 1 = Disabled, peak current fixed to the values set by BBstIPSet1 and BBstIPSet2. Valley current is fixed to 0mA. This setting is equivalent to forcing discontinuous conduction mode and greatly diminishes the output power capability of the part. Generally, this is not a recommended setting.	
BBstOvloSel	1:0	CAP OVLO threshold	00: 2.5V 01: 5V 10: 6.3V 11: 10V

BBstCfg2 (0x9)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstTankTmoSel[1:0]		BBstTmoSelLg[2:0]			BBSimoSel
Reset	–	–						
Access Type	–	–	Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BBstTankTmoSel	5:4	Timeout value to charge supercap. Bit is latched internally and can only be changed when BBstEna = 0.	00: 100ms 01: 1s 10: 10s 11: 100s
BBstTmoSelLg	3:1	SIMO "long" timeout, selected when SIMO configuration is 1 (priority to output). Bit is latched internally and can only be changed when BBstEna = 0.	000: 31.25µs 001: 93.75µs 010: 125µs 011: 250µs 100: 375µs 101: 500µs
BBSimoSel	0	Controls arbitrator priority either to be equal between CAP and BBOUT or to show preference to BBOUT. Valid only when the SIMO pin is pulled low.	0: CAP and BBOUT receive equal inductor priority 1: BBOUT receives inductor preference for output regulation

BBstVSetCap (0xA)

BIT	7	6	5	4	3	2	1	0

Field	BBstActDscCap	BBstPsvDscCap	BBstStepCap[1:0]	BBstVsetCap[3:0]
Reset				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BBstActDscCap	7	Buck-Boost CAP Active Discharge Control 0 = Buck-boost not actively discharged 1 = Buck-boost actively discharged when disabled
BBstPsvDscCap	6	Buck-Boost CAP Passive Discharge Control 0 = Buck-boost not passively discharged 1 = Buck-boost passively discharged when disabled
BBstStepCap	5:4	Step width for the voltage regulation of the CAP voltage. Depending on the value of the bitfield BBstVsetCap, the mapping is: BBstStepCap = 2'b00 BBstVsetCap = 0 -> 2.5V BBstVsetCap = 1 -> 3V BBstVsetCap = 2 -> 3.5V BBstVsetCap = 3 -> 4V BBstVsetCap = 4 -> 4.5V BBstVsetCap = 5 -> 5V BBstVsetCap = 6 -> 5.5V BBstVsetCap = 7 -> 6V BBstVsetCap = 8 -> 6.5V BBstVsetCap = 9 -> 7V BBstVsetCap = 10 -> 7.5V BBstVsetCap = 11 -> 8V BBstVsetCap = 12 -> 8.5V BBstVsetCap = 13 -> 9V BBstVsetCap = 14 -> 9.5V BBstVsetCap = 15 -> 9.5V BBstStepCap = 2'b01 BBstVsetCap = 0 -> 1.6V BBstVsetCap = 1 -> 1.85V BBstVsetCap = 2 -> 2.1V BBstVsetCap = 3 -> 2.35V BBstVsetCap = 4 -> 2.6V BBstVsetCap = 5 -> 2.85V BBstVsetCap = 6 -> 3.1V BBstVsetCap = 7 -> 3.35V BBstVsetCap = 8 -> 3.6V BBstVsetCap = 9 -> 3.85V BBstVsetCap = 10 -> 4.1V BBstVsetCap = 11 -> 4.35V BBstVsetCap = 12 -> 4.6V BBstVsetCap = 13 -> 4.85V BBstVsetCap = 14 -> 5.1V BBstVsetCap = 15 -> 5.35V BBstStepCap = 2'b10 BBstVsetCap = 0 -> 1.65V BBstVsetCap = 1 -> 1.65V BBstVsetCap = 2 -> 1.65V BBstVsetCap = 3 -> 1.65V BBstVsetCap = 4 -> 1.65V BBstVsetCap = 5 -> 1.775V BBstVsetCap = 6 -> 1.9V BBstVsetCap = 7 -> 2.025V BBstVsetCap = 8 -> 2.15V

BITFIELD	BITS	DESCRIPTION
		BBstVsetCap = 9 -> 2.275V BBstVsetCap = 10 -> 2.4V BBstVsetCap = 11 -> 2.525V BBstVsetCap = 12 -> 2.65V BBstVsetCap = 13 -> 2.775V BBstVsetCap = 14 -> 2.9V BBstVsetCap = 15 -> 3.025V BBstStepCap = 2'b11 RESERVED
BBstVsetCap	3:0	Step width for the voltage regulation of the CAP voltage. Depending on the value of the bitfield BBstVsetCap, the mapping is: BBstStepCap = 2'b00 BBstVsetCap = 0 -> 2.5V BBstVsetCap = 1 -> 3V BBstVsetCap = 2 -> 3.5V BBstVsetCap = 3 -> 4V BBstVsetCap = 4 -> 4.5V BBstVsetCap = 5 -> 5V BBstVsetCap = 6 -> 5.5V BBstVsetCap = 7 -> 6V BBstVsetCap = 8 -> 6.5V BBstVsetCap = 9 -> 7V BBstVsetCap = 10 -> 7.5V BBstVsetCap = 11 -> 8V BBstVsetCap = 12 -> 8.5V BBstVsetCap = 13 -> 9V BBstVsetCap = 14 -> 9.5V BBstVsetCap = 15 -> 9.5V BBstStepCap = 2'b01 BBstVsetCap = 0 -> 1.6V BBstVsetCap = 1 -> 1.85V BBstVsetCap = 2 -> 2.1V BBstVsetCap = 3 -> 2.35V BBstVsetCap = 4 -> 2.6V BBstVsetCap = 5 -> 2.85V BBstVsetCap = 6 -> 3.1V BBstVsetCap = 7 -> 3.35V BBstVsetCap = 8 -> 3.6V BBstVsetCap = 9 -> 3.85V BBstVsetCap = 10 -> 4.1V BBstVsetCap = 11 -> 4.35V BBstVsetCap = 12 -> 4.6V BBstVsetCap = 13 -> 4.85V BBstVsetCap = 14 -> 5.1V BBstVsetCap = 15 -> 5.35V BBstStepCap = 2'b10 BBstVsetCap = 0 -> 1.65V BBstVsetCap = 1 -> 1.65V BBstVsetCap = 2 -> 1.65V BBstVsetCap = 3 -> 1.65V BBstVsetCap = 4 -> 1.65V BBstVsetCap = 5 -> 1.775V BBstVsetCap = 6 -> 1.9V BBstVsetCap = 7 -> 2.025V BBstVsetCap = 8 -> 2.15V BBstVsetCap = 9 -> 2.275V BBstVsetCap = 10 -> 2.4V BBstVsetCap = 11 -> 2.525V BBstVsetCap = 12 -> 2.65V BBstVsetCap = 13 -> 2.775V BBstVsetCap = 14 -> 2.9V BBstVsetCap = 15 -> 3.025V

BITFIELD	BITS	DESCRIPTION
		BBstStepCap = 2'b11 RESERVED

BBstISetCap (0xB)

BIT	7	6	5	4	3	2	1	0
Field	BBstIPSetCap2[3:0]				BBstIPSetCap1[3:0]			
Reset								
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
BBstIPSetCap2	7:4	Buck-Boost Nominal Maximum Peak Current Setting 2. Sets the extra peak current from BBIN to CAP on top of IPSET1 when $V_{BBIN} > V_{CAP}$. From 100 to 475mA step 25mA. 0000 = 100mA 0001 = 125mA .... 1111 = 475mA Suggested value 350mA Note1: The values are increased by ~+30% when BBL2P2Sel = 0 is set. Note2: Actual peak current in the inductor is larger due to the delay of the peak comparator and power stage. See the buck-boost operation section for a description of the peak current settings.
BBstIPSetCap1	3:0	Buck-boost nominal peak current setting 1. Nominal peak current pulse from BBIN to CAP when charging the inductor between V_{BBIN} and GND. See the buck-boost operation section for a description of the peak current settings. From 100mA to 475mA step 25mA. 0000 = 100mA 0001 = 125mA .... 1111 = 475mA Suggested values to get optimal efficiency: 350mA Note1: The values are increased by ~+30% when BBL2P2Sel = 0 is set. Note2: Actual peak current in the inductor is larger due to the delay of the peak comparator and power stage. Note 3: Real ipeak current ref is automatically reduced when $V_{BBIN} > V_{BAT}$.

BBIngenCfg0 (0xC)

BIT	7	6	5	4	3	2	1	0
Field	BBIngenDrp[1:0]		BBIngenSel[5:0]					
Reset								

Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BBIngenDrp	7:6	Selects the voltage drop from BAT to BBIN when Buck-Boost operates in current limit. A bigger drop reduces efficiency. 00 = 55mV 01 = 100mV 10 = 150mV 11 = 200mV
BBIngenSel	5:0	Battery Input Current Limit Value. Controls the maximum current flowing from BAT. It limits the current flowing to CAP, but not the current flowing from CAP to BBOUT. From 5mA to 50mA step 1mA 000000 = 5mA 000001 = 6mA .... ≥101101 = 50mA

Status (0x10)

BIT	7	6	5	4	3	2	1	0
Field	BBCapOvloSts	BBCapUvloSts	BBstOnSts	BBstOffSts	VddaUvloSts	BBoutUvloSts	BstSts	ThmFltSts
Reset			0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
BBCapOvloSts	7	Status bit for CAP Ovlo fault.
BBCapUvloSts	6	Status bit for CAP Uvlo fault. This bit is set when the fault occurs and is reset back to zero when either BBstEna is written to zero or the autoretry time elapses (if enabled, depending on OTP bit LtchOffFlt).
BBstOnSts	5	Status bit of buck-boost on. This bit goes to 1 when the buck-boost finally turns on, so that DVS operations are possible, and goes back to zero when the buck-boost is disabled or a fault occurs.
BBstOffSts	4	BStatus bit of buck-boost off. This bit goes to 1 when the buck-boost finally turns off after being disabled and having gone through safe freewheeling and output discharge, and goes back to zero when the buck-boost is enabled again.
VddaUvloSts	3	Status bit of V_{DDA} UVLO fault. This bit is set when the fault occurs and is reset back to zero when either BBstEna is written to zero or the autoretry time elapses (if enabled, depending on OTP bit LtchOffFlt).
BBoutUvloSts	2	Status bit of BBOUT UVLO fault. This bit is set when the fault occurs and is reset back to zero when either BBstEna is written to zero or the autoretry time elapses (if enabled, depending on OTP bit LtchOffFlt).
BstSts	1	Status bit of bootstrap fault. This bit goes to 1 when the fault occurs and goes back to zero when either BBstEna is set to zero or the autoretry time elapses (if enabled, depending on OTP bit LtchOffFlt).

BITFIELD	BITS	DESCRIPTION
ThmFltSts	0	Status bit of thermal fault. This bit is set when a thermal fault occurs and is reset back to zero when either BBstEna is written to zero or the autoretry time elapses (if enabled, depending on OTP bit LtchOffThm).

IngenSts (0x12)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	OutTmoSts	DrpMinSts	TnkTmoSts	SimoPinSts	BBDrpMaxSts
Reset	–	–	–					
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
OutTmoSts	4	Status bit for OUT startup phase charging fault. This bit is set when either CAP or BBOUT were not charged within the time set by the BBstTankTmoSel, and is reset back to zero when either BBstEna is written to zero or the autoretry time elapses (if enabled, depending on OTP bit LtchOffFlt).
DrpMinSts	3	Status bit for DROPMIN flag. This bit is set if the voltage drop across the INGEN (V_{BAT} - V_{BBIN}) exceeds 40mV.
TnkTmoSts	2	Status bit of the CAP recharging fault. This bit is set when CAP was not recharged within the time set by the BBstTankTmoSel, and is reset back to zero when either BBstEna is written to zero or the autoretry time elapses (if enabled, depending on OTP bit LtchOffFlt).
SimoPinSts	1	Status of the pin SIMO (debounced 500µs).
BBDrpMaxSts	0	Status bit for DROPMAX flag. This bit is set if the voltage drop across the INGEN exceeded the maximum allowed value.

LDOStatus (0x13)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LDODivSts	LDOShrSts	LDOThmSts	LDOClpSts
Reset	–	–	–	–				
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
LDODivSts	3	Status bit for divider fault interrupt (a switch opens in the LDO resistive divider due to VDD falling).
LDOShrSts	2	Status bit for LDO output shorted to ground fault.
LDOThmSts	1	Status bit for thermal fault interrupt.

BITFIELD	BITS	DESCRIPTION
LDOClpSts	0	Status bit for output clipping interrupt (the target voltage value for the output is not reachable, so it is being "clipped").

Int (0x14)

BIT	7	6	5	4	3	2	1	0
Field	BBCapOvloInt	BBCapUvloInt	BBstOnInt	BBstOffInt	VddaUvloInt	BBoutUvloInt	BstFltInt	ThmFltInt
Reset			0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BBCapOvloInt	7	Interrupt bit for CAP Ovlo fault. If set, CAP voltage exceeded the value set by the BBstOvloSel bitfield.
BBCapUvloInt	6	Interrupt bit for CAP UVLO. Read to clear.
BBstOnInt	5	Interrupt bit for buck-boost on. Read to clear.
BBstOffInt	4	Interrupt bit for buck-boost off. Read to clear.
VddaUvloInt	3	Interrupt bit for V_{DDA} UVLO fault. Read to clear.
BBoutUvloInt	2	Interrupt bit for BBOUT UVLO fault. Read to clear.
BstFltInt	1	Interrupt bit for bootstrap fault. Read to clear.
ThmFltInt	0	Interrupt bit for thermal fault. Read to clear.

CommInt (0x15)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ChgModDone	RRTimeout	RRInc	SPIDone	SPITimeout	SPIParErr
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
ChgModDone	5	Change DVS mode done interrupt. Read to clear.
RRTimeout	4	Round-robin timeout expired interrupt. Read to clear.
RRInc	3	Round-robin pointer increase interrupt. The interrupt is raised when a pulse that moves the round-robin to the next step is detected. Read to clear.

BITFIELD	BITS	DESCRIPTION
SPIDone	2	If 1, the pseudo-SPI operation is completed. Read to clear.
SPITimeout	1	If 1, the pseudo-SPI operation was ended because of timeout expiration. Read to clear.
SPIParErr	0	If 1, a parity error was found, and the DVS operation was not executed. Read to clear.

IngenInt (0x16)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	OutTmoInt	BootTmoInt	TnkTmoInt	SimoPinInt	BBDrpMaxInt
Reset	–	–	–					
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
OutTmoInt	4	Interrupt bit for OUT startup phase charging fault. If set, either CAP or BBOUT were not charged within the time set by the BBstTankTmoSel bitfield.
BootTmoInt	3	Boot Timeout interrupt. If 1, the BBIN voltage does not reach BAT voltage within 100ms from EN = 1.
TnkTmoInt	2	Interrupt bit for CAP recharge phase after BBOUT startup. If set, CAP was not charged within the time set by the BBstTankTmoSel bitfield.
SimoPinInt	1	Simo Pin interrupt. If 1, SIMO pin has been toggled. If round-robin mode or pseudo-SPI mode is enabled, this bit sets as soon as the mode changes. If I^2C mode is enabled, this bit is set immediately.
BBDrpMaxInt	0	Interrupt bit for DROPMAX flag. If 1, the BBDrpMaxSts has changed.

LDOInt (0x17)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LDODivInt	LDOShrInt	LDOThmInt	LDOClpInt
Reset	–	–	–	–				
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LDODivInt	3	Interrupt bit for LDO divider fault interrupt (a switch opens in the LDO resistive divider due to VDD falling).
LDOShrInt	2	Interrupt bit for LDO output shorted to ground fault.
LDOThmInt	1	Interrupt bit for thermal fault interrupt.

BITFIELD	BITS	DESCRIPTION
LDOClpInt	0	Interrupt bit for LDO output clipping fault (the target voltage value for the output is not reachable, so it is being "clipped").

Mask (0x18)

BIT	7	6	5	4	3	2	1	0
Field	BBCapOvloMsk	BBCapUvloMsk	BBstOnMsk	BBstOffMsk	VddaUvloMsk	BBoutUvloMsk	BstFltMsk	ThmFltMsk
Reset			0b1	0b1	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BBCapOvloMsk	7	Mask bit for BBCapOvloInt. If 1, BBCapOvloInt does not cause the assertion (pull down) of nINT pin.
BBCapUvloMsk	6	Mask bit for BBCapUvloInt. If 1, BBCapUvloInt does not cause the assertion (pull down) of nINT pin.
BBstOnMsk	5	Mask bit for BBstOnInt. If 1, bit BBstOnInt does not cause the assertion (pull down) of nINT pin.
BBstOffMsk	4	Mask bit for BBstOffInt. If 1, bit BBstOffInt does not cause the assertion (pull down) of nINT pin.
VddaUvloMsk	3	Mask bit for VddaUvloInt . If 1, bit VddaUvloInt does not cause the assertion (pull down) of nINT pin.
BBoutUvloMsk	2	Mask bit for BBoutUvloInt . If 1, bit BBoutUvloInt does not cause the assertion (pull down) of nINT pin.
BstFltMsk	1	Mask bit for BstFltInt. If 1, bit BstFltInt does not cause the assertion (pull down) of nINT pin.
ThmFltMsk	0	Mask bit for ThmFltInt. If 1, bit ThmFltInt does not cause the assertion (pull down) of nINT pin.

CommMsk (0x19)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ChgModDoneMsk	RRTimeoutMsk	RRIncMsk	SPIDoneMsk	SPITimeoutMsk	SPIParErrMsk
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
ChgModDoneMsk	5	Mask bit for ChgModDone. If 1, bit ChgModDone does not cause the assertion (pull down) of nINT pin.
RRTimeoutMsk	4	Mask bit for RRTimeout. If 1, bit RRTimeout does not cause the assertion (pull down) of nINT pin.
RRIncMsk	3	Mask bit for RRInc. If 1, bit RRInc does not cause the assertion (pull down) of nINT pin.
SPIDoneMsk	2	Mask bit for SPIDone. If 1, bit SPIDone does not cause the assertion (pull down) of nINT pin.
SPITimeoutMsk	1	Mask bit for SPITimeout. If 1, bit SPITimeout does not cause the assertion (pull down) of nINT pin.
SPIParErrMsk	0	Mask bit for SpiParErr. If 1, bit SpiParErr does not cause the assertion (pull down) of nINT pin.

IngenMsk (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	OutTmoMsk	BootTmoMsk	TnkTmoMsk	SimoPinMsk	BBDrpMaxMsk
Reset	–	–	–					
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
OutTmoMsk	4	Mask bit for OutTmoInt. If 1, OutTmoInt does not cause the assertion (pull down) of nINT pin.
BootTmoMsk	3	Mask bit for BootTmoInt. If 1, BootTmoInt does not cause the assertion (pull down) of nINT pin.
TnkTmoMsk	2	Mask bit for TnkTmoInt. If 1, TnkTmoInt does not cause the assertion (pull down) of nINT pin.
SimoPinMsk	1	Mask bit for SImoPinInt. If 1, SimoPinInt does not cause the assertion (pull down) of nINT pin.
BBDrpMaxMsk	0	Mask bit for BBDrpMaxInt. If 1, BBDrpMaxInt does not cause the assertion (pull down) of nINT pin.

LDOMsk (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LDODivMsk	LDOShrMsk	LDOThmMsk	LDOClpMsk
Reset	–	–	–	–				
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LDODivMsk	3	Mask bit for LDODivInt. If 1, LDODivInt does not cause the assertion (pull down) of nINT pin.
LDOShrMsk	2	Mask bit for LDOShrInt. If 1, LDOShrInt does not cause the assertion (pull down) of nINT pin.
LDOThmMsk	1	Mask bit for LDOThmInt. If 1, LDOThmInt does not cause the assertion (pull down) of nINT pin.
LDOClpMsk	0	Mask bit for LDOClpInt. If 1, LDOClpInt does not cause the assertion (pull down) of nINT pin.

BBstIMaxPRb (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BBIMaxPRb[4:0]				
Reset	–	–	–					
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION
BBIMaxPRb	4:0	Readback for BBIMaxP value (the actual value might be clamped with respect to register BBstIMaxP).

BBFsmState (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBCtrlState[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
BBCtrlState	5:0	Current State of Buck-Boost Control FSM: 000001= Off 000010 = Power-up 000100 = Functional DVS 001000 = Safe Freewheeling 010000 = Active Output Discharge 100000 = Timeout

BBVset (0x1E)

BIT	7	6	5	4	3	2	1	0

Field	BB_LOWPB	BB_VSET[6:0]
Reset	0b0	0b0000000
Access Type	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
BB_LOWPB	7	BBstFpwm read back register. This is the actual value set to the analog circuitry.	In round-robin or in pseudo-SPI, if FPWM or FAST is enabled, BB_LOWPB = 1. In I^2C mode, BB_LOWPB reads 1 in any of the following three conditions. 1) FPWM = 1, FAST = 0, FpwmFast = 1 2) FPWM = 0, FAST = 1, FpwmFast = 0 3) FPWM = 1, FAST = 1, FpwmFast = 0 or 1
BB_VSET	6:0	BBstVset read back register. This is the actual value set to the analog circuitry. 1.5V to 5.5V, Linear Scale, 50mV increments.	0000000: 1.50V 0000001: 1.55V ...: ... ≥1010000: 5.50V

RRpoint (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RRPointer[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION
RRPointer	4:0	Current step of progression for the round-robin. This bitfield displays the number of the step the round-robin has reached so far.

RRVset00 (0x20)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB00	RRVset00[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB00	7	DVS Round-Robin Low Power value 0x00
RRVset00	6:0	DVS Round-Robin voltage value 0x00

RRVset01 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB01	RRVset01[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB01	7	DVS Round-Robin Low Power value 0x01
RRVset01	6:0	DVS Round-Robin voltage value 0x01

RRVset02 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB02	RRVset02[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB02	7	DVS Round-Robin Low Power value 0x02
RRVset02	6:0	DVS Round-Robin voltage value 0x02

RRVset03 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB03	RRVset03[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB03	7	DVS Round-Robin Low Power value 0x03
RRVset03	6:0	DVS Round-Robin voltage value 0x03

RRVset04 (0x24)

BIT	7	6	5	4	3	2	1	0

Field	RRLowPB04	RRVset04[6:0]
Reset	0b0	0b0000000
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RRLowPB04	7	DVS Round-Robin Low Power value 0x04
RRVset04	6:0	DVS Round-Robin voltage value 0x04

RRVset05 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB05	RRVset05[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB05	7	DVS Round-Robin Low Power value 0x05
RRVset05	6:0	DVS Round-Robin voltage value 0x05

RRVset06 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB06	RRVset06[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB06	7	DVS Round-Robin Low Power value 0x06
RRVset06	6:0	DVS Round-Robin voltage value 0x06

RRVset07 (0x27)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB07	RRVset07[6:0]						

Reset	0b0	0b0000000
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RRLowPB07	7	DVS Round-Robin Low Power value 0x07
RRVset07	6:0	DVS Round-Robin voltage value 0x07

RRVset08 (0x28)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB08	RRVset08[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB08	7	DVS Round-Robin Low Power value 0x08
RRVset08	6:0	DVS Round-Robin voltage value 0x08

RRVset09 (0x29)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB09	RRVset09[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB09	7	DVS Round-Robin Low Power value 0x09
RRVset09	6:0	DVS Round-Robin voltage value 0x09

RRVset0A (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB0A	RRVset0A[6:0]						
Reset	0b0	0b0000000						

Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RRLowPB0A	7	DVS Round-Robin Low Power value 0x0A
RRVset0A	6:0	DVS Round-Robin voltage value 0x0A

RRVset0B (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB0B	RRVset0B[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB0B	7	DVS Round-Robin Low Power value 0x0B
RRVset0B	6:0	DVS Round-Robin voltage value 0x0B

RRVset0C (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB0C	RRVset0C[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB0C	7	DVS Round-Robin Low Power value 0x0C
RRVset0C	6:0	DVS Round-Robin voltage value 0x0C

RRVset0D (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB0D	RRVset0D[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB0D	7	DVS Round-Robin Low Power value 0x0D
RRVset0D	6:0	DVS Round-Robin voltage value 0x0D

RRVset0E (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB0E	RRVset0E[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB0E	7	DVS Round-Robin Low Power value 0x0E
RRVset0E	6:0	DVS Round-Robin voltage value 0x0E

RRVset0F (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB0F	RRVset0F[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB0F	7	DVS Round-Robin Low Power value 0x0F
RRVset0F	6:0	DVS Round-Robin voltage value 0x0F

RRVset10 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB10	RRVset10[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB10	7	DVS Round-Robin Low Power value 0x10
RRVset10	6:0	DVS Round-Robin voltage value 0x10

RRVset11 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB11	RRVset11[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB11	7	DVS Round-Robin Low Power value 0x11
RRVset11	6:0	DVS Round-Robin voltage value 0x11

RRVset12 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB12	RRVset12[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB12	7	DVS Round-Robin Low Power value 0x12
RRVset12	6:0	DVS Round-Robin voltage value 0x12

RRVset13 (0x33)

BIT	7	6	5	4	3	2	1	0
Field	RRLowPB13	RRVset13[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RRLowPB13	7	DVS Round-Robin Low Power value 0x13
RRVset13	6:0	DVS Round-Robin voltage value 0x13

LDOCfg (0x40)

BIT	7	6	5	4	3	2	1	0
Field	–	–	LDOBBstSupp	LDOPropMd	LDOLowIq	LDOAct	LDOPsv	LDOEna
Reset	–	–						
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LDOBBstSupp	5	If the LDO is powered by the buck-boost, this bit must be written to 1 so that the LDO control can wait for the buck-boost to turn on before enabling the LDO.
LDOPropMd	4	Enable proportional regulation for general purpose LDO
LDOLowIq	3	Enable low quiescent mode for general purpose LDO
LDOAct	2	Active discharge for general purpose LDO
LDOPsv	1	Passive discharge for general purpose LDO
LDOEna	0	Enable for general purpose LDO

LDOVSet (0x41)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LDOVSet[4:0]				
Reset	–	–	–					
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
LDOVSet	4:0	LDO Output Voltage Setting. Limited by input supply. LDOVSet cannot be changed when LDO is enabled. LDOVSet change is effective after toggling LDOEna bit. 0.9V to 4V, linear scale, 100mV increments 000000 = 0.9V 000001 = 1V … 11110 = 3.9V 11111 = 4V

LockMsk (0x50)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	BBLck
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
BBLck	0	Lock Mask for Buck-Boost Registers 0 = Buck-Boost Registers not masked from locking/unlocking 1 = Buck-Boost Registers masked from locking/unlocking

LockUnlock (0x51)

BIT	7	6	5	4	3	2	1	0
Field	PASSWD[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PASSWD	7:0	Lock/Unlock Password Write 0xAA with BBLck unmasked to lock the BBstVSet register (0x02) Write 0x55 with BBLck unmasked to unlock the BBstVSet register (0x02) All Other Codes: no effect

DVSCfg (0x54)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	I2CLkptDis	RRWrap	RREna	DVSSource
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2CLkptDis	3	If I^2C mode is selected for DVS, the look-up table for BBstIPSet1 is disabled. This means that the value of the current is the one programmed on bitfield BBstIPSet1 with no further elaboration.	0: Look-up table enabled for I^2C 1: Look-up table disabled for I^2C
RRWrap	2	Defines if the round-robin DVS modes stops at the last value (if set to 0) or wraps back to the first one (if set to 1).	0: Round-Robin does not wrap around 1: Round-Robin does wrap around

BITFIELD	BITS	DESCRIPTION	DECODE
RREna	1	DVS Round-Robin enable. After changing this value, wait at least 300µs before trying to send another DVS command, regardless of the DVS mode. DVSSource setting is ignored if this bit is set to 1.	0: Round-Robin disabled 1: Round-Robin enabled
DVSSource	0	Choose interface for DVS After changing this value, wait at least 300µs before trying to send another DVS command, regardless of the DVS mode.	0: I²C enabled to set DVS 1: Dedicated pins enabled to set DVS

RRCfg1 (0x55)

BIT	7	6	5	4	3	2	1	0
Field	–	RRClkPolarity	RRTimeoutRes	RRSize[4:0]				
Reset	–	0b0	0b0	0b00000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RRClkPolarity	6	Round-Robin Clock Polarity If 0, the clock is active low (voltage is updated on its falling edge); if 1, the clock is active high (voltage is updated on its rising edge). This bit should not be changed when round-robin is enabled.	0x0: Falling edge active 0x1: Rising edge active
RRTimeoutRes	5	Round-Robin Timeout Reset This bit determines if round-robin pointer is reset after timeout. This bit should not be changed when round-robin is enabled.	0x0: Timeout does not reset Round Robin pointer 0x1: Timeout resets Round Robin pointer
RRSize	4:0	Number of Steps in Round-Robin Mode This bit should not be changed when round-robin is enabled.	0x0: 0 Step (initial voltage) 0x1: 1 Step ... 0x13: 19 Steps

RRCfg2 (0x56)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RRTimeoutLength[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
RRTimeoutLength	2:0	Round-Robin Timeout Duration 000 = Timeout disabled 001= 500µs 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 16ms 111 = Reserved Cannot be written with Round-Robin Enabled.

SPICfg (0x57)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SPITimeoutEna
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPITimeoutEna	0	Pseudo-SPI Timeout Enable	0x0: Pseudo-SPI timeout disabled 0x1: Pseudo-SPI timeout enabled

ConfOtp (0x6E)

BIT	7	6	5	4	3	2	1	0
Field	BGDscSkip	SSpcEna	SSpcFullScale[1:0]		SSpcFunc	SSpcSize[1:0]		FpwmFast
Reset		0b0	0b00		0b0	0b00		0b0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BGDscSkip	7	Skip discharge of tank cap if enable is logic high again	0x0: When EN is high again, the BBOUT doesn't get turn on again until the discharge on CAP is completed. 0x1: When EN is high again, the BBOUT turns on without waiting the discharge on CAP to be completed.
SSpcEna	6	Spread Spectrum Enable	0x0: Spread Spectrum off 0x1: Spread Spectrum on
SSpcFullScale	5:4	Spreading amplitude: 0x00 -> 10% 0x01 -> 20% 0x10 -> 30% 0x11 -> 40%	
SSpcFunc	3	Selection between triangular ramp and pseudo-random function.	0x0: Triangular Ramp 0x1: Pseudo-random Function

BITFIELD	BITS	DESCRIPTION	DECODE
SSpcSize	2:1	Bit width of the spread-spectrum output code.	0x0: 3 bits-wide spread spectrum 0x1: 4 bits-wide spread spectrum 0x2: 5 bits-wide spread spectrum 0x3: 6 bits-wide spread spectrum
FpwmFast	0	In round-robin and pseudo-SPI modes, this bit sets the high-performance feature (0 = Fast and 1 = FPWM). In I^2C mode, this bit selects the high-performance feature for status check. BB_LOWPB reads 1 in any of the following three conditions. 1) FPWM = 1, FAST = 0, FpwmFast = 1 2) FPWM = 0, FAST = 1, FpwmFast = 0 3) FPWM = 1, FAST = 1, FpwmFast = 0 or 1	

FuncDef (0x6F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LtchOffFlt	LtchOffThm
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LtchOffFlt	1	Latch Off bit for all faults but the thermal fault: 0 = fault is cleared at the end of a 1s autoretry time; 1 = fault is only cleared by writing 0 on bit BBstEna	0x0: Automatic retry after fault 0x1: Operation is only resumed after cycling (writing 0 and then 1) bit BBstEna
LtchOffThm	0	Latch Off bit for thermal fault: 0 = fault is cleared at the end of a 1s autoretry time; 1 = fault is only cleared by writing 0 on bit BBstEna	0x0: Automatic retry after fault 0x1: Operation is only resumed after cycling (writing 0 and then 1) bit BBstEna

Register Values

The following tables provide the default values for device and register bits for the various available parts.

Table 9. Register Bit Default Values

REGISTER BITS	MAX20362A
BBHalfBW	Full BW
BBstLowEMIB	Nominal Slope
BBstEna	Disabled
BBstFast	Disabled
BBFHighSh	Enabled
BBstActDsc	Enabled
BBstPsvDsc	Enabled
BBstFpwm	Disabled
BBstVSet	3.5V
BBstIPSet2	400mA
BBstIPSet1	400mA
BBIMaxP	1100mA
BBIMaxN	-1400mA
BBstOvloSel	10V
BBIPwpMaxP	200mA
BBstTmoSelLg	31.25µs
BBSimoSel	equal priority
BBstTmoSel	1µs
BBL2P2Sel	2.2µH Inductor
BBstIpPadPEnb	Enable
BBstStepCap	0.5V
BBstVsetCap	9.5V
BBstTankTmoSel	100ms
BBstIPSetCap2	350mA
BBstIPSetCap1	350mA
BBstActDscCap	Disabled
BBstPsvDscCap	Disabled
BBIngenSel	5mA
LDOAct	Disabled
LDOPsv	Disabled
LDOEna	Disabled
ChgModDoneMsk	Masked
BBstOnMsk	Masked
BBIngenDrp	55mV
SPITimeoutEna	Disabled
DVSSource	I2C
LDOVset	0.9V
LDOBBstSupp	Disabled
BGDscSkip	Skip
SSpcEna	Disabled
SSpcFullScale	10%

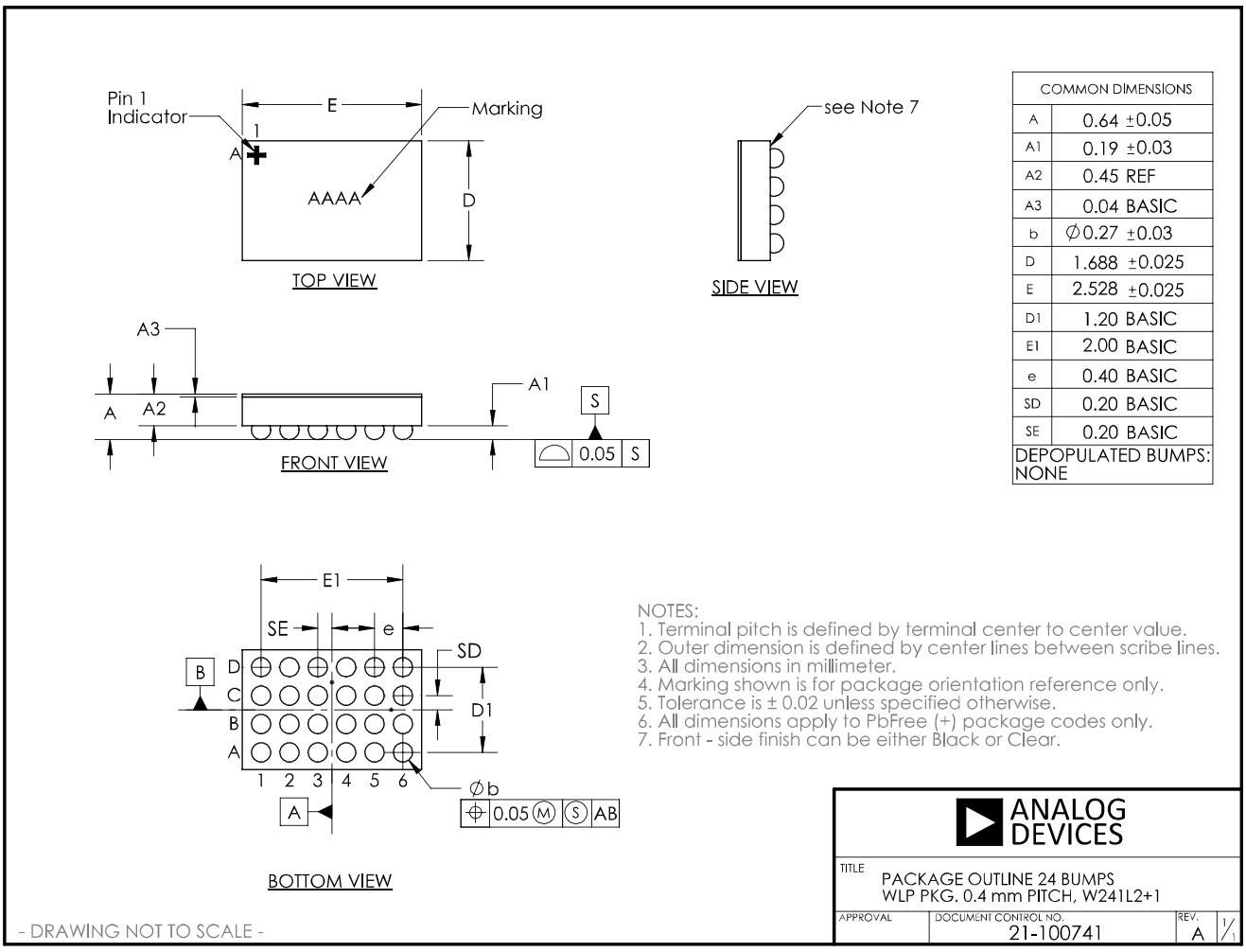
SSpcFunc	Triangular
SSpcSize	3 bit
FpwmFast	Fast
i2c_2nd_sid	0x68
LtchOffFlt	Autoretry Enabled
LtchOffThm	Autoretry Enabled

Table 10. Register Default Values

REGISTER	NAME	MAX20362A
0x00	ChipID	0x01
0x01	BBstCfg0	0x4F
0x02	BBstVSet	0x28
0x03	BBstISet	0xCC
0x04	BBstIMaxN	0x1C
0x05	BBstIMaxP	0x16
0x06	BBstIPwpMaxP	0x04
0x08	BBstCfg1	0x0B
0x09	BBstCfg2	0x00
0x0A	BBstVSetCap	0x0E
0x0B	BBstISetCap	0xAA
0x0C	BBIngenCfg0	0x00
0x10	Status	—
0x12	IngenSts	—
0x13	LDOStatus	—
0x14	Int	0x00
0x15	CommInt	0x00
0x16	IngenInt	0x00
0x17	LDOInt	0x00
0x18	Mask	0x30
0x19	CommMsk	0x20
0x1A	IngenMsk	0x00
0x1B	LDOMsk	0x00
0x1C	BBstIMaxPRb	0x04
0x1D	BBFsmState	0x01
0x1E	BBVset	0x28
0x1F	RRpoint	0x00
0x20	RRVset00	0x00
0x21	RRVset01	0x00
0x22	RRVset02	0x00
0x23	RRVset03	0x00
0x24	RRVset04	0x00
0x25	RRVset05	0x00
0x26	RRVset06	0x00
0x27	RRVset07	0x00
0x28	RRVset08	0x00

0x29	RRVset09	0x00
0x2A	RRVset0A	0x00
0x2B	RRVset0B	0x00
0x2C	RRVset0C	0x00
0x2D	RRVset0D	0x00
0x2E	RRVset0E	0x00
0x2F	RRVset0F	0x00
0x30	RRVset10	0x00
0x31	RRVset11	0x00
0x32	RRVset12	0x00
0x33	RRVset13	0x00
0x40	LDOCfg	0x00
0x41	LDOVSet	0x00
0x50	LockMsk	0x01
0x51	LockUnlock	0x01
0x54	DVSCfg	0x00
0x55	RRCfg1	0x00
0x56	RRCfg2	0x00
0x57	SPICfg	0x00
0x6E	ConfOtp	0x80
0x6F	FuncDef	0x00

OUTLINE DIMENSIONS



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.04 BASIC
b	Ø0.27 ±0.03
D	1.688 ±0.025
E	2.528 ±0.025
D1	1.20 BASIC
E1	2.00 BASIC
e	0.40 BASIC
SD	0.20 BASIC
SE	0.20 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

ANALOG DEVICES

TITLE: PACKAGE OUTLINE 24 BUMPS
WLP PKG. 0.4 mm PITCH, W241L2+1

APPROVAL | DOCUMENT CONTROL NO. 21-100741 | REV. A | 1/1

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION
MAX20362AEWG+	-40°C to +85°C	24 WLP (2.53mm x 1.69mm)	W241L2+1
MAX20362AEWG+T	-40°C to +85°C	24 WLP (2.53mm x 1.69mm)	W241L2+1

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/26	Initial release	—