19-4818; Rev 0; 6/11

EVALUATION KIT AVAILABLE

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

MAX17039

General Description

The MAX17039 is a dual-output, step-down, constant-on-time controller for VR12/IMVP7 CPU core supplies. The controller consists of two high-current-switching power supplies for the CPU and GPU cores. The CPU regulator (regulator A) is a three-phase constant-on-time architecture. The optional third phase is configured with an external MAX17491 driver. The second GPU regulator (regulator B) is also a constant-on-time architecture with only single phase.

Both regulators A and B include true differential voltage and current sensing to improve load-line and current-limit accuracy. Switching frequencies are independently programmable, allowing 100kHz to 600kHz per phase operation. Output overvoltage protection (OVP), undervoltage protection (UVP), and thermal protection ensure effective and highly reliable operation. When any of these protection features detect a fault, the controller shuts down both channels.

Regulator A includes transient-phase overlap, which speeds up the response time, reducing the total output capacitance. It also includes active overshoot suppression to further reduce the required output decoupling capacitance.

The CPU and GPU outputs are controlled independently by writing the appropriate data into a function-mapped register file. A slew-rate controller allows controlled transitions between VID codes with controlled soft-start. The SVID interface also allows each regulator to be individually set into a low-power pulse-skipping state. Individual phases can be shut down based on the processors' operating conditions to optimize efficiency. The MAX17039 is available in a lead-free, 56-pin, 7mm x 7mm TQFN package.

Applications

VR12/IMVP7 CPU Core Power Supplies

Voltage-Positioned Step-Down Converters

Notebooks/Desktops/Servers

Features

- **Three-Phase Quick-PWM™ CPU Core (Regulator A)**
  - **Two Internal Drivers and One External Driver**
  - **Active Overshoot Suppression**
  - **Transient-Phase Overlap Mode**
  - **Dynamic Phase Selection**
  - **Phase-Good Fault Detection (Internal)**
- **One-Phase Quick-PWM with Internal Driver (Regulator B)**
- **8-Bit IMVP7 DAC**
- **±0.4% V_{OUT} Accuracy Over Line, Load, and Temperature**
- **Active Voltage Positioning with Programmable Gain**
- **Accurate Lossless Current Balance**
- **Accurate Droop and Current Limit**
- **Remote Output and Ground Sense**
- **Power-Good Window Comparators (VR__READY)**
- **Output Current Monitors (IMON_)**
- **4.5V to 26V Battery-Input Range**
- **Drives Large Synchronous Rectifier MOSFETs**
- **Programmable 100kHz to 600kHz Switching Frequency**
- **External Thermal-Fault Detection (VR_HOT#) Output**
- **Overvoltage, Undervoltage, and Thermal-Fault Protection**
- **Soft-Start and Soft-Shutdown**
- **Integrated Boost Switches**
- **Low-Profile, 56-Pin TQFN Package**

Ordering Information

PART	PIN-PACKAGE	FEATURE
MAX17039GTN+	56 TQFN-EP*	3-phase + 1 phase (1 external driver)

Note: *This device is specified over the -40°C to +105°C operating temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

ABSOLUTE MAXIMUM RATINGS

V_{CC}, VDDA, VDDB to AGND .....-0.3V to +6V
VDIO, VCLK to AGND .....-0.3V to +6V
CSPA1, CSNA1, CSPA2, CSNA2 to AGND .....-0.3V to +6V
CSPA3, CSNA3 to AGND.....-0.3V to +6V
CSPB, CSNB to AGND.....-0.3V to +6V
THERMA, THERMB, IMAXA, IMAXB, TMAX to AGND .....-0.3V to +6V
VBOOTA, VBOOTB to AGND.....-0.3V to (V_{CC} + 0.3V)
VRA_READY, VRB_READY, VR_HOT#, ALERT# to AGND.....-0.3V to +6V
VR_ENABLE to AGND.....-0.3V to +6V
IMONA, IMONB to AGND .....-0.3V to +6V
FBA, FBB, CCVA, CCVB to AGND .....-0.3V to (V_{CC} + 0.3V)
CCI1, CCI2 to AGND .....-0.3V to (V_{CC} + 0.3V)
GNDSA, GNDSB to AGND.....-0.3V to +0.3V
PWM_OUT, $\overline{DRSKIP}$ to AGND .....-0.3V to (V_{VDDA} + 0.3V)
DLA1, DLA2 to AGND.....-0.3V to (V_{VDDA} + 0.3V)
DLB to AGND.....-0.3V to (V_{VDDB} + 0.3V)
DLG to AGND..... -0.3V to (V_{DDB} + 0.3V)
BSTA1, BSTA2 to VDDA .....-0.3V to +30V
BSTB to VDDB.....-0.3V to +30V
LXA1 to BSTA1, LXA2 to BSTA2.....-6V to +0.3V
LXB to BSTB.....-6V to +0.3V
DHA1 to LXA1 ..... -0.3V to (V_{BSTA1} + 0.3V)
DHA2 to LXA2 ..... -0.3V to (V_{BSTA2} + 0.3V)
DHB to LXB ..... -0.3V to (V_{BSTB} + 0.3V)
TONA, TONB to AGND .....-0.3V to +30V
SRA, SRB to AGND..... -0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 40mW/°C above T_A = +70°C) 3200mW
Operating Temperature Range..... -40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
θ_{JC} ..... 1°C/W
θ_{JA} ..... 25°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, VDDA, VDDB		4.5		5.5	V
DC Output-Voltage Accuracy	$V_{FB\_}$	Measured at FB_ with respect to GNDS_; includes load-regulation error (Note 2)	DAC codes from 0.800V to 1.520V	-0.4		+0.4	%
			DAC codes from 0.370V to 0.795V	-7		+7	mV
			DAC codes from 0V to 0.365V	-20		+20	
Line-Regulation Error		V_{CC} = 4.5V to 5.5V, V_{IN} = 4.5V to 26V			0.1		%
$V_{SETTLED}$ Bit Accuracy		Upward transitions		-16	-10	-4	mV
		Downward transitions		4	10	16	
GNDS_ Input Range				-200		+200	mV
GNDS_ Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.97	1.00	1.03	V/V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Slew-Rate Accuracy		$R_{SR\_}$ = 71.5kΩ	SR = 20mV/µs, fast slew rate	-10		+10	%
			SR = 5mV/µs, slow slew rate, 1/4 default setting	-15		+15	
			SR = 10mV/µs, slow slew rate, 1/2 setting	-15		+15	
		$R_{SR\_}$ = 56.9kΩ (Note 3)	SR = 25mV/µs, fast slew rate	-15		+15	
			SR = 6.25mV/µs, slow slew rate, 1/4 default setting	-20		+20	
			SR = 12.50mV/µs, slow slew rate, 1/2 setting	-20		+20	
		$R_{SR\_}$ = 89.8kΩ (Note 3)	SR = 16mV/µs, fast slew rate	-15		+15	
			SR = 4mV/µs, slow slew rate, 1/4 default setting	-20		+20	
			SR = 8mV/µs, slow slew rate, 1/2 setting	-20		+20	
		$R_{SR\_}$ = 114kΩ	SR = 12.50mV/µs, fast slew rate	-15		+15	
			SR = 3.125mV/µs, slow slew rate, 1/4 default setting	-20		+20	
			SR = 6.25mV/µs, slow slew rate, 1/2 setting	-20		+20	
		Soft-shutdown		-3	-1.2		mV/µs
DHA_ On-Time (Note 3)	t_{ONA}	V_{IN} = 12V	R_{TONA} = 96.75kΩ (540kHz)	156	183	210	ns
			R_{TONA} = 200kΩ (270kHz)	329	366	403	
			R_{TONA} = 303.25kΩ (180kHz)	468	550	633	
DHB On-Time (Note 3)	t_{ONB}	V_{IN} = 12V	R_{TONB} = 96.75kΩ (660kHz)	127	149	171	ns
			R_{TONB} = 200kΩ (300kHz + 10%)	270	300	330	
			R_{TONB} = 303.25kΩ (220kHz)	383	450	518	

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH (Note 4)		250	300	ns
Minimum PWM_OUT Pulse Width				40		ns
BIAS CURRENTS						
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, SVID code = 1.2V, FB_ forced above the regulation point		6	12	mA
Quiescent Supply Current (VDD_)	I_{DD}	T_A = +25°C, measured at VDD_, SVID code = 1.2V, FB_ forced above the regulation point		0.02	1	µA
FB_ Input Bias Current		(Note 2)	-1.5		+1.5	µA
GNDS_ Input Bias Current		-0.3V < $V_{GNDS\_}$ < +0.3V	-20		+20	µA
TON_ Shutdown Input Current		T_A = +25°C, VR_ENABLE = AGND, V_{IN} = 26V, V_{CC} = $V_{VDD\_}$ = 0V or 5V		0.01	1	µA
Shutdown Supply Current (V_{CC})				6	15	µA
Shutdown Supply Current (VDD_)		T_A = +25°C, measured at VDD_, VR_ENABLE = AGND		0.01	1	µA
FAULT PROTECTION						
Output Overvoltage-Protection Threshold	V_{OVP}	Skip mode: measured after output reaches the regulation voltage, or PWM mode; measured at FB_ with respect to the voltage target set by the SVID code	260	300	340	mV
		Soft-start, soft-shutdown, skip mode, and output have not reached the regulation voltage; measured at FB_	1.78	1.82	1.86	
		Minimum OVP threshold; measured at FB_		0.8		V
Output Overvoltage-Propagation Delay	t_{OVP}	FB_ forced 25mV above trip threshold		10		µs
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB_ with respect to unloaded output voltage	-450	-400	-350	mV
VR__READY High Threshold		Measured at FB_ with respect to the SVID code; hysteresis = 20mV typical	160	200	240	mV
VR__READY Low Threshold		Measured at FB_ with respect to the SVID code; hysteresis = 20mV typical	-350	-300	-250	mV
VR__READY Output-Low Voltage		I_{SINK} = 3mA			0.4	V
VR__READY Leakage Current		T_A = +25°C, high state, VR__READY forced to 5V			1	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VR__READY Startup Delay and Transitions Blanking Time	$t_{VR\_\_READY}$	Measured from the time when FB_ reaches the target voltage			20		µs
CSN_ Pulldown Resistance in Shutdown		VR_ENABLE = AGND (not switching)			20		Ω
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 50mV typical hysteresis, controller disabled below this level		4.05	4.25	4.45	V
THERMAL PROTECTION							
VR_HOT# Trip Threshold		Measured at THERM_ with respect to V_{CC} falling edge		49.4		50.6	%
VR_HOT# Delay	$t_{VRHOT\#}$	THERM _forced 25mV below the VR_HOT# trip threshold, falling edge			10		µs
Thermal-Zone Registers Trip Points		Thermal zone comparator trip points, measured with respect to V_{CC}; voltage threshold corresponding to T_{MAX} x (1-3 x N%), N = -1 to 6	Bit 0	63.4	64.4	65.1	%
			Bit 1	61.0	62	62.7	
			Bit 2	58.6	59.6	60.4	
			Bit 3	56.2	57.2	58	
			Bit 4	53.9	54.8	55.6	
			Bit 5	51.5	52.4	53.2	
			Bit 6	49.2	50	50.8	
			Bit 7	46.8	47.6	48.5	
THERM_ Input Leakage	$I_{THRM\_}$	$V_{THRM\_}$ = 0V to 5V		-1	+0.01	+1	µA
Thermal-Shutdown Threshold	t_{SHDN}	Typical hysteresis = 15°C			+160		°C
VALLEY CURRENT LIMIT AND DROOP							
Current-Limit Threshold Voltage (Positive) Set Through IMAX_	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$	IMAX_ = AGND	11	15	19	mV
			$V_{IMAX\_}$ = 2V	16	20	24	
			$V_{IMAX\_}$ = 3V	21	25	29	
			$V_{IMAX\_}$ = V_{CC}	26	30	34	
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	$V_{CSP\_}$ - $V_{CSN\_}$, nominally -125% of V_{LIMIT}		-4		+4	mV
Current-Limit Threshold Voltage (Zero Crossing)	V_{ZX}	V_{PGND} - $V_{LX\_}$			0.33		mV
Current-Balance Offset Voltage		(V_{CSPA1} - V_{CSNA1}) - (V_{CSPAX} - V_{CSNAX}) at $I_{CCI\_}$ = 0A, X = 2, 3		-1.6		+1.6	mV
CSP_, CSN_ Common-Mode Input Range				0		2	V
CSP_ Input Current	$I_{CSP\_}$	T_A = +25°C		-0.2		+0.2	µA
CSN_ Input Current	$I_{CSN\_}$				50		µA
DC Droop Amplifier (G_{MD}) Offset		($V_{CSP\_}$ - $V_{CSN\_}$) at $I_{FB\_}$ = 0		-1.0		+1.0	mV
DC Droop Amplifier (G_{MD}) Transconductance	GMD_	$\Delta I_{FB\_}/\Delta(V_{CSP\_} - V_{CSN\_})$; FB_ = CSN_ = 0.45V to 1.52V, and ($V_{CSP\_}$ - $V_{CSN\_}$) = -40mV to +40mV		588	600	608	µS

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GLITCH CATCHER							
Firing Threshold	V_{TH}	High threshold = multiple of VID code		Code + 25mV	Code + 33mV	Code + 40mV	V
		Hysteresis			0.012		
Off-Time					420		ns
On-Time		V_{CPU} = 1.200V			750		ns
		V_{CPU} = 1.500V			600		
		V_{CPU} = 0.400V			2000		
GATE DRIVERS							
LX_ Input-Voltage Range				-1		+26	V
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ – LX_ forced to 5V	High state (pullup)		0.9	2.5	Ω
			Low state (pulldown)		0.7	2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			0.7	2.0	Ω
		Low state (pulldown)			0.25	0.8	
DLG Gate-Driver On-Resistance	$R_{ON(DLG)}$	High state (pullup)			0.9	2.5	Ω
		Low state (pulldown)			0.7	2.0	
DH_ Gate-Driver Source Current	$I_{DH(SOURCE)}$	DH_ forced to 2.5V, BST_ – LX_ forced to 5V			2.2		A
DH_ Gate-Driver Sink Current	$I_{DH(SINK)}$	DH_ forced to 2.5V, BST_ – LX_ forced to 5V			2.7		A
DL_ Gate-Driver Source Current	$I_{DL(SOURCE)}$	DL_ forced to 2.5V			2.7		A
DL_ Gate-Driver Sink Current	$I_{DL(SINK)}$	DL_ forced to 2.5V			8		A
Driver Propagation Delay		DH_ low to DL_ high		12	30	45	ns
		DL_ low to DH_ high		12	30	45	
DL_ Transition Time		DL_ falling, C_{DL} = 3nF			20		ns
		DL_ rising, C_{DL} = 3nF			20		
DH_ Transition Time		DH_ falling, C_{DH} = 3nF			20		ns
		DH_ rising, C_{DH} = 3nF			20		
Internal BST_ Switch On-Resistance	R_{BST}	I_{BST} = 10mA, $V_{VDD\_}$ = 5V			10	20	Ω
CURRENT MONITOR (IMON_)							
Current-Monitor Output IMON_ Voltage for Typical Operating Conditions	V_{IMON}	$I_{IMON\_}$ = 0µA (offset), ($V_{CSP\_}$ - $V_{CSN\_}$) = 0mV, $R_{IMON\_}$ = 10kΩ			0		V
Current-Monitor Output IMON_ Maximum Output Level		Clamp level to protect the processor, I_{CLAMP} = 50µA			1.1	1.15	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Monitor Gain Referred to Output Voltage $V_{IMON\_}$ - V_{GNDS}					1		V/V
Current-Monitor Gain Referred to ($V_{CSP\_}$ - $V_{CSN\_}$)		($V_{CSP\_}$ - $V_{CSN\_}$) equal to IMAX_ setting, set gain to correspond to a full-scale voltage of 1V typical		2.360	2.430	2.500	µA/mV
IMAX_ Accuracy				-5		+5	%
IMAX_ Registers Trip Points		Current zone comparator trip points, measured with respect to IMON_ - GNDS_	B0	475	500	525	mV
			B1	575	600	625	
			B2	675	700	725	
			B3	775	800	825	
			B4	875	900	925	
			B5	925	950	975	
			B6	975	1000	1025	
			B7	1075	1100	1125	
LOGIC AND I/O							
Logic-Input High Voltage	V_{IH}	VR_ENABLE		0.67			V
Logic-Input Low Voltage	V_{IL}	VR_ENABLE				0.33	V
Logic-Input Current		VR_ENABLE, T_A = +25°C		-1		+1	µA
		VBOOTA, IMAXA, IMAXB, TMAX, VBOOTB, T_A = +25°C		-1		+1	
Four-Level Logic Thresholds		TMAX, IMAXA, IMAXB, VBOOTA, VBOOTB	Low			0.4	V
			2V	1.65		2.35	
			3V	2.75		3.85	
			High	V_{CC} - 0.4			
PWM_OUT, $\overline{DRSKIP}$ High Voltage		I_{SOURCE} = 3mA		V_{CC} - 0.4			V
PWM_OUT, $\overline{DRSKIP}$ Low Voltage		I_{SINK} = 3mA				0.4	V
SVID INTERFACE							
Logic-Input High Voltage VCLK, VDIO	V_{IH}			0.65			V
Logic-Input Low Voltage VCLK, VDIO	V_{IL}					0.45	V
Output Low-Level VDIO	V_{OH}	I_{SINK} = 30mA				0.4	V
VDIO, ALERT# Out On-Resistance	$R_{ON(IO)}$			3		13	Ω
Logic-Input Current VCLK, VDIO				-10		+10	µA

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Off-State Leakage Current ALERT#		$V_{ALERT\#}$ = 3.3V, T_A = +25°C			1	µA
Input Capacitance	C_{IN}	(Note 3)			4	pF
VCLK Frequency	f_{CLK}	(Note 3)	5.5	25	33	MHz
VCLK High Time	t_{HIGH}	Specified as a percentage of t_{CLK} period	45			%
VCLK Low Time	t_{LOW}	Specified as a percentage of t_{CLK} period	45			%
Rise Time	t_{RISE}	(Note 3)	0.25		2.5	ns
Fall Time	t_{FALL}	(Note 3)	0.25		2.5	ns
Duty Cycle		(Note 3)	45		55	%
SVID Inactivity Timeout	t_{RSTNA}				4	µs

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, VDDA, VDDB		4.5		5.5	V
DC Output Voltage Accuracy	$V_{FB\_}$	Measured at FB_ with respect to GNDS_; includes load regulation error (Note 2)	DAC codes from 0.800V to 1.520V	-0.7		+0.7	%
			DAC codes from 0.370V to 0.795V	-10		+10	mV
			DAC codes from 0 to 0.365V	-20		+20	
$V_{SETTLED}$ Bit Accuracy		Upward transitions		-17		-3	mV
		Downward transitions		3		17	
GNDS_ Input Range				-200		+200	mV
GNDS_ Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.97		1.03	V/V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Slew-Rate Accuracy		$R_{SR\_}$ = 71.5kΩ	SR = 20mV/µs, fast slew rate	-10		+10	%
			SR = 5mV/µs, slow slew rate, 1/4 default setting	-15		+15	
			SR = 10mV/µs, slow slew rate, 1/2 setting	-15		+15	
		$R_{SR\_}$ = 56.9kΩ	SR = 25mV/µs, fast slew rate	-15		+15	
			SR = 6.25mV/µs, slow slew rate, 1/4 default setting	-20		+20	
			SR = 12.5mV/µs, slow slew rate, 1/2 setting	-20		+20	
		$R_{SR\_}$ = 89.8kΩ	SR = 16mV/µs, fast slew rate	-15		+15	
			SR = 4mV/µs, slow slew rate, 1/4 default setting	-20		+20	
			SR = 8mV/µs, slow slew rate, 1/2 setting	-20		+20	
		$R_{SR\_}$ = 114kΩ	SR = 12.5mV/µs, fast slew rate	-15		+15	
			SR = 3.125mV/µs, slow slew rate, 1/4 default setting	-20		+20	
			SR = 6.25mV/µs, slow slew rate, 1/2 setting	-20		+20	
		Soft-shutdown		-3			mV/µs
DHA_ On-Time (Note 3)	t_{ONA}	V_{IN} = 12V	R_{TONA} = 96.75kΩ (540kHz), 183ns nominal	156	183	210	ns
			R_{TONA} = 200kΩ (270kHz), 366ns nominal	329	366	403	
			R_{TONA} = 303.25kΩ (180kHz), 550ns nominal	468	550	633	

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DHB On-Time (Note 3)	t_{ONB}	V_{IN} = 12V	R_{TONB} = 96.75kΩ (660kHz), 149ns nominal	127	149	171	ns
			R_{TONB} = 200kΩ (330kHz), 300ns nominal	270	300	330	
			R_{TONB} = 303.25kΩ (220kHz), 450ns nominal	383	450	518	
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	Measured at DH_				300	ns
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, SVID code = 1.2V, FB_ forced above the regulation point				12	mA
FB_ Input Bias Current				-1.5		+1.5	µA
GNDS_ Input Bias Current		-0.3V < $V_{GNDS\_}$ < +0.3V		-20		+20	µA
Output Overvoltage-Protection Threshold	V_{OVP}	Skip mode, measured after output reaches the regulation voltage or PWM mode: measured at FB_ with respect to the voltage target set by the SVID code		260		340	mV
		Soft-start, soft-shutdown, skip mode, and output have not reached the regulation voltage; measured at FB_		1.78		1.86	V
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB_ with respect to unloaded output voltage		-450		-350	mV
VR__READY High Threshold		Measured at FB_ with respect to the SVID code, hysteresis = 20mV typical		160		240	mV
VR__READY Low Threshold		Measured at FB_ with respect to the SVID code, hysteresis = 20mV typical		-350		-250	mV
VR__READY Output Low Voltage		I_{SINK} = 3mA				0.4	V
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 50mV typical hysteresis		4.05		4.45	V
VR_HOT# Trip Threshold		Measured at THERM_ with respect to V_{CC} falling edge, specify as % error for all temp MAX DAC code settings; typical hysteresis = 100mV		49.4		50.6	%

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Thermal-Zone Registers Trip Points		Thermal-zone comparator trip points, measured with respect to V_{CC}, voltage threshold corresponding to T_{MAX} x (1 - 3 x N%), N = -1 to +6	Bit 0	63.4		65.1	%
			Bit 1	61.0		62.7	
			Bit 2	58.6		60.4	
			Bit 3	56.2		58	
			Bit 4	53.9		55.6	
			Bit 5	51.5		53.2	
			Bit 6	49.2		50.8	
			Bit 7	46.8		48.5	
THERM_ Input Leakage	$I_{THRM\_}$	$V_{THRM\_}$ = 0V to 5V		-4		+4	µA
Current-Limit Threshold Voltage (Positive) Set Through IMAX_	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_\_}$	IMAX_ = AGND	10.5		19.5	mV
			$V_{IMAX\_}$ = 2V	15.5		24.5	
			$V_{IMAX\_}$ = 3V	20.5		29.5	
			IMAX_ = V_{CC}	25.5		34.5	
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	$V_{CSP\_}$ - $V_{CSN\_}$, nominally -125% of V_{LIMIT}		-4		+4	mV
Current-Balance Offset Voltage		(V_{CSPA1} - V_{CSNA1}) - (V_{CSPAX} - V_{CSNAX}) at $I_{CSI\_}$ = 0A, X = 2, 3		-2		+2	mV
CSP_, CSN_ Common-Mode Input Range				0		2	V
DC Droop Amplifier (GMD) Offset		(V_{CSP} - V_{CSN}) at $I_{FB\_}$ = 0		-1.0		+1.0	mV
DC Droop Amplifier (GMD_) Transconductance	$G_{MD\_}$	$\Delta I_{FB\_}/\Delta(V_{CSP}$ - $V_{CSN})$; $V_{FB\_}$ = $V_{CSN\_}$ = 0.45V to 1.52V, and ($V_{CSP\_}$ - $V_{CSN\_}$) = -40mV to +40mV		585		611	µS
Glitch Catcher Firing Threshold	V_{TH}	High threshold = multiple of VID code		Code + 22mV		Code + 43mV	V
LX_ Input Voltage Range				-1		+26	V
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V	High state (pullup)			2.5	Ω
			Low state (pulldown)			2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)				2.0	Ω
		Low state (pulldown)				0.8	
DLG Gate-Driver On-Resistance	$R_{ON(DLG)}$	High state (pullup)				2.5	Ω
		Low state (pulldown)				2.0	
Driver Propagation Delay		DH_ low to DL_ high		12		45	ns
		DL_ low to DH_ high		12		45	
Internal BST_ Switch On-Resistance	R_{BST}	$I_{BST\_}$ = 10mA, $V_{VDD\_}$ = 5V				20	Ω

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT MONITOR (IMON_)							
Current Monitor Output IMON_ Maximum Output Level		Clamp level to protect the processor, I_{CLAMP} = 50µA				1.15	V
Current Monitor Gain Referred to (V_{CSP} - V_{CSN})		(V_{CSP} - V_{CSN}) equal to IMAX_ setting; set gain to correspond to a full-scale voltage of 1V typical		2.360		2.500	µA/mV
IMAX_ Accuracy				-5		+5	%
IMAX_ Register Trip Points		Current-zone comparator trip points, measured with respect to IMON_ - GNDS_	B0	475		525	mV
			B1	575		625	
			B2	675		725	
			B3	775		825	
			B4	875		925	
			B5	925		975	
			B6	975		1025	
			B7	1075		1130	
LOGIC AND I/O							
Logic-Input High Voltage	V_{IH}	VR_ENABLE		0.67			V
Logic-Input Low Voltage	V_{IL}	VR_ENABLE				0.33	V
Four-Level Logic Thresholds		TMAX, IMAXA, IMAXB, VBOOTA, VBOOTB	Low			0.4	V
			2V	1.65		2.35	
			3V	2.75		3.85	
			High	V_{CC} - 0.4			
PWM_OUT, $\overline{DRSKIP}$ High Voltage		I_{SOURCE} = 3mA		V_{CC} - 0.4			V
PWM_OUT, $\overline{DRSKIP}$ Low Voltage		I_{SINK} = 3mA				0.4	V
SVID INTERFACE							
Logic-Input High Voltage VCLK, VDIO	V_{IH}			0.65			V
Logic-Input Low Voltage VCLK, VDIO	V_{IL}					0.45	V
Output Low-Level VDIO	V_{OH}	I_{SINK} = 30mA				0.4	V
VDIO, ALERT# Out On-Resistance	$R_{ON(IO)}$			3		13	Ω

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{VDD\_}$ = V_{VR_ENABLE} = 5V, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = $V_{CCI\_}$ = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.2000V; V_{SVID} = 1.200V, FPWM mode; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic-Input Current VCLK, VDIO			-10		+10	µA
Input Capacitance	C_{IN}				4	pF
VCLK Frequency	f_{CLK}		5.5		33	MHz
VCLK High Time	t_{HIGH}	Specified as a percentage of t_{CLK} period	45			%
VCLK Low Time	t_{LOW}	Specified as a percentage of t_{CLK} period	45			%
Rise Time	t_{RISE}		0.25		2.5	ns
Fall Time	t_{FALL}		0.25		2.5	ns
Duty Cycle			45		55	%
SVID Inactivity Timeout	t_{RSTNA}				4	µs

Note 2: The equation for the target voltage V_{TARGET} is:
V_{TARGET} = the slew-rate-controlled version of either V_{DAC}
where:
V_{DAC} = 0V for shutdown, V_{DAC} = V_{BOOT} during startup, otherwise:
V_{DAC} = V_{VID} (the V_{VID} voltages for all possible VID codes are given in Table 3 and V_{OFFSET} = the negative or positive offset to the output voltage based on the voltage set from the offset register and the mode of operation (startup, shutdown, deeper sleep, or normal operation), as defined elsewhere in this document. In pulse-skipping mode, the output rises by approximately 1.5% when transitioning from continuous conduction to no load.

Note 3: The listed specification is guaranteed by design.

Note 4: On-time and minimum off-time specifications are measured from 50% to 50% at the DH_ pin, with LX_ forced to 0V, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

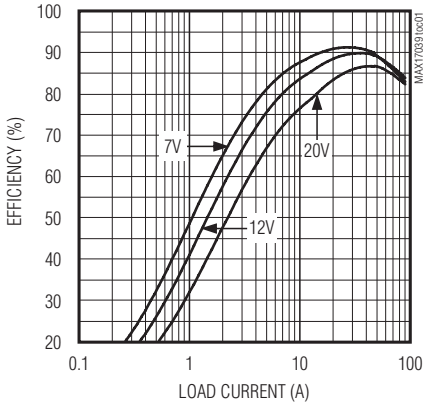
Note 5: Specifications to T_A = -40°C and +105°C are guaranteed by design, not production tested.

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

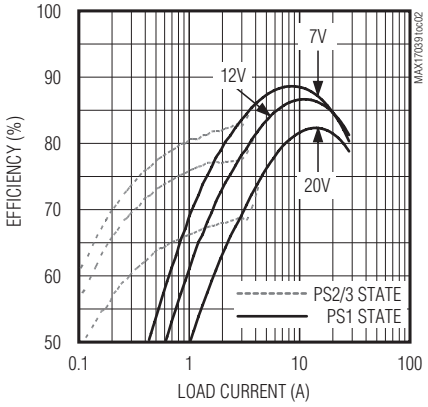
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = $V_{VDD\_}$ = 5V, VR_ENABLE = V_{CC}, V_{SVID} = 1.2V, unless otherwise specified.)

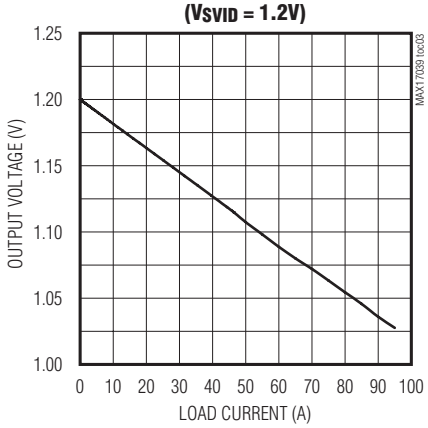
REG A EFFICIENCY vs. LOAD CURRENT IN PS0 STATE (V_{SVID} = 1.2V)



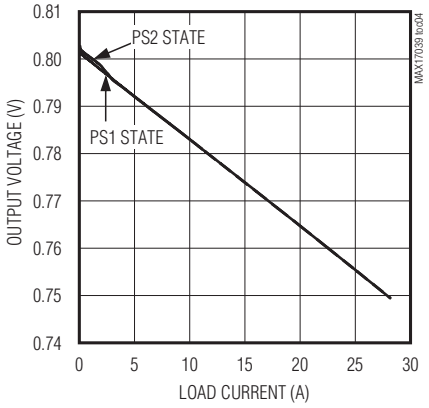
REG A EFFICIENCY vs. LOAD CURRENT (V_{SVID} = 0.8V)



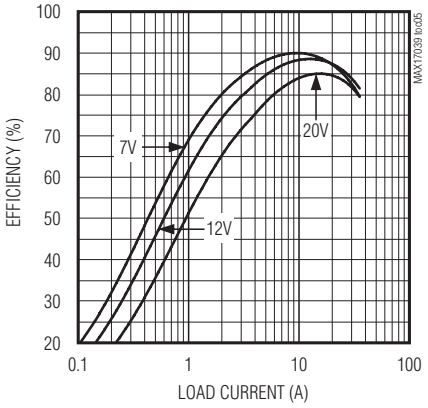
REG A OUTPUT VOLTAGE vs. LOAD CURRENT IN PS0 STATE (V_{SVID} = 1.2V)



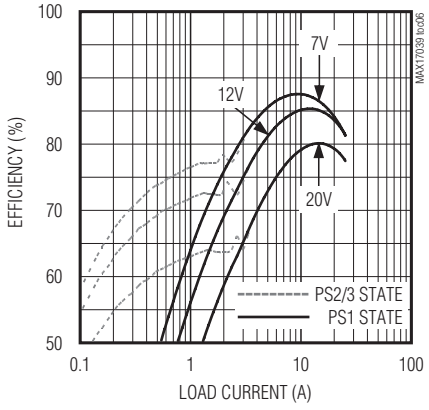
REG A OUTPUT VOLTAGE vs. LOAD CURRENT (V_{SVID} = 0.8V)



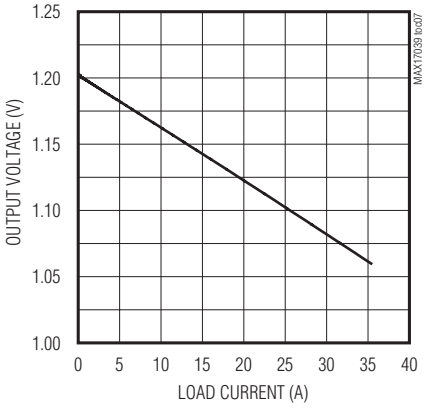
REG B EFFICIENCY vs. LOAD CURRENT IN PS0 STATE (V_{SVID} = 1.2V)



REG B EFFICIENCY vs. LOAD CURRENT (V_{SVID} = 0.8V)



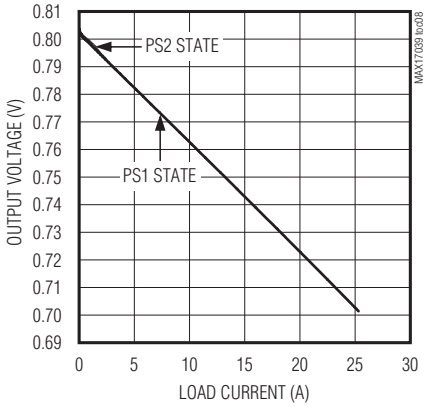
REG B OUTPUT VOLTAGE vs. LOAD CURRENT IN PS0 STATE (V_{SVID} = 1.2V)



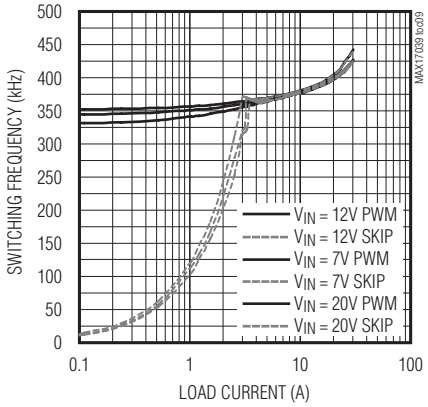
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = $V_{VDD\_}$ = 5V, VR_ENABLE = V_{CC}, V_{SVID} = 1.2V, unless otherwise specified.)

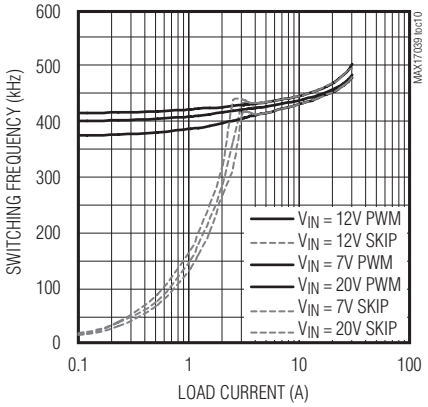
REG B OUTPUT VOLTAGE vs. LOAD CURRENT (V_{SVID} = 0.8V)



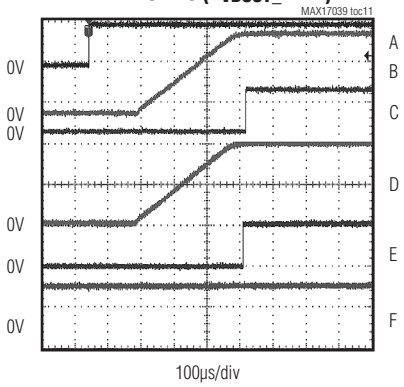
REG A SWITCHING FREQUENCY vs. LOAD CURRENT (V_{SVID} = 1.2V)



REG B SWITCHING FREQUENCY vs. LOAD CURRENT (V_{SVID} = 1.2V)



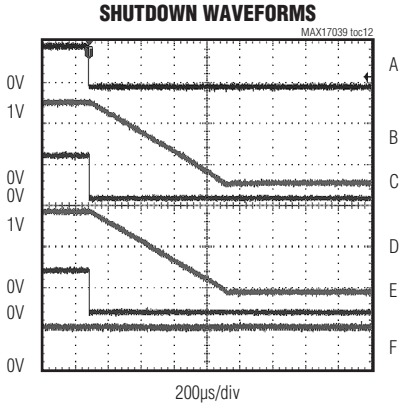
NONZERO VBOOT STARTUP WAVEFORMS ($V_{VBOOT\_}$ = 1V)



A. V_{VR_ENABLE}, 5V/div
B. V_{OUTA}, 500m/div
C. V_{VRA_READY}, 1V/div
D. V_{OUTB}, 500m/div
E. V_{VRB_READY}, 1V/div
F. $V_{ALERT\#}$, 1V/div

V_{IN} = 12V
V_{VBOOTA} = V_{VBOOTB} = 1V

SHUTDOWN WAVEFORMS



A. V_{VR_ENABLE}, 5V/div
B. V_{OUTA}, 500m/div
C. V_{VRA_READY}, 1V/div
D. V_{OUTB}, 500m/div
E. V_{VRB_READY}, 1V/div
F. $V_{ALERT\#}$, 1V/div

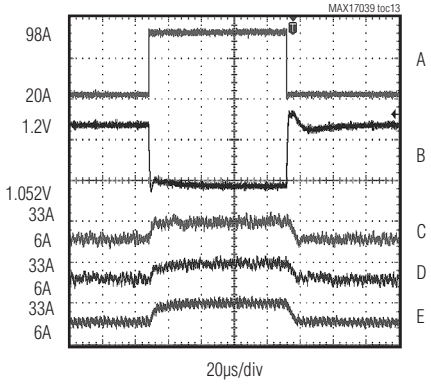
V_{IN} = 12V
V_{LOADA} = 5A
V_{LOADB} = 5A

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = $V_{VDD\_}$ = 5V, VR_ENABLE = V_{CC}, V_{SVID} = 1.2V, unless otherwise specified.)

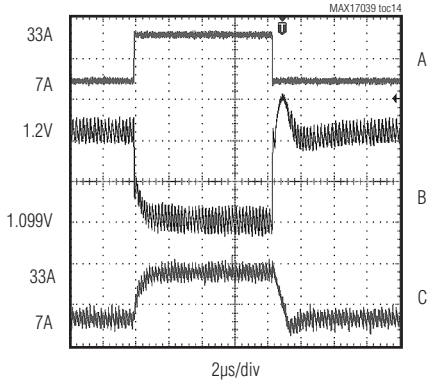
REGULATOR A LOAD-TRANSIENT RESPONSE



A. I_{OUTA} = 20A TO 98A, 50A/div
B. V_{OUTA}, 100m/div
C. I_{LX1}, 50A/div
D. I_{LX2}, 50A/div
E. I_{LX3}, 50A/div

V_{IN} = 12V
V_{OUT1} = 1.2V
I_{LOADA} = 20A TO 98A TO 20A
PWM MODE

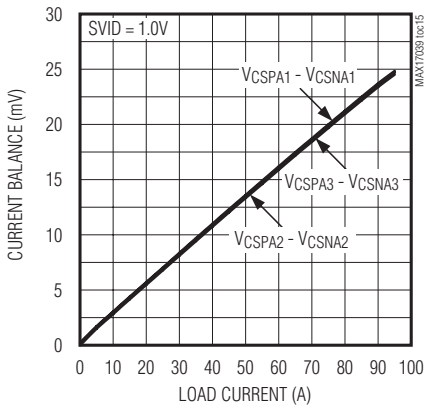
REGULATOR B LOAD-TRANSIENT RESPONSE



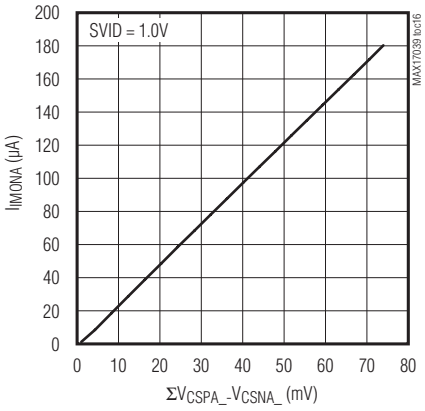
A. I_{OUTB} = 7A TO 33A, 25A/div
B. V_{OUTB}, 50mV/div
C. I_{LXB}, 25A/div

V_{IN} = 12V
V_{OUT1} = 1.2V
I_{LOADA} = 7A TO 33A TO 7A
PWM MODE

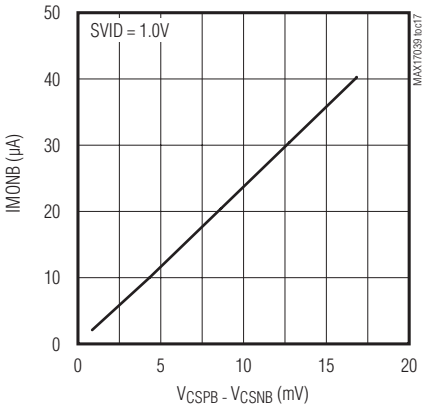
CURRENT BALANCE vs. LOAD CURRENT



I_{IMONA} vs. LOAD CURRENT

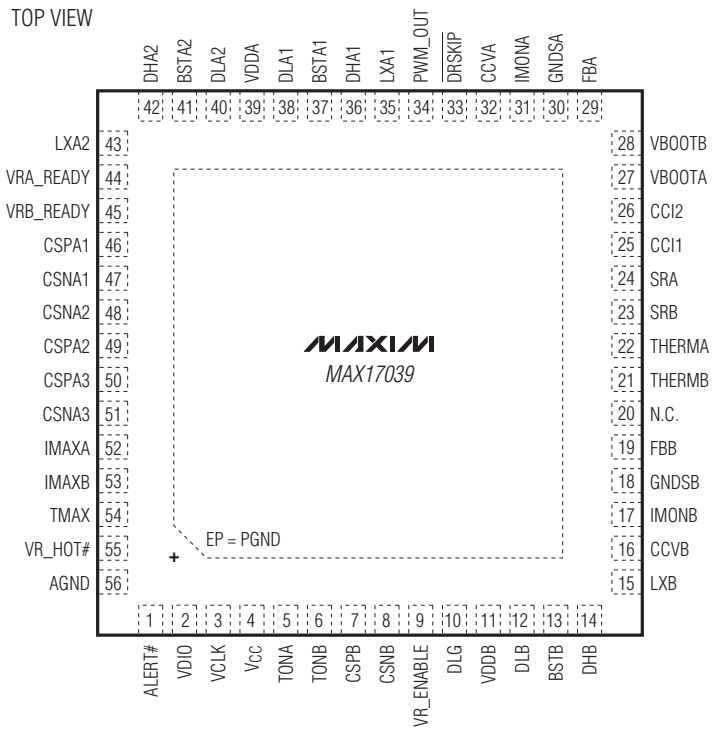


I_{IMONB} vs. LOAD CURRENT



Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

Pin Configuration



TQFN

Pin Description

PIN	NAME	FUNCTION
1	ALERT#	Serial VID Alert Output. ALERT# is in the high state in shutdown.
2	VDIO	Serial VID I/O Pin
3	VCLK	Serial VID Clock Input
4	V_{CC}	Controller Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to AGND with a 1µF or greater ceramic capacitor.
5	TONA	Switching Frequency Setting Input for Regulator A. An external resistor between the input power source and this pin sets the switching frequency per phase according to the following equation: $f_{SW} = 1/(K_P \times (R_{TONA} + 6.5k\Omega))$ where K_P = 17.89pF. R_{TONA} is high impedance in shutdown.
6	TONB	Switching Frequency-Setting Input for Regulator B. An external resistor between the input power source and this pin sets the switching frequency per phase according to the following equation: $f_{SW} = 1/(K_P \times (R_{TONB} + 6.5k\Omega))$ where K_P = 14.63pF. R_{TONB} is high impedance in shutdown.

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

Pin Description (continued)

PIN	NAME	FUNCTION
7	CSPB	Positive Input of the Output Current Sense of Phase 1 of Regulator B. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
8	CSNB	Negative Input of the Output Current Sense of Phase 1 of Regulator B. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. A 20Ω discharge FET is enabled from CSNB to AGND when regulator B completes soft-shutdown.
9	VR_ENABLE	Regulators A and B Shutdown Control Input. This input cannot withstand the battery voltage. Connect to V_{CC} for normal operation. Connect to ground to put the MAX17039 into its shutdown state. When $V_{VBOOT\_}$ = 0V and VR_ENABLE is pulled high, the SVID interface is activated, and the output is regulated to 0V. When $2V \le V_{VBOOT\_} \le V_{CC}$ (nonzero VBOOT_) and VR_ENABLE is pulled high, the SVID interface is activated, and the output voltage ramps up to the programmed boot voltage at the slow slew rate set by the SR_ input. During the transition from normal operation to shutdown, the output voltages ramp down at -1.2mV/µs (typ). Toggling VR_ENABLE resets the fault latches for regulators A and B.
10	DLG	Glitch Catcher Driver Output. DLG swings from VDDB to AGND. DLG is forced low in shutdown. DLG is also forced low when an output overvoltage fault is detected.
11	VDDB	Supply Voltage Input for the DLB and DLG Drivers. VDDB is the supply voltage used to internally recharge the BSTB flying capacitor during the on-time of the DLB. Connect VDDB to the 4.5V to 5.5V system supply voltage. Bypass VDDB to power ground with a 1µF or greater ceramic capacitor.
12	DLB	Regulator B, Low-Side Gate-Driver Output. DLB swings from VDDB to AGND. DLB is forced low in shutdown. DLB is forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DLB is forced low in skip mode whenever an inductor current zero crossing (AGND - LXB) is detected.
13	BSTB	Regulator B, Boost Flying Capacitor Connection for the DHB High-Side Gate Driver. An internal switch regulator between VDDB and BSTB charges the flying capacitor during the time the low-side FET is on.
14	DHB	Regulator B High-Side Gate-Driver Output. DHB swings from LXB to BSTB. DHB is low in shutdown.
15	LXB	Regulator B Inductor Connection. LXB is the internal lower supply rail for the DHB high-side gate driver. Also used as an input to the regulator B zero-crossing comparator.
16	CCVB	Integrator Capacitor Connection for Regulator B. Connect a 100pF to 10nF (470pF, typ) capacitor from CCVB to AGND to set the integration time constant. The integrator is internally disabled when the part is in skip mode and the output is above regulation.
17	IMONB	Current-Monitor Output for Regulator B: $I_{(IMONB)} = G_{M(IMONB)} \times (V_{CSPB} - V_{CSNB})$ where $G_{M(IMONB)}$ = 2.43mS (typ). An external resistor R_{IMONB} between IMONB and GNDSB sets the current-monitor output voltage: $V_{IMONB} = I_{LOAD} \times R_{SENSB} \times G_{M(IMONB)} \times R_{IMONB}$ where R_{SENSEB} is the value of the effective current-sense resistance. Choose R_{IMONB} such that V_{IMONB} is 999mV at the maximum expected load current IMAXB. IMONB is high impedance when the MAX17039 is in shutdown.

Pin Description (continued)

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>18</td><td>GNDSB</td><td>Feedback Remote-Sense Input, Negative Side for Regulator B. Normally connected to AGND directly at the load. GNDSB internally connects to a transconductance amplifier that fine-tunes the output voltage—compensating for voltage drops from the regulator ground to the load ground.</td></tr>
<tr><td>19</td><td>FBB</td><td>Feedback Input for Regulator B. Output of the DC voltage-positioning transconductance amplifier. Connect a resistor R_{FBB} between FBB and the positive side of the feedback remote sense to set the DC steady-state droop based on the voltage-positioning gain requirement:
$R_{FBB} = R_{DROOPB}/(R_{SENSEB} \times G_{MDB})$
where R_{DROOPB} is the desired voltage-positioning slope and G_{MDB} = 600µs (typ). R_{SENSEB} is the value of the current-sense resistors that are used to provide the (CSPB, CSNB) current-sense voltages. DC droop can be disabled by shorting FBB to the positive remote-sense point. FBB is high impedance in shutdown.</td></tr>
<tr><td>20</td><td>N.C.</td><td>No Connection</td></tr>
<tr><td>21</td><td>THERMB</td><td>Thermistor Input B. Connect a thermistor to this input. An internal bridge circuit is used to condition the voltage signal from the thermistor prior to digitization with an ADC. A 1% thermistor must be used to meet the ±3°C accuracy required for measuring T_{MAX}.</td></tr>
<tr><td>22</td><td>THERMA</td><td>Thermistor Input A. Connect a thermistor to this input. An internal bridge circuit is used to condition the voltage signal from the thermistor prior to digitization with an ADC. A 1% thermistor must be used to meet the ±3°C accuracy required for measuring T_{MAX}.</td></tr>
<tr><td>23</td><td>SRB</td><td>Fast Slew-Rate Adjustment for Regulator B. Connect a 1% accurate resistor R_{SRB} from SRB to AGND to set the fast slew rate. The MAX17039 digitizes the voltage at SRB to set one of four discrete slew rates. The selected fast and slow slew rates are reflected in registers 24h and 25h, respectively.
<table>
<tr><th>R_{SRB} (kΩ)</th><th>FAST SLEW RATE (mV/µs)</th><th>SLOW SLEW RATE (mV/µs)</th></tr>
<tr><td>114</td><td>±12.5</td><td>±3.125</td></tr>
<tr><td>89.8</td><td>±16</td><td>±4</td></tr>
<tr><td>71.5</td><td>±20</td><td>±5</td></tr>
<tr><td>56.9</td><td>±25</td><td>±6.25</td></tr>
</table></td></tr>
<tr><td>24</td><td>SRA</td><td>Fast Slew-Rate Adjustment for Regulator A. Connect a 1% accurate resistor R_{SRA} from SRA to GND to set the fast slew rate. The MAX17039 digitizes the voltage at SRA to set one of four discrete slew rates. The selected fast and slow slew rates are reflected in registers 24h and 25h, respectively.
<table>
<tr><th>R_{SRB} (kΩ)</th><th>FAST SLEW RATE (mV/µs)</th><th>SLOW SLEW RATE (mV/µs)</th></tr>
<tr><td>114</td><td>±12.5</td><td>±3.125</td></tr>
<tr><td>89.8</td><td>±16</td><td>±4</td></tr>
<tr><td>71.5</td><td>±20</td><td>±5</td></tr>
<tr><td>56.9</td><td>±25</td><td>±6.25</td></tr>
</table></td></tr>
<tr><td>25</td><td>CCI1</td><td>Current-Balance Compensation for Regulator A, Phase 1 to Phase 2. Connect a 470pF capacitor between CCI and the positive side of the feedback remote sense (or between CCI and AGND). CCI is internally forced low in shutdown.</td></tr>
<tr><td>26</td><td>CCI2</td><td>Current-Balance Compensation for Regulator A, Phase 1 to Phase 3. Connect a 470pF capacitor between CCI2 and the positive side of the feedback remote sense (or between CCI2 and AGND). CCI2 is internally forced low in shutdown.</td></tr>
</table>

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

Pin Description (continued)

PIN	NAME	FUNCTION
27	VBOOTA	Regulator A Boot Voltage-Control Input. Four-level boot voltage setting for regulator A.
		VBOOTA / **BOOT VOLTAGE V_{OUTA} (V)**
		V_{CC} / 1.10
		3V / 1.00
		2V / 0.9
		AGND / 0
28	VBOOTB	Regulator B Boot Voltage-Control Input. Four-level boot voltage setting for regulator B.
		VBOOTB / **BOOT VOLTAGE V_{OUTB} (V)**
		V_{CC} / 1.10
		3V / 1.00
		2V / 0.9
		AGND / 0
29	FBA	Feedback Input for Regulator A. Output of the DC voltage-positioning transconductance amplifier. Connect a resistor R_{FBA} between FBA and the positive side of the feedback remote sense to set the DC steady-state droop based on the voltage-positioning gain requirement: $R_{FBA} = R_{DROOPA}/(R_{SENSEA} \times G_{MDA})$ where R_{DROOPA} is the desired voltage-positioning slope and G_{MDA} = 600µs (typ). R_{SENSEA} is the value of the current-sense resistors that are used to provide the (CSPA_, CSNA_) current-sense voltages. DC droop can be disabled by shorting FBA to the positive remote-sense point. FBA is high impedance in shutdown.
30	GNDSA	Feedback Remote-Sense Input, Negative Side for Regulator A. Normally connected to AGND directly at the load. GNDSA internally connects to a transconductance amplifier that fine-tunes the output voltage—compensating for voltage drops from the regulator ground to the load ground.
31	IMONA	Current-Monitor Output for Regulator A: $I_{IMONA} = G_{M(IMONA)} \times \Sigma (V_{CSPA\_} - V_{CSNA\_})$ where $G_{M(IMONA)}$ = 2.43mS (typ) and Σ denotes summation over all enabled phases. An external resistor R_{IMONA} between IMONA and GNDSA sets the current-monitor output voltage: $V_{IMONA} = I_{LOAD} \times R_{SENSEA} \times G_{M(IMONA)} \times R_{IMONA}$ where R_{SENSEA} is the value of the effective current-sense resistance. Choose R_{IMONA} so that V_{IMONA} is 999mV at the maximum expected load current IMAXA. IMONA is in high impedance when the MAX17039 is in shutdown.
32	CCVA	Integrator Capacitor Connection for Regulator A. Connect a 100pF to 10nF (470pF, typ) capacitor from CCVA to AGND to set the integration time constant. The integrator is internally disabled when the part is in skip mode and the output is above regulation.
33	$\overline{DRSKIP}$	Driver Skip-Mode Output for the External Third Phase Driver for the Regulator A Controller for the CPU Core. The $\overline{DRSKIP}$ output is low in shutdown to save current.
34	PWM_OUT	Direct-Drive PWM Output for Controlling the External Third Phase Driver for the Regulator A Controller for the CPU Core. PWM_OUT is in three-state in shutdown to save current.
35	LXA1	Phase 1 Regulator A Inductor Connection. LXA1 is the internal lower supply rail for the DHA1 high-side gate driver. Also used as an input to the regulator A phase 1 zero-crossing comparator.

Pin Description (continued)

PIN	NAME	FUNCTION
36	DHA1	Phase 1 High-Side Gate-Driver Output. DHA1 swings from LXA1 to BSTA1. DHA1 is low in shutdown.
37	BSTA1	Boost Flying Capacitor Connection for the DHA1 High-Side Gate Driver. An internal switch between VDDA and BSTA1 charges the flying capacitor during the time the low-side FET is on.
38	DLA1	Phase 1 Low-Side Gate-Driver Output. DLA1 swings from VDDA to AGND. DLA1 is forced low in shutdown. DLA1 is forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DLA1 is forced low in skip mode after an inductor current zero crossing (AGND - LXA1) is detected.
39	VDDA	Supply Voltage Input for the DLA1 and DLA2 Drivers. VDDA is also the supply voltage used to internally recharge the BSTA1 and BSTA2 flying capacitors during the on-times of the respective DLA_. Connect VDDA to the 4.5V to 5.5V system supply voltage. Bypass VDDA to power ground with a 1µF or greater ceramic capacitor.
40	DLA2	Phase 2 Low-Side Gate-Driver Output. DLA2 swings from VDDA to AGND. DLA2 is forced low in shutdown. DLA2 is forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DL2 is forced low in skip mode after an inductor current zero crossing (AGND - LXA2) is detected.
41	BSTA2	Boost Flying Capacitor Connection for the DHA2 High-Side Gate Driver. An internal switch between VDDA and BSTA2 charges the flying capacitor during the time the low-side FET is on.
42	DHA2	Phase 2 Regulator A High-Side Gate-Driver Output. DHA2 swings from LXA2 to BSTA2. DHA2 is low in shutdown.
43	LXA2	Phase 2 Regulator A Inductor Connection. LXA2 is the internal lower supply rail for the DHA2 high-side gate driver. Also used as an input to the regulator A, phase 2 zero-crossing comparator.
44	VRA_READY	Open-Drain Power-Good Output for Regulator A. After output voltage transitions, except during power-up and power-down, if FBA is in regulation, then VRA_READY is high impedance. For zero VBOOT, VRA_READY is held low and continues to be low until 20µs (typ) after the output reaches the new voltage set by the new SVID command after boot-up. For nonzero VBOOT, VRA_READY is held low and continues to be low until 20µs (typ) after the output reaches the boot voltage set by the VBOOTA input. VRA_READY is forced low in shutdown. VRA_READY is forced high impedance whenever the slew-rate controller is active (output-voltage transitions). When in pulse-skipping mode, the upper VRA_READY threshold comparator is blanked. A pullup resistor on VRA_READY causes additional finite shutdown current. Do not pull up VRA_READY to a voltage above V_{CC}.

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

Pin Description (continued)

PIN	NAME	FUNCTION
45	VRB_READY	Open-Drain Power-Good Output for Regulator B. After output-voltage transitions, except during power-up and power-down, if FBB is in regulation, then VRB_READY is high impedance. For zero VBOOT, VRB_READY is held low and continues to be low until 20µs (typ) after the output reaches the new voltage set by the new SVID command after boot-up. For nonzero VBOOT_, VRB_READY is held low until 20µs (typ) after the output reaches the boot voltage set by the VBOOTB input. VRB_READY is forced low in shutdown. VRB_READY is forced high impedance whenever the slew-rate controller is active (output-voltage transitions). When in pulse-skipping mode, the upper VRB_READY threshold comparator is blanked. A pullup resistor on VRB_READY causes additional finite shutdown current. Do NOT pull up VRB_READY to a voltage above V_{CC}.
46	CSPA1	Positive Input of the Output Current Sense of Phase 1 of Regulator A. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
47	CSNA1	Negative Input of the Output Current Sense of Phase 1 of Regulator A. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. A 20Ω discharge FET is enabled from CSNA1 to AGND when regulator A completes soft-shutdown.
48	CSNA2	Negative Input of the Output Current Sense of Phase 2 of Regulator A. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
49	CSPA2	Positive Input of the Output Current Sense of Phase 2 of Regulator A. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. Tie this pin to V_{CC} for one-phase operation.
50	CSPA3	Positive Current-Sense Input for the Third Phase of the Regulator A Controller for the CPU Core. Tying CSPA3 to V_{CC} disables the third phase. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
51	CSNA3	Negative Current-Sense Input for the Third Phase of the Regulator A Controller for the CPU Core. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
52	IMAXA	ILIM Threshold for Regulator A. This multivalued logic input sets the valley current-limit sense voltage per phase. The total available current is the current limit multiplied by the number of active phases.

IMAXA	V_{ILIMA} ($V_{CSPA\_}$ - $V_{CSNA\_}$)(mV)
V_{CC}	30
3V	25
2V	20
AGND	15

Pin Description (continued)

PIN	NAME	FUNCTION	
53	IMAXB	ILIM Threshold for Regulator B. This multivalued logic input sets the valley current-limit sense voltage.	
		IMAXB	**V_{ILIMB} (V_{CSPB} - V_{CSNB})(mV)**
		V_{CC}	30
		3V	25
		2V	20
		AGND	15
54	TMAX	Thermal Maximum Threshold for Regulator A and Regulator B. This value is digitized and stored in register 22h.	
		TMAX	**REGISTER 22h (°C)**
		V_{CC}	105
		3V	100
		2V	95
		AGND	90
55	VR_HOT#	Open-Drain Output of the Thermal Comparators that Monitor THERMA and THERMB. These comparators are wire-ORed with output at VR_HOT#. This output is required as backup to the temperature zone register in the event of an SVID bus failure. The comparator responds to the temperature threshold set by data in the Temp MAX register (22h).	
56	AGND	Analog Ground	
—	EP	Exposed Pad. Internally connected to PGND. Connect this pad to the ground plane with thermally enhanced vias.	

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

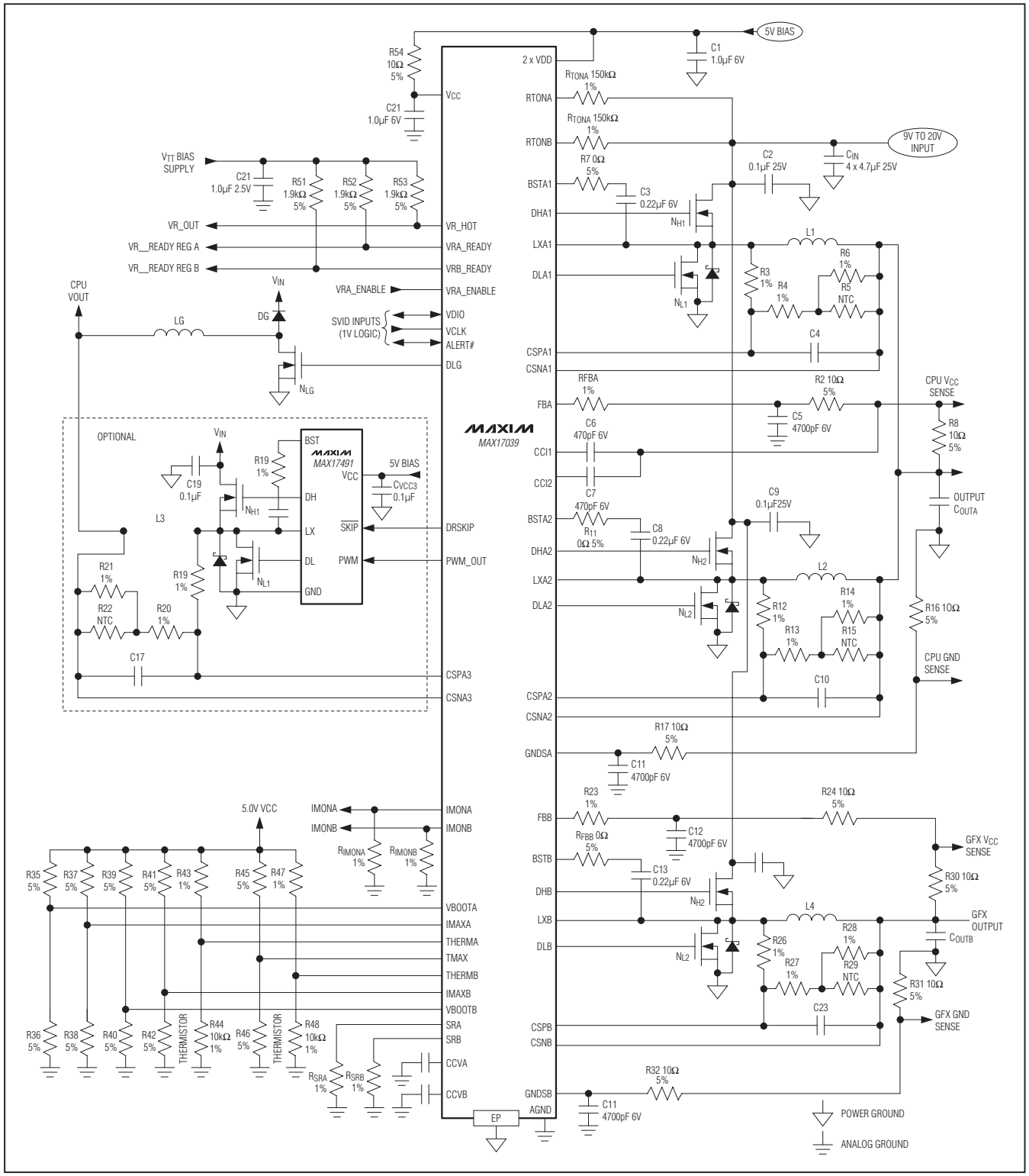


Figure 1. Typical CPU Core Application Circuit

Detailed Description

The MAX17039 is a dual-output step-down, constant-on-time controller for VR12/IMVP7 CPU core supplies. The controller consists of two high-current SMPSs for the CPU and GPU cores. The CPU regulator (regulator A, ADDR0) is a 3-phase constant-on-time architecture. The optional third phase is configured with an external MAX17491 driver. The second GPU regulator (regulator B, ADDR1) is also a constant-on-time architecture with single phase only. The three-phase CPU core regulator runs 120° out-of-phase for true interleaved operation, minimizing input capacitance. Figure 2 is the high-level block diagram. Table 1 lists regulator A typical component values and Table 2 lists regulator B typical component values.

Table 1. Regulator A Typical Component Values

COMPONENT	REF	QTY	VR12/IMVP7 SV CPU TDC = 36A/ I_{MAX} = 53A 350kHz OPERATION	VR12/IMVP7 XE CPU TDC = 52A/ I_{MAX} = 94A 350kHz OPERATION
Conditions	—	—	V_{IN} = 7V to 20V, V_{SVID} = 1V	V_{IN} = 7V to 20V, V_{SVID} = 1V
Phases	—	—	2	3
High-Side FET	$N_{H\_}$	1 per phase	Fairchild FDMS8680 Vishay (Siliconix) SiR402DP	Fairchild FDMS8680 Vishay (Siliconix) SiR402DP
Low-Side FET	$N_{L\_}$	2 per phase	Fairchild FDMS8660AS Vishay (Siliconix) Si7658ADP	Fairchild FDMS8660AS Vishay (Siliconix) Si7658ADP
Schottky Diode	$D_{L\_}$	None; most applications do not use Schottkys	None	None
Sense Resistor	$R_{SENSE\_}$	None; most applications use DCR sensing	1mΩ, 1%, 1W Panasonic ERJM1WTJ1M0U	1mΩ, 1%, 1W Panasonic ERJM1WTJ1M0U
Inductor	L1, L2, L3	1 per phase	0.36µH, 36A, 0.82mΩ power inductor Panasonic ETQP4LR36ZFC NEC/TOKIN MPC1055LR36 TOKO FDUE1040D-R36M	0.36µH, 36A, 0.82mΩ power inductor Panasonic ETQP4LR36ZFC NEC/TOKIN MPC1055LR36 TOKO FDUE1040D-R36M
Output Capacitors	C_{OUTA}	—	4 x 470µF, 2V, 4.5mΩ low-ESR polymer capacitor (D case) Panasonic EEFSX0D471E4 or NEC/TOKIN PSGV0E477M4.5 +15x22µF + 13x10µF ceramic	4 x 470µF, 2V, 4.5mΩ low-ESR polymer capacitor (D case) Panasonic EEFSX0D471E4 or NEC/TOKIN PSGV0E477M4.5 +15x22µF + 13x10µF ceramic
Input Capacitors	$C_{IN\_}$	2 per phase	10µF, 25V, X5R ceramic capacitors	10µF, 25V, X5R ceramic capacitors
Switching Frequency	R_{TONA}	1	150kΩ, 1% (350kHz)	150kΩ, 1% (350kHz)

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

Table 1. Regulator A Typical Component Values (continued)

COMPONENT	REF	QTY	VR12/IMVP7 SV CPU TDC = 36A/ I_{MAX} = 53A 350kHz OPERATION	VR12/IMVP7 XE CPU TDC = 52A/ I_{MAX} = 94A 350kHz OPERATION
Current Limit	R_{ILIM1}, R_{ILIM2}	—	200kΩ, 1%, open, 1%, V_{CS} = 30mV	200kΩ, 1%, open, 1%, V_{CS} = 30mV
Slew Rate	R_{SRA}	—	115kΩ, 10mV/µs (min)	115kΩ, 10mV/µs (min)
FB Droop Setting	R_{FBA}	1	3.83kΩ, 1% (load-line = -1.9mV/A)	3.83kΩ, 1% (load-line = -1.9mV/A)
THERMA Setting	R_{THERM}, R_{NTC}	—	4.87kΩ, 1% + 100kΩ, 5% NTC thermistor B = 4250 (0603) Murata NCP18WF104J03RB TDK NTCG163JF104J (0402) or Panasonic ERT-J1VR104J	4.87kΩ, 1% + 100kΩ, 5% NTC thermistor B = 4250 (0603) Murata NCP18WF104J03RB TDK NTCG163JF104J (0402) or Panasonic ERT-J1VR104J
IMONA	R_{IMONA}	1	7.68kΩ, 1% $V_{IMON\_}$ = 0.999V at 66A	5.11kΩ, 1% $V_{IMON\_}$ = 0.999V at 99A

Table 2. Regulator B Typical Component Values

COMPONENT	REF	QTY	VR12/IMVP7 GT TDC = 25A/EDC = 33A 640kHz OPERATION
Conditions	—	—	V_{IN} = 7V to 20V, V_{SVID} = 1V
Phases	—	—	1
High-Side FET	$N_{H\_}$	1	Fairchild FDMS8680 Vishay (Siliconix) SiR402DP
Low-Side FET	$N_{L\_}$	2	Fairchild FDMS8660AS Vishay (Siliconix) Si7658ADP
Schottky Diode	$D_{L\_}$	None; most applications do not use Schottkys	3A, 30V Schottky diode Nihon EC31QS03L Central Semiconductor CMSH3-40M
Sense Resistor	$R_{SENSE\_}$	None; most applications use DCR sensing	1mΩ, 1%, 1W Panasonic ERJM1WTJ1M0U
Inductor	L4	1	0.36µH, 36A, 0.82mΩ power inductor Panasonic ETQP4LR36ZFC NEC/TOKIN MPC1055LR36 TOKO FDUE1040D-R36M
Output Capacitors	$C_{OUTB\_}$	—	3 x 470µF, 2V, 4.5mΩ low-ESR polymer capacitor (D case) Panasonic EEFSX0D471E4 or NEC/TOKIN PSGV0E477M4.5 + 10x22µF

Table 2. Regulator B Typical Component Values (continued)

COMPONENT	REF	QTY	VR12/IMVP7 GT TDC = 25A/EDC = 33A 640kHz OPERATION
Input Capacitors	$C_{IN\_}$	2	10µF, 25V X5R ceramic capacitors
Switching Frequency	R_{TONB}	1	150kΩ, 1% (440kHz)
Current Limit OCP Set at 1.2x I_{MAX}	R_{ILIM1}, R_{ILIM2}	—	200kΩ, 1% open, 1%, V_{CS} = 30mV
Slew Rate	RSRB	—	115kΩ, 10mV/µs (min)
FB Droop Setting	R_{FBB}	1	8.05kΩ, 1% (load-line = -3.9mV/A)
VRHOT Setting	R_{THRM}, R_{NTC}	—	4.87kΩ, 1% + 100kΩ, 5% NTC thermistor B = 4250 (0603) Murata NCP18WF104J03RB TDK NTCG163JF104J (0402) or Panasonic ERT-J1VR104J
IMON_	R_{IMONB}	1	15.4kΩ, 1% $V_{IMON\_}$ = 0.999V at 33A

CPU and GPU outputs are controlled independently by writing the appropriate data into a function-mapped register file. Output voltages are dynamically changed through a 3-wire serial VID interface (3-wire SVID: clock, data, ALERT#), allowing the switching regulators to be individually programmed to different voltages. A slew-rate controller allows controlled transitions between SVID codes with controlled soft-start. The SVID interface also allows each regulator to be individually set into a low-power pulse-skipping state. Individual phases can be shut down based on the processors' operating conditions (1-, 2-, or 3-phase operation is possible under software control). Transient-phase overlap mode improves regulator A's current delivery-response time to reduces the total output capacitance.

Regulator A includes active overshoot suppression to reduce the required output decoupling capacitance. Regulator A also includes a boost-mode glitch catcher. During a load release, this simple external switch-boost circuit returns the excess energy stored in the inductor to the input supply. The glitch catcher can reduce output voltage soar by approximately 30% compared with the unassisted controller.

The MAX17039 includes output OVP, UVP, and thermal protection. When any of these protection features detect a fault, the controller shuts down both channels. True differential voltage and current sensing improves load-line and current-limit accuracy. Both regulators A and B feature programmable switching frequency, allowing 100kHz to 600kHz per phase operation.

VR12/IMVP7 requires current and temperature measurement for the individual outputs. For this reason, a 3-bit ADC with MUX is included to digitize the analog variables of interest. A thermistor-based temperature sensor provides a programmable thermal-fault output (VR_HOT#).

Free-Running, Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed frequency, constant-on-time, current-mode regulator with voltage feed-forward (Figures 3 and 4). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage, and directly proportional to the output

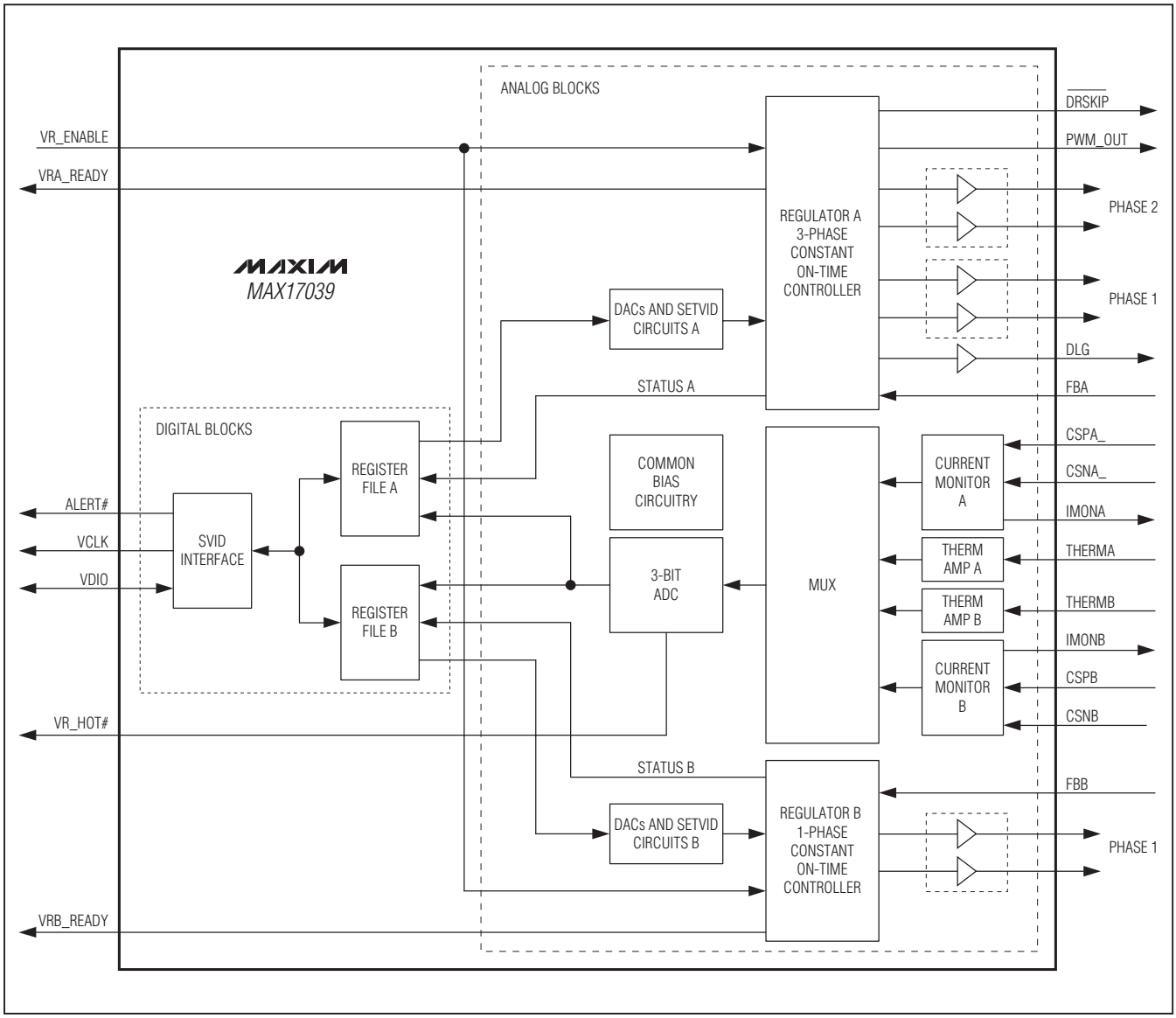


Figure 2. High-Level Block Diagram

voltage or the difference between the main and secondary inductor currents. See the *On-Time One-Shot* section. Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low, the inductor current of the selected phase is below the valley current-limit threshold, and the minimum off-time one-shot times out. The multiphase controller (regulator A) maintains 120° out-of-phase operation by alternately triggering the three phases after the error comparator drops below the output-voltage set point.

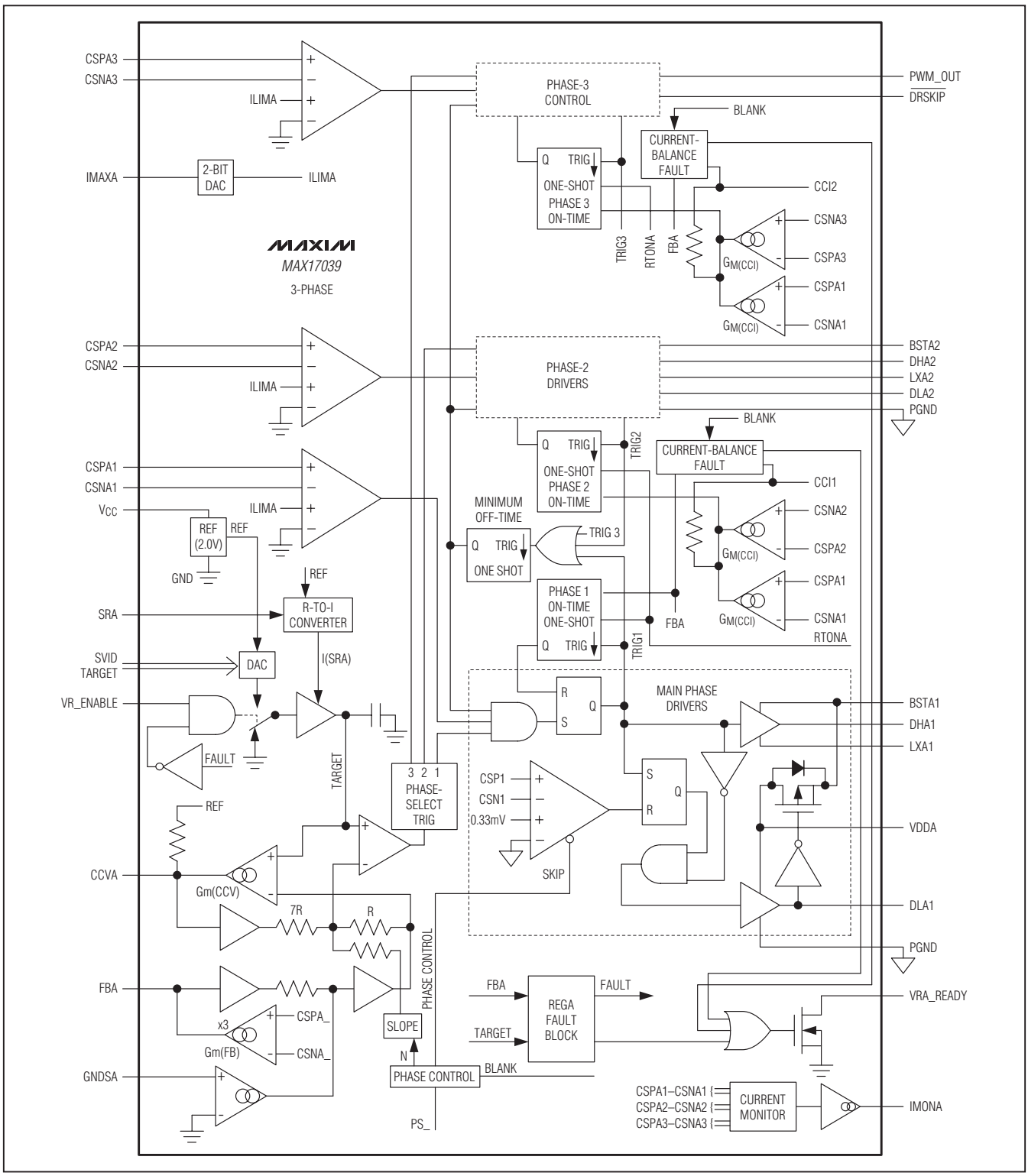


Figure 3. Regulator A Block Diagram with SVID Functions

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

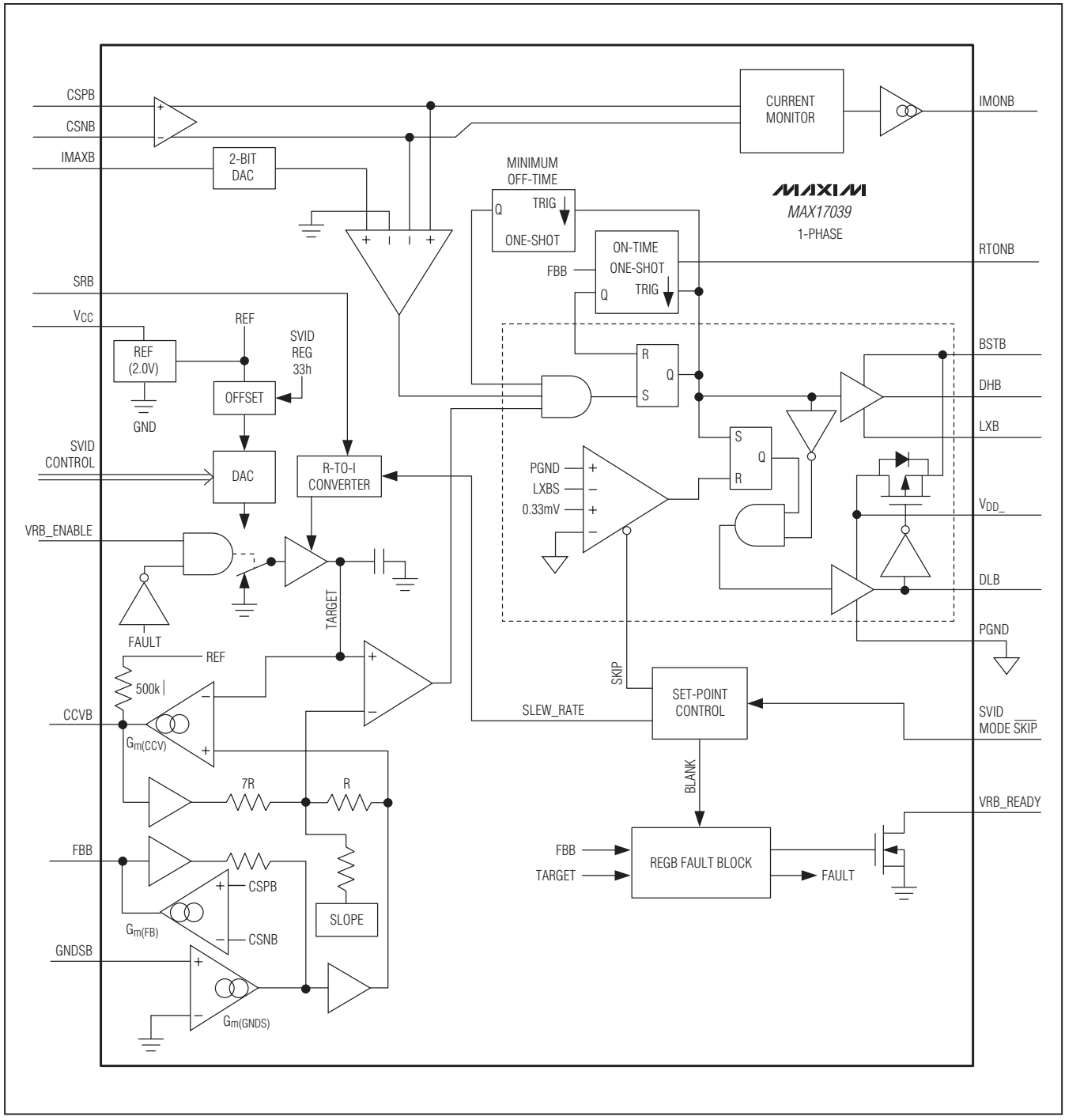


Figure 4. Regulator B Block Diagram with SVID Functions

Triple 120° Out-of-Phase Operation

The three phases in the MAX17039 operate 120° out-of-phase to minimize input and output filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements—making the MAX17039 ideal for high-power, cost-sensitive applications. The MAX17039 shares the current between three phases that operate 120° out-of-phase, so the high-side MOSFETs never turn on simultaneously during normal operation. The instantaneous input current of each phase is effectively reduced, resulting in reduced input voltage ripple, ESR power loss, and RMS ripple current. See the *Input-Capacitor Selection* section. Therefore, the same performance can be achieved with fewer or less-expensive input capacitors.

+5V Bias Supply (V_{CC}, VDDA, and VDDB)

The Quick-PWM controllers require an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95% efficient +5V system supply. The +5V bias supply must provide V_{CC} (PWM controller) and VDDA and VDDB (gate-drive power). VDDA and VDDB can be shorted together on the PCB. The maximum current drawn from the +5V bias supply is:

$$I_{BIAS} = I_{CC} + f_{SW}(Q_{G(LOW)} + Q_{G(HIGH)}) \mid REGA + f_{SW}(Q_{G(LOW)} + Q_{G(HIGH)}) \mid REGB$$

where I_{CC} is provided in the *Electrical Characteristics*, f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

V_{IN}, VDDA, and VDDB can be connected together if the input power source is a fixed 4.5V to 5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal (VR_ENABLE going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (TON_)

Connect a resistor ($R_{TON\_}$) between TON_ and V_{IN} to set the switching period T_{SW} = 1/f_{SW}, per phase:

$$T_{SW} = C_{TON} \times (R_{TON} + 6.5k\Omega)$$

where C_{TON} = 17.89pF for regulator A and C_{TON} = 14.63pF for regulator B.

High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

TON_ Open-Circuit Protection

The TON_ inputs include open-circuit protection to avoid long, uncontrolled on-times that could result in an overvoltage condition on the output. The MAX17039 detects an open-circuit fault if the TON_ current drops below 10µA for any reason—the TON_ resistor ($R_{TON\_}$) is unpopulated, a high resistance value is used, the input voltage is low, etc. Under these conditions, the MAX17039 stops switching (DH_ and DL_ pulled low) and immediately sets the fault latch. Toggle VR_ENABLE or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

On-Time One-Shot

Regulators A and B contain fast, low-jitter, adjustable one-shots that set the respective high-side MOSFETs on-time. In regulator A, the one-shot timing is shared among the three phases. The one-shot for the main phase varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage as measured by the V+ input, and proportional to the feedback voltage (V_{FB}):

$$t_{ON} = \frac{T_{SW}(V_{FB} + 0.075V)}{V_{IN}}$$

The one-shot for the second phase and third phase varies the on-time in response to the input voltage and the difference between the main and other inductor currents. Two identical transconductance amplifiers integrate the difference between the master and each slave's current-sense signals at CCI1 and CCI2. The respective error signals are used to correct the second and third phase's high-side MOSFET TON_ timers:

$$t_{ON(SEC)} = T_{SW}\left(\frac{V_{CCI} + 0.075V}{V_{IN}}\right)$$

$$= T_{SW}\left(\frac{V_{FB} + 0.075V}{V_{IN}}\right) + T_{SW}\left(\frac{I_{CCI}Z_{CCI}}{V_{IN}}\right)$$

$$= (\text{Main On-time}) + (\text{Secondary Current-Balance Correction})$$

where V_{CCI} is the integrator node for each slave's current-balance integrator, and Z_{CCI} is the effective impedance at that node. Analogous equations describe the timing correction for the third phase. During phase overlap, $t_{ON(SEC)}$ is calculated based on phase 1's on-time requirements, but reduced by 33% when operating with three phases. For a 3-phase regulator, each phase cannot be enabled until the other two phases have completed their on-time and the minimum off-times have expired. As such, the minimum period is limited by

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

3 x (t_{ON} + $t_{OFF(MIN)}$). Maximum t_{ON} is dependent on minimum input and maximum output voltage:

$$T_{SW(MIN)} = NPH \times (t_{ON(MAX)} + t_{OFF(MIN)})$$

where:

$$t_{ON(MAX)} = V_{FB(MAX)}/V_{IN(MIN)} \times T_{SW(MIN)}$$

so:

$$T_{SW(MIN)} = t_{OFF(MIN)}/[1/N_{PH} - V_{FB(MAX)}/V_{IN(MIN)}]$$

Hence, for a 7V input and 1.1V output, 500kHz is the maximum switching frequency. Running at this limit is not desirable as there is no room to allow the regulator to make adjustments without triggering phase overlap. For a three-phase, high-current application with minimum 8V input, the practical switching frequency is 300kHz. On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* are influenced by parasitics in the conduction paths and propagation delays. For loads above the critical conduction point, where the dead-time effect (LX flying high and conducting through the high-side FET body diode) is no longer a factor, the actual switching frequency (per phase) is:

$$f_{SW} = \frac{(V_{OUT} + V_{DIS})}{t_{ON}(V_{IN} + V_{DIS} - V_{CHG})}$$

where V_{DIS} and V_{CHG} are the sum of the parasitic voltage drops in the inductor discharge and charge paths, including MOSFET, inductor, and PCB resistances; V_{CHG} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time as determined above.

Current Sense

The MAX17039 senses the output current of each phase, allowing the use of current-sense resistors on inductor DCR as the current-sense element. Low-offset amplifiers are used for current balance, voltage-positioning gain, and current limit. Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency. The initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and current monitor. This current-sense method uses an RC filtering network to extract the current information from the output inductor (Figure 5).

The RC network should match the inductor's time constant (L/R_{DCR}):

$$R_{CS} = \left(\frac{R2}{R1 + R2}\right) R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}}\left[\frac{1}{R1} + \frac{1}{R2}\right]$$

where R_{CS} is the required current-sense resistance, and R_{DCR} is the inductor's series DC resistance. Use the typical inductance and R_{DCR} values provided by the inductor manufacturer. To minimize the current-sense error due to the current-sense inputs' bias current ($I_{CSP\_}$ and $I_{CSN\_}$), choose R1//R2 to be less than 2kΩ and use the above equation to determine the sense capacitance (C_{EQ}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Voltage Positioning and Loop Compensation* section for detailed information. When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance (L_{ESL}) of the current-sense resistor (Figure 5). The ESL-induced voltage step might affect the average current-sense voltage. The RC filter's time constant should match the L_{ESL}/R_{SENSE} time constant formed by the current-sense resistor's parasitic inductance:

$$\frac{L_{ESL}}{R_{SENSE}} = C_{EQ}R_{EQ}$$

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is the current-sense resistance value, and C_{EQ} and R_{EQ} are the time-constant matching components.

Inductor Sensing vs. Resistor Sensing

Regulators A and B can be configured to sense the inductor current of each phase, improving efficiency by eliminating the current-sense resistors. This requires low-input currents at each of the current-sense pins. Inductor current sensing achieves acceptable current balance as the temperature coefficient of the inductors' copper winding is better than that of a MOSFET. The temperature rise in each phase should track the others. Any increase in one phase's current causes the temperature to rise in that phase, increasing the DC resistance of the copper, signaling an imbalance to the controller. Thus, the current balance between phases should track quite accurately.

To maintain accurate droop while using inductor sensing, a thermistor is placed between the FB_ and V_{CPU} nodes, and located near the inductors to sense their temperature rise, and correct the droop. With inductor

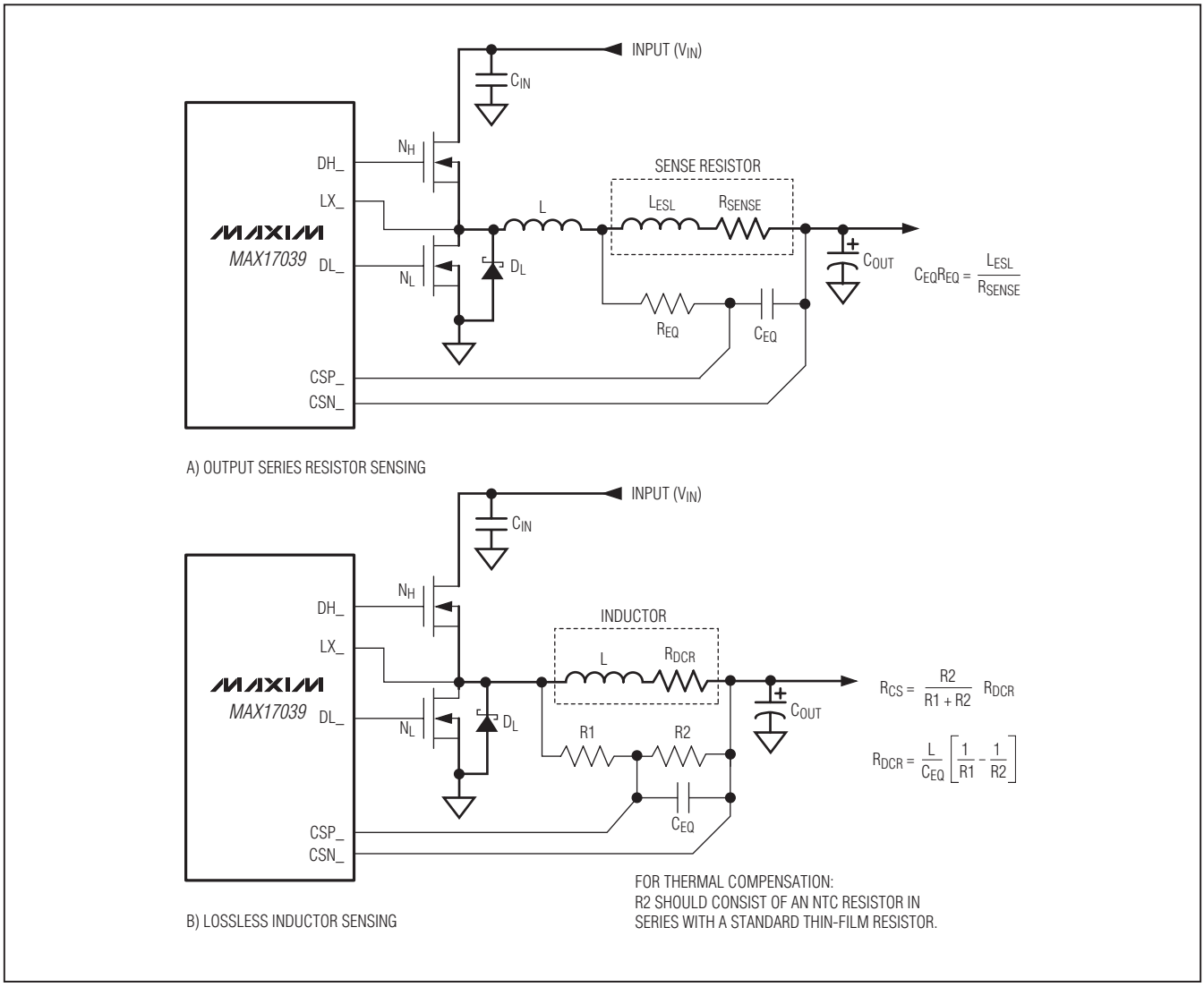


Figure 5. Current-Sense Methods

sensing, current limit has to be set based on the higher DCR at high temperature, unless a second thermistor is used at ILIM. Alternatively, a thermistor could be placed below each inductor, compensating for the DCR change with temperature and keeping a fairly constant effective DC resistance.

Current-sense inputs must have low-leakage currents to allow for the use of the higher resistances for DCR sensing. Zero crossing (for regulators A and B) is sensed from LX_ to GND. The zero crossing of Phase 3 is determined by the driver used.

Current Balance

Regulator A integrates the difference between the current-sense voltages and adjusts the on-time of the second and third phases to maintain current balance. The current balance relies on the accuracy of the current-sense signals across the current-sense resistor or inductor DCR. With active current balancing, the current mismatch is determined by the current-sense resistor or inductor DCR values and the offset voltage of the transconductance amplifiers:

$$I_{OS(IBAL)} = I_{LMAIN} - I_{LSEC} = \frac{V_{OS(IBAL)}}{R_{SENSE}}$$

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

where R_{SENSE} is the equivalent DCR sense resistance. and $V_{OS(IBAL)}$ is the current-balance offset specification in the *Electrical Characteristics*. The worst-case current mismatch occurs immediately after a load transient due to inductor value mismatches, resulting in different dI/dt for the two phases. The time it takes the current-balance loop to correct the transient imbalance depends on the mismatch between the inductor values and switching frequency.

Current Limit

The current-limit circuit employs a valley current-sensing algorithm that senses the voltage across the current-sense resistors or inductor DCR at the current-sense inputs (CSP_ to CSN_). If the current-sense signal of the selected phase is above the current-limit threshold, the PWM controller does not initiate a new cycle until the inductor current of the selected phase drops below the valley current-limit threshold. When any one phase exceeds the current limit, all phases are effectively current limited since the interleaved controller does not initiate a cycle with the next phase. Since only the valley current is actively limited, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and battery voltage. The positive valley current-limit threshold voltage at CSP_ to CSN_ is preset using the IMAX_ multivalue logic input.

The negative current-limit threshold (forced-PWM mode only) is nominally -125% of the corresponding valley current-limit threshold. When the inductor current drops below the negative current limit, the controller immediately activates an on-time pulse—DL_ turns off, and DH_ turns on—allowing the inductor current to remain above the negative-current threshold. Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by the current-sense inputs (CSP_, CSN_).

Feedback Adjustment Amplifiers

Voltage-Positioning Amplifier (Steady-State Droop)

Regulators A and B include transconductance amplifiers for adding gain to the voltage-positioning sense path. The amplifier's input is generated by summing the current-sense inputs, which differentially sense the voltage across either current-sense resistors or the inductor's DCR. The amplifier's output connects directly to the regulator's voltage-positioned feedback input (FB_), so the resistance between FB_ and the output-voltage sense point determines the voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FB}I_{FB}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output Voltage Selection* section, and the FB amplifier's output current (I_{FB}) is determined by the sum of the current-sense voltages:

$$I_{FB} = G_{m(FB)} \sum_{X=1}^{\eta_{PH}} V_{CSX}$$

where $V_{CSX} = V_{CSP} - V_{CSN}$ is the differential current-sense voltage, and $G_{m(FB)}$ is typically 600µs as defined in the *Electrical Characteristics*.

Differential Remote Sense

Both regulators A and B include differential, remote-sense inputs to eliminate the effects of voltage drops along the PCB traces and through the processor's power pins. The feedback-sense node connects to the voltage-positioning resistor ($R_{FB\_}$). The ground-sense (GNDS_) input connects to an amplifier that adds an offset directly to the target voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the voltage-positioning resistor ($R_{FB\_}$) and ground sense (GNDS_) input directly to the processor's remote-sense outputs as shown in Figure 1. The correction range is bounded to less than ±200mV. The remote-sense lines draw less than ±20µA to minimize offset errors.

Integrator Amplifier

Regulators A and B utilize internal integrator amplifiers that force the DC average of the FB_ voltage to equal the target voltage, allowing accurate DC output-voltage regulation regardless of the output voltage. The integrators are compensated at CCV_. Connect a 100pF to 10nF (470pF, typ) capacitor from CCV_ to AGND to set the integration time constant. The MAX17039 disables the integrators by connecting the amplifier inputs together at the beginning of all VID transitions done in pulse-skipping mode (PS2, PS3). The integrators remain disabled until 20µs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

Transient-Phase Overlap Operation

When a transient occurs, the response time of the controller depends on how quickly it can slew the inductor current. Multiphase controllers that remain 120° out-of phase when a transient occurs actually respond slower than an equivalent single-phase controller. In order to provide fast-transient response, regulator A supports phase-overlap mode that allows the triple regulators to operate in-phase when heavy load transients are detected, effectively reducing the response time. After any high-side MOSFET turns off, if the output voltage does not exceed the regulation voltage when the minimum off-time expires, the controller simultaneously turns on all high-side MOSFETs with the same on-time during the next on-time cycle. The phases remain overlapped until the output voltage exceeds the regulation voltage after the minimum off-time expires. The on-time for each phase is based on the input voltage to FBA ratio (i.e., follows the master on-time), but reduced by 33% in a three-phase configuration, and not reduced in a two-phase configuration. This maximizes the total inductor current slew rate. After the phase-overlap mode ends, the controller automatically begins with the next phase. For example, if phase 2 provided the last on-time pulse before overlap operation begins, the controller starts switching with phase 3 when overlap operation ends.

Nominal Output Voltage Selection

The nominal no-load output voltage (V_{TARGET}) is defined by the selected voltage reference (SVID DAC), plus the remote ground-sense adjustment (V_{GNDS}) as defined in the following equation:

$$V_{TARGET} = V_{FB} = V_{DAC} + V_{GNDS}$$

where V_{DAC} is the selected SVID voltage. On startup, the MAX17039 slews the target voltage from ground to the preset boot voltage. Table 3 lists the SVID code set for VR12/IMVP7.

Table 3. VR12/IMVP7 8-Bit DAC Code SVID[7:0]

LINE NO.	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
0	0	0	0	0	0	0	0	0	0	0	0.0000	—
1	0	0	0	0	0	0	0	1	0	1	0.2500	±20mV
2	0	0	0	0	0	0	1	0	0	2	0.2550	±20mV
3	0	0	0	0	0	0	1	1	0	3	0.2600	±20mV
4	0	0	0	0	0	1	0	0	0	4	0.2650	±20mV
5	0	0	0	0	0	1	0	1	0	5	0.2700	±20mV
6	0	0	0	0	0	1	1	0	0	6	0.2750	±20mV
7	0	0	0	0	0	1	1	1	0	7	0.2800	±20mV
8	0	0	0	0	1	0	0	0	0	8	0.2850	±20mV
9	0	0	0	0	1	0	0	1	0	9	0.2900	±20mV
10	0	0	0	0	1	0	1	0	0	A	0.2950	±20mV
11	0	0	0	0	1	0	1	1	0	B	0.3000	±20mV
12	0	0	0	0	1	1	0	0	0	C	0.3050	±20mV
13	0	0	0	0	1	1	0	1	0	D	0.3100	±20mV
14	0	0	0	0	1	1	1	0	0	E	0.3150	±20mV
15	0	0	0	0	1	1	1	1	0	F	0.3200	±20mV
16	0	0	0	1	0	0	0	0	1	0	0.3250	±20mV
17	0	0	0	1	0	0	0	1	1	1	0.3300	±20mV
18	0	0	0	1	0	0	1	0	1	2	0.3350	±20mV
19	0	0	0	1	0	0	1	1	1	3	0.3400	±20mV
20	0	0	0	1	0	1	0	0	1	4	0.3450	±20mV
21	0	0	0	1	0	1	0	1	1	5	0.3500	±20mV

Table 3. VR12/IMVP7 8-Bit DAC Code SVID[7:0] (continued)

LINE NO.	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
22	0	0	0	1	0	1	1	0	1	6	0.3550	±20mV
23	0	0	0	1	0	1	1	1	1	7	0.3600	±20mV
24	0	0	0	1	1	0	0	0	1	8	0.3650	±20mV
25	0	0	0	1	1	0	0	1	1	9	0.3700	±7mV
26	0	0	0	1	1	0	1	0	1	A	0.3750	±7mV
27	0	0	0	1	1	0	1	1	1	B	0.3800	±7mV
28	0	0	0	1	1	1	0	0	1	C	0.3850	±7mV
29	0	0	0	1	1	1	0	1	1	D	0.3900	±7mV
30	0	0	0	1	1	1	1	0	1	E	0.3950	±7mV
31	0	0	0	1	1	1	1	1	1	F	0.4000	±7mV
32	0	0	1	0	0	0	0	0	2	0	0.4050	±7mV
33	0	0	1	0	0	0	0	1	2	1	0.4100	±7mV
34	0	0	1	0	0	0	1	0	2	2	0.4150	±7mV
35	0	0	1	0	0	0	1	1	2	3	0.4200	±7mV
36	0	0	1	0	0	1	0	0	2	4	0.4250	±7mV
37	0	0	1	0	0	1	0	1	2	5	0.4300	±7mV
38	0	0	1	0	0	1	1	0	2	6	0.4350	±7mV
39	0	0	1	0	0	1	1	1	2	7	0.4400	±7mV
40	0	0	1	0	1	0	0	0	2	8	0.4450	±7mV
41	0	0	1	0	1	0	0	1	2	9	0.4500	±7mV
42	0	0	1	0	1	0	1	0	2	A	0.4550	±7mV
43	0	0	1	0	1	0	1	1	2	B	0.4600	±7mV
44	0	0	1	0	1	1	0	0	2	C	0.4650	±7mV
45	0	0	1	0	1	1	0	1	2	D	0.4700	±7mV
46	0	0	1	0	1	1	1	0	2	E	0.4750	±7mV
47	0	0	1	0	1	1	1	1	2	F	0.4800	±7mV
48	0	0	1	1	0	0	0	0	3	0	0.4850	±7mV
49	0	0	1	1	0	0	0	1	3	1	0.4900	±7mV
50	0	0	1	1	0	0	1	0	3	2	0.4950	±7mV
51	0	0	1	1	0	0	1	1	3	3	0.5000	±7mV
52	0	0	1	1	0	1	0	0	3	4	0.5050	±7mV
53	0	0	1	1	0	1	0	1	3	5	0.5100	±7mV
54	0	0	1	1	0	1	1	0	3	6	0.5150	±7mV
55	0	0	1	1	0	1	1	1	3	7	0.5200	±7mV
56	0	0	1	1	1	0	0	0	3	8	0.5250	±7mV
57	0	0	1	1	1	0	0	1	3	9	0.5300	±7mV
58	0	0	1	1	1	0	1	0	3	A	0.5350	±7mV
59	0	0	1	1	1	0	1	1	3	B	0.5400	±7mV
60	0	0	1	1	1	1	0	0	3	C	0.5450	±7mV
61	0	0	1	1	1	1	0	1	3	D	0.5500	±7mV

Table 3. VR12/IMVP7 8-Bit DAC Code SVID[7:0] (continued)

LINE NO.	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
62	0	0	1	1	1	1	1	0	3	E	0.5550	±7mV
63	0	0	1	1	1	1	1	1	3	F	0.5600	±7mV
64	0	1	0	0	0	0	0	0	4	0	0.5650	±7mV
65	0	1	0	0	0	0	0	1	4	1	0.5700	±7mV
66	0	1	0	0	0	0	1	0	4	2	0.5750	±7mV
67	0	1	0	0	0	0	1	1	4	3	0.5800	±7mV
68	0	1	0	0	0	1	0	0	4	4	0.5850	±7mV
69	0	1	0	0	0	1	0	1	4	5	0.5900	±7mV
70	0	1	0	0	0	1	1	0	4	6	0.5950	±7mV
71	0	1	0	0	0	1	1	1	4	7	0.6000	±7mV
72	0	1	0	0	1	0	0	0	4	8	0.6050	±7mV
73	0	1	0	0	1	0	0	1	4	9	0.6100	±7mV
74	0	1	0	0	1	0	1	0	4	A	0.6150	±7mV
75	0	1	0	0	1	0	1	1	4	B	0.6200	±7mV
76	0	1	0	0	1	1	0	0	4	C	0.6250	±7mV
77	0	1	0	0	1	1	0	1	4	D	0.6300	±7mV
78	0	1	0	0	1	1	1	0	4	E	0.6350	±7mV
79	0	1	0	0	1	1	1	1	4	F	0.6400	±7mV
80	0	1	0	1	0	0	0	0	5	0	0.6450	±7mV
81	0	1	0	1	0	0	0	1	5	1	0.6500	±7mV
82	0	1	0	1	0	0	1	0	5	2	0.6550	±7mV
83	0	1	0	1	0	0	1	1	5	3	0.6600	±7mV
84	0	1	0	1	0	1	0	0	5	4	0.6650	±7mV
85	0	1	0	1	0	1	0	1	5	5	0.6700	±7mV
86	0	1	0	1	0	1	1	0	5	6	0.6750	±7mV
87	0	1	0	1	0	1	1	1	5	7	0.6800	±7mV
88	0	1	0	1	1	0	0	0	5	8	0.6850	±7mV
89	0	1	0	1	1	0	0	1	5	9	0.6900	±7mV
90	0	1	0	1	1	0	1	0	5	A	0.6950	±7mV
91	0	1	0	1	1	0	1	1	5	B	0.7000	±7mV
92	0	1	0	1	1	1	0	0	5	C	0.7050	±7mV
93	0	1	0	1	1	1	0	1	5	D	0.7100	±7mV
94	0	1	0	1	1	1	1	0	5	E	0.7150	±7mV
95	0	1	0	1	1	1	1	1	5	F	0.7200	±7mV
96	0	1	1	0	0	0	0	0	6	0	0.7250	±7mV
97	0	1	1	0	0	0	0	1	6	1	0.7300	±7mV
98	0	1	1	0	0	0	1	0	6	2	0.7350	±7mV
99	0	1	1	0	0	0	1	1	6	3	0.7400	±7mV
100	0	1	1	0	0	1	0	0	6	4	0.7450	±7mV
101	0	1	1	0	0	1	0	1	6	5	0.7500	±7mV

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

Table 3. VR12/IMVP7 8-Bit DAC Code SVID[7:0] (continued)

LINE NO.	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
102	0	1	1	0	0	1	1	0	6	6	0.7550	±7mV
103	0	1	1	0	0	1	1	1	6	7	0.7600	±7mV
104	0	1	1	0	1	0	0	0	6	8	0.7650	±7mV
105	0	1	1	0	1	0	0	1	6	9	0.7700	±7mV
106	0	1	1	0	1	0	1	0	6	A	0.7750	±7mV
107	0	1	1	0	1	0	1	1	6	B	0.7800	±7mV
108	0	1	1	0	1	1	0	0	6	C	0.7850	±7mV
109	0	1	1	0	1	1	0	1	6	D	0.7900	±7mV
110	0	1	1	0	1	1	1	0	6	E	0.7950	±7mV
111	0	1	1	0	1	1	1	1	6	F	0.8000	±0.4%
112	0	1	1	1	0	0	0	0	7	0	0.8050	±0.4%
113	0	1	1	1	0	0	0	1	7	1	0.8100	±0.4%
114	0	1	1	1	0	0	1	0	7	2	0.8150	±0.4%
115	0	1	1	1	0	0	1	1	7	3	0.8200	±0.4%
116	0	1	1	1	0	1	0	0	7	4	0.8250	±0.4%
117	0	1	1	1	0	1	0	1	7	5	0.8300	±0.4%
118	0	1	1	1	0	1	1	0	7	6	0.8350	±0.4%
119	0	1	1	1	0	1	1	1	7	7	0.8400	±0.4%
120	0	1	1	1	1	0	0	0	7	8	0.8450	±0.4%
121	0	1	1	1	1	0	0	1	7	9	0.8500	±0.4%
122	0	1	1	1	1	0	1	0	7	A	0.8550	±0.4%
123	0	1	1	1	1	0	1	1	7	B	0.8600	±0.4%
124	0	1	1	1	1	1	0	0	7	C	0.8650	±0.4%
125	0	1	1	1	1	1	0	1	7	D	0.8700	±0.4%
126	0	1	1	1	1	1	1	0	7	E	0.8750	±0.4%
127	0	1	1	1	1	1	1	1	7	F	0.8800	±0.4%
128	1	0	0	0	0	0	0	0	8	0	0.8850	±0.4%
129	1	0	0	0	0	0	0	1	8	1	0.8900	±0.4%
130	1	0	0	0	0	0	1	0	8	2	0.8950	±0.4%
131	1	0	0	0	0	0	1	1	8	3	0.9000	±0.4%
132	1	0	0	0	0	1	0	0	8	4	0.9050	±0.4%
133	1	0	0	0	0	1	0	1	8	5	0.9100	±0.4%
134	1	0	0	0	0	1	1	0	8	6	0.9150	±0.4%
135	1	0	0	0	0	1	1	1	8	7	0.9200	±0.4%
136	1	0	0	0	1	0	0	0	8	8	0.9250	±0.4%
137	1	0	0	0	1	0	0	1	8	9	0.9300	±0.4%
138	1	0	0	0	1	0	1	0	8	A	0.9350	±0.4%
139	1	0	0	0	1	0	1	1	8	B	0.9400	±0.4%
140	1	0	0	0	1	1	0	0	8	C	0.9450	±0.4%
141	1	0	0	0	1	1	0	1	8	D	0.9500	±0.4%

Table 3. VR12/IMVP7 8-Bit DAC Code SVID[7:0] (continued)

LINE NO.	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
142	1	0	0	0	1	1	1	0	8	E	0.9550	±0.4%
143	1	0	0	0	1	1	1	1	8	F	0.9600	±0.4%
144	1	0	0	1	0	0	0	0	9	0	0.9650	±0.4%
145	1	0	0	1	0	0	0	1	9	1	0.9700	±0.4%
146	1	0	0	1	0	0	1	0	9	2	0.9750	±0.4%
147	1	0	0	1	0	0	1	1	9	3	0.9800	±0.4%
148	1	0	0	1	0	1	0	0	9	4	0.9850	±0.4%
149	1	0	0	1	0	1	0	1	9	5	0.9900	±0.4%
150	1	0	0	1	0	1	1	0	9	6	0.9950	±0.4%
151	1	0	0	1	0	1	1	1	9	7	1.0000	±0.4%
152	1	0	0	1	1	0	0	0	9	8	1.0050	±0.4%
153	1	0	0	1	1	0	0	1	9	9	1.0100	±0.4%
154	1	0	0	1	1	0	1	0	9	A	1.0150	±0.4%
155	1	0	0	1	1	0	1	1	9	B	1.0200	±0.4%
156	1	0	0	1	1	1	0	0	9	C	1.0250	±0.4%
157	1	0	0	1	1	1	0	1	9	D	1.0300	±0.4%
158	1	0	0	1	1	1	1	0	9	E	1.0350	±0.4%
159	1	0	0	1	1	1	1	1	9	F	1.0400	±0.4%
160	1	0	1	0	0	0	0	0	A	0	1.0450	±0.4%
161	1	0	1	0	0	0	0	1	A	1	1.0500	±0.4%
162	1	0	1	0	0	0	1	0	A	2	1.0550	±0.4%
163	1	0	1	0	0	0	1	1	A	3	1.0600	±0.4%
164	1	0	1	0	0	1	0	0	A	4	1.0650	±0.4%
165	1	0	1	0	0	1	0	1	A	5	1.0700	±0.4%
166	1	0	1	0	0	1	1	0	A	6	1.0750	±0.4%
167	1	0	1	0	0	1	1	1	A	7	1.0800	±0.4%
168	1	0	1	0	1	0	0	0	A	8	1.0850	±0.4%
169	1	0	1	0	1	0	0	1	A	9	1.0900	±0.4%
170	1	0	1	0	1	0	1	0	A	A	1.0950	±0.4%
171	1	0	1	0	1	0	1	1	A	B	1.1000	±0.4%
172	1	0	1	0	1	1	0	0	A	C	1.1050	±0.4%
173	1	0	1	0	1	1	0	1	A	D	1.1100	±0.4%
174	1	0	1	0	1	1	1	0	A	E	1.1150	±0.4%
175	1	0	1	0	1	1	1	1	A	F	1.1200	±0.4%
176	1	0	1	1	0	0	0	0	B	0	1.1250	±0.4%
177	1	0	1	1	0	0	0	1	B	1	1.1300	±0.4%
178	1	0	1	1	0	0	1	0	B	2	1.1350	±0.4%
179	1	0	1	1	0	0	1	1	B	3	1.1400	±0.4%
180	1	0	1	1	0	1	0	0	B	4	1.1450	±0.4%
181	1	0	1	1	0	1	0	1	B	5	1.1500	±0.4%

Table 3. VR12/IMVP7 8-Bit DAC Code SVID[7:0] (continued)

LINE NO.	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
182	1	0	1	1	0	1	1	0	B	6	1.1550	±0.4%
183	1	0	1	1	0	1	1	1	B	7	1.1600	±0.4%
184	1	0	1	1	1	0	0	0	B	8	1.1650	±0.4%
185	1	0	1	1	1	0	0	1	B	9	1.1700	±0.4%
186	1	0	1	1	1	0	1	0	B	A	1.1750	±0.4%
187	1	0	1	1	1	0	1	1	B	B	1.1800	±0.4%
188	1	0	1	1	1	1	0	0	B	C	1.1850	±0.4%
189	1	0	1	1	1	1	0	1	B	D	1.1900	±0.4%
190	1	0	1	1	1	1	1	0	B	E	1.1950	±0.4%
191	1	0	1	1	1	1	1	1	B	F	1.2000	±0.4%
192	1	1	0	0	0	0	0	0	C	0	1.2050	±0.4%
193	1	1	0	0	0	0	0	1	C	1	1.2100	±0.4%
194	1	1	0	0	0	0	1	0	C	2	1.2150	±0.4%
195	1	1	0	0	0	0	1	1	C	3	1.2200	±0.4%
196	1	1	0	0	0	1	0	0	C	4	1.2250	±0.4%
197	1	1	0	0	0	1	0	1	C	5	1.2300	±0.4%
198	1	1	0	0	0	1	1	0	C	6	1.2350	±0.4%
199	1	1	0	0	0	1	1	1	C	7	1.2400	±0.4%
200	1	1	0	0	1	0	0	0	C	8	1.2450	±0.4%
201	1	1	0	0	1	0	0	1	C	9	1.2500	±0.4%
202	1	1	0	0	1	0	1	0	C	A	1.2550	±0.4%
203	1	1	0	0	1	0	1	1	C	B	1.2600	±0.4%
204	1	1	0	0	1	1	0	0	C	C	1.2650	±0.4%
205	1	1	0	0	1	1	0	1	C	D	1.2700	±0.4%
206	1	1	0	0	1	1	1	0	C	E	1.2750	±0.4%
207	1	1	0	0	1	1	1	1	C	F	1.2800	±0.4%
208	1	1	0	1	0	0	0	0	D	0	1.2850	±0.4%
209	1	1	0	1	0	0	0	1	D	1	1.2900	±0.4%
210	1	1	0	1	0	0	1	0	D	2	1.2950	±0.4%
211	1	1	0	1	0	0	1	1	D	3	1.3000	±0.4%
212	1	1	0	1	0	1	0	0	D	4	1.3050	±0.4%
213	1	1	0	1	0	1	0	1	D	5	1.3100	±0.4%
214	1	1	0	1	0	1	1	0	D	6	1.3150	±0.4%
215	1	1	0	1	0	1	1	1	D	7	1.3200	±0.4%
216	1	1	0	1	1	0	0	0	D	8	1.3250	±0.4%
217	1	1	0	1	1	0	0	1	D	9	1.3300	±0.4%
218	1	1	0	1	1	0	1	0	D	A	1.3350	±0.4%
219	1	1	0	1	1	0	1	1	D	B	1.3400	±0.4%
220	1	1	0	1	1	1	0	0	D	C	1.3450	±0.4%
221	1	1	0	1	1	1	0	1	D	D	1.3500	±0.4%

Table 3. VR12/IMVP7 8-Bit DAC Code SVID[7:0] (continued)

LINE NO.	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
222	1	1	0	1	1	1	1	0	D	E	1.3550	±0.4%
223	1	1	0	1	1	1	1	1	D	F	1.3600	±0.4%
224	1	1	1	0	0	0	0	0	E	0	1.3650	±0.4%
225	1	1	1	0	0	0	0	1	E	1	1.3700	±0.4%
226	1	1	1	0	0	0	1	0	E	2	1.3750	±0.4%
227	1	1	1	0	0	0	1	1	E	3	1.3800	±0.4%
228	1	1	1	0	0	1	0	0	E	4	1.3850	±0.4%
229	1	1	1	0	0	1	0	1	E	5	1.3900	±0.4%
230	1	1	1	0	0	1	1	0	E	6	1.3950	±0.4%
231	1	1	1	0	0	1	1	1	E	7	1.4000	±0.4%
232	1	1	1	0	1	0	0	0	E	8	1.4050	±0.4%
233	1	1	1	0	1	0	0	1	E	9	1.4100	±0.4%
234	1	1	1	0	1	0	1	0	E	A	1.4150	±0.4%
235	1	1	1	0	1	0	1	1	E	B	1.4200	±0.4%
236	1	1	1	0	1	1	0	0	E	C	1.4250	±0.4%
237	1	1	1	0	1	1	0	1	E	D	1.4300	±0.4%
238	1	1	1	0	1	1	1	0	E	E	1.4350	±0.4%
239	1	1	1	0	1	1	1	1	E	F	1.4400	±0.4%
240	1	1	1	1	0	0	0	0	F	0	1.4450	±0.4%
241	1	1	1	1	0	0	0	1	F	1	1.4500	±0.4%
242	1	1	1	1	0	0	1	0	F	2	1.4550	±0.4%
243	1	1	1	1	0	0	1	1	F	3	1.4600	±0.4%
244	1	1	1	1	0	1	0	0	F	4	1.4650	±0.4%
245	1	1	1	1	0	1	0	1	F	5	1.4700	±0.4%
246	1	1	1	1	0	1	1	0	F	6	1.4750	±0.4%
247	1	1	1	1	0	1	1	1	F	7	1.4800	±0.4%
248	1	1	1	1	1	0	0	0	F	8	1.4850	±0.4%
249	1	1	1	1	1	0	0	1	F	9	1.4900	±0.4%
250	1	1	1	1	1	0	1	0	F	A	1.4950	±0.4%
251	1	1	1	1	1	0	1	1	F	B	1.5000	±0.4%
252	1	1	1	1	1	1	0	0	F	C	1.5050	±0.4%
253	1	1	1	1	1	1	0	1	F	D	1.5100	±0.4%
254	1	1	1	1	1	1	1	0	F	E	1.5150	±0.4%
255	1	1	1	1	1	1	1	1	F	F	1.5200	±0.4%

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

Output-Voltage-Transition Timing

At the beginning of an output-voltage transition, the MAX17039 blanks both power-good thresholds, preventing the VR__READY open-drain outputs from changing states during the transition. The controller enables the lower power-good threshold approximately 20µs after the slew-rate controller reaches the target output voltage, but the upper threshold is enabled only if the controller remains in forced-PWM operation. If the controller enters pulse-skipping operation, the upper threshold remains blanked. The slew rate must be set fast enough to ensure that the transition can be completed within the maximum allotted time. The MAX17039 automatically controls the current to the minimum level required to complete the transition. The total transition time depends on the SR_ input setting, the particular SETVID command (fast, slow) and the voltage difference, and the accuracy of the slew-rate controller (C_{SLEW} accuracy, see the *Electrical Characteristics* table). The slew rate is not dependent on the total output capacitance, as long as the surge current is less than the current limit. For dynamic SVID transitions, the transition time (t_{TRAN}) is given by:

$$t_{TRAN} = \frac{|V_{NEW} - V_{OLD}|}{(dV_{TARGET}/dt)}$$

where dV_{TARGET}/dt is the slew rate set with the SR_ input and the SETVID command, V_{OLD} is the original output voltage, and V_{NEW} is the new target voltage. See Slew-Rate Accuracy in the *Electrical Characteristics* table for slew-rate limits. The maximum programmable slew rate is I_{LIM}/C_{OUT}.

For nonzero V_{BOUT}, the soft-start slew rate is the same as a SETVID slow command. For soft-shutdown, the controller automatically reduces the slew rate to -1.2mV/µs (typ). The average inductor current per phase required to make an output voltage transition is:

$$I_L \cong \frac{C_{OUT}}{\eta_{TOTAL}} \times (dV_{TARGET}/dt)$$

where dV_{TARGET}/dt is the required slew rate, C_{OUT} is the total output capacitance, and η_{TOTAL} is the number of active phases.

Forced-PWM Operation (PS0, PS1)

During soft-shutdown and normal operation—when the CPU is actively running (PS0, PS1)—the MAX17039 operates with the low-noise, forced-PWM control scheme. Forced-PWM operation disables the zero-crossing comparators of all active phases, forcing the low-side gate-drive waveforms to constantly be the complement of the high-side gate-drive waveforms. This keeps the switching frequency constant and allows the inductor current to reverse under light loads, providing fast, accurate negative output-voltage transitions by quickly discharging the output capacitors. Forced-PWM operation comes at a cost: the no-load +5V bias supply current remains between 10mA to 50mA per phase, depending on the external MOSFETs and switching frequency. To maintain high efficiency under light-load conditions, the processor can switch the controller to a low-power pulse-skipping control scheme by entering PS2 or PS3.

Light-Load Pulse-Skipping Operation (PS2, PS3)

When the SVID bus master issues a SETPS command to PS2 or PS3, the MAX17039 immediately disables phases 2 and 3 (DH2, DL2 forced low, PWM_OUT three-state, $\overline{DRSKIP}$ low), and enters pulse-skipping operation. The pulse-skipping mode enables the driver's zero-crossing comparator, so the controller pulls DL_ low when its current-sense inputs detect zero inductor current. This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output. If the VIDs are set to a lower voltage setting, the output drops at a rate determined by the load and the output capacitance. The internal target still ramps as before, and VR__READY remains blanked high impedance until 20µs after the output voltage reaches the internal target. Once this time expires, VR__READY monitors only the lower threshold. Upon entering pulse-skipping operation, the controller temporarily sets the OVP threshold to 1.82V, preventing false OVP faults when the transition to pulse-skipping operation coincides with an SVID code change. Once the VR_SETTLED comparator detects that the output voltage is in regulation, the OVP threshold tracks the selected SVID DAC code. The MAX17039 automatically uses forced-PWM operation during soft-start and soft-shutdown, regardless of the SETPS command.

Automatic Pulse-Skipping Switchover

In SKIP mode (PS2, PS3), an inherent automatic switchover to PFM takes place at light loads (Figure 6). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across the low-side MOSFETs. Once $V_{LX\_}$ drops below the zero-crossing comparator threshold (see the *Electrical Characteristics*), the comparator forces DL_ low. This mechanism causes the threshold between pulse-skipping PFM and nonskipping

PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load current of each phase is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value. For a battery input range of 7V to 20V, this threshold is relatively constant, with only a minor dependence on the input voltage due to the typically low duty cycles. The total load current at the PFM/PWM crossover threshold ($I_{LOAD(SKIP)}$) is approximately:

$$I_{LOAD(SKIP)} = \left(\frac{T_{SW}V_{OUT}}{2L}\right)\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

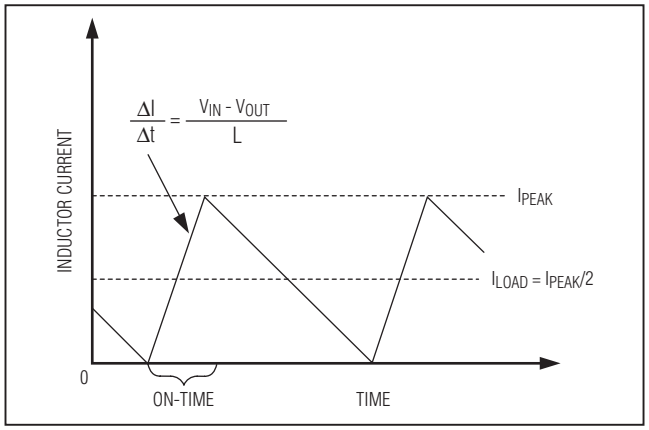


Figure 6. Pulse-Skipping/Discontinuous Crossover Point

Power-Up Sequence (POR, UVLO)

The MAX17039 is enabled when VR_ENABLE is driven high (Figure 7). The reference powers up first. Once the reference exceeds its UVLO threshold, the internal analog blocks are turned on and masked by a 150µs one-shot delay. The PWM controller then begins switching. Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and preparing the controller for operation. The V_{CC} UVLO circuitry inhibits switching until V_{CC} rises above 4.25V. The controller powers up the reference once the system enables the controller, V_{CC} is above 4.25V, and VR_ENABLE is driven high. With the reference in regulation, the controller ramps the output voltage to the programmed boot voltage at the slow slew rate set by the SR_ input:

$$t_{TRAN(START)} = \frac{V_{BOOT}}{(dV_{TARGET}/dt)}$$

where dV_{TARGET}/dt is the slew rate.

The soft-start circuitry does not use a variable current limit, so full output current is available immediately.

Note the IMAX_, VBOOT_, SR_, and TMAX multivalued logic inputs are sampled at POR and the data is latched into the respective registers. These values cannot be changed without driving the MAX17039 through another POR cycle.

The startup sequence is as follows:

1) The MAX17039 has power and chip V_{CC} is > UVLO.
2) The MAX17039 receives hardware enable.
3) The MAX17039 SVID bus is active and idle.
4) If the V_{BOOT} register = 00h, the MAX17039 waits at 0V, VR__READY is deasserted and ALERT# remains deasserted.

   If the V_{BOOT} register is programmed to a VID setting other than zero, the MAX17039 ramps to the programmed voltage, asserts VR__READY and ALERT#, and holds until the SVID command.
5) CPU initiates the SVID clock.
6) CPU sends out the SetVID_Slow command to program the initial output voltage.
7) The MAX17039 acknowledges and ramps to the voltage in the SetVIDSlow command at the slow slew rate.
8) The MAX17039 asserts VR__READY for that rail, and ALERT# asserts.
9) Repeat steps 4, 5, 6, 7, and 8 for regulator B.

If V_{CC} drops below 4.25V after POR, the MAX17039 sets the fault latch and turns off.

Shutdown Control

When VR_ENABLE goes low, the MAX17039 enters low-power shutdown mode. VR__READY is pulled low immediately, and the output voltage ramps down at a slew rate of dV_{TARGET}/dt = -1.2mV/µs (typ):

$$t_{TRAN(SHDN)} = \frac{4V_{OUT}}{(dV_{TARGET}/dt)}$$

After the output voltage drops to 0mV, the MAX17039 shuts down completely—the drivers are disabled (DL_ and DH_ driven low, PWM_OUT is three-state, and $\overline{DRSKIP}$ is low), the reference turns off, the 20Ω CSN_ discharge FET is turned on, and the supply current drops below 1µA. When an undervoltage fault condition activates the shutdown sequence, the protection circuitry sets the fault latch to prevent the controller

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

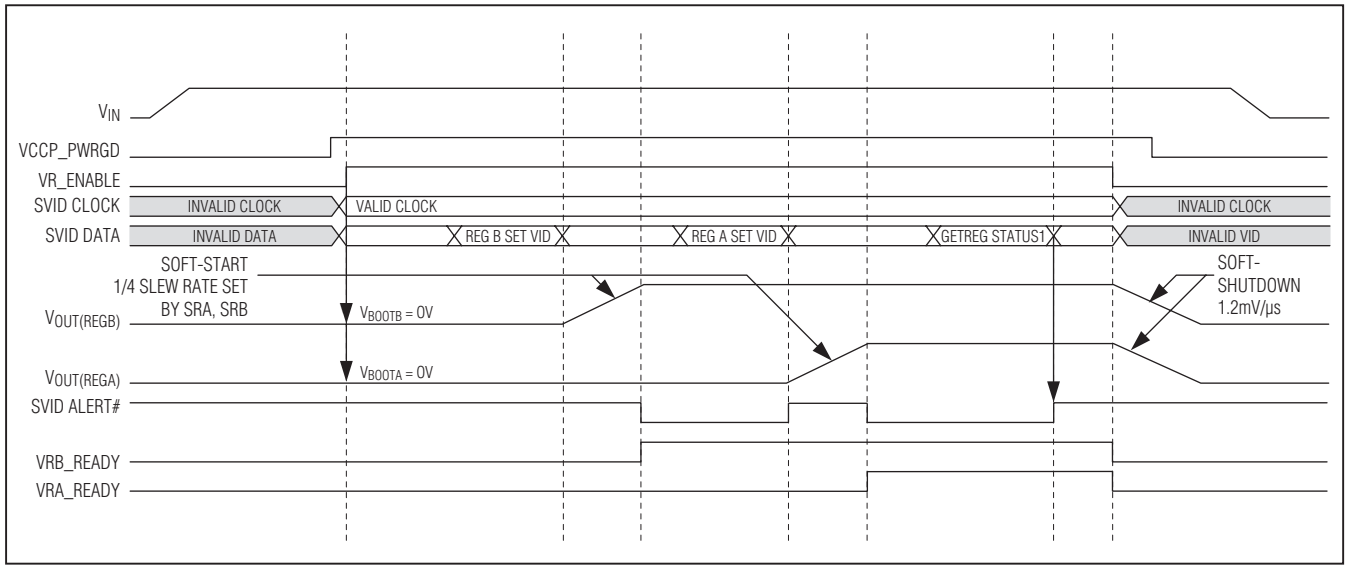


Figure 7. Startup Sequence for Zero V_{BOOT}

from restarting. To clear the fault latch and reactivate the controller, toggle VR_ENABLE or cycle V_{CC} power below 0.5V.

The VR_ENABLE pin controls both regulator A and regulator B outputs. The pin is active high and is compatible with 1V logic. When VR_ENABLE is asserted, with $V_{VBOOT\_}$ = 0V, the SVID bus is active within 200µs and enters an idle state, waiting for first commands and initial voltage target.

For nonzero VBOOT_, the SVID interface can accept commands after the output voltage reaches its target.

Power-Good (VRA_READY, VRB_READY)

Regulators A and B have independent power-good signals (VRA_READY, VRB_READY). These active- high outputs indicate the startup sequence is complete and the respective output voltage has moved to the programmed SVID value. These signals are used for system sequencing for other voltage regulators, the clock, and microprocessor reset. VR__READY remains asserted during normal DC-DC operating conditions and is deasserted for any fault or shutdown conditions.

Current Monitor (IMONA, IMONB)

The MAX17039 includes two unidirectional transconductance amplifiers that source current proportional to the positive current-sense voltage for regulators A and B. Each IMON_ output current is defined by:

$$I_{IMON\_} = G_{m(IMON\_)} \times \Sigma(V_{CSP\_} - V_{CSN\_})$$

where $G_{m(IMON\_)}$ = 2.43mS (typ) and the IMON_ current is unidirectional (sources current out of IMON_ only) for positive current-sense values. For negative current-sense voltages, the IMON_ current is zero. Connect an external resistor between IMON_ and GNDS_ to create the desired IMON gain based on the following equation:

$$R_{IMON\_} = 0.999V/(I_{MAX\_} \times R_{SENSE} \times G_{m(IMON\_)})$$

where $I_{MAX\_}$ is defined in the *Current Monitor* section of the Intel VR12/IMVP7 specification, R_{SENSE} is the typical value of the current-sense element (sense resistor or inductor DCR) that is used to provide the current-sense voltage, and $G_{m(IMON\_)}$ is the transconductance amplifier gain as defined in the *Electrical Characteristics* table. The IMON_ voltage is internally clamped to a maximum of 1.15V, preventing the IMON_ output from exceeding the IMON voltage rating even under overload or short-circuit conditions. When the controller is disabled, IMON_ is pulled to ground. The transconductance amplifier and voltage clamp are internally compensated, so IMON_ cannot directly drive large capacitance values. To filter the IMON_ signal, use a parallel RC filter instead of a purely resistive load on IMON_.

Temperature Comparator (VR_HOT#)

The MAX17039 features two independent comparators with inputs at THERMA and THERMB. These comparators have accurate thresholds matching the appropriate thermal levels required for the Temperature Zone register (12h). Because these thresholds are nonlinear, it is

essential to use the correct resistor and thermistor values specified in Figure 1. When TMAX is exceeded at either THERMA or THERMB, VR_HOT# is pulled low. For each regulator, place the thermistor as close to the MOSFETs and inductors as possible. The MAX17039 Evaluation kit provides a good example of thermistor placement.

Fault Protection (Latched)

Output Overvoltage Protection

The OVP circuit is designed to protect the load against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The MAX17039 continuously monitors each output for an overvoltage fault. An OVP fault is detected if the output voltage exceeds the SVID DAC voltage by more than 300mV, or the fixed 1.82V (typ) threshold during a downward VID transition in SKIP mode. During pulse-skipping operation (PS2, PS3), the OVP threshold tracks the SVID DAC voltage as soon as the output is in regulation; otherwise, the fixed 1.82V (typ) threshold is used. For regulator A, when the OVP circuit detects an overvoltage fault while in multiphase mode (PS0), the MAX17039 immediately forces DL_ high, PWM_OUT low, and $\overline{DRSKIP}$ high, and pulls DH_ low. This action turns on the synchronous-rectifier MOSFETs with 100% duty and, in turn, rapidly discharges the output filter capacitor and forces the output low. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse blows. Toggle VR_ENABLE or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller. For regulator A, when an overvoltage fault occurs while in one-phase operation (PS1, PS2, PS3), the MAX17039 immediately forces DLA1 high and pulls DHA1 low. DLA2 and DHA2 remain low as phase 2 was disabled.

Regulator B's behavior is analogous in response to OVP, with only one set of drivers affected.

Output Undervoltage Protection

If the output voltage on regulator A or B is 400mV below the target voltage, the controller activates the shutdown sequence and sets the fault latch. Once the output voltage ramps down to 0mV, it forces the DL_ low and pulls DH_ low, three-states PWM_OUT, sets $\overline{DRSKIP}$ low, and 20Ω CSN_ discharge FET is turned on. Toggle VR_ENABLE or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

Thermal-Fault Protection

The MAX17039 features a thermal-fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor sets the fault latch and forces the DL_ and DH_ low, three-states PWM_OUT, sets $\overline{DRSKIP}$ low, and enables both internal 20Ω CSN_ discharge FETs. Toggle VR_ENABLE or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller after the junction temperature cools by 15°C.

MOSFET Gate Drivers

The DH_ and DL_ drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. The high-side gate drivers (DH_) source 2.2A and sink 2.7A, and the low-side gate drivers (DL_) source 2.7A and sink 8A. This ensures robust gate drive for high-current applications. The DH_ floating high-side MOSFET drivers are powered by internal boost switch charge pumps at BST_, while the DL_ synchronous-rectifier drivers are powered directly by the 5V bias supply (VDD_). Adaptive dead-time circuits monitor the DL_ and DH_ drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. A low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates is required for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX17039 interprets the MOSFET gates as off while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver). The DL_ low on-resistance of 0.25Ω (typ) helps prevent DL_ from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX_) quickly switches from ground to V_{IN}. The capacitive coupling between LX_ and DL_ created by the MOSFET's gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold to prevent shoot-through currents:

$$V_{GS(TH)} > V_{IN(MAX)}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

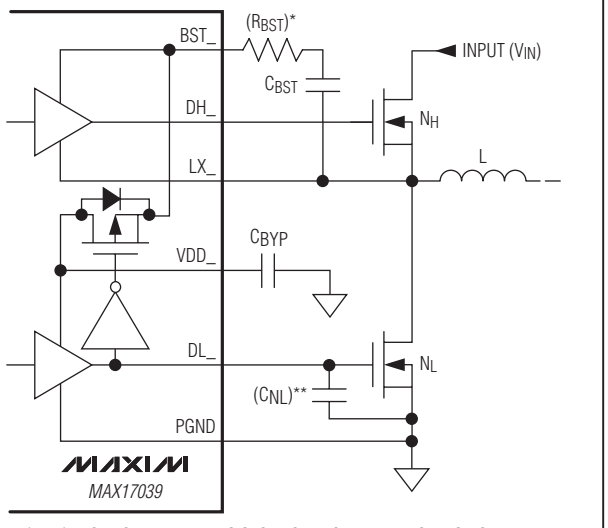
Adding a 4700pF between DL_ and power ground (C_{NL} in Figure 8) close to the low-side MOSFETs greatly

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays. Shoot-through currents can also be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with BST_ slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 8). Slowing down the high-side MOSFET also reduces the LX_ node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

External Driver and Disabling Phases

The MAX17039 supports a single external driver, MAX17491, for 3-phase operation. The PWM_OUT output provides the signal to trigger the driver. $\overline{DRSKIP}$ forces the driver into SKIP mode by turning off both DH_ and DL_. There are two current-sense inputs CSPA3 and CSNA3. Tying CSPA3 to V_{CC} disables the third phase. Similarly, phase 2 can be disabled for single-phase operation by tying CSPA2 to V_{CC}.



(RBST)* OPTIONAL—THE RESISTOR LOWERS EMI BY DECREASING THE SWITCHING NODE RISE TIME.
(CNL)** OPTIONAL—THE CAPACITOR REDUCES LX TO DL CAPACITIVE COUPLING THAT CAN CAUSE SHOOT-THROUGH CURRENT.

Figure 8. Gate-Drive Circuit

Data-Acquisition System

Current and thermal-monitoring functions are required in VR12/IMVP7. A simplified data-acquisition system is required to convert the analog signals from the IMON_ and THERM_ inputs to scaled eight discrete levels in the ICC MAX and TMAX zone registers. See Figure 9. An independent VR_HOT# output is available to make certain the system is alerted to an overtemperature fault in the event of SVID bus failure. The data-acquisition system periodically scans and converts the inputs from the mux. A modified successive approximation algorithm is used to make the measurements in order to simplify the design.

Output-Voltage Overshoot Suppression

Regulator A reduces output voltage overshoot by turning off the low-side MOSFET when the output voltage exceeds the SVID set point by 33mV (typ). This action increases the differential voltage across the inductor, thereby increasing the dI/dt available to discharge the output capacitor. Normal synchronous rectification resumes when the output voltage drops inside the SVID set point + 21mV (typ). This feature is not present on regulator B.

The MAX17039 includes a boost converter with regulator A that can be used to actively suppress output overshoot when the load releases. The boost converter takes the CPU core voltage as its input and the V_{IN} as its output. A simplified block diagram of this circuit is shown in Figure 10. When the output voltage overshoots by 33mV above the SVID set point, this boost converter turns on to discharge the output capacitor. The duty cycle is DC = 900ns/(900ns + 420ns x V_{OUT}/1V), which is the equation of a simple boost converter. The operating frequency is proportional to 1/V_{OUT} with a minimum off-time of 420ns (typ). The boost converter shuts off when the output voltage drops below the SVID set point + 21mV (typ). This feature is not present on regulator B.

The required inductance for this circuit L_G is very small (20nH < L_G < 50nH). It is possible to create LG using wide PCB traces. Transient overshoot conditions usually last for very short intervals. So while the peak currents in the circuit are very high, average power dissipation is very low. L_G, D_G, and N_{G1} can therefore be rated for the peak current rather than the maximum DC current. Refer to the MAX17039 EV kit for the complete design example.

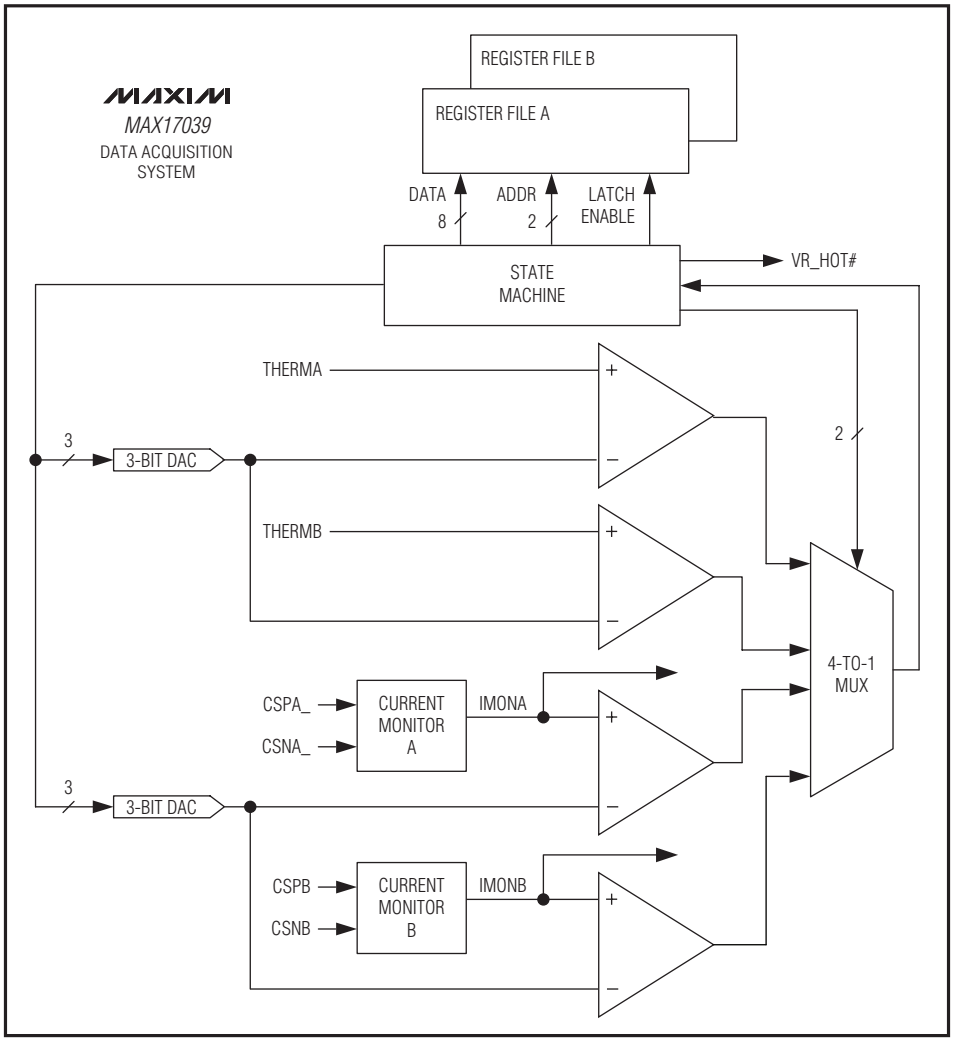


Figure 9. Data-Acquisition System Block Diagram

The boost converter is not required to achieve the required output-voltage accuracy for VR12/IMVP7. If it is not desired, leave DLG open and do not populate L_G, D_G, and N_{G1}.

Serial VID Interface, Commands, Registers, and Digital Control

A simplified block diagram of the MAX17039's SVID interface is shown in Figure 11. The interface consists of a high-speed transceiver, control logic, and two independent, identically configured register files for

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

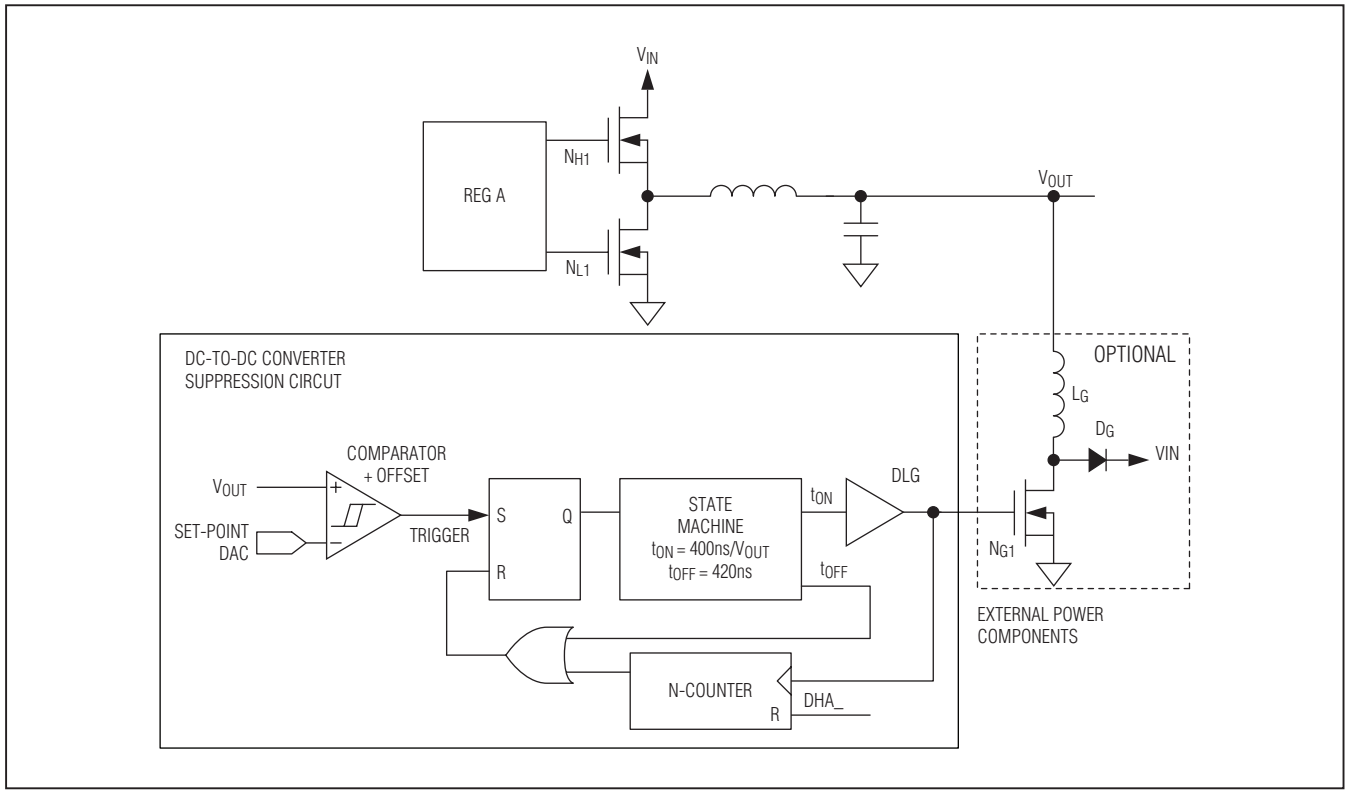


Figure 10. Glitch Catcher Block Diagram

regulators A and B. Refer to Intel's VR12/IMVP7 SVID protocol documentation for complete details on the interface and the required configuration of SVID data packets.

Regulator Addressing

The MAX17039 does not feature programmable addressing. Regulator A is hard coded to be SVID bus address 0, and regulator B is hard coded to be SVID bus address 1.

Serial VID Commands

The MAX17039 supports the following commands (Table 4) and registers according to Intel's VR12/IMVP7 protocol specification. Note the MAX17039 supports ALL CALL commands.

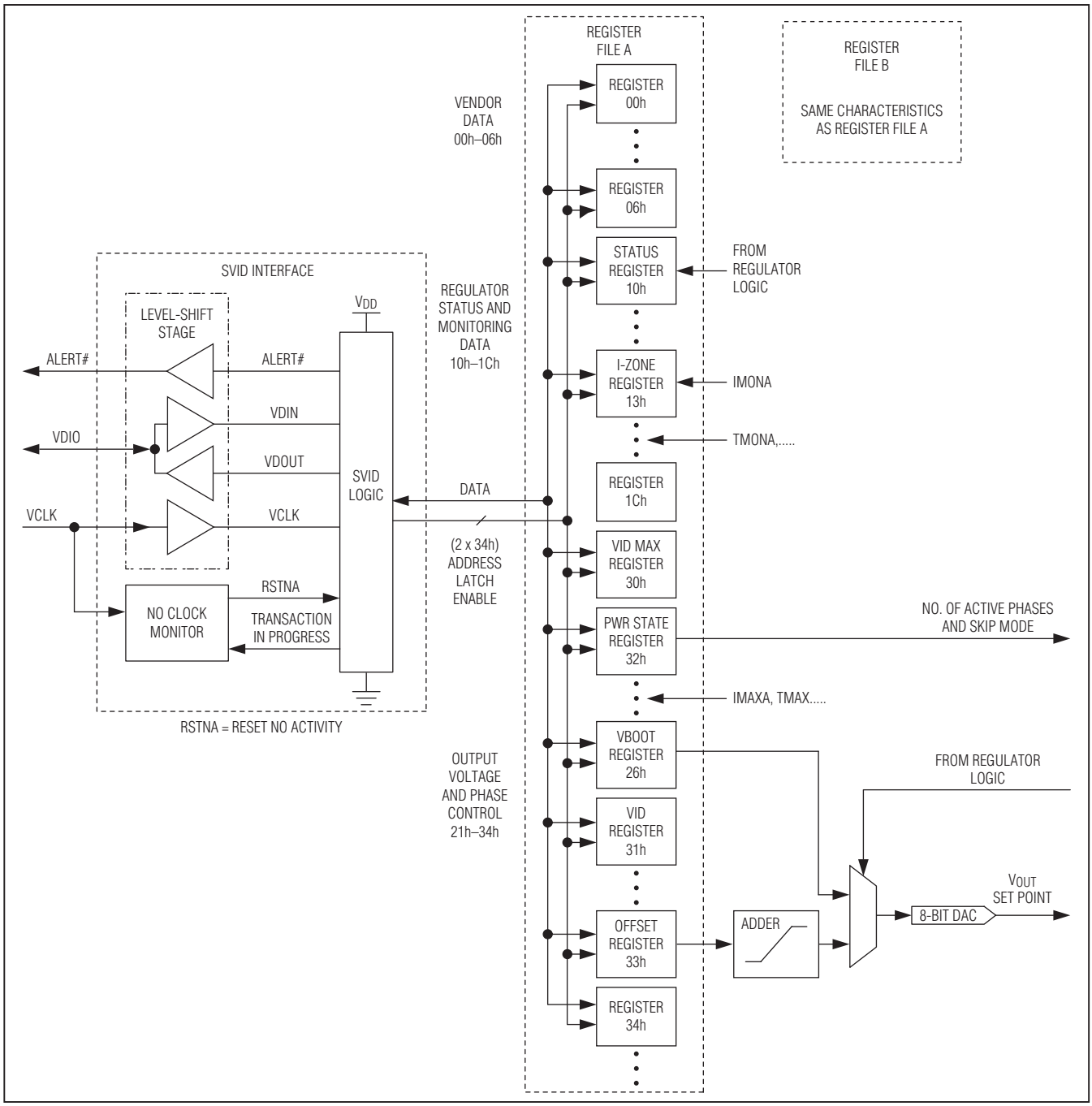


Figure 11. SVID Interface Block Diagram

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

Table 4. Serial VID Commands

INDEX	COMMAND	MASTER PAYLOAD CONTENTS	SLAVE PAYLOAD CONTENTS	DESCRIPTION
00h	Extended	Extended command index	—	Not supported.
01h	SetVID_Fast	VID code	—	Command sets the new SVID target (up or down) at the fast slew rate programmed by the SR_ input. When the MAX17039 receives SVID for an upward transition, it exits all low-power states to PS0 to ensure the fastest slew to the new voltage. When the output reaches the new VID target, the VR_settled bit is set and ALERT# goes low.
02h	SetVID_Slow	VID code	—	Command sets the new SVID target (up or down) at the slow slew rate equal to 1/4 the fast slew rate programmed by the SR_ input. When the MAX17039 receives SVID for an upward transition, it exits all low-power states to PS0 to ensure the fastest slew to the new voltage. When the output reaches the new VID target, the VR_settled bit is set and ALERT# goes low.
03h	SetVID_Decay	VID code	—	Command sets the new SVID target, but **does not** control the slew rate. The output is allowed to decay at a rate defined by the load. This command is normally used for only high-to-low output transitions. When the output reaches the new VID target, the VR_settled bit is set but ALERT# does not go low.
04h	SetPS	Byte indicating power status of CPU	—	Command sets the power state PS_ of the MAX17039 so it can enable the correct number of phases and control SKIP mode for optimized operation. See the *Power States (PS)* section.
05h	SetRegADR	Address of the index in the register file; see Table 5.	—	Command sets the address pointer in the data register table. Typically, the next command, SetRegDAT, is the payload that gets loaded into this address. However, for multiple writes to the same address, only one SetRegADR is needed.
06h	SetRegDAT	New data register contents	—	Command writes the contents to the data register that was previously identified by the address pointer with SetRegADR.
07h	GetReg	Define which register	Specified register contents	Command returns the contents of the specified register as the payload. See the *Data and Configuration Registers* section for a description of supported registers.
08h	TestMode	—	—	—
09h–1Fh	Reserved	—	—	—

SetVID_Fast (01h)

The SetVID_Fast command contains the target SVID in the payload byte. The range of voltage is defined in Table 3. The MAX17039 drives the respective output voltage to the new VID setting with a fast slew rate as defined in the Fast-Slew-Rate Data register (24h). This register is programmed with the SR_ pin.

The SetVID_Fast command is preemptive. If the SVID bus master interrupts current transition and attempts to move the output to a new VID, the regulator responds immediately after registering the new command. With back-to-back SetVID commands, the MAX17039 resets the ALERT# line after the ACK, and it starts moving its output voltage to the new target. For the case of back-to-back SetVID commands to the same voltage, the VR asserts ALERT# immediately since there is no settling time.

SetVID_Slow (02h)

The SetVID_Slow command contains the target SVID in the payload byte. The range of voltage is defined in Table 3. The MAX17039 drives the respective output voltage to the new VID setting with a slow slew rate as defined in the Slow-Slew-Rate Data register (25h). SetVID_Slow transitions occur at 1/4 the fast slew rate.

The SetVID_Slow command is preemptive. If the SVID bus master interrupts current transition and attempts to move the output to a new VID, the regulator responds immediately after registering the new command. With back-to-back SetVID commands, the MAX17039 resets the ALERT# line after the ACK and it starts moving its output voltage to the new target. For the case of back-to-back SetVID commands to the same voltage, the VR asserts ALERT# immediately since there is no settling time.

SetVID_Decay (03h)

The SetVID_Decay command contains the target SVID in the payload byte. The range of voltage is defined in Table 3. It is normally used for VID down transitions. The MAX17039 does not control the slew rate, instead the output voltage decays at a rate defined by the output load current.

The SetVID_Decay command is preemptive for positive-going SetVID_Fast or SetVID_Slow commands. If the SVID bus master interrupts current transition and attempts to move the output to a new VID, the regulator responds immediately after registering the new command. The ALERT# line remains high during the SetVID_Decay transition. The SVID bus master normally does not issue a SetVID_Decay with target voltage higher than current setting. If this occurs, the MAX17039 rejects the command (acknowledge = 11b) and remains at the same voltage setting.

SetPS—Set Power State (04h)

The SetPS command sends a byte that is encoded as to the power state of the CPU. Based on the power-state command, the MAX17039 can change its configuration to meet the processor's power needs with greater efficiency. See the *Power States (PS)* section. The format of the SetPS command payload is:

B7	B6	B5	B4	B3	B2	B1	B0
PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0

If the SVID bus master attempts to program a power state that is not supported, the MAX17039 acknowledges with NAK (01b) and enters the lowest power state that is supported. The MAX17039 enters the new power state after it sends back the ACK of the SetPS command. If the MAX17039 is in a low-power state and receives a SetVID_ command (either up or down), then the regulator exits the low-power state to normal mode (PS0) to move the voltage up as fast as possible and resets the Power-State register to 00h when it acknowledges the SetVID(UP) command. The microprocessor must reissue a low-power state command if it is in a low-current condition at the new higher voltage.

The SetPS command is not preemptive; the MAX17039 waits until it has completed the previous command or the output has settled, then it changes power state. If the VR receives a SetPS command while it is still slewing from the previous SetVID command, the MAX17039 rejects (11b) the SetPS command, indicating it cannot carry out the command. The MAX17039 enters the new power state after it sends back the ACK of the SetPS command.

SetRegADR (05h), SetRegDAT (06h), and GetReg (07h)

Accessing the MAX17039's register file is accomplished with three commands: SetRegADR, SetRegDAT, and GetReg. SetRegADR sets the target register address, SetRegDAT writes data to the specified register, and GetReg retrieves data from the specified register.

To program a register, two commands must be executed in order. SetRegADR picks the address in Table 5 and then the next command would be a SetRegDAT to write or set the data into the previously defined address. For multiple writes to the same address, only one SetRegADR command is sent, followed by multiple SetRegDAT commands.

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

All the telemetry data from the MAX17039 is accessed through the GetReg command. The payload byte in the command contains an index into the data register file. A slave device that receives the GetReg command must insert the contents of the indexed data register into the payload of the response.

If the SVID bus master issues a SetRegADR or GetReg command that contains a nonsupported address, the MAX17039 responds with the REJECT (11b) acknowledge.

TestMode (08h)

The TestMode command is used to place the MAX17039 into test mode.

Data and Configuration Registers

The MAX17039 supports the data and configuration registers listed in Table 5. The registers retain data as long as V_{CC} is powered up and in regulation. All data is lost and registers returned to default contents during hard reset (VR_ENABLE = low) or V_{CC} = 0V. Regulator A and regulator B include separate, independent register files. Access definitions for these registers are as follows:

- RO = Read only
- RW = Read write
- R-M = Read by SVID bus master (CPU)
- W-PWM = Written by MAX17039 only
- HC = Hard coded into the MAX17039
- Platform = Programmed at PCB assembly using pin strapping—cannot be overwritten by master
- Master = Programmed by the SVID bus master through the SVID bus with SetRegADR, SetRegDAT
- PWM = Programmed by MAX17039 during operation for reporting information to the master.

Table 5. Data and Configuration Register File Definition

INDEX	REGISTER NAME	DESCRIPTION	ACCESS	DEFAULT DATA
00h	Vendor ID	The vendor ID is unique to Maxim and is assigned by Intel.	RO HC	17h
01h	Product ID	Uniquely identifies the MAX17039 product.	RO HC	01h
02h	Product Revision	Uniquely identifies the revision or stepping of the MAX17039.	RO HC	01h
03h	Product Date Code	Not supported.	—	—
04h	Lot Code	Not supported.	—	—
05h	Protocol ID	Identifies what version of SVID protocol supported by the MAX17039.	RO HC	01h
06h	Capability	SVID capability register	RO HC	00h
07h–0Fh	Not Used	—	—	—
10h	Status1	Data register containing the Status1 data. This register is read after the ALERT# signal is asserted. It communicates the status of the MAX17039. Status1 is cleared after a GetReg (10h) command.	R-M W-PWM	01h
11h	Status2	Data register containing the Status2 data. Status2 is cleared after a GetReg (11h) command.	R-M W-PWM	00h
12h	Temperature-Zone	Data register containing the measurement data from the THERM_ input.	R-M W-PWM	00h
13h	ICC Zone	Data register containing current zones that have been entered. I_{OUT} is also mirrored on the IMON_ pin from PWM IC where 0V = 0A, 999mV = ICCMax	R-M W-PWM	00h
14h	SVID Bus Error	This status register contains information on errors that have occurred on the bus.	R-M W-PWM	00h

Table 5. Data and Configuration Register File Definition (continued)

INDEX	REGISTER NAME	DESCRIPTION	ACCESS	DEFAULT DATA
15h	Current	Not supported.	R-M W-PWM	—
16h	Voltage	Not supported.	R-M W-PWM	—
17h	Temperature	Not supported.	R-M W-PWM	—
18h	Power	Not supported.	R-M W-PWM	—
19h	Input Current	Not supported.	R-M W-PWM	—
1Ah	Input Voltage	Not supported.	R-M W-PWM	—
1Bh	Input Power	Not supported.	R-M W-PWM	—
1Ch	Status2 Last Read	This register contains a copy of the Status2 data that was last read with the GetReg (Status2) command. In the case of a communications error or parity error, when the MAX17039 sends the payload back to the SVID bus master, the master can read the Status2 Last Read register so the alert data is not lost.	R-M W-PWM	—
1Dh–20h	Not Used	—	—	—
21h	ICC Max	Data register containing the maximum output current limit that the regulator supports. The register uses a binary format in amps (e.g., 64h = 100A).	RO Platform	Based on the IMAX_ Logic Voltage-Level Input
22h	Temp Max	Data register containing the temperature max the platform supports and the level VR_HOT# asserts. The platform design engineer programs this value during the design process. Binary format is in °C (e.g., 64h = +100°C).	RO Platform	Set Using the TMAX Multivalued Logic Input
23h	DC_LL	Not supported.	RO Platform	—
24h	SR Fast	Data register containing the fast slew-rate capability of the MAX17039 programmed at the SR_ input. Register format is in mV/µs (e.g., 0Ah = 10mV/µs).	RO Platform	Based on the SR_ Logic Voltage-Level Input
25h	SR Slow	Data register containing the slow slew-rate capability of the MAX17039. This value is 1/4 the rate programmed at the SR_ input. Register format is in mV/µs (e.g., 03h = 3mV/µs).	RO Platform	Based on the SR_ Logic Voltage-Level Input
26h	V_{BOOT}	Data register containing the boot voltage programmed at the VBOOT_ multivalued logic input. The register uses SVID data format (e.g., 97h = 1.0V).	RO Platform	Based on the VBOOT_ Logic Voltage-Level Input

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

Table 5. Data and Configuration Register File Definition (continued)

INDEX	REGISTER NAME	DESCRIPTION	ACCESS	DEFAULT DATA
27h	VR Tolerance	Not supported.	RO Platform	—
28h	Current-Offset	Not supported.	RO Platform	—
29h	Temperature Offset	Not supported.	RO Platform	-—
2Ah–2Fh	Not Used	—	—	—
30h	V_{OUT_MAX}	This register is programmable by the master and sets the maximum VID that the MAX17309 supports. If a higher VID code is received, the MAX17039 responds with a not supported acknowledge. The register uses SVID data format. **This register must be programmed by MASTER during boot-up sequence.**	RW Master	BFh (1.2V)
31h	VID Setting	Data register containing currently programmed VID voltage. The register uses SVID data format.	RW Master	At POR, this register contains the data based on the VBOOT_ input. Thereafter, it contains the last SVID code.
32h	Power State PS_	Register containing the current programmed power state. Default is 00h, normal power mode.	RW Master W-PWM	00h
33h	Offset	This register contains an offset added to the programmed SVID data. Data format is the number of SVID steps. Negative offsets are in the two's-complement format. Default 00h = no offset Bit 7 = sign bit 0000001 = offset +1 VID step 0000011 = offset +3 VID steps 1111111 = offset -1 VID step	RW Master	00h
34h	Multi-VR Configuration	This register contains the bit-mapped data for configuring multiple regulators that utilize the SVID bus.	RW Master	00h
35h	SetRegADR	This register is a scratchpad for temporarily storing the SetRegADR payload. The data is the address pointer for subsequent SetRegDAT commands.	RW Master	00h
36h–40h	Not Used	—	—	—

Status1 Register (10h)

The data in the Status1 register answers the questions: Is the output voltage in regulation? Is the regulator temperature approaching the thermal limit? Is the regulator's output current approaching current limit? Also, should the SVID bus master check the MAX17039 for SVID data errors? When there are any bit changes in Status1, the MAX17039 asserts the ALERT# pin to notify the SVID bus master to start the polling process of reading the status from each address on the bus.

Bit 0 in Status1 indicates that a SetVID command is completed and the output voltage has transitioned to within ±16mV (max) of the final target voltage. Bit 1 indicates that there has been a change to the Thermal-Zone register (12h). Bit 3 indicates that there has been a change to the ICC Zone register (13h). Bit 7 indicates that a change to the Status2 register was recorded. When bits 0, 1, or 7 change, the respective registers should be read in order to take further action.

The format of the Status1 register is:

B7	B6	B5	B4	B3	B2	B1	B0
Read Status 2	RSV 0b	RSV 0b	RSV 0b	RSV 0b	ICC MAX Alert	Therm Alert	VR Settled

Status2 Register (11h)

Parity and data frame errors are recorded in the Status2 register. When the SVID bus master reads Status2, the MAX17039 copies the contents into Status2 Last Read register (1Ch), then clears the contents of the Status2 register. In the case of a parity error in the payload, the master can read the Status2 Last Read register to get the status prior to reset.

The format of the Status2 register is:

B7	B6	B5	B4	B3	B2	B1	B0
RSV 0b	RSV 0b	RSV 0b	RSV 0b	RSV 0b	RSV 0b	SVID Data Frame Error	SVID Parity Error

Temperature-Zone Register (12h)

The digitized measurements from the thermistor bridges at THERMA and THERMB are recorded in the Temperature-Zone register. The required thresholds of the Temperature-Zone register are nonlinear, but equate to 3°C increments listed below. It is essential to use the correct resistor and thermistor values specified in Figure 1. When TMAX (bit 6) for either is exceeded at either THERMA or THERMB, VR_HOT# is pulled low. For each regulator, place the thermistor as close to the MOSFETs and inductors as possible. The MAX17039 EV kit provides a good example of thermistor placement.

The Temperature-Zone register and VR_HOT# functions are independent. In the event of an SVID bus problem, the VR_HOT# signal always responds correctly to force thermal throttling to prevent the CPU from catastrophically overheating.

ICC Zone Register (13h)

Current measurements from IMONA and IMONB are digitized and recorded in the ICC Zone register. IMAX_ or 100% point is scaled to the ICC MAX setting by the selection of the IMON_ load resistor. When bit 6 is asserted, the MAX17039 sets the IMAX_ alert bit in the Status1 register and asserts the alert line. The SVID bus master determines the appropriate action on the IMAX_ alert.

COMPARATOR TRIP POINTS AND EXAMPLE TEMPERATURES SCALED TO +100°C = 100%							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
103%	100%	97%	94%	91%	88%	85%	82%
+103°C	+100°C	+97°C	+94°C	+91°C	+88°C	+85°C	+82°C
EXAMPLE REGISTER CONTENTS FOR +95°C							
0	0	0	1	1	1	1	1

OUT OF SPECIFICATION	IMAX_	OUTPUT-CURRENT ZONES					
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
110%	100%	95%	90%	80%	70%	60%	50%

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

The analog IMON_ signals are scaled such that 999mV = IMAX_ and 0mV = 0 current. See the section on IMON_.

SVID Bus Error Register (14h)

Any transmission errors that result in a rejected bit pattern (11b) are recorded in the SVID Bus Error register. Similar to Status2, this register is cleared when the SVID bus master reads the register.

B7	B6	B5	B4	B3	B2	B1	B0
RSU 0	RSU 0	RSU 0	RSU 0	SVID Buffer Overflow	Register Not Set	Data Frame Count	Parity Error

Status2 Last Read (1Ch)

This register contains a copy of the Status2 data that was last read with the GetREG (Status2) command. In the case of a communications error or parity error, when the MAX17039 is sending the payload back to the SVID bus master, which can read the Status2 Last Read register so the alert data is not lost.

Platform Performance Registers

These registers are programmed on the platform PCB during manufacturing. The data tells the SVID bus master the performance capability of the MAX17039. Multivalued logic inputs are used to set the data in these registers.

ICC Max (21h)

This register contains information on the maximum current the motherboard VR supports. ICC Max is programmed with the IMAX_ multivalue logic input.

The current limit computed from the ILIM_ sense voltage is multiplied by the number of active phases in the regulator to determine the data in the ICC Max register. The data in this register is 8-bit binary format in amps (1A/LSB) (e.g., 4Bh = 75A).

IMAX_	$V_{ILIM\_}$ ($V_{CSP\_}$ - $V_{CSN\_}$) (mV)
V_{CC}	30
3V	25
2V	20
AGND	15

Temp Max (22h)

This register contains the maximum temperature the VR supports prior to issuing a thermal alert or VR_HOT#. Temp Max is programmed with the TMAX multivalue logic input.

TMAX	TEMPERATURE THRESHOLD (°C)
V_{CC}	+105
3V	+100
2V	+95
AGND	+90

The single-temperature threshold applies to both regulators A and B. The data in this register is in 8-bit binary format in degrees C. (e.g., 64h = +100°C).

SR Fast (24h)

This register contains the guaranteed minimum fast slew-rate data programmed at the SR_ multivalued logic input with an external resistor to ground. The data is in 8-bit binary format in dV/dt (e.g., 10mV/µs = 0Ah). See Table 6.

SR Slow (25h)

This register contains the guaranteed minimum slow slew-rate data, which is 1/4 the value programmed at the SR_ input. The data is in 8-bit binary format in dV/dt (e.g., 2mV/µs = 02h). See Table 6.

Table 6. Programmed Slew-Rate Data

R_{SRB} (kΩ)	FAST SLEW RATE (TYP) (mV/µs)	MINIMUM VALUE REPORTED IN 24h	SLOW SLEW RATE (TYP) (±mV/µs)	MINIMUM VALUE REPORTED IN 25h
114	±12.5	0Ah (±10mV/µs)	±3.925	02h (±2mV/µs)
89.8	±16.0	0Dh (±13mV/µs)	±4.000	03h (±3mV/µs)
71.5	±20.0	10h (±16mV/µs)	±5.000	04h (±4mV/µs)
56.9	±25.0	14h (±20mV/µs)	±6.250	05h (±5mV/µs)

V_{BOOT} (26h)

This register contains the value of the V_{BOOT} voltage as programmed at the VBOOT_ multivalued logic input.

The data format is the SVID code.

VBOOT_	BOOT VOLTAGE $V_{OUT\_}$ (V)
V_{CC}	1.10
3V	1.000
2V	0.900
AGND	0.000

V_{OUT_MAX} (30h)

This register is programmed by the CPU or SVID bus master to the maximum output voltage the CPU load can support. Any attempts to set the SVID above V_{OUT_MAX} are blanked and ignored. The MAX17039 responds with a not-supported acknowledge. The default value is 1.2V.

VID Setting (31h)

This register contains a copy of the currently programmed SVID data. The default value is 00h.

Power State PS_ (32h)

The Power State PS_ register contains information on the CPU's power-consumption status. The MAX17039 supports states PS0 through PS3. See the *Power States (PS)* section for a complete description of these states and the resulting operating mode change in the MAX17039. If a power state is requested that is not supported by the MAX17039, it acknowledges with a command rejected (11b) back to the SVID bus master. The PS_ register format is:

B7	B6	B5	B4	B3	B2	B1	B0
PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0

Offset Register (33h)

This register contains an offset that is added to the programmed SVID data. The format of this data is the number of SVID steps. For negative offsets, the value is the two's complement of the number of SVID steps.

The format of the Offset register is:

OFFSET OR VOLTAGE MARGIN							
B7	B6	B5	B4	B3	B2	B1	B0
Sign 0 = + 1 = -	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0

Default 00h = no offset

Bit 7 = Sign bit

0000001 = Offset +1 VID step

0000011 = Offset +3 VID steps

1111111 = Offset -1 VID step

Multi-VR Configuration Register (34h)

This register contains the bit-mapped data for configuring multiple regulators that utilize the SVID bus.

Bit 0 (VR__READY 0V) changes the response of the VR__READY power-good outputs. Writing a 0 (default) to this bit enables the standard definition for the VR__READY response. When a SetVID (0.0V) command is issued, the respective regulator turns off and VR__READY deasserts to 0V. Writing a 1 to bit 0 causes VR__READY to remain high when SetVID (0.0V) is issued and VR__READY only goes low under fault conditions or when the regulator is powered down using VR_ENABLE or the input supplies turn off.

Bit 1 (LOCK VID/PS) controls a lock function for the SVID code and power state PS_. When bit 1 is a 0, the MAX17039 is in normal mode and the SVID and PS are not locked. When bit 1 is a 1, the MAX17039 locks the SVID and PS_ data and rejects all SetVID and SetPS commands. Bit 1 must be changed back to 0 before the MAX17039 accepts new commands. The format of the Multi-VR Configuration register is:

MULTI-VR CONFIG (34h)							
B7	B6	B5	B4	B3	B2	B1	B0
RSV	RSV	RSV	RSV	RSV	RSV	Lock VID/PS	VR__READY 0V

SetRegADR Register (35h)

This register is a scratchpad register for temporarily storing the SetRegADR payload. The data is the address pointer for subsequent SetRegDAT commands.

Critical VR12/IMVP7 Functions

Voltage-Settled Function

The MAX17039 includes an auxiliary bank of comparators that detect when the SVID transition is complete and the output voltage is within the load-line tolerance window at the new SVID setting. After the output has settled, the MAX17039 sets the VR_settled bit in the Status1 register and asserts the ALERT# line.

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

Table 7. Power State (PS) Control of Regulator Operation

PS_	PHASE 1	PHASE 2	PHASE 3	SKIP MODE	COMMENTS
0	1	1	1	0	Full-power FPWM mode
1	1	0	0	0	1-phase FPWM
2	1	0	0	1	1-phase SKIP
3	1	0	0	1	1-phase SKIP
4	—	—	—	—	Not used
5	—	—	—	—	Not used
6	—	—	—	—	Not used
7	—	—	—	—	Not used

Power States (PS)

The SVID bus can be used to place the MAX17039 into multiple operating states to optimize the efficiency and power delivery capability. These states are entered by issuing a SetPS command and the programmed state is reflected in the Power State PS_ register (32h). The power states are listed in order of power savings:

PS0 = Represents full power or active mode.

PS1 = Used in active mode or sleep mode and it represents a low-current state.

PS2 = Used in sleep mode and it represents a low-voltage state and lower current state than PS1.

PS3 = Ultra-low-power sleep mode.

PS4–PS7 are undefined.

The SVID code and power states are independent and can change at any time as determined by the CPU operating state. When the MAX17039 exits any low-power state, it automatically enters PS0 for any SVID command that causes the output to increase from the previous value. Note the SVID bus master must reissue a low-power state command to return the MAX17039 to a low-current condition at the new higher voltage.

Regulators A and B respond identically to the PS_ commands described in Table 7. Regulator B controls only phase 1.

Multiphase Quick-PWM Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input voltage range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum load current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$. For multiphase systems, each phase supports a fraction of the load, depending on the current balancing. When properly balanced, the load current is evenly distributed among each phase:

$$I_{LOAD(PHASE)} = \frac{I_{LOAD}}{\eta_{TOTAL}}$$

  where η_{TOTAL} is the total number of active phases.
- **Switching frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor operating point:** This choice provides trade-offs between size vs. efficiency and transient response

vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 30% and 50% ripple current. For a multiphase core regulator, select an LIR value of ~ 0.4.

Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \eta_{TOTAL}\left(\frac{V_{IN} - V_{OUT}}{f_{SW} I_{LOAD(MAX)} LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where η_{TOTAL} is the total number of phases. Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must not saturate at the peak-inductor current (I_{PEAK}):

$$I_{PEAK} = \left(\frac{I_{LOAD(MAX)}}{\eta_{TOTAL}}\right)\left(1 + \frac{LIR}{2}\right)$$

Output-Capacitor Selection

Output-capacitor selection is determined by the controller stability requirements, and the transient soar and sag requirements of the application.

Output-Capacitor ESR

The output-filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high-enough ESR to satisfy stability requirements. In CPU VCORE converters and other applications where the output is subject to large-load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

The output voltage ripple of a step-down controller equals the total inductor ripple current multiplied by the output-capacitor's ESR. When operating multiphase systems out-of-phase, the peak inductor currents of each phase are staggered, resulting in lower output ripple voltage by reducing the total inductor ripple current. For multiphase operation, the maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \left[\frac{V_{IN} f_{SW} L}{(V_{IN} - \eta_{TOTAL} V_{OUT}) V_{OUT}}\right] V_{RIPPLE}$$

where η_{TOTAL} is the total number of active phases and f_{SW} is the switching frequency per phase. The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by the ESR and voltage rating rather than by capacitance value (this is true of polymer types). When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem. See the V_{SAG} and V_{SOAR} equations in the *Transient Response* section.

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi R_{EFF} C_{OUT}}$$

and:

$$R_{EFF} = R_{ESR} + R_{DROOP} + R_{PCB}$$

where C_{OUT} is the total output capacitance, R_{ESR} is the total equivalent series resistance, R_{DROOP} is the voltage-positioning gain, and R_{PCB} is the parasitic board resistance between the output capacitors and sense resistors. For a standard 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum, SANYO POSCAP, and Panasonic SP capacitors in widespread use at the time of publication have typical ESR zero frequencies below 50kHz. In the standard application circuit, the ESR needed to support a 30mV$_{P-P}$ ripple is 30mV/(40A x 0.3) = 2.5mΩ. Four 330µF/2.5V Panasonic SP (type SX) capacitors in parallel provide 1.5mΩ (max) ESR. With a 2mΩ droop and 0.5mΩ PCB resistance, the typical combined ESR results

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

in a zero at 30kHz. Ceramic capacitors have a high-ESR zero frequency, but applications with significant voltage positioning can take advantage of their size and low ESR. When using only ceramic output capacitors, output overshoot (V_{SOAR}) typically determines the minimum output capacitance requirement. Their relatively low capacitance value favors high switching-frequency operation with small inductor values to minimize the energy transferred from inductor to capacitor during load-step recovery. Unstable operation manifests itself in two related, but distinctly different ways: double-pulsing and feedback loop instablility.

Double-Pulsing and Feedback Loop Instability

Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This fools the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits. The easiest method for checking stability is to apply a very fast 10% to 90% maximum load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Transient Response

The inductor-ripple current impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time. For a dual-phase controller, the worst-case output sag voltage can be determined by:

$$V_{SAG} \approx \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2}{2\eta_{TOTAL} C_{OUT} V_{OUT}} \times \frac{T_{MIN}}{[KT_{SW} - T_{MIN}]}$$

and:

$$T_{MIN} = t_{ON} + t_{OFF(MIN)}$$

where $t_{OFF(MIN)}$ is the minimum off-time. See the *Electrical Characteristics* table. KT_{SW} is the programmed switching period, and η_{TOTAL} is the total number of active phases. K = 66% when NPH = 3, and K = 100% when NPH = 2. V_{SAG} must be less than the transient droop $\Delta I_{LOAD(MAX)} \times R_{DROOP}$. The capacitive soar voltage due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2\eta_{TOTAL} C_{OUT} V_{OUT}}$$

where η_{TOTAL} is the total number of active phases. The actual peak of the soar voltage is dependent on the time where the decaying ESR step and rising capacitive soar are at their maximum. This is best simulated or measured.

Input-Capacitor Selection

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. The multiphase Quick-PWM controllers operate out-of-phase, reducing the RMS input current. For duty cycles less than $100\%/\eta_{TOTAL}$ per phase, the I_{RMS} requirements can be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{\eta_{TOTAL} V_{IN}}\right)\sqrt{\eta_{TOTAL} V_{OUT}\left(V_{IN} - \eta_{TOTAL} V_{OUT}\right)}$$

where η_{TOTAL} is the total number of out-of-phase switching regulators. The worst-case RMS current requirement occurs when operating with $V_{IN} = 2\eta_{TOTAL}V_{OUT}$. At this point, the above equation simplifies to $I_{RMS} = 0.5 \times I_{LOAD}/\eta_{TOTAL}$. Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters.

High-Side MOSFET Power Dissipation

The conduction loss in the high-side MOSFET (N_H) is a function of the duty factor, with the worst-case power dissipation occurring at the minimum input voltage:

$$PD\left(N_H\,Resistive\right) = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

where η_{TOTAL} is the total number of phases. Calculating the switching losses in the high-side MOSFET (N_H) is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These

factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\ (N_H\ Switching) = \left(\frac{V_{IN} I_{LOAD} f_{SW}}{\eta_{TOTAL}}\right)\left(\frac{Q_{G(SW)}}{I_{GATE}}\right) + \frac{C_{OSS} V_{IN}^2 f_{SW}}{2}$$

where C_{OSS} is the N_H MOSFET's output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the N_H MOSFET, and I_{GATE} is the peak gate-drive source/sink current. The optimum high-side MOSFET trades the switching losses with the conduction ($R_{DS(ON)}$) losses over the input voltage range. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Low-Side MOSFET Power Dissipation

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD\ (N_L\ Resistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, the circuit can be overdesigned to tolerate:

$$I_{LOAD} = \eta_{TOTAL}\left(I_{VALLEY(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}\right)$$

$$= \eta_{TOTAL}\left(I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)} LIR}{2}\right)\right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good-size heatsink to handle the overload power dissipation. Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two thermally enhanced 8-pin SOs), and is reasonably priced. Make sure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems might occur. See the *MOSFET Gate Drivers* section. The optional Schottky diode (DL) should have a low forward voltage and be able to handle the load current per phase during the dead times.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified in the MOSFET's data sheet. For example, assume (1) FDS6298 n-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single FDS6298 has a maximum gate charge of 10nC (VGS = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{1 \times 10nC}{200mV} = 0.05\mu F$$

Selecting the closest standard value, this example requires a 0.1µF ceramic capacitor.

Current Limit (IMAX_)

The MAX17039 has a current limit that is programmed in discrete increments using a multivalue logic input IMAX_. The regulator's maximum current limit, which is the current limit per phase times the maximum number of active phases, is reflected in the IMAX_ register (21h) for the respective regulator.

IMAX_	$V_{ILIM\_}$ ($V_{CSP\_}$ - $V_{CSN\_}$)(mV)
V_{CC}	30
3V	25
2V	20
AGND	15

The IMAX_ voltage determines the valley current-sense threshold $V_{ILIM\_}$.

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{VALLEY} > I_{LOAD(MAX)}\left(1-\frac{LIR}{2}\right)$$

where:

$$I_{VALLEY} = \frac{V_{LIMIT}}{R_{SENSE}}$$

where R_{SENSE} is the sensing resistor or effective inductor DCR.

Slew-Rate Control

The MAX17039 has slew-rate control that is programmed in discrete increments using a multivalue logic-input SR_. Connect a 1% accurate resistor $R_{SR\_}$ from SR_ to AGND to set the fast slew rate. The MAX17039 digitizes the voltage at SR_ to set one of four discrete slew rates. The regulator's slow slew rate is set automatically relative to the fast slew rate (SR_SLOW = 1/4 SR_FAST). The selected fast and slow slew rates are reflected in registers 24h and 25h, respectively.

Voltage Positioning and Loop Compensation

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the output capacitance and processor's power-dissipation requirements. The MAX17039 uses a transconductance amplifier to set the transient and DC output-voltage droop (Figures 3 and 4) as a function of the load. This adjustability allows flexibility in the selected current-sense resistor value or inductor DCR, and allows smaller current-sense resistance to be used, reducing the overall power dissipated.

Steady-State Voltage Positioning

Connect a resistor (R_{FB}) between FB and V_{OUT} to set the DC steady-state droop (load line) based on the required voltage-positioning slope (R_{DROOP}):

$$R_{FB} = \frac{R_{DROOP}}{R_{SENSE}G_{m(FB)}}$$

where the effective current-sense resistance (R_{SENSE}) depends on the current-sense method (see the *Current Sense* section), and the voltage-positioning amplifier's transconductance ($G_{m(FB)}$) is typically 600µS as defined in the *Electrical Characteristics*. The controller sums together the input signals of the current-sense inputs (CSP_, CSN_). When the inductors' DCR is used as the current-sense element (R_{SENSE} = R_{DCR}), each current-sense input should include an NTC thermistor to minimize the temperature dependence of the voltage-positioning slope.

Applications Information

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board with their ground terminals flush against one another. The layout of the MAX17039 is intimately related to the layout of the CPU. The high-current output paths from the regulator must flow cleanly into the high-current inputs on the processor. For VR12/IMVP7 processors, these inputs are orthogonal. This arrangement effectively forces the regulator to be located diagonally with respect to the processor. Refer to the MAX17039 Evaluation Kit specifications for a layout example and follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
- Connect all analog grounds to a separate solid copper plane, which connects to the ground pin of the Quick-PWM controller. This includes the V_{CC} bypass capacitor, FB, and GNDS bypass capacitors.
- Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCB (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
- Keep the high-current, gate-driver traces (DL_, DH_, LX_, and BST_) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents. CSP_ and CSN_ connections for current limiting and voltage positioning must be made using Kelvin-sense connections to guarantee the current-sense accuracy.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side

MOSFET or between the inductor and the output filter capacitor.

- Route high-speed switching nodes away from sensitive analog areas (FB_, CSP_, CSN_, etc.).

Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET. The DL gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC).
3) Group the gate-drive components (BST_ diodes and capacitors, VDD_ bypass capacitors) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in the standard application circuits. This diagram can be viewed as having four separate ground planes:
   - Input/output ground, where all the high-power components go; the power ground plane, where the ground pin and VDD_ bypass capacitors go; the master's analog ground plane, where sensitive analog components, the master's ground pin, and V_{CC} bypass capacitor go; and the slave's analog ground plane, where the slave's GND pin and V_{CC} bypass capacitor go. The master's GND plane must meet the GND plane only at a single point directly beneath the IC. Similarly, the slave's GND plane must meet the GND plane only at a single point directly beneath the IC. The respective master and slave ground planes should connect to the high-power output ground with a short metal trace from GND to the source of the low-side MOSFET (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.
5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN-EP	T5677+2	21-0144	90-0043

Dual-Output, 3-Phase + 1-Phase Quick-PWM Controller for VR12/IMVP7

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—