

2.5A Octal Three-Level Digital Pulsers with TR Switches

MAX14988

General Description

The MAX14988 octal three-level, high-voltage (HV) pulser device generates high-frequency HV bipolar pulses (up to $\pm 105\text{V}$) from low-voltage control logic inputs for driving piezoelectric transducers in ultrasound systems. All eight channels have embedded overvoltage-protection diodes and an integrated active return-to-zero clamp. The device has embedded independent (floating) power supplies (FPS) and level shifters that allow signal transmission without the need for external HV capacitors. The device also features eight integrated transmit/receive (T/R) switches.

The device features two modes of operation: shutdown mode and octal three-level pulser mode (with integrated active return-to-zero clamp). In octal three-level pulser mode, each channel is controlled by two logic inputs (DINN_ /DINP_) and the active return to zero features half the current driving of the pulser 1.25A (typ).

The device can operate both in clocked and transparent mode. In clocked mode, data inputs can be synchronized with a clean differential or single-ended clock to reduce phase noise associated with FPGA output signals that are detrimental for Doppler analysis. In transparent mode, the synchronization feature is disabled and output reflects the data input after a 10.8ns delay. The device features adjustable maximum current (0.44A to 2.5A) to reduce power consumption when full current capability is not required.

The device features integrated grass-clipping diodes (with low parasitic capacitance) for receive (Rx) and transmit (Tx) isolations. The device features a damping circuit that can be activated as soon as the transmit burst is over. The damping circuit has an on-resistance of 200 Ω . It fully discharges the pulser's output internal node before the grass-clipping diodes.

The device is available in a 68-pin (10mm x 10mm) TQFN package with an exposed pad and are specified over the -40°C to $+85^{\circ}\text{C}$ extended temperature range.

Ordering Information appear at end of data sheet.

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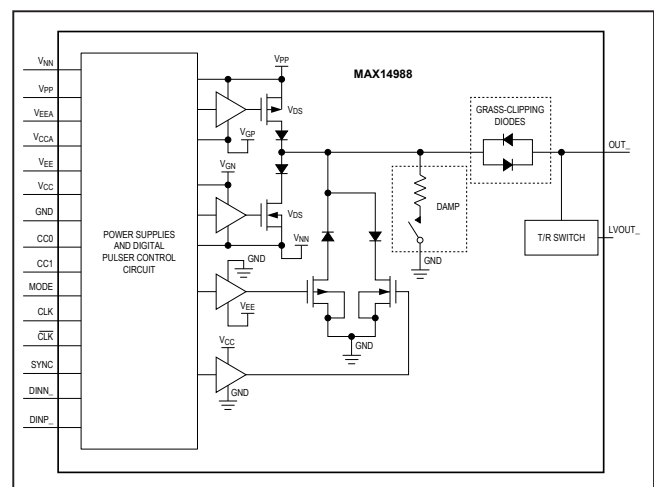
Benefits and Features

- Saves Space in High-Channel-Count and Portable Systems
 - High Density
 - 8 Channels (Three-Level Operation)
 - Integrated Low-Power T/R Switches
 - DirectDrive® Architecture Eliminates External High-Voltage Capacitor
 - No External Floating Power Supply (FPS) Required
- High Performance Enhances Image Quality)
 - Excellent -43dBc (typ) THD for Second Harmonic at 5MHz
 - Sync Function Eliminates Effects of FPGA Jitter and Improves Performance in Doppler Mode
 - Low Propagation Delay 10.8ns (typ)
 - Strong Active Return to Zero
- Conserves Power
 - Low Quiescent Power Dissipation (13mW/Channel)
 - Programmable Current Capability
 - Shutdown Mode

Applications

- Ultrasound Medical Imaging
- Industrial Flaw Detection
- Piezoelectric Drivers
- Test Equipment

Functional Diagram



19-7467; Rev 0; 12/14

Absolute Maximum Ratings

(All voltages referenced to GND.)

V_{DD} Logic Supply Voltage Range-0.3V to +5.6V
 V_{CC}, V_{CCA} Positive Driver Supply Voltage Range ..-0.3V to +5.6V
 V_{EE}, V_{EEA} Negative Driver Supply Voltage Range...-5.6V to +0.3V
 V_{NN} High Negative Supply Voltage Range -110V to +0.3V
 V_{PP} High Positive Supply Voltage Range -0.3V to +110V
 OUT_ Output Voltage Range V_{NN} to V_{PP}
 LVOUT_ Output Voltage Range (100mA Maximum Current)..... -1.2V to +1.2V
 DINN_, DINP_, CC_, SYNC, MODE.....-0.3V to +5.6V
 CLK, CLK Voltage Range..... -0.3V to (V_{CC} + 0.3V)

THP Logic Output Voltage Range.....-0.3V to +5.6V
 V_{GP} Output Voltage Range.....max[(V_{PP} - 5.6V), (V_{EE} + 0.6V)] to (V_{PP} + 0.3V)
 V_{GN} Output Voltage Range.....(V_{NN} - 0.3V) to min [(V_{CC} + 0.6V), (V_{NN} + 5.6V)]
 Continuous Power Dissipation (T_A = +70°C)
 TQFN (derate 50mW/NC above +70°C).....4000mW
 Operating Temperature Range..... -40°C to +85°C
 Maximum Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (soldering, 10s) +300°C
 Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA})20°C/W Junction-to-Case Thermal Resistance (θ_{JC}).....0.5°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.analog.com/thermal-tutorial.

DC Electrical Characteristics

(V_{DD} = +3V, V_{CC} = +5V, V_{CCA} = +5V, V_{EE} = -5V, V_{EEA} = -5V, V_{PP} = +105V, V_{NN} = -105V, 1µF bypass capacitor between V_{GN} and V_{NN}, 1µF bypass capacitor between V_{GP} and V_{PP}, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------|--|-----------------------|-----------------------|-------|------------------|
| POWER SUPPLIES (V_{DD}, V_{CC}, V_{EE}, V_{PP}, V_{NN}) | | | | | | |
| Logic Supply Voltage | V _{DD} | | +1.7 | +3 | +5.25 | V |
| Positive Drive Supply Voltage | V _{CC_} | | +4.9 | +5 | +5.1 | V |
| Negative Drive Supply Voltage | V _{EE_} | | -5.1 | -5 | -4.9 | V |
| High-Side Supply Voltage | V _{PP} | | 0 | | +105 | V |
| Low-Side Supply Voltage | V _{NN} | | -105 | | 0 | V |
| LOGIC INPUTS/OUTPUTS (DINN_, DINP_, MODE, SYNC, CC_) | | | | | | |
| Low-Level Input Threshold | V _{IL} | | | 0.2 x V _{DD} | | V |
| High-Level Input Threshold | V _{IH} | | 0.8 x V _{DD} | | | V |
| Differential Input Resistance Between DINP _x and DINN _x | RIND | | 70 | 100 | 170 | kΩ |
| Pulldown Input Resistance Pins MODE, SYNC, CC0, CC1 | RPD | | 70 | 100 | 170 | kΩ |
| Logic Input Capacitance | C _{IN} | | | 4 | | pF |
| Logic Input Leakage DINP, DINN | I _{IN} | V _{IN} = 0V or V _{DD} | -1 | 0 | +1 | µA |
| THP Low-Level Output Voltage | V _{OL} | Pullup resistor to V _{DD} (R _{PULLUP} = 1kΩ) | | | 0.1 | V |
| CLOCK INPUTS (CLK, CLK)—DIFFERENTIAL MODE | | | | | | |
| Differential Clock Input Voltage Range | V _{CLKD} | | 0.2 | | 2 | V _{P-P} |

DC Electrical Characteristics (continued)

($V_{DD} = +3V$, $V_{CC} = +5V$, $V_{CCA} = +5V$, $V_{EE} = -5V$, $V_{EEA} = -5V$, $V_{PP} = +105V$, $V_{NN} = -105V$, $1\mu F$ bypass capacitor between V_{GN} and V_{NN} , $1\mu F$ bypass capacitor between V_{GP} and V_{PP} , no load, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|-------------------------------------|---|--|---------------------|-----|-------------------|------------|
| Common-Mode Voltage | V_{CLKCM} | | | $V_{CC}/2$ | | | V |
| Common-Mode Voltage Range | V_{CL} | | | $V_{CC}/2 - 0.45$ | | $V_{CC}/2 + 0.45$ | V |
| Input Resistance | R_{CLK} , $R_{\overline{CLK}}$ | Differential | | 4.9 | 7 | 10.2 | k Ω |
| | | Common mode | | 16 | 23 | 31 | k Ω |
| Input Capacitance | C_{CLK} , $C_{\overline{CLK}}$ | Capacitance to GND (each input) | | 4 | | | pF |
| CLOCK INPUTS (CLK, \overline{CLK})—SINGLE-ENDED MODE ($V_{CLK} < 0.1V$) | | | | | | | |
| Low-Level Input | V_{IL} | CLK | | $0.2 \times V_{DD}$ | | | V |
| High-Level Input | V_{IH} | CLK | | $0.8 \times V_{DD}$ | | | V |
| Single-Ended Mode Selection Threshold Low | V_{IL} | CLK | | 0.1 | | | V |
| Single-Ended Mode Selection Threshold High | V_{IH} | CLK | | 1 | | | V |
| Input Capacitance (CLK) | C_{CLK} | | | 4 | | | pF |
| Logic Input Leakage (CLK) | I_{CLK} | $V_{CLK} = 0V$ or V_{DD} | | -1 | 0 | +1 | μA |
| Pullup Current (CLK) | I_{CLK} | $V_{CLK} = 0V$ | | 120 | | 180 | μA |
| SUPPLY CURRENT—SHUTDOWN MODE (MODE = Low) | | | | | | | |
| V_{DD} Supply Current | I_{DD} | All inputs connected to GND or V_{DD} | | 12 | | 20 | μA |
| V_{CC} Supply Current | I_{CC} | All inputs connected to GND or V_{DD} | | 22 | | 35 | μA |
| V_{CCA} Supply Current | I_{CCA} | All inputs connected to GND or V_{DD} | | 0 | | 1 | μA |
| V_{EE} Supply Current | I_{EE} | All inputs connected to GND or V_{DD} | | 30 | | 50 | μA |
| V_{EEA} Supply Current | I_{EEA} | All inputs connected to GND or V_{DD} | | 0 | | 1 | μA |
| V_{PP} Supply Current | I_{PP} | All inputs connected to GND or V_{DD} | | 0 | | 10 | μA |
| V_{NN} Supply Current | I_{NN} | All inputs connected to GND or V_{DD} | | 0 | | 10 | μA |
| SUPPLY CURRENT—NORMAL OPERATION MODE, NO LOAD (MODE = High) | | | | | | | |
| V_{DD} Supply Current (Quiescent Mode) | I_{DD} | All inputs connected to GND or V_{DD} | Transparent or single-ended clock mode | 13 | | 30 | μA |
| V_{EE} Supply Current (Quiescent Mode) | I_{EEQ} | | | 0.15 | | 0.3 | mA |
| V_{EEA} Supply Current (Quiescent Mode) | I_{EEAQ} | $DINN_ = DINP_ = GND$ | | | | 0.01 | mA |
| | | $DINN_ = DINP_ = V_{DD}$ | | 8 | | 13 | |

DC Electrical Characteristics (continued)

($V_{DD} = +3V$, $V_{CC} = +5V$, $V_{CCA} = +5V$, $V_{EE} = -5V$, $V_{EEA} = -5V$, $V_{PP} = +105V$, $V_{NN} = -105V$, $1\mu F$ bypass capacitor between V_{GN} and V_{NN} , $1\mu F$ bypass capacitor between V_{GP} and V_{PP} , no load, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------|---|-----|------|-----|---------|
| V_{CC} Supply Current (Quiescent Mode) | I_{CCQ} | $DINN_ = DINP_ = GND$ | | 0.25 | 0.5 | mA |
| V_{CCA} Supply Current (Quiescent Mode) | I_{CCAQ} | $DINN_ = DINP_ = GND$ | | 0.01 | | mA |
| | | $DINN_ = DINP_ = V_{DD}$ | | 8 | 13 | |
| $V_{CC_}$ Supply Current Increase in Clocked Mode | $\Delta I_{CC_}$ | Differential clock mode | | 3.7 | 7 | mA |
| V_{NN} Total Supply Current (Quiescent Mode) | I_{NNQ} | All inputs connected to GND or V_{DD} | | 100 | 170 | μA |
| V_{PP} Total Supply Current (Quiescent Mode) | I_{PPQ} | All inputs connected to GND or V_{DD} | | 100 | 170 | μA |
| Total Power Dissipation per Channel (Quiescent Mode) | P_{PDIS1} | T/R switch off, damp off (transparent mode) | | 3 | | mW |
| | P_{PDIS2} | $DINN_ = DINP_ = V_{DD}$ (transparent mode) | | 13 | | |
| V_{DD} Supply Current | I_{DD1} | CW Doppler (Note 4), transparent or single-ended clock mode | | 0.1 | 0.2 | mA |
| | I_{DD2} | B mode (Note 5), transparent or single-ended clock mode (Figure 1) | | | 30 | μA |
| V_{EE} Supply Current | I_{EE1} | 8 channels switching, CW Doppler (Note 4), $CC0 = high$, $CC1 = high$ | | 37 | 80 | mA |
| | I_{EE2} | 8 channels switching, B mode (Note 5) (Figure 1), $CC0 = low$, $CC1 = low$ | | 0.5 | | |
| V_{EEA} Supply Current | I_{EEA1} | 8 channels switching, CW Doppler (Note 4), $CC0 = high$, $CC1 = high$ | | 0 | | mA |
| | I_{EEA2} | 8 channels switching, B mode (Note 5) (Figure 1), $CC0 = low$, $CC1 = low$ | | 8 | | |
| V_{CC} Supply Current | I_{CC1} | 8 channels switching, CW Doppler (Note 4), $CC0 = high$, $CC1 = high$ | | 21 | 40 | mA |
| | I_{CC2} | 8 channels switching, B mode (Note 5) (Figure 1), $CC0 = low$, $CC1 = low$ | | 0.5 | 1 | |

DC Electrical Characteristics (continued)

($V_{DD} = +3V$, $V_{CC} = +5V$, $V_{CCA} = +5V$, $V_{EE} = -5V$, $V_{EEA} = -5V$, $V_{PP} = +105V$, $V_{NN} = -105V$, $1\mu F$ bypass capacitor between V_{GN} and V_{NN} , $1\mu F$ bypass capacitor between V_{GP} and V_{PP} , no load, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|--|------------------------|-----|-----|----------|
| V_{CCA} Supply Current | I_{CCA1} | 8 channels switching, CW Doppler (Note 4), CC0 = high, CC1 = high | | 0 | | mA |
| | I_{CCA2} | 8 channels switching, B mode (Note 5) (Figure 1), CC0 = low, CC1 = low | | 8 | | |
| V_{CC} Supply Current Increase in Clocked Mode | ΔI_{CC} | Differential clock mode | | 5.6 | | mA |
| V_{NN} Supply Current | I_{NN1} | 8 channels switching, CW Doppler, CC0 = high, CC1 = high, $R_L = 1k\Omega$, $C_L = 240pF$ (Note 4) | | 127 | 200 | mA |
| | I_{NN2} | 8 channels switching, B mode (Figure 1), CC0 = low, CC1 = low, $R_L = 1k\Omega$, $C_L = 240pF$ (Note 5) | | 1.9 | 2.8 | |
| V_{PP} Supply Current | I_{PP1} | 8 channels switching, CW Doppler, CC0 = high, CC1 = high, $R_L = 1k\Omega$, $C_L = 240pF$ (Note 4) | | 146 | 230 | mA |
| | I_{PP2} | 8 channels switching, B mode (Figure 1), CC0 = low, CC1 = low, $R_L = 1k\Omega$, $C_L = 240pF$ (Note 5) | | 3.3 | 5 | |
| Power Dissipation per Channel (Octal Three-Level Mode) | PD_{CW} | 1 channel switching, CW Doppler (Note 4) | | 207 | | mW |
| | PD_{PW} | 1 channel switching, B mode (Note 5) (Figure 1), CC0 = low, CC1 = low, $R_L = 1k\Omega$, $C_L = 240pF$ | | 79 | | |
| OUTPUT STAGE | | | | | | |
| V_{NN} Connected Low-Side Output Impedance | R_{OLS} | $I_{OUT_} = -50mA$ | CC0 = low, CC1 = low | 7 | 16 | Ω |
| | | | CC0 = high, CC1 = low | 9 | | |
| | | | CC0 = low, CC1 = high | 17 | | |
| | | | CC0 = high, CC1 = high | 32 | 60 | |
| V_{PP} Connected High-Side Output Impedance | R_{OHS} | $I_{OUT_} = +50mA$ | CC0 = low, CC1 = low | 7 | 16 | Ω |
| | | | CC0 = high, CC1 = low | 9 | | |
| | | | CC0 = low, CC1 = high | 17 | | |
| | | | CC0 = high, CC1 = high | 32 | 60 | |

DC Electrical Characteristics (continued)

($V_{DD} = +3V$, $V_{CC} = +5V$, $V_{CCA} = +5V$, $V_{EE} = -5V$, $V_{EEA} = -5V$, $V_{PP} = +105V$, $V_{NN} = -105V$, $1\mu F$ bypass capacitor between V_{GN} and V_{NN} , $1\mu F$ bypass capacitor between V_{GP} and V_{PP} , no load, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|--------------|---|------------------------|------|------|-----|------------|
| Clamp nFET Output Impedance | R_{ONG} | $I_{OUT_} = -50mA$, | | | 11 | 22 | Ω |
| Clamp pFET Output Impedance | R_{OPG} | $I_{OUT_} = +50mA$ | | | 11 | 22 | Ω |
| Active Damp Output Impedance | R_{DAMP} | Before grass-clipping diode | | | | 200 | Ω |
| V_{NN} Connected Low-Side Output Current | I_{OLS} | $V_{DS} = +100V$ | CC0 = low, CC1 = low | | 2.5 | | A |
| | | | CC0 = high, CC1 = low | | 1.76 | | |
| | | | CC0 = low, CC1 = high | | 0.88 | | |
| | | | CC0 = high, CC1 = high | | 0.44 | | |
| V_{PP} Connected High-Side Output Current | I_{OHS} | $V_{DS} = +100V$ | CC0 = low, CC1 = low | | 2.5 | | A |
| | | | CC0 = high, CC1 = low | | 1.76 | | |
| | | | CC0 = low, CC1 = high | | 0.88 | | |
| | | | CC0 = high, CC1 = high | | 0.44 | | |
| GND-Connected nFET Output Current | I_{ONG} | $V_{DS} = +100V$ | | | 1.25 | | A |
| GND-Connected pFET Output Current | I_{OPG} | $V_{DS} = +100V$ | | | 1.25 | | A |
| Diode Voltage Drop (Blocking Diode and Grass-Clipping Diode) | V_{DROP} | $I_{OUT_} = \pm 50mA$ | | | 1.7 | | V |
| LVOUT_ Diode Clamping Voltage | LV_{CLAMP} | $I_{LOAD} = 1mA$ | | -0.9 | | +1 | V |
| OUT_ Equivalent Small-Signal Shunt Capacitance | C_{LS} | 0.1V _{P-P} signal | | | 12 | | pF |
| OUT_ Equivalent Large-Signal Shunt Capacitance | C_{HS} | 200V _{P-P} signal | | | 80 | | pF |
| T/R Switch On Impedance | R_{ON} | $f = 5MHz$ | | | 6.5 | | Ω |
| T/R Switch Off Impedance | R_{OFF} | | | | 5 | | M Ω |
| LVOUT_ Output Offset | LV_{OFF} | LVOUT_, OUT_ unconnected, $V_{CC_} = +5V$, $V_{EE_} = -5V$ | | -40 | 0 | +40 | mV |
| THERMAL PROTECTION | | | | | | | |
| Thermal Warning | T_{THP} | Temperature rising | | | 125 | | $^\circ C$ |
| Thermal-Shutdown Threshold | T_{SDN} | Temperature rising | | | +150 | | $^\circ C$ |
| Thermal-Shutdown Hysteresis | T_{HYS} | | | | 20 | | $^\circ C$ |

AC Electrical Characteristics

($V_{DD}=+3V$, $V_{CC}=+5V$, ($V_{DD}=+3V$, $V_{CC}=+5V$, $V_{CCA}=+5V$, $V_{EE}=-5V$, $V_{EEA}=-5V$, $V_{PP}=+100V$, $V_{NN}=-100V$, V_{GN} connected to V_{NN} with $1\mu F$ capacitor, V_{GP} connected to V_{PP} with $1\mu F$ capacitor, $V_{CC0}=0V$, $V_{CC1}=0V$, $R_L=1k\Omega$, $C_L=220pF$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---------------|--|-----|------|-----|---------|
| Logic Input to Output Rise Propagation Delay | t_{PLH} | From 50% DINP_/DINN_ (transparent mode) to 10% OUT_ transition swing (Figure 2a) | | 10.8 | | ns |
| Logic Input to Output Fall Propagation Delay | t_{PHL} | From 50% DINP_/DINN_ (transparent mode) to 10% OUT_ transition swing (Figure 2a) | | 10.8 | | ns |
| Logic Input to Output Rise to GND Propagation Delay | t_{PL0} | From 50% DINP_/DINN_ (transparent mode) to 10% OUT_ transition swing (Figure 2a) | | 10.8 | | ns |
| Logic Input to Output Fall to GND Propagation Delay | t_{PH0} | From 50% DINP_/DINN_ (transparent mode) to 10% OUT_ transition swing (Figure 2a) | | 10.8 | | ns |
| OUT_ Fall Time (V_{PP} to V_{NN}) | t_{FPN} | Figure 2b | 20 | 24 | 30 | ns |
| OUT_ Rise Time (V_{NN} to V_{PP}) | t_{RNP} | Figure 2b | 20 | 24 | 30 | ns |
| OUT_ Rise Time (GND to V_{PP}) | t_{R0P} | Figure 2b | 7.5 | 10 | 13 | ns |
| OUT_ Fall Time (GND to V_{NN}) | t_{F0N} | Figure 2b | 7.5 | 10 | 13 | ns |
| OUT_ Rise Time (V_{NN} to GND) | t_{RN0} | 20% to 80% transition (Figure 2b) | 15 | | 27 | ns |
| OUT_ Fall Time (V_{PP} to GND) | t_{FP0} | 20% to 80% transition (Figure 2b) | 15 | | 27 | ns |
| T/R Switch Turn-On Time | t_{ONTRSW} | Figure 3 | | 0.65 | 1.1 | μs |
| T/R Switch Turn-Off Time | $t_{OFFTRSW}$ | Figure 3 (Note 6) | | 0.02 | 0.1 | μs |
| Setup Time from Receive to Transmit | t_{RXTX} | (Note 7) | 1 | | | μs |
| Output Enable Time (Shutdown Mode to Normal Operation) | t_{EN1} | | | | 100 | μs |
| Output Disable Time (Normal Operation to Shutdown Mode) | t_{DIS1} | | | | 10 | μs |
| Output Enable Time (Normal Operation to Sync Mode) | t_{EN2} | | | | 5 | μs |
| Output Disable Time (Sync Mode to Normal Operation) | t_{DIS2} | | | | 200 | ns |
| CLK Frequency | f_{CLK} | $V_{DD} = 2.5V$ | | | 200 | MHz |
| Input Setup Time (DINN_, DINP_) S. E. | t_{SETUP} | $V_{DD} = 2.5V$, Single-Ended Clock | 0.8 | | | ns |
| Input Hold Time (DINN_, DINP_) S. E. | t_{HOLD} | $V_{DD} = 2.5V$ | 1.4 | | | ns |

AC Electrical Characteristics (continued)

($V_{DD} = +3V$, $V_{CC} = +5V$, ($V_{DD} = +3V$, $V_{CC} = +5V$, $V_{CCA} = +5V$, $V_{EE} = -5V$, $V_{EEA} = -5V$, $V_{PP} = +100V$, $V_{NN} = -100V$, V_{GN} connected to V_{NN} with $1\mu F$ capacitor, V_{GP} connected to V_{PP} with $1\mu F$ capacitor, $V_{CC0} = 0V$, $V_{CC1} = 0V$, $R_L = 1k\Omega$, $C_L = 220pF$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------|--|-----|----------|-----|-------|
| Input Setup Time (DINN, DINP) Differential Clock | $T_{SETUP-D}$ | $V_{DD} = 2.5V$ - Differential Clock | 0.6 | | | ns |
| Input Hold Time (DINN, DINP) Differential Clock | T_{HOLD-D} | $V_{DD} = 2.5V$ - Differential Clock | 1.7 | | | ns |
| Second-Harmonic Distortion (Low Voltage) | THD2LV | $f_{OUT_} = 5MHz$, $V_{PP} = -V_{NN} = +5V$, square wave (all modes), $R_L = 100\Omega$, $C_L = 200pF$ | | -36 | | dBc |
| Second-Harmonic Distortion (High Voltage) | THD2HV | $f_{OUT_} = 5MHz$, $V_{PP} = -V_{NN} = +40V$ to $+105V$, square wave (all modes), $R_L = 100\Omega$, $C_L = 200pF$ | | -43 | | dBc |
| Pulse Cancellation | PC1 | $f_{OUT_} = 5MHz$, $V_{PP} = -V_{NN} = +80V$, 2 periods, all harmonics of the summed signed with respect to the carrier | | -43 | | dBc |
| Pulsar Bandwidth | BW | $V_{PP} = +60V$, $V_{NNA} = -60V$ (Figure 4) | | 30 | | MHz |
| RMS Output Jitter | t_j | $f_{OUT_} = 5MHz$, $V_{PPA} = -V_{NNA} = +5V$, $V_{PPB} = -V_{NNB} = +5V$, clocked mode (Figure 5) | | 5.4 | | ps |
| T/R Switch Harmonic Distortion | THDTRSW | $R_{LOAD} = 200\Omega$, $V_{SIGNAL} = 100mV_{P-P}$ | | -55 | | dB |
| T/R Switch Turn-On/Off Voltage Spike | V_{SPIKE} | $R_{LOAD} = 1k\Omega$ at both sides of T/R switch | | ± 20 | | mV |
| Crosstalk | CT | $f = 5MHz$, adjacent channels, $R_{LOUT_} = 50\Omega$ | | -53 | | dB |

Note 2: All devices are 100% production tested at $T_A = +85^\circ C$. Limits over the operating temperature range are guaranteed by design.

Note 3: CW Doppler: continuous wave, $f = 5MHz$, $V_{DD} = +3V$, $V_{CC_} = -V_{EE_} = +5V$, $V_{PP} = -V_{NN} = +5V$.

Note 4: B mode: $f = 5MHz$, PRF = 5kHz, 1 period, $V_{DD} = +3V$, $V_{CC_} = -V_{EE_} = +5V$, $V_{PP} = -V_{NN} = +105V$.

Note 5: T/R switch turn-off time is the time required to switch off the bias current of the T/R switch. The off-isolation is not guaranteed.

Note 6: Both the T/R switch and Damp are designed to be self-protected against the HV transmission. The part is not damaged even if the Transmit setup time is not respected. We recommend having at least $1\mu s$ setup time when moving from receive (INP = INN = 1 to transmit (INP = INN = 0). To further reduce the Transmit leakage through the TRSW a longer setup time is recommended (see T/R switch paragraph in the Detailed Description section). See [Timing Diagrams](#).

Timing Diagrams

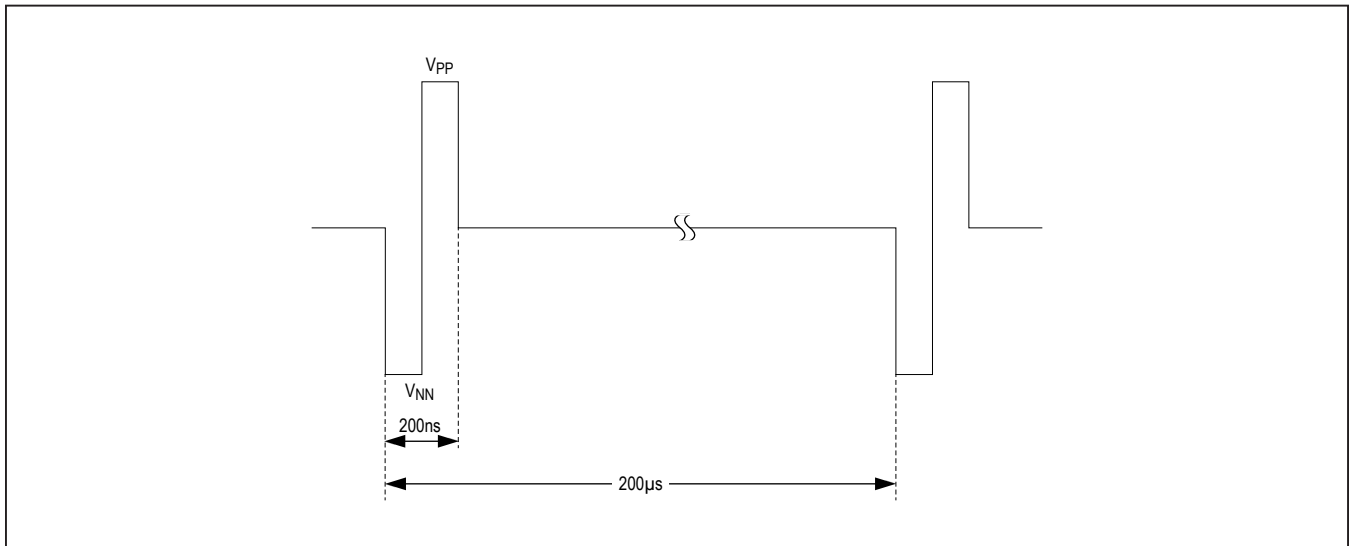


Figure 1. High-Voltage Burst Test

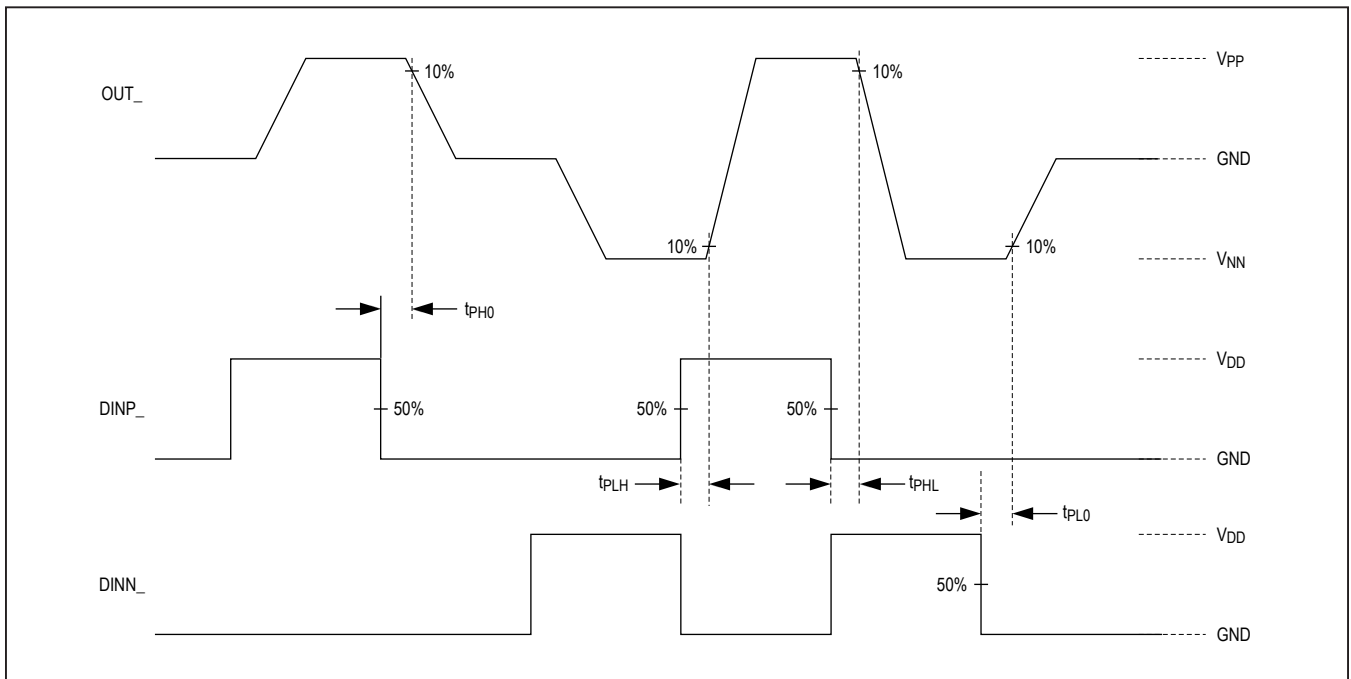


Figure 2a. Propagation Delay Timing

Timing Diagrams (continued)

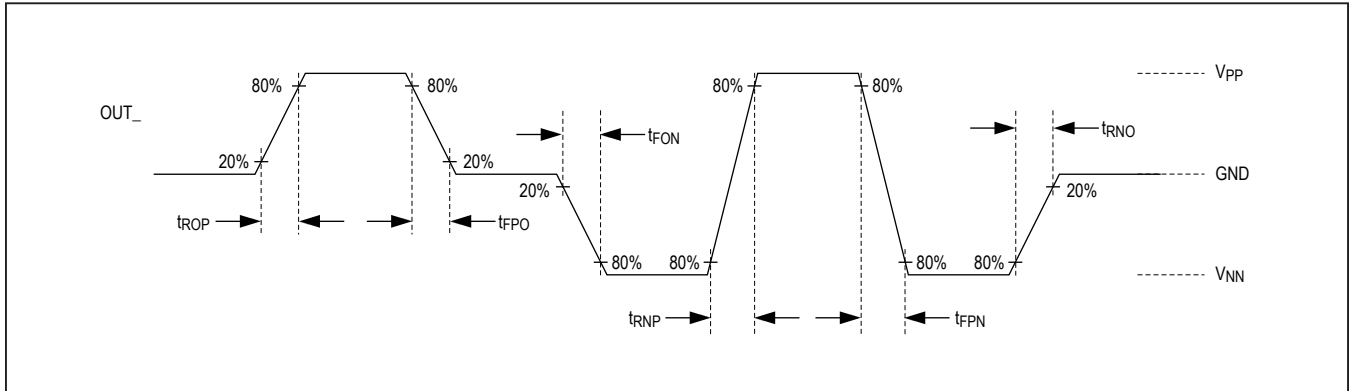


Figure 2b. Output Rise/Fall Timing

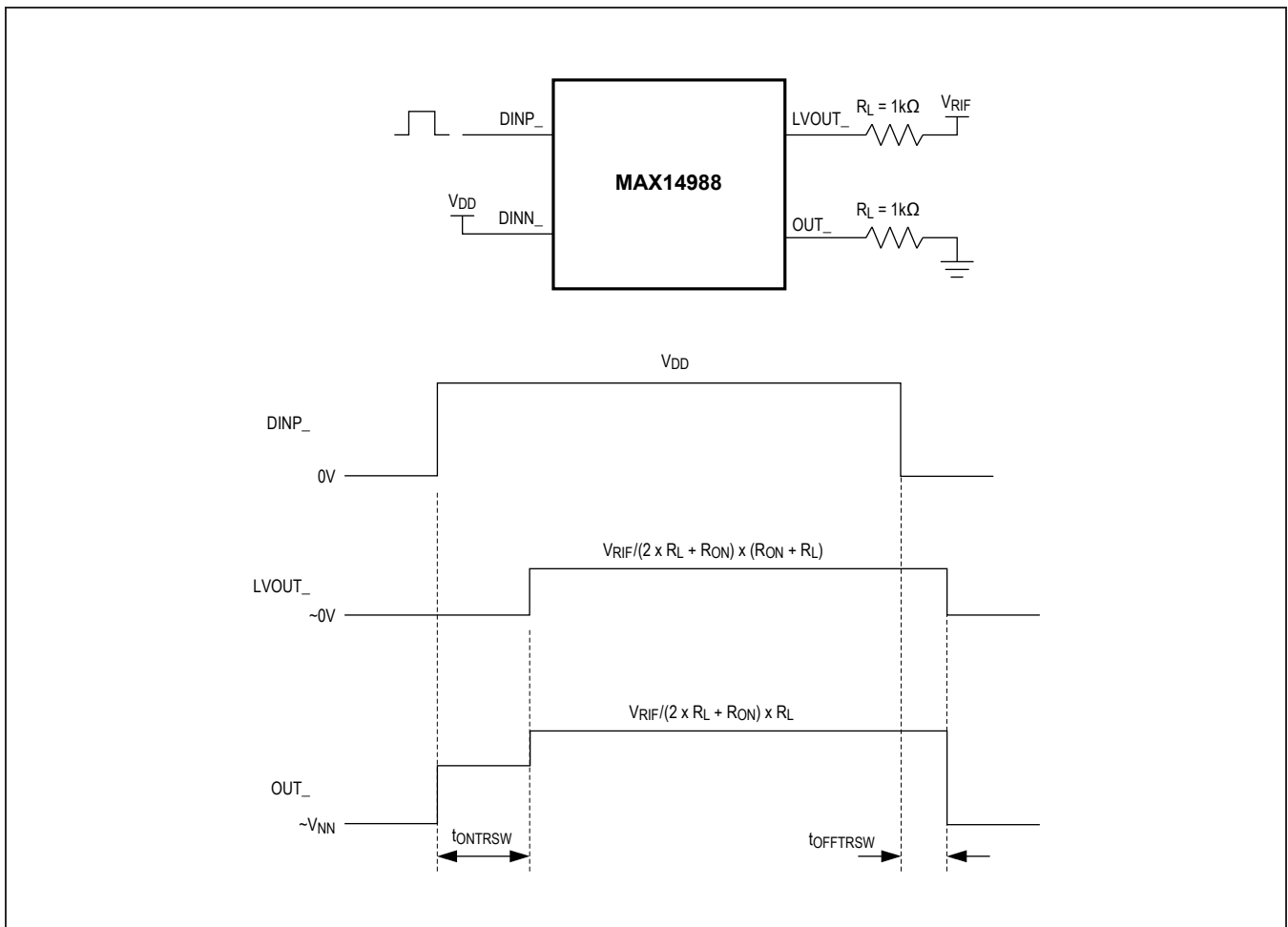


Figure 3. T/R Switch Turn-On/Off Time

Timing Diagrams (continued)

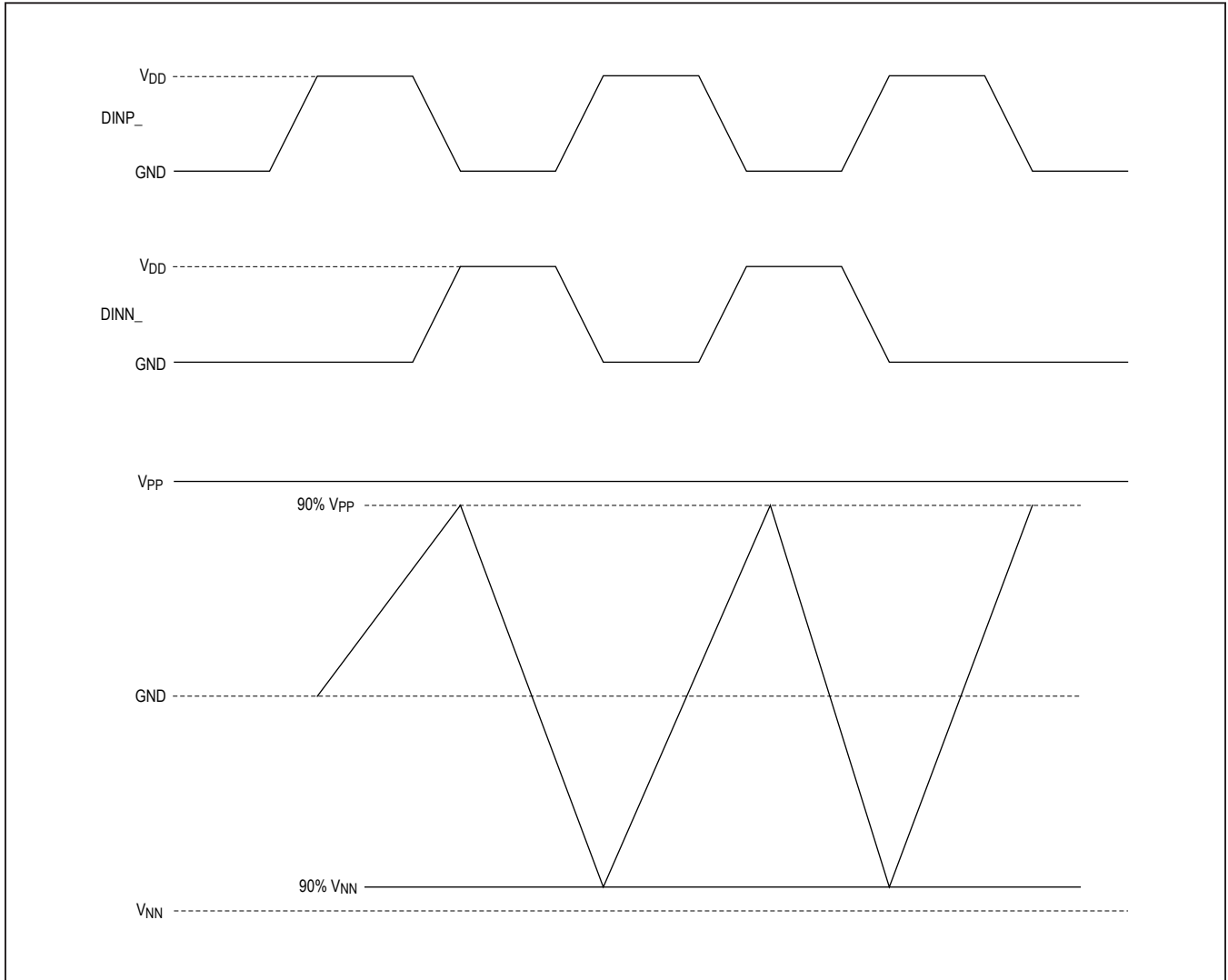


Figure 4. Bandwidth

Timing Diagrams (continued)

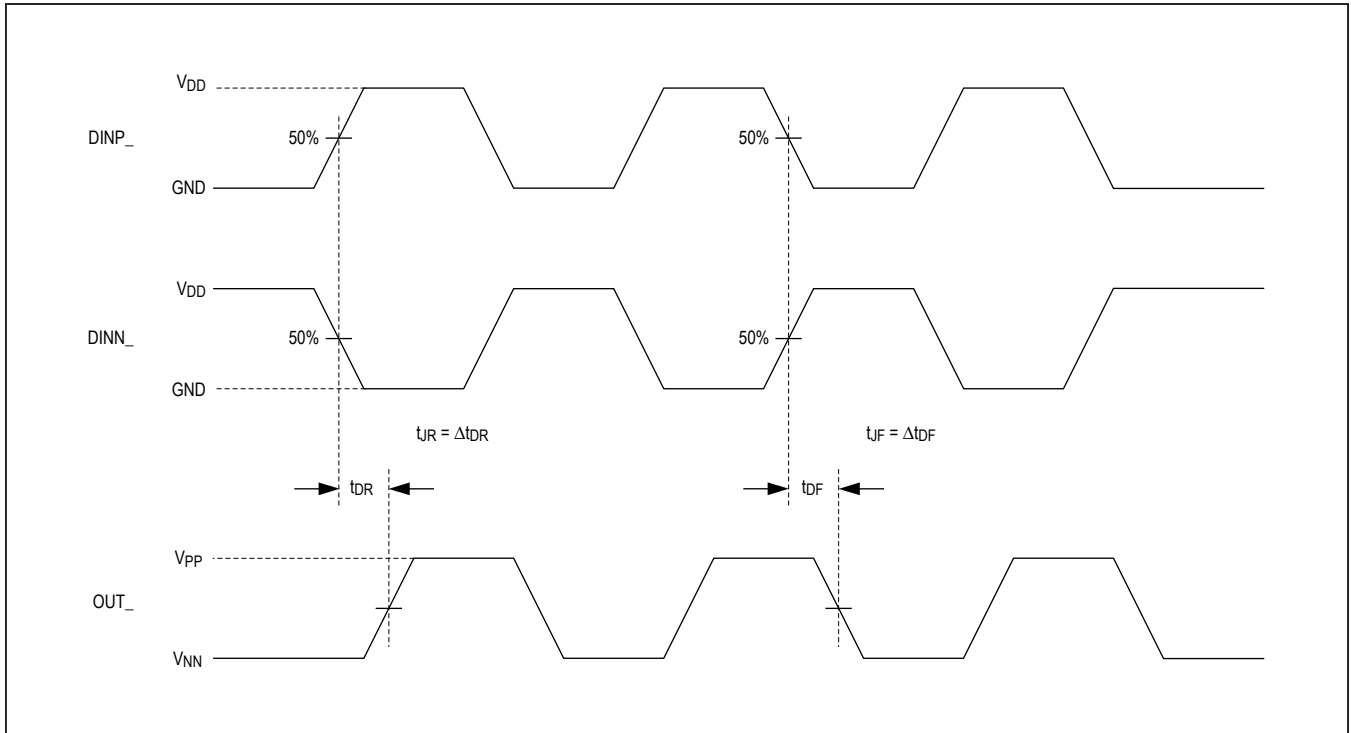
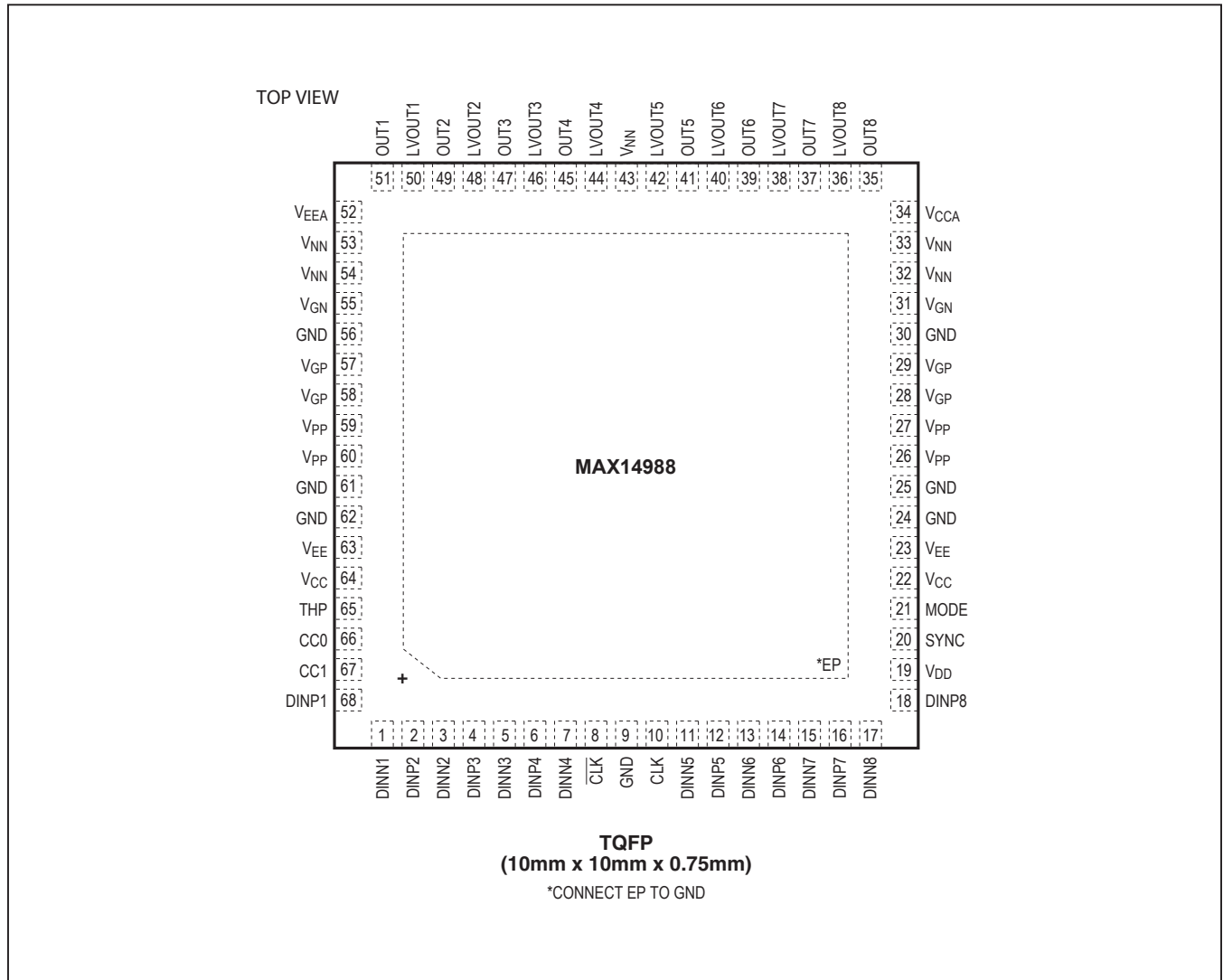


Figure 5. Jitter Timing

Pin Configuration



Pin Description

| PIN | NAME | FUNCTION |
|---------------------------------|-----------------|---|
| 50 | LVOOUT1 | Low-Voltage T/R Switch Output 1 |
| 48 | LVOOUT2 | Low-Voltage T/R Switch Output 2 |
| 46 | LVOOUT3 | Low-Voltage T/R Switch Output 3 |
| 44 | LVOOUT4 | Low-Voltage T/R Switch Output 4 |
| 65 | THP | Open-Drain Thermal-Protection Output. THP asserts and sinks a TBD mA current to GND when the junction temperature exceeds +125°C. |
| 20 | SYNC | CMOS Control Input. Drive SYNC high to enable clocked-input mode. Drive SYNC low to operate in transparent mode (see the Truth Tables section). |
| 10 | CLK | CMOS Control Input. Clock positive phase input. Data inputs are clocked in at the rising edge of CLK and CLK in differential clocked mode or at the rising edge of CLK in single-ended clocked mode. Clock maximum frequency is 160MHz. |
| 8 | CLK | CMOS Control Input. Clock negative phase input. Data inputs are clocked in at the edge of CLK and CLK in differential clocked mode. Clock maximum frequency is 160MHz. If CLK is connected to GND, the CLK input is a single-ended logic-level clock input. Otherwise, CLK and CLK are self-biased differential clock inputs. |
| 66 | CC0 | Current Control Input. Control current capability (see the Truth Tables section). |
| 67 | CC1 | Current Control Input. Control current capability (see the Truth Tables section). |
| 21 | MODE | Mode Control Input. Control operation mode (see the Truth Tables section). |
| 42 | LVOOUT5 | Low-Voltage T/R Switch Output 5 |
| 40 | LVOOUT6 | Low-Voltage T/R Switch Output 6 |
| 38 | LVOOUT7 | Low-Voltage T/R Switch Output 7 |
| 36 | LVOOUT8 | Low-Voltage T/R Switch Output 8 |
| 9, 24, 25, 30, 56, 61, 62 | GND | Ground |
| 19 | V _{DD} | Logic Supply Voltage. Bypass V _{DD} (both pins) to GND with a 0.1µF capacitor as close as possible to the device. |
| 12 | DINP5 | Digital Signal Positive Input 5 (see the <i>Truth Tables</i> section) |
| 11 | DINN5 | Digital Signal Negative Input 5 (see the <i>Truth Tables</i> section) |
| 14 | DINP6 | Digital Signal Positive Input 6 (see the <i>Truth Tables</i> section) |
| 13 | DINN6 | Digital Signal Negative Input 6 (see the <i>Truth Tables</i> section) |
| 16 | DINP7 | Digital Signal Positive Input 7 (see the <i>Truth Tables</i> section) |
| 15 | DINN7 | Digital Signal Negative Input 7 (see the <i>Truth Tables</i> section) |
| 18 | DINP8 | Digital Signal Positive Input 8 (see the <i>Truth Tables</i> section) |
| 17 | DINN8 | Digital Signal Negative Input 8 (see the <i>Truth Tables</i> section) |

Pin Description (continued)

| PIN | NAME | FUNCTION |
|-----------------------|------------------|--|
| 22, 64 | V _{CC} | V _{CC} Supply Voltage. Bypass V _{CC} (both pins) to GND with a 220nF capacitor as close as possible to the device. |
| 23, 63 | V _{EE} | V _{EE} Supply Voltage. Bypass V _{EE} (both pins) to GND with a 220nF capacitor as close as possible to the device. |
| 31, 55 | V _{GN} | Driver Voltage Supply Output. Connect a 1μF capacitor to V _{NN} as close as possible to the device. |
| 28, 29, 57, 58 | V _{GP} | Driver Voltage Supply Output. Connect a 1μF capacitor to V _{PP} as close as possible to the device. |
| 26, 27, 59, 60 | V _{PP} | High-Voltage Positive Supply Input. Bypass V _{PP} to GND with a 0.1μF capacitor as close as possible to the device. |
| 32, 33, 43, 53, 54 | V _{NN} | High-Voltage Negative Supply Input. Bypass V _{NN} to GND with a 0.1μF capacitor as close as possible to the device. |
| 35 | OUT8 | Pulser Output 8 |
| 37 | OUT7 | Pulser Output 7 |
| 39 | OUT6 | Pulser Output 6 |
| 41 | OUT5 | Pulser Output 5 |
| 45 | OUT4 | Pulser Output 4 |
| 47 | OUT3 | Pulser Output 3 |
| 49 | OUT2 | Pulser Output 2 |
| 51 | OUT1 | Pulser Output 1 |
| 7 | DINN4 | Digital Signal Negative Input 4 (see the <i>Truth Tables</i> section) |
| 6 | DINP4 | Digital Signal Positive Input 4 (see the <i>Truth Tables</i> section) |
| 5 | DINN3 | Digital Signal Negative Input 3 (see the <i>Truth Tables</i> section) |
| 4 | DINP3 | Digital Signal Positive Input 3 (see the <i>Truth Tables</i> section) |
| 3 | DINN2 | Digital Signal Negative Input 2 (see the <i>Truth Tables</i> section) |
| 2 | DINP2 | Digital Signal Positive Input 2 (see the <i>Truth Tables</i> section) |
| 1 | DINN1 | Digital Signal Negative Input 1 (see the <i>Truth Tables</i> section) |
| 68 | DINP1 | Digital Signal Positive Input 1 (see the <i>Truth Tables</i> section) |
| — | EP | Exposed Pad. Connect EP to GND. Not intended as an electrical connection point. |
| 34 | V _{CCA} | V _{CCA} Analog Supply Voltage. Bypass V _{CCA} to GND with a 220nF capacitor as close as possible to the device. |
| 52 | V _{EEA} | V _{EEA} Analog Supply Voltage. Bypass V _{EEA} to GND with a 220nF capacitor as close as possible to the device. |

Detailed Description

The MAX14988 octal three-level, high-voltage (HV) pulser device generates high-frequency, HV bipolar pulses (up to ±105V) from low-voltage control logic inputs for driving piezoelectric transducers in ultrasound systems. All 8 channels have embedded overvoltage-protection diodes and integrated active return-to-zero clamp. The device has embedded independent (floating) power supplies (FPSs) and level shifters that allow signal transmission without the need for external HV capacitors. The MAX14988 also features eight integrated transmit receive (T/R) switches.

In octal three-level pulser mode, each channel is controlled by two logic inputs (DINN_/DINP_) and the active return to zero features half the current driving of the pulser, 1.25A (typ).

The device can operate both in clocked and transparent mode. In clocked mode, data inputs can be synchronized with a clean differential or single-ended clock to reduce phase noise associated with FPGA output signals that are detrimental for Doppler analysis. In transparent mode, the synchronization feature is disabled and output reflects the data input after an 10.8ns delay. The device features adjustable maximum current (0.44A to 2.5A) to reduce power consumption when full current capability is not required.

The device features integrated grass-clipping diodes (with low parasitic capacitance) for receive (Rx) and transmit (Tx) isolations. The device features a damping circuit that can be activated as soon as the transmit burst is over. The damping circuit has an on-resistance of 200Ω. It fully discharges the pulser’s output internal node before the grass-clipping diodes.

Operation Mode

The devices have two operation modes: shutdown and octal three-level. Use the MODE input to select the operation mode.

Shutdown Mode

All channels are disabled, no transmission and reception is possible. This mode has the lowest power consumption. See [Table 1](#).

Octal Three-Level Mode

The devices operate in eight independent channels. Each channel can generate a three-level pulse. The high-side and low-side FET of each channel are capable of providing 2.5A current, while the clamp is capable of 1.25A current. See [Table 2](#).

Truth Tables

Table 1. Shutdown Mode (MODE = Low)

| INPUTS | | OUTPUTS | |
|--------|-------|----------------|---------------------------------|
| DINN_ | DINP_ | OUT_ | LVOUT_ |
| X | X | High impedance | High impedance (T/R switch off) |

X = Don't care

Table 2. Normal Operation Mode (MODE = High)

| INPUTS | | OUTPUTS | |
|--------|-------|----------------------------|-------------------------------|
| DINN_ | DINP_ | OUT_ | LVOUT_ |
| 0 | 0 | Clamp on (damp off) | T/R switch off (LVOUT_ = GND) |
| 1 | 0 | V _{NN} (damp off) | T/R switch off (LVOUT_ = GND) |
| 0 | 1 | V _{PP} (damp off) | T/R switch off (LVOUT_ = GND) |
| 1 | 1 | Clamp on (damp on) | T/R switch on |

0 = logic-low, 1 = logic-high

Current Capability Selection

The device features pulser current drive capability selection. Two control inputs (CC0, CC1) control the current drive capability (Table 3).

Sync Function

The device provides the ability to resynchronize all the data inputs by means of a clean clock signal. In ultrasound systems, the FPGA output signals are often affected by a high jitter. The jitter induces phase noise that is detrimental in Doppler analysis. The input clock can be either a differential signal or a single-ended signal running up to 200MHz. Data are clocked in on the rising edge of the CLK input (falling-edge of $\overline{\text{CLK}}$). Connect $\overline{\text{CLK}}$ to GND for single-ended operation. The sync feature can be enabled or disabled by the SYNC control input. Drive the SYNC input low to disable the synchronization function

Table 3. Current Drive Selection

| INPUTS | | PULSER OUTPUT CURRENT (typ) |
|--------|-----|-----------------------------|
| CC0 | CC1 | |
| 0 | 0 | 2.5A |
| 1 | 0 | 1.76A |
| 0 | 1 | 0.88A |
| 1 | 1 | 0.44A |

(no external clock signal). Drive the SYNC input high to enable the synchronization function (with an external clock signal). Figure 6 shows the simplified CLK and $\overline{\text{CLK}}$ inputs schematic.

T/R Switches

Each channel features a low-power T/R switch. The T/R switch recovery time after the transmission is less than 1 μ s. The T/R switches are controlled by the same pulser digital inputs (see the Truth Tables section). No dedicated input signals are required to activate/deactivate the T/R switches. The MAX14988 provides dedicated voltage supplies (V_{CCA} , V_{EEA}) which are used for T/R switches only. The integrated T/R switches do not require any special timings and can operate synchronously with the digital pulser. To minimize the leakage current during transmission, it's recommended to switch off the T/R switches 3 μ s before the beginning of the transmit burst.

Grass-Clipping Diodes

A pair of diodes in antiparallel configuration (referred to as grass-clipping diodes) is presented at each pulser's output. The diodes' reverse capacitance is extremely low, allowing a perfect isolation between the receive path and the actual pulser's output stage.

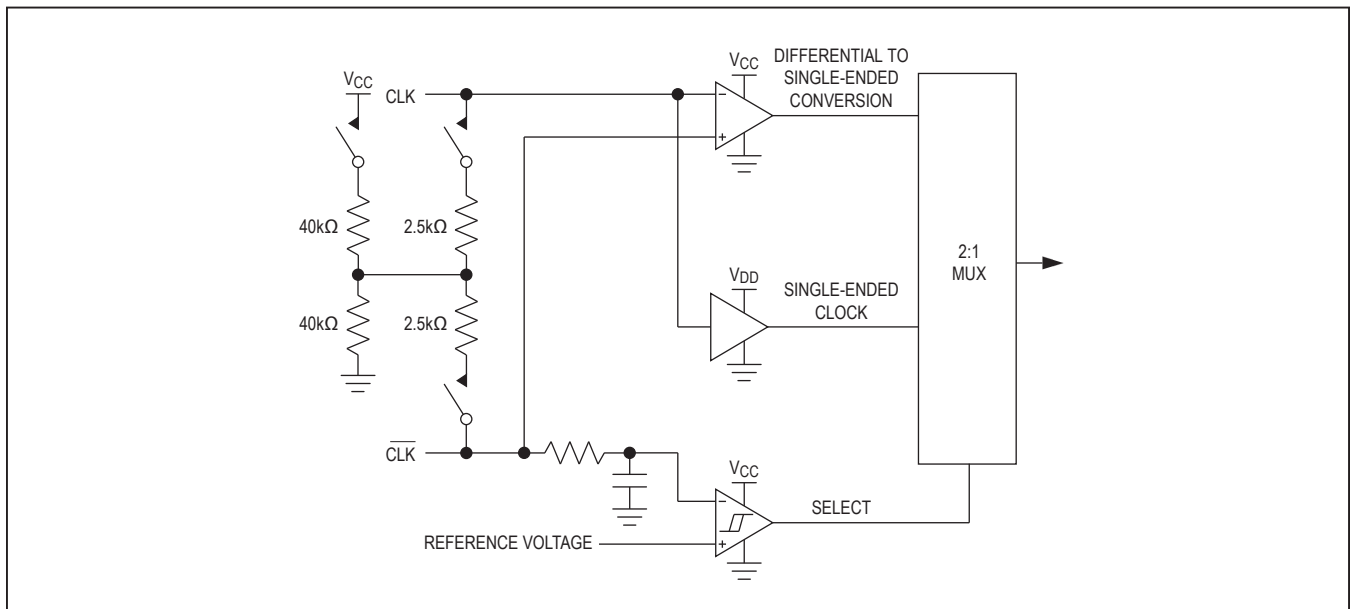


Figure 6. Simplified CLK and $\overline{\text{CLK}}$ Inputs Schematic

Active Damp Circuit

An active damp circuit is integrated between the internal pulser output node (before grass-clipping diodes) and GND. The purpose of this circuit is to fully discharge the pulser output internal node so that the node is not left in high-impedance condition as soon as the transmit burst is over. This results in two main advantages:

- 1) The grass-clipping isolation is more effective.
- 2) Suppression of any low-frequency oscillation of a node that could be detrimental for Doppler mode performances.

The integrated damp circuit is self-protected. To reduce power consumption, it is recommended to switch off the damp circuit as least 1 μ s before the beginning of the transmit burst.

Thermal Warning Outputs

The devices feature an open-drain thermal-protection output (THP). When the internal junction temperature exceeds +125°C, THP asserts. When the internal junction temperature exceeds +150°C, the device automatically enters shutdown mode. The devices reenter normal operation and the THP deasserts when the die temperature drops below +120°C.

Power Sequencing

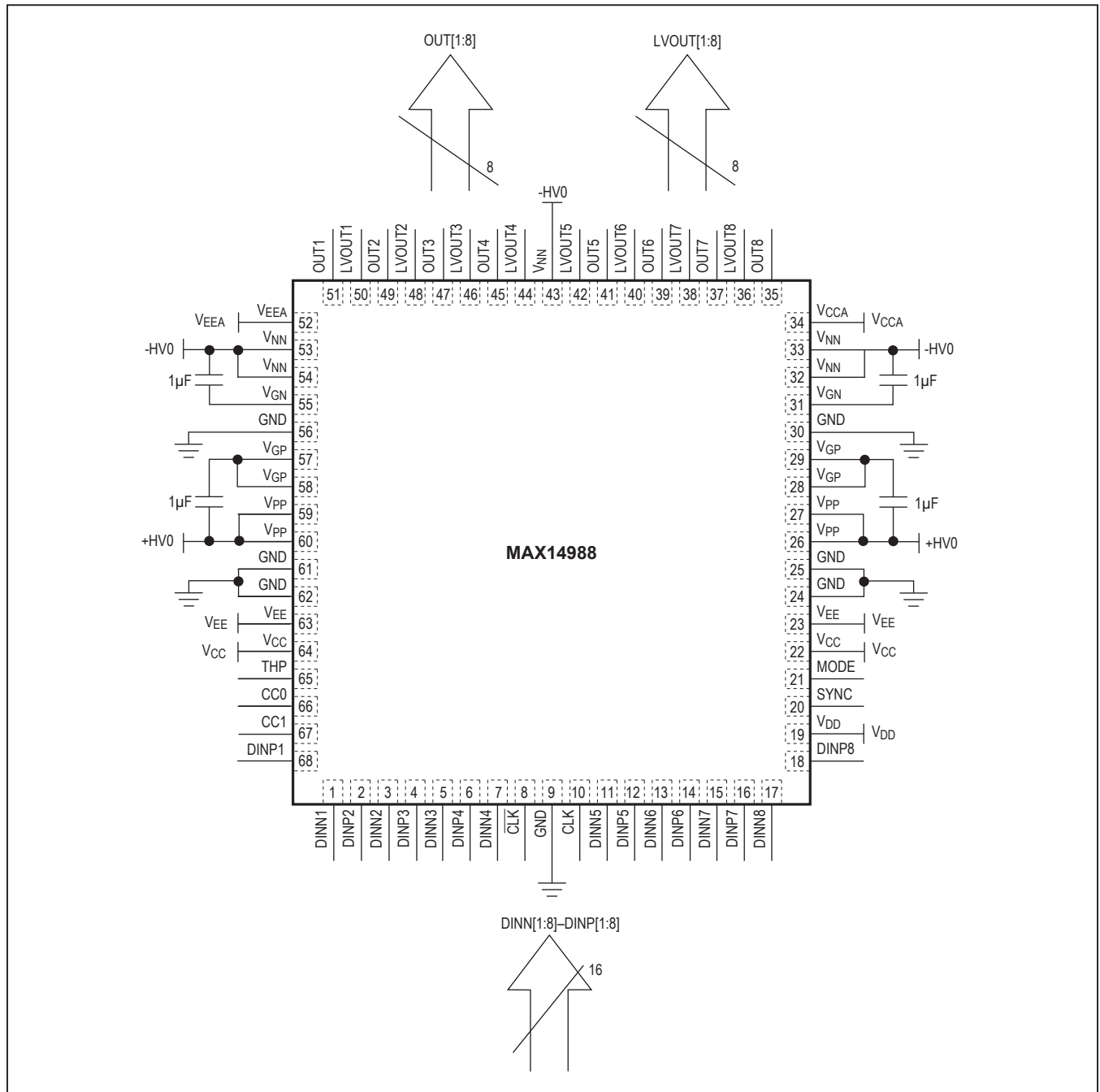
The device does not require any power-up/power-down sequence. However, the MODE pin must be forced to GND or leave unconnected during power-up/power-down sequence to prevent the transmitter to be turned on inadvertently.

Applications Information**Exposed Pad and Layout Concerns**

The device provides an exposed pad (EP) underneath the TQFN package for improved thermal performance. Connect EP to GND externally and do not run traces under the package to avoid possible short circuits. To aid heat dissipation, connect EP to a similarly sized pad on the component side of the PCB. This pad should be connected through to the solder-side copper by several plated holes to a large heat-spreading copper area to conduct heat away from the device.

The device's high-speed pulser requires low-inductance bypass capacitors to their supply inputs. High-speed PCB trace design practices are recommended. Pay particular attention to minimize trace lengths and use sufficient trace width to reduce inductance. Use of surface-mount components is recommended.

Typical Application Circuit



MAX14988

2.5A Octal Three-Level Digital Pulsers with TR Switches

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|--------------|----------------|-------------|
| MAX14988ETK+ | -40°C to +85°C | 68 TQFN-EP* |

+Denotes a lead(Pb)-free/RoHS-compliant package.
*EP = Exposed pad.

Chip Information

PROCESS: BICMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.analog.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 68 TQFN-EP | T6800+3 | 21-0142 | 90-0100 |

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|-----------------|---------------|
| 0 | 12/14 | Initial release | — |



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