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2.5A Octal Five-Level Digital Pulsers

MAX14987

General Description

The MAX14987 octal five-level, high-volage (HV) pulser device generates high-frequency HV bipolar pulses (up to ±105V) from low-voltage control logic inputs for driving piezoelectric transducers in ultrasound systems. All eight channels have embedded overvoltage-protection diodes and an integrated active return-to-zero clamp. The device has embedded independent (floating) power supplies (FPS) and level shifters that allow signal transmission without the need for external HV capacitors. The device also features eight integrated transmit/receive (T/R) switches.

The device features two modes of operation: shutdown mode and octal five-level mode pulsing (with integrated active return-to-zero clamp). In octal five-level mode pulsing, each channel is controlled by three logic inputs (DINN_/DINP_/SEL_). Each channel features two HV half-bridges operating from independent pairs of voltage supplies (V_{PPA}, V_{NNA} and V_{PPB}, V_{NNB}) and sharing the same output. The half-bridge operating from V_{PPA}, V_{NNA} is named HB1 while the half-bridge operating from V_{PPB}, V_{NNB} is named HB2. The voltage rating is the same for the two half-bridges. They can both operate from 0 to ±105V.

HB1 is sized to provide a maximum driving current in excess of ±2.5A and is optimized in terms of Bandwidth and PWM performances.

HB2 is sized to provide a maximum driving current of ±1.6A and is normally intended to be used in Doppler modes (CWD, CFM, PWD). The driving current of HB2 can be programmed at 1.6A, 1.1A, 0.5A, and 0.3A. This allows reducing the power dissipation in particular for CWD modality. HB2 exhibits excellent jitter (< 6ps) and phase noise performances (156dBc @1kHz offset) in CWD modality.

The return-to-zero (clamp) driving current can also be programmed either at 1.25A or 2.5A by means of a dedicated CMOS input (RTZ).

The device is available in a 228-bump (10mm x 16mm) BGA package and are specified over the -40°C to +85°C extended temperature range.

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Benefits and Features

- Saves Space (Optimized for High-Channel-Count Systems/Portable Systems)
  - High Density
    - 8 Channels (Five-Level Operation)
  - Integrated Low-Power T/R Switches
  - DirectDrive® Architecture Eliminates External High-Voltage Capacitor
  - No External Floating Power Supply (FPS) Required
- High Performance (Designed to Enhance Image Quality)
  - Excellent -40dBc (typ) THD for Second Harmonic at 5MHz
  - High Bandwidth and Ultra-Fast Rise/Fall Edges Enable High-Order PWM Burst Shaping
  - Sync Function Eliminates Effects of FPGA Jitter and Improves Performance in Doppler Mode
  - Low Propagation Delay 11 (typ)
  - Strong Active Return to Zero
- Saves Power
  - Low Quiescent Power Dissipation (21mW/Channel in Octal Mode)
  - Programmable Current Capability
  - Shutdown Mode

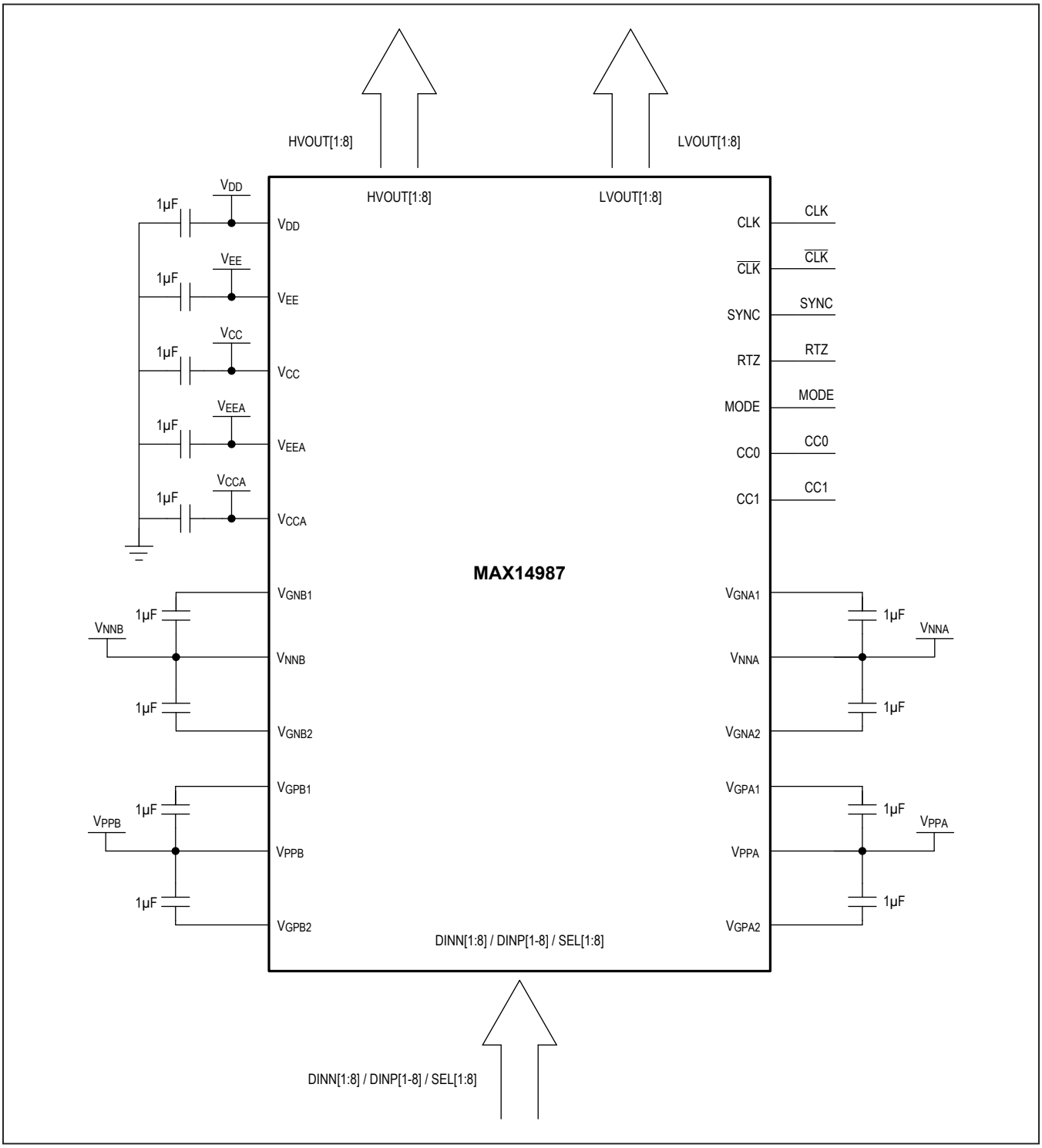
Applications

- Ultrasound Medical Imaging
- Industrial Flaw Detection
- Piezoelectric Drivers
- Test Equipment

***Ordering Information* and *Functional Diagram* appears at end of data sheet.**

19-7484; Rev 2; 4/16

Typical Application Circuit



Absolute Maximum Ratings

V_{DD} Logic Supply Voltage.....-0.3V to +5.6V
V_{CC}, V_{CCA} Supply Voltage.....-0.3V to +5.6V
V_{EE}, V_{EEA} Supply Voltage.....-5.6V to +0.3V
V_{NNA}, V_{NNB} Negative High Supply Voltage.....-110V to +0.3V
V_{PPA}, V_{PPB} Positive High Supply Voltage.....-0.3V to +110V
$V_{PP\_}$ - $V_{NN\_}$ Differential High Voltage Supply..... 0 to +220V
HVOUT Output Voltage Range..... $V_{NN\_}$ - 0.3V to $V_{PP\_}$ + 0.3V
LVOUT_ Output Voltage Range.....-1V to +1V
DINP_, DINN_, SEL_, MODE, CC0, CC1, RTZ, SYNC, THP Input Voltage Range .....-0.3V to +5.6V
CLK, $\overline{CLK}$, Voltage Range.....-0.3V to (V_{CC} + 0.3V)
V_{GPA1}, V_{GPA2} Driver Supply Voltage Supply max[V_{PPA} - 5.6V, V_{EE} + 0.6V] to V_{PPA} + 0.3V
V_{GPB1}, V_{GPB2} Driver Supply Voltage Supply .....max [V_{PPB} - 5.6V, V_{EE} + 0.6V] to V_{PPB} + 0.3V
V_{GNA1}, V_{GNA2} Driver Supply Voltage Supply .....V_{NNA} - 0.3V to min[V_{CC} + 0.6V, V_{NNA} + 5.6V]
V_{GNB1}, V_{GNB2} Driver Supply Voltage Supply .....V_{NNB} - 0.3V to min[V_{CC} + 0.6V, V_{NNB} + 5.6V]
Continuous Power Dissipation (T_A = +70°C)
BGA (derate 89mW/°C above +70°C).....7162mW
Operating Temperature Range..... -40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

BGA
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....11.2°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2.7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.analog.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{DD} = +3V, V_{CC} = +5V, V_{CCA} = +5V, V_{EE} = -5V, V_{EEA} = -5V, V_{PPA} = V_{PPB} = -V_{NNA}= -V_{NNB} = 100V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES (V_{DD}, V_{CC}, V_{EE}, V_{PP}, $V_{NN\_}$)						
Logic Supply Voltage	V_{DD}		+1.7	+3	+5.25	V
Positive Drive Supply Voltage	$V_{CC\_}$		+4.9	+5	+5.1	V
Negative Drive Supply Voltage	$V_{EE\_}$		-5.1	-5	-4.9	V
High-Side Supply Voltage	$V_{PP\_}$		0		+105	V
Low-Side Supply Voltage	$V_{NN\_}$		-105		0	V
LOGIC INPUTS/OUTPUTS (DINN_, DINP_, SEL_, THP MODE, SYNC, CC_, RTZ)						
Low-Level Input Threshold	V_{IL}				0.2 x V_{DD}	V
High-Level Input Threshold	V_{IH}		0.8 x V_{DD}			V
Differential Input Resistance Between DINP_ and DINN_	RIND		70	100	170	kΩ
Pulldown Input Resistance Pins MODE, SYNC, CC0, CC1, SEL_, RTZ	RPD		70	100	170	kΩ
Logic Input Capacitance	C_{IN}			4		pF
Logic Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}	+1		-1	µA
THP Low-Level Output Voltage	V_{OL}	Pullup resistor to V_{DD} (R_{PULLUP} = 1kΩ)			0.1 x V_{DD}	V

DC Electrical Characteristics (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{CCA} = +5V, V_{EE} = -5V, V_{EEA} = -5V, V_{PPA} = V_{PPB} = $-V_{NNA}$= $-V_{NNB}$ = 100V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUTS (CLK, $\overline{CLK}$)—DIFFERENTIAL MODE						
Differential Clock Input Voltage Range	V_{CLKD}		0.4		2	V_{P-P}
Common-Mode Voltage	V_{CLKCM}		$V_{CC}/2$ + 0.45		$V_{CC}/2$ - 0.45	V
Input Resistance	R_{CLK}, $R_{\overline{CLK}}$	Differential		7		kΩ
		Common mode		22		kΩ
Input Capacitance	C_{CLK}, $C_{\overline{CLK}}$	Capacitance to GND (each input)		4		pF
CLOCK INPUTS (CLK, BCLK)—SINGLE-ENDED MODE (V_{BCLK} < 0.1V)						
Low-Level Input	V_{IL}	CLK			0.2 x V_{DD}	V
High-Level Input	V_{IH}	CLK	0.8 x V_{DD}			V
Single-Ended Mode Selection Threshold Low	V_{IL}	BCLK			0.1	V
Single-Ended Mode Selection Threshold High	V_{IH}	BCLK	1			V
Input Capacitance (CLK)	C_{CLK}			4		pF
Logic Input Leakage (CLK)	I_{CLK}	V_{CLK} = 0V or V_{DD}	-1		+1	µA
Pullup Current ($\overline{CLK}$)	$I_{\overline{CLK}}$	$V_{\overline{CLK}}$ = 0V		120	180	µA
SUPPLY CURRENT—SHUTDOWN MODE (MODE = LOW)						
V_{DD} Supply Current	I_{DD}	All inputs connected to GND or V_{DD}			20	µA
V_{CC} Supply Current	I_{CC}	All inputs connected to GND or V_{DD}			36	µA
V_{CCA} Supply Current	I_{CCA}	All inputs connected to GND or V_{DD}			4	µA
V_{EE} Supply Current	I_{EE}	All inputs connected to GND or V_{DD}			58	µA
V_{EEA} Supply Current	I_{EEA}	All inputs connected to GND or V_{DD}			4	µA
V_{PP} Supply Current	I_{PP}	All inputs connected to GND or V_{DD}		0	24	µA
V_{NN} Supply Current	I_{NN}	All inputs connected to GND or V_{DD}		0	24	µA
SUPPLY CURRENT—NORMAL OPERATION MODE, NO LOAD (MODE = HIGH)						
V_{DD} Supply Current (Quiescent Mode)	I_{DDQ}	All inputs connected to GND or V_{DD}		13	20	µA
V_{EE} Supply Current (Quiescent Mode)	I_{EEQ}			0.6	0.9	mA
V_{EEA} Supply Current (Quiescent Mode)	I_{EEAQ}	DINN_ = DINP_ = GND		1		µA
		DINN_ = DINP_ = V_{DD}		8.1	12	

DC Electrical Characteristics (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{CCA} = +5V, V_{EE} = -5V, V_{EEA} = -5V, V_{PPA} = V_{PPB} = -V_{NNA}= -V_{NNB} = 100V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Current (Quiescent Mode)	I_{CCQ}			0.9	1.2	mA
V_{CCA} Supply Current (Quiescent Mode)	I_{CCAQ}	DINN_ = DINP_ = GND		1		µA
		DINN_ = DINP_ = V_{DD}		8.7	13	
$V_{CC\_}$ Supply Current Increase in Clocked Mode	$\Delta I_{CC\_}$	Differential clock mode		3.4	4.8	mA
$V_{NN\_I(VNNA) + I(VNNB)}$ Total Supply Current (Quiescent Mode)	$I_{NNQ\_}$	All inputs connected to GND or V_{DD}		500	700	µA
$V_{PP\_I(VPPA) + I(VPPB)}$ Total Supply Current (Quiescent Mode)	$I_{PPQ\_}$	All inputs connected to GND or V_{DD}		470	700	µA
Total Power Dissipation per Channel (Quiescent Mode)	P_{PDIS1}	T/R switch off, damp off (transparent mode)		13		mW
	P_{PDIS2}	DINN_ = DINP_ = V_{DD} (transparent mode)		21		
V_{DD} Supply Current	I_{DD1}	CW Doppler (Note 4)		1.8	2.6	mA
	I_{DD2}	B mode (Note 5), (Figure 1a)		15	40	µA
V_{EE} Supply Current	I_{EE1}	8 channels switching, CW Doppler (Note 4)		38	50	mA
	I_{EE2}	8 channels switching, B mode (Note 5) (Figure 1a)		1	2	
V_{EEA} Supply Current	I_{EEA1}	8 channels switching, CW Doppler (Note 4)		2		µA
	I_{EEA2}	8 channels switching, B mode (Note 5) (Figure 1a)		8.1		
V_{CC} Supply Current	I_{CC1}	8 channels switching, CW Doppler (Note 4)		30	45	mA
	I_{CC2}	8 channels switching, B mode (Note 5) (Figure 1a)		1	2	
V_{CCA} Supply Current	I_{CCA1}	8 channels switching, CW Doppler (Note 4)		2		µA
	I_{CCA2}	8 channels switching, B mode (Note 5) (Figure 1a)		8.7		
V_{NN} Total Supply Current I(VNNA) + I(VNNB)	I_{NN1}	8 channels switching, CW Doppler, (Note 4)		150	190	mA
	I_{NN2}	8 channels switching, B mode (Figure 1a), (Note 5)		4	7	

DC Electrical Characteristics (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{CCA} = +5V, V_{EE} = -5V, V_{EEA} = -5V, V_{PPA} = V_{PPB} = -V_{NNA}= -V_{NNB} = 100V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{PP} Total Supply Current I(VPPA) + I(VPPB)	I_{PP1}	8 channels switching, CW Doppler, (Note 4)			166	210	mA
	I_{PP2}	8 channels switching, B mode (Figure 1a), (Note 5)			2.6	5	
Power Dissipation per Channel	PD_{CW}	1 channel switching, CW Doppler (Note 4)			240		mW
	PD_{PW}	1 channel switching, B mode (Note 5), (Figure 1a)			94		
OUTPUT STAGE							
V_{NNA} Connected Low-side Output Impedance	R_{OLS}	$I_{OUT\_}$ = -50mA			8		Ω
V_{PPA} Connected Low-side Output Impedance	R_{OHS}	$I_{OUT\_}$ = +50mA			8		Ω
V_{NNB} Connected Low-Side Output Impedance	R_{OLS}	$I_{OUT\_}$ = -50mA	CC0 = low, CC1 = low		12		Ω
			CC0 = high, CC1 = low		16		
			CC0 = low, CC1 = high		28		
			CC0 = high, CC1 = high		59	120	
V_{PPB} Connected High-Side Output Impedance	R_{OHS}	$I_{OUT\_}$ = +50mA	CC0 = low, CC1 = low		12		Ω
			CC0 = high, CC1 = low		16		
			CC0 = low, CC1 = high		28		
			CC0 = high, CC1 = high		59	120	
Clamp nFET Output Impedance	R_{ONG}	$I_{OUT\_}$ = -50mA,	RTZ = 0		8		Ω
			RTZ = 1		12		
Clamp pFET Output Impedance	R_{OPG}	$I_{OUT\_}$ = +50mA	RTZ = 0		8		Ω
			RTZ = 1		12		
Active Damp Output Impedance	R_{DAMP}	Before grass-clipping diode			100		Ω
V_{NNA} Connected Low-side Output Current	I_{OLS}	V_{DS} = +100V			2.5		A
V_{PPA} Connected Low-side Output Current	I_{OHS}	V_{DS} = +100V			2.5		A

DC Electrical Characteristics (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{CCA} = +5V, V_{EE} = -5V, V_{EEA} = -5V, V_{PPA} = V_{PPB} = -V_{NNA}= -V_{NNB} = 100V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{NNB} Connected Low-Side Output Current	I_{OLS}	V_{DS} = +100V	CC0 = low, CC1 = low		1.6		A
			CC0 = high, CC1 = low		1.1		
			CC0 = low, CC1 = high		0.5		
			CC0 = high, CC1 = high		0.3		
V_{PPB} Connected High-Side Output Current	I_{OHS}	V_{DS} = +100V	CC0 = low, CC1 = low		1.6		A
			CC0 = high, CC1 = low		1.1		
			CC0 = low, CC1 = high		0.5		
			CC0 = high, CC1 = high		0.3		
GND-Connected nFET Output Current	I_{ONG}	V_{DS} = +100V	RTZ = 0		2.5		A
			RTZ = 1		1.25		
GND-Connected pFET Output Current	I_{OPG}	V_{DS} = +100V	RTZ = 0		2.5		A
			RTZ = 1		1.25		
Diode Voltage Drop (Blocking Diode and Grass-Clipping Diode)	V_{DROP}	$I_{OUT\_}$ = ±50mA			1.7		V
LVOUT_Diode Clamping Voltage	LV_{CLAMP}	I_{LOAD} = 1mA		-0.9		+1	V
OUT_ Equivalent Small-Signal Shunt Capacitance	C_{LS}	0.1V_{P-P} signal			15		pF
OUT_ Equivalent Large-Signal Shunt Capacitance	C_{HS}	200V_{P-P} signal			80		pF
T/R Switch On Impedance	R_{ON}	f = 5MHz			8		Ω
T/R Switch Off Impedance	R_{OFF}	f = 5MHz			5		MΩ
LVOUT_ Output Offset	LV_{OFF}	LVOUT_, OUT_ unconnected		-40		+40	mV
THERMAL PROTECTION							
Thermal-Shutdown Threshold	T_{SDN}	Temperature rising			+150		°C
Thermal-Shutdown Hysteresis	T_{HYS}				20		°C

AC Electrical Characteristics

(V_{DD} = +3V, $V_{CC\_}$ = +5V, $V_{EE\_}$ = -5V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, CC0 = CC1 = low, RTZ = low, R_L = 1kΩ, C_L = 220pF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HB1 PROPAGATION DELAY TIMING – SEL_ = LOW, FIGURE 2A						
Logic Input to HB1 Output Rise Propagation Delay	t_{PLH1}	From DINP_/DINN_ at 50% (or clock rising edge in clocked mode) to output at 0.9 x V_{NNA}		11		ns
Logic Input to HB1 Output Fall Propagation Delay	t_{PHL1}	From DINP_/DINN_ at 50% (or clock rising edge in clocked mode) to output at 0.9 x V_{PPA}		11		ns
Logic Input to HB1 Output Rise to GND Propagation Delay	t_{PL01}	From DINP_/DINN_ at 50% (or clock rising edge in clocked mode) to output at 0.9 x V_{NNA}		11		ns
Logic Input to HB1 Output Fall to GND Propagation Delay	t_{PH01}	From DINP_/DINN_ at 50% (or clock rising edge in clocked mode) to output at 0.9 x V_{PPA}		11		ns
Logic Input to HB1 Output Rise from GND Propagation Delay	t_{P0H1}	From DINP_/DINN_ at 50% (or clock rising edge in clocked mode) to output at 0.1 x V_{PPA}		11		ns
Logic Input to HB1 Output Fall from GND Propagation Delay	t_{P0L1}	From DINP_/DINN_ at 50% (or clock rising edge in clocked mode) to output at 0.1 x V_{NNA}		11		ns
HB1 RISE AND FALL TIMING – SEL_ = LOW, FIGURE 2B						
HVOUT_ Fall Time (V_{PPA} to V_{NNA})	t_{FPNA}	From 0.8 x V_{PPA} to 0.8 x V_{NNA}		22	38	ns
HVOUT_ Rise Time (V_{NNA} to V_{PPA})	t_{RNPA}	From 0.8 x V_{NNA} to 0.8 x V_{PPA}		22	38	ns
HVOUT_ Rise Time (GND to V_{PPA})	t_{R0PA}	From 0.1 x V_{PPA} to 0.9 x V_{PPA}		8	14	ns
HVOUT_ Fall Time (GND to V_{NNA})	t_{F0NA}	From 0.1 x V_{NNA} to 0.9 x V_{NNA}		8	14	ns
HVOUT_ Fall Time (V_{NNA} to GND)	t_{RN0A}	From 0.9 x V_{NNA} to 0.1 x V_{NNA}		11	18	ns
HVOUT_ Fall Time (V_{PPA} to GND)	t_{FP0A}	From 0.9 x V_{PPA} to 0.1 x V_{PPA}		12	23	ns
Slew Rate 220pF	SR1	C_L = 220pF, $V_{PP\_}$ = -$V_{NN\_}$ = 60V		6.4		V/ns
Slew Rate 70pF in Parallel with 100Ω	SR2	C_L = 220pF, RL = 70Ω, $V_{PP\_}$ = -$V_{NN\_}$ = 60V		10		V/ns

AC Electrical Characteristics (continued)

(V_{DD} = +3V, $V_{CC\_}$ = +5V, $V_{EE\_}$ = -5V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, CC0 = CC1 = low, RTZ = low, R_L = 1kΩ, C_L = 220pF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HB2 PROPAGATION DELAY TIMING – SEL_ = HIGH, FIGURE 2A						
Logic Input to HB2 Output Rise Propagation Delay	t_{PLH2}	From DINP_/DINN_ at 50% (or clock rising-edge in clocked mode) to output at 0.9 x V_{NNB}		13		ns
Logic Input to HB2 Output Fall Propagation Delay	t_{PHL2}	From DINP_/DINN_ at 50% (or clock rising-edge in clocked mode) to output at 0.9 x V_{PPB}		13		ns
Logic Input to HB2 Output Rise to GND Propagation Delay	t_{PL02}	From DINP_/DINN_ at 50% (or clock rising-edge in clocked mode) to output at 0.9 x V_{NNB}		12		ns
Logic Input to HB2 Output Fall to GND Propagation Delay	t_{PH02}	From DINP_/DINN_ at 50% (or clock rising-edge in clocked mode) to output at 0.9 x V_{PPB}		11		ns
Logic Input to HB2 Output Rise from GND to V_{PPB} Propagation Delay	t_{P0H2}	From DINP_/DINN_ at 50% (or clock rising-edge in clocked mode) to output at 0.1 x V_{PPB}		12		ns
Logic Input to HB2 Output Fall from GND to V_{NNB} Propagation Delay	t_{P0L2}	From DINP_/DINN_ at 50% (or clock rising-edge in clocked mode) to output at 0.1 x V_{NNB}		12		ns
HB2 RISE AND FALL TIMING – SEL_ = HIGH, FIGURE 2B						
HVOUT_ Fall Time (V_{PPB} to V_{NNB})	t_{FPNB}	From 0.8 x V_{PPB} to 0.8 x V_{NNB}			65	ns
HVOUT_ Rise Time (V_{NNB} to V_{PPB})	t_{RNPB}	From 0.8 x V_{NNB} to 0.8 x V_{PPB}			60	ns
HVOUT_ Rise Time (GND to V_{PPB})	t_{R0PB}	From 0.1 x V_{PPB} to 0.9 x V_{PPB}			29	ns
HVOUT_ Fall Time (GND to V_{NNB})	t_{F0NB}	From 0.1 x V_{NNB} to 0.9 x V_{NNB}			29	ns
HVOUT_ Fall Time (V_{NNB} to GND)	t_{RN0B}	From 0.9 x V_{NNB} to 0.1 x V_{NNB}			20	ns
HVOUT_ Fall Time (V_{PPB} to GND)	t_{FP0B}	From 0.9 x V_{PPB} to 0.1 x V_{PPB}			20	ns
T/R Switch Turn-On Time	t_{ONTRSW}	Figure 3		0.58	1	µs
T/R Switch Turn-Off Time	$t_{OFFTRSW}$	Figure 3 (Note 6)		0.08	.2	µs
Setup Time from Receive to Transmit	TXSETUP	See Note 7	1			µs
Output Enable Time (Shutdown Mode to Normal Operation)	t_{EN1}				100	µs
Output Disable Time (Normal Operation to Shutdown Mode)	t_{DIS1}				10	µs

AC Electrical Characteristics (continued)

(V_{DD} = +3V, $V_{CC\_}$ = +5V, $V_{EE\_}$ = -5V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, CC0 = CC1 = low, RTZ = low, R_L = 1kΩ, C_L = 220pF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Transparent to Sync Mode Change Time	t_{TP2SY}				5	µs
Sync Mode to Transparent Time	t_{SY2TP}				500	ns
Input Setup Time Single-Ended	t_{SETUP1}	V_{DD} = 2.5V; single-ended clock	1.5			ns
Input Hold Time Single-Ended	t_{HOLD1}	V_{DD} = 2.5V; single-ended clock	1.5			ns
Input Setup Time Differential	t_{SETUP2}	V_{DD} = 2.5V; differential clock	1.4			ns
Input Hold Time Differential	T_{HOLD2}	V_{DD} = 2.5V; differential clock	1.1			ns
Second-Harmonic Distortion (Low Voltage)	THD2LV	$f_{OUT\_}$ = 5MHz, V_{PP} = -V_{NN} = +5V, square wave (all modes)		-40		dBc
Second-Harmonic Distortion (High Voltage)	THD2HV	$f_{OUT\_}$ = 5MHz, V_{PP} = -V_{NN} = +20V to +100V, square wave (all modes)		-43		dBc
Pulse Cancellation	PC1	$f_{OUT\_}$ = 5MHz, V_{PP} = -V_{NN} = +20V to +100V, 2 periods, all harmonics of the sum signal with respect to the carrier		-40		
Pulser Bandwidth	BW	V_{PP} = +60V, V_{NN} = -60V (Figure 4), SEL = low		30		MHz
RMS Output Jitter	t_J	$f_{OUT\_}$ = 5MHz, V_{PP} = -V_{NN} = +5V, both in clocked mode or transparent mode (Figure 5)		5		ps
T/R Switch Harmonic Distortion	THD_{TRSW}	R_{LOAD} = 200Ω, V_{SIGNAL} = 100mV_{P-P}		-50		dB
T/R Switch Turn-On/Off Voltage Spike	V_{SPIKE}	R_{LOAD} = 1kΩ at both sides of T/R switch		50		mV
Crosstalk	CT	f = 5MHz, adjacent LVOUT_ pins, $R_{LOUT\_}$ = 50Ω		-51		dB

Note 2: All devices are 100% production tested at T_A = +85°C. Limits over the operating temperature range are guaranteed by design.

Note 3: Maximum operating current from $V_{GN\_}$ and $V_{GP\_}$ external power sources can vary depending on application requirements. The suggested minimum values assume 8 channels running in continuous transmission (CWD) at 5MHz with CC0 = CC1 = high.

Note 4: CW Doppler: continuous wave, f = 5MHz, V_{DD} = +3V, $V_{CC\_}$ = -$V_{EE\_}$ = +5V, $V_{PP\_}$ = -$V_{NN\_}$ = 5V, SEL_ = high (HB2 active), R_L = 1KΩ, C_L = 220pF, CC0 = CC1 = 1.

Note 5: B mode: f = 5MHz, PRF = 5kHz, 1 period, V_{DD} = +3V, $V_{CC\_}$ = -$V_{EE\_}$ = +5V, $V_{PP\_}$ = -$V_{NN\_}$ = 100V, SEL_ = low (HB1 active), R_L = 1KΩ, C_L = 220pF, PRF = 5KHz. (Figure 1a)

Note 6: T/R switch turn-off time is the time required to switch off the bias current of the T/R switch. The off-isolation is not guaranteed.

Note 7: Both the T/R switch and Damp are designed to be self protected against the HV transmission. The part is not damaged even if the Transmit setup time is not respected. We recommend having at least 1µs setup time when moving from receive (DINP_ = DINN_ = 1 to transmit DINP_ = DINN_ = 0). For further reducing the inrush leakage through the T/R switch, a longer setup time is recommended (3µs). (T/R Switches)

Timing Diagrams

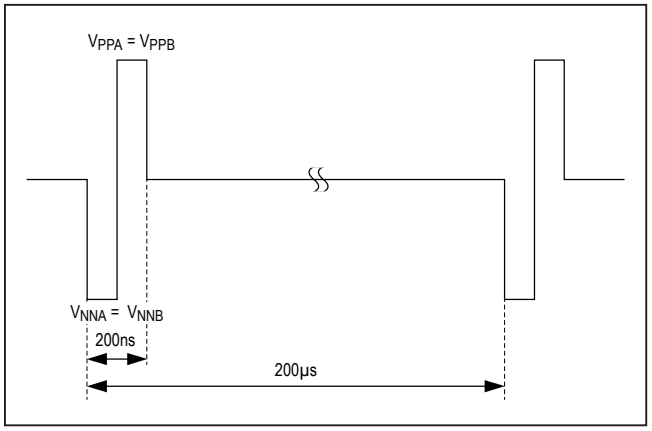


Figure 1a. High-Voltage Burst Test (Three Levels)

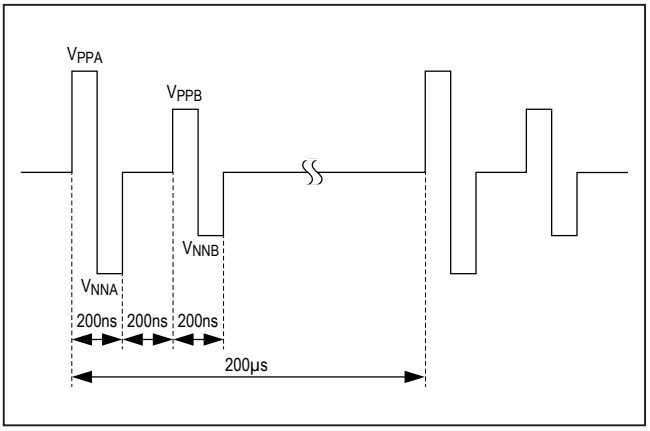


Figure 1b. High-Voltage Burst Test (Five Levels)

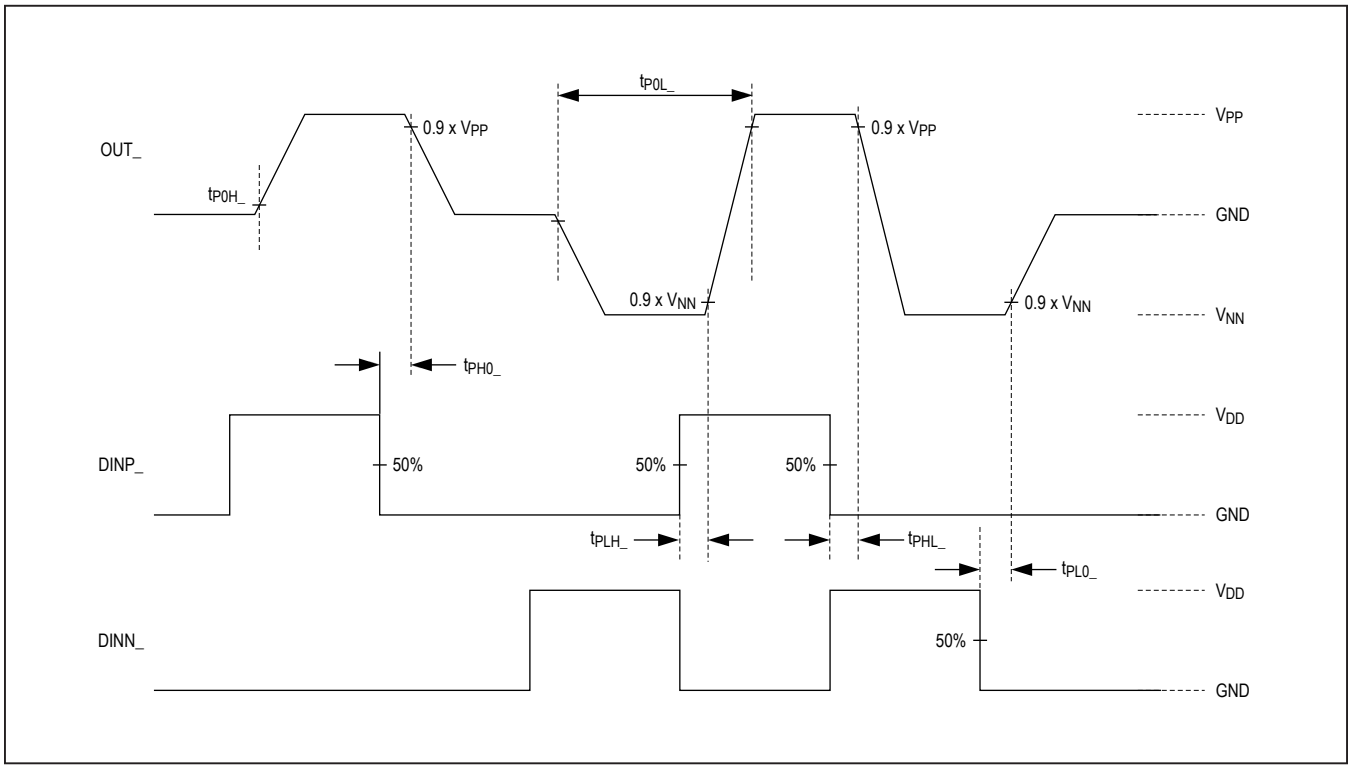


Figure 2a. Propagation Delay Timing

Timing Diagrams (continued)

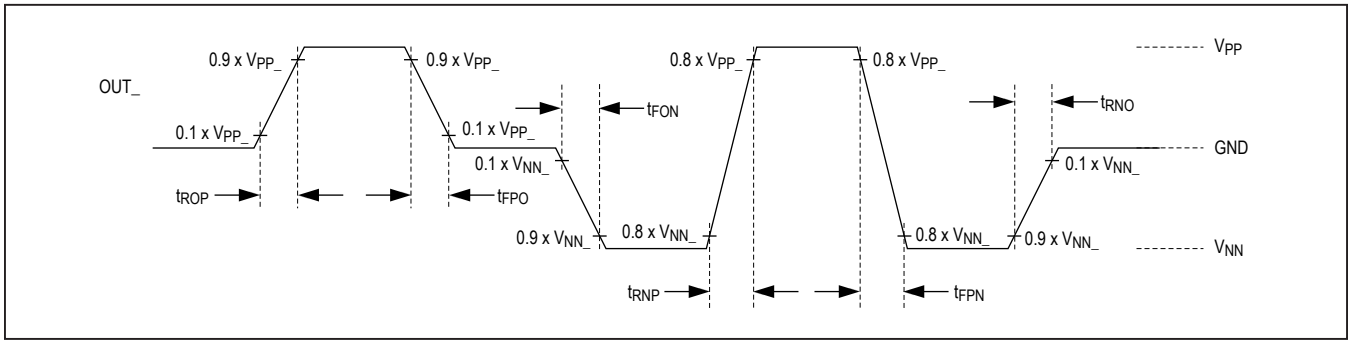


Figure 2b. Output Rise/Fall Timing

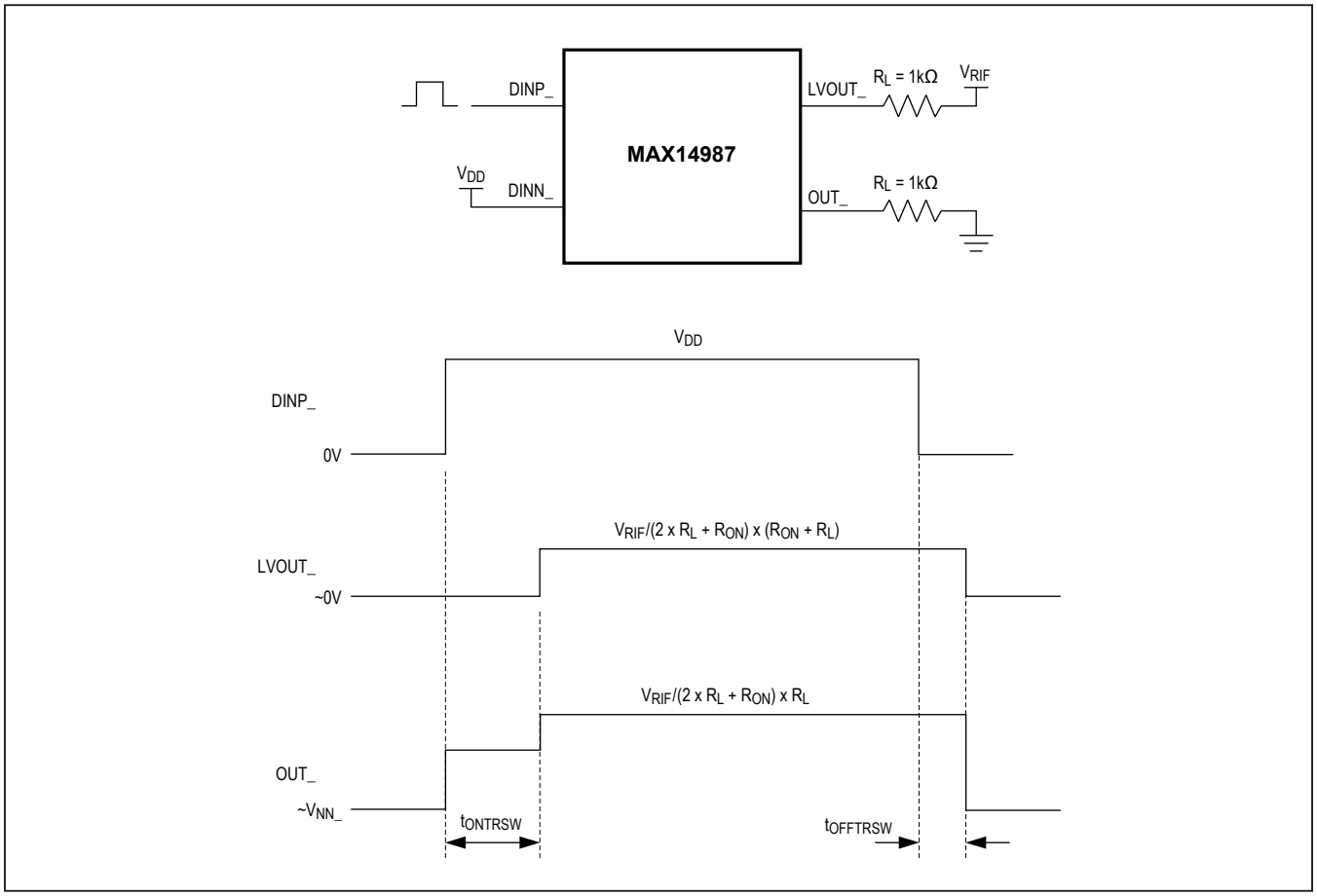


Figure 3. T/R Switch Turn-On/Off Time

Timing Diagrams (continued)

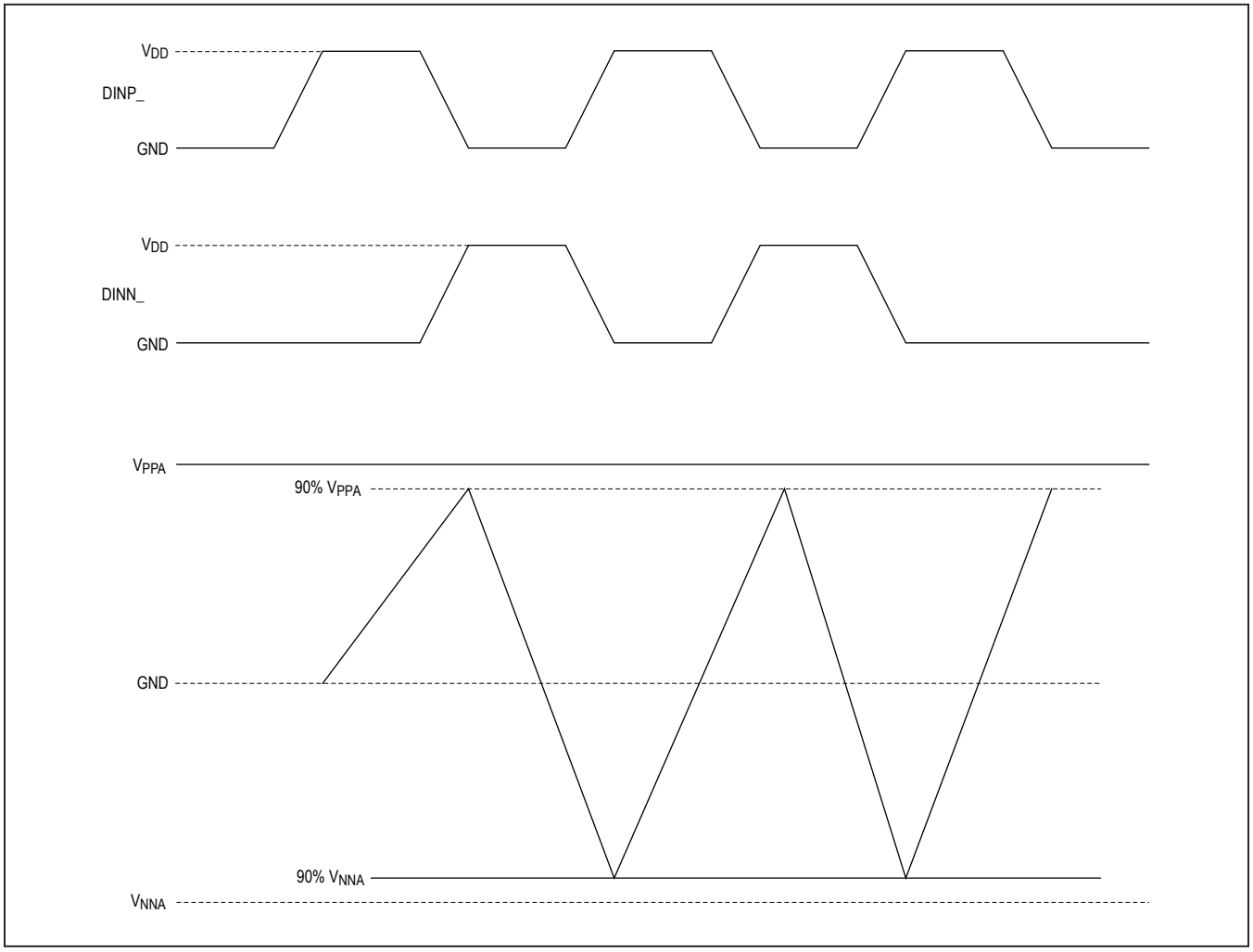


Figure 4. Bandwidth

Timing Diagrams (continued)

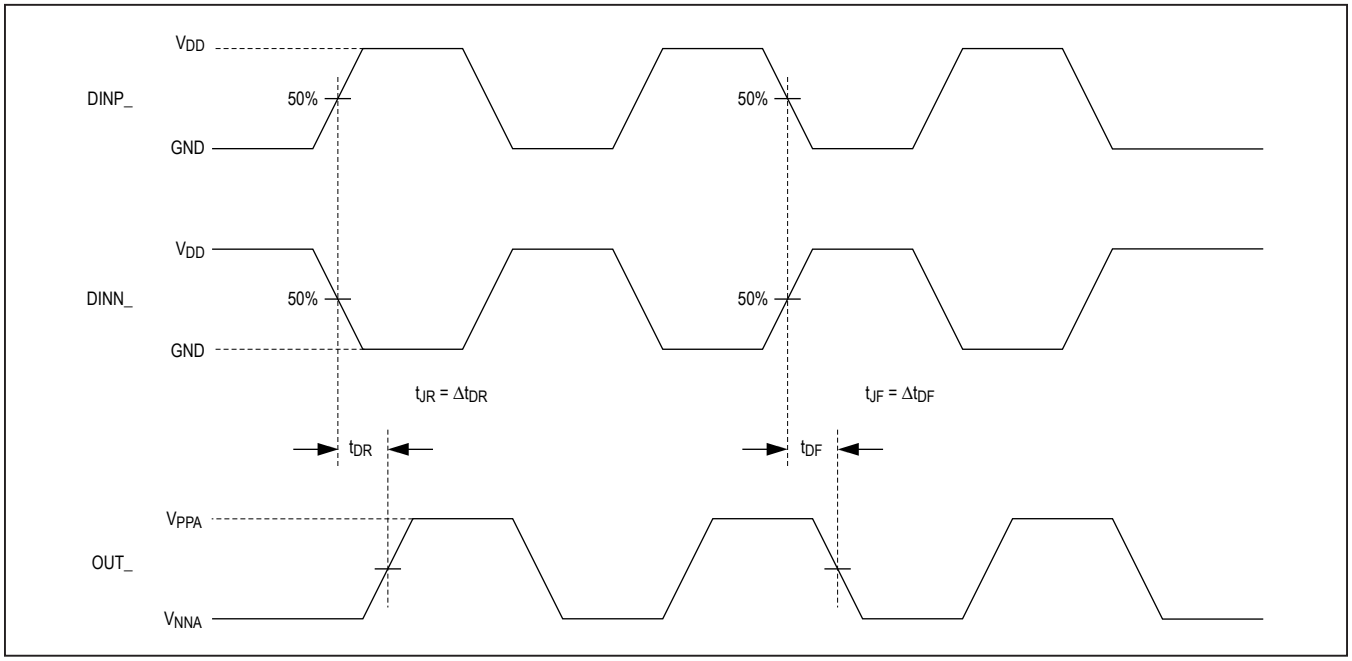
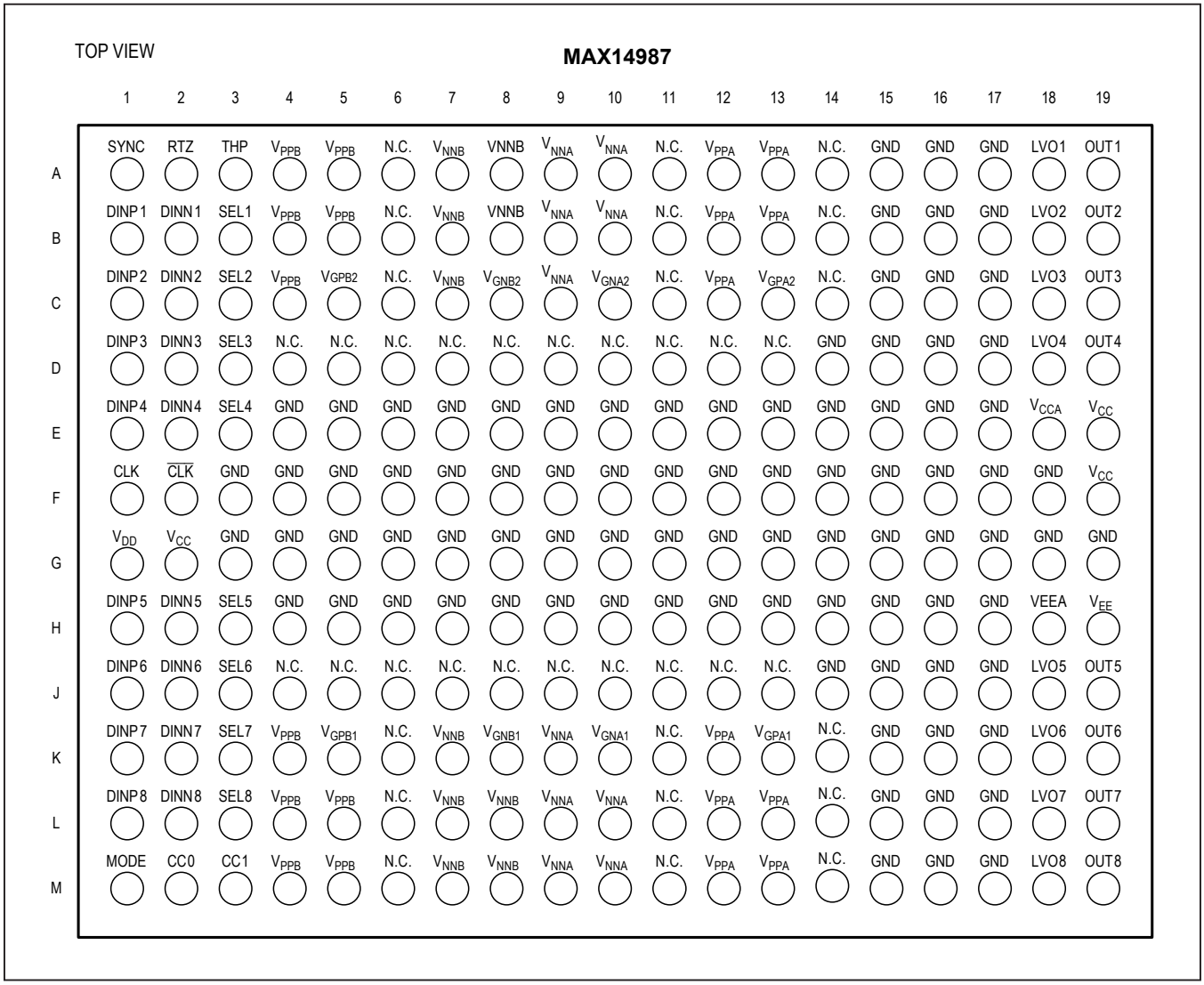


Figure 5. Jitter Timing

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
B2	DINN1	Digital Signal Negative Input 1 (see *Truth Tables* section)
B1	DINP1	Digital Signal Positive Input 1 (see *Truth Tables* section)
B3	SEL1	Digital Signal Select Input 1 (see *Truth Tables* section)
C2	DINN2	Digital Signal Negative Input 2 (see *Truth Tables* section)
C1	DINP2	Digital Signal Positive Input 2 (see *Truth Tables* section)
C3	SEL2	Digital Signal Select Input 2 (see *Truth Tables* section)
D2	DINN3	Digital Signal Negative Input 3 (see *Truth Tables* section)
D1	DINP3	Digital Signal Positive Input 3 (see *Truth Tables* section)
D3	SEL3	Digital Signal Select Input 3 (see *Truth Tables* section)
E2	DINN4	Digital Signal Negative Input 4 (see *Truth Tables* section)
E1	DINP4	Digital Signal Positive Input 4 (see *Truth Tables* section)
E3	SEL4	Digital Signal Select Input 4 (see *Truth Tables* section)
G1	V_{DD}	Logic Supply Voltage Input
H2	DINN5	Digital Signal Negative Input 5 (see *Truth Tables* section)
H1	DINP5	Digital Signal Positive Input 5 (see *Truth Tables* section)
H3	SEL5	Digital Signal Select Input 5 (see *Truth Tables* section)
J2	DINN6	Digital Signal Negative Input 6 (see *Truth Tables* section)
J1	DINP6	Digital Signal Positive Input 6 (see *Truth Tables* section)
J3	SEL6	Digital Signal Select Input 6 (see *Truth Tables* section)
K2	DINN7	Digital Signal Negative Input 7 (see *Truth Tables* section)
K1	DINP7	Digital Signal Positive Input 7 (see *Truth Tables* section)
K3	SEL7	Digital Signal Select Input 7 (see *Truth Tables* section)
K2	DINN8	Digital Signal Negative Input 8 (see *Truth Tables* section)
K1	DINP8	Digital Signal Positive Input 8 (see *Truth Tables* section)
K3	SEL8	Digital Signal Select Input 8 (see *Truth Tables* section)

Pin Description (continued)

PIN	NAME	FUNCTION
A15–A17, B15–B17, C15–C17, D14–D17, E4–E17, F3–F18, G3–G19, H4–H17, J14–J17, K15, K16, K17, L15–L17, M15–M17	GND	Ground
A18	LVO1	Low-Voltage T/R Switch Output 1
B18	LVO2	Low-Voltage T/R Switch Output 2
C18	LVO3	Low-Voltage T/R Switch Output 3
D18	LVO4	Low-Voltage T/R Switch Output 4
J18	LVO5	Low-Voltage T/R Switch Output 5
K18	LVO6	Low-Voltage T/R Switch Output 6
L18	LVO7	Low-Voltage T/R Switch Output 7
M18	LVO8	Low-Voltage T/R Switch Output 8
H19	V_{EE}	V_{EE} Digital Supply Voltage Input. Connect 470nF or greater bypass capacitor to GND as close as possible to the device
E19, F19, G2	V_{CC}	V_{CC} Digital Supply Voltage Input. Connect 470nF or greater bypass capacitor to GND as close as possible to the device
H18	V_{EEA}	V_{EE} Analog Supply Voltage Input. Connect 470nF or greater bypass capacitor to GND as close as possible to the device
E18	V_{CCA}	V_{CC} Analog Supply Voltage Input. Connect 470nF or greater bypass capacitor to GND as close as possible to the device
K5	V_{GPB1}	High Side Driver Floating Voltage Supply Outputs. Connect 1µF bypass capacitor between V_{GPB1} and V_{PPB} as close as possible to the device.
K8	V_{GNB1}	Low Side Driver Floating Voltage Supply Outputs. Connect 1µF bypass capacitor between V_{GNB1} and V_{NNB} as close as possible to the device

Pin Description (continued)

PIN	NAME	FUNCTION
K13	V_{GPA1}	High Side Driver Floating Voltage Supply Outputs. Connect 1µF bypass capacitor between V_{GPA1} and V_{PPA} as close as possible to the device
K10	V_{GNA1}	Low-Side Driver Floating Voltage Supply Outputs. Connect 1µF bypass capacitor between V_{GNA1} and V_{NNA} as close as possible to the device
C5	V_{GPB2}	High-Side Driver Floating Voltage Supply Outputs. Connect 1µF bypass capacitor between V_{GPB2} and V_{PPB} as close as possible to the device
C8	V_{GNB2}	Low-Side Driver Floating Voltage Supply Outputs. Connect 1µF bypass capacitor between V_{GNB2} and V_{NNB} as close as possible to the device
C13	V_{GPA2}	High-Side Driver Floating Voltage Supply Outputs. Connect 1µF bypass capacitor between V_{GPA2} and V_{PPA} as close as possible to the device
C10	V_{GNA2}	Low-Side Driver Floating Voltage Supply Outputs. Connect 1µF bypass capacitor between V_{GNA2} and V_{NNA} as close as possible to the device
A7, A8, B7, B8, C7, K7, L7, L8, M7, M8	V_{NNB}	HV Negative Power Supply Input. Connect 1µF bypass capacitor between V_{NNB} and GND as close as possible to the device
A4, A5, B4, B5, C4, K4, L4, L5, M4, M5,	V_{PPB}	HV Positive Power Supply Input. Connect 1µF bypass capacitor between V_{PPB} and GND as close as possible to the device
A9, A10, B9, B10, C9, K9, L9, L10, M9, M10	V_{NNA}	HV Negative Power Supply Input. Connect 1µF bypass capacitor between V_{NNA} and GND as close as possible to the device
A12, A13, B12, B13, C12, K12, L12, L13, M12, M13	V_{PPA}	HV Positive Power Supply Input. Connect 1µF bypass capacitor between V_{PPA} and GND as close as possible to the device
M19	HVOUT8	High-Voltage Pulser Output 8
L19	HVOUT7	High-Voltage Pulser Output 7
K19	HVOUT6	High-Voltage Pulser Output 6
J19	HVOUT5	High-Voltage Pulser Output 5
D19	HVOUT4	High-Voltage Pulser Output 4
C19	HVOUT3	High-Voltage Pulser Output 3
B19	HVOUT2	High-Voltage Pulser Output 2
A19	HVOUT1	High-Voltage Pulser Output 1
M1	MODE	Mode Control Input. Control operation mode (see Truth Tables section).
M2	CC0	Current Control Input. Control current capability (see Truth Tables section).
M3	CC1	Current Control Input. Control current capability (see Truth Tables section).
A2	RTZ	Return-to-Zero current capability control input. Drive RTZ high for 2.5A driving current. Drive RTZ low for 1.25A driving current.
A3	THP	Open-Drain Thermal-Protection Output. THP asserts and sinks a 3mA current to GND. When the junction temperature exceeds 150°C
F1	CLK	Clock positive phase Input.

Pin Description (continued)

PIN	NAME	FUNCTION
F2	$\overline{CLK}$	Clock negative phase Input. Connect this pin to GND to operate in single ended mode onto CLK.
A1	SYNC	CMOS Control Input. Drive SYNC high to enable clocked-input mode. Drive SYNC low to operate in transparent mode (see Truth Tables section).
A6, A11, A14, B6, B11, B14, C6, C11, C14, D4–D13, J4–J13, K6, K11, K14, L6, L11, L14, M6, M11, M14	N.C.	No Connect.

General Description

The MAX14987 octal five-level, high-volage (HV) pulser device generates high-frequency HV bipolar pulses (up to ±105V) from low-voltage control logic inputs for driving piezoelectric transducers in ultrasound systems. All eight channels have embedded overvoltage-protection diodes and an integrated active return-to-zero clamp. The device has embedded independent (floating) power supplies (FPS) and level shifters that allow signal transmission without the need for external HV capacitors. The device also features eight integrated transmit/receive (T/R) switches.

The device features two modes of operation: shutdown mode and octal five-level mode pulsing (with integrated active return-to-zero clamp). In octal five-level mode pulsing, each channel is controlled by three logic inputs (DINN_/DINP_/SEL_). Each channel features two HV half-bridges operating from independent pairs of voltage supplies (V_{PPA}, V_{NNA} and V_{PPB}, V_{NNB}) and sharing the same output. The half-bridge operating form V_{PPA}, V_{NNA} is named HB1 while the half-bridge operating from V_{PPB}, V_{NNB} is named HB2. The voltage rating is the same for the two half-bridges. They can both operate from 0 to ±105V.

HB1 is sized to provide a maximum driving current in excess of ±2.5A and is optimized in terms of bandwidth and PWM performances.

HB2 is sized to provide a maximum driving current of ±1.6A and is normally intended to be used in Doppler modes (CWD, CFM, PWD). The driving current of HB2 can be programmed at 1.6A, 1.1A, 0.5A, and 0.3A. This allows reducing the power dissipation in particular for CWD modality. HB2 exhibits excellent jitter (< 6ps) and phase noise performances (156dBc @1kHz offset) in CWD modality.

The return-to-zero (clamp) driving current can also be programmed either at 1.25A or 2.5A by mean of a dedicated CMOS input (RTZ).

The device can operate both in clocked and transparent mode. In clocked mode, data inputs can be synchronized with a clean differential or single-ended clock to reduce phase noise associated with FPGA output signals that are detrimental for Doppler analysis. In transparent mode, the synchronization feature is disabled and output reflects the data input after a 500ns delay.

The device features integrated grass-clipping diodes (with low parasitic capacitance) for receive (Rx) and transmit (Tx) isolations. The device features a damping circuit that can be activated as soon as the transmit burst is over. It fully discharges the pulser's output internal node before the grass-clipping diodes.

The device is available in a 228-bump (10mm x 16mm) BGA package and is specified over the -40°C to +85°C extended temperature range.

Operation Mode

The device has two operation modes: shutdown and octal five-level. Use the MODE input to select the operation mode.

Shutdown Mode

This is the lowest power dissipation mode. No transmission and no reception is possible. See Table 1.

Octal 5 Levels—Normal Operation Mode

In this mode the MAX14987 features eight independent channels that can generate a five-level, dual-mode pulsing scheme. The part features two fully independent dual-voltage supplies (V_{PPA}, V_{NNA} and V_{PPB}, V_{NNB}). Depending on the logic level of the SELX input pin, the pulser operates either from V_{PPA}, V_{NNA} or from V_{PPB}, V_{NNB}, respectively, with 2A and up to 1.6A current capability.

The return-to-zero clamp current capability can be programmed at 1.25A or 2.5A (see Truth Tables section) by way of a dedicated CMOS input.

Three inputs per channel are provided to control the pulser output status. This implies that each channel has a dedicated SELX digital control input. This allows 5 levels burst shaping like:

GND - V_{PPB} - V_{NNA} - V_{PPA} - V_{NNB} - GND or

GND - V_{NNB} - V_{PPA} - V_{NNA} - V_{PPB} - GND.

In case burst-shaping is not required, all the SELX digital inputs can be tied together and used as a unique global control signal for composite modes.

The transmitter exhibits excellent slew rate and can generate minimum pulses down to 10ns resulting in optimal performances whenever PWM is used to shape the transmit burst.

A minimum 1µs setup time before the transmit burst must be respected. During the setup time DINN_ and DINP_, must be kept low. This timing is required to completely switch off the T/R switch and the damp before the Transmit burst (see Figure 6) See Table 2.

Truth Tables

Table 1. Shutdown Mode (MODE = Low)

INPUTS			OUTPUTS	
DINN_	DINP_	SEL_	OUT_	LVOUT_
X	X	X	High impedance	High impedance (T/R switch off)

X = Don't care

Table 2. Normal Operation Mode (MODE = High)

DINN_	DINP_	SEL_	HVOUT_	LVOUT_
0	0	X	Clamp ON Damp OFF	TR Switch OFF LVOUT = GND
0	1	0	V_{PPA} Damp OFF	TR Switch OFF LVOUT = GND
1	0	0	V_{NNA} Damp OFF	TR Switch OFF LVOUT = GND
0	1	1	V_{PPB} Damp OFF	TR Switch OFF LVOUT = GND
1	0	1	V_{NNB} Damp OFF	TR Switch OFF LVOUT = GND
1	1	X	Clamp ON Damp ON	TR Switch ON

0 = logic-low, 1 = logic-high.

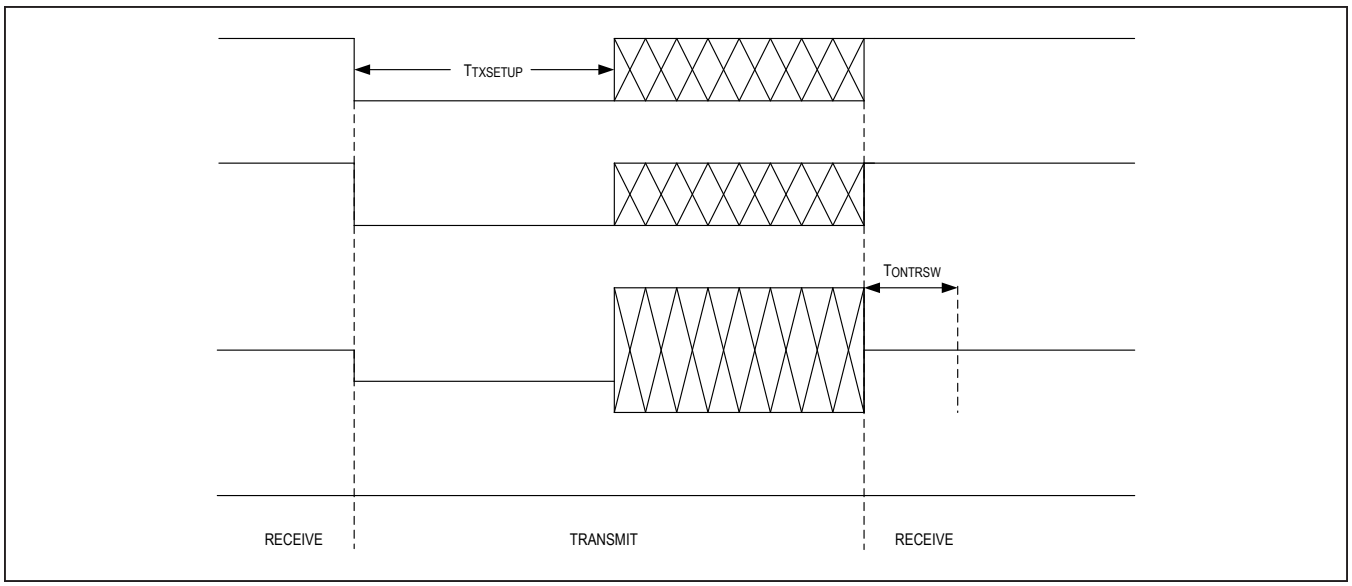


Figure 6. Timing Diagram

Current Capability Selection

The current capability of the HB2 pulser can be programmed by controlling inputs CC0 and CC1. This feature can be used to save power when working in low-voltage mode (like CWD) and the maximum current capability is no longer required.

The current capability of the RTZ (return-to-zero or clamp) can also be programmed between two levels 1.25A and 2.5A respectively. See Table 3 for CC0, CC1, and RTZ.

Sync Function

The device provides the ability to resynchronize all the data inputs by means of a clean clock signal. In ultrasound systems, the FPGA output signals are often affected by high jitter. The jitter induces phase noise that is detrimental in Doppler analysis. The input clock can be either a differential signal or a single-ended signal running up to 200MHz. Data is clocked in on the rising-edge of the CLK input (falling-edge of BCLK). Connect BCLK to GND for single-ended operation. The sync feature can be enabled or disabled by the SYNC control input. Drive the SYNC input low to disable the synchronization function (no external clock signal). Drive the SYNC input high to enable the synchronization function (with an external clock signal). Figure 7 shows the simplified CLK and $\overline{CLK}$ inputs schematic.

Table 3. Current Drive Selection

INPUTS		PULSER OUTPUT CURRENT (typ)
CC0	CC1	
0	0	1.5
1	0	1.1
0	1	0.5
1	1	0.3

T/R Switches

Each channel features a low-power T/R switch. The T/R switch recovery time after the transmission is 0.5µs (typ). The T/R switches are controlled by the same pulser digital inputs (see Table 3).

The MAX14987 features dedicated analog voltage supply pins which are internally used for the T/R switches only (V_{CCA}, V_{EEA}).

The T/R switch must be turned off at least 1µs before the transmission (see Figure 3). A longer setup time (up to 3µs) is recommended to further minimize the inrush leakage current flowing through the T/R switch during transmission.

Grass-Clipping Diodes

A pair of diodes in antiparallel configuration (referred to as grass-clipping diodes) is presented at each pulser's output. The diodes' reverse capacitance is extremely low, allowing a perfect isolation between the receive path and the actual pulser's output stage.

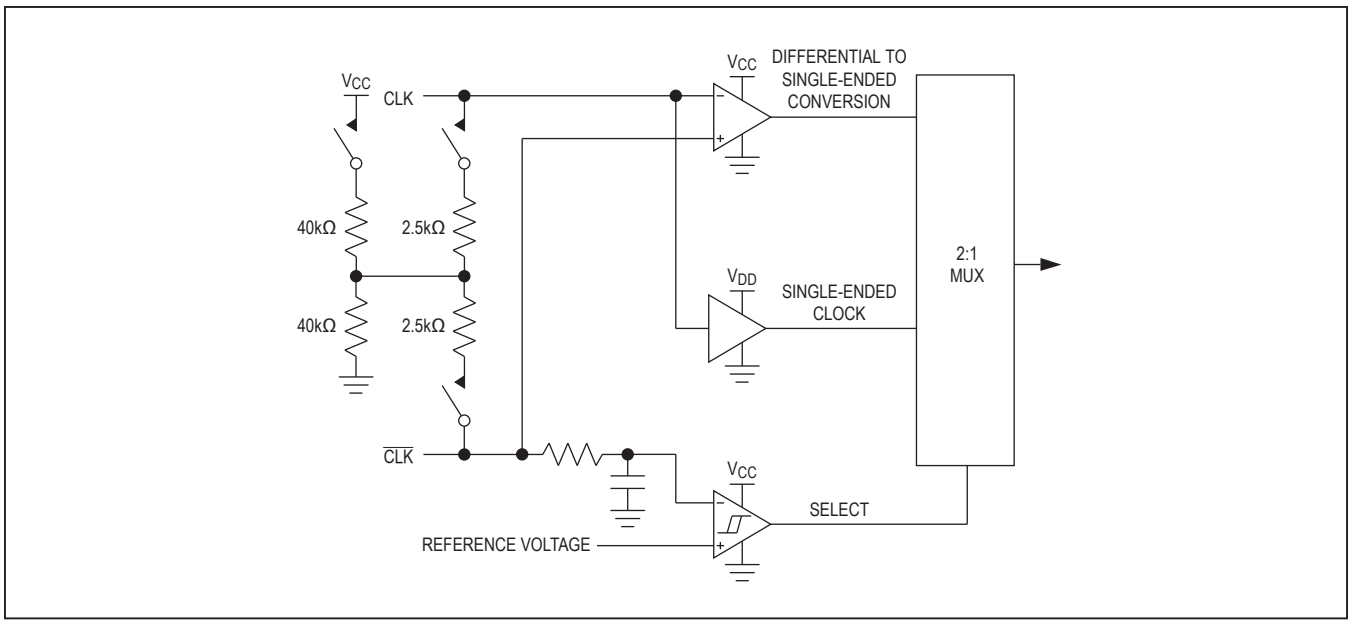


Figure 7. Simplified CLK and $\overline{CLK}$ Inputs Schematic

Table 4. HB2 Pulser Output Current Drive Selection

CC0	CC1	PULSER OUTPUT CURRENT (typ)
0	0	1.6A
0	1	0.5A
1	0	1.1A
1	1	0.3A

Active Damp Circuit

An active damp circuit is integrated between the internal pulser output node (before grass-clipping diodes) and GND. The purpose of this circuit is to fully discharge the pulser output internal node so that the node is not left in high-impedance condition as soon as the transmit burst is over. This results in two main advantages:

1) The grass-clipping isolation is more effective.
2) Suppression of any low-frequency oscillation of a node that could be detrimental for Doppler mode performances.

Table 5. RTZ Current Selection

RTZ	RTZ PROGRAMMED CURRENT
0	2.5A
1	1.25A

The integrated damp circuit is self-protected. The damp circuit must be turned off at least 1µs before the transmission (transmit setup time).

Thermal Warning Outputs

As soon as the internal junction temperature exceeds 150°C, the part automatically enters in shutdown mode and the open-drain THP is asserted. The part again enters normal operation and the open-drain output pin is released as soon as the temperature drops below 120°C.

Power Sequencing

The device does not require any power-up/power-down sequence. However, the MODE pin must be forced to GND or left unconnected during power-up/power-down sequence to prevent the transmitter to be turned on inadvertently.

Applications Information

Floating power supplies

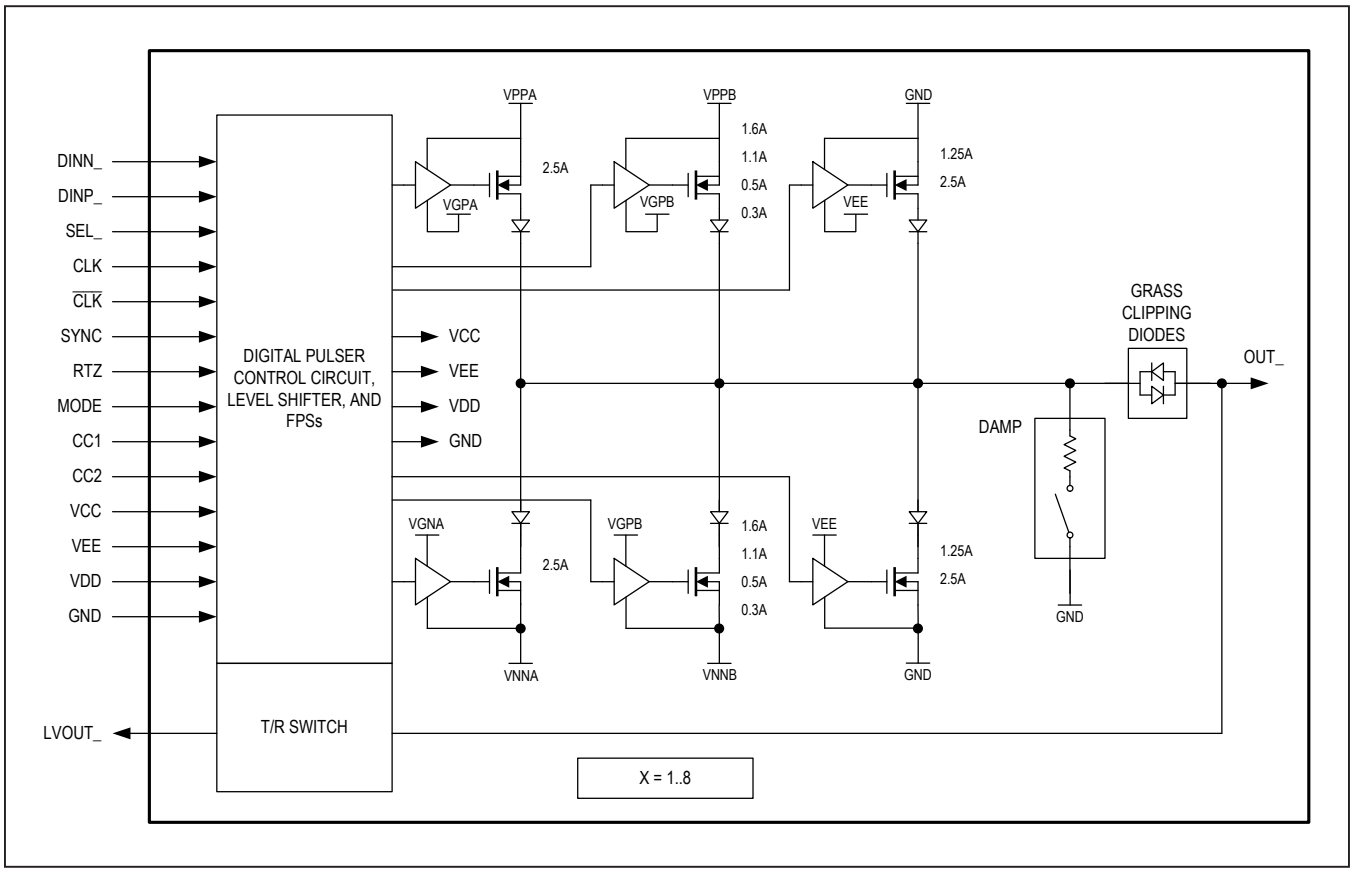
The MAX14987 Floating power supply regulator outputs (pins V_{GPA1}, V_{GPA2}, V_{GNA1}, V_{GNA2}, V_{GPB1}, V_{GNB1}, V_{GPB2}, V_{GNB2}) are independent and must remain separated. Connect 1µF bypass capacitors between each pin and the paired voltage supply as per the pin description and the application diagram. Place capacitors as close as possible to the device and minimize trace length. Use SMD bypass capacitance with voltage rating greater then 6V, low ESR, and ESL.

Layout Concerns

The inner balls of the BGA array must be connected to GND. To aid heat dissipation, having a ground plane connecting the MAX14807 GND balls on the top layer of the PCB is recommended. Such a plane must be properly connected to the inner GND layers using multiple thermal viases.

The device's high-speed pulser requires low-inductance bypass capacitors to their supply inputs. High-speed PCB trace design practices are recommended. Pay particular attention to minimize trace lengths and use sufficient trace width to reduce inductance. Use of surface-mount components is recommended.

Functional Diagram



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14987EXP+CKR	-40°C to +85°C	228 BGA
MAX14987EXP+	-40°C to +85°C	228 BGA

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.analog.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.
228 BGA	X22860+3	**21-1047**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/15	Initial release	—
1	6/15	Removed future product designation from MAX14987EXP+	4, 5, 9, 10, 24
2	4/16	Changed *Input Setup Time Differential* and *Input Hold Time Differential* units	12