MAX14918, MAX14918A

SPI / Parallel Controlled Quad Low-Side Switches with Reverse Current Detection

General Description

The MAX14918 and MAX14918A are quad 700mA low-side switches for industrial applications. Each device features four 140mΩ (typ) on-resistance (R_{ON}) switches with integrated ±1.2kV/42Ω surge protection. Two or more outputs can be connected in parallel to provide higher load current.

The maximum load current is actively limited and is resistor settable between 100mA (typ) and 900mA (typ). For load that draws high inrush current, the MAX14918 and MAX14918A have the inrush mode which provides 2x current after switch turn-on for 10ms (min).

The MAX14918 has an SPI allowing control of multiple MAX14918 devices through a common daisy-chained interface for high channel-count applications, minimizing galvanic isolation channels. Per-channel diagnostics are returned on the serial data output (SDO). Data corruption on the serial data input (SDI) is automatically detected and signaled on the $\overline{\text{SPIFLT}}$ output.

The MAX14918A offers a pin-based switch control with a latch option (LATCHEN) which allows sharing of the four IN_ control signals among multiple MAX14918A devices.

Slew rate control provides controlled turn-on edge for reducing electromagnetic interference or EMI emissions. Simultaneously, a global $\overline{\text{DIS}}$ control signal allows disabling of all OUT_ switches quickly.

The integrated 5V low dropout (LDO) regulator in the MAX14918 and MAX14918A can be used to power external isolators or other logic circuitry.

Applications

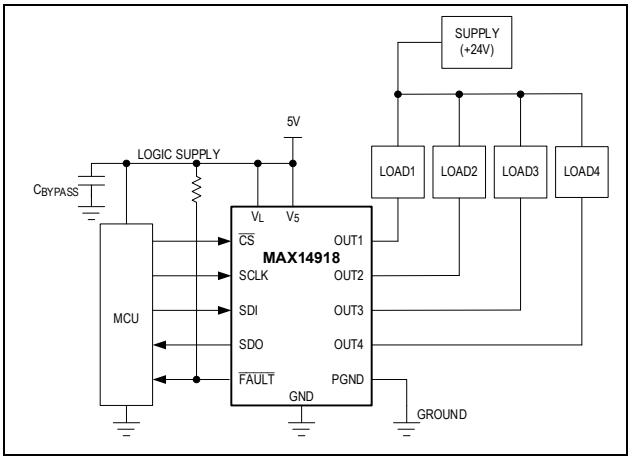
- Industrial Digital Outputs
- Relay and Solenoid Drivers
- Programmable Logic Controllers and Distributed Control Systems
- Motor Control
- Industrial/Process/Building Automation

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- +5V (V_5) or +7V to +65V (V_{DD}) Supply Voltage Operation
- 700mA DC Capability Per Channel across Temperature Range
- 140mΩ (typ) On-Resistance Per Channel
- Settable Load Current Limit 100mA (typ) to 900mA (typ)
- +5V to +48V Load Voltage Range
- 2x Inrush Load Current Option for 10ms (min)
- Robust Design Features
  - Internal Inductive Energy Clamp at +55V (typ)
  - Short-Circuit Protection at OUT_ of up to +49V
  - Reverse Current Detection against Load-Supply Miswiring
  - ±1.2kV/42Ω Surge Protection
  - ±8kV Contact and ±25kV Air-Gap ESD Protection
  - -40°C to +125°C Operating Ambient Temperature
- Diagnostic $\overline{\text{FAULT}}$ Indication for
  - Thermal Overload
  - Reverse Load Current Detection
  - Undervoltage Lockout (UVLO) on V_5 Supply
- Compact 24-Pin, 4mm x 5mm TQFN Package

Simplified Application Diagram



19-101689; Rev 1; 09/23

Absolute Maximum Ratings

V_{DD} to GND ..... -0.3V to +70V

V_5, V_L to GND ..... -0.3V to +6V

$\overline{REV}$, RCLIM to GND ..... -0.3V to (V_5 + 0.3)V

$\overline{CS}$, SCLK, SDI, $\overline{DIS}$, HISLEW, INRUSH, IN_, LATCHEN to GND ..... -0.3V to +6V

$\overline{FAULT}$, $\overline{SPIFLT}$ to GND ..... -0.3V to +6V

SDO to GND ..... -0.3V to (V_L + 0.3)V

GND to PGND ..... -0.3V to +0.3V

OUT1, OUT2, OUT3, OUT4 to PGND ..... -0.3V to V_{CLAMP}

Continuous OUT_ Current ..... +700mA

Continuous Power Dissipation (T_A = +70°C)

24 TQFN (Single-Layer Board) (derate at 20.8 mW/°C above +70°C) 1666.7mW

24 TQFN (Multilayer Board) (derate at 28.6 mW/°C above +70°C) 2285.7mW

Temperature Ratings

Operating Temperature Range ..... -40°C to +125°C

Maximum Junction Temperature ..... +150°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24 TQFN	
Package Code	T2445+2C
Outline Number	21-0201
Land Pattern Number	90-0083
THERMAL RESISTANCE, SINGLE LAYER BOARD	
Junction-to-Ambient (θ_{JA})	48°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1.8°C/W
THERMAL RESISTANCE, MULTILAYER BOARD	
Junction-to-Ambient (θ_{JA})	35°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1.8°C/W

Electrical Characteristics

(V_{DD} = +7V to +65V, V_5 = +4.5V to +5.5V, V_L = +1.62V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC, V_{DD} = +24V, V_L = V_5) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY (V_5, V_L)						
V_5 Supply Voltage	V_5	V_{DD} = GND or unconnected	4.5	5.0	5.5	V
V_5 Supply Current	I_{5_ON}	All OUT_ switches on or off, V_{DD} = GND or unconnected		2.0	3.0	mA
V_5 Undervoltage Lockout Threshold	V_{5_UVLO}	V_5 falling, OUT_ switches are three-state in UVLO, V_{DD} = GND or unconnected	3.5		4.2	V
V_5 Undervoltage Lockout Hysteresis	$V_{5\_UVLO\_HYS}$	V_{DD} = GND or unconnected		0.2		V
V_L Supply Voltage	V_L		1.62		5.5	V
V_L Supply Current	I_L	Logic inputs are at GND or V_L		11	50	µA
V_L Undervoltage Lockout Voltage	V_{L_UVLO}	V_L falling	0.7		1.4	V
V_L Undervoltage Lockout Hysteresis	$V_{L\_UVLO\_HYS}$			50		mV

(V_{DD} = +7V to +65V, V_5 = +4.5V to +5.5V, V_L = +1.62V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC, V_{DD} = +24V, V_L = V_5) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LINEAR REGULATOR (V_{DD}, V_5)							
V_{DD} Supply Voltage Range	V_{DD}			7		65	V
V_{DD} Supply Current	I_{DD}	V_{DD} ≥ 7V, no load on V_5			2.0	3.0	mA
V_5 Regulator Output Voltage	V_5	V_{DD} ≥ 7V, 0mA to 30mA load current on V_5		4.75	5.0	5.25	V
V_5 Regulator Current Limit	I_{CL_V5}	V_{DD} ≥ 7V, V_5 = 4V		35			mA
V_5 Line Regulation		7V ≤ V_{DD} ≤ 65V, I_5 = 5mA			0.035		mV/V
V_5 Load Regulation		0 ≤ I_5 ≤ 20mA, V_{DD} ≥ 7V			0.175		%
SWITCH OUTPUTS (OUT_)							
On-Resistance	R_{ON}	$I_{OUT\_}$ = 500mA			140	300	mΩ
Current Limit	I_{LIM}	INRUSH = 0, or INRUSH = 1 and t_{LIM} > 15ms	R_{CLIM} = 100kΩ	140	200	270	mA
			R_{CLIM} = 27kΩ	700	800	900	
			R_{CLIM} = open	650		950	
Inrush Current Limit	I_{INRUSH_LIM}	INRUSH = 1 or high for 10ms after switch turn-on			2 x I_{LIM}		mA
Inductive Clamp Voltage	V_{CLAMP}	OUT_ is off, $I_{OUT\_}$ = 500mA		49	55		V
Off-State Leakage Current at OUT_	I_{LKG}	IN_ = low, $V_{OUT\_}$ = 0V to 45V (*Note 2*)		0		3.0	µA
RCLIM Voltage	V_{RCLIM}	R_{CLIM} = 27kΩ		1.165	1.2	1.235	V
RCLIM Short Resistance Threshold	R_{CLIM_SHORT}			4.5	6.5	9	kΩ
RCLIM Open Resistance Threshold	R_{CLIM_OPEN}			400	650	1000	kΩ
Maximum Switching Rate	SR	50% IN_ Duty Cycle	HISLEW = low		50		kHz
			HISLEW = high		500		
Turn-Off Propagation Delay (Low-to-High)	t_{OFF}	HISLEW = low	MAX14918: delay from $\overline{CS}$ going high to OUT_ rising by 0.5V, R_L = 48Ω, C_L = 100pF, V_{LOAD} = 24V (see *Figure 1*)		110	220	ns
			MAX14918A: delay from IN_ switching low to OUT_ rising by 0.5V, R_L = 48Ω, C_L = 100pF, V_{LOAD} = 24V (see *Figure 1*)		110	220	
		HISLEW = high	MAX14918: delay from $\overline{CS}$ going high to OUT_ rising by 0.5V, R_L = 48Ω, C_L = 100pF,		110	220	

(V_{DD} = +7V to +65V, V_5 = +4.5V to +5.5V, V_L = +1.62V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC, V_{DD} = +24V, V_L = V_5) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			V_{LOAD} = 24V (see *Figure 1*)				
			MAX14918A: delay from IN_ switching low to OUT_ rising by 0.5V, R_L = 48Ω, C_L = 100pF, V_{LOAD} = 24V (see *Figure 1*)		110	220	
Turn-On Propagation Delay (High-to-Low)	t_{ON}	HISLEW = low	MAX14918: delay from $\overline{CS}$ going high to OUT_ falling by 0.5V, R_L = 48Ω, C_L = 100pF, V_{LOAD} = 24V (see *Figure 1*)		370	750	ns
			MAX14918A: delay from IN_ switching high to OUT_ falling by 0.5V, R_L = 48Ω, C_L = 100pF, V_{LOAD} = 24V (see *Figure 1*)		370	750	
		HISLEW = high	MAX14918: delay from $\overline{CS}$ going high to OUT_ falling by 0.5V, R_L = 48Ω, C_L = 100pF, V_{LOAD} = 24V (see *Figure 1*)		70	150	
			MAX14918A: delay from IN_ switching high to OUT_ falling by 0.5V, R_L = 48Ω, C_L = 100pF, V_{LOAD} = 24V (see *Figure 1*)		70	150	
Output Fall-Time	t_F	HISLEW = low	Output falling 80% to 20% of final value, V_{LOAD}= 24V, R_L= 48Ω, C_L= 100pF (see *Figure 2*)		1030	1900	ns
		HISLEW = high	Output falling 80% to 20% of final value, V_{LOAD}= 24V, R_L= 48Ω, C_L= 100pF (see *Figure 2*)		125	250	

(V_{DD} = +7V to +65V, V_5 = +4.5V to +5.5V, V_L = +1.62V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC, V_{DD} = +24V, V_L = V_5) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Rise-Time	t_R	HISLEW = low	Output rising 20% to 80% of final value, V_{LOAD}= 24V, R_L= 48Ω, C_L= 100pF (see *Figure 2*)		110		ns
		HISLEW = high	Output rising 20% to 80% of final value, V_{LOAD}= 24V, R_L= 48Ω, C_L= 100pF (see *Figure 2*)		110		
REVERSE CURRENT DETECTION ($\overline{REV}$)							
Reverse Current Detection Threshold	$I_{TH\_OUT\_RV\_OFF}$	$V_5 > V_{5\_UVLO}$, current flow out of any OUT_	OUT_ switch is off	-185	-135	-95	mA
	$I_{TH\_OUT\_RV\_ON}$	$V_5 > V_{5\_UVLO}$, current flow out of any OUT_	OUT_ switch is on	-190	-150	-115	
$\overline{REV}$ Pullup Current (Not in Reverse Condition)	I_{REV_PU}	$V_5 > V_{5\_UVLO}$, $I_{OUT\_} \geq I_{TH\_OUT\_RV\_X}$, $V_{REV} = V_5 - 0.4V$		25	45		µA
$\overline{REV}$ Pulldown Resistance (Reverse Condition)	R_{REV_PD}	$V_5 > V_{5\_UVLO}$, $I_{OUT\_} < I_{TH\_OUT\_RV\_X}$			8	16	Ω
Auto-Retry Delay	t_{REV_AR}	Delay until $\overline{REV}$ output is turned back on after reverse condition turn-off			2		s
LOGIC INPUTS (INRUSH, HISLEW, $\overline{DIS}$, IN_, LATCHEN, SDI, SCLK, $\overline{CS}$)							
Input Voltage High	V_{IH}			0.8 x V_L			V
Input Voltage Low	V_{IL}					0.2 x V_L	V
Input Threshold Hysteresis	V_{I_TH}				0.1		V
Input Pulldown Resistor	R_{PD}	All logic input pins, except $\overline{CS}$			100		kΩ
Input Pullup Resistor	R_{PU}	$\overline{CS}$ input			100		kΩ
LOGIC OUTPUT ($\overline{FAULT}$, $\overline{SPIFLT}$, SDO)							
Output Logic Low	V_{OL}	$\overline{FAULT}$, $\overline{SPIFLT}$, I_{LOAD} = 5mA sink				0.33	V
Output Logic High	V_{OH}	SDO, I_{LOAD} = -5mA source		V_L - 0.33			V
Three-State Leakage	I_{LEAK}	Open-drain output $\overline{FAULT}$, $\overline{SPIFLT}$, V_{PULLUP} = 5V (*Note 2*)		-1		+1	µA
SDO Pulldown Resistor	R_{PD}	$\overline{CS}$ is high			100		kΩ
TIMING CHARACTERISTICS							
SPI (MAX14918) (see *Figure 3*)							
SCLK Clock Period	t_{CH+CL}			100			ns
SCLK Pulse Width High	t_{CH}			35			ns
SCLK Pulse Width Low	t_{CL}			45			ns
$\overline{CS}$ Falling to SCLK Rising Time	t_{CLK_SU}			50			ns

(V_{DD} = +7V to +65V, V_5 = +4.5V to +5.5V, V_L = +1.62V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC, V_{DD} = +24V, V_L = V_5) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDI Hold Time	t_{DH}		10			ns
SDI Setup Time	t_{DS}		10			ns
SDO Propagation Delay	t_{DO}	C_{LOAD} = 10pF at SDO pin, SCLK falling edge to SDO stable			35	ns
SDO Rise and Fall Times	t_{FT}			1		ns
SCLK Rising to $\overline{CS}$ Rising Time	t_{CSH}		100			ns
$\overline{CS}$ Pulse Width High	t_{CSPW}		50			ns
MAX14918A (see *Figure 4*)						
IN_ to LATCHEN Setup Time	$t_{LATCHSU}$	MAX14918A only, see *Figure 4*	10			ns
THERMAL PROTECTION						
Per-Channel Thermal Shutdown Temperature	T_{JSHDN}	Junction temperature rising per-channel		160		°C
Per-Channel Thermal Shutdown Hysteresis	T_{JSHDN_HYS}			15		°C
Chip Thermal Shutdown	T_{CSHDN}	Temperature rising		150		°C
Chip Thermal-Shutdown Hysteresis	T_{CSHDN_HYS}			10		°C
LDO Shutdown Temperature	T_{DSHDN}	Temperature rising		160		°C
ELECTROMAGNETIC COMPATIBILITY						
Surge Tolerance	V_{SURGE}	OUT_ to COM, IEC 61000-4-5 1.2µs/50µs waveform (42Ω/0.5µF)		±1.2		kV
ESD Contact Discharge	V_{ESD_C}	OUT_ to COM, IEC 61000-4-2		±8		kV
ESD Air-Gap Discharge	V_{ESD_A}	OUT_ to COM, IEC 61000-4-2		±25		kV
ESD HBM		All pins		±2		kV

Note 1: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: Current into the device is positive and current out of the device is negative.

Timing Diagrams

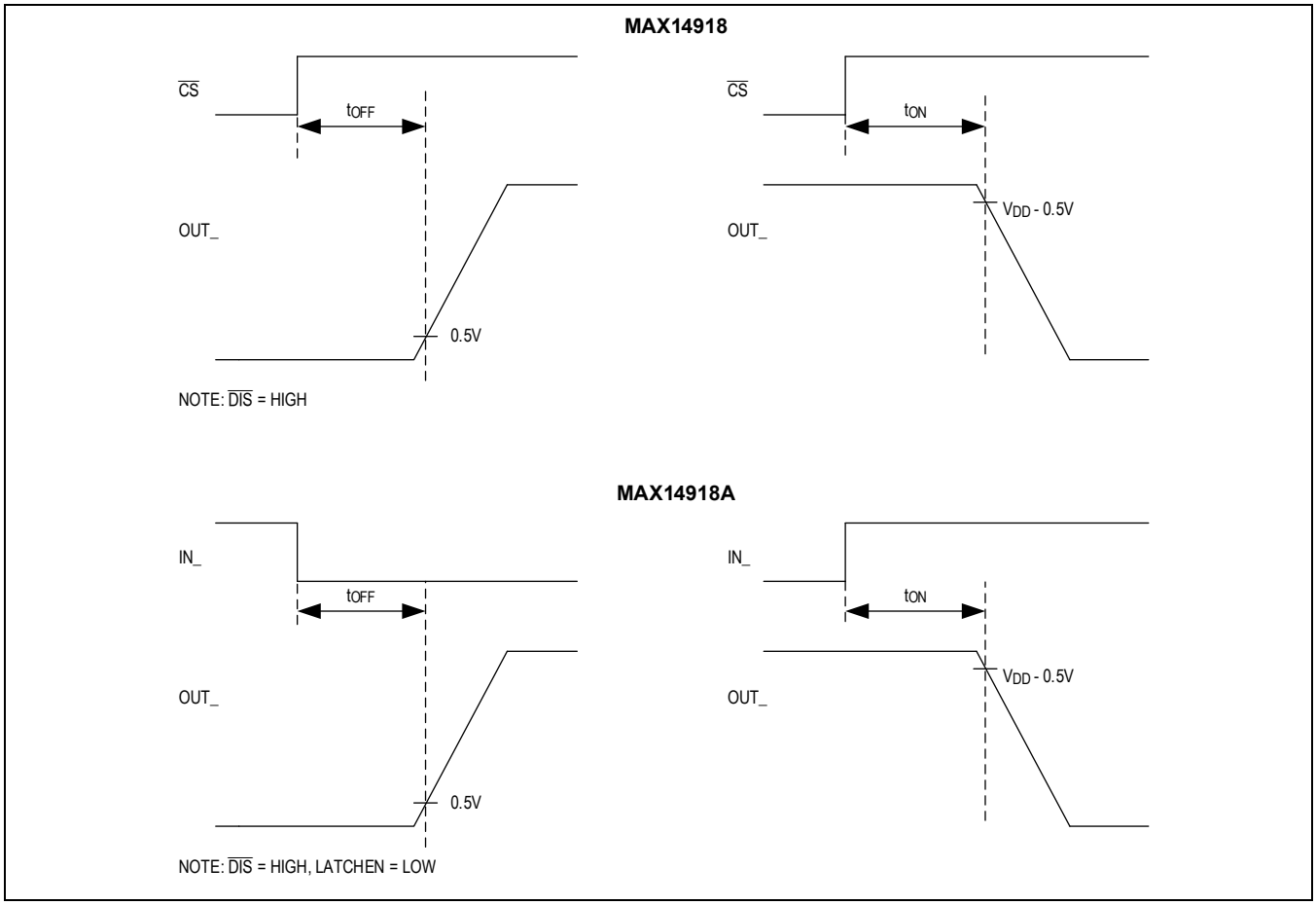


Figure 1. OUT_ Propagation Delay in MAX14918 and MAX14918A

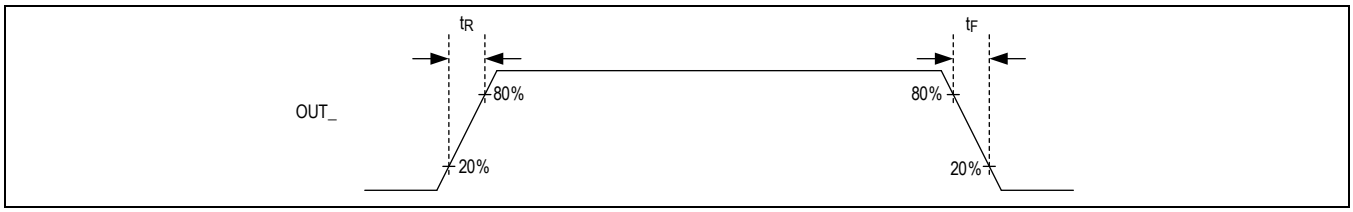


Figure 2. OUT_ Rise and Fall Times

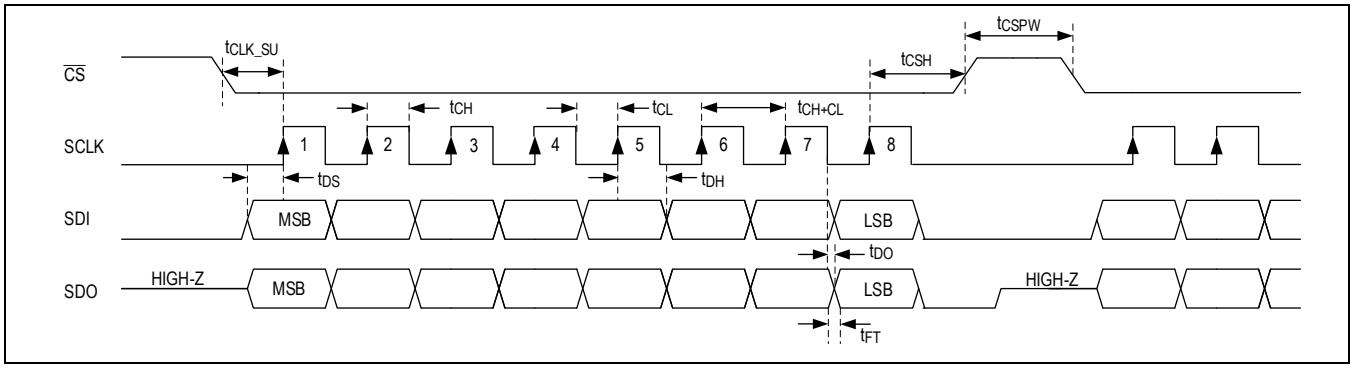


Figure 3. SPI Timing Diagram

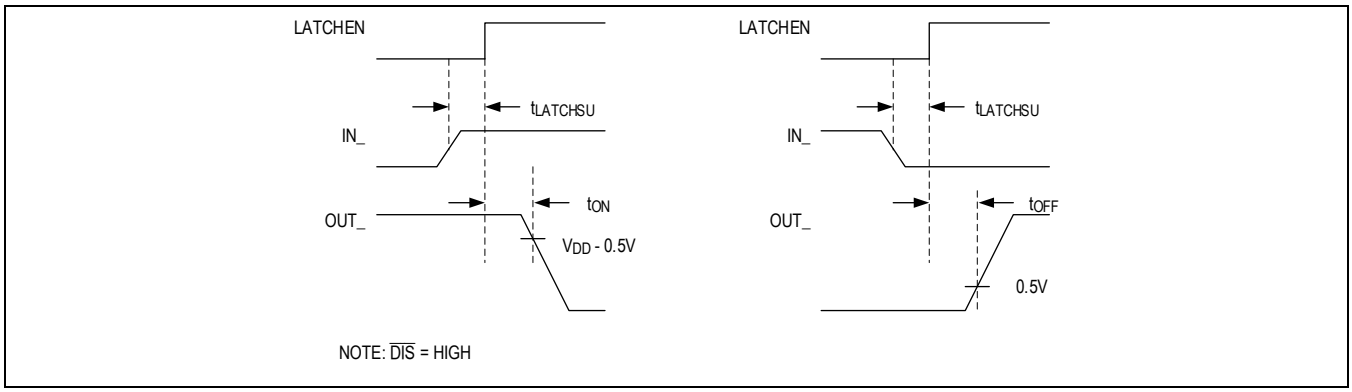
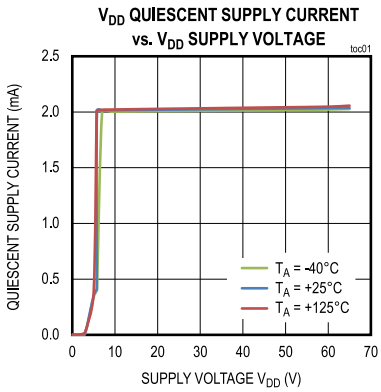
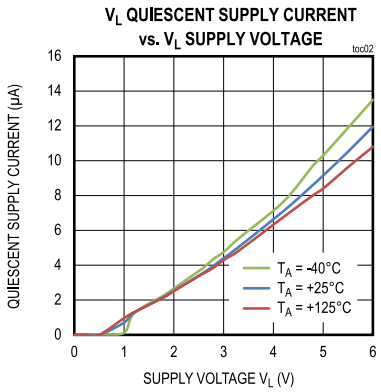


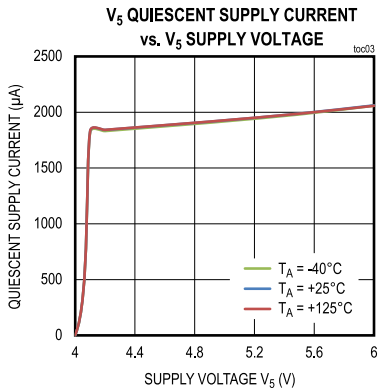
Figure 4. IN_ to LATCHEN Setup Time

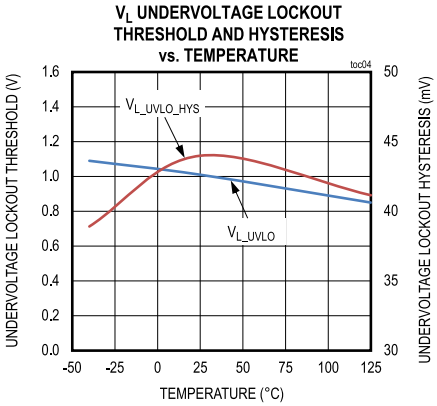
Typical Operating Characteristics

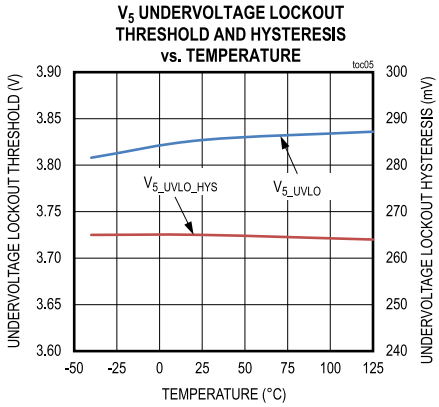
(V_{DD} = +24V, V_L = V_5, INRUSH = 0V, HISLEW = V_L, T_A = +25°C, unless otherwise noted)

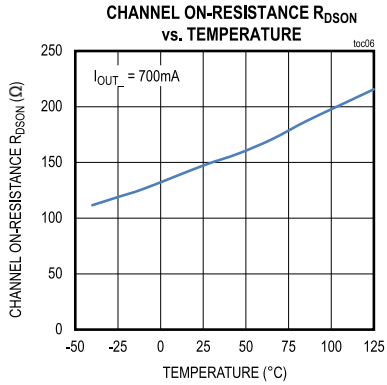


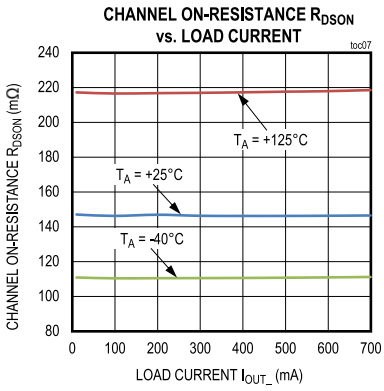


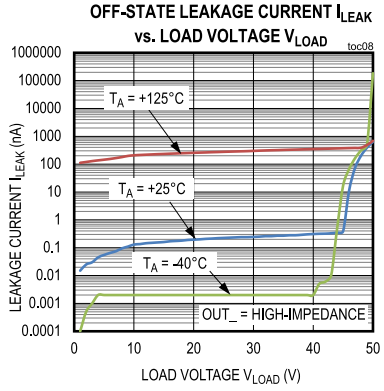


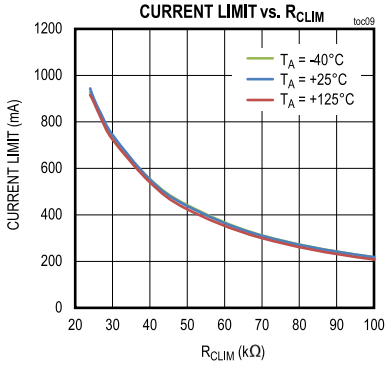






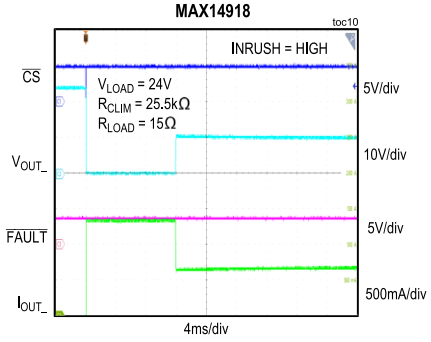




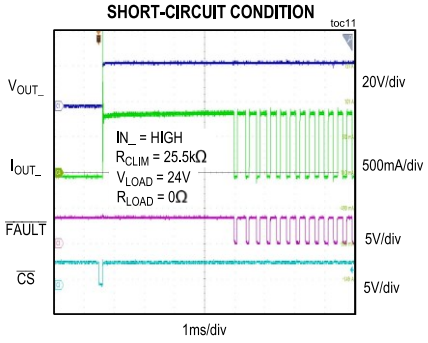


(V_{DD} = +24V, V_L = V_5, INRUSH = 0V, HISLEW = V_L, T_A = +25°C, unless otherwise noted)

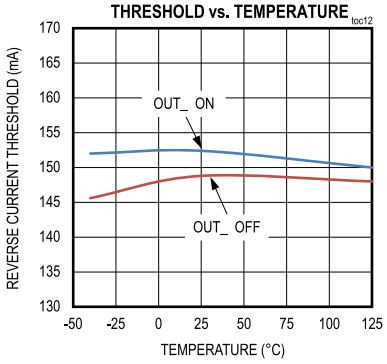
INRUSH RESPONSE IN CURRENT LIMIT MAX14918



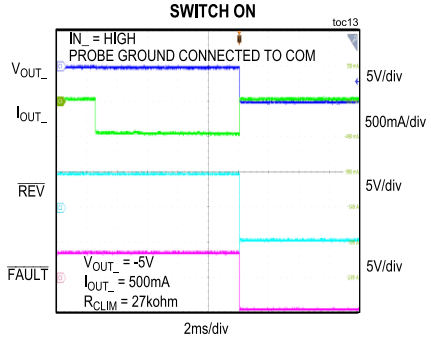
SHORT-CIRCUIT CONDITION



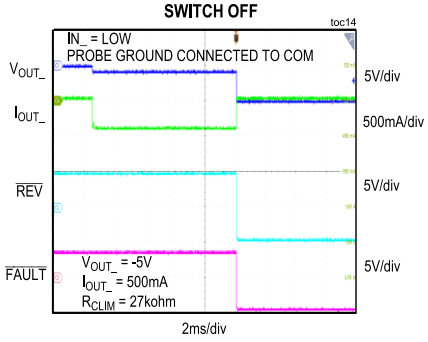
REVERSE CURRENT DETECTION THRESHOLD vs. TEMPERATURE



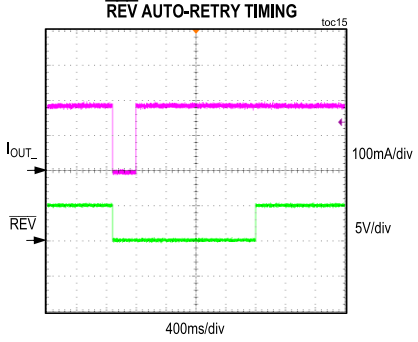
REVERSE CURRENT DETECTION SWITCH ON



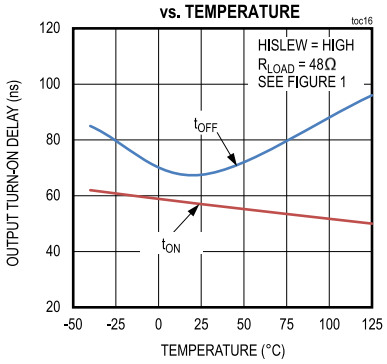
REVERSE CURRENT DETECTION SWITCH OFF



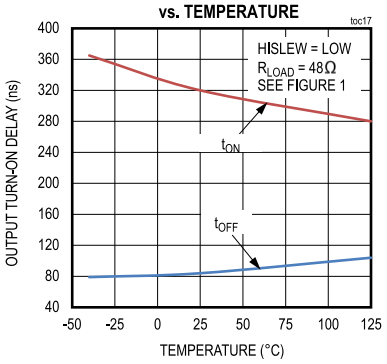
$\overline{REV}$ AUTO-RETRY TIMING



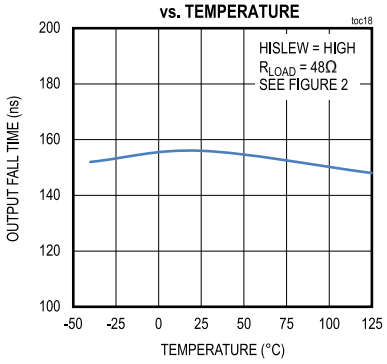
OUTPUT TURN-ON AND TURN-OFF TIME vs. TEMPERATURE



OUTPUT TURN-ON AND TURN-OFF TIME vs. TEMPERATURE

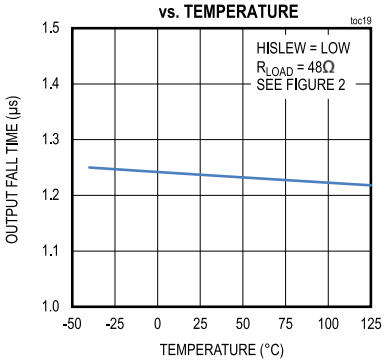


OUTPUT FALL TIME vs. TEMPERATURE

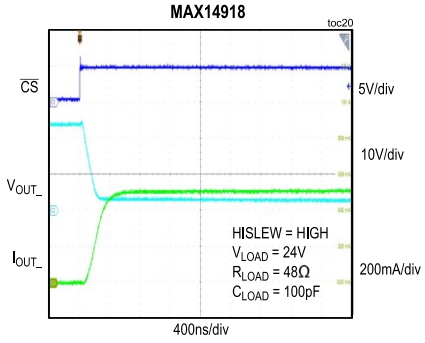


(V_{DD} = +24V, V_L = V_5, INRUSH = 0V, HISLEW = V_L, T_A = +25°C, unless otherwise noted)

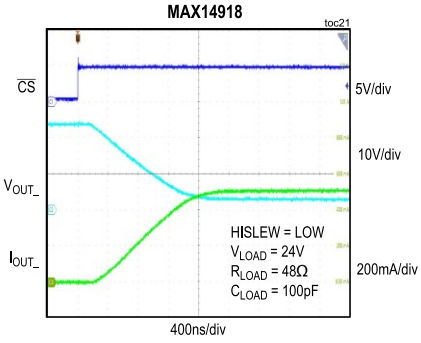
OUTPUT FALL TIME vs. TEMPERATURE



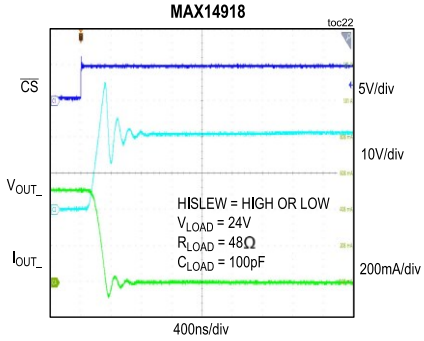
OUTPUT TURN-ON RESPONSE MAX14918



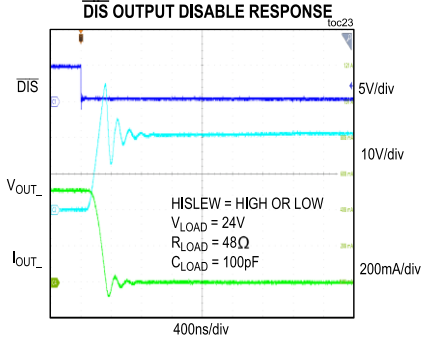
OUTPUT TURN-ON RESPONSE MAX14918



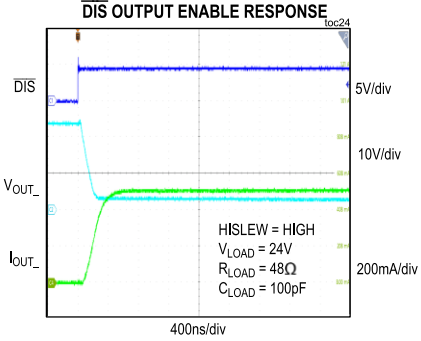
OUTPUT TURN-OFF RESPONSE MAX14918



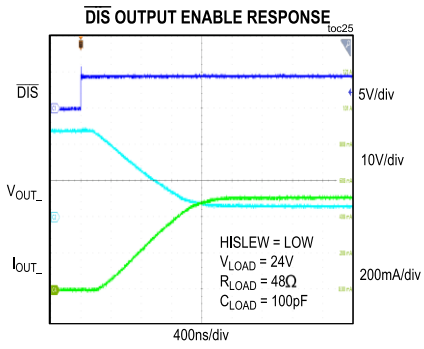
DIS OUTPUT DISABLE RESPONSE



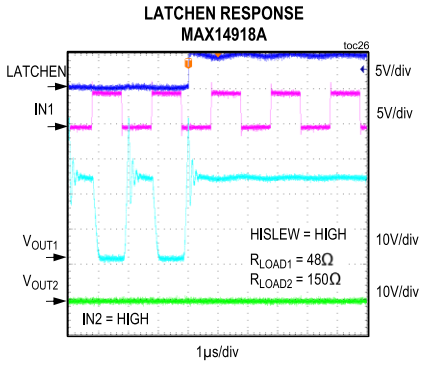
DIS OUTPUT ENABLE RESPONSE



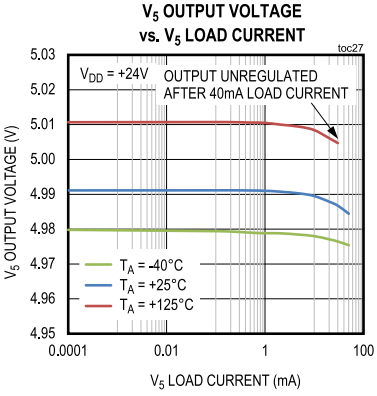
DIS OUTPUT ENABLE RESPONSE



LATCHEN RESPONSE MAX14918A

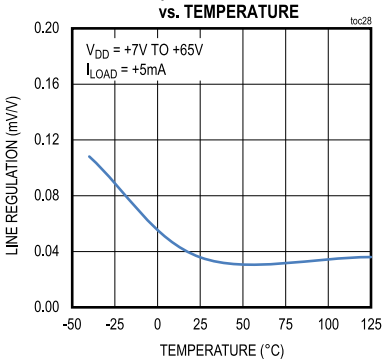


V_5 OUTPUT VOLTAGE vs. V_5 LOAD CURRENT

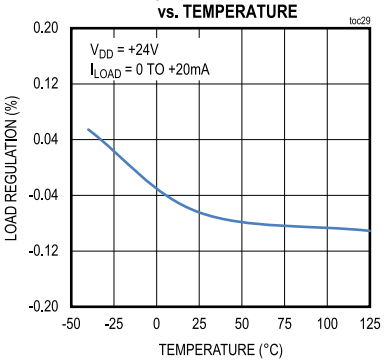


(V_{DD} = +24V, V_L = V_5, INRUSH = 0V, HISLEW = V_L, T_A = +25°C, unless otherwise noted)

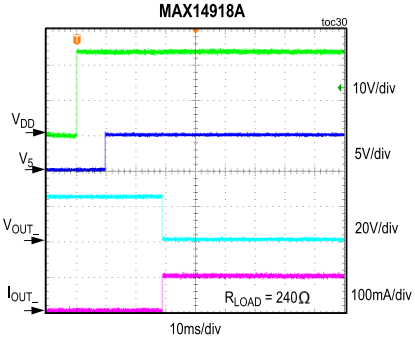
V_5 LINE REGULATION vs. TEMPERATURE



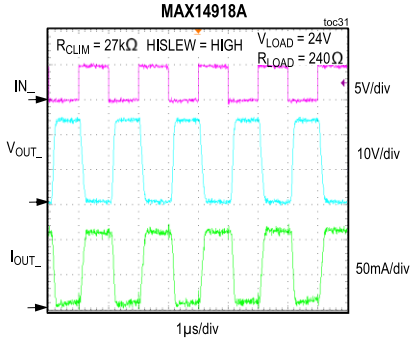
V_5 LOAD REGULATION vs. TEMPERATURE



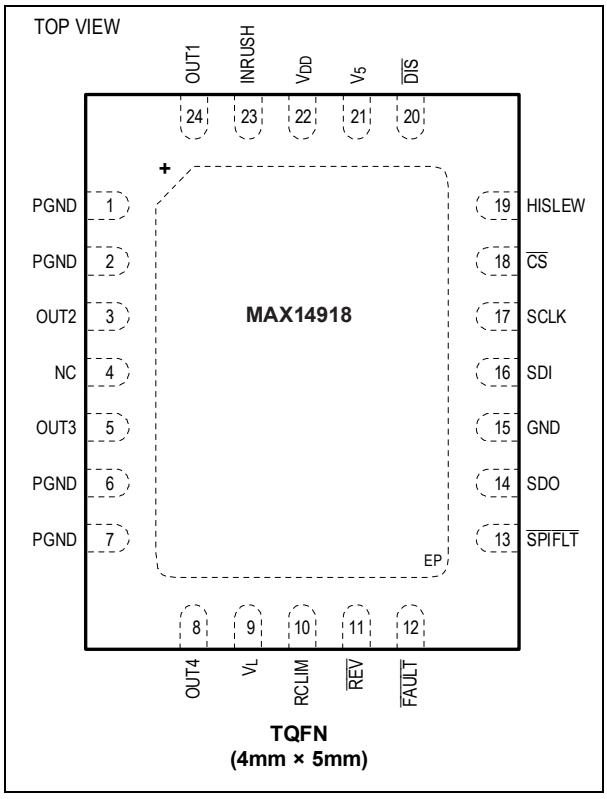
POWER-UP RESPONSE (IN_ = HIGH) MAX14918A



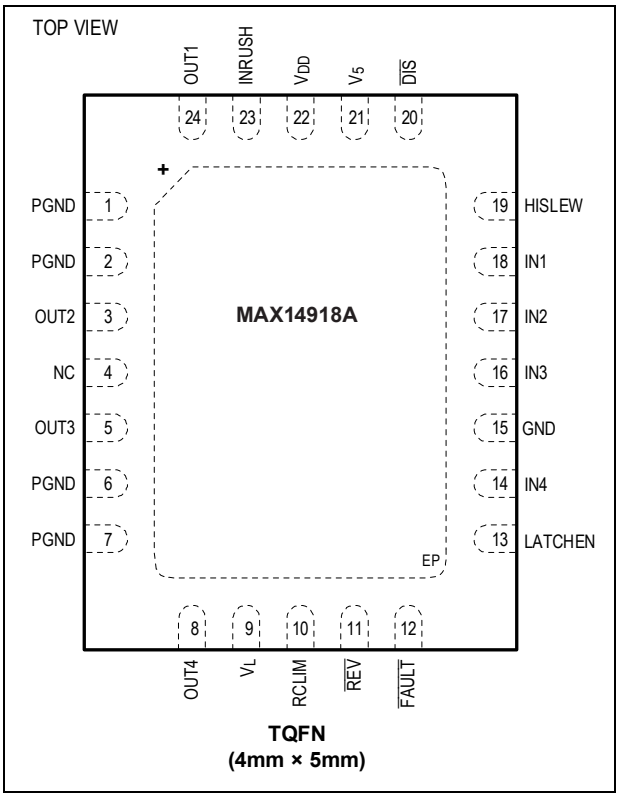
OUTPUT SWITCHING AT 500kHz MAX14918A



Pin Configuration



TQFN
(4mm × 5mm)



TQFN
(4mm × 5mm)

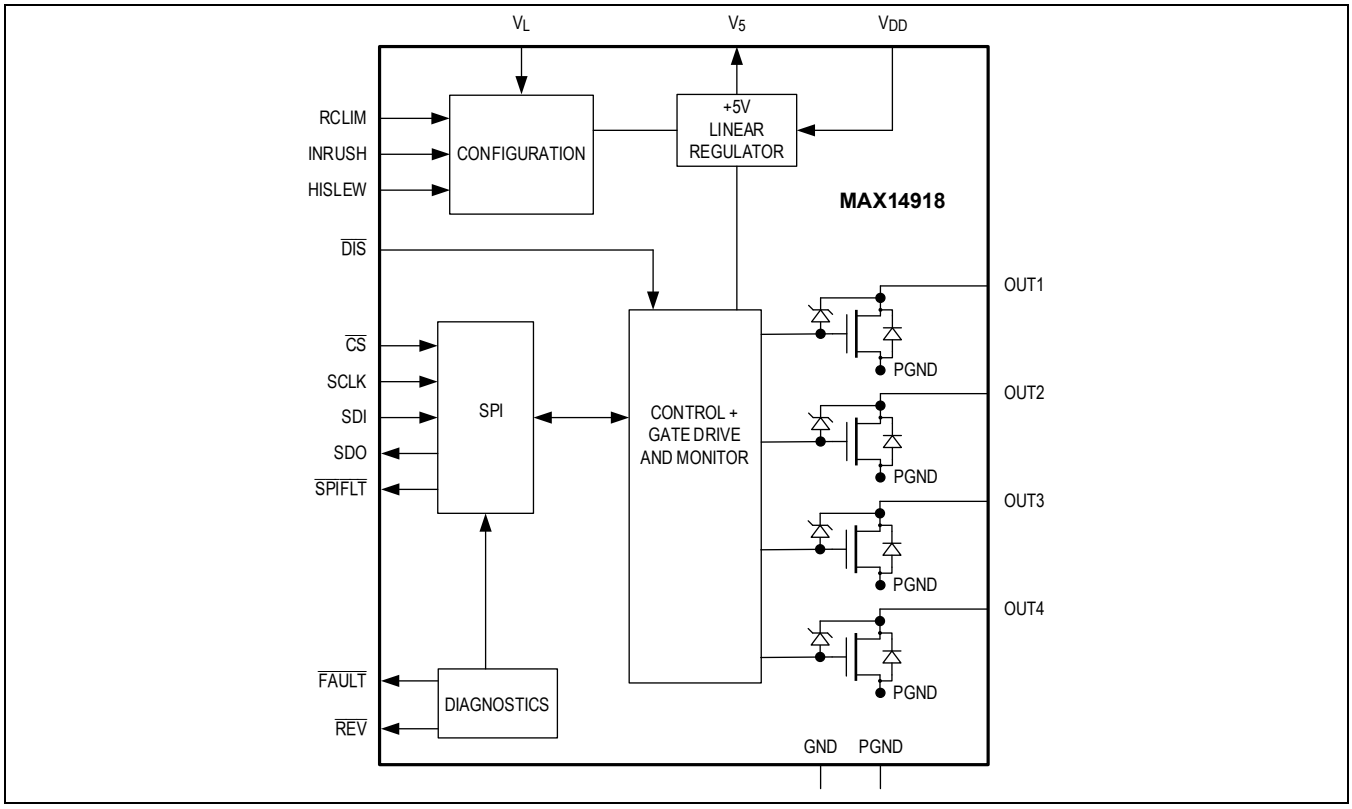
Pin Descriptions

PIN		NAME	FUNCTION	REF SUPPLY	Type
MAX14918	MAX14918A				
22	22	V_{DD}	Linear Regulator Supply Input. Connect to 24V supply if powering V_5 with the internal 5V regulator. If the MAX14918 or MAX14918A is powered by an external 5V supply at the V_5 input, V_{DD} input must either be connected to GND or left unconnected. Bypass V_{DD} to GND using a 1µF ceramic capacitor.		Power
21	21	V_5	5V Supply Input or 5V Linear Regulator Output. Bypass V_5 to GND using a 1µF ceramic capacitor. V5 is the primary device supply and is required for normal operations.		Power
9	9	V_L	Logic Supply Input. Connect a voltage supply between 1.62V and 5.5V. Bypass V_L to GND using a 0.1µF ceramic capacitor.		Power
1, 2, 6, 7	1, 2, 6, 7	PGND	Power Ground. Connect PGND to GND and Exposed Pad (EP).		Ground
15	15	GND	Common ground for all power supplies, logic pins, and input signals. Connect to Exposed Pad.		Ground
24	24	OUT1	Low-Side Switch Output 1		Output
3	3	OUT2	Low-Side Switch Output 2		Output
5	5	OUT3	Low-Side Switch Output 3		Output
8	8	OUT4	Low-Side Switch Output 4		Output

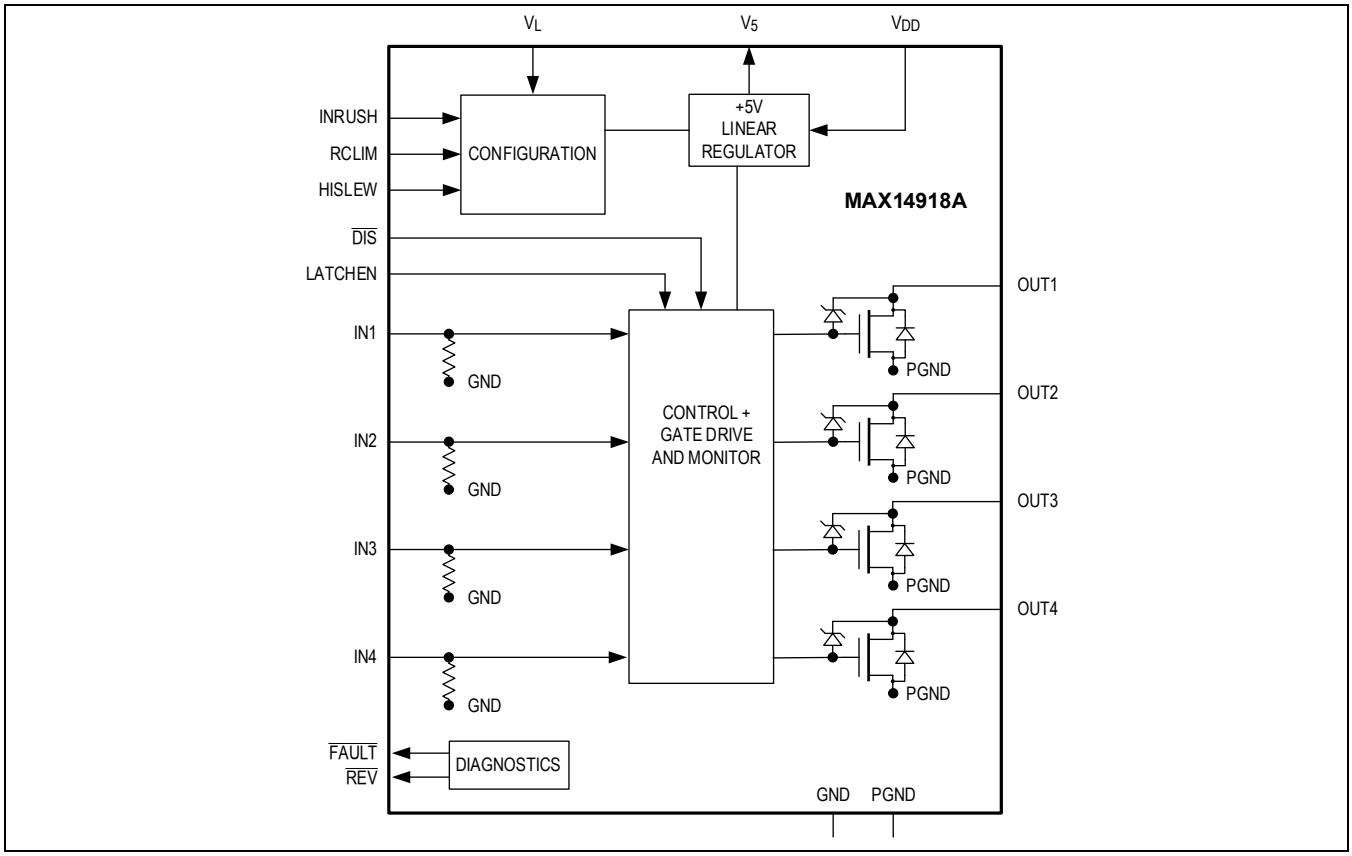
4	4	NC	No Connection		
18		$\overline{CS}$	Chip Select Input. Assert low to latch the input states and enable the SPI interface. Has a weak internal pullup.	VL	Logic Input
17		SCLK	Serial Clock Input. Has a weak internal pulldown.	VL	Logic Input
16		SDI	Serial Data Input. Data is clocked into SDI on the rising edge of SCLK. Has a weak internal pulldown.	VL	Logic Input
14		SDO	Serial Data Output. Data on SDO is updated on the falling edge of SCLK. SDO is three-stated with internal 100kΩ pulldown resistor when $\overline{CS}$ is high.	VL	Logic Output Push-Pull
13		$\overline{SPIFLT}$	SPI Fault. $\overline{SPIFLT}$ transitions low when a fault is detected on the SPI interface. Connect a pullup resistor to V_L.	VL	Logic Output Open-Drain
	18	IN1	Control Logic Input for OUT1. Has a weak internal pulldown. IN1-to-OUT1 control is transparent when LATCHEN is low.	VL	Logic Input
	17	IN2	Control Logic Input for OUT2. Has a weak internal pulldown. IN2-to-OUT2 control is transparent when LATCHEN is low.	VL	Logic Input
	16	IN3	Control Logic Input for OUT3. Has a weak internal pulldown. IN3-to-OUT3 control is transparent when LATCHEN is low.	VL	Logic Input
	14	IN4	Control Logic Input for OUT4. Has a weak internal pulldown. IN4-to-OUT4 control is transparent when LATCHEN is low.	VL	Logic Input
	13	LATCHEN	Set LATCHEN low for transparent IN_-to-OUT_ operation. Set LATCHEN high to latch the logic at the IN_ inputs. When LATCHEN is high, the OUT_ switches are not affected by the logic state change at the IN_ inputs. Has a weak internal pulldown.	VL	Logic Input
10	10	RCLIM	Global Current Limit Setting Resistor for OUT1 to OUT4. Place a resistor between RCLIM and GND to define maximum load current through the switches. See *Current Limiting* section for details.	V5	Analog Input
19	19	HISLEW	Slew Rate Setting Input. Drive HISLEW high to enable high slew rate on all outputs. Set HISLEW low for low slew rate. Has a weak internal pulldown.	VL	Logic Input
23	23	INRUSH	Inrush Current Enable Input. Drive INRUSH high to enable 2x current limiting for 10ms (min) after any switch is turned on. Drive INRUSH low to disable inrush current. Has a weak internal pulldown.	VL	Logic Input
20	20	$\overline{DIS}$	Drive $\overline{DIS}$ low to turn off all OUT_ switches, independent of the IN_ status (MAX14918A) or SPI setting (MAX14918). Has a weak internal pulldown.	VL	Logic Input
12	12	$\overline{FAULT}$	Global Open-Drain Fault Output. The $\overline{FAULT}$ output is low when the device detects a fault condition. See *Fault Signaling* section for all the conditions that assert the $\overline{FAULT}$ pin. Connect a pullup resistor to V_L.	VL	Logic Output Open-Drain
11	11	$\overline{REV}$	Reverse Current Gate Driver. $\overline{REV}$ is low when a reverse current is detected on any output. Connect $\overline{REV}$ to the gate of an external nMOS transistor for supply-load reverse-polarity protection.	V5	Logic Output Open-Drain
EP	EP	EP	Exposed Pad. Connect EP to GND.		

Functional Diagrams

MAX14918



MAX14918A


VL
V5
VDD
INRUSH
RCLIM
HISLEW
CONFIGURATION
+5V
LINEAR
REGULATOR
MAX14918A
DIS
LATCHEN
IN1
IN2
IN3
IN4
GND
CONTROL +
GATE DRIVE
AND MONITOR
PGND
OUT1
OUT2
OUT3
OUT4
FAULT
REV
DIAGNOSTICS
GND
PGND

Detailed Description

The MAX14918 and MAX14918A are quad 700mA low-side switches for industrial applications, featuring 140mΩ (typ) low on-resistance with integrated surge protection. The maximum load current through the switches are actively limited. The current limit can be set to meet different system needs and is resistor-settable between 100mA (typ) and 900mA (typ). The switch outputs are protected against short circuit to voltages in the range of 0V to 49V and are protected against thermal overload. Integrated line-to-GND surge protection of up to ±1.2kV/42Ω makes external TVS protection unnecessary.

The internal active clamps limit the OUT_ voltages to +55V (typ), enabling fast turn-off of inductive loads. The devices offer additional control for protection and diagnostics, including thermal overload, reverse-current detection, V_5 supply undervoltage detection, and faults on the RCLIM current-limit setting pin. For load that draws high inrush current, the MAX14918 and MAX14918A have the inrush mode, which provides double the current after switch turn-on for 10ms (min). The devices feature reverse-current detection which can be used to prevent damage caused by high reverse current resulting from field load and supply miswiring.

The MAX14918 has an SPI allowing control of multiple MAX14918 devices through a common daisy-chained SPI for high channel-count applications minimizing galvanic isolation requirements. Per-channel diagnostics are returned in the SPI readback. Data corruption on the SDI data is automatically detected and signaled on the $\overline{\text{SPIFLT}}$ output. See *Serial Peripheral Interface (MAX14918 Only)* section for information on configuring and reading diagnostics with single or daisy-chained devices.

The MAX14918A offers pin-based switch control with a latch option (LATCHEN), which reduces number of isolation channels through multiplexing of shared IN1 to IN4 control inputs while using LATCHEN signals as chip select inputs among multiple MAX14918A devices.

Output slew rate control (HISLEW) provides controlled turn-on edges to reduce LC oscillation due to long cables. A global $\overline{\text{DIS}}$ control signal allows quick turn-off of all OUT_ switches.

Power Supply Options with V_{DD} and V_5

The MAX14918 and MAX14918A offer flexible powering options. It can either be powered by V_{DD} or V_5. The V_{DD} supply supports a wide input range from +7V to +65V with a typical case of +24V field supply. The internal LDO regulator handles the wide input to provide a stable +5V output. Applications with limited power rails or unregulated supplies can power the MAX14918 and MAX14918A without the need of external power converters.

In the presence of a stable +5V external supply, the internal LDO can be bypassed, and the MAX14918 and MAX14918A are only powered by external +5V at the V_5 pin. When using the V_5 pin as the supply input, V_{DD} is grounded or left unconnected.

5V Linear Regulator

The integrated 5V linear regulator (V_5) can supply up to 35mA load current. Note that the linear regulator has high power dissipation when high load current is drawn while powered from high supply voltage. Calculate the power dissipation in the regulator as:

$$P_{DIS} = (V_{DD} - V_5) \times I_5$$

The power dissipation might be excessive with high V_5 load current in combination with high V_{DD} supply voltage, resulting in self-heating of the device. Care must be taken that the MAX14918 and MAX14918A maximum thermal ratings are not exceeded at the highest operating temperature. When the device enters thermal shutdown, the V_5 linear regulator is automatically turned off at junction temperature of 160°C (typ). The regulator turns on automatically when the junction temperature drops by 10°C (typ).

Logic Supply V_L

The logic supply V_L supports a wide voltage range of +1.62V to +5.5V. V_L can either be powered by V_5 or by external +1.8V or +3.3V supply to enable interfacing with microcontrollers, FPGAs, or digital isolators. The logic supply powers the digital interface and logic blocks of the MAX14918 and MAX14918A.

Undervoltage Lockout

When the V_{DD}, V_5, or V_L supply voltage is under their respective UVLO threshold, all OUT_ switches are off.

Current Limiting

The MAX14918 and MAX14918A feature resistor-settable active current limiting, common to all output switches (OUT1 to OUT4). When the current across the switch exceeds the current limit, the load current is limited by the low-side switch. The current limit can be set between 100mA (typ) and 900mA (typ) by R_{CLIM} resistor between RCLIM pin and GND. The equation to determine R_{CLIM} for a required I_{LIM} is:

$$R_{CLIM}\ (k\Omega) = \frac{V_{CLIM} \times K_1}{(I_{LIM} - K_2)(mA)}$$

where

V_{CLIM} = 1.165V (min), 1.2V (typ), 1.235V (max)

K_1 = 17260 (min), 18000 (typ), 19418 (max)

K_2 (mA) = -67.1 (min), 0 (typ), 36.98 (max)

The recommended R_{CLIM} is between 24kΩ and 100kΩ. Use the minimum value of V_{CLIM}, K_1 and K_2 to calculate the R_{CLIM} value associated with the minimum I_{LIM}. If no resistor is connected to the RCLIM pin or R_{CLIM} is more than 650kΩ (typ), I_{LIM} is internally set to 650mA (min). If the R_{CLIM} resistor is less than 6.5kΩ (typ), all OUT_ switches are turned off. The RCLIM pin is short-circuit protected.

For example, assuming the maximum operating load current of a system is less than 600mA, to ensure that the current limit is always higher than 600mA, the R_{CLIM} resistor is:

$$R_{CLIM}\ (k\Omega) = \frac{V_{CLIM} \times K_1}{(I_{LIM} - K_2)(mA)} = \frac{1.165 \times 17260}{(600 + 67.1)(mA)} = 30.14k\Omega$$

Fault Signaling

The $\overline{FAULT}$ pin is a global fault indication. It is an open-drain logic output that transitions low when the MAX14918 or MAX14918A detects a fault condition. When the device exits fault status and all switches are in normal operation, the $\overline{FAULT}$ pin transitions passive high. $\overline{FAULT}$ is asserted for any of the following conditions:

- Chip thermal shutdown
- Any of the OUT_ switches that are turned on are in thermal overload
- Reverse current detected at OUT_
- V_5 UVLO
- Short-circuit detected on the RCLIM pin

During power-up, $\overline{FAULT}$ is asserted until V_5 goes above its UVLO condition (V_{5_UVLO}). $\overline{FAULT}$ is asserted if any of the switches in ON state are in thermal overload or reverse current condition.

In addition to the open-drain $\overline{FAULT}$ pin, the MAX14918 also provides fault signaling through the SPI. See *MAX14918 Thermal Faults (FLT_ and LFLT_) on SDO* section on how real-time and latched faults are transmitted in each SPI transaction.

Chip Thermal Protection

The device temperature is constantly monitored when the MAX14918 and MAX14918A are powered up ($V_5 > V_{5\_UVLO}$). When the device die temperature rises above 150°C (T_{CSHDN}, typ), the device enters thermal shutdown, the global $\overline{FAULT}$ is asserted low, and all OUT_ switches are turned off until the chip temperature drops below 140°C ($T_{CSHDN} - T_{CSHDN\_HYS}$).

If the temperature of an output channel rises above 160°C (T_{JSHDN}), that output is turned off. When the per-channel temperature falls by the hysteresis amount of 15°C (T_{JSHDN_HYS}), the output is restored to normal operation.

The integrated LDO features a separate temperature sensor that monitors the temperature resulted from the LDO power dissipation. If the LDO temperature rises above 160°C (T_{DSHDN}), the LDO is turned off. It wakes up after cooling down by 10°C (T_{CSHDN_HYS}).

During normal operation, if any of the above temperature thresholds are triggered, the $\overline{FAULT}$ output transitions low.

INRUSH Mode

The MAX14918 and MAX14918A offer the inrush mode which supports loads that draw higher current during turn-on. In the inrush mode, each switch provides at least double the current set by the R_{CLIM} resistor for the inrush duration of 10ms (min) or 12.5ms (typ). After the inrush period, the switch current limit reverts to the value set by R_{CLIM}.

Global Disable ($\overline{DIS}$)

The MAX14918 and MAX14918A feature a global $\overline{DIS}$ input that turns off output switches (OUT1 to OUT4) regardless of its input state. When $\overline{DIS}$ transitions low, the outputs are in high-impedance within 100ns.

When $\overline{DIS}$ transitions high, all outputs are switched according to their associated input state. The disable and enable response times for the MAX14918 and MAX14918A are similar to the output turn-on and turn-off propagation delay times.

The disable output option is useful when the microcontroller or the FPGA has to intervene and quickly force all outputs off in the event of a fault.

Latch Enable (LATCHEN) (MAX14918A Only)

The latch enable input (LATCHEN) allows the MAX14918A to be used in transparent or hold mode. When the latch enable is high, the output is not affected by its associated input (IN_). When the latch enable is low, the input (IN_) to output (OUT_) control is transparent. The MAX14918A LATCHEN-to-OUT_ delay is the same as IN_-to-OUT_ delay specified in the *Electrical Characteristics*.

The LATCHEN input reduces number of isolation channels through multiplexing of shared IN1 to IN4 control inputs while using LATCHEN signals as chip select inputs among multiple MAX14918A devices. See *Figure 11* for details.

Output Slew Rate Control

The HISLEW pin controls the output turn-on edges. When the HISLEW input is low, output transitions are slower, and the MAX14918 and MAX14918A operate up to 50kHz switching frequency. The slow slew rate mode (HISLEW = low) is useful in applications where the load is capacitive and is connected through a long cable. The cable inductance and possible load capacitance generate LC oscillation during turn-on transitions. If the current during oscillation exceeds the reverse current detection threshold, it is detected as a reverse condition. The MAX14918 and MAX14918A force the $\overline{REV}$ pin low for 2 seconds, which is the auto-retry time (t_{REV_AR}). See *Reverse Current Detection* section for details. The slow slew rate during the output turn-on reduces the magnitude of LC oscillation and EMI.

When the HISLEW input is high, the output transitions are much faster, and the MAX14918 and MAX14918A can operate up to 500kHz switching frequency. This mode is useful in applications where the devices drive resistive loads.

Reverse Current Detection

The MAX14918 and MAX14918A feature reverse current detection, which is signaled by the $\overline{REV}$ logic output. A reverse current on any output (OUT_) can happen when the field supply is miswired with a reverse polarity. The device also protects against a direct reverse connection of the field supply between OUT_ and COM.

Reverse currents are drawn out of outputs (OUT_) when a negative voltage is applied across any OUT_ and COM with the OUT_ switch either in on or off state. If the reverse current flowing out of any output exceeds 150mA (typ), the $\overline{REV}$ output transitions low to signal a reverse current condition.

The MAX14918 and MAX14918A drive $\overline{REV}$ low and automatically turns off all four OUT_ switches when it detects a reverse current condition. The $\overline{REV}$ output is held low and all four output switches remain off for the auto-retry duration (t_{REV_AR}) of 2 seconds (typ) to protect against all possible reverse load miswiring combinations. After the auto-retry delay, the outputs are turned back to the state defined by the IN_ inputs (MAX14918A) or O_ bits (MAX14918), and $\overline{REV}$ is pulled high. If the cause for reverse current is still present and a reverse current is again detected, the auto-retry scheme turns $\overline{REV}$ low again, forcing all outputs off for 2s (t_{REV_AR}).

The $\overline{REV}$ output can drive the gate of an external nMOS which opens the PCB field ground to the field COM connection, thereby stopping the reverse current flow. The on-resistance of the external nMOS should be chosen such that it does not contribute significantly to a channel R_{ON} since all four output currents flow through the reverse-protecting nMOS. Its R_{ON} should be significantly less than one-fourth of the R_{ON} of the internal switch, which is less than 35mΩ (typ).

Transient Energy Protection

The MAX14918 and MAX14918A feature an integrated clamp at each of the four output channels. In typical applications, the integrated clamp eliminates the external clamp on each output, reducing component cost and saving board space. In case of an overvoltage event caused by surge, ESD, or inductive load turn-off, the clamp turns on at +55V (typ) to dissipate the energy.

Short-Circuit and Overcurrent Protection

The MAX14918 and MAX14918A outputs are designed to handle hard short-circuit as well as overcurrent. In case of a short-circuit at output (OUT_) to field supply with the switch turned on, the device actively limits the current to I_{LIM}. The temperature of the shorted channel increases at a rate determined by the power dissipation $V_{OUT\_}$ x I_{LIM}. The channel enters per-channel thermal shutdown when its temperature is above 160ºC (typ). After the channel cools down by 15°C (typ), the switch is automatically turned on if its associated IN_ input (MAX14918A) or O_ bit (MAX14918) is high. The MAX14918 and MAX14918A outputs indefinitely cycle in and out of thermal shutdown until the switch is turned off or the short circuit is removed.

Serial Peripheral Interface (MAX14918 Only)

The MAX14918 communicates with the host controller through a high-speed SPI. The interface has three logic inputs, Clock (SCLK), Chip Select ($\overline{CS}$), and Serial Data In (SDI), and one logic output Serial Data Out (SDO) (see *Figure 5*). Data at SDI is sampled on the rising edge of SCLK and data at SDO is updated on the falling edge of SCLK. SDO is three-stated when $\overline{CS}$ is high, allowing multiple SPI devices to share a common SPI host. The SPI complies with clock polarity CPOL = 0 and clock phase CPHA = 0. The maximum allowable SPI clock rate is 10MHz.

The outputs (OUT1 to OUT4) of the MAX14918 are configured through the SPI. The SPI frame is 8-bit long and is daisy-chainable allowing control of many MAX14918s through one SPI controller and a common chip-select signal.

SDI

The SDI frame consists of first four MSBs (O4 to O1) as output switch on or off configuration, and next four LSBs as even parity bits to check for SPI data integrity.

- O_ bits set the output switches on or off. Set O_ = 1 to close the switch (OUT_) and O_ = 0 to open the switch (OUT_)
- P_ are parity bits, which are calculated using the XOR function as follows:
  - PO = O1 ⊕ O3
  - PE = O2 ⊕ O4
  - PA = O1 ⊕ O2 ⊕ O3 ⊕ O4
  - PAn = NOT (O1 ⊕ O2 ⊕ O3 ⊕ O4)

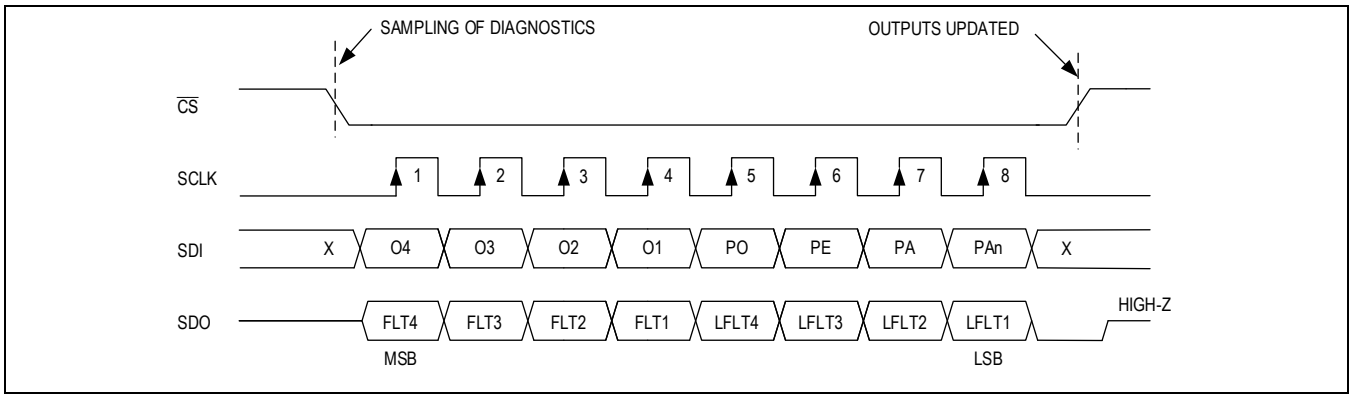


Figure 5. 8-bit SPI Frame for MAX14918 Configuration

After receiving the SDI, the MAX14918 verifies the data integrity. The parity bits are checked against the output configuration O_ bits (SDI [7:4]) for integrity. If the P_ bits (SDI [3:0]) do not match the result that the MAX14918 calculates on the received O_ bits, the outputs are not changed and the $\overline{SPIFLT}$ pin goes low. In addition, the MAX14918 checks if the number of received SCLK pulses is a multiple of 8. In the event of an error, the $\overline{SPIFLT}$ pin is set low.

MAX14918 Thermal Faults (FLT_ and LFLT_) on SDO

When the chip-select ($\overline{CS}$) transitions low, indicating the start of an SPI transaction, the MAX14918 samples internal diagnostics at this instant and sends real-time fault bits as the four MSBs on the SDO data frame (FLT4 to FLT1). The next four LSBs are latched version of the fault bits (LFLT4 to LFLT1).

The real-time faults and latched faults indicate the thermal overload of each channel based on the per-channel temperature sensor. The real-time faults (FLT_) are the real-time switch overload diagnostics, indicating a thermal overload on a switch in ON state. The FLT_ bits are sampled at starting of the $\overline{CS}$ falling edge. Latched faults (LFLT_) are the latched diagnostics that indicate per-channel thermal overload status between two SPI transactions. For an active channel x (Ox bit = high), if the thermal overload event briefly occurs and the condition is no longer present when the $\overline{CS}$ transitions low and the per-channel faults are sampled, the real-time fault bit FLTx is 0 as the overload condition is no longer present, but the latched fault bit LFLTx is set to 1, indicating a thermal overload event has occurred. LFLT_ are reset on SPI read or cleared on the following SPI transaction if the fault does not happen again before the following SPI transaction. Both FLT_ and LFLT_ are 0 when the OUT_ channel is off.

When the local temperature at a certain channel rises beyond T_{JSHDN} (160°C, typ), the real-time fault FLT_ and the latched fault LFLT_ are set. If the temperature cools down by T_{JSHDN_HYS} (15°C, typ), the real-time fault FLT_ goes low but the LFLT_ is latched high and is reset only after the end of each SPI transaction when the $\overline{CS}$ transitions high.

The LFLT_ is cleared at the end of the SPI transaction only if:

- The real-time version of the thermal overload has been cleared.
- The SPI transaction does not produce any errors that trigger $\overline{SPIFLT}$ low.

In case of an $\overline{SPIFLT}$ fault generated by any SPI transaction, the latched fault (LFLT_) bits are not cleared.

MAX14918 $\overline{SPIFLT}$ Signal

The $\overline{SPIFLT}$ signal is asserted low for two different conditions:

- The parity bits calculated by the MAX14918 differ from the ones transmitted by the SPI controller (see *Figure 6*).
- The number of SCLK pulses sent by the SPI controller is not a multiple of 8 (see *Figure 7*).

The $\overline{SPIFLT}$ is asserted after the rising edge of the $\overline{CS}$ signal.

In between two SPI transactions, SPI clock pulses are ignored when $\overline{CS}$ is de-asserted (high). SCLK must idle low when $\overline{CS}$ is asserted. Otherwise, the $\overline{SPIFLT}$ is asserted at the end of SPI transaction, as the first falling edge of the SCLK after $\overline{CS}$ is asserted is used to count the number of clock pulses recorded in a single SPI transaction.

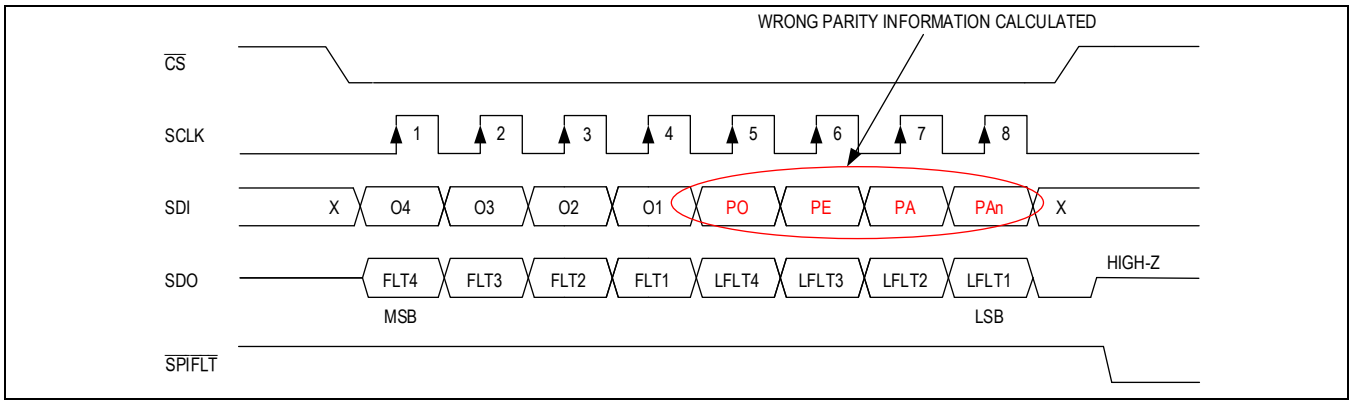


Figure 6. $\overline{SPIFLT}$ Signaling Due to Incorrect Parity Bits on SDI

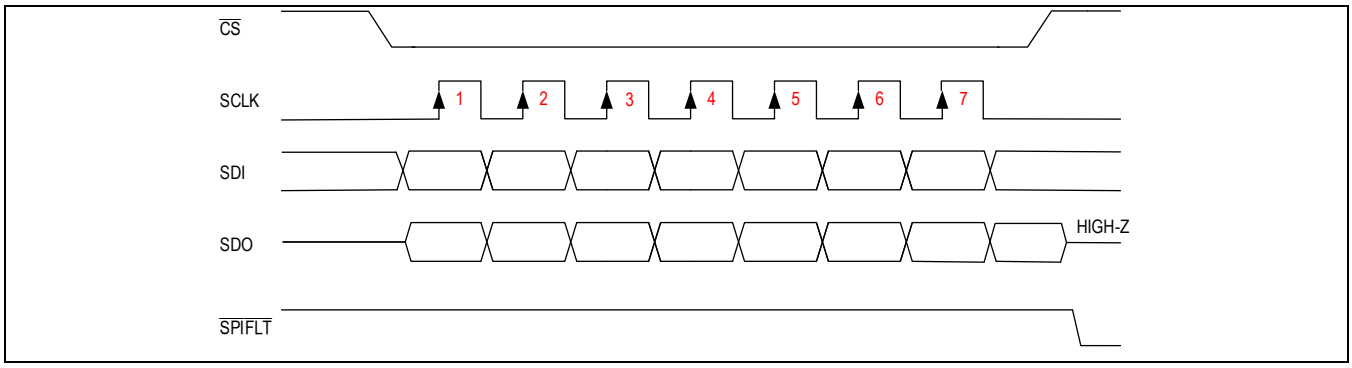


Figure 7. SPIFLT Signaling Due to Incorrect Number of SCLK Pulses

Daisy-Chaining Multiple MAX14918 Devices

When daisy-chaining multiple MAX14918 devices, the MOSI output from the controller is connected to the SDI of the first MAX14918 device, the SDO of this device is connected to the SDI of the next MAX14918. The final MAX14918 SDO is connected to the MISO input of the controller. For all the MAX14918 devices in daisy chain, the SCLK and CS signals are common. See *Figure 8* for daisy-chaining diagram of four MAX14918 devices.

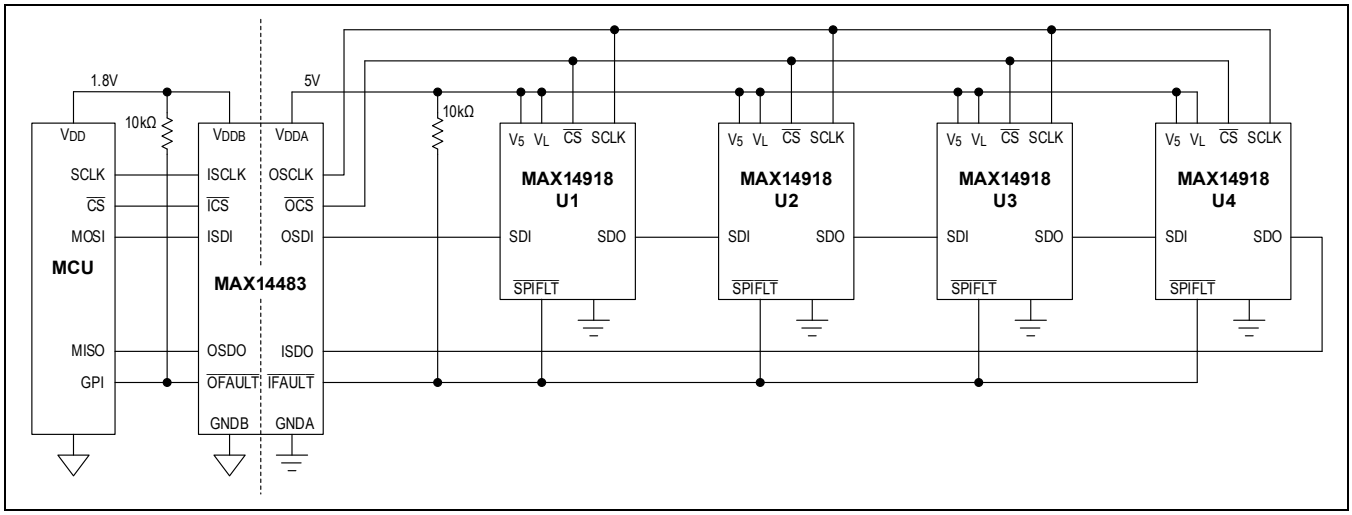


Figure 8. Daisy-Chain, Isolated 16-Channel Low-Side Digital Output

Figure 9 shows the command sequence to configure the four MAX14918 devices (U1 to U4) with DATA-4, DATA-3, DATA-2, and DATA-1.

The DATA-x configures a given device that contains the output configuration O_ bits followed by the parity bits. In the figure, DATA-4 configures the U4 device, DATA-3 configures the U3 device, DATA-2 configures the U2 device, and DATA-1 configures the U1 device.

During the first set of 8 SCLK pulses, DATA-4 is loaded in the shift register of U1. With CS remaining low, this data propagates through U1 and is the output at SDO1 during the next set of 8 SCLK pulses. The per-channel diagnostics of the four devices are generated at its respective SDO during the first set of 8 SCLK pulses. The U4 diagnostic data at SDO4 are sent to the MISO input of the controller.

During the second set of 8 SCLK pulses, the data from SDO1 moves into SDI2, and DATA_4 is loaded into U2 shift register. Simultaneously, a new command, DATA-3 gets loaded in U1 shift register, thus overwriting the previous command. During this 8 SCLK pulses, the per-channel diagnostics get shifted to next device SDO in the chain. The U3 diagnostic data is shifted to SDO4, which is connected to the MISO input of the controller.

In the fourth set of 8 SCLK pulses, the first command DATA-4 is loaded into U4 shift register. The second command DATA-3 gets loaded into U3 and the third command DATA-2 is loaded into U2. The device U1 receives a new command, DATA-1. All four devices now have its respective command, and all the per-channel diagnostics have been shifted to SDO4 connected to MISO input of the controller. When $\overline{CS}$ goes high, the loaded configuration of the four devices are executed simultaneously.

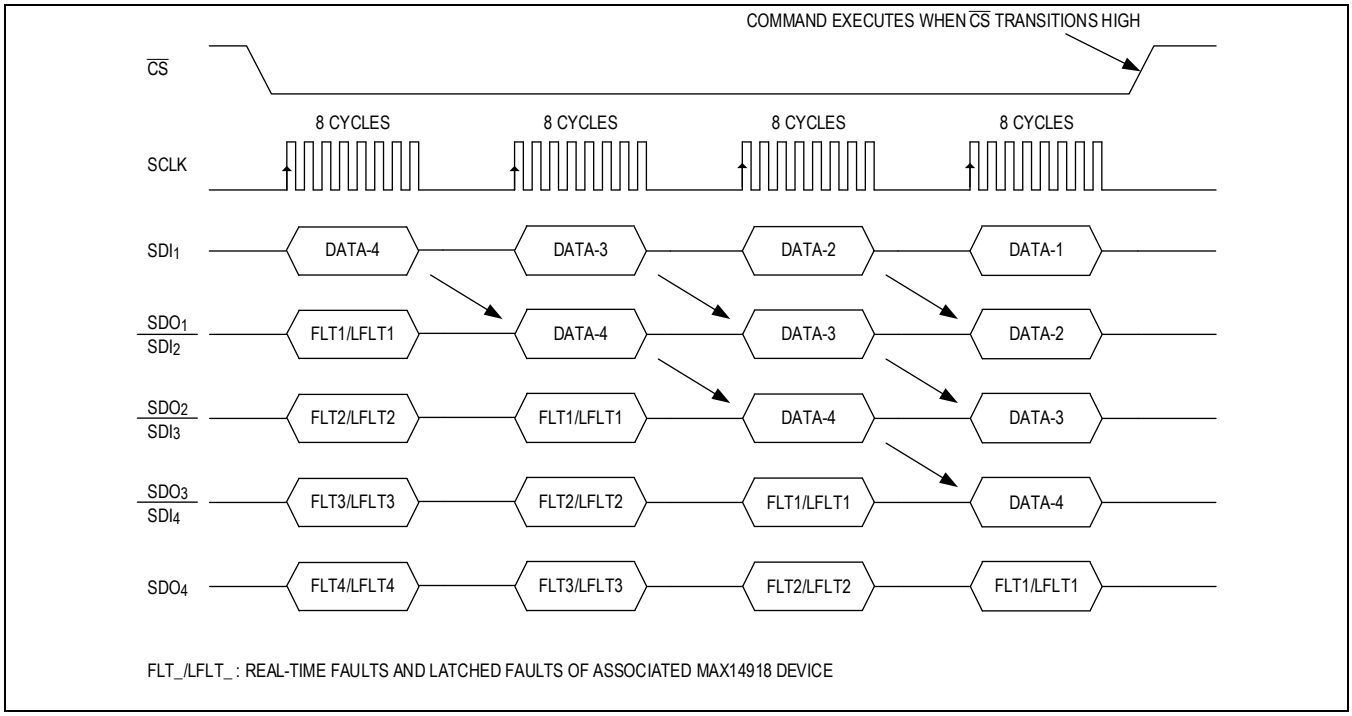


Figure 9. Daisy Chain Command Sequence for Four Devices

Applications Information

Paralleling the Outputs

The MAX14918 and MAX14918A support paralleling of output channels in applications requiring a higher load current. For the MAX14918A, when paralleling multiple channels, connect the inputs (IN_) of the paralleled channels together and the corresponding outputs (OUT_) together.

When multiple outputs are connected in parallel, the resulting current limit is the sum of each output's current limit. For example, paralleling of two channels doubles the available load current. When multiple outputs are paralleled, an external TVS diode (Z_D) might be required per output to dissipate high energy during inductive load turn-off. The clamp voltage of the external TVS diode must be lower than the minimum internal clamp voltage (+49V).

See application note *Increasing Output Current by Paralleling Multiple Channels of MAX14919/MAX14919A* for information on how to design the protection circuit when paralleling multiple channels for higher load current.

PCB Layout

High-current low R_{ON} switches require proper layout to achieve optimal performance. Ensure that power-supply bypass capacitors are placed as close to the device as possible. A 1µF low-ESL/ESR capacitor is placed as close to the V_{DD} pin as possible. Ensure that the PGND and GND pins are interconnected to achieve the least board resistance.

Connect the exposed pad to a large GND plane to dissipate heat in case of large load current. Maximize the metal coverage for all layers, especially for top and bottom layers to optimize the heat conduction and dissipation. Maximize the number of thermal vias under the exposed pad ("via farm") to further enhance the vertical heat transfer through the PCB.

Surge Protection

Each output of the MAX14918 and MAX14918A is protected against IEC 61000-4-5 1.2µs/50µs surges of up to ±1.2kV/(42Ω + 0.5µF) line-to-ground without the need for external protection diodes from OUT_ to PGND. When using an external nMOS for reverse current protection, a TVS diode is necessary to be placed in parallel to the external nMOS to protect it from overvoltage due to surge events. The TVS diode clamping voltage should be below the maximum V_{DS} of the external nMOS. It should be able to withstand the surge energy from all channels.

Inductive Load Demagnetization

During inductive load turn-off by a low-side switch, the kickback voltage generated by the inductive load is clamped by the internal clamp to a voltage of +55V (typ) relative to PGND allowing fast demagnetization. Larger load inductance and higher load current increase the time for the inductor to be demagnetized. Since large energy is dissipated in the device through the voltage clamp, care must be taken to calculate and maintain the maximum allowable load inductance and operating current. Otherwise, excessive energy could damage the device. Each switch is able to dissipate up to 200mJ of clamp energy during inductive load clamping at +125ºC junction temperature (T_J). The $\overline{FAULT}$ pin, FLT_ bits, and LFLT_ bits are not asserted during the inductive load demagnetization.

Typical Application Circuits

Isolated Four-Channel Digital Output with Reverse Protection Using MAX14918

Figure 10 illustrates an isolated, SPI-controlled, field-powered, four-channel low-side digital output with reverse polarity protection and 700mA current limit. An external nMOS (i.e., NTTFS5820NLTAG) with the $\overline{REV}$ connected to its gate provides reverse polarity protection by cutting off the reverse current through the device. The unipolar TVS (i.e., SMCJ36A) protects the external nMOS during surge events.

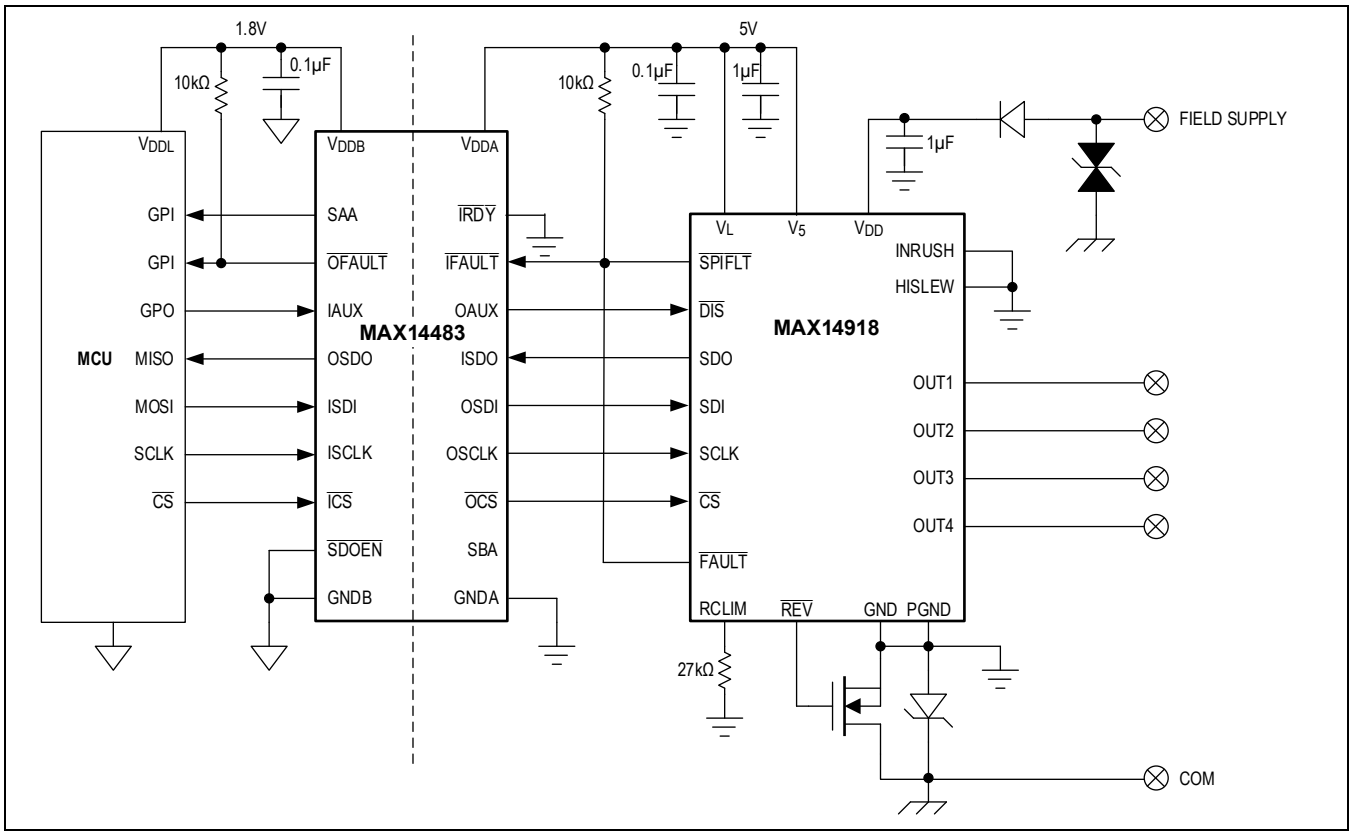


Figure 10. Isolated Four-Channel Digital Output with Reverse Protection Using MAX14918

Isolated 16-Channel Digital Output Using MAX14918A with Shared IN_ Pins

Figure 11 illustrates an isolated 16-channel low-side digital output with simplified isolation using four MAX14918A devices. The IN_ control signals are shared across four MAX14918A devices. Isolated LATCHEN signals are served as chip select signals to enable multiplexing of shared IN1 to IN4 signals among four MAX14918A devices, reducing the number of isolation channels from 16 to 8.

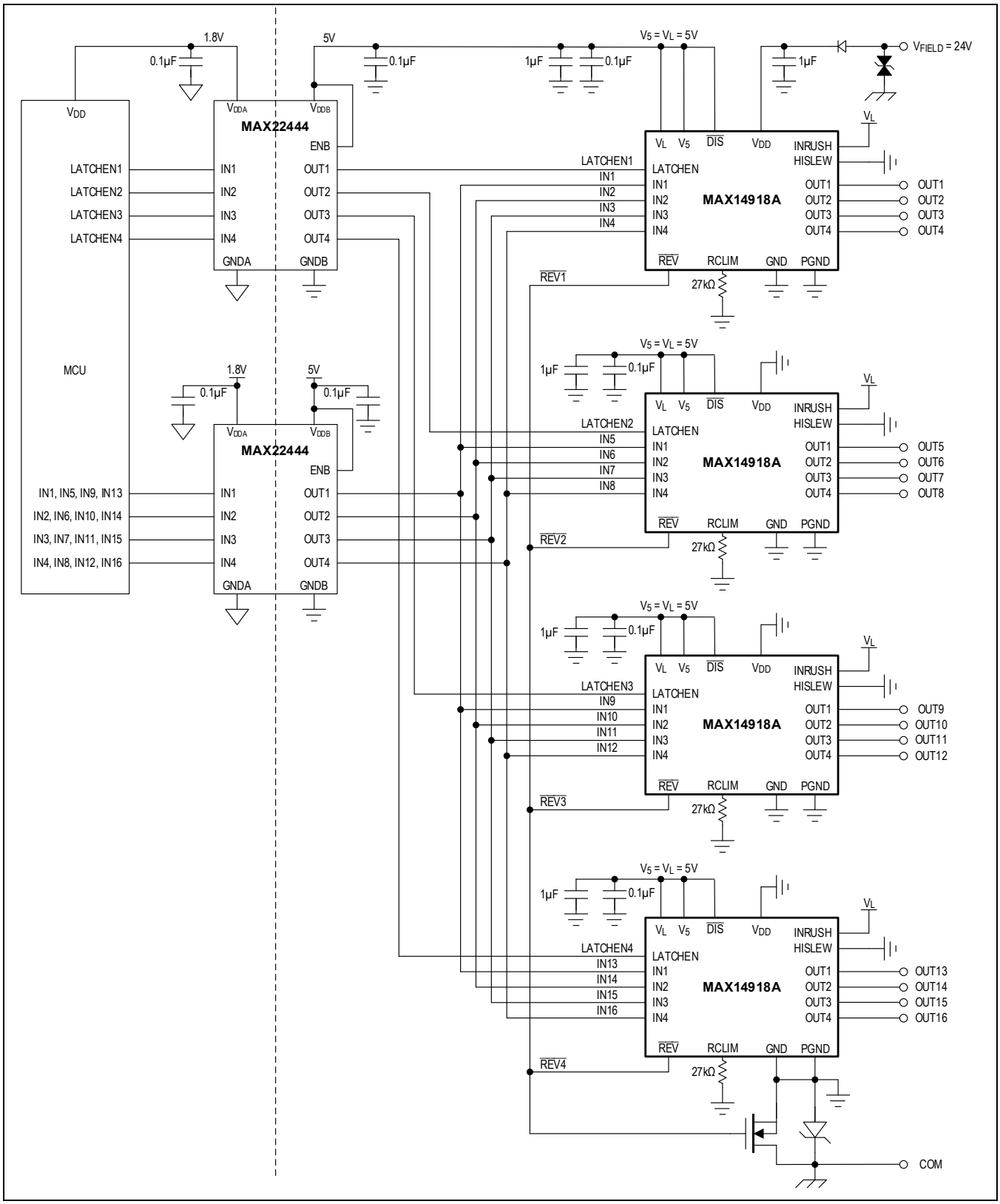


Figure 11. Isolated 16-Channel Digital Output Using MAX14918A with Shared IN_ Pins

Ordering Information

PART NUMBER	INTERFACE	TEMPERATURE RANGE	PIN-PACKAGE
MAX14918ATG+	SPI	-40°C to +125°C	24 TQFN-EP
MAX14918ATG+T	SPI	-40°C to +125°C	24 TQFN-EP
MAX14918AATG+	Parallel	-40°C to +125°C	24 TQFN-EP
MAX14918AATG+T	Parallel	-40°C to +125°C	24 TQFN-EP

+Denotes lead(Pb)-free/RoHS-compliance.

T = Tape and reel.

EP = Exposed pad.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	05/23	Release for Market Intro	—
1	09/23	Updated General Description, Benefits and Features, Absolute Maximum Ratings, and Electrical Characteristics table; added Figure 4; updated TOC06, TOC07 and TOC09; updated Detailed Description and Current Limiting section; removed future asterisks on MAX14918AATG+ and MAX14918AATG+T	1, 2, 5, 6, 8, 9, 17, 18, 27