Quad 40V<sub>IN</sub>, Silent Switcher μModule Regulator with Configurable 3A Output Array

**FEATURES**
- Four Complete Step-Down Switching Power Supplies
- Low Noise Silent Switcher® Architecture
- CISPR22 Class B Compliant
- CISPR25 Class 5 Compliant
- Wide Input Voltage Range: 3V to 40V
- Wide Output Voltage Range: 0.8V to 8V
- 3A Continuous Output Current per Channel at 12V<sub>IN</sub>, 3.3V<sub>OUT</sub>, T<sub>A</sub> = 80°C
- 4A Continuous Output Current per Channel at 12V<sub>IN</sub>, 3.3V<sub>OUT</sub>, f<sub>SW</sub> = 2MHz, T<sub>A</sub> = 60°C
- Multiphase or Multi-μModule Parallelable for Increased Output Current
- Low Thermal Resistance, θ<sub>JA</sub> = 8.4°C/W, θ<sub>JCtop</sub> = 5.0°C/W, θ<sub>JCbot</sub> = 1.8°C/W
- Selectable Switching Frequency: 200kHz to 3MHz
- Compact Package

**APPLICATIONS**
- Automated Test Equipment
- Industrial Supplies
- Medical Equipment

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**DESCRIPTION**

The LTM<sup>®</sup>8060 is quad 40V<sub>IN</sub>, 3A step-down Silent Switcher μModule<sup>®</sup> regulator. The Silent Switcher architecture minimizes EMI while delivering high efficiency at frequencies up to 3MHz. Included in the package are the controllers, power switches, inductors, and support components. Operating over a wide input voltage range, the LTM8060 supports output voltages from 0.8V to 8V, and a switching frequency range of 200kHz to 3MHz, each set by a single resistor. Only the bulk input and output filter capacitors, are needed to finish the design. The LTM8060 product video is available on website.

The LTM8060 is packaged in a compact (11.9mm × 16mm × 3.32mm) over-molded Ball Grid Array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8060 is available with SnPb (BGA) or RoHS compliant.

**Configurable Output Array**

The LTM8060 outputs can be paralleled in an array for up to 12A capability.

3A 3A 6A 9A 12A

**TYPICAL APPLICATION**

Quad 3A Output from 8.5V to 40V Input

Efficiency, V<sub>IN</sub> = 24V, BIAS = 5V

Click to view associated Video Design Idea.
LTM8060

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

- \( V_{INn}, RUNn, PGn \) .............................................42V
- \( V_{OUTn}, BIASn, AUXn \) .............................................10V
- \( FBn, TRSSn, SHAREn, RTn \) .....................................4V
- \( SYNCn \) ..............................................................6V

Maximum Internal Temperature (Note 2) ..................125°C
Storage Temperature ........................................–55°C to 125°C
Peak Solder Reflow Package Body Temperature ..........245°C

**PIN CONFIGURATION**

![Pin Configuration Diagram]

**ORDER INFORMATION**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>BALL FINISH</th>
<th>PART MARKING*</th>
<th>PACKAGE TYPE</th>
<th>MSL RATING</th>
<th>TEMPERATURE RANGE (SEE NOTE 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTM8060EY#PBF</td>
<td>SAC305 (RoHS)</td>
<td>LTM8060Y e1</td>
<td>BGA</td>
<td>4</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTM8060IY#PBF</td>
<td>SAC305 (RoHS)</td>
<td>LTM8060Y e0</td>
<td>BGA</td>
<td>4</td>
<td>–40°C to 125°C</td>
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<tr>
<td>LTM8060IY</td>
<td>SAC305 (RoHS)</td>
<td>LTM8060IY</td>
<td>BGA</td>
<td>4</td>
<td>–40°C to 125°C</td>
</tr>
</tbody>
</table>

- Device temperature grade is indicated by a label on the shipping container.
- Pad code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow.
- This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

NOTE:
1) \( \theta \) VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS;
2) \( \theta_{JA} \) VALUE IS OBTAINED WITH DEMO BOARD;
3) REFER TO PAGES 7, 8, 9 AND 17 FOR LAB MEASUREMENT AND DERATING INFORMATION.
### ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating internal temperature range, otherwise specifications are at $T_A = 25^\circ C$. $V_{IN}\bar{n} = 12V$, RUN$n = 2V$ unless otherwise noted (Notes 2, 3).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>Minimum $V_{IN}$ Input Voltage</td>
<td>$V_{IN} = 3V$</td>
<td>●</td>
<td>3.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Minimum $V_{IN2}$ Input Voltage</td>
<td>●</td>
<td>3.0</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td>Minimum $V_{IN3}$ Input Voltage</td>
<td>●</td>
<td>2.0</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output DC Voltage</td>
<td>FB$n$ open</td>
<td>0.8</td>
<td>0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FB$n = 21.5k\Omega$</td>
<td>10</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Maximum Output DC Current</td>
<td>(Note 4)</td>
<td>6</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Quiescent Current into $V_{IN}$</td>
<td>RUN$n = 0$, BIAS$n = 5V$, SYNC$n = 3.3V$, No load</td>
<td>7</td>
<td>8</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Current into BIAS$n$</td>
<td>RUN$n = 0$, BIAS$n = 5V$, BIAS$n = 5V$, SYNC$n = 3.3V$, No load</td>
<td>0.5</td>
<td>18</td>
<td>μA</td>
<td></td>
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<tr>
<td>Line Regulation</td>
<td>$5V &lt; V_{IN} &lt; 40V$, I$_{OUT}$ = 1A</td>
<td>0.05</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$12V_{IN}$, 0.1A &lt; I$_{OUT}$ &lt; 4A</td>
<td>0.1</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Output RMS Ripple</td>
<td>$3.3V_{OUT}$, I$_{OUT}$ = 4A</td>
<td>10</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>FB$n$ Voltage</td>
<td>⧲</td>
<td>792</td>
<td>800</td>
<td>808</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>⧲</td>
<td>784</td>
<td>800</td>
<td>816</td>
<td>mV</td>
</tr>
<tr>
<td>Current out of FB$n$</td>
<td>$V_{OUT}$ = 1V, FB$n$ = 0V</td>
<td>4</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Minimum BIAS$n$ for Proper Operation</td>
<td></td>
<td></td>
<td>3.2</td>
<td>V</td>
<td></td>
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<tr>
<td>Switching Frequency</td>
<td>RT$n = 200k\Omega$</td>
<td>200</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RT$n = 35.7k\Omega$</td>
<td>1</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RT$n = 8.06k\Omega$</td>
<td>3</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RUN$n$ Threshold</td>
<td></td>
<td>0.74</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>RUN$n$ Input Current</td>
<td>RUN$n = 0V$</td>
<td>100</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>PG$n$ Threshold at FB$n$</td>
<td>Lower Threshold</td>
<td>740</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Upper Threshold</td>
<td>860</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>PG$n$ Output Sink Current</td>
<td>PG$n = 0.1V$</td>
<td>100</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>CLKOUT$n$ $V_{OL}$</td>
<td></td>
<td>0.2</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CLKOUT$n$ $V_{OH}$</td>
<td></td>
<td>3.2</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>SYNC$n$ Input High Threshold</td>
<td></td>
<td>1.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>SYNC$n$ Input Low Threshold</td>
<td></td>
<td>0.8</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>SYNC$n$ Threshold to Enable Spread Spectrum</td>
<td></td>
<td>2.8</td>
<td>4.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>SYNCl Current</td>
<td>SYNCl = 6V</td>
<td></td>
<td>60</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>TRSS$n$ Source Current</td>
<td>TRSS$n = 0V$</td>
<td></td>
<td>2</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>TRSS$n$ Pull-Down Resistance</td>
<td>Fault Condition, TRSS$n = 0.1V$</td>
<td></td>
<td>200</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTM8060E is guaranteed to meet performance specifications from $0^\circ C$ to $125^\circ C$ internal. Specifications over the full $-40^\circ C$ to $125^\circ C$ internal operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** $n$ Represents each individual channel. Four outputs are tested separately and the same testing condition is applied to each output.

**Note 4:** The maximum current out of any channel may be limited by the internal temperature of the LTM8060. See output current derating curves for different $V_{IN}$, $V_{OUT}$ and $T_A$.

The LTM8060I is guaranteed to meet specifications over the full $-40^\circ C$ to $125^\circ C$ internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.
TYPICAL PERFORMANCE CHARACTERISTICS \( T_A = 25^\circ \text{C} \), operating per Table 1, unless otherwise noted.

Efficiency and Power Loss
\( V_{OUT} = 0.8\text{V}, \text{BIAS} = 5\text{V}, \text{Burst Mode} \)

Efficiency and Power Loss
\( V_{OUT} = 1\text{V}, \text{BIAS} = 5\text{V}, \text{Burst Mode} \)

Efficiency and Power Loss
\( V_{OUT} = 1.2\text{V}, \text{BIAS} = 5\text{V}, \text{Burst Mode} \)

Efficiency and Power Loss
\( V_{OUT} = 1.5\text{V}, \text{BIAS} = 5\text{V}, \text{Burst Mode} \)

Efficiency and Power Loss
\( V_{OUT} = 1.8\text{V}, \text{BIAS} = 5\text{V}, \text{Burst Mode} \)

Efficiency and Power Loss
\( V_{OUT} = 2\text{V}, \text{BIAS} = 5\text{V}, \text{Burst Mode} \)

Efficiency and Power Loss
\( V_{OUT} = 2.5\text{V}, \text{BIAS} = 5\text{V}, \text{Burst Mode} \)

Efficiency and Power Loss
\( V_{OUT} = 3.3\text{V}, \text{BIAS} = 5\text{V}, \text{Burst Mode} \)

Efficiency and Power Loss
\( V_{OUT} = 5\text{V}, \text{BIAS} = 5\text{V}, \text{Burst Mode} \)
Efficiency and Power Loss

\[ V_{OUT} = 8V, BIAS = 5V, \text{ Burst Mode} \]

- 12V\textsubscript{IN}
- 24V\textsubscript{IN}
- 36V\textsubscript{IN}

Input vs Load Current, \( V_{OUT} = 0.8V \)

- 12V\textsubscript{IN}
- 24V\textsubscript{IN}
- 36V\textsubscript{IN}

Input vs Load Current, \( V_{OUT} = 1V \)

- 12V\textsubscript{IN}
- 24V\textsubscript{IN}
- 36V\textsubscript{IN}

Input vs Load Current, \( V_{OUT} = 1.2V \)

- 12V\textsubscript{IN}
- 24V\textsubscript{IN}
- 36V\textsubscript{IN}

Input vs Load Current, \( V_{OUT} = 1.5V \)

- 12V\textsubscript{IN}
- 24V\textsubscript{IN}
- 36V\textsubscript{IN}

Input vs Load Current, \( V_{OUT} = 1.8V \)

- 12V\textsubscript{IN}
- 24V\textsubscript{IN}
- 36V\textsubscript{IN}

Input vs Load Current, \( V_{OUT} = 2V \)

- 12V\textsubscript{IN}
- 24V\textsubscript{IN}
- 36V\textsubscript{IN}

Input vs Load Current, \( V_{OUT} = 2.5V \)

- 12V\textsubscript{IN}
- 24V\textsubscript{IN}
- 36V\textsubscript{IN}

Input vs Load Current, \( V_{OUT} = 3.3V \)

- 12V\textsubscript{IN}
- 24V\textsubscript{IN}
- 36V\textsubscript{IN}
TYPICAL PERFORMANCE CHARACTERISTICS  $T_A = 25^\circ\text{C}$, operating per Table 1, unless otherwise noted.

- **Input vs Load Current, $V_{OUT} = 5\text{V}$**
  - BIAS = 5V, Burst Mode

- **Input vs Load Current, $V_{OUT} = 8\text{V}$**
  - BIAS = 5V, Burst Mode

- **Derating, $V_{OUT} = 0.8\text{V}$**
  - BIAS = 5V, DC2820A Demo Board
  - $T_J = 120^\circ\text{C}$, Burst Mode
  - All Channels at Same Load

- **Derating, $V_{OUT} = 1\text{V}$**
  - BIAS = 5V, DC2820A Demo Board
  - $T_J = 120^\circ\text{C}$, Burst Mode
  - All Channels at Same Load

- **Derating, $V_{OUT} = 1.2\text{V}$**
  - BIAS = 5V, DC2820A Demo Board
  - $T_J = 120^\circ\text{C}$, Burst Mode
  - All Channels at Same Load

- **Derating, $V_{OUT} = 1.5\text{V}$**
  - BIAS = 5V, DC2820A Demo Board
  - $T_J = 120^\circ\text{C}$, Burst Mode
  - All Channels at Same Load

- **Derating, $V_{OUT} = 1.8\text{V}$**
  - BIAS = 5V, DC2820A Demo Board
  - $T_J = 120^\circ\text{C}$, Burst Mode
  - All Channels at Same Load

- **Derating, $V_{OUT} = 2\text{V}$**
  - BIAS = 5V, DC2820A Demo Board
  - $T_J = 120^\circ\text{C}$, Burst Mode
  - All Channels at Same Load

- **Derating, $V_{OUT} = 2.5\text{V}$**
  - BIAS = 5V, DC2820A Demo Board
  - $T_J = 120^\circ\text{C}$, Burst Mode
  - All Channels at Same Load

For more information [www.analog.com](http://www.analog.com)
TYPICAL PERFORMANCE CHARACTERISTICS \( T_A = 25^\circ C \), operating per Table 1, unless otherwise noted.

Derating, \( V_{OUT} = 3.3V \)
BIAS = 5V, DC2820A Demo Board
\( T_J = 120^\circ C \), Burst Mode
All Channels at Same Load

Derating, \( V_{OUT} = 3.3V \), \( f_{SW} = 2MHz \)
BIAS = 5V, DC2820A Demo Board
\( T_J = 120^\circ C \), Burst Mode
All Channels at Same Load

Derating, \( V_{OUT} = 5V \)
BIAS = 5V, DC2820A Demo Board
\( T_J = 120^\circ C \), Burst Mode
All Channels at Same Load

Derating with Airflow
\( 12V_{IN} \) to 1.5\( V_{OUT} \), \( T_J = 120^\circ C \)
BIAS = 5V, DC2820A Demo Board
Forced Continuous Mode
All Channels at Same Load

Derating with Airflow
\( 36V_{IN} \) to 1.5\( V_{OUT} \), \( T_J = 120^\circ C \)
BIAS = 5V, DC2820A Demo Board
Forced Continuous Mode
All Channels at Same Load

Derating with Airflow
\( 12V_{IN} \) to 3.3\( V_{OUT} \), \( T_J = 120^\circ C \)
BIAS = 5V, DC2820A Demo Board
Forced Continuous Mode
All Channels at Same Load
For more information www.analog.com
TYPICAL PERFORMANCE CHARACTERISTICS  \( T_A = 25^\circ C \), operating per Table 1, unless otherwise noted.

**BIAS Current vs Frequency**

12\(V_{IN} \) to 3.3\(V_{OUT} \)

Forced Continuous Mode

**Dropout Voltage vs Load Current**

**Input Current vs \( V_{IN} \)**

\( V_{OUT} \) Short Circuited

**Single Channel Derating, \( V_{OUT} = 1.5 \) \(V\) CH1 ON, CH2/CH3/CH4 OFF**

BIAS = 5\(V\), DC2820A Demo Board

\( T_J = 120^\circ C \), Burst Mode

**Single Channel Derating, \( V_{OUT} = 3.3 \) \(V\) CH1 ON, CH2/CH3/CH4 OFF**

BIAS = 5\(V\), DC2820A Demo Board

\( T_J = 120^\circ C \), Burst Mode

**Single Channel Derating, \( V_{OUT} = 5 \) \(V\) CH1 ON, CH2/CH3/CH4 OFF**

BIAS = 5\(V\), DC2820A Demo Board

\( T_J = 120^\circ C \), Burst Mode

**Dual Channel Derating, \( V_{OUT} = 1.5 \) \(V\) CH1/CH3 ON, CH2/CH4 OFF**

BIAS = 5\(V\), DC2820A Demo Board

\( T_J = 120^\circ C \), Burst Mode

**Dual Channel Derating, \( V_{OUT} = 3.3 \) \(V\) CH1/CH3 ON, CH2/CH4 OFF**

BIAS = 5\(V\), DC2820A Demo Board

\( T_J = 120^\circ C \), Burst Mode

**Dual Channel Derating, \( V_{OUT} = 5 \) \(V\) CH1/CH3 ON, CH2/CH4 OFF**

BIAS = 5\(V\), DC2820A Demo Board

\( T_J = 120^\circ C \), Burst Mode

For more information [www.analog.com](http://www.analog.com)
PIN FUNCTIONS

**VIN1 (Bank 6):** Input power for the channel 1 regulator. The VIN1 powers the internal control circuitry for channel 1/2 and is monitored by undervoltage lockout circuitry. The VIN1 voltage must be greater than 3V for either channel 1/2 of the LTM8060 to operate. Decouple VIN1 to ground with an external, low ESR capacitor. See Table 1 for recommended values.

**VIN2 (Bank 4):** Input power for the channel 2 regulator. Decouple VIN2 to ground with an external, low ESR capacitor. See Table 1 for recommended values.

**VIN34 (Bank 5):** Input power for the channel 3/4 regulator. The VIN34 bank powers the internal control circuitry for both channel 3/4 and is monitored by undervoltage lockout circuitry. The VIN34 voltage must be greater than 3V for either channel 3/4 of the LTM8060 to operate. Decouple VIN34 to ground with an external, low ESR capacitor. See Table 1 for recommended values.

**GND (Bank 2):** Tie these GND pins to a local ground plane below the LTM8060 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8060 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider (RFB) to this net.

**VOUT1/2/3/4 (Banks 8/3/1/7):** Power output for Channel 1/2/3/4, Respectively. Apply the output filter capacitor and the output load between these pins and GND plane.

**AUX1/2/3/4 (Pins N10/L10/C2/E2):** Low Current Voltage Source for BIAS. In many designs, the BIAS pin is simply connected to VOUT by way of the AUX pin. The AUXp pins are internally connected to VOUT and placed adjacent to the BIASp pins to ease printed circuit board routing. Although these pins are internally connected to VOUT, it is not intended to deliver a higher current, so do NOT connect these pins to the load. If these pins are not tied to BIAS, leave it floating.

**BIAS12/34 (Pins M10/D2):** The internal regulator will draw current from BIASp instead of VIN1 or VIN34 when BIASp is tied to a voltage higher than 3.2V. For output voltages of 3.3V and above these pins should be tied to VOUTn. If these pins are tied to a supply other than VOUTn use a local bypass capacitor on these pins.

**SYNC12/34 (Pins C11/N1):** External Clock Synchronization Input. Ground these pins for low ripple Burst Mode® operation at low output loads; this will also disable the CLKOUT function. Apply a DC voltage between 2.8V and 4V for forced continuous mode operation with spread spectrum modulation. Float the SYNCn pin for forced continuous mode operation without spread spectrum modulation. Apply a clock source to the SYNCn pin for synchronization to an external frequency. The LTM8060 will be in forced continuous mode when an external frequency is applied.

**CLKOUT12/34 (Pins C10/N2):** Synchronization Output. When SYNC12/34 > 2.8V, the CLKOUT12/34 pins provide a waveform about 90 degrees out-of-phase with Channel 1/3, respectively. This allows synchronization with other regulators with up to four phases. When an external clock is applied to the SYNC12/34 pins, the CLKOUT12/34 pins will output a waveform with about the same phase, duty cycle, and frequency as the SYNC12/34 waveform. In Burst Mode operation, the CLKOUT12/34 pins will be internally grounded. Float these pin if the CLKOUT12/34 function is not used. Do not drive these pins.

**FB1/2/3/4 (Pins K11/K10/F1/F2):** The LTM8060 regulates the FBn pin to 800mV. Connect the feedback resistor to this pin to set the output voltage.

**RT12/34 (Pins L11/E1):** Connect a resistor between RTn and ground to set the switching frequency. Do not drive these pins.

**RUN1/2/3/4 (Pins E11/D11/L1/M1):** The corresponding channel of the LTM8060 is shutdown when these pins are low and active when these pins are high. Tie to VIN if shutdown feature is not used. An external resistor divider from VIN can be used to program a VIN threshold below which the corresponding channel of the LTM8060 will shut down. Do not float these pins.
PIN FUNCTIONS

TRSS1/2/3/4 (Pins N11/M11): Output Tracking and Soft-Start Pins. These pins allow user control of output voltage ramp rate during start-up. A TRSS\textsubscript{n} voltage below 0.8V forces the LTM8060 to regulate the FB\textsubscript{n} pin to equal the TRSS\textsubscript{n} pin voltage. When TRSS\textsubscript{n} is above 0.8V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2\(\mu\)A pull-up current on these pins allow a capacitor to program output voltage slew rate. These pins are pulled to ground during shutdown and fault conditions; use a series resistor if driving from a low impedance output. These pins may be left floating if the soft-start feature is not being used.

PG1/2/3/4 (Pins E9/D10/L3/M2): The PG\textsubscript{n} pin is the open-drain output of an internal comparator. PG\textsubscript{n} remains low until the FB\textsubscript{n} pin is within \(\pm 7.5\%\) of the final regulation voltage, and there are no fault conditions. PG\textsubscript{n} is pulled low during \(V_{\text{IN}}\) UVLO, thermal shutdown, or when the RUN\textsubscript{n} pins are low.

SHARE1/2/3/4 (Pins K8/K9/F4/F3): Channel 1/2/3/4 Current Sharing Control. Tie SHARE\textsubscript{n} together when paralleling outputs. LTM8060 can also share current between modules. See Typical Applications section for current sharing between channels and current sharing between modules.

DNC (Pins E10/L2): Do not connect.
OPERATION

The LTM8060 is a quad standalone nonisolated step-down switching DC/DC power supply that can deliver a peak current of up to 6A per channel. The continuous current is determined by the internal operating temperature. It provides a precisely regulated output voltage programmable via one external resistor from 0.8V to 8V. The input voltage range for VIN1 and VIN34 is 3V to 40V, while the input voltage range for VIN2 is 2V to 40V.

Given that the LTM8060 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. See simplified Block Diagram.

The LTM8060 contains current mode controllers, power switching elements, power inductors and a modest amount of input and output capacitance. The LTM8060 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RTn pin to GND.

Internal regulators provide power to the control circuitries. Bias regulators normally draw power from the VINn pin, but if the BIASn pin is connected to an external voltage higher than 3.2V, bias power is drawn from the external source (typically the regulated output voltage). This improves efficiency. Tie BIASn to GND if it is not used.

To enhance efficiency, the LTM8060 automatically switches to Burst Mode operation in light or no load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to just a few µA.

The TRSSn node acts as an auxiliary input to the error amplifier. The voltage at FBn servos to the TRSSn voltage until TRSSn goes above 0.8V. Soft-start is implemented by generating a voltage ramp at the TRSSn pin using an external capacitor which is charged by an internal 2µA constant current. Alternatively, driving the TRSSn pin with a signal source or resistive network provides a tracking function. Do not drive the TRSSn pin with a low impedance voltage source. See the Applications Information section for more details.

The LTM8060 contains power good comparators which trip when the FBn pin is at about ±8% of its regulated value. The PGn output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PGn pin high.

The LTM8060 is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above the maximum temperature rating to avoid interfering with normal operation, so prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.
APPLICATIONS INFORMATION

For most applications, the design process is straightforward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended $C_{IN}$, $C_{OUT}$, $R_{FB}$ and $R_T$ values.
3. Connect BIAS as indicated.

When using the LTM8060 with different output voltages, the higher frequency recommended by Table 1 will usually result in the best operation. While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system’s line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant $R_T$ value) at which the LTM8060 should be allowed to switch is given in Table 1 in the Maximum $f_{SW}$ column, while the recommended frequency (and $R_T$ value) for optimal efficiency over the given input condition is given in the $f_{SW}$ column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

### Set Output Voltage

The Output Voltage is programmed with a FB resistor as shown in the Figure below. Choose the resistor value according to Equation 1.

$$R_{FB} = \frac{249k\Omega}{\frac{V_{OUT}}{0.8V} - 1}$$

1% resistor is recommended to maintain output voltage accuracy.

![Figure 1. Set Output Voltage with a FB Resistor](image-url)
APPLICATIONS INFORMATION

Capacitor Selection Considerations

The $C_{\text{IN}}$ and $C_{\text{OUT}}$ capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system’s line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8060’s switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8060 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear.

If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8060. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM8060 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device’s rating. This situation is easily avoided; see the Hot-Plugging Safely section.

---

### Table 1. Recommended Component Values and Configuration ($T_A = 25°C$)

<table>
<thead>
<tr>
<th>$V_{\text{IN}}$ $V_{\text{OUT}}$</th>
<th>$R_{FB}$ (Ω)</th>
<th>$C_{\text{IN}}^2$</th>
<th>$C_{\text{OUT}}$</th>
<th>$BIAS$</th>
<th>$C_{\text{FF}}$</th>
<th>$f_{SW}$ (Hz)</th>
<th>$R_T$ (Ω)</th>
<th>$\text{MAX } f_{SW}$ (Hz)</th>
<th>$\text{MIN } R_T$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3V to 40V</td>
<td>0.8V</td>
<td>Open</td>
<td>$4.7\mu F$ 50V X5R 1206</td>
<td>$2 \times 100\mu F$ 4V X5R 0805</td>
<td>3.2V to 10V</td>
<td>100pF</td>
<td>400k</td>
<td>100k</td>
<td>600k</td>
</tr>
<tr>
<td>3V to 40V</td>
<td>1V</td>
<td>1M</td>
<td>$4.7\mu F$ 50V X5R 1206</td>
<td>$2 \times 100\mu F$ 4V X5R 0805</td>
<td>3.2V to 10V</td>
<td>100pF</td>
<td>400k</td>
<td>100k</td>
<td>725k</td>
</tr>
<tr>
<td>3V to 40V</td>
<td>1.2V</td>
<td>$499k$</td>
<td>$4.7\mu F$ 50V X5R 1206</td>
<td>$2 \times 100\mu F$ 4V X5R 0805</td>
<td>3.2V to 10V</td>
<td>68pF</td>
<td>500k</td>
<td>76.8k</td>
<td>875k</td>
</tr>
<tr>
<td>3.2V to 40V</td>
<td>1.5V</td>
<td>$287k$</td>
<td>$4.7\mu F$ 50V X5R 1206</td>
<td>$2 \times 100\mu F$ 4V X5R 0805</td>
<td>3.2V to 10V</td>
<td>–</td>
<td>600k</td>
<td>64.9k</td>
<td>1M</td>
</tr>
<tr>
<td>3.5V to 40V</td>
<td>1.8V</td>
<td>$200k$</td>
<td>$4.7\mu F$ 50V X5R 1206</td>
<td>$1 \times 100\mu F$ 4V X5R 0805</td>
<td>3.2V to 10V</td>
<td>–</td>
<td>650k</td>
<td>59k</td>
<td>1.3M</td>
</tr>
<tr>
<td>3.5V to 40V</td>
<td>2V</td>
<td>$165k$</td>
<td>$4.7\mu F$ 50V X5R 1206</td>
<td>$1 \times 100\mu F$ 4V X5R 0805</td>
<td>3.2V to 10V</td>
<td>–</td>
<td>700k</td>
<td>54.9k</td>
<td>1.4M</td>
</tr>
<tr>
<td>4.2V to 40V</td>
<td>2.5V</td>
<td>$118k$</td>
<td>$4.7\mu F$ 50V X5R 1206</td>
<td>$1 \times 47\mu F$ 4V X5R 0805</td>
<td>3.2V to 10V</td>
<td>–</td>
<td>800k</td>
<td>46.4k</td>
<td>1.7M</td>
</tr>
<tr>
<td>5.5V to 40V</td>
<td>3.3V</td>
<td>$78.7k$</td>
<td>$4.7\mu F$ 50V X5R 1206</td>
<td>$1 \times 47\mu F$ 6.3V X5R 0805</td>
<td>3.2V to 10V</td>
<td>–</td>
<td>1M</td>
<td>35.7k</td>
<td>2.2M</td>
</tr>
<tr>
<td>8.5V to 40V</td>
<td>5V</td>
<td>$47.5k$</td>
<td>$4.7\mu F$ 50V X5R 1206</td>
<td>$1 \times 47\mu F$ 6.3V X5R 1206</td>
<td>3.2V to 10V</td>
<td>–</td>
<td>1.2M</td>
<td>27.4k</td>
<td>3M</td>
</tr>
<tr>
<td>11V to 40V</td>
<td>8V</td>
<td>$27.4k$</td>
<td>$4.7\mu F$ 50V X5R 1206</td>
<td>$1 \times 47\mu F$ 10V X5R 1206</td>
<td>3.2V to 10V</td>
<td>–</td>
<td>1.6M</td>
<td>19.6k</td>
<td>3M</td>
</tr>
</tbody>
</table>

**Note 1:** The LTM8060 may be capable of operating at lower input voltages but may skip switching cycles.

**Note 2:** A bulk input capacitor is required.
APPLICATIONS INFORMATION

Frequency Selection
The LTM8060 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 3MHz by using a resistor tied from the RT pin to ground. Table 2 provides a list of $R_T$ resistor values and their resultant frequencies. The resistors in the table are standard 1% E96 values.

Operating Frequency Trade-Offs
It is recommended that the user apply the optimal $R_T$ value given in Table 1 for the input and output operating condition. When using the LTM8060 with different output voltages, the higher frequency recommended by Table 1 will usually result in the best operation. System level or other considerations, however, may necessitate another operating frequency. While the LTM8060 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8060 if the output is overloaded or short-circuited. A frequency that is too low can result in a design that has too much output ripple or too large of an output capacitor.

BIAS$_n$ Pin Considerations
The BIAS$_n$ pin is used to provide drive power for the internal power switching stage and operate other internal circuitry. For proper operation, it must be powered by at least 3.2V. If the output voltage is programmed to 3.2V or higher, BIAS$_n$ may be simply tied to V$_{OUT}$$_n$. If V$_{OUT}$$_n$ is less than 3.2V, BIAS$_n$ can be tied to V$_{IN}$$_n$ or some other voltage source. If the BIAS$_n$ pin voltage is too high, the efficiency of the LTM8060 may suffer. The optimum BIAS$_n$ voltage is dependent upon many factors, such as load current, input voltage, output voltage and switching frequency. In all cases, ensure that the maximum voltage at the BIAS$_n$ pin is less than 10V. If BIAS$_n$ power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the pin. A 1µF ceramic capacitor works well. The BIAS$_n$ pin may also be tied to GND at the cost of a small degradation in efficiency.

Table 2. Switching Frequency vs $R_T$ Value

<table>
<thead>
<tr>
<th>$f_{SW}$ (MHz)</th>
<th>$R_T$ (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2</td>
<td>200</td>
</tr>
<tr>
<td>0.3</td>
<td>137</td>
</tr>
<tr>
<td>0.4</td>
<td>100</td>
</tr>
<tr>
<td>0.5</td>
<td>76.8</td>
</tr>
<tr>
<td>0.6</td>
<td>64.9</td>
</tr>
<tr>
<td>0.7</td>
<td>54.9</td>
</tr>
<tr>
<td>0.8</td>
<td>46.4</td>
</tr>
<tr>
<td>0.9</td>
<td>41.2</td>
</tr>
<tr>
<td>1.0</td>
<td>35.7</td>
</tr>
<tr>
<td>1.2</td>
<td>27.4</td>
</tr>
<tr>
<td>1.4</td>
<td>23.2</td>
</tr>
<tr>
<td>1.6</td>
<td>19.6</td>
</tr>
<tr>
<td>1.8</td>
<td>16.9</td>
</tr>
<tr>
<td>2.0</td>
<td>14.7</td>
</tr>
<tr>
<td>2.2</td>
<td>12.7</td>
</tr>
<tr>
<td>2.4</td>
<td>11.3</td>
</tr>
<tr>
<td>2.6</td>
<td>10.2</td>
</tr>
<tr>
<td>2.8</td>
<td>9.09</td>
</tr>
<tr>
<td>3.0</td>
<td>8.06</td>
</tr>
</tbody>
</table>

Maximum Load
The maximum practical continuous load that the LTM8060 can drive per channel, while rated at 3A, actually depends upon both the internal current limit and the internal temperature. The internal current limit is designed to prevent damage to the LTM8060 in the case of overload or short-circuit. The internal temperature of the LTM8060 depends upon operating conditions such as the ambient temperature, the power delivered, and the heat sinking capability of the system. For example, if V$_{OUT1}$ of LTM8060 is configured to regulate at 1.5V, and the other 3 channels are turned off, V$_{OUT1}$ may continuously deliver 6A from 24V$_{IN}$ if the ambient temperature is controlled to less than 60°C. This is quite a bit higher than the 3A continuous rating. Please see graphs in the Typical Performance Characteristics section. Similarly, if all 4 channels of the LTM8060 are delivering 3.3V$_{OUT}$ and the ambient temperature is 100°C, each channel will deliver at most 1.5A from 24V$_{IN}$, which is less than the 3A continuous rating.
Power Derating

The 12\(V_{\text{IN}}\), 24\(V_{\text{IN}}\) and 36\(V_{\text{IN}}\) power loss curves can be used in coordination with the load current derating curves for calculating an approximate \(\theta_{\text{JA}}\) thermal resistance for the LTM8060 with airflow conditions. The power loss curves are taken at room temperature, and are increased with a 1.35 to 1.4 multiplicative factor at 125°C. These factors come from the fact that the power loss of the regulator increases about 45% from 25°C to 150°C, thus a 45% spread over 125°C delta equates to ~0.35%/°C loss increase. A 125°C maximum junction minus 25°C room temperature equates to a 100°C increase. This 100°C increase multiplied by 0.35%/°C equals a 35% power loss increase at the 125°C junction, thus the 1.35 multiplier.

The derating curves are plotted with four \(V_{\text{OUT}}\) at the same operating condition starting at 16A of total load current and low ambient temperature. The derating curves with airflow are measured at output voltages of 1.5V, 3.3V and 5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal FEA modeling.

The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at ~120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased.

The derived thermal resistances in Table 3 through Table 5 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the power loss curves and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick 6-layer board with two ounce copper (50μm) for all the layers.

### Table 3. 1.5V Output

<table>
<thead>
<tr>
<th>DERATING CURVE</th>
<th>(V_{\text{IN}}) (V)</th>
<th>POWER LOSS CURVE</th>
<th>AIRFLOW (LFM)</th>
<th>HEAT SINK</th>
<th>(\theta_{\text{JA}}) (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8060 G33-35</td>
<td>12, 24, 36</td>
<td>8060 G04</td>
<td>0</td>
<td>None</td>
<td>9</td>
</tr>
<tr>
<td>8060 G33-35</td>
<td>12, 24, 36</td>
<td>8060 G04</td>
<td>200</td>
<td>None</td>
<td>7.5</td>
</tr>
<tr>
<td>8060 G33-35</td>
<td>12, 24, 36</td>
<td>8060 G04</td>
<td>400</td>
<td>None</td>
<td>6.5</td>
</tr>
</tbody>
</table>

### Table 4. 3.3V Output

<table>
<thead>
<tr>
<th>DERATING CURVE</th>
<th>(V_{\text{IN}}) (V)</th>
<th>POWER LOSS CURVE</th>
<th>AIRFLOW (LFM)</th>
<th>HEAT SINK</th>
<th>(\theta_{\text{JA}}) (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8060 G36-38</td>
<td>12, 24, 36</td>
<td>8060 G08</td>
<td>0</td>
<td>None</td>
<td>9</td>
</tr>
<tr>
<td>8060 G36-38</td>
<td>12, 24, 36</td>
<td>8060 G08</td>
<td>200</td>
<td>None</td>
<td>7.5</td>
</tr>
<tr>
<td>8060 G36-38</td>
<td>12, 24, 36</td>
<td>8060 G08</td>
<td>400</td>
<td>None</td>
<td>6.5</td>
</tr>
</tbody>
</table>

### Table 5. 5V Output

<table>
<thead>
<tr>
<th>DERATING CURVE</th>
<th>(V_{\text{IN}}) (V)</th>
<th>POWER LOSS CURVE</th>
<th>AIRFLOW (LFM)</th>
<th>HEAT SINK</th>
<th>(\theta_{\text{JA}}) (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8060 G39-41</td>
<td>12, 24, 36</td>
<td>8060 G09</td>
<td>0</td>
<td>None</td>
<td>9</td>
</tr>
<tr>
<td>8060 G39-41</td>
<td>12, 24, 36</td>
<td>8060 G09</td>
<td>200</td>
<td>None</td>
<td>7.5</td>
</tr>
<tr>
<td>8060 G39-41</td>
<td>12, 24, 36</td>
<td>8060 G09</td>
<td>400</td>
<td>None</td>
<td>6.5</td>
</tr>
</tbody>
</table>
Load Sharing

The four LTM8060 channels may be paralleled to produce higher currents. To do this on two or more LTM8060, tie the \( V_{INn} \), \( V_{OUTn} \), \( FBn \) and \( SHAREN \) pins of all the paralleled channels/modules together. To ensure that paralleled channels start up together, the TRSS\( n \) pins may be tied together, as well. If it is inconvenient to tie the TRSS\( n \) pins together, make sure that the same value soft-start capacitors are used for each \( \mu \)Module regulator. When load sharing among \( n \) units and using a single \( R_{FB} \) resistor, the value of the resistor is given by Equation 1.

\[
R_{FB} = \frac{199.2}{n(V_{OUT} - 0.8)} \text{ where } R_{FB} \text{ is in } k\Omega
\]  

Equation 1

Examples of load sharing applications are given in Figure 6 through Figure 9.

Burst Mode Operation

To enhance efficiency at light loads, the LTM8060 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the quiescent current. During Burst Mode operation, the LTM8060 delivers single cycle bursts of current to the output capacitor followed by sleep periods where most of the internal circuitry is powered off and energy is delivered to the load by the output capacitor. During the sleep time, \( V_{INn} \) and BIAS\( n \) quiescent currents are greatly reduced, so, as the load current decreases towards a no load condition, the percentage of time that the LTM8060 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher light load efficiency.

Burst Mode operation is enabled by tying SYNC to GND.

Minimum Input Voltage

The LTM8060 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. Keep the input above 3V to ensure proper operation. Voltage transients or ripple valleys that cause the input to fall below 3V may turn off the LTM8060.

\( V_{IN1} \) must be above 3V for channel 1 and channel 2 to operate. If \( V_{IN1} \) is above 3V, channel 2 will operate as long as \( V_{IN2} \) is above 2V.

\( V_{IN34} \) must be above 3V for channel 3 and channel 4 to operate.

Output Voltage Tracking and Soft-Start

The LTM8060 allows the user to adjust its output voltage ramp rate by means of the TRSS\( n \) pin. An internal 2\( \mu \)A pulls up the TRSS\( n \) pin to about 2.4V. Putting an external capacitor on TRSS\( n \) enables soft starting the output to reduce current surges on the input supply. During the soft-start ramp the output voltage will proportionally track the TRSS\( n \) pin voltage. For output tracking applications, TRSS\( n \) can be externally driven by another voltage source. From 0V to 0.8V, the TRSS\( n \) voltage will override the internal 0.8V reference input to the error amplifier, thus regulating the FB\( n \) pin voltage to that of the TRSS\( n \) pin. When TRSS\( n \) is above 0.8V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The TRSS\( n \) pin may be left floating if the function is not needed.

Pre-Biased Output

As discussed in the Output Voltage Tracking and Soft-Start section, the LTM8060 regulates the output to the FB\( n \) voltage determined by the TRSS\( n \) pin whenever TRSS\( n \) is less than 0.8V. If the LTM8060 output is higher than the target output voltage, and SYNC\( n \) is not held below 0.8V, the LTM8060 will attempt to regulate the output to the target voltage by returning a small amount of energy back to the input supply. If there is nothing loading the input supply, its voltage may rise. Take care that it does not rise so high that the input voltage exceeds the absolute maximum rating of the LTM8060. If SYNC is grounded, the LTM8060 will not return current to the input.
APPLICATIONS INFORMATION

Frequency Foldback

The LTM8060 is equipped with frequency foldback which acts to reduce the thermal and energy stress on the internal power elements during a short circuit or output overload condition. If the LTM8060 detects that the output has fallen out of regulation, the switching frequency is reduced as a function of how far the output is below the target voltage. This in turn limits the amount of energy that can be delivered to the load under fault. During the start-up time, frequency foldback is also active to limit the energy delivered to the potentially large output capacitance of the load. When a clock is applied to the SYNC\textsubscript{n} pin, the SYNC\textsubscript{n} pin is floated or held high, the frequency foldback is disabled, and the switching frequency will slow down only during overcurrent conditions.

Synchronization

To select low ripple Burst Mode operation, tie the SYNC\textsubscript{n} pin below about 0.8V (this can be ground or a logic low output). To synchronize the LTM8060 oscillator to an external frequency, connect a square wave (with about 20\% to 80\% duty cycle) to the SYNC\textsubscript{n} pin. The square wave amplitude should have valleys that are below 0.8V and peaks above 1.5V.

The LTM8060 may be synchronized over a 200kHz to 3MHz range. The LTM8060 will not enter Burst Mode operation at light output loads while synchronized to an external clock. The R\textsubscript{T} resistor should be chosen to set the switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R\textsubscript{T} should be selected for 500kHz or lower.

The LTM8060 features spread spectrum operation to further reduce EMI/EMC emissions. To enable spread spectrum operation, apply between 2.8V and 4V to the SYNC\textsubscript{n} pin. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by R\textsubscript{T} to about 20\% higher than that value. The modulation frequency is about 7kHz. For example, when the LTM8060 is programmed to 2MHz, the frequency will vary from 2MHz to 2.4MHz at a 7kHz rate. When spread spectrum operation is selected, Burst Mode operation is disabled, and the part may run in discontinuous mode.

Shorted Input Protection

Care needs to be taken in systems where the output is held high when the input to the LTM8060 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR’ed with the LTM8060’s output. If the \( \text{VIN}_{\text{n}} \) pin is allowed to float and the RUN\textsubscript{n} pin is held high (either by a logic signal or because it is tied to \( \text{VIN}_{\text{n}} \)), then the LTM8060’s internal circuitry pulls its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN\textsubscript{n} pin, the internal current drops to essentially zero. However, if the \( \text{VIN}_{\text{n}} \) pin is grounded while the output is held high, parasitic diodes inside the LTM8060 can pull large currents from the output through the \( \text{VIN}_{\text{n}} \) pin. Figure 2 shows a circuit that runs only when the input voltage is present and that protects against a shorted or reversed input.

![Figure 2. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8060 Runs Only When the Input Is Present.](image)

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8060. The LTM8060 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 3 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.
APPLICATIONS INFORMATION

A few rules to keep in mind are:

1. Place the \( R_{FB} \) and \( R_T \) resistors as close as possible to their respective pins.

2. Place the \( C_{IN} \) capacitor as close as possible to the \( V_{IN} \) and GND connection of the LTM8060.

3. Place the \( C_{OUT} \) capacitor as close as possible to the \( V_{OUT} \) and GND connection of the LTM8060.

4. Place the \( C_{IN} \) and \( C_{OUT} \) capacitors such that their ground current flow directly adjacent to or underneath the LTM8060.

5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8060.

6. Use vias to connect the GND copper area to the board’s internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 3. The LTM8060 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8060. However, these capacitors can cause problems if the LTM8060 is plugged into a live supply (see Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the \( V_{IN} \) pin of the LTM8060 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8060’s rating and damaging the part. If the input supply is poorly controlled or the LTM8060 is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to \( V_{IN} \), but the most popular method of controlling input voltage overshoot is add an electrolytic bulk cap to the \( V_{IN} \) net. This capacitor’s relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Thermal Considerations

The LTM8060 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The derating curves given in the Typical Performance Characteristics section can be used as a guide. These
APPLICATIONS INFORMATION

Curves were generated by the LTM8060 mounted to a 104cm² 6-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system’s line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA (Finite Element Analysis) or CFD (Computational Fluid Dynamics) to predict thermal performance. To that end, the Pin Configuration typically gives three dominant thermal coefficients:

1. $\theta_{JA}$ – Thermal resistance from junction to ambient
2. $\theta_{JCbot}$ – Thermal resistance from junction to the bottom of the product case
3. $\theta_{JCtop}$ – Thermal resistance from junction to top of the product case

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

1. $\theta_{JA}$ is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

2. $\theta_{JCbot}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don’t generally match the user’s application.

3. $\theta_{JCtop}$ is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbot}$, this value may be useful for comparing packages but the test conditions don’t generally match the user’s application.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product’s data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical approximation of these dominant thermal resistances is given in Figure 4. Some thermal resistance elements, such as heat flow out the side of the package, are not defined by the JEDEC standard, and are not shown. The blue resistances are contained within the µModule regulator, and the green are outside.

The die temperature of the LTM8060 must be lower than the maximum rating, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8060. The bulk of the heat flow out of the LTM8060 is through the bottom of the package and the pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.
APPLICATIONS INFORMATION

Figure 4. Graphical Representation of Thermal Coefficients, Including JESD51-12 Terms

Figure 5. 8.5V to 40V Input to 5V at 3A, 3.3V at 3A, 5V at 3A, and 3.3V at 3A
Figure 6. 5.5V to 40V Input to Paralleled 3.3V at 6A; 3.2V to 40V Input to Paralleled 1.5V at 6A
Figure 7. 3V to 40V Input to Paralleled 1V at 12A
Figure 8. Two LTM8060 are Paralleled to Supply 1V/24A Output in Forced Continuous Mode
Figure 9. Two LTM8060 are Paralleled to Supply 1V/24A Output with 45° Phase Shift Interleaving Through All Eight Channels
## PACKAGE DESCRIPTION

### Table 6. LTM8060 Pinout (Sorted by Pin Number)

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BGA Package
165-Lead (16mm x 11.9mm x 3.32mm)
(Reference LTC DWG# 05-08-1605 Rev B)

DIMENSIONS

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MIN: Minimum
NOM: Nominal
MAX: Maximum

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY!
7. PACKAGE IN TRAY LOADING ORIENTATION

For more information www.analog.com
## REVISION HISTORY

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<td>Updated thermal resistance. Updated MSL rating. Updated graph G4S.</td>
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Digital Power System Management

Analog Devices’ family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.

### RELATED PARTS

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<td>36V, 8A Low EMI Step-Down µModule Regulator</td>
<td>5V ≤ VIN ≤ 36V, 3.3V ≤ VOUT ≤ 15V, EN55022B Compliant, 15mm × 15mm × 4.32mm LGA, 15mm × 15mm × 4.92mm BGA Packages</td>
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<td>40V, 2A Step-Down Silent Switcher µModule Regulator</td>
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