15V_{IN}, Single 10A Step-Down µModule Regulator with PMBus

FEATURES

- Complete Solution in <1cm² (Single-Sided PCB) or 0.5cm² (Dual-Sided PCB)
- PMBus Telemetry of Output Current, Output Voltage, Input Voltage, and Junction Temperature
- Input Voltage Range: 3V to 15V
- Output Voltage Range: 0.4V to 5.5V
- Adjustable Reference Voltage: 0.4V to 0.8V (Default 0.5V)
- 10A Continuous Output Current at 12V_{IN} and 1.8V_{OUT}, (T_A = 90°C)
- 90% Full Load Efficiency from 12V_{IN} to 1V_{OUT} at 10A
- ±1% Maximum DC Output Error Overtemperature
- Wide Frequency Range: 500kHz to 2MHz
- Internal Compensation
- Power Good Indicator
- Constant Frequency Peak Current Mode Control
- Differential Remote Sense
- Single-Phase Point-of-Load (POL) Operation
- *49-Lead 6.25mm × 6.25mm × 5.07mm* BGA package

APPLICATIONS

- Data Center Power, Servers, and Storage
- Telecom, Networking, and Industrial Equipment
- Point-of-Load Voltage Regulators

GENERAL DESCRIPTION

The *LTM4739* is a complete 10A step-down switching mode power µModule® (micromodule) regulator with PMBus interface in a tiny 6.25mm × 6.25mm × 5.07mm, Ball grid array (BGA) package. The package includes the switching controller, the power MOSFETs, an inductor, and the supporting components. Operating over an input voltage range of 3V to 15V, the LTM4739 supports an output voltage range of 0.4V to 5.5V. Its high-efficiency design delivers up to 10A of continuous output current. Only bulk input and output capacitors are needed. The switching frequency of the LTM4739 can be configured from 500kHz to 2MHz to provide the capability of optimizing the design in terms of size and performance.

The LTM4739 has an optional BIAS input pin, allowing connection from a 2.8V to 5.5V bias input supply for optimized efficiency. Operation settings and configurable features can be selected by connecting two pin-strap resistors from the PGMn pins to ground and later adjusted using PMBus commands. The LTM4739 has multiple protections, including positive and negative overcurrent (POC/NOC), output overvoltage (OV), and overtemperature (OT) to ensure a robust design. The LTM4739 is available with a RoHS-compliant terminal finish.

TYPICAL APPLICATION

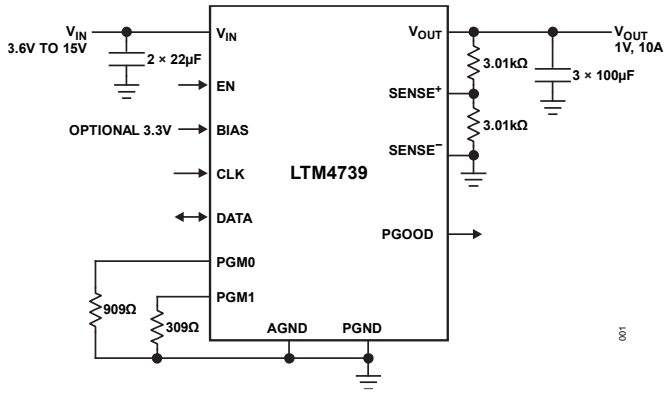

Figure 1. 3.6V to 15V Input to 1V, 10A Output

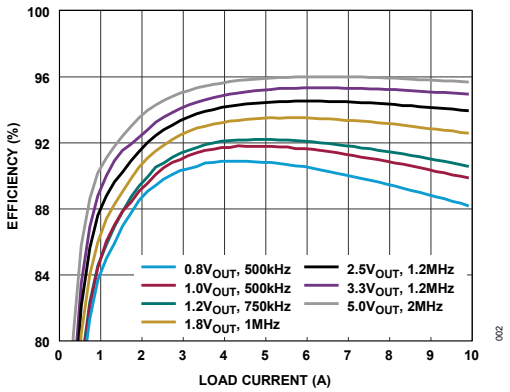

Figure 2. Efficiency, V_{IN} = 12V, V_{BIAS} = 3.3V

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	6/25	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics [1]

(T_A = 25°C, V_{IN} = 12V)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Input DC voltage	V_{IN}		–40°C ≤ T_J ≤ 125°C	3		15	V
Optional BIAS input voltage range	V_{BIAS}		–40°C ≤ T_J ≤ 125°C	2.8		5.5	V
Output voltage range	$V_{OUT(RANGE)}$		–40°C ≤ T_J ≤ 125°C	0.4		5.5	V
Output voltage, total variation with line and load	$V_{OUT(DC)}$	C_{IN} = 22µF, C_{OUT} = 300µF ceramic, V_{IN} = 3V to 15V, I_{OUT} = 0A to 10A	–40°C ≤ T_J ≤ 125°C	0.99	1	1.01	V
Input supply current (shutdown)	$I_{S(VIN)}$	Shutdown, EN = 0, V_{IN} = 12V, BIAS = 3.3V		90	120	150	µA
BIAS pin input current	I_{BIAS}	Shutdown, EN = 0, BIAS = 3.3V			1	10	µA
Input supply quiescent current	$I_{Q(VIN)}$	V_{IN} = 12V, EN = 1V, V_{OUT} = 1V, Forced continuous mode (FCM), BIAS is open		40	47	55	mA
		V_{IN} = 12V, EN = 1V, V_{OUT} = 1V, Discontinuous-conduction mode (DCM), BIAS is open		9	10	11	mA
Start-up time	t_{START}	C_{OUT} = 300µF ceramic, no load, V_{IN} = 12V, V_{OUT} = 1V			1.3		ms
Soft-start slew rate	SS	$SENSE^+$ – $SENSE^-$			0.5		V/ms
EN pin rising threshold	$V_{EN(RISE)}$	EN rising	–40°C ≤ T_J ≤ 125°C	0.8	0.85		V
EN pin falling threshold	$V_{EN(FALL)}$	EN falling	–40°C ≤ T_J ≤ 125°C		0.66	0.7	V
Output continuous current range	$I_{OUT(DC)}$	V_{IN} = 12V, V_{OUT} = 1V [4]				10	A
Line regulation accuracy	$\Delta V_{VOUT(LINE)}/V_{OUT}$	V_{OUT} = 1V, V_{IN} = 3V to 15V, I_{OUT} = 0A	–40°C ≤ T_J ≤ 125°C		0.001	0.02	%/V
Load regulation accuracy	$\Delta V_{OUT(LOAD)}/V_{OUT}$	V_{OUT} = 1V, I_{OUT} = 0A to 10A	–40°C ≤ T_J ≤ 125°C		0.2	0.6	%

(T_A = 25°C, V_{IN} = 12V)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Output ripple voltage[4]	$V_{OUT(AC)}$	I_{OUT} = 0A, C_{OUT} = 300µF ceramic, V_{IN} = 12V, V_{OUT} = 1V			5		mV
Output current limit	I_{OUTPK}	V_{IN} = 12V, V_{OUT} = 1V		11	13	15	A
Positive overcurrent (POC) protection threshold[5]	I_{POC}	Inductor peak current, POC = 15A		14	15	16.5	A
Fast positive overcurrent (FPOC) protection threshold[5]	I_{FPOC}	Inductor peak current, FPOC = 19A, will shutdown the µModule		17.1	19	21.6	A
Minimum on-time	$t_{ON(MIN)}$				50	60	ns
PGOOD output low	V_{PGOODL}	I_{PGOOD} = 4mA				0.4	V
PGOOD trip level V_{REF} = 0.5V	V_{PGOOD}	Output undervoltage threshold		–16	–13	–10	%
		Output OV protection threshold		10	13	16	%
PGOOD leakage	I_{PGOOD}					0.1	µA
PGOOD pull-down resistance	R_{PGOOD}				67		Ω
Oscillator frequency	f_{OSC}	R_{PGM1} = 309Ω			500		kHz
		R_{PGM1} = 21.5kΩ			1		MHz
		R_{PGM1} = 115kΩ			2		MHz
Internal LDO-regulated output to power gate drives	V_{CC}	V_{IN} = 3V to 15V		1.7	1.8	1.9	V
Analog AV_{DD} voltage to power internal circuitry	V_{AVDD}	V_{IN} = 3V to 15V			1.8		V
V_{IN} undervoltage lockout	V_{IN_UVLO}	Rising		2.4	2.5	2.6	V
		Hysteresis			100		mV
Feedback voltage accuracy	$SENSE^+$/ $SENSE^-$	$SENSE^+$ and $SENSE^-$, over line and load range	–40°C ≤ T_J ≤ 125°C	0.495	0.5	0.505	V
Feedback voltage range	$SENSE^+$/ $SENSE^-$	Set by PMBus command, 1.95mV resolution		0.4		0.8	V
Negative voltage sense input range	V_{SENSE^-}			–0.1		0.1	V
Positive voltage sense current	I_{SENSE^+}			–1		1	µA
Negative voltage sense current	I_{SENSE^-}				300		µA

(T_A = 25°C, V_{IN} = 12V)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
PMBus Interface							
CLK, DATA input logic low voltage						0.8	V
CLK, DATA input logic high voltage				1.45			V
CLK, DATA input leakage current				–1		1	µA
DATA output logic low		Sinking 4mA				0.4	V
PMBus operating frequency	f_{CLK}					1	MHz
PMBus Telemetry							
Reading update rate[4]		READ_IOUT, READ_VOUT, and READ_VIN			1.47		ms
		READ_TEMPERATURE			2.86		ms
READ_IOUT range						10	A
READ_IOUT accuracy		I_{OUT} = 0A		–1		1	A
		0A < I_{OUT} < 10A		–1.5		1.5	A
READ_VOUT range				400		800	mV
READ_VOUT accuracy				–1		1	%
READ_VIN range				3		15	V
READ_VIN accuracy				–350		350	mV
READ_TEMPERATURE range				–40		125	°C
READ_TEMPERATURE accuracy [4]					±4		°C

1 The LTM4739 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4739E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4739I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

2 The minimum on-time is tested at wafer sort.

3 See output current derating curves, *Figure 35* through *Figure 42*, for different V_{IN}, V_{OUT}, and T_A conditions.

4 Guaranteed by design.

5 100% tested at wafer level.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}, SW	18V
V_{OUT}, BIAS	6V
PGOOD, DATA, CLK, EN	4V
AV_{DD}, V_{CC}	2.5V
$SENSE^+$, PGM0, PGM1	AV_{DD}
$SENSE^-$	0.3V
Internal operating temperature range (E-grade, I-grade)	–40°C to 125°C
Storage temperature range	–55°C to 150°C
Peak solder reflow body temperature	250°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to Printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only: Human body model (HBM) per ANSI/ESDA/JEDEC JS-001, Field induced charged device model (FICDM), and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002. International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2. Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings

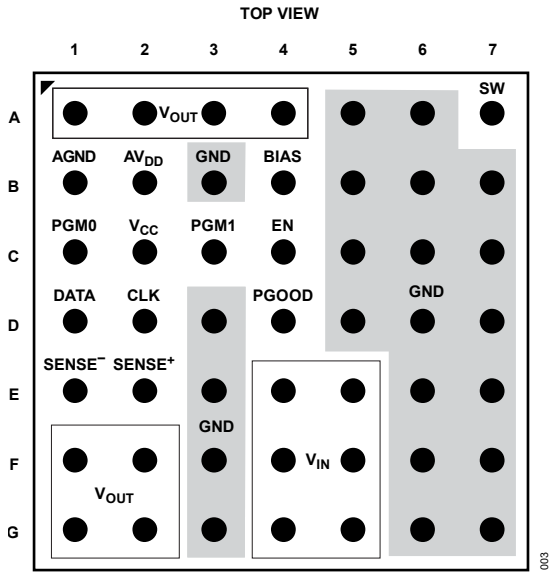
Table 3. LTM4739 ESD Ratings

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±4000	3A
CDM	±1250	C3

ESD Caution

Electrostatic discharge (ESD) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



BGA PACKAGE
49-LEAD (6.25mm × 6.25mm × 5.07mm)
T_{JMAX} = 125°C, θ_{JA} = 16°C/W, θ_{JCtop} = 9.2°C/W,
θ_{JCbot} = 6.1°C/W
WEIGHT = 0.71g

θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
FOR LAB MEASURED DERATING CURVES, SEE APPLICATIONS INFORMATION SECTION.

Figure 3. Pin Configuration

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Pin Descriptions

Table 4. Pin Descriptions

PIN	NAME	DESCRIPTION
A1, A2, A3, A4, F1, F2, G1, G2	V_{OUT}	Power Output Pins. Apply the output load between these pins and the GND pins. Recommend placing the output decoupling capacitor directly between these pins and the GND pins. See the *Decoupling Requirements* table for more details.
A5, A6, B3, B5-B7, C5-C7, D5- D7, E6, E7, F6, F7, G6, G7, D3, E3, F3, G3	GND	Power Ground Pins for Both Input and Output Returns.
A7	SW	Switching node of LTM4739. This pin is for test purposes only. Do not load the SW pin with external circuitry.
B1	AGND	Analog Ground. Single point connecting this pin to GND plane.

PIN	NAME	DESCRIPTION
B2	AV_{DD}	1.8V Supply for Analog Circuitry. There is an internal 1µF ceramic capacitor from AV_{DD} to AGND. The AV_{DD} pin could be left open.
B4	BIAS	Optional 2.8V to 5.5V LDO Input Supply. External BIAS helps to improve efficiency. A 2.2µF external bias capacitor is required. Leave the BIAS pin floating if unused.
C1	PGM0	Program Input. Connect the PGM0 pin to ground through a programming resistor. The PGM0 sets overcurrent (OC) protection and the PMBus address.
C2	V_{CC}	Internal 1.8V Regulator Bypass Pin. The internal power drivers and control circuits are powered by this voltage. There is an internal 4.4µF capacitor from V_{CC} to GND. Do not load the V_{CC} pin with external circuitry. The V_{CC} pin should be floated.
C3	PGM1	Program Input. Connect the PGM1 pin to ground through a programming resistor. The PGM1 sets the frequency and the control loop gain.
C4	EN	EN control input of each switching mode regulator channel. Enables device operation by connecting EN above 1V. Connecting this pin to GND shuts down the device.
D1	DATA	PMBus Data.
D2	CLK	PMBus Clock.
D4	PGOOD	Output Power Good Indicator. The PGOOD pin is the open-drain output of an internal comparator. The PGOOD pin remains low until the $V_{SENSE}^+ - V_{SENSE}^-$ voltage is within ±13% of the final regulation voltage, and there are no fault conditions.
E1	$SENSE^-$	Output Voltage Remote Sense Negative Input Pin.
E2	$SENSE^+$	Output Voltage Remote Sense Positive Input Pin. Connect V_{SENSE}^+ to the output voltage at the load. A resistive voltage divider can be inserted between the output and V_{SENSE}^+ to regulate the output above the reference voltage.
E4, E5, F4, F5, G4, G5	V_{IN}	Power Input Pins. Apply input voltage between the V_{IN} pins and GND pins. Recommend placing input decoupling capacitors directly between V_{IN} pins and GND pins.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

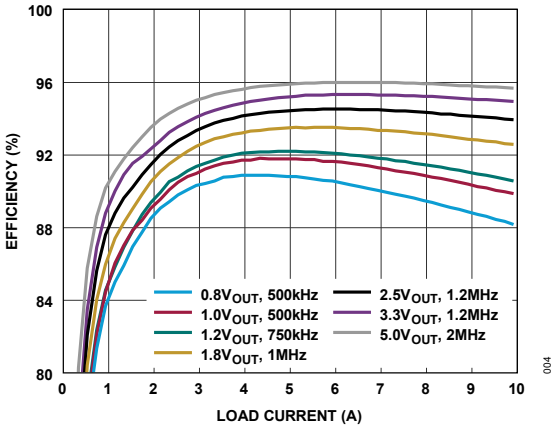


Figure 4. Efficiency, V_{IN} = 12V, V_{BIAS} = 3.3V

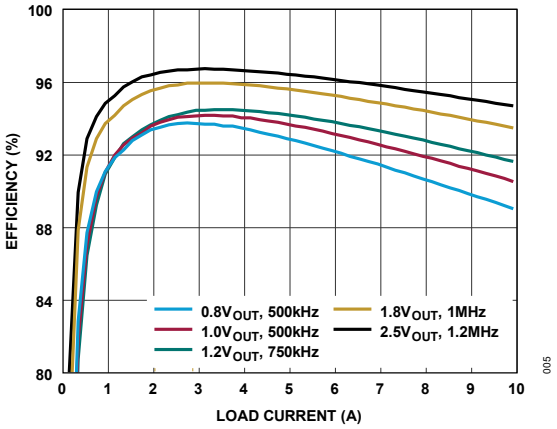


Figure 5. Efficiency, V_{IN} = 5V, V_{BIAS} = 3.3V

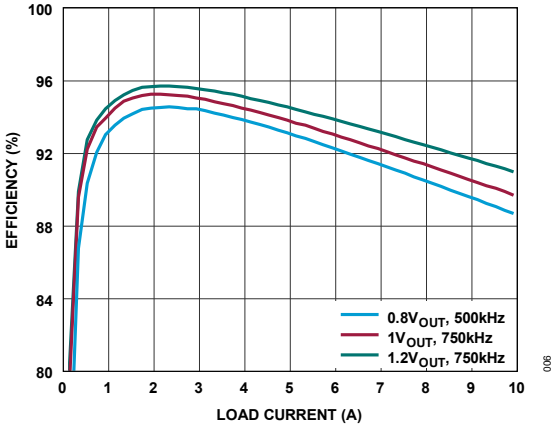


Figure 6. Efficiency, V_{IN} = 3.3V, V_{BIAS} = 3.3V

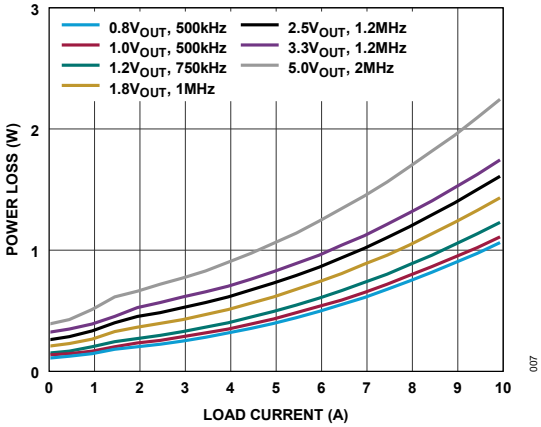


Figure 7. Power Loss, V_{IN} = 12V, V_{BIAS} = 3.3V

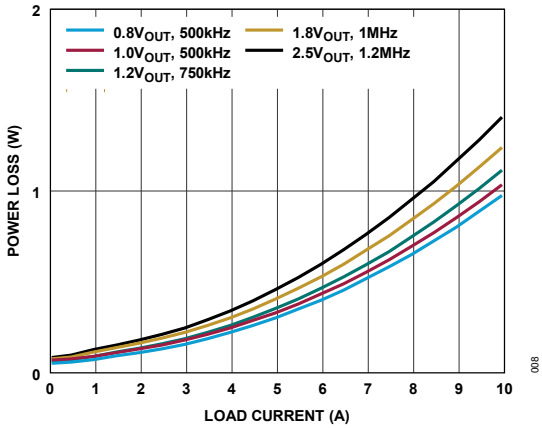


Figure 8. Power Loss, V_{IN} = 5V, V_{BIAS} = 3.3V

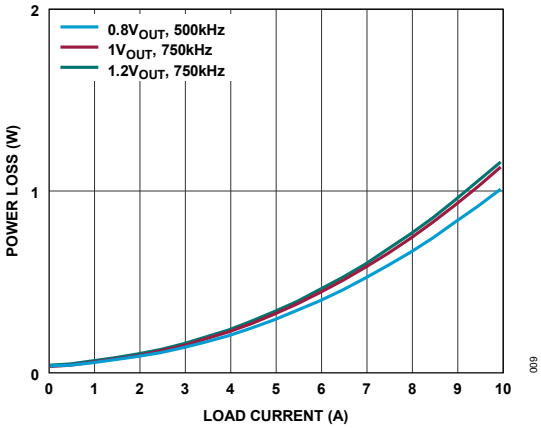


Figure 9. Power Loss, V_{IN} = 3.3V, V_{BIAS} = 3.3V

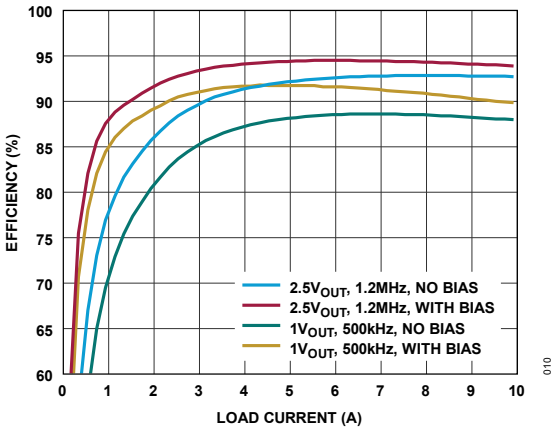


Figure 10. Efficiency vs. Load, V_{IN} = 12V, with and without External Bias

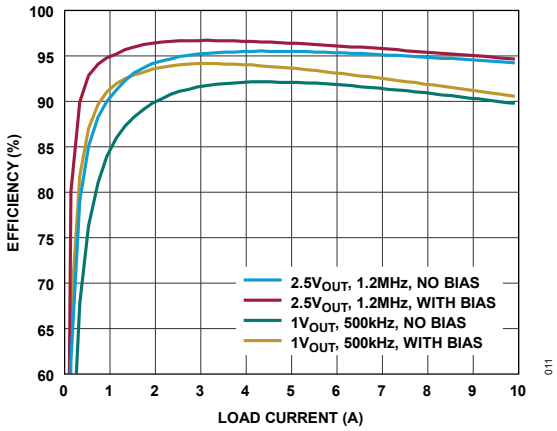


Figure 11. Efficiency vs. Load, V_{IN} = 5V, with and without External Bias

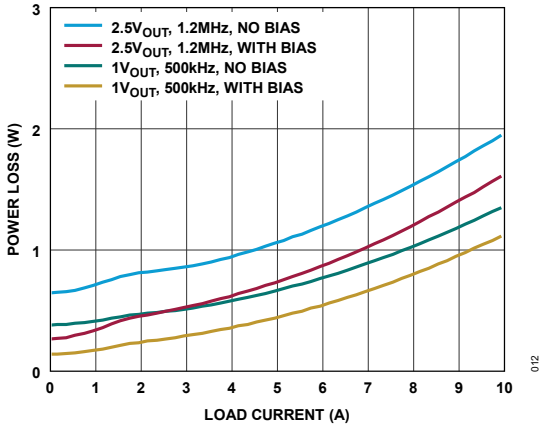


Figure 12. Power Loss vs. Load, V_{IN} = 12V, with and without External Bias

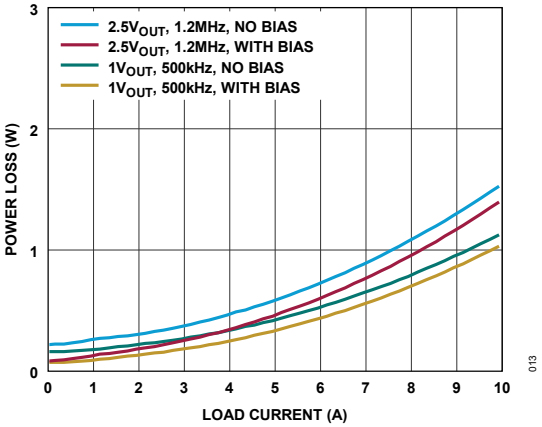


Figure 13. Power Loss vs. Load, V_{IN} = 5V, with and without External Bias

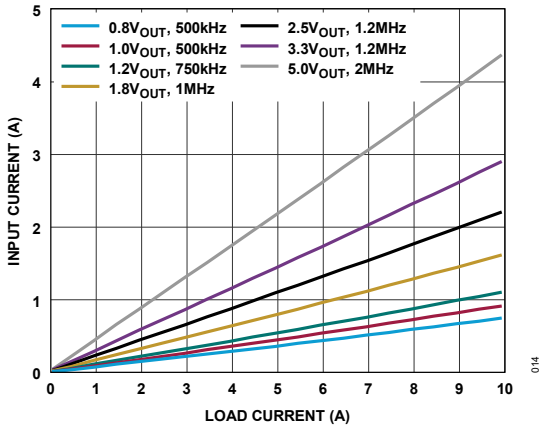


Figure 14. Input Current, V_{IN} = 12V, V_{BIAS} = 3.3V

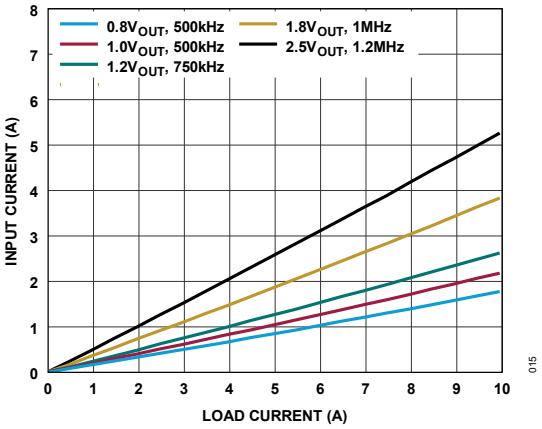


Figure 15. Input Current, V_{IN} = 5V, V_{BIAS} = 3.3V

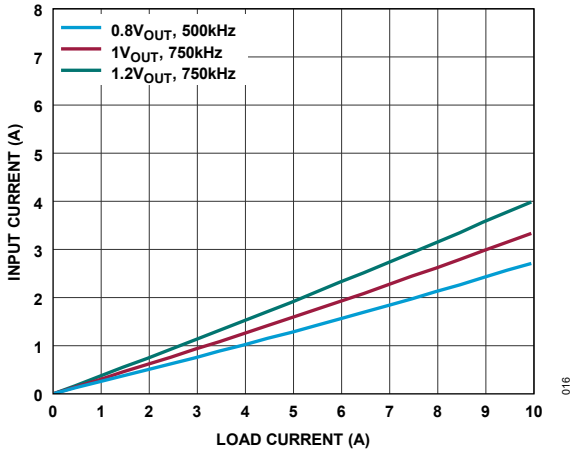
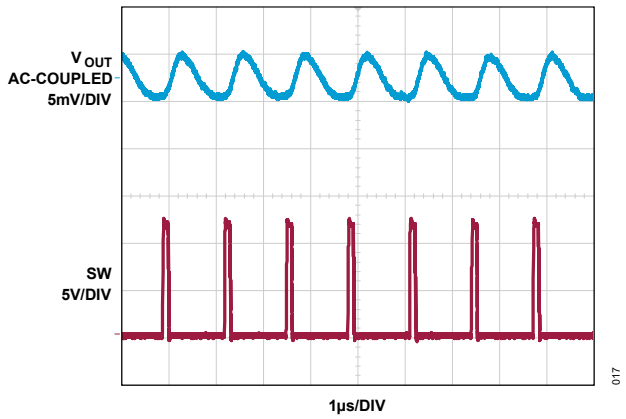
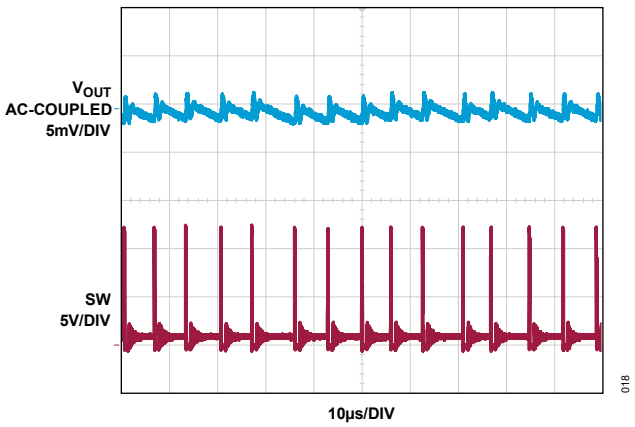


Figure 16. Input Current, V_{IN} = 3.3V, V_{BIAS} = 3.3V



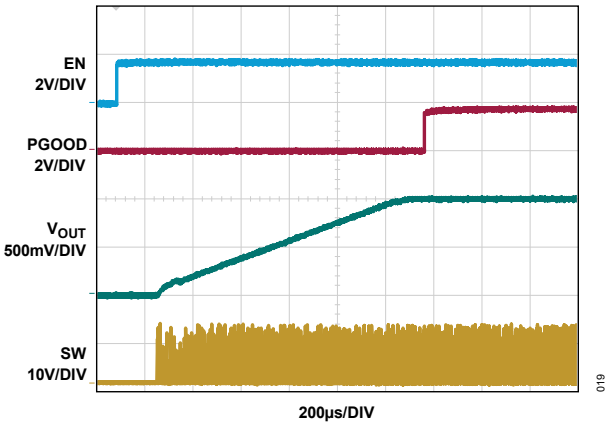
V_{OUT} = 1V, I_{OUT} = 10A, f_{SW} = 750kHz

Figure 17. Output Voltage Ripple (FCM)



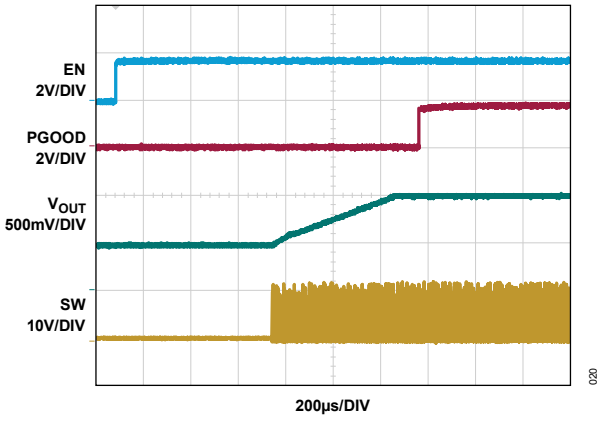
V_{OUT} = 1V, I_{OUT} = 0.1A

Figure 18. Output Voltage Ripple (DCM)



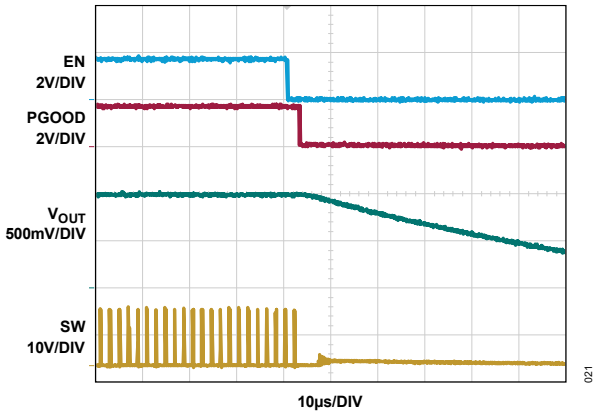
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 10A, f_{SW} = 2MHz

Figure 19. Startup without Pre-Bias



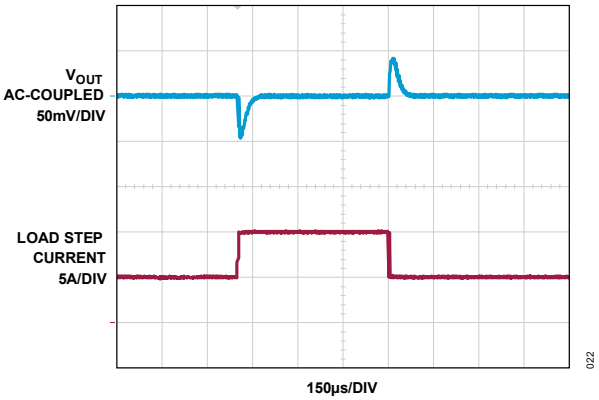
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A, f_{SW} = 2MHz

Figure 20. Startup with Pre-Bias, 0.5V



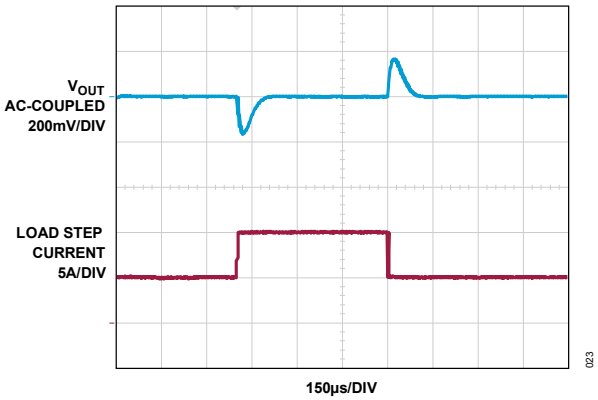
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 10A, f_{SW} = 2MHz

Figure 21. Shutdown



V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 5A TO 10A,
C_{OUT} = 4 × 220µF CERAMIC CAPACITOR, f_{SW} = 2MHz

Figure 22. Output Transient Response, 1V



V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 5A TO 10A,
C_{OUT} = 4 × 220µF CERAMIC CAPACITOR, f_{SW} = 2MHz

Figure 23. Output Transient Response, 5V

THEORY OF OPERATION

LTM4739 Overview

The LTM4739 is a single-phase POL buck regulator with PMBus that can deliver up to 10A. The continuous current is determined by the internal operating temperature. It provides a precisely regulated output voltage programmable through two external resistors from 0.4V to 5.5V. The input voltage range is 3V to 15V. Given that the LTM4739 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. See the simplified Block Diagram (*Figure 24*). The Analog Devices *LTpowerPlay®* graphical user interface (GUI), the *DC1613A* USB-to-PMBus adapter, and the *EVAL-LTM4739-AZ* evaluation board are available.

The LTM4739 contains a current mode controller, power switching elements, a power inductor, and a modest amount of input and output capacitance. The LTM4739 is a fixed-frequency pulse-width modulation (PWM) regulator. The switching frequency is set by simply connecting the appropriate resistor value from the PGM1 pin to GND. The LTM4739 features a selectable advanced modulation scheme (AMS) to provide improved performance during fast-load transients. Operation settings and configurable features can be selected by connecting pin-strap resistors from the PGMn pins to ground or using PMBus commands. See the *Applications Information* section for more details. An internal regulator provides power to control circuitry. To improve efficiency across all loads, supply current to control circuitry can be sourced from an external $3.3V_{BIAS}$, instead of leaving BIAS floating. The EN pin is used to place the LTM4739 in operation or in shutdown. The LTM4739 can operate in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. When in FCM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. A negative inductor current is allowed. The LTM4739 can sink current from the output and return this charge to the input in this mode, improving load step transient response. To enhance efficiency at light load, the LTM4739 can operate in discontinuous-conduction mode (DCM) in light load situations. The DCM is by default disabled; it can be enabled with PMBus commands. See the *Applications Information* section for more details.

The LTM4739 contains a power good comparator which trips when the $SENSE^+$ and $SENSE^-$ pins voltage is within ±10% of the typical value (say 0.5V, the PGOOD range is 0.45V to 0.55V). The PGOOD output is an open-drain transistor that is off when the output is regulated, allowing an external resistor to pull the PGOOD pin high. The LTM4739 is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above 125°C to avoid interfering with normal operation, so prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device. The LTM4739 does not support the parallel operation to produce higher currents.

LTM4739 Major Features

- FCM and DCM operation.
- Fixed frequency control loop.
- Configurable and programmable frequency from 500kHz to 2MHz.
- Selectable advanced modulation scheme (AMS) to improve transient response.
- High efficiency with an optional external bias input supply.
- Pin-strap programmability.
- PMBus telemetry of output current, output/input voltage, and junction temperature.
- PMBus adaptive voltage scaling (AVS) of 0.4V to 0.8V reference range.
- PMBus fault or warning monitoring for input/output undervoltage, overvoltage, overcurrent, overpower, and communication, memory, or logic (CML) faults.

Simplified Block Diagram

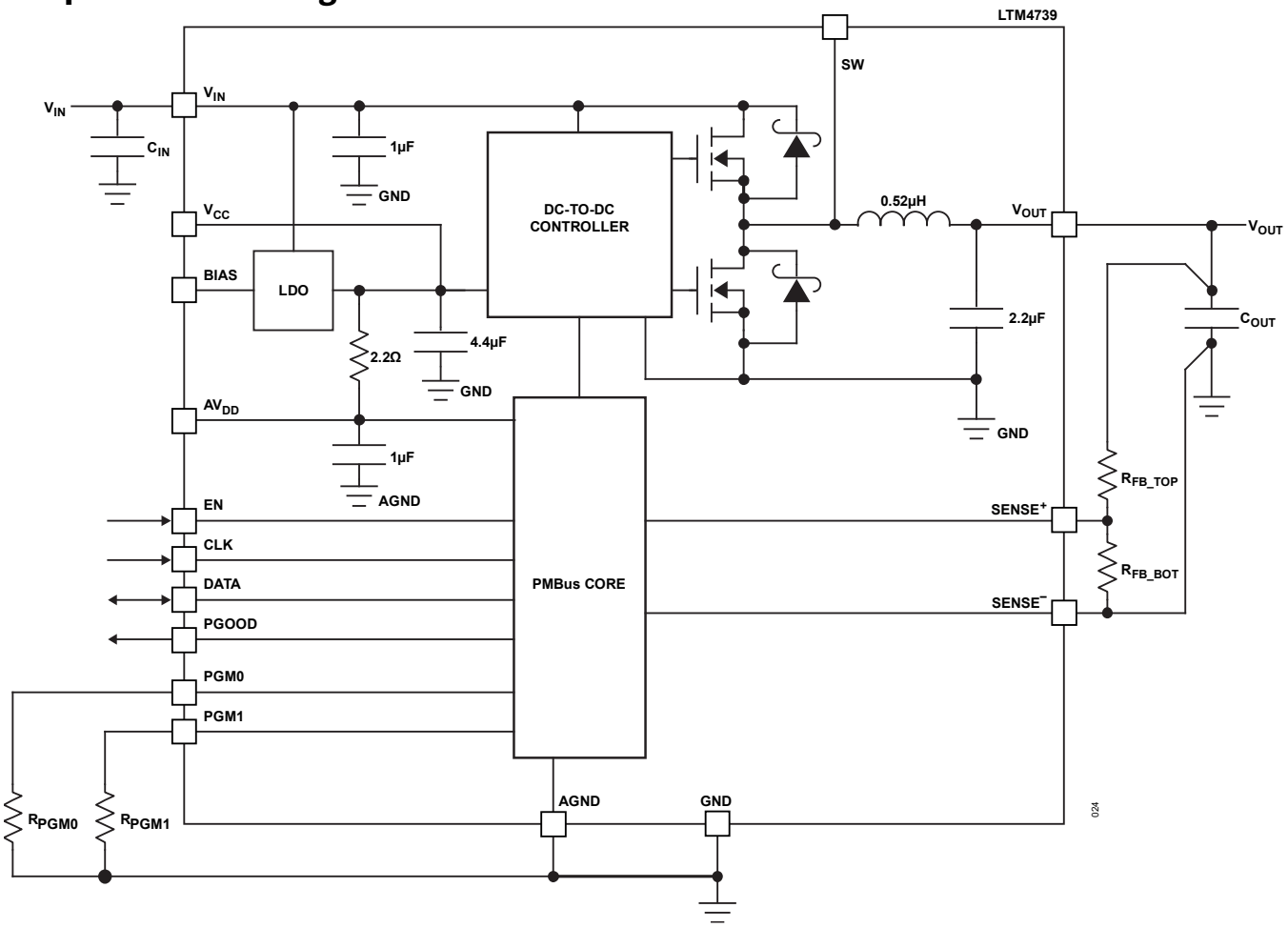


Figure 24. LTM4739 Simplified Block Diagram

Decoupling Requirements

Table 5. Decoupling Requirements

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External input capacitor requirement (V_{IN} = 12V, V_{OUT} = 1.5V)	I_{OUT} = 10A	10	22		µF
C_{OUT}	External output capacitor requirement (V_{IN} = 12V, V_{OUT} = 1.5V)	I_{OUT} = 10A	200	300		µF

APPLICATIONS INFORMATION

For most applications, the design process is straightforward and is summarized as follows.

1. See *Table 6* and find the row with the desired input range and output voltage.
2. Apply the recommended C_{IN} and C_{OUT} resistor values.

While these component combinations have been tested for proper operation, it is the user's responsibility to verify proper operation over the intended system's line, load, and environmental conditions. Remember that the maximum output current is limited by the junction temperature, the relationship between the input and output voltage magnitude, and the polarity, as well as other factors. See the graphs in the *Typical Performance Characteristics* section for guidance.

The recommended frequency (and the R_{PGM1} value) for optimal efficiency over the given input condition is shown in *Table 6*.

Table 6. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN} (V)	V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	C_{IN} (µF)	C_{OUT} (µF)	f_{SW} (Hz)	R_{PGM1} (Ω)
3 to 15	0.8	1.82	3.01	2 × 22 (25V)	3 × 100	500k	309
3.6 to 15	1	3.01	3.01	2 × 22 (25V)	3 × 100	500k	309
3 to 15	1.2	4.22	3.01	2 × 22 (25V)	3 × 100	750k	2.15k
3.6 to 15	1.5	6.02	3.01	2 × 22 (25V)	3 × 100	750k	2.15k
3.6 to 15	1.8	7.87	3.01	2 × 22 (25V)	3 × 100	1M	21.5k
5 to 15	2.5	12.01	3.01	2 × 22 (25V)	3 × 100	1.2M	56.2k
6.6 to 15	3.3	16.9	3.01	2 × 22 (25V)	3 × 100	1.2M	56.2k
10 to 15	5	22.6	2.49	2 × 22 (25V)	3 × 100	2M	115k

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in *Table 6* are the minimum recommended values for the associated operating conditions. Applying capacitor values below the values indicated in *Table 6* is not recommended and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if necessary. Again, the user is responsible for verifying the proper operation conditions over the intended system's line, load, and environmental conditions.

Ceramic capacitors are small, robust, and have very low ESR. However, not all ceramic capacitors are suitable. The X5R and X7R types are stable over temperature and applied voltage, and they provide dependable service. Other types, including Y5V and Z5U, have very large temperature and voltage coefficients of capacitance. In an application circuit, they may have only a small fraction of their nominal capacitance, resulting in a much higher output voltage ripple than expected. Ceramic capacitors are also piezoelectric. In DCM operation, the LTM4739's switching frequency depends on the load current, and can stimulate a ceramic capacitor at audio frequencies, generating audible noise. Only if DCM is enabled, the LTM4739 may skip pulses during light load conditions. If this occurs, the effective switching frequency could be lowered enough to operate in the audible frequency range. During this scenario, the LTM4739 operates with a lower current limit, which helps suppress audible noise. If this audible noise is unacceptable, use a high-performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low-cost electrolytic capacitor. A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM4739. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM4739 circuit is plugged into a live supply, the input

voltage can rise to twice its nominal value, possibly exceeding the device's rating. This situation can be easily avoided; see the *Hot-Plugging Safely* section for more details.

Pin-Strap Programmability

The LTM4739 has two program pins (PGM0 and PGM1) to set some of the key configurations of the device (see *Table 7* and *Table 8*) for more details. The PGMn pin values are read during startup initialization. The PGM0 and PGM1 pins each have 32 detection levels. A pin-strap resistor is connected from the PGMn pin to AGND to select one of the 32 codes. The PGM0 is used to select the POC level and PMBus address. The PGM1 pin is used to select the switching frequency and a predefined scenario, which corresponds to the voltage loop gain and the advanced modulation scheme (AMS) selection. Predefined scenarios are summarized in *Table 9.*

Table 7. PGM0, POC, and PMBus Address Selection

CODES	R_{PGM0} (Ω)	POC (A)	PMBus ADDRESS
0	95.3	15	0x38h
1	200		0x39h
2	309		0x3Ah
3	422		0x3Bh
4	536		0x3Ch
5	649		0x3Dh
6	768		0x3Eh
7	909		0x3Fh
8	1.05k	13	0x38h
9	1.21k		0x39h
10	1.4k		0x3Ah
11	1.62k		0x3Bh
12	1.87k		0x3Ch
13	2.15k		0x3Dh
14	2.49k		0x3Eh
15	2.87k		0x3Fh
16	3.74k	11	0x38h
17	8.06k		0x39h
18	12.4k		0x3Ah
19	16.9k		0x3Bh
20	21.5k		0x3Ch
21	26.1k		0x3Dh
22	30.9k		0x3Eh
23	36.5k		0x3Fh
24	42.2k	9	0x38h
25	48.7k		0x39h
26	56.2k		0x3Ah
27	64.9k		0x3Bh
28	75k		0x3Ch
29	86.6k		0x3Dh
30	100k		0x3Eh
31	115k		0x3Fh

Table 8. PGM1 Switching Frequency and Scenario Selection

CODES	R_{PGM1} (Ω)	SWITCHING FREQUENCY (Hz)	SCENARIO #
0	95.3	500k	A
1	200		B
2	309		C
3	422		D
4	536		E
5	649		F
6	768	600k	A
7	909		B
8	1.05k		C
9	1.21k		D
10	1.4k		E
11	1.62k		F
12	1.87k	750k	A
13	2.15k		B
14	2.49k		C
15	2.87k		D
16	3.74k		E
17	8.06k		F
18	12.4k	1M	A
19	16.9k		B
20	21.5k		C
21	26.1k		D
22	30.9k		E
23	36.5k		F
24	42.2k	1.2M	A
25	48.7k		B
26	56.2k		C
27	64.9k		D
28	75k		E
29	86.6k		F
30	100k	2M	A
31	115k		B

The LTM4739 has six predefined scenarios, as summarized in *Table 9*, which can be selected by a pin-strap resistor connected from the PGM1 pin to AGND. See the *Voltage Loop Gain* section for information on selecting the voltage loop gain resistance (R_{VGA}) to optimize the control loop performance. For each scenario, the advanced modulation scheme (AMS) option can also be selected.

Table 9. Predefined Scenarios

SCENARIO #	R_{VGA} (kΩ)	AMS OPTION
A	15.7	Disabled
B	22.7	Disabled
C	22.7	Enabled
D	26.8	Enabled
E	31.3	Enabled
F	44.8	Enabled

PMBus Interface

The PMBus is an industry standard that defines a means of communication with power conversion devices. It is comprised of an industry-standard SMBus serial interface and the PMBus command language. The LTM4739 supports the PMBus interface to communicate with a host (controller) device. The device PMBus address is selected by a pin-strap resistor connected from the PGM0 pin to AGND (see the *Pin-Strap Programmability* section for more details). *Table 10* shows the supported PMBus commands. Refer to the *LTM4739 User Reference Manual* for complete details.

Table 10. Supported PMBus Commands

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	FACTORY VALUE
0x01	OPERATION	Output enable/disable.	R/W byte	Bit field	0x80
0x02	ON_OFF_CONFIG	EN pin and PMBus operation command setting.	R/W byte	Bit field	0x1F
0x03	CLEAR_FAULTS	Clear any fault bits that have been set.	Send byte		N/A
0x10	WRITE_PROTECT	The level of protection provided by the device against accidental changes.	R/W byte	Bit field	0x20
0x19	CAPABILITY	Summary of PMBus optional communication protocols supported by the LTM4739.	R byte	Bit field	0xA0
0x20	VOUT_MODE	Output voltage data format and mantissa exponent.	R byte	Bit field	0x17
0x21	VOUT_COMMAND	Feedback reference voltage setpoint.	R/W word	ULINEAR16	0x0100

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	FACTORY VALUE
0x24	VOUT_MAX	The upper limit of the reference voltage setpoint.	R/W word	ULINEAR16	0x019A
0x78	STATUS_BYTE	One-byte summary of the unit's fault condition.	R byte	Bit field	N/A
0x79	STATUS_WORD	Two-bytes summary of the unit's fault condition.	R word	Bit field	N/A
0x7A	STATUS_VOUT	Output voltage fault and warning status.	R byte	Bit field	N/A
0x7B	STATUS_IOUT	Output current fault and warning status.	R byte	Bit field	N/A
0x7C	STATUS_INPUT	Input voltage fault and warning status.	R byte	Bit field	N/A
0x7D	STATUS_TEMPERATURE	IC junction temperature fault and warning status.	R byte	Bit field	N/A
0x7E	STATUS_CML	Communication fault and warning status.	R byte	Bit field	N/A
0x80	STATUS_MFR_SPECIFIC	Manufacturing-specific faults and warning status.	R byte	Bit field	N/A
0x88	READ_VIN	Input voltage telemetry.	R word	LINEAR11	N/A
0x8B	READ_VOUT	Feedback voltage telemetry.	R word	ULINEAR16	N/A
0x8C	READ_IOUT	Output current telemetry.	R word	LINEAR11	N/A
0x8D	READ_TEMPERATURE_1	IC junction temperature telemetry.	R word	LINEAR11	N/A
0xAD	IC_DEVICE_ID	Device root part number.	R block	ASCII	"LTM4739"
0xAE	IC_DEVICE_REV	Device revision code.	R block	ASCII	N/A
0xD0	MFR_PINSTRAP	Manufacturer-specific device operating configurations.	R/W byte	Bit field	PGM0/PGM1 dependent
0xD1	MFR_SCENARIO_0	Manufacturer-specific device operating configurations.	R/W byte	Bit field	PGM1 dependent
0xD2	MFR_SCENARIO_1	Manufacturer-specific device operating configurations.	R/W byte	Bit field	PGM1 dependent
0xD3	MFR_SCENARIO_2	Manufacturer-specific device operating configurations.	R/W byte	Bit field	N/A

LTpowerPlay: An Interactive GUI for Digital Power Management

The LTpowerPlay is a powerful Windows-based development environment that supports Analog Devices digital power system management (PSM) ICs, including the LTM4739. See *Figure 25* for the LTpowerPlay main interface.

The LTpowerPlay can be used to evaluate Analog Devices ICs by connecting to an evaluation board or to the user application. The LTpowerPlay design software supports a variety of tasks. It can also be used in offline mode (with no hardware present) to build multiple IC configuration files that can be saved and reloaded later. The LTpowerPlay provides unprecedented diagnostic and debugging features. It becomes a valuable diagnostic tool during board bring-up to program or tweak the power system, or to diagnose power issues when bringing up rails. The LTpowerPlay utilizes the Analog Devices USB-to-I²C/SMBus/PMBus *DC1613A* adapter to communicate with one of the many potential targets, including the Analog Devices *EVAL-LTM4739-AZ* evaluation board. The software also provides an automatic update feature to keep the revisions current with the latest set of device drivers and documentation. A great deal of context-sensitive help is available with LTpowerPlay, along with several tutorial demos. For complete information, refer to the Analog Devices *LTpowerPlay* web page.

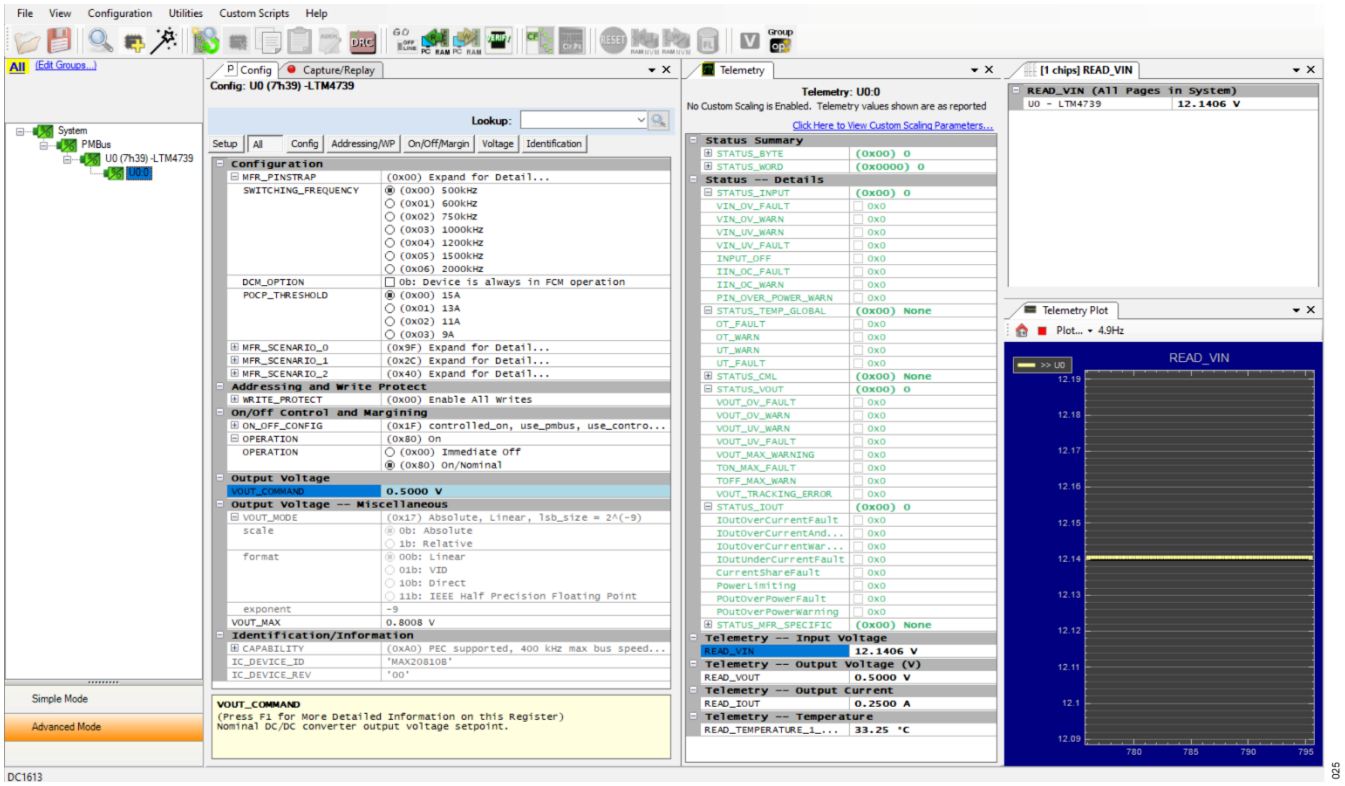


Figure 25. LTpowerPlay Main Interface

Frequency Selection

The LTM4739 uses constant frequency PWM architecture that can be programmed to switch from 500kHz to 2MHz by using a resistor connected from the PGM1 pin to ground. For more details, see *Table 8*.

Advanced Modulation Scheme

The LTM4739 offers a selectable advanced modulation scheme (AMS) to provide an improved transient response. The AMS provides a significant advantage over conventional fixed-frequency PWM schemes. Enabling the AMS feature allows for modulation at both the leading and trailing edges, which results in a temporary increase or decrease of the switching frequency during large load transients. *Figure 26* shows the scheme to include leading-edge modulation to the traditional trailing-edge modulation when AMS is enabled in the LTM4739.

The modulation scheme allows for the turn-on and off with minimal delay. Since the total inductor current increases quickly, thus satisfying the load demand, the current drawn from the output capacitors is reduced. With AMS enabled, the system's closed-loop bandwidth can be extended without a phase-margin penalty. As a result, the output capacitance can be minimized.

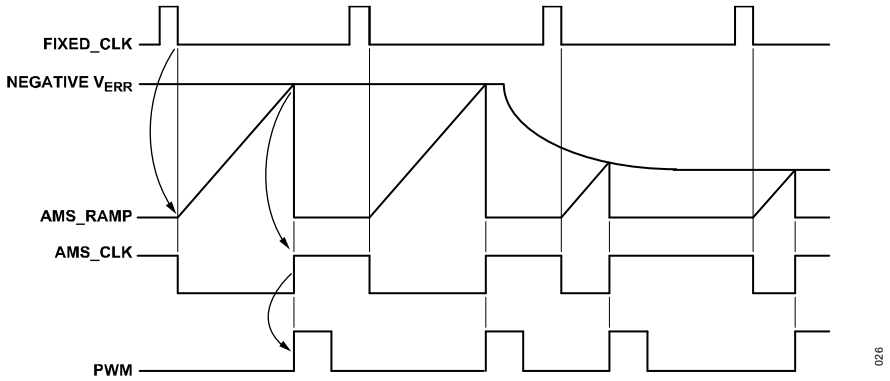


Figure 26. Advanced Modulation Scheme Operation

Output Voltage Sensing

The LTM4739 has a default 0.5V reference voltage. The reference voltage can be adjusted by the PMBus VOUT_COMMAND from 0.4V to 0.8V with 1.95mV resolution. When the desired output voltage is higher than V_{REF}, it is required to use a resistor dividers R_{FB1} and R_{FB2} to sense the output voltage. It is recommended that the value R_{FB2} does not exceed 5kΩ. The resistor-divider ratio is given by the Equation *1*.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{RFB1}}{R_{RFB2}}\right) \quad (1)$$

Where:

V_{OUT} is the output voltage.
V_{REF} is the reference voltage.
R_{FB1} is the top divider resistor.
R_{FB2} is the bottom divider resistor.

Operating Frequency Trade-Offs

It is recommended that the user apply the optimal R_{PGM1} value given in *Table 6* for the input and output operating conditions. System-level or other considerations, however, may necessitate another operating frequency. While the LTM4739 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may

result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat, or even damage the LTM4739 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

The LTM4739 internally has a slope compensation applied to the current loop during on-time to guarantee stability and improve noise immunity. To avoid the slope compensation saturating the current loop, it is required that the maximum on-time be limited using Equation 2.

$$t_{ON(MAX)} = \frac{5pF\left[800mV - \left(I_{OUT(MAX)} + \frac{I_{RIPPLE}}{2}\right) \times \frac{1.6\Omega}{62.5}\right]}{I_{SLOPE}} \quad (2)$$

where:

$t_{ON(MAX)}$ is the maximum on-time of the high-side MOSFET.
$I_{OUT(MAX)}$ is the maximum load current.
I_{RIPPLE} is the inductor current ripple peak-to-peak value.
I_{SLOPE} is the internal slope compensation amplitude. The default value is 3.78µA and the value can be adjusted by the PMBus MFR_SCENARIO_0 command.

The minimum recommended switching frequency is calculated with Equation 3.

$$f_{SW(MIN)} = \frac{V_{OUT}}{t_{ON(MAX)} \times V_{IN(MIN)}} \quad (3)$$

where:

$f_{SW(MIN)}$ is the minimum selectable switching frequency.

Because of the system noise injection, even at steady-state operation, typically the SW rising and falling edges would have some random jittering noise. The selection of the switching frequency (f_{SW}) should take into consideration the jittering and be higher than $f_{SW(MIN)}$ and lower than $f_{SW(MAX)}$. To improve the SW jittering, it is recommended to use smaller inductor values and lower voltage loop gain to minimize the noise sensitivity.

It is required that the frequency be selected so that the minimum controllable on-time and minimum controllable off-time are not violated. The maximum recommended switching frequency is calculated by Equation 4.

$$f_{SW(MAX)} = MIN\left\{\frac{V_{OUT}}{t_{ON(MIN)} \times V_{IN(MAX)}}, \frac{V_{IN(MIN)} - V_{OUT}}{t_{OFF(MIN)} \times V_{IN(MIN)}}\right\} \quad (4)$$

where:

$f_{SW(MAX)}$ is the maximum selectable switching frequency.
$V_{IN(MAX)}$ is the maximum input voltage.
$V_{IN(MIN)}$ is the minimum input voltage.
$t_{ON(MIN)}$ is the minimum controllable on-time.
$t_{OFF(MIN)}$ is the minimum controllable off-time.

Maximum Load

The maximum practical continuous load that the LTM4739 can drive, while rated at 10A, depends upon both the internal current limit and the internal temperature. The internal current limit is designed to prevent damage to the LTM4739 in the case of an overload or a short circuit. The internal temperature of the LTM4739 depends upon operating conditions such as the ambient temperature, the power delivered, and the heat-sinking capability of the system. For example, if the LTM4739 is configured to regulate at 1V, it may continuously deliver 10A from $12V_{IN}$ if the ambient temperature is controlled to less than 60°C. See *Figure 35*, derating curve, for the V_{OUT} = 1V condition. Similarly, if the output voltage is 5V and the ambient temperature is 85°C, the LTM4739 will deliver at most 8.5A from $12V_{IN}$, which is less than the 10A continuous rating.

Voltage Loop Gain

For stability purposes, it is recommended that the voltage loop bandwidth (BW) be lower than 1/5 of the switching frequency. Consider the case of using Multilayer ceramic output capacitors that have nearly ideal impedance characteristics in the frequency range of interest, with negligible ESR and ESL. The voltage loop BW can be estimated with the Equation *5*.

$$BW = \frac{\frac{R_{FB2}}{R_{FB2} + R_{FB1}} \times \frac{R_{VGA}}{10k\Omega}}{2\pi \times 8m\Omega \times C_{OUT}} \quad (5)$$

where:

R_{VGA} = The voltage loop gain resistance, which is set by the scenario selected (see *Table 9* for more details).

Minimum Input Voltage

The LTM4739 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. Keep V_{IN} above 3V to ensure proper operation.

Prebiased Output

The LTM4739 regulates the output to the $SENSE^+$ and $SENSE^-$ voltage. If the LTM4739 output is higher than the target output voltage, the LTM4739 will attempt to regulate the output to the target voltage by returning a small amount of energy back to the input supply. If nothing is loading the input supply, its voltage may rise. Take care that it does not rise so high that the input voltage exceeds the *Absolute Maximum Ratings* of the LTM4739.

Discontinuous-Conduction Mode Operation

The DCM operation is an optional feature that is used to improve light-load efficiency. The device has a DCM current-detection comparator to monitor the inductor valley current while operating in FCM. At light load, if the inductor valley current is below the DCM comparator threshold for 56 consecutive cycles, the LTM4739 transitions seamlessly to DCM. Once in DCM, the switching frequency decreases as the load decreases. The device transitions back to FCM operation as soon as the inductor valley current is higher than 0A. For LTM4739, the DCM is by default disabled, it can be enabled with PMBus commands.

Shorted Input Protection

Care needs to be taken in systems where the output is held high when the power input to the LTM4739 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR-ed with the LTM4739's output. If the V_{IN} pin is allowed to float and the EN pin is held high (either by a logic signal or because it is connected to V_{IN}), then the LTM4739's internal circuitry pulls its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the EN pin, the internal current drops to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, parasitic diodes inside the LTM4739 can pull large currents from the output through the V_{IN} pin. *Figure 27* shows a circuit that runs only when the input voltage is present, and that protects against a shorted or reversed input. The input diode prevents a shorted input from discharging a backup battery connected to the output. It also protects the circuit from a reversed input. The LTM4739 runs only when the input is present.

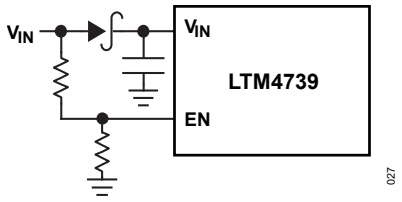


Figure 27. Shorted Input Protection from a Reversed Input

Fault Handling

The LTM4739 features comprehensive fault detection and handling mechanisms to protect both the device and the load. The LTM4739 monitors conditions such as overcurrent (OC), overvoltage (OV), undervoltage (UV), overtemperature (OT), and short-circuit faults. Upon detecting a fault, the device can respond by shutting down or entering safe mode, depending on the configuration. Fault status is communicated via the PMBus, allowing the host (controller) to identify and take corrective action.

Input Undervoltage Lockout

The LTM4739 internally monitors the V_{IN} voltage level. When the input supply voltage is below the undervoltage lockout (UVLO) threshold, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the UVLO status is cleared.

Output Overvoltage Protection

The feedback voltage on V_{SENSE}^+ and V_{SENSE}^- is monitored for the output overvoltage once the soft start ramp is complete. If the feedback voltage is above the overvoltage (OV) protection threshold beyond the OV deglitch filtering delay, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the OV status is cleared.

Positive Overcurrent Protection

The LTM4739's peak current mode control architecture provides inherent current limiting and short-circuit protection. The inductor current is continuously monitored while switching. The inductor peak current is limited on a cycle-by-cycle basis. In each switching cycle, once the sensed inductor current exceeds the overcurrent (OC) protection threshold, the device turns off the high-side MOSFET and turns on the low-side MOSFET to allow the inductor current to be discharged by the output voltage. An up-down counter is used to accumulate the number of consecutive OC events in each switching cycle. If the counter exceeds 1024, the device stops switching and drives the PGOOD pin low. The OC is a hiccup protection, and the device restarts after 20ms.

The LTM4739 offers four OC thresholds (15A, 13A, 11A, and 9A), which can be selected by the PGM0 pin (see the *Pin-Strap Programmability*). Because of the OC deglitch delay, for a specific application use case, the actual OC threshold should be higher.

Besides the current limiting OC protection, the device also features a fast positive overcurrent (FPOC) protection, which is intended to protect against extreme overcurrent conditions, including inductor short or saturation. The FPOC has a threshold of 19A. Once the sensed inductor current exceeds the FPOC threshold, the device stops switching, drives the PGOOD pin low, and latches the device. It requires cycling power to clear the latched FPOC fault and resume operation.

Negative Overcurrent Protection

The device also has negative overcurrent (NOC) protection against inductor valley current. The NOC threshold is –83% of the POC threshold. In each switching cycle, once the sensed inductor current exceeds the NOC threshold, the device turns off the low-side MOSFET and turns on the high-side MOSFET for a fixed 180ns time to allow the inductor current to be charged by the input voltage. Similar to the POC, an up-down counter is used to accumulate the number of consecutive NOC events. If the counter exceeds 1024, the device stops switching and drives the PGOOD pin low. The NOC is a hiccup protection and the device restarts after 20ms.

Overtemperature Protection

The overtemperature (OT) protection threshold is 155°C with 20°C hysteresis. If the junction temperature reaches the OT threshold during operation, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the OT status is cleared.

Hot-Plugging Safely

The small size, robustness, and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM4739. However, these capacitors can cause problems if the LTM4739 is plugged into a live supply (Refer to the Analog Devices *Application Note 88* for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pins of the LTM4739 can ring to more than twice the nominal input voltage, possibly exceeding the LTM4739's rating and damaging the part. If the input supply is poorly controlled or the LTM4739 is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is adding an electrolytic bulk cap to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low-frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Safety Consideration

The LTM4739 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current must be provided to protect each unit from catastrophic failure. The device supports thermal shutdown and overcurrent protection.

Thermal Considerations and Output Current Derating

The LTM4739 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power, and ambient temperature. The derating curves, *Figure 35* through *Figure 42*, can be used as a guide. These curves were generated by the LTM4739 mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load, and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use thermal simulation software to predict thermal performance. The *Pin Configurations and Function Descriptions* section typically gives the following four thermal coefficients.

1. θ_{JA} – Thermal resistance from junction to ambient through the bottom of the package case to the board, see *Figure 28*.
2. θ_{JCbot} – Thermal resistance from the junction.
3. θ_{JCtop} – Thermal resistance from the junction to the top of the package case.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12 and are quoted or paraphrased as follows.

1. θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in one cubic foot sealed enclosure. This environment is sometimes referred to as still air, although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. θ_{JCbot} is the junction-to-board thermal resistance with all the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don't generally match the user's application.
3. θ_{JCtop} is determined with nearly all the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot}, this value may be useful for comparing packages, but the test conditions don't generally match the user's application.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs. load graphs given in the product's datasheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in *Figure 28*. The blue resistances are contained within the µModule regulator, and the green ones are outside.

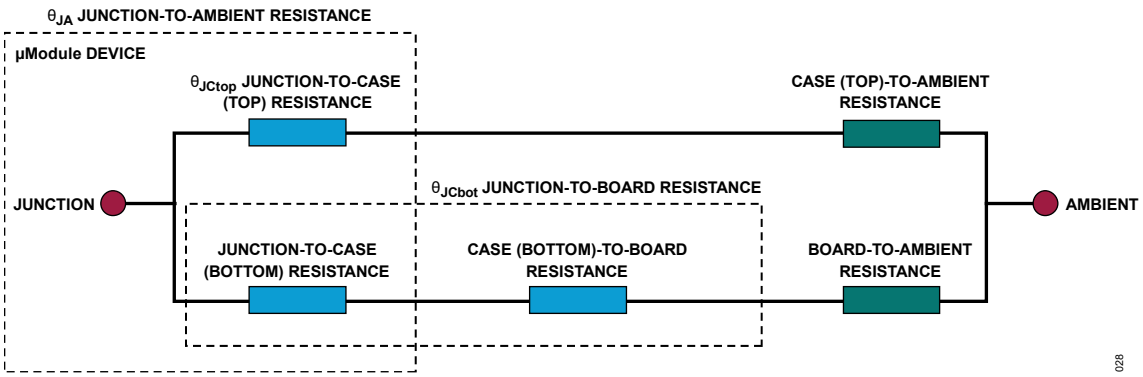


Figure 28. Graphical Representation of the Thermal Resistance between the Device Junction and Ambient, including JESD5112 Terms

Figure 29 shows a temperature plot of the LTM4739 with 12V input, 500kHz, 1V output at 10A without a heat sink and a no airflow condition.

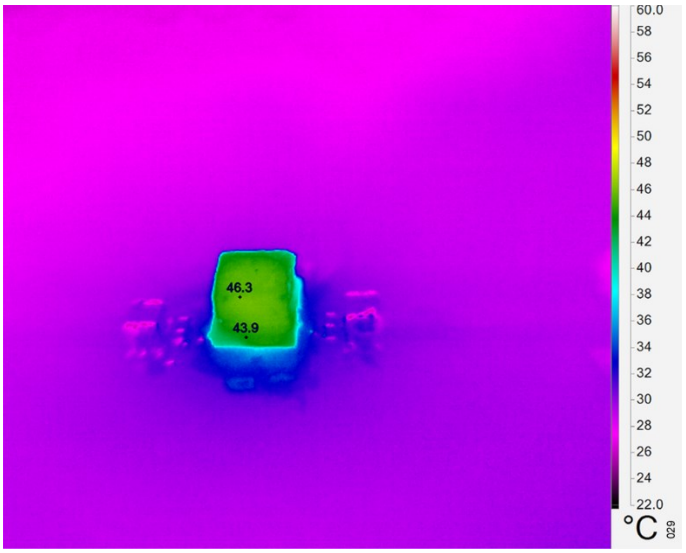


Figure 29. Thermal Image at $12V_{IN}$, 1V, 10A Output, No Airflow and Heat Sink, T_A = 25°C.

The die temperature of the LTM4739 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM4739. The bulk of the heat flow out of the LTM4739 is through the bottom of the package and the pads into the printed circuit board. Consequently, a poor Printed circuit board (PCB) design can cause excessive heating, resulting in impaired performance or reliability. See the *PCB Layout Recommendations* section for printed circuit board design suggestions.

Thermal Derating Curves

The thermal derating curves in *Figure 30* through *Figure 42* can be used to calculate approximate values of θ_{JA} thermal resistance with various airflow conditions.

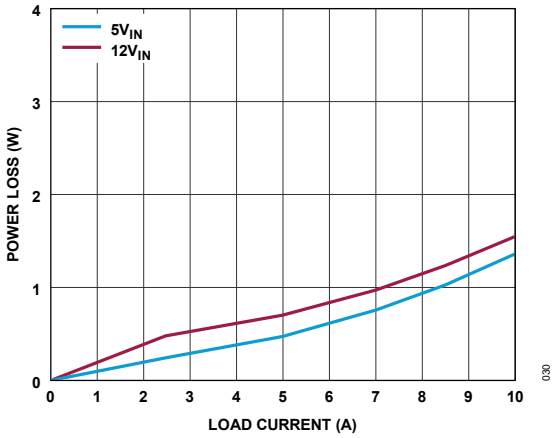


Figure 30. Thermal Derating, Power Loss vs. Load Current, V_{OUT} = 1V, f_{SW} = 500kHz, No V_{BIAS}

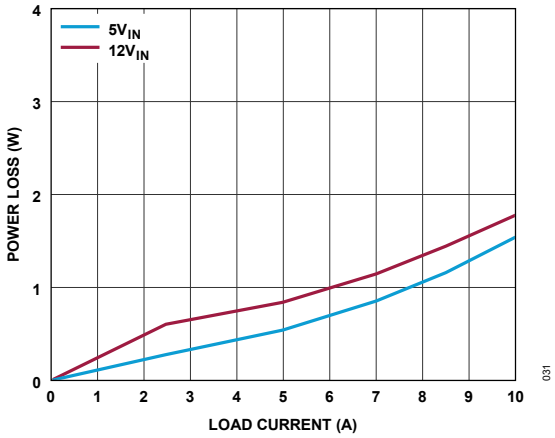


Figure 31. Thermal Derating, Power Loss vs. Load Current, V_{OUT} = 1.5V, f_{SW} = 750kHz, No V_{BIAS}

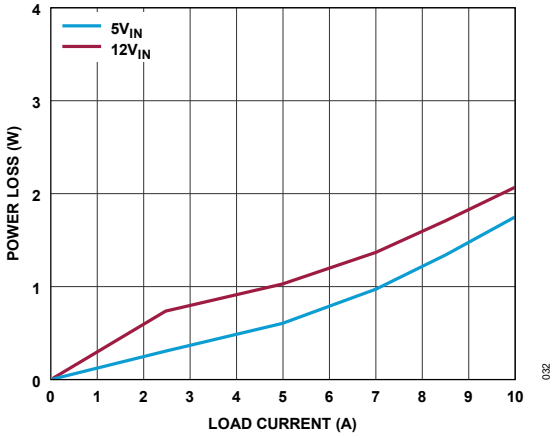


Figure 32. Thermal Derating, Power Loss vs. Load Current, V_{OUT} = 2.5V, f_{SW} = 1MHz, No V_{BIAS}

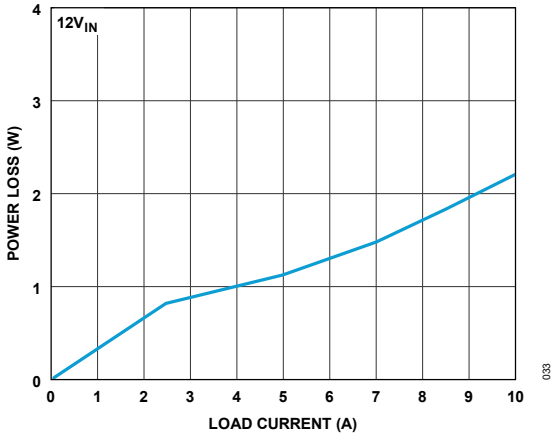


Figure 33. Thermal Derating, Power Loss vs. Load Current, V_{OUT} = 3.3V, f_{SW} = 1MHz, No V_{BIAS}

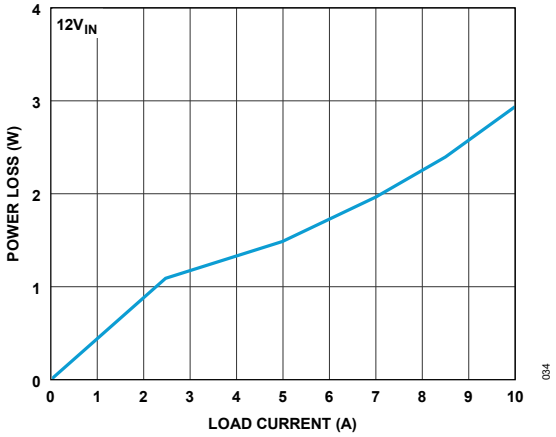


Figure 34. Thermal Derating, Power Loss vs. Load Current, V_{OUT} = 5V, f_{SW} = 2MHz, No V_{BIAS}

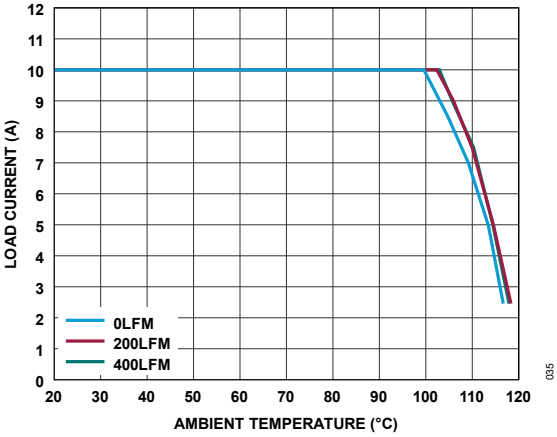


Figure 35. Derating Curve, No Heat Sink, V_{IN} = 5V, V_{OUT} = 1V, f_{SW} = 500kHz

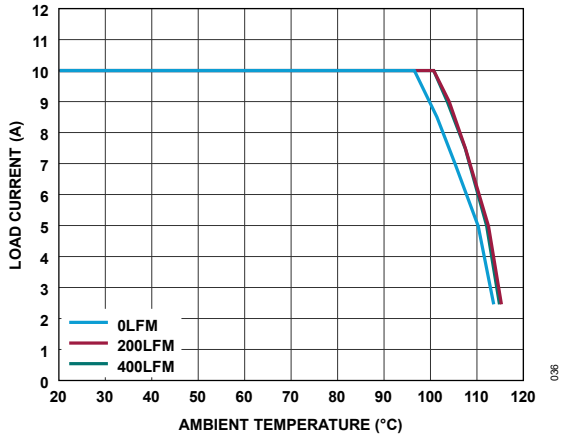


Figure 36. Derating Curve, No Heat Sink, V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 500kHz

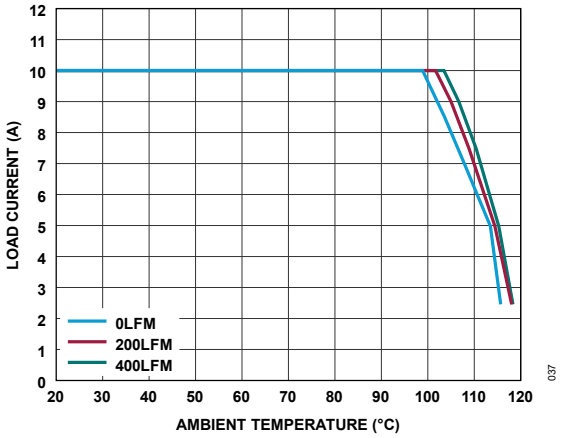


Figure 37. Derating Curve, No Heat Sink, V_{IN} = 5V, V_{OUT} = 1.5V, f_{SW} = 750kHz

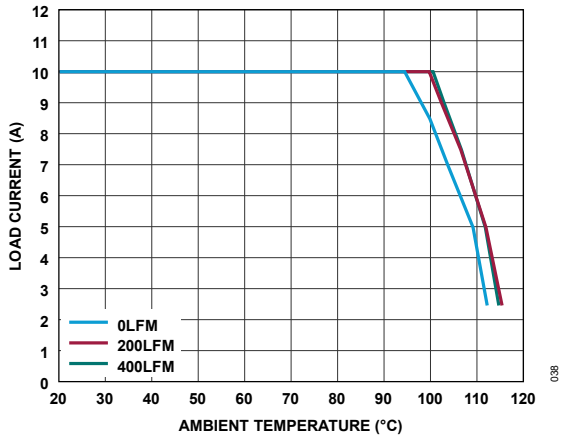


Figure 38. Derating Curve, No Heat Sink, V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 750kHz

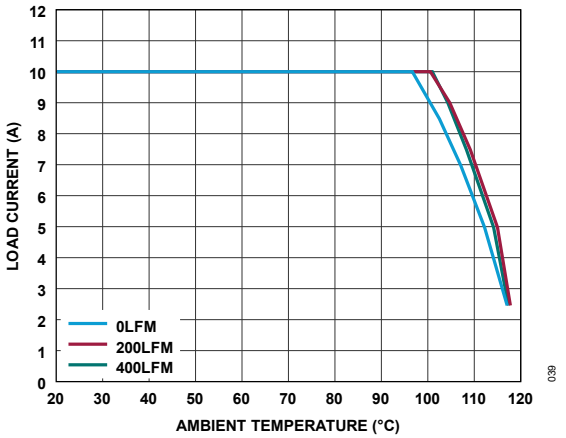


Figure 39. Derating Curve, No Heat Sink, V_{IN} = 5V, V_{OUT} = 2.5V, f_{SW} = 1MHz

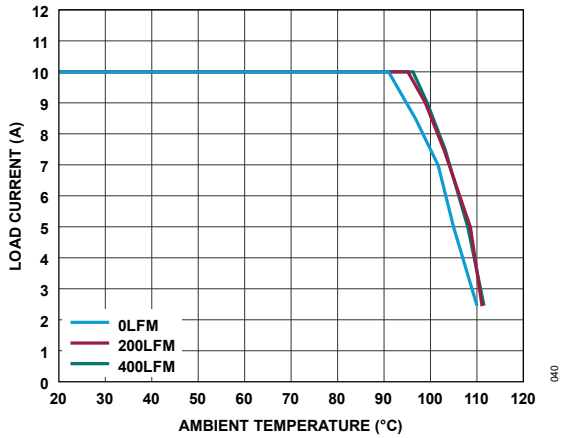


Figure 40. Derating Curve, No Heat Sink, V_{IN} = 12V, V_{OUT} = 2.5V, f_{SW} = 1MHz

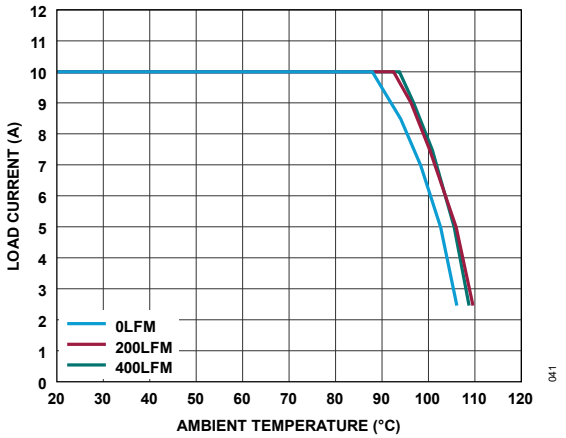


Figure 41. Derating Curve, No Heat Sink, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz

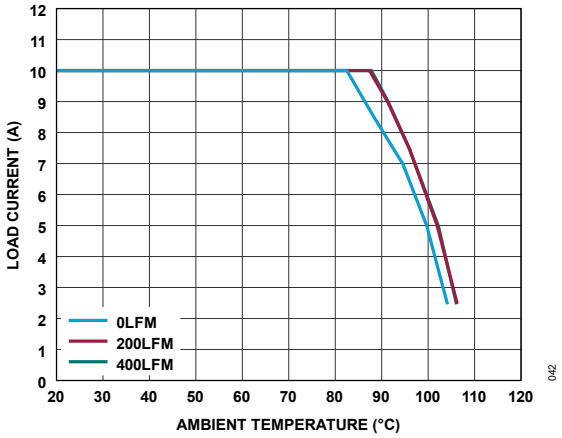


Figure 42. Derating Curve, No Heat Sink, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2MHz

Table 11. 1V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 35, Figure 36	5, 12	*Figure 30*	0	None	14.81, 14.94
Figure 35, Figure 36	5, 12	*Figure 30*	200	None	12.71, 12.27
Figure 35, Figure 36	5, 12	*Figure 30*	400	None	12.37, 12.3

Table 12. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 37, Figure 38	5, 12	*Figure 31*	0	None	13.63, 14.20
Figure 37, Figure 38	5, 12	*Figure 31*	200	None	11.74, 11.27
Figure 37, Figure 38	5, 12	*Figure 31*	400	None	10.83, 10.93

Table 13. 2.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 39, Figure 40	5, 12	*Figure 32*	0	None	13.21, 13.86
Figure 39, Figure 40	5, 12	*Figure 32*	200	None	10.88, 11.80
Figure 39, Figure 40	5, 12	*Figure 32*	400	None	10.66, 11.28

Table 14. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 41	12	*Figure 33*	0	None	14.4
Figure 41	12	*Figure 33*	200	None	12.24
Figure 41	12	*Figure 33*	400	None	11.7

Table 15. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 42	12	*Figure 34*	0	None	12.74
Figure 42	12	*Figure 34*	200	None	11
Figure 42	12	*Figure 34*	400	None	10.84

PCB Layout Recommendations

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM4739. The LTM4739 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve the specified operation with a haphazard or poor layout. See *Figure 43* for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

The following are a few rules to keep in mind.

1. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM4739.
2. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM4739.
3. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent to or underneath the LTM4739.
4. Connect all the GND connections to as large a copper pour or plane area as close as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM4739.
5. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in *Figure 43*. The LTM4739 can benefit from the heatsinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.
6. The feedback resistor divider and the optional external compensation network should be placed as close as possible to the LTM4739 to minimize the noise injection.

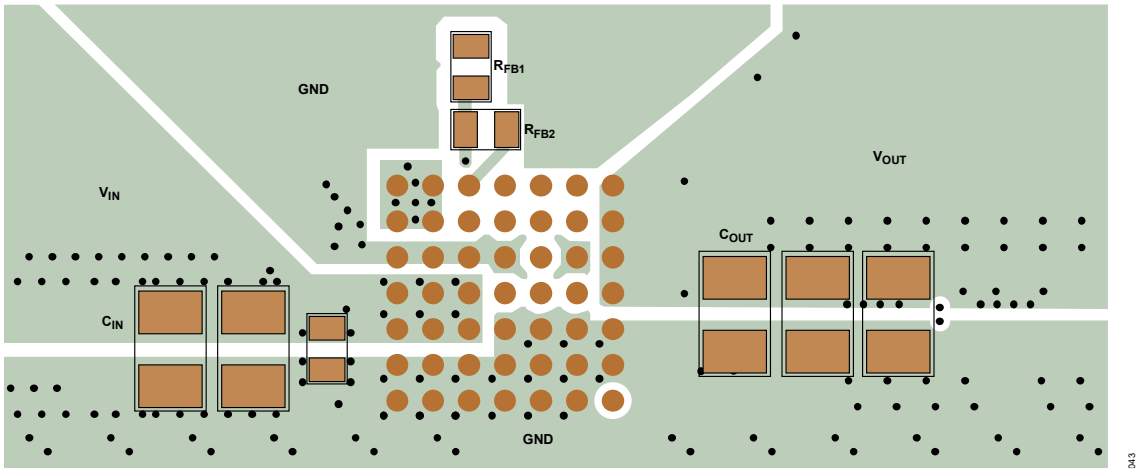


Figure 43. Recommended PCB Layout showing suggested External Components, GND Plane, and Thermal Vias

Typical Applications

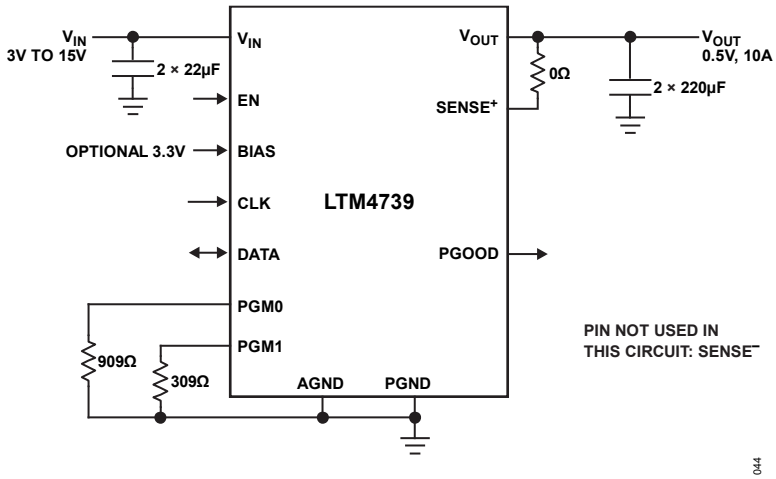


Figure 44. 0.5V, 10A Load from 3V to 15V Input, 500kHz Switching Frequency Design

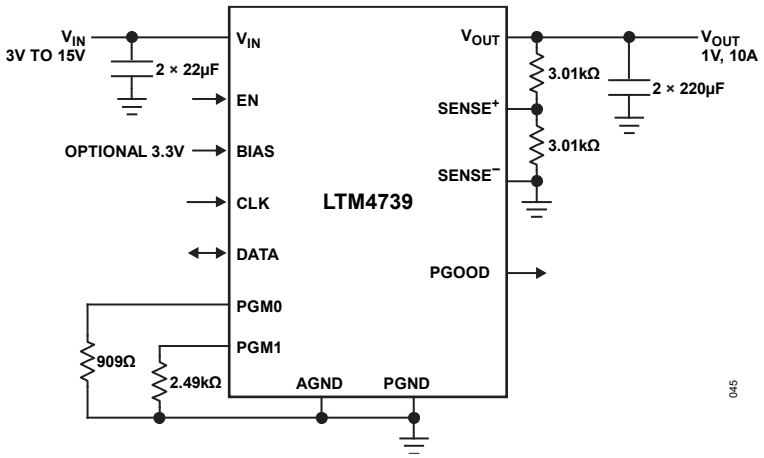


Figure 45. 1V, 10A Load from 3V to 15V Input, 750kHz Switching Frequency Design

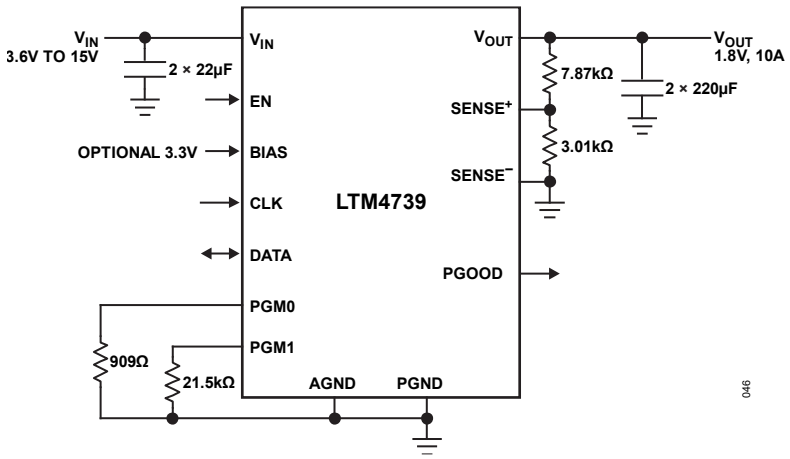


Figure 46. 1.8V, 10A Load from 3.6V to 15V Input, 1MHz Switching Frequency Design

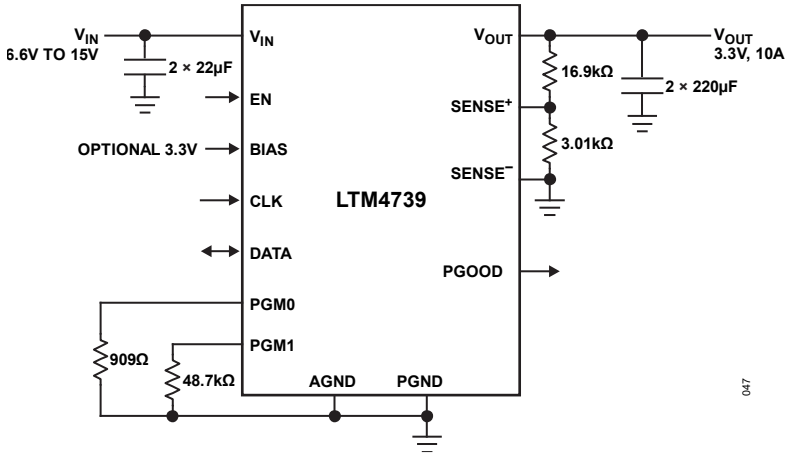


Figure 47. 3.3V Output, 10A Load from 6.6V to 15V Input, 1.2MHz Switching Frequency Design

Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LTM4657	8A µModule regulator, pin compatible with LTM4626, LTM4638, and LTM4640	$3.1V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 3.87mm BGA
LTM4626	12A µModule regulator, pin compatible with LTM4657, LTM4638, and LTM4640	$3.1V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 3.87mm BGA
LTM4638	15A µModule regulator, pin compatible with LTM4657, LTM4626, and LTM4640	$3.1V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 5.02mm BGA
LTM4640	20A µModule regulator, pin compatible with LTM4657, LTM4626, and LTM4638	$3.1V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 3.3V$, 6.25mm × 6.25mm × 5.07mm BGA
LTM4702	10A Silent Switcher®3 µModule regulator, pin compatible with LTM4703 and LTM4707	$3V \le V_{IN} \le 16V$, $0.3V \le V_{OUT} \le 6V$, 6.25mm × 6.25mm × 5.07mm BGA
LTM4703	12A Silent Switcher 3 µModule regulator, pin compatible with LTM4702 and LTM4707	$3V \le V_{IN} \le 16V$, $0.3V \le V_{OUT} \le 6V$, 6.25mm × 6.25mm × 5.07mm BGA
LTM4707	15A Silent Switcher 3 µModule regulator, pin compatible with LTM4702 and LTM4703	$3V \le V_{IN} \le 16V$, $0.3V \le V_{OUT} \le 6V$, 6.25mm × 6.25mm × 5.07mm BGA
LTM4686	Ultrathin dual 10A or single 20A µModule regulator with digital power system management	$4.5V \le V_{IN} \le 15V$, $0.6V \le V_{OUT} \le 3.6V$, 11.9mm × 16mm × 1.82mm LGA
LTM4686-1	Ultrathin dual 10A or single 20A µModule regulator with digital power system management	$2.375V \le V_{IN} \le 17V$ with $5V_{BIAS}$, $0.6V \le V_{OUT} \le 3.6V$, 11.9mm × 16mm × 1.82mm LGA
LTM4675	Dual 9A or single 18A step-down µModule regulator with digital power system management	$4.5V \le V_{IN} \le 17V$, $0.5V \le V_{OUT} \le 5.5V$, 11.9mm × 16mm × 5.01mm BGA
LTM4676A	Dual 13A or single 26A step-down µModule regulator with digital power system management	$4.5V \le V_{IN} \le 26.5V$, $0.5V \le V_{OUT} \le 5.5V$, 16mm × 16mm × 5.01mm BGA
LTM4677	Dual 18A or single 36A step-down µModule regulator with digital power system management	$4.5V \le V_{IN} \le 16V$, $0.6V \le V_{OUT} \le 1.8V$, 16mm × 16mm × 5.01mm BGA
LTM4678	Dual 25A or single 50A µModule regulator with digital power system management	$4.5V \le V_{IN} \le 16V$, $0.5V \le V_{OUT} \le 3.3V$, 16mm × 16mm × 5.86mm BGA

OUTLINE DIMENSIONS

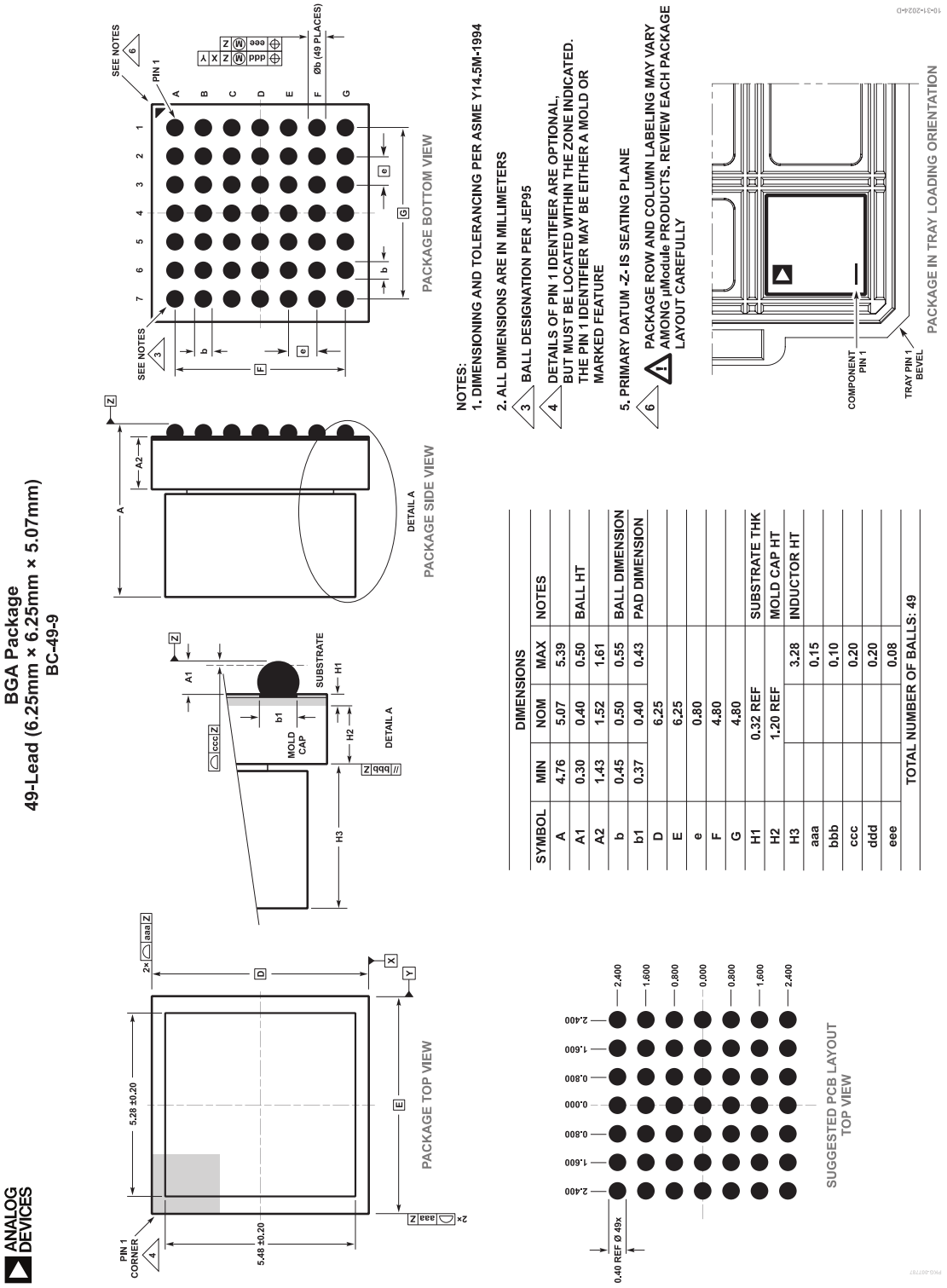


Figure 48. 49-Lead 6.25mm × 6.25mm × 5.07mm BGA

ORDERING GUIDE

Table 16. LTM4739 Ordering Information

MODEL[4]	TEMPERATURE RANGE[1, 2]	PACKAGE DESCRIPTION	PACKAGE OPTION[6]
LTM4739EY#PBF	–40°C to 125°C	Part marking: 4739 SAC305 (RoHS) pad finish[3] e1 finish code Moisture sensitivity level 4 (MSL 4) rated device [5]	*49-Lead 6.25mm × 6.25mm × 5.07mm* BGA
LTM4739IY#PBF	–40°C to 125°C	Part marking: 4739 SAC305 (RoHS) pad finish[3] e1 finish code Moisture sensitivity level 4 (MSL 4) rated device[5]	*49-Lead 6.25mm × 6.25mm × 5.07mm* BGA

1 The LTM4739 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4739E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4739I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

2 Contact the factory for specified parts with wider operating temperature ranges.

3 The pad finish code is per IPC/JEDEC J-STD-609.

4 The device temperature grade is indicated by a label on the shipping container.

5 This product is not recommended for second-side reflow, and it is moisture sensitive. For more information, refer to the Analog Devices *µModule LGA and BGA Packaging Care and Assembly Instructions* document.

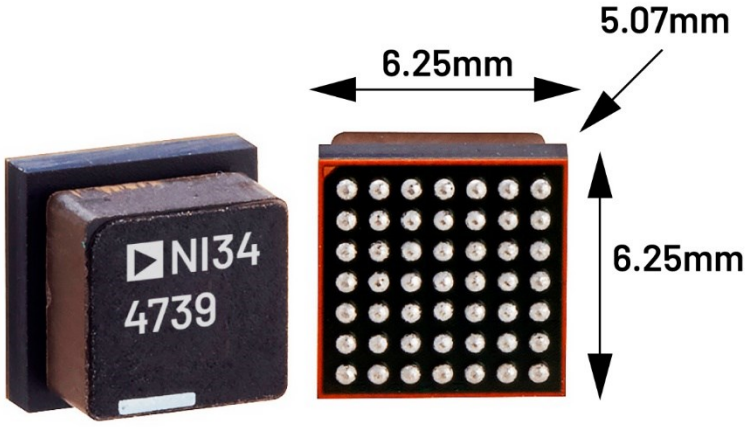
6 The BGA package should follow assembly and manufacturing procedures. For more information, refer to the Analog Devices *Assembly Considerations for the µModule BGA and LGA Packages* guidelines.

Table 17. Evaluation Board Ordering Information

MODEL	DESCRIPTION
EVAL-LTM4739-AZ	15V, 10A µModule regulator evaluation board with PMBus feature.

SELECTOR GUIDE

Package Photos



(Part Marking Is Laser Mark)

Design Resources

Table 18. µModule Power Technology

RESOURCES	DESCRIPTION	
µModule Design, Manufacturing, and Assembly	**Design** ▶ Evaluation board and Gerber files ▶ Free design tools, including LTspice® and LTpowerCAD® ▶ Circuit simulations	**Manufacturing** ▶ Quick start guides ▶ PCB design, assembly, and manufacturing guidelines ▶ Package and board level reliability
µModule Regulator Products Search	▶ Sort table of products by parameters and download the result as a spread sheet. ▶ Search using the Quick Power Search parametric table. Quick Search Input V_{in} (Min) V V_{in} (Max) V Output V_{out} V I_{out} A Features ☐ Low EMI ☐ Ultrathin ☐ Internal Heat Sink Multiple Outputs	
Digital Power System Management	The Analog Devices family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	