Data Sheet

LTM4723

Low V_{IN}, Ultrathin Dual 5A or Single 10A Step-Down DC-to-DC µModule Regulator

FEATURES

- Input Voltage Range: 2.25V to 5.5V
- Programmable 0.5V to 3.6V Output
- Dual 5A or Single 10A Output Current
- ±1% Total Output Voltage Regulation
- Current Mode Control, Fast Transient
- External CLK Synchronization: 1MHz to 3MHz
- 180° Out-of-Phase Operation
- Output Voltage Tracking and Soft-Start
- Burst Selectable Pulse-Skipping Mode (PSM), Burst Mode® Operation, Forced Continuous Mode (FCM) or at Light Load
- Overvoltage, Overcurrent, and Overtemperature Protection
- Available in a Tiny, Ultrathin *36-Terminal, 4.25mm × 4.25mm × 1.15mm,* LGA package

APPLICATIONS

- Optical Module
- Telecom, Networking, and Industrial Equipment
- Field-Programmable Gate Array (FPGA) and Application-Specific Integrated Circuit (ASIC) Core Supplies
- Point-of-Load (POL) Regulation

GENERAL DESCRIPTION

The *LTM4723* is a complete dual 5A output switching mode step-down µModule® (micromodule) DC-to-DC power supply in a tiny 4.25mm × 4.25mm × 1.15mm land grid array (LGA) package. The package includes the switching controller, MOSFETs, inductors, and all supporting components. Operating over an input voltage range of 2.25V to 5.5V, the LTM4723 supports two outputs with a programmable output voltage range of 0.5V to 3.6V set by external resistors. The two outputs can be paralleled for a single 10A load. Only a few ceramic input and output capacitors are needed. The LTM4723 operates in forced continuous mode (FCM) for low-noise, pulse-skipping mode (PSM), or Burst Mode operation for high efficiency at light loads. The LTM4723 supports output voltage tracking for supply-rail sequencing. LTM4723 high switching frequency and current-mode architecture enable a fast transient response to line-and-load changes without sacrificing stability. Other features include precision run thresholds, PGOOD signals, output overvoltage protection, thermal shutdown, and output short-circuit protection. The LTM4723 is a lead (Pb) free and RoHS-compliant device.

TYPICAL APPLICATION

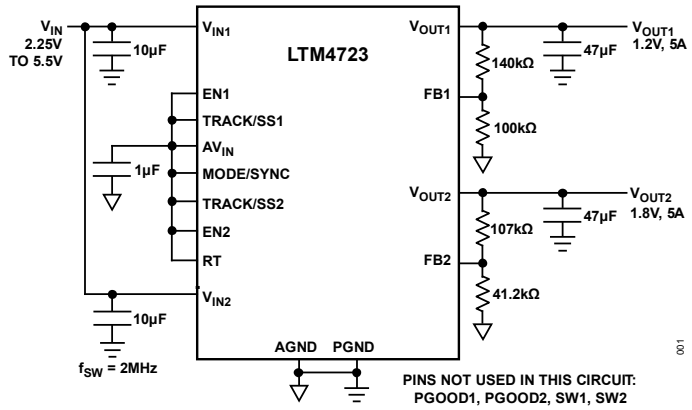


Figure 1. Dual 5A Step-Down µModule Regulator

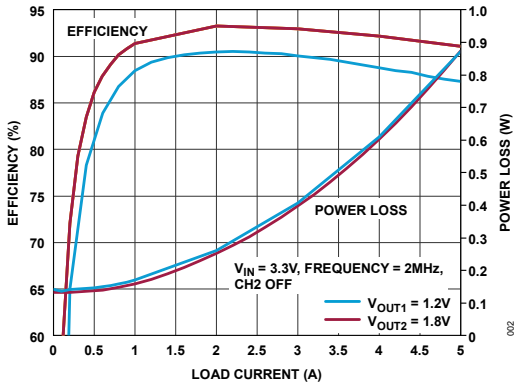


Figure 2. Efficiency vs. Load Current

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	10/26	Initial release.	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C[1], V_{IN} = 3.3V per *Figure 1*, per channel. No output load unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Input DC voltage	V_{IN}	V_{IN} = 2.25V to 5.5V	–40°C ≤ T_J ≤ 125°C	2.25		5.5	V
Output voltage range	$V_{OUT(RANGE)}$	MODE/SYNC = float, V_{IN} = 2.5V to 5.5V, V_{OUT} =1.5V, I_{OUT} = 0A to 5A	–40°C ≤ T_J ≤ 125°C	0.5		3.6	V
V_{IN} undervoltage lockout	$V_{INUVLOR}$	Rising		2.0	2.1	2.2	V
V_{IN} undervoltage lockout hysteresis	$V_{INUVLOHYS}$				150		mV
RUN pin on threshold	V_{RUN}	Rising		0.375	0.4	0.425	V
RUN pin hysteresis	V_{RUNHYS}				50		mV
RUN pin leakage current	I_{RUN}	RUN = 0.4V				±200	nA
Input supply bias current, Burst Mode operation	$I_{Q(VIN)}$	Both bucks enabled, V_{OUT} = 1.5V, MODE/SYNC = V_{IN}			0.09		mA
Input supply bias current, pulse-skipping mode	$I_{Q(VIN)}$	Both bucks enabled, V_{OUT} = 1.5V, MODE/SYNC = GND			1.3		mA
Input supply bias current, forced continuous mode	$I_{Q(VIN)}$	Both bucks enabled, V_{OUT} = 1.5V, MODE/SYNC = float			50		mA
Input supply bias current in shutdown	$I_{Q(VIN)}$	Both bucks disabled			1.3		µA
Input supply current at load, both bucks on	$I_{(VIN)}$	V_{OUT1} = V_{OUT2} = 1.5V, I_{OUT} = 2A per buck			1		A

(T_A = 25°C[1], V_{IN} = 3.3V per *Figure 1*, per channel. No output load unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Output continuous current range (per buck)	$I_{OUT(DC)}$	V_{OUT} = 1.5V				5	A
Line regulation accuracy	$\Delta V_{OUT(LINE)}/V_{OUT}$	V_{OUT} = 1.5V	–40°C ≤ T_J ≤ 125°C		0.01		%
Load regulation accuracy	$\Delta V_{OUT(LOAD)}/V_{OUT}$	V_{OUT} = 1.5, I_{OUT} = 0A to 5A	–40°C ≤ T_J ≤ 125°C			1	%
Output ripple voltage	$V_{OUT(AC)}$	V_{OUT} =1.5V, I_{OUT} = 0A, C_{OUT} =100µF + 22µF ceramic[2]				12	mV
Turn-on overshoot	$\Delta V_{OUT(START)}$	V_{OUT} =1.5V, I_{OUT} = 0A, C_{OUT} =100µF + 22µF ceramic[2]				0	mV
Turn-on time	t_{START}	V_{OUT} =1.5V, C_{OUT} = 100µF + 22µF ceramic, I_{OUT} = 0A, SSTT = 0.1µF[2]			12		ms
Track pin soft-start pull-up current	$I_{TRACK/SS}$	$V_{TRACK/SS}$ = 0.5V			4		µA
Settling time for dynamic load step	t_{SETTLE}	Load: 0% to 60% of full load, C_{OUT} = 100µF + 22µF ceramic[2]			10		µs
Output current limit	I_{OUTPK}	V_{IN} = 3.3V, V_{OUT} = 1.5V			7.5		A
Voltage at V_{FB} pin	V_{FB}		–40°C ≤ T_J ≤ 125°C	0.495	0.50	0.505	V
Current at V_{FB} pin	I_{FB}	V_{FB} = 0.5V				±20	nA
PGOOD trip level as a percentage of V_{OUT}, V_{FB} ramping negative	$V_{PGOODUVLOF}$	V_{FB} ramping negative		–4	–3	–2	%
		V_{FB} ramping positive		7	10	13	%
PGOOD rising threshold		As a percentage of the regulated V_{FB}	–40°C ≤ T_J ≤ 125°C	97	98	99	%

(T_A = 25°C[1], V_{IN} = 3.3V per *Figure 1*, per channel. No output load unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
PGOOD hysteresis		As a percentage of the regulated V_{FB}			1.1		%
Overvoltage rising threshold		As a percentage of the regulated V_{FB}		107	110	114	%
Overvoltage hysteresis		As a percentage of the regulated V_{FB}		1	2.2	3.5	%
PGOOD leakage	I_{PGOOD}	V_{PGOOD} = 5.5V				±50	nA
Oscillator frequency	f_{OSC}	RT = AV_{IN} default RT = 34.8kΩ to AGND			2		MHz
SYNC frequency range	$f_{SYNCRANGE}$			1		3	MHz
Clock level high on SYNC	$SYNC_{LEVEL}$	SYNC = 1.5MHz		1.2			V
Clock level low on SYNC	$SYNC_{LEVEL}$	SYNC = 1.5MHz				0.4	V

1 The LTM4723 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4723E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4723I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

2 Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}, AV_{IN}	–0.3V to 6V
V_{OUT}	–0.3V to V_{IN}
PGOOD	–0.3V to 6V
EN, TRACK/SS, MODE/SYNC, FB, RT	–0.3V to V_{IN}
Operating junction temperature range[1]	–40°C to 125°C
Storage temperature range	–40°C to 150°C
Peak solder reflow body temperature	260°C

1 See the *Output Current Derating Curves* in the *Applications Information* section for different V_{IN}, V_{OUT}, and T_A.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to printed board circuit (PCB) design and operating environment. Close attention to printed circuit board (PCB) thermal design is required.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only: human body model (HBM) per ANSI/ESDA/JEDEC JS-001, field-induced charged device model (FICDM), and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002. International electrotechnical commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2. Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings

Table 3. LTM4723 ESD Ratings

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±4000	3A
CDM	±1250	C3

ESD Caution



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

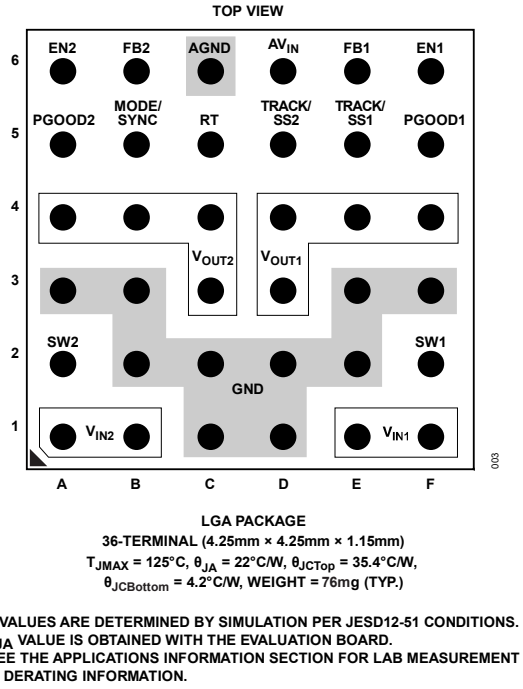


Figure 3. Pinout Configuration

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Pin Descriptions

Table 4. Pin Descriptions

PIN CFG 1	NAME	DESCRIPTION
A1, B1, E1, F1	V_{IN2}, V_{IN1}	Power Input Pins. Apply input voltage between these pins and GND pins. Each V_{IN} should have its own input bypass capacitor. It is recommended to place input decoupling capacitors as close as possible to the pins.
A2, F2	SW2, SW1	Switching Node Internal High-Current Path from the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) to the Inductor. Connect to a solid copper area or leave it floating.
A5, F5	PGOOD2, PGOOD1	Output Power Good Pins with Open-Drain Logic of each Switching Mode Regulator Channel. The PGOOD pins are pulled to ground when the voltage on the FB pin is not within ±8% (typical) of the internal 0.5V reference open-drain output.
A6, F6	EN2, EN1	Active High Enable Input for Each Buck Regulator. The EN pins have a precision threshold and an external resistor divider from each V_{IN}, or another supply can be used to program when the buck regulator is enabled. If the enable function is not required, connect EN directly to AV_{IN} to enable. The EN pins should not be left floating.

PIN CFG 1	NAME	DESCRIPTION
B5	MODE/SYNC	Mode Selection and External Clock Synchronization Input. Ground this pin to enable PSM. For higher efficiency at light loads, connect this pin to AV_{IN} to enable Burst Mode operation. For fast transient response and constant-frequency operation over a wide load range, float this pin to enable FCM. Drive MODE/SYNC with an external clock to synchronize both buck converters to the applied frequency. When syncing, the operating mode is FCM. Slope compensation is automatically adapted to the external clock frequency. Without an external clock, the RT pin controls the switching frequency.
B6, E6	FB2, FB1	Feedback Input for Buck Regulator. It programs the output voltage by connecting this pin to the middle node of a resistor divider between the output and ground; see *Figure 19* for more details. The FB pin is regulated to 500mV. A phase lead capacitor connected between V_{OUT12} and FB12 may be used to optimize transient response.
C1, D1, B2, C2, D2, E2, A3, B3, E3, F3	GND	Power Ground Pins for both Input and Output Returns.
C3, A4, B4, C4, D3, D4, E4, F4	V_{OUT2}, V_{OUT1}	Power Output Pins of each Switching Mode Regulator. Apply the output load between these pins and the GND pins. It is recommended to place output decoupling capacitance directly between these pins and GND pins.
C5	RT	The RT pin sets the switching frequency using an external resistor to AGND. If this pin is connected to AV_{IN}, the buck switches at the default oscillator frequency of 2MHz. If the external clock is driving the MODE/SYNC pin, the RT pin is ignored. See the *Setting the Switching Frequency* in the *Applications Information* section for frequency adjustment.
C6	AGND	Analog Ground Pin. The AGND pin is the ground pin for the internal bias circuits, including the bandgap reference. Connect the bottom resistors of the FB1 and FB2 resistor dividers to the AGND pin for accurate output voltage regulation.
D5, E5	TRACK/SS2, TRACK/SS1	Soft-Start, Tracking, Temperature Monitor Input for both Buck Regulators. An internal 4µA current into an external capacitor on the soft-start pin programs the output voltage ramp rate at startup. When the TRACK/SS pin is below 0.5V, the FB pin voltage tracks the TRACK/SS pin voltage. When the TRACK/SS is above 0.5V, the tracking function is disabled, the internal reference resumes control of the error amplifier, and the TRACK/SS pin servos to a voltage proportional to the junction temperature. For a clean recovery from an output short-circuit condition, the TRACK/SS pin is pulled down to approximately 100mV above the V_{FB} voltage, and a new soft start cycle is initiated. During shutdown and fault conditions, the TRACK/SS pin is pulled to ground. Short the TRACK/SS pin to AV_{IN} to use an internally set default soft start time of 1ms (typical).
D6	AV_{IN}	Filtered input supply used to bias the internal bandgap reference and buck control circuits. There are 20Ω internal resistors from V_{IN1} to AV_{IN}, and from V_{IN2} to AV_{IN}. Do not externally load these pins.

Table 5. LTM4723 Pinout (Sorted by Pin Number, Alphanumerical)

PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME
A1 TO F3					
A1	V_{IN2}	A2	SW2	A3	GND
B1	V_{IN2}	B2	GND	B3	GND
C1	GND	C2	GND	C3	V_{OUT2}
D1	GND	D2	GND	D3	V_{OUT1}
E1	V_{IN1}	E2	GND	E3	GND
F1	V_{IN1}	F2	SW1	F3	GND
A1 TO F3					
A4	V_{OUT2}	A5	PGOOD2	A6	EN2
B4	V_{OUT2}	B5	MODE/SYNC	B6	FB2
C4	V_{OUT2}	C5	RT	C6	AGND
D4	V_{OUT1}	D5	TRACK/SS2	D6	AV_{IN}
E4	V_{OUT1}	E5	TRACK/SS1	E6	FB1
F4	V_{OUT1}	F5	PGOOD1	F6	EN1

TYPICAL PERFORMANCE CHARACTERISTICS

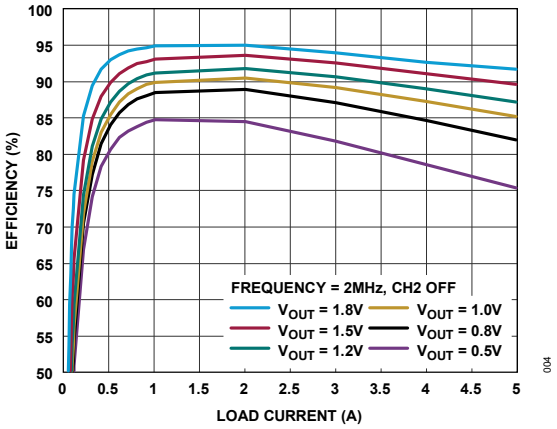


Figure 4. Efficiency vs. Load Current at 2.5V_{IN}

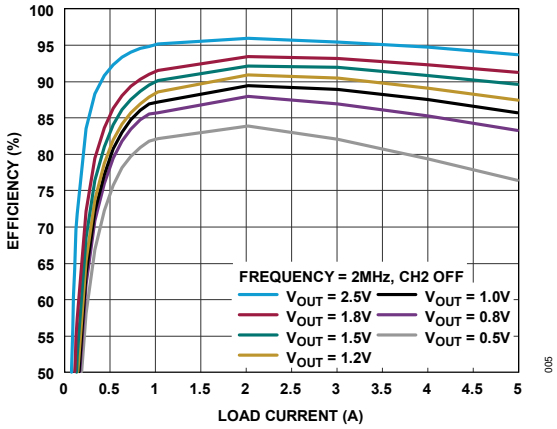


Figure 5. Efficiency vs. Load Current at 3.3V_{IN}

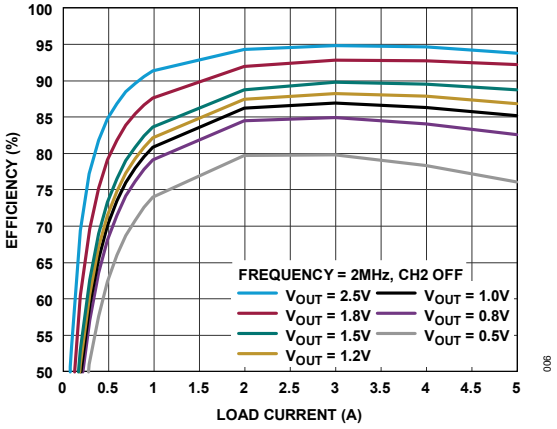


Figure 6. Efficiency vs. Load Current at 5V_{IN}

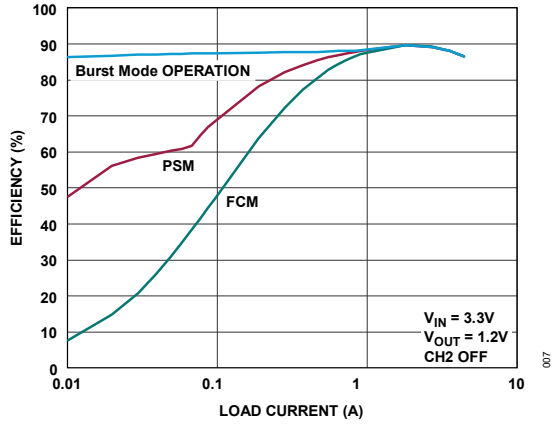


Figure 7. Efficiency vs. Load Current at 3.3V and Different Modes of Operation

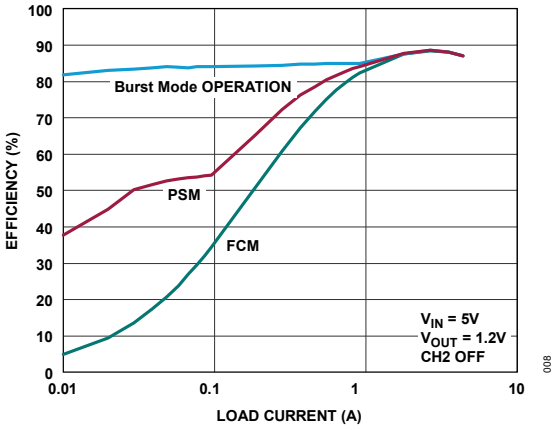


Figure 8. Efficiency vs. Load Current at 5V and Different Modes of Operation

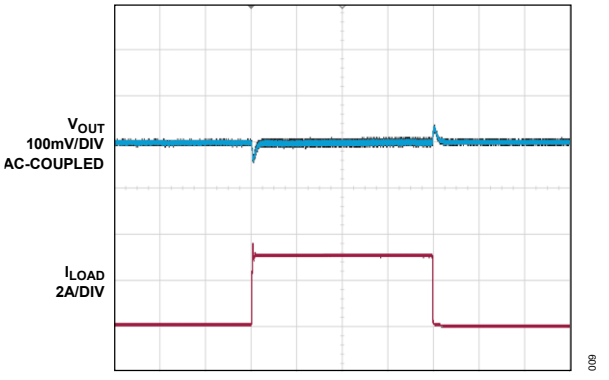


Figure 9. Output Transient Response

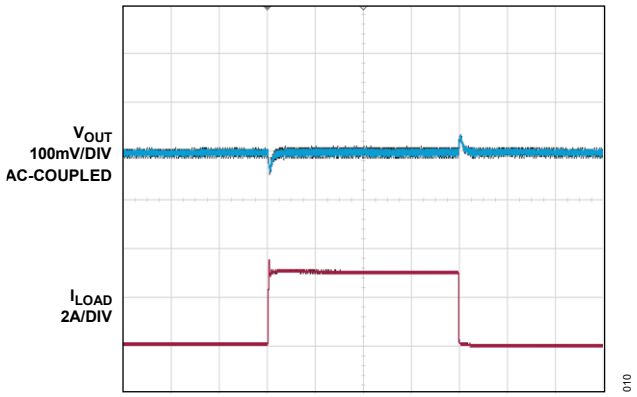


Figure 10. Output Transient Response

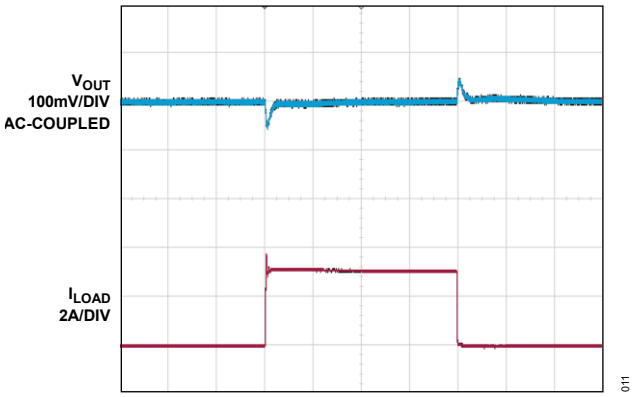


Figure 11. Output Transient Response

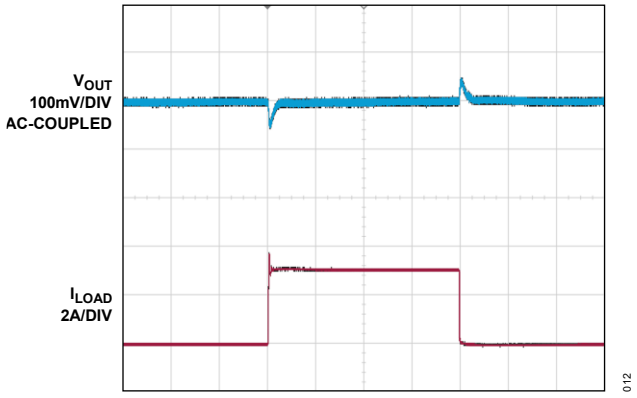


Figure 12. Output Transient Response

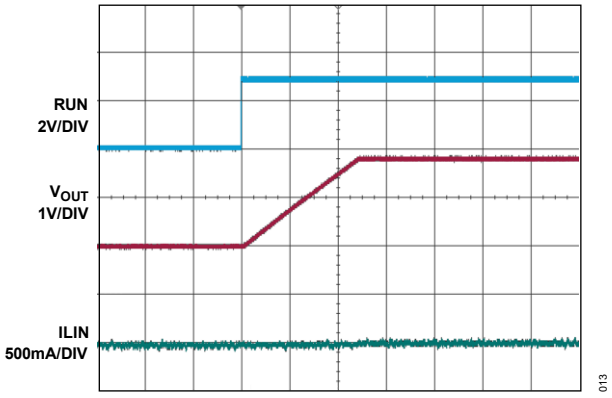


Figure 13. Startup, No Load

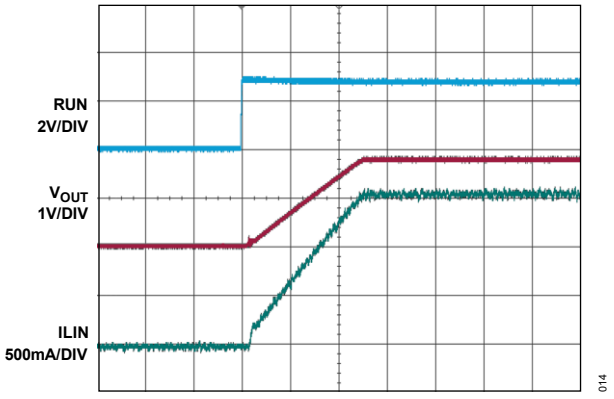


Figure 14. Startup, 5A Load

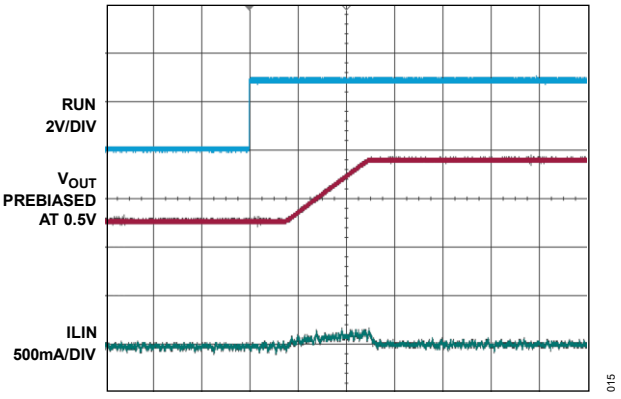


Figure 15. Startup, Prebiased Output, No Load

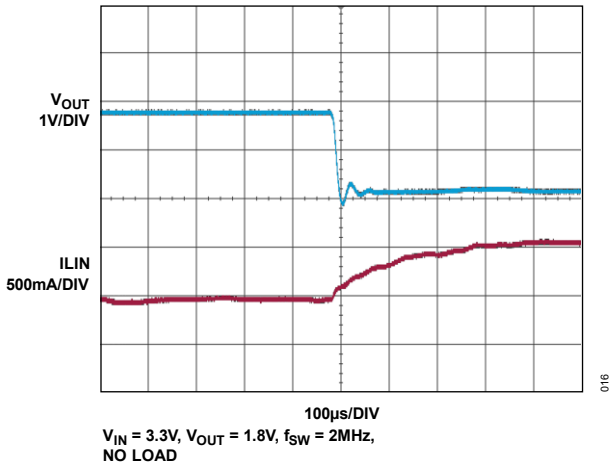


Figure 16. Short-Circuit, No Load

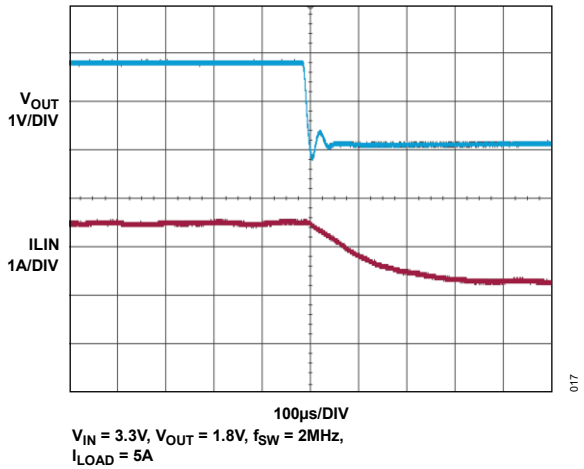


Figure 17. Short-Circuit, Full Load

THEORY OF OPERATION

Dual Buck Switching Regulators

The LTM4723 is a 5V dual 5A, constant-frequency, peak current mode step-down DC-to-DC µModule regulator. The synchronous buck switching regulators are internally compensated and require only external feedback resistors to set the output voltage. See *Figure 18* for the simplified block diagram.

An internal oscillator, with frequency set using a resistor on the RT pin, or synchronized to an external clock, turns on the internal top power switch at the start of each clock cycle (the clock's rising edge for Buck 1). Inductor Current increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by an internal V_C voltage. The error amplifier regulates V_C by comparing the voltage on the FB pin with an internal 500mV reference. When the load current increases, the feedback voltage drops relative to the reference, causing the error amplifier to raise V_C until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on and ramps down the inductor current for the remainder of the clock cycle, or if in PSM or Burst Mode operation, until the inductor current falls to zero. If overload conditions cause excessive current flowing through the bottom switch, the next clock cycle is skipped until the switch current returns to a safe level. The top switches of the two buck regulators are turned on 180 degrees out-of-phase to reduce input current ripple.

Each buck switching regulator has its own SW, FB, TRACK/SS, PGOOD, and EN pins. The enable pins have precision 400mV thresholds, which provide event-based power-up sequencing by connecting the enable pin to the output of another buck through a resistor divider. If a buck's EN pin is low, the buck is in shutdown and in a low quiescent-current state. If both EN pins are low, both bucks are in shutdown. The SW pins are high impedance, and the quiescent current of the LTM4723 is 1.3µA (typical). If either EN pin exceeds the 400mV enable threshold, its respective buck is enabled.

Both buck regulators have forward and reverse current limiting, short-circuit protection, output overvoltage protection, and soft start to limit inrush current during startup or recovery from a short-circuit.

Block Diagram

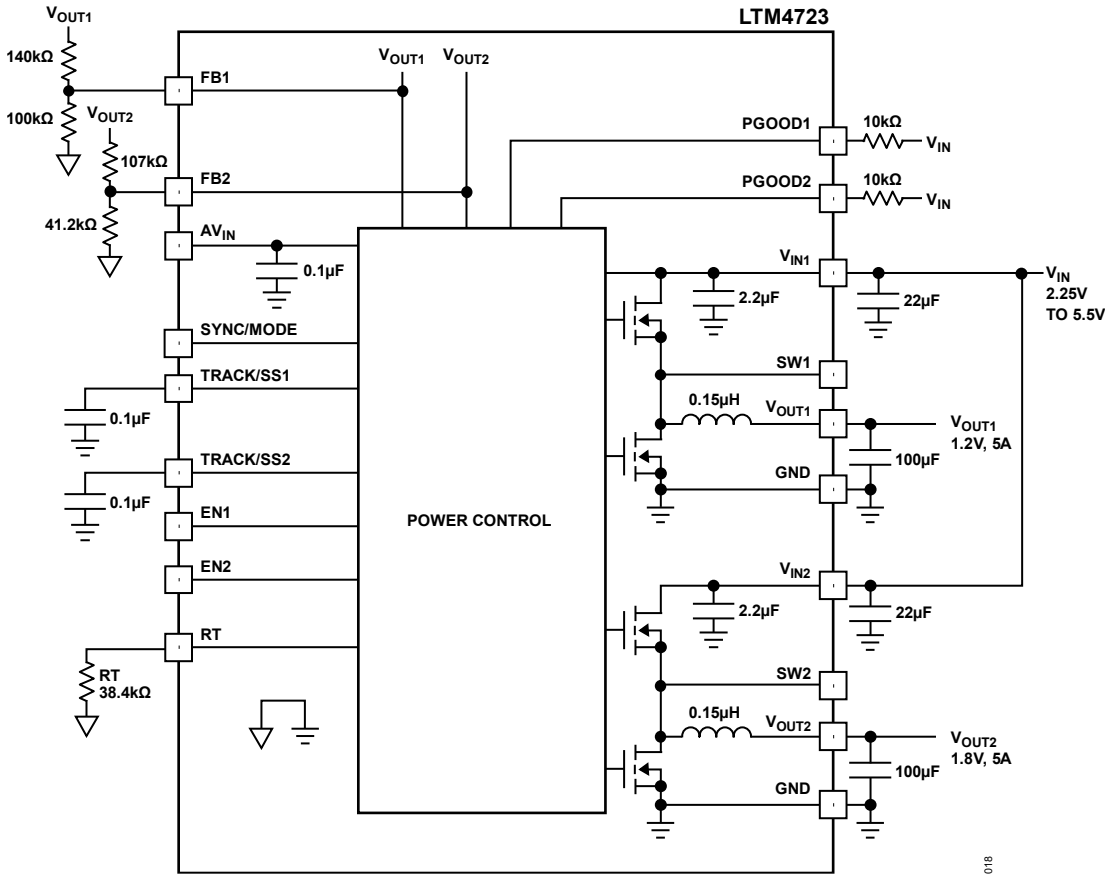


Figure 18. LTM4723 Simplified Block Diagram

Decoupling Requirements

Table 6. Decoupling Requirements

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN12}	External input capacitor requirement (V_{IN} = 2.25V to 5.5V, V_{OUT} = 1.5V)	I_{OUT} = 3A (each channel)	22 (each channel)			µF
C_{OUT12}	External output capacitor requirement (V_{IN} = 2.25V to 5.5V, V_{OUT} = 1.5V)	I_{OUT} = 3A (each channel)	47 (each channel)			µF

2-Phase, Single Output Operation

The LTM4723 is easily configured as a single-output, 2-phase, 10A buck regulator by connecting the FB2 and TRACK/SS pins to AV_{IN}, and connecting the EN2 pin to AGND. The PGOOD2 pin can be floated or shorted to ground. The EN1 pin enables both power stages, and the PGOOD1 pin functions as the power good indicator. The LTM4723 detects if the FB2 pin is connected high, and it uses the error-amplifier output (V_C) for Buck 1 to control the peak inductor current for both buck power stages. The top switches of the two phases are turned on 180 degrees out-of-phase to reduce input current ripple. The difference between the peak inductor currents of the two phases is determined by internal matching, typically within 10% of each other at high currents.

The total capacitance on the 2-phase output should be double of what is calculated for a single phase 5A buck (see *Applications Information* section for output capacitor selection). When waking up from sleep, in Burst Mode operation, the top switches of the two phases are turned on initially without a delay, to improve the transient response coming out of sleep. The 180° phase difference starts on the subsequent turn-on after exiting sleep.

Input Supply

The AV_{IN} pin is a noise-filtered version of V_{IN} used to bias the internal bandgap reference and buck control circuits. Connect a 1µF external filter capacitor from AV_{IN} to AGND, and ensure the external circuits draw no current. The AV_{IN} pin connects to V_{IN1} and V_{IN2} pins through internal 20Ω filter resistors. The V_{IN1} and V_{IN2} pins are not connected internally and should be externally shorted to a single input supply. Each V_{IN} pin should have its own input bypass capacitor to PGND.

Mode Selection

The buck switching regulators operate in the following three different modes set by the MODE/SYNC pin.

1. PSM (when the MODE/SYNC pin is connected to AGND).
2. FCM (when the MODE/SYNC pin is floating).
3. Burst Mode operation (when the MODE/SYNC pin is connected to AV_{IN}).

The MODE/SYNC pin sets the operating mode for both buck switching regulators. In PSM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. Negative inductor current is disallowed, and the switch skips pulses at light loads to regulate the output voltage. In FCM, the oscillator operates continuously. The top switch turns on every cycle, and regulation is maintained by allowing the inductor current to reverse at light load. This mode allows the buck to run at a fixed frequency with minimal output ripple. In FCM, if the inductor current reaches 5A (typical) into the SW pin, the bottom switch turns off for the remainder of the cycle to limit the current. In Burst Mode operation at light loads, the output capacitor is charged to a voltage slightly higher than its regulation point. The regulator then enters into a sleep state, during which the output capacitor provides the load current. In sleep, most of the regulator's circuitry is powered down, helping conserve input power. When the output voltage drops below its programmed value, the circuitry powers on and another burst cycle begins. The sleep time decreases as load current increases. In Burst Mode operation, the regulator bursts at light loads, whereas at higher loads it operates in constant frequency pulse-width modulation (PWM) mode.

Synchronizing the Oscillator to an External Clock

The LTM4723's internal oscillator is synchronized through an internal phase-locked loop (PLL) circuit to an external frequency by applying a square-wave clock signal to the MODE/SYNC pin. During synchronization, the Buck 1 top power switch turn-on is locked to the rising edge of the external frequency source. The Buck 2 top switch turns on 180° out of phase with respect to Buck 1. While synchronizing, the buck switching regulators operate in FCM. Slope compensation automatically adapts to the external clock frequency. The synchronization frequency range is 1MHz to 3MHz.

After detecting an external clock on the first rising edge of the MODE/SYNC pin, the internal PLL gradually adjusts its operating frequency to match the frequency and phase of the signal on the MODE/SYNC pin. When the external clock is removed, the LTM4723 detects the absence of the external clock within approximately 10µs. During this time, the PLL continues to provide clock cycles. Once the external clock removal has been detected, the oscillator gradually adjusts its operating frequency to the one programmed by the RT pin.

Output Power Good

Both buck switching regulators have an external open-drain PGOOD pin, each operating independently of the other. When a buck output voltage is within the –2/+10% (typical) window of the nominal regulation voltage, the output is considered good. The corresponding open-drain PGOOD pin goes high impedance and is typically pulled high with an external resistor. Otherwise, an internal pull-down device pulls the corresponding PGOOD pin low. Each PGOOD pin is also pulled low during the following fault conditions: When the corresponding buck EN pin is low, V_{IN} is too low, or during thermal shutdown. To filter noise and short duration output voltage transients, the lower thresholds have a hysteresis of 1.1% (typical), the upper thresholds have a hysteresis of 2.2% (typical), and transitions of the PGOOD pins have a built-in time delay, typically 100µs.

Output Overvoltage Protection

If there is an output overvoltage event, which occurs when the FB pin voltage is greater than 110% of nominal, the buck regulator's top power switch is turned off. If the output remains out of regulation for more than 100µs, the PGOOD pin is pulled low. An output overvoltage should not happen under normal operating conditions.

Overtemperature Protection

To prevent thermal damage to the LTM4723, the device incorporates an overtemperature (OT) function. If the die temperature reaches 165°C (typically, not tested), both buck switching regulators shutdown and remain shutdown until the die temperature falls to 160°C (typically, not tested).

Soft Start/Tracking/Temperature Monitor

The soft-start tracking function facilitates supply sequencing, limits V_{IN} inrush current, and reduces startup output overshoot. Each buck regulator has a TRACK/SS pin, that sources a 4µA current when the buck is enabled. When the TRACK/SS pin voltage is low, it replaces the 500mV reference, normally used to regulate the FB voltage. A capacitor from the TRACK/SS pin to ground can set the soft-start ramp time for each buck regulator. When soft-starting is completed, each TRACK/SS pin parks itself at a voltage representative of the LTM4723 die junction temperature. An alternative is to connect an TRACK/SS pin to AV_{IN}, which selects an internally set 1ms default soft-start time for that buck regulator.

An active pull-down circuit is connected to either the TRACK/SS pin, or to the internal soft start node if TRACK/SS is connected high. This is used to discharge it in the case of fault conditions. The soft-start ramp restarts when the fault is cleared. The fault conditions that clear the soft start voltage ramp are: the EN pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Dropout Operation

As the input supply voltage approaches the output voltage, the duty-cycle increases until SW is low for a minimum time of 30ns (typical). Further reduction of the supply voltage forces the main switch to remain on for more than one cycle, allowing the duty-cycle to increase despite the internally set minimum SW low time. As the input drops further, the main switch stays on for more cycles, until it reaches the maximum allowed 16 cycles. At least one minimum low time is forced every 16 cycles in dropout, limiting the maximum duty-cycle to 99% (typical). Deep in dropout, the output voltage is approximately determined by 0.99 times the input voltage, minus the voltage drops across the internal high-side MOSFET and the inductor.

Low Supply Operation

The LTM4723 is designed to operate down to an input supply voltage of 2.25V. One important consideration, at low input supply voltages, is that the $R_{DS(ON)}$ of the internal power switches increases. Calculate the worst case LTM4723 power dissipation and the die junction temperature at the lowest input voltages.

Output Short-Circuit Protection and Recovery

The peak inductor current level, at which the current comparator shuts off the top power switch, is controlled by the internal V_C voltage. If the output current increases, the error amplifier raises V_C until the average inductor current matches the load current. The LTM4723 clamps the maximum V_C voltage, thereby limiting the peak inductor current.

When the output is shorted to ground, the inductor current decays very slowly when the bottom power switch is on, because the voltage across the inductor is low. A secondary limit is applied to the inductor current valley to prevent excessive inductor current. If the inductor current, measured through the bottom power switch, is greater than I_{LIMN} at the end of a cycle, the top power switch is held off. Subsequent switching cycles are skipped until the inductor current is reduced below I_{LIMN}.

Recovery from an output short-circuit may involve a soft start cycle if V_{FB} falls more than ~100mV below regulation. During this output short-circuit recovery, the V_{FB} quickly charges up by ~100mV and then follows the soft start ramp until regulation is reached.

APPLICATIONS INFORMATION

Output Voltage and Feedback Network

The buck switching regulator's output voltage is programmed by a resistor divider between the output and the FB pin. Choose the resistor values according to Equation 1.

$$R_A = R_B \left(\frac{V_{OUT}}{500mV} - 1\right) \quad (1)$$

as shown in Figure 19.

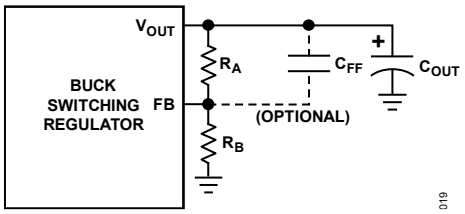


Figure 19. Feedback Components

Typical R_B values range from 40kΩ to 400kΩ. The 0.1% resistors are recommended to maintain output voltage accuracy. The buck regulator transient response can improve with an optional phase lead capacitor C_{FF} that helps cancel the pole created by the feedback resistors and the input capacitance of the FB pin. Experimentation with capacitor values between 2pF and 40pF may improve transient response. The values used in the typical application circuits are a good starting point.

Setting the Switching Frequency

The LTM4723 uses a constant-frequency peak current mode control architecture. Set the switching frequency using one of the following three methods. The first method, connecting the RT pin to V_{IN}, sets the switching frequency to the internal default with a nominal value of 2MHz. The second method, a resistor (R_T) connected from the RT pin to ground. The frequency can be programmed from 1MHz to 3MHz. Table 7 and Equation 2 show the necessary R_T value for a desired switching frequency.

$$R_T = \frac{73.4}{f_{SW}} - 1.9 \quad (2)$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz, ranging from 1MHz to 3MHz.

The third method to set the switching frequency is by synchronizing the internal PLL circuit to an external square-wave clock applied to the MODE/SYNC pin. The synchronization frequency range is 1MHz to 3MHz. The square-wave amplitude should have valleys that are below 0.4V and peaks above 1.2V. High and low pulse widths should both be at least 40ns.

Table 7. R_T Value vs. Switching Frequency

f_{SW} (MHz)	R_T (kΩ)
1.0	71.5
1.2	59.0
1.4	51.1
1.6	44.2
1.8	39.2

f_{SW} (MHz)	R_T (kΩ)
2.0	34.8
2.2	31.6
2.4	28.7
2.6	26.1
2.8	24.3
3.0	22.6

Input Capacitors

Bypass the LTM4723 input with at least two ceramic capacitors close to the part, one near each V_{IN} pin. Connect each capacitor's ground to a wide PCB trace on the top layer of the PCB that connects to GND. See the *PCB Layout Considerations* section for more details. The X7R or X5R capacitors are recommended for best performance across temperature and input voltage variations (see *Table 8*). Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with an electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high-quality (underdamped) tank circuit. If the LTM4723 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LTM4723's voltage rating. This situation can be easily avoided (Refer to the Analog Devices *Application Note AN88*).

Table 8. Ceramic Capacitor Manufacturers

VENDOR	WEBSITE
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com
Taiyo Yuden	www.t-yuden.com
Samsung	www.samsungsem.com
Wurth Elektronik	www.we-online.com

Output Capacitor, Output Ripple, and Transient Response

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LTM4723 to produce the DC output. In this role, it determines the output ripple; thus, low impedance at the switching frequency is important. The second function is to store energy to satisfy transient loads and stabilize the LTM4723's control loop.

The LTM4723 is internally compensated and has been designed to operate at a high bandwidth for fast transient response capability. C_{OUT} selection affects system bandwidth, but V_{OUT}, V_{IN}, f_{SW}, and other factors also affect transient response. A good place to start is with the output capacitor value given by Equation *3*.

$$C_{OUT} = 20 \times \frac{I_{MAX}}{f_{SW}} \sqrt{\frac{0.5}{V_{OUT}}} \qquad (3)$$

where C_{OUT} is the recommended output capacitor value in µF, f_{SW} is the switching frequency in MHz, I_{MAX} = 5A per phase is the rated output current in Amps, and V_{OUT} is in volts. A lower value of output capacitor can be used to save space and cost, but transient performance suffers, and loop stability must be verified.

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best output ripple and transient performance. Use X5R or X7R ceramic capacitors (see *Table 8*). Even better output ripple and transient performance can be achieved by using low-ESL reverse geometry or three-terminal ceramic capacitors.

During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop increases the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. Although affected by V_{OUT}, V_{IN}, f_{SW}, and $t_{ON(MIN)}$, the equivalent series inductance (ESL) of the output capacitor, and other factors. The output droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle (Equation *4*).

$$V_{DROOP} = \frac{3 \times \Delta I_{OUT}}{C_{OUT} \times f_{SW}} \qquad (4)$$

Transient performance and control loop stability can be improved with a higher C_{OUT} and/or the addition of a feedforward capacitor C_{FF} placed between V_{OUT} and FB. Capacitor C_{FF} provides phase-lead compensation by creating a high-frequency zero, which improves the phase margin and the high-frequency response. The values used in the typical application circuits are good starting points. The *LTpowerCAD®* is a useful tool for optimizing C_{FF} and C_{OUT} for a desired transient performance.

Applying a load transient and monitoring the system's response, or using a network analyzer to measure the actual loop response, are two ways to experimentally verify transient performance and control loop stability, and to optimize C_{FF} and C_{OUT}.

When using the load transient response method to stabilize the control loop, apply an output current pulse of 20% to 100% of full-load current with a very fast rise time. This produces a transient on the output voltage. Monitor V_{OUT} for overshoot or ringing that would indicate a stability problem (Refer to the Analog Devices *Application Note AN149*).

Output Voltage Sensing

The LTM4723's AGND pin is the ground reference for the internal analog circuitry, including the bandgap voltage reference. For the single-output, 2-phase application, load regulation can be improved by connecting the AGND pin to the negative terminal of the output capacitor (C_{OUT}) at the load. Any drop in the high-current power ground return path is compensated. All the signal components, such as the FB resistor dividers and the R_T resistor, should be referenced to the AGND node. The AGND carries very little current and, therefore, can be a minimal size trace.

For dual-buck applications, connect the FB resistor dividers, the R_T resistor ground, and the AV_{IN} capacitor ground to the AGND pin close to the part. Connect AGND, using a via, to a low resistance ground plane that minimizes any voltage drops between AGND and the negative terminals of the buck output capacitors.

Enable Threshold Programming

The LTM4723 has precision threshold enable pins for each buck regulator to enable or disable each buck. When both are forced low, the device enters a low-current shutdown mode.

The rising threshold of both EN comparators is 400mV, with 50mV of hysteresis. The EN pins can be connected to AV_{IN} if the shutdown feature is not used. Adding a resistor divider from V_{IN} to an EN pin programs the LTM4723 to regulate that output only when V_{IN} is above a desired voltage. Typically, this threshold, $V_{IN(EN)}$, when the input supply is current limited or has a relatively high source resistance. A switching regulator draws near constant power from its input source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where problems may occur. See *Figure 20*, this threshold can be adjusted by setting the values R1 and R2 such that they satisfy Equation *5*.

$$RV_{IN(EN)} = \left(\frac{R1}{R2} + 1\right) \times 400mV \qquad (5)$$

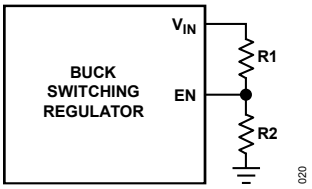


Figure 20. EN Divider

The buck regulator remains off until V_{IN} is above $V_{IN(EN)}$. The buck regulator remains enabled until V_{IN} falls to $0.875 \times V_{IN(EN)}$ and EN is 350mV.

Alternatively, a resistor divider from the output of one buck to the EN pin of the second buck provides event-based power-up sequencing, as the first buck reaching regulation enables the second buck. Replace $V_{IN(EN)}$ in Equation *5* with the desired output voltage of the first buck, (for example: 90% of the regulated value), at which the second buck is enabled.

Output Voltage Tracking and Soft Start

Each buck regulator has an independent TRACK/SS pin. An internal 4µA current pulls up each TRACK/SS pin when that buck is enabled, allowing an external capacitor from TRACK/SS to AGND to set the soft-start time, calculated using Equation *6*.

$$t_{SS} = C_{SS} \times \frac{500mV}{4\mu A} \qquad (6)$$

From 0V to 0.5V, the TRACK/SS voltage overrides the internal 0.5V reference input to the error amplifier, thus regulating the FB pin voltage to that of the TRACK/SS pin. When TRACK/SS is above 0.5V, tracking is disabled, and the feedback voltage regulates to the internal reference voltage.

Alternatively, connect the TRACK/SS pin to AV_{IN} to select an internally set 1ms default soft-start time for that buck regulator.

An active pull-down circuit is connected to either the TRACK/SS pin, or to the internal soft start node if TRACK/SS is connected high. This is used to discharge it in the case of fault conditions. The soft start ramp restarts when the fault is cleared. Fault conditions that clear the soft start voltage ramp are the EN pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Figure 21 and *Figure 22* show examples of some of the ways to control power-up sequencing using the EN, TRACK/SS, and PGOOD pins.

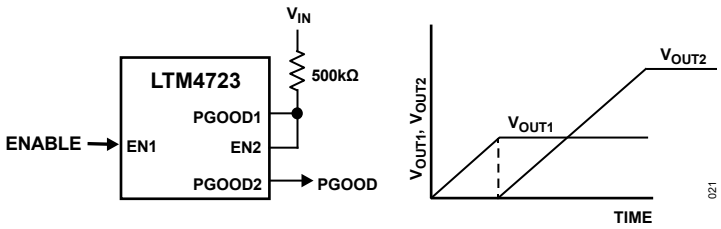


Figure 21. Sequential Voltage at Powerup

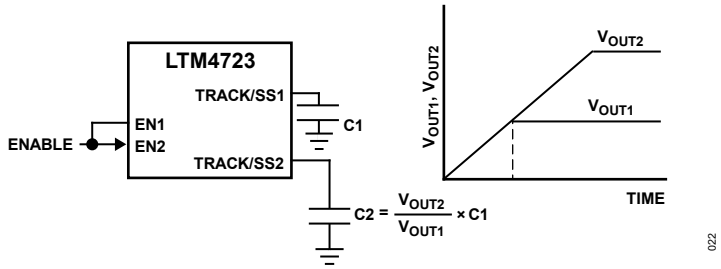


Figure 22. Tracking Voltage at Powerup

Temperature Monitor

After the soft-start cycle has completed and the output power good flag is high, the TRACK/SS pin voltages are set to a P_{TAT} (proportional to absolute temperature) voltage. Use the following procedure to accurately measure the die junction temperature.

1. Measure the ambient temperature (T_A), and one of the TRACK/SS pin voltages ($V_{TRACK/SS}$), when both buck regulators are unloaded. Use Equation 7 to calculate an accurate slope for the temperature sensing circuit.

$$Slope\ \left(\frac{V}{^\circ K}\right) = \frac{V_{TRACK/SS}}{T_A + 273} \qquad (7)$$

2. The calibrated slope can then be used to accurately determine the die temperature for any load or ambient conditions using Equation 8.

$$T_{JDIE}\ (^\circ C) = \frac{V_{TRACK/SS}}{Slope} - 273 \qquad (8)$$

3. When an output voltage goes out of regulation or is disabled, and the PGOOD pin is pulled low, the corresponding TRACK/SS pin no longer reports the temperature (see Figure 23).

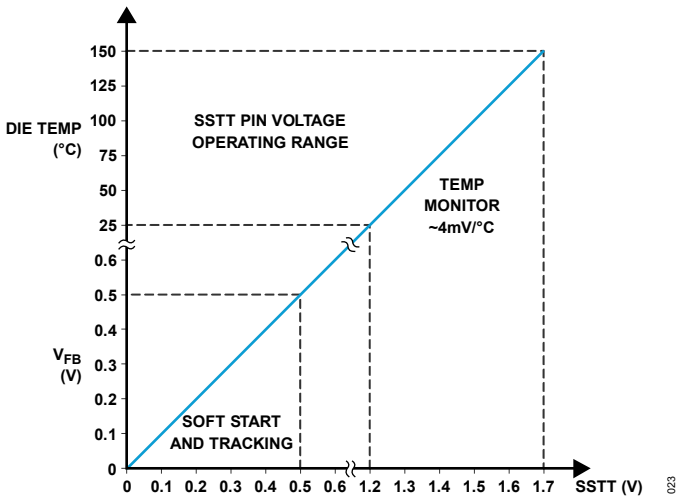


Figure 23. Soft- Start and Temperature Monitor Operation

Thermal Considerations and Output Current Derating

The thermal resistance reported in the *Pin Configurations and Function Descriptions* section is consistent with those parameters defined by JESD51-9. They are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients is found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Designers typically use laboratory equipment and a test vehicle, such as the evaluation (demo) board, to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to complement any FEA activities. Without FEA software, the thermal resistances reported in the *Pin Configurations and Function Descriptions* section are in-and-of themselves not relevant to providing guidance on thermal performance. Instead, see the *Derating Curves* in this data sheet that provides insight and guidance for the user's application and is adapted to correlate thermal performance to the user's application.

The *Pin Configurations and Function Descriptions* section typically gives four thermal coefficients explicitly defined in JESD51-12. These coefficients are quoted or paraphrased as follows.

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one-cubic-foot sealed enclosure. This environment is sometimes referred to as "still air," although natural convection causes the air to move. This value is determined by the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. θ_{JCbot}, the thermal resistance from junction to bottom of the product case, is determined with all the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions do not generally match the user's application.
3. θ_{JCtop}, the thermal resistance from the junction to the top of the product case, is determined with nearly all the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are at the bottom of the package, it is rare for an application to operate in such a manner, in which most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot},

this value may be useful for comparing packages, but the test conditions do not generally match the user's application.

Figure 24 shows a graphical representation of these thermal resistances; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

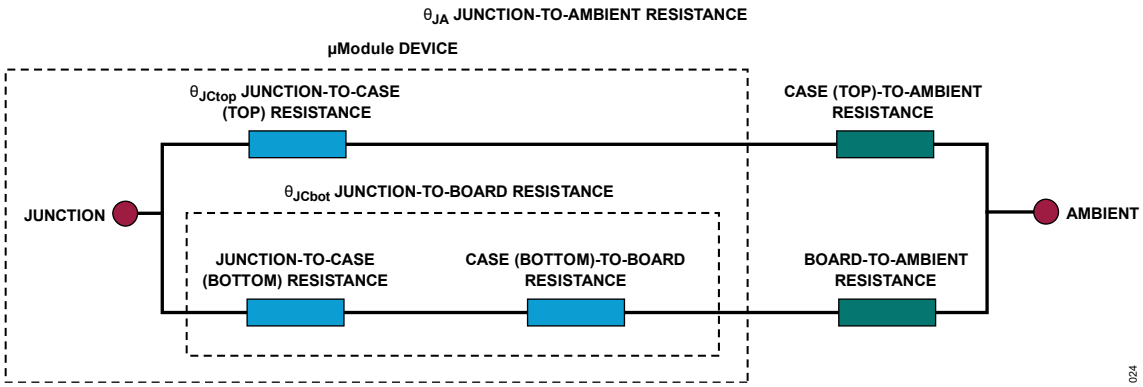


Figure 24. Graphical Representation of Thermal Coefficients, Including JESD51-12 Terms

In practice, no individual thermal resistance parameter, or combination of the four parameters defined by JESD51-12 and provided in the *Pin Configurations and Function Descriptions* section, represents the normal operating conditions of a µModule device. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) conduct thermally exclusively through the top or exclusively through the bottom of the µModule—as the standard defines for θ_{JCtop} and θ_{JCbot}, respectively. In practice, power loss dissipates thermally in both directions away from the package—though, without a heat sink and airflow, most heat flows into the board.

Within a SIP (system-in-package) module, note that multiple power devices and components dissipate power, so thermal resistance relative to different component or die junctions is not exactly linear with total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. This process and due diligence yield a set of derating curves.

The $2.5V_{IN}$, $3.3V_{IN}$, and $5V_{IN}$ power loss curves in *Figure 25* to *Figure 27* can be used in coordination with the load current derating curves in *Figure 28* to *Figure 33* for calculating an approximate θ_{JA} thermal resistance for the LTM4723 with various heat sinking and airflow conditions. The power-loss curves are taken at room temperature and are increased with multiplicative factors according to the junction temperature. This approximate factor is ~1.2, assuming the junction temperature reaches 120°C. The maximum load current is achievable as ambient temperature increases as long as the junction temperature stays below 120°C, a 5°C guard band below the maximum junction temperature of 125°C. When the ambient temperature reaches the point where the junction temperature is 120°C, then the load current is reduced to maintain the junction at 120°C while increasing the ambient temperature up to 120°C. The

derating curves are plotted with the output current starting at 10A and the ambient temperature at 30°C. The output voltages are 1.0V, 1.5V, and 2.5V. These values span the lower and upper output-voltage range to correlate with thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber, along with thermal modeling analysis. The junction temperatures are monitored as the ambient temperature increases, with and without airflow. The power loss increases when the ambient temperature change is factored into the derating curves. The junctions are maintained at a maximum of 120°C by lowering output current or power as ambient temperature increases. Lower output current reduces internal module loss as ambient temperature increases. The monitored junction temperature of 120°C minus the ambient operating temperature specifies the maximum allowed module temperature rise. For example, for a dual-phase single-output application, to determine the maximum ambient temperature allowable when V_{IN} = 3.3V, V_{OUT} = 1V and 10A load current without a heat sink and airflow, see *Figure 26* for the power loss, which is equal to 1.75W in this case, then multiply by the 1.2 coefficient for a 120°C junction temperature, which is 2.1W. If the 76.4°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 43.6°C divided by 2.1W equals a 20.8°C/W for θ_{JA} the system equivalent thermal resistance. *Table 9* specifies a 22°C/W value, which is very close. *Table 10* and *Table 11* provide equivalent thermal resistance for 1.5V and 2.5V outputs with and without airflow. The *Pin Configurations and Function Descriptions* section shows the simulation data for the worst-case scenario. *Table 9* to *Table 11* provide equivalent thermal resistances for 1.0V, 1.5V, and 2.5V outputs with and without airflow. The thermal resistances derived from *Table 9* to *Table 11* for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the *Typical Performance Characteristics* section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick, four-layer board with two ounces of copper on the two outer layers and one ounce of copper on the two inner layers. The PCB dimensions are 76mm × 76mm.

Derating Curves

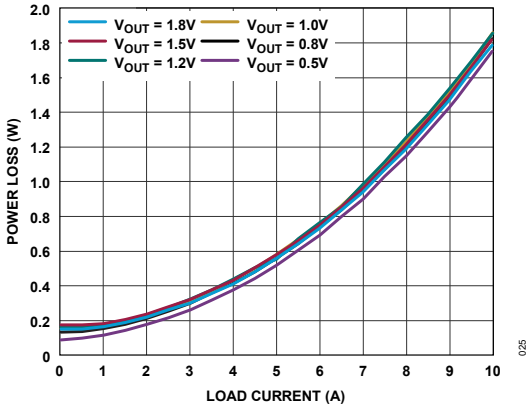


Figure 25. Power Loss vs. Load Current at 2.5V_{IN}, Dual-Phase, Single Output

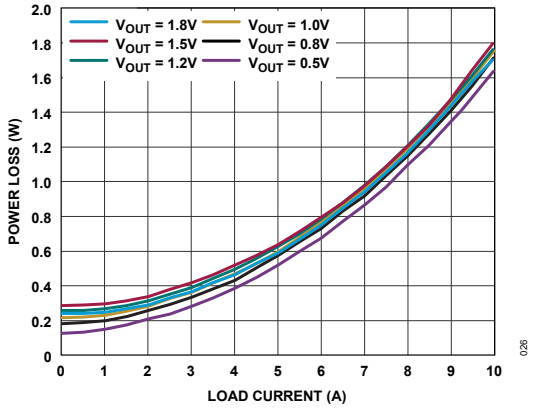


Figure 26. Power Loss vs. Load Current at 3.3V_{IN}, Dual-Phase, Single Output

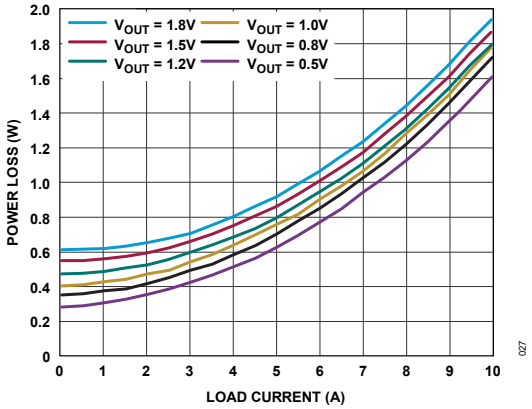


Figure 27. Power Loss vs. Load Current at 5V_{IN}, Dual-Phase, Single Output

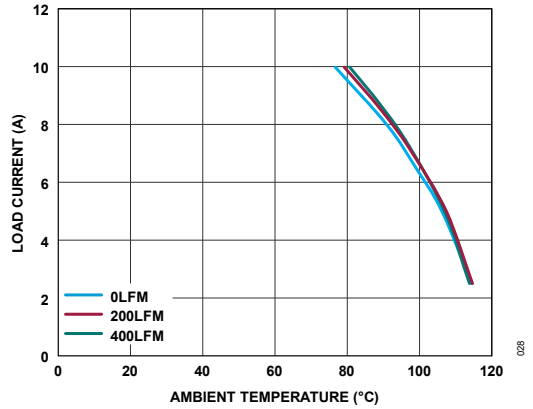


Figure 28. 3.3V to 1V Derating Curve, No Heat Sink

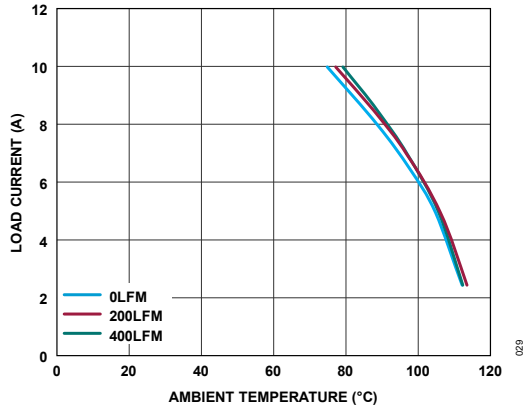


Figure 29. 3.3V to 1.5V Derating Curve, No Heat Sink

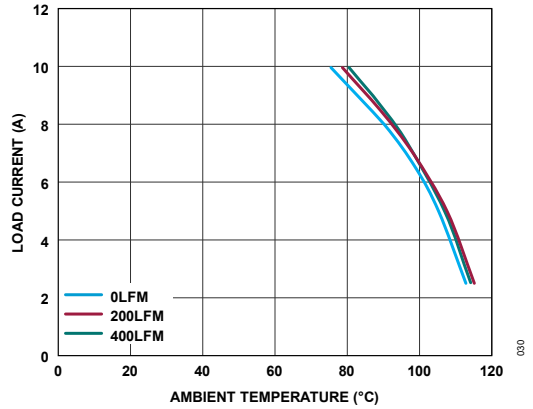


Figure 30. 3.3V to 2.5V Derating Curve, No Heat Sink

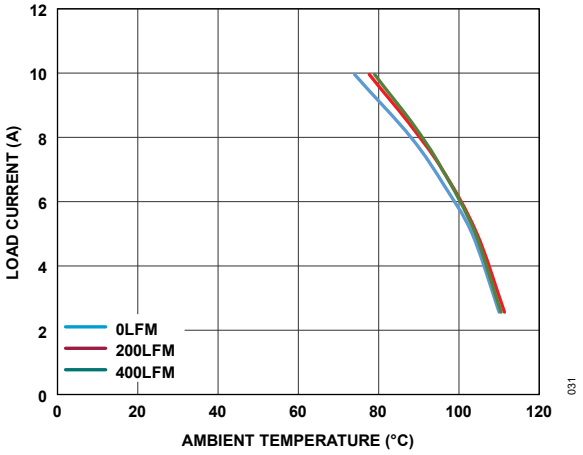


Figure 31. 5V to 1V Derating Curve, No Heat Sink

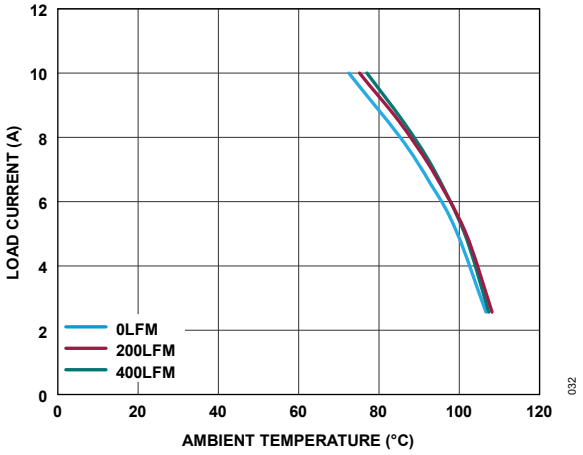


Figure 32. 5V to 1.5V Derating Curve, No Heat Sink

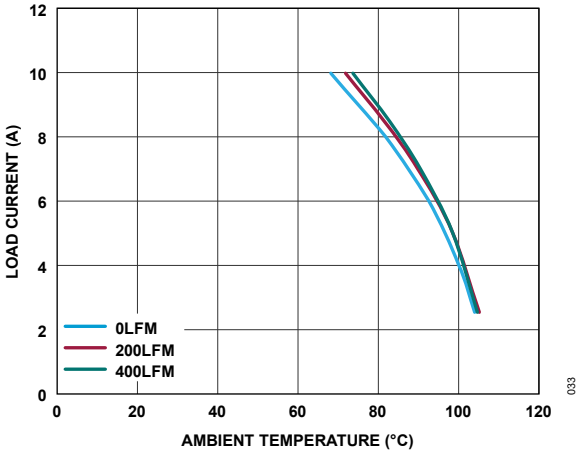


Figure 33. 5V to 2.5V Derating Curve, No Heat Sink

Table 9. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 28, Figure 31	3.3, 5	*Figure 26, Figure 27*	0	None	21
Figure 28, Figure 31	3.3, 5	*Figure 26, Figure 27*	200	None	20
Figure 28, Figure 31	3.3, 5	*Figure 26, Figure 27*	400	None	19

Table 10. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 29, Figure 32	3.3, 5	*Figure 26, Figure 27*	0	None	21
Figure 29, Figure 32	3.3, 5	*Figure 26, Figure 27*	200	None	29
Figure 29, Figure 32	3.3, 5	*Figure 26, Figure 27*	400	None	19

Table 11. 2.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 30, Figure 33	3.3, 5	*Figure 26, Figure 27*	0	None	23
Figure 30, Figure 33	3.3, 5	*Figure 26, Figure 27*	200	None	20
Figure 30, Figure 33	3.3, 5	*Figure 26, Figure 27*	400	None	19

Table 12. Output Voltage Response vs. Component Matrix (See the *Typical Applications* Section Figures)
0A to 5A Load Step Typical Measured Values

C_{IN} CERAMIC VENDORS	VALUE (µF)	PART NUMBER	C_{OUT} VENDORS	VALUE (µF)	PART NUMBER
Taiyo Yuden	10	EMK212BB7106MG-T	Murata	22	GRM188R60J226MEA0D
Murata	22	GRM188R61A226ME15D	Murata	100	GRM21BR60J107ME15K

V_{OUT} (V)	C_{IN} CERAMIC (µF)	C_{IN} (BULK)	C_{OUT} CERAMIC (µF)	C_{FF} (pF)	V_{IN} (V)	DROOP (mV)	P-P DEVIATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A/µs)	LOAD STEP SLEW RATE (A/µs)	FREQ.
0.5	2 × 10	150	100 + 2 × 22	Open	3.3	40	78	5	5	5	1kHz
0.8	2 × 10	150	100 + 2 × 22	Open	3.3	45	92	10	5	5	2MHz
0.8	2 × 10	150	100 + 2 × 22	Open	5	45	90	10	5	5	2MHz
1	2 × 10	150	100 + 2 × 22	Open	3.3	55	109	10	5	5	2MHz
1	2 × 10	150	100 + 2 × 22	Open	5	55	105	10	5	5	2MHz
1.5	2 × 10	150	100 + 2 × 22	Open	3.3	80	157	10	5	5	2MHz
1.5	2 × 10	150	100 + 2 × 22	Open	5	80	156	10	5	5	2MHz
2.5	2 × 10	150	100 + 2 × 22	Open	3.3	120	239	15	5	5	2MHz
2.5	2 × 10	150	100 + 2 × 22	Open	5	120	241	15	5	5	2MHz
3.3	2 × 10	150	100 + 2 × 22	Open	5	120	291	15	5	5	2MHz

PCB Layout Considerations

The LTM4723 is a high-performance module regulator designed for high efficiency and fast transient response. For optimal results, carefully consider the layout of the PCB board and follow the recommendations below to ensure proper operation. See *Figure 34* for a recommended PCB layout.

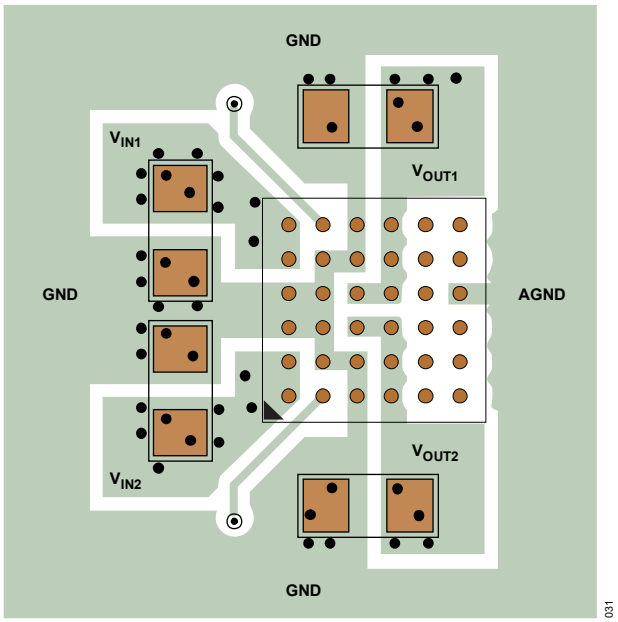
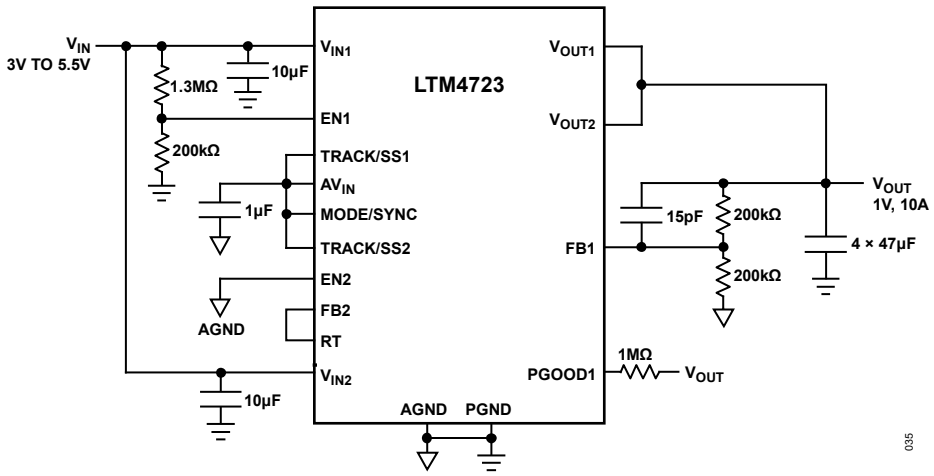


Figure 34. Recommended PCB Layout

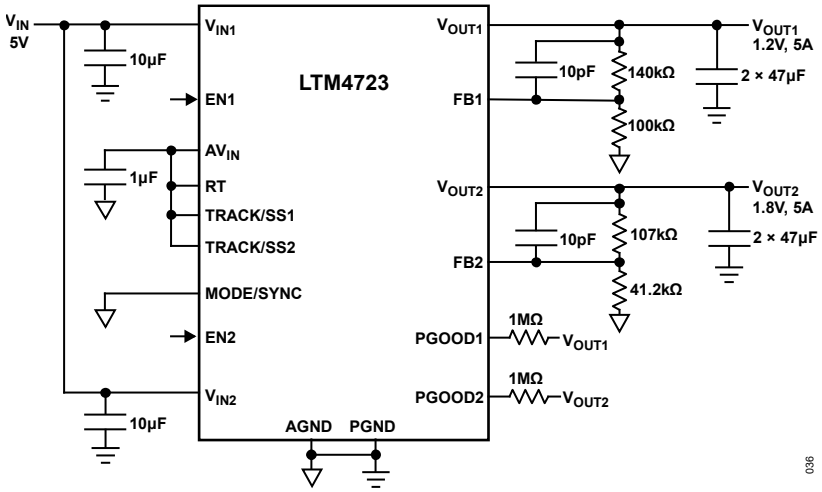
1. The V_{IN1} and V_{IN2} input supply pins should have local decoupling capacitors with the ground side of the capacitors connected on the top layer to the ground plane. These capacitors provide the AC to the internal power MOSFETs and their drivers. Large, switched currents flow through these capacitors, and it is important to minimize inductance from these capacitors by choosing a small case size, such as 0603, and placing them close to the pins on the top side of the board.
2. Connect the ground side of any FB, RT, and TRACK/SS components to AGND. Connect a 4.7µF decoupling capacitor from AV_{IN} to AGND, close to the pins. For all layouts, only connect AGND to the rest of the PCB ground plane in one location, to prevent transient currents in the ground plane from also flowing through the AGND trace, which would cause voltage noise between AGND referenced circuits.
3. For dual-buck applications, connect the AGND pin to the ground plane with a single via, close to the AGND pin. Use an unbroken low-resistance ground plane to minimize any voltage drops between AGND and the negative terminals of the output capacitors.
4. For 2-phase, single output designs, optionally connect the AGND pin to the negative terminal of the output capacitor (C_{OUT}) at the load. This reduces any load regulation caused by voltage drops between the ground at the load and the LTM4723 voltage reference ground. The AGND node carries very little current and, therefore, can be a minimal size trace. The ground side of any FB, RT, and TRACK/SS components, and the AV_{IN} capacitor ground should connect to the AGND node.

Typical Applications



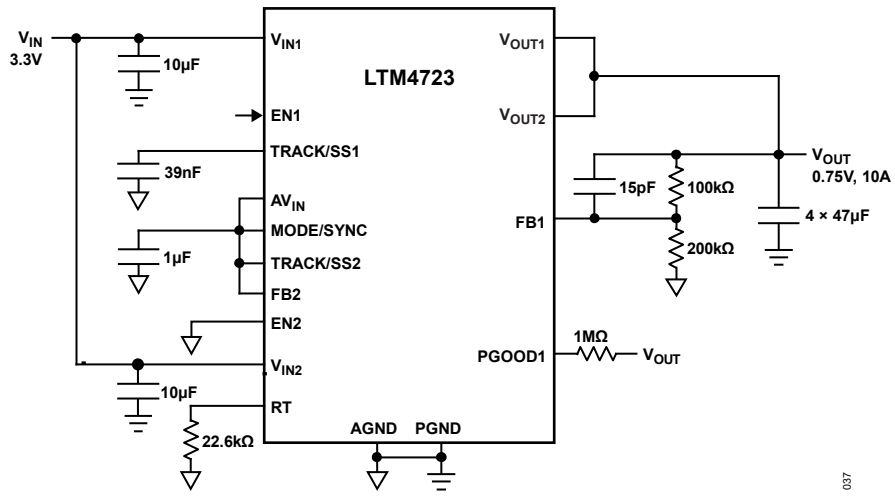
PINS NOT USED IN THIS CIRCUIT: PGOOD2, SW1, SW2

Figure 35. Single Output 2-Phase, 1.0V, 2MHz, 10A, UVLO = 3.0V, Burst Mode Operation



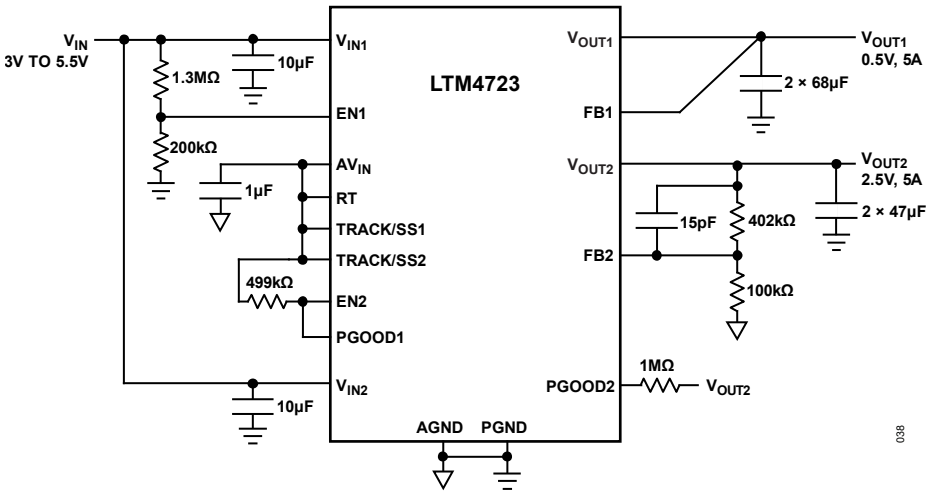
PINS NOT USED IN THIS CIRCUIT: SW1, SW2

Figure 36. Dual 1.2V and 1.8V, 2MHz, 5A, V_{IN} = 5V, Pulse-Skipping Mode



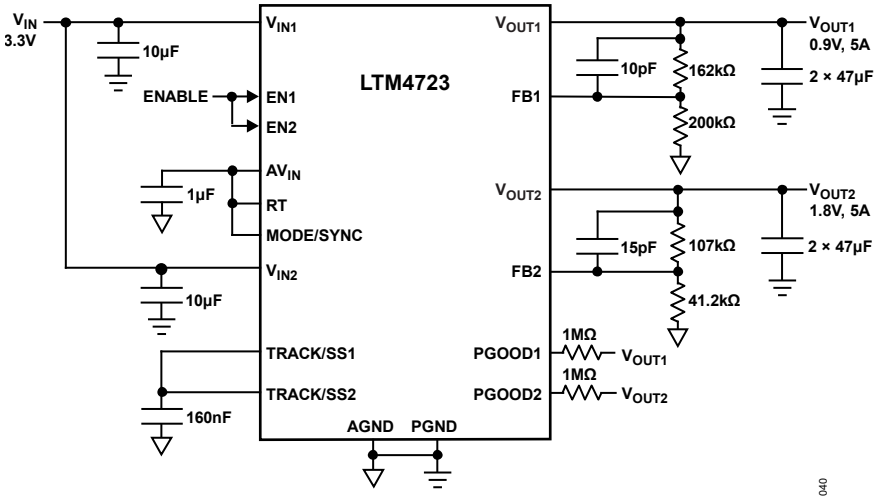
PINS NOT USED IN THIS CIRCUIT: PGOOD2, SW1, SW2

Figure 37. Single Output 2-Phase, 0.75V, 3MHz, 10A, V_{IN} = 3.3V, t_{SS} = 4.9ms, Burst Mode Operation



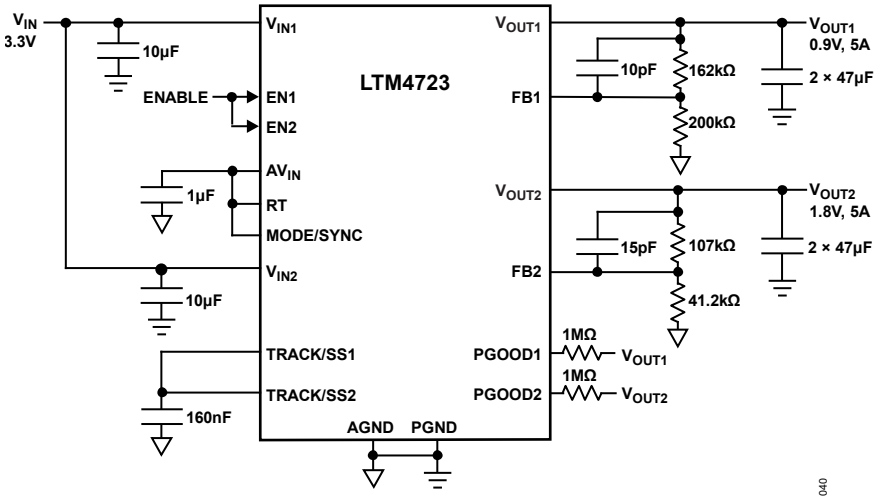
PINS NOT USED IN THIS CIRCUIT: MODE/SYNC, SW1, SW2

Figure 38. Dual 0.5V and 2.5V, 2MHz, 5A, UVLO = 3.0V, Sequential Powerup Sequencing (V_{OUT1} Powers First), Forced Continous Mode



PINS NOT USED IN THIS CIRCUIT: SW1, SW2

Figure 39. Dual 1.0V and 2.5V, 2MHz, 5A, V_{IN} = 3.3V, Voltage Tracking Powerup Sequencing (with t_{SS1} = 4.9ms, t_{SS2} = 12.5ms), Burst Mode Operation



PINS NOT USED IN THIS CIRCUIT: MODE/SYNC, SW1, SW2

Figure 40. Dual 0.9V and 1.8V, 2MHz, 5A, V_{IN} = 3.3V, Burst Mode Operation Ratio Metric Powerup with t_{SS} = 10ms

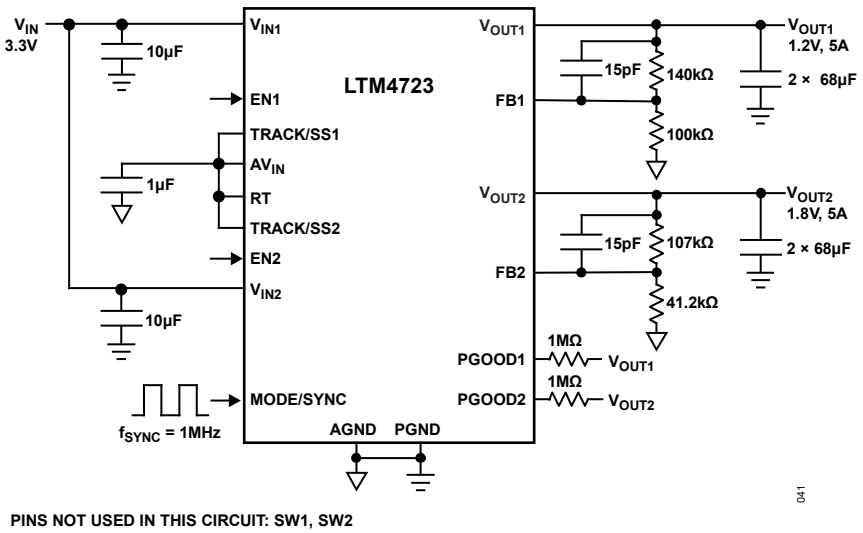


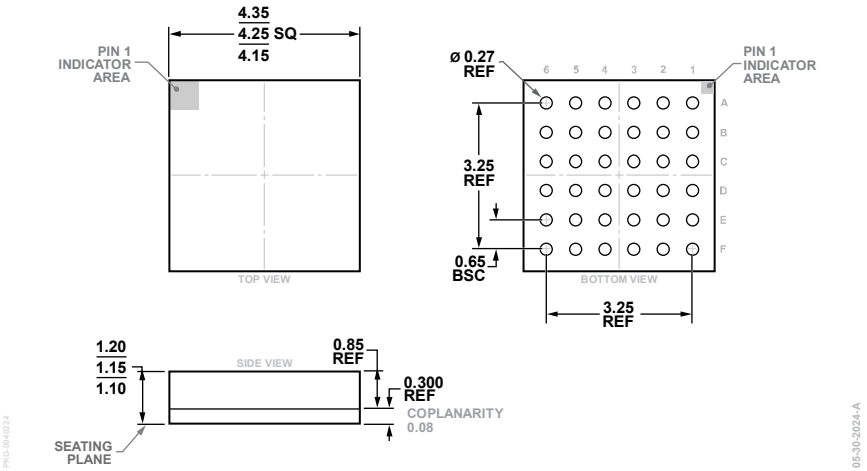
Figure 41. Dual 1.2V and 1.8V, 1MHz, 5A, V_{IN} = 3.3V, Syncing to 1MHz

Related Parts

Table 13. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LTM4658	Low V_{IN}, high efficiency 10A step-down DC-to-DC µModule regulator	2.25V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ V_{IN}, 4mm × 4mm × 4.32mm LGA, 4mm × 4mm × 4.62mm BGA
LTM4659	Ultrathin, low V_{IN} 10A step-down DC-to-DC µModule regulator	2.25V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ V_{IN}, 4mm × 4mm × 1.43mm LGA
LTM4691	Low V_{IN}, high efficiency, ultrathin, dual 2A step-down DC-to-DC µModule regulator	2.25V ≤ V_{IN} ≤ 3.6V, 0.5V ≤ V_{OUT} ≤ 2.5V, 3mm × 4mm × 1.18mm LGA 3mm × 4mm × 1.48mm BGA
LTM4710-1	Low V_{IN}, quad 8A Silent Switcher® µModule regulator	2.5V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ 3.6V, 6mm × 12mm × 3.54mm LGA with presolder package
LTM4693	Low V_{IN}, ultrathin, 2A buck-boost µModule regulator	2.6V ≤ V_{IN} ≤ 5.5V, 1.8V ≤ V_{OUT} ≤ 5.5V, 3.5mm × 4mm × 1.25mm LGA
LTM4611	Ultralow V_{IN}, 15A DC-to-DC power µModule regulator	1.5V ≤ V_{IN} ≤ 5.5V, 0.8V ≤ V_{OUT} ≤ 5V, 15mm × 15mm × 4.32mm LGA
LTM4670	Low V_{IN}, quad µModule regulator with configurable 10A output array	2.25V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ V_{IN}, 5mm × 15mm × 4.65mm BGA
LTM3360B	5V_{IN}, 33A high density step-down DC-to-DC µModule regulator with I^2C and integrated capacitors	2.9V ≤ V_{IN} ≤ 5.5V, 0.3V ≤ V_{OUT} ≤ 1V, 5mm × 6.55mm × 3.31mm BGA
LTM4663	Ultrathin 1.5A µModule thermoelectric cooler (TEC) regulator	2.7V ≤ V_{IN} ≤ 5.5V, 3.5mm × 4mm × 1.3mm LGA

OUTLINE DIMENSIONS



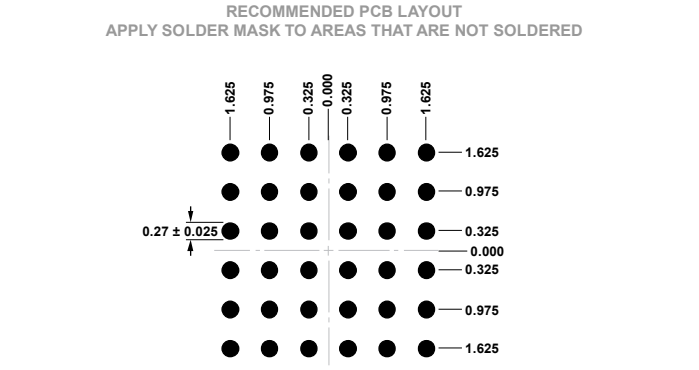


Figure 42. 36-Terminal, 4.25mm × 4.25mm × 1.15mm, LGA

ORDERING GUIDE

Table 14. LTM4723 Ordering Information

MODEL[4]	TEMPERATURE RANGE[1,2]	PACKAGE DESCRIPTION	PACKAGE OPTION[6]
LTM4723EV#PBF	0°C to 125°C	Part marking: 4723 Au (RoHS) pad finish[3] e4 finish code Moisture sensitivity level 4 (MSL 4) rated device[5]	*36-Terminal, 4.25mm × 4.25mm × 1.15mm,* LGA
LTM4723IV#PBF	–40°C to 125°C	Part marking: 4723 Au (RoHS) pad finish[3] e4 finish code Moisture sensitivity level 4 (MSL 4) rated device[5]	*36-Terminal, 4.25mm × 4.25mm × 1.15mm,* LGA

1 The LTM4723 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4723E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4723I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

2 Contact the factory for parts specified with wider operating temperature ranges.

3 Pad finish code is per IPC/JEDEC J-STD-609.

4 The device temperature grade is indicated by a label on the shipping container.

5 This product is not recommended for second-side reflow, and it is moisture sensitive. For more information, refer to the Analog Devices *µModule LGA and BGA Packaging Care and Assembly Instructions* document.

6 The LGA package should follow assembly and manufacturing procedures. For more information, refer to the Analog Devices *Assembly Considerations for the µModule BGA and LGA Packages* guidelines.

Table 15. Evaluation Board Ordering Information

MODEL	DESCRIPTION
EVAL-LTM4723-AZ	Evaluation board featuring the LTM4723, dual 5A or single 10A step-down DC-to-DC µModule regulator.

SELECTOR GUIDE

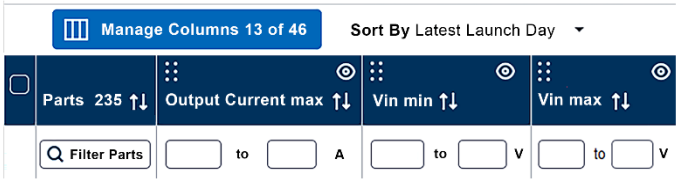
Package Photos



Figure 43. Part Marking Is Laser Mark, 36-Terminal, 4.25mm × 4.25mm × 1.15mm, LGA

Design Resources

Table 16. µModule Power Technology

RESOURCES	DESCRIPTION	
µModule Design, Manufacturing, and Assembly	**Design** ▶ Evaluation guide boards and Gerber files ▶ Free design tools, including LTspice® and LTpowerCAD® ▶ Circuit simulations	**Manufacturing** ▶ Quick start guides ▶ PCB design, assembly, and manufacturing guidelines ▶ Package and board level reliability
µModule Regulator Products Search	▶ Manage columns and sort table of products by parameters, and download the result as a spread sheet. 	
Digital Power System Management	The Analog Devices family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining, and sequencing, and feature EEPROM for storing user configurations and fault logging.	

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