FEATURES
- Quad Digitally Adjustable Analog Loops with Digital Interface for Control and Monitoring
- Wide Input Voltage Range: 4.5V to 14V
- Output Voltage Range: 0.3V to 0.7V
- ±0.5% DC Output Accuracy at 0.7V
- ±4.5% Current Readback Accuracy: 0°C to 125°C
- Optimized for Low Output Voltage Ranges
- 400kHz PMBus-Compliant I2C Serial Interface
- Supports Telemetry Polling Rates Up to 125Hz
- Integrated 16-Bit ΔΣ ADC
- Parallel and Current Share Multiple Modules
- 15mm × 22mm × 5.71mm BGA Package

Readable Data
- Input and Output Voltages, Currents, and Temperatures
- Running Peak Values, Uptime, Faults, and Warnings
- Onboard EEPROM Fault Log Record

Writable Data and Configurable Parameters
- Output Voltage, Voltage Sequencing, and Margining
- Digital Soft-Start/Soft-Stop Ramp, Program Analog Loop
- OV/UV/SHORT, UVLO, Frequency and Phasing

APPLICATIONS
- Multi-Rail Processor Power, Configurable Core Power

DESCRIPTION

The LTM®4683 is a quad 31.25A or single 125A step-down µModule® (power micromodule) DC/DC regulator featuring remote configurability and telemetry monitoring of power management parameters over PMBus. The LTM4683 is comprised of digitally programmable analog control loops, and is optimized for higher bandwidth and transient response.

The LTM4683’s 2-wire serial interface allows outputs to be margined, tuned, and ramped up and down at programmable slew rates with sequencing delay times. True input current sense, output currents and voltages, output power, temperatures, uptime and peak values are readable. Custom configuration of the EEPROM contents is not required. At start-up, output voltages, switching frequency, and channel phase angle assignments can be set by pin-strapping resistors. The LTpowerPlay® graphical user interface (GUI), DC1613A USB-to-PMBus converter, and evaluation kits are available.

The LTM4683 is offered in a 15mm × 22mm × 5.71mm BGA package available with a RoHS-compliant terminal finish.

All registered trademarks and trademarks are the property of their respective owners. Protected by U.S. Patents including 5408150, 5481178, 5705919, 5929620, 6144194, 6177787, 6580258, 7420359, 8163643. Licensed under U.S. Patent 7000125 and other related patents worldwide.
Table of Contents

Table 7. PMBus Commands Summary (NOTE: The Data Format Abbreviations are Detailed in Table 8). 49
Table 8. Data Format Abbreviations. 54
Applications Information. 55
V_in to V_out Step-Down Ratios. 55
Input Capacitors. 55
Output Capacitors. 55
Light Load Current Operation. 55
Switching Frequency and Phase. 56
Output Current Limit Programming. 57
Minimum On-Time Considerations. 58
Variable Delay Time, Soft-Start and Output Voltage Ramping. 58
Digital Servo Mode. 58
Soft Off (Sequenced Off). 59
Undervoltage Lockout. 60
Fault Detection and Handling. 60
Open-Drain Pins. 61
Phase-Locked Loop and Frequency Synchronization. 61
Input Current Sense Amplifier. 62
Programmable Loop Compensation. 62
Checking Transient Response. 62
PolyPhase Configuration. 64
Connecting The USB to I2C/SMBus/PMBus Controller to the LTM4683 In System. 64
LTpowerPlay: An Interactive GUI for Digital Power. 65
PMBus Communication and Command Processing. 65
Thermal Considerations and Output Current Derating. 67
Table 13. Single Channel Output Voltage vs. Capacitor Selection, 10A to 20A Load Step with 10A/μs Slew Rate. 72
Table 14. Single Channel Output Voltage vs. Capacitor Selection, All Ceramic Configuration, 10A to 20A Load Step with 10A/μs Slew Rate. 73
Table 15. Dual Connected Channels Output Voltage vs. Capacitor Selection, Bulk and Ceramic Cap Configuration, 10A to 30A Load Step with 20A/μs Slew Rate. 74
Table 16. Quad Connected Channels Output Voltage vs. Capacitor Selection, Bulk and Ceramic Cap Configuration, 10A to 40A Load Step with 15A/μs Slew Rate. 75
EMI Performance. 76
Safety Considerations. 76
Layout Checklist/Example. 76
Typical Applications. 78
PMBus Command Details. 83
Addressing and Write Protect. 83
General Configuration Commands. 85
On/Off/Margin. 86
PWM Configuration. 88
Voltage. 91
Input Voltage and Limits. 91
Output Voltage and Limits. 92
Output Current and Limits. 95
Input Current and Limits. 97
Temperature. 98
Power Stage DCR Temperature Calibration. 98
Power Stage Temperature Limits. 98
Timing. 99
Timing—On Sequence/Ramp. 99
Timing—Off Sequence/Ramp. 100
Precondition for Restart. 101
Fault Response. 101
Fault Responses All Faults. 101
Fault Responses Input Voltage. 102
Fault Responses Output Voltage. 102
Fault Responses Output Current. 105
Fault Responses IC Temperature. 106
Fault Responses External Temperature. 107
Fault Sharing. 108
Fault Sharing Propagation. 108
Fault Sharing Response. 110
Scratchpad. 110
Identification. 111
Fault Warning and Status. 112
Telemetry. 118
NVM Memory Commands. 122
Store/Restore. 122
Fault Logging. 123
Block Memory Write/Read. 127
Package Description. 128
Table 25. LTM4683 BGA Pinout. 128
Package Description. 129
Revision History. 131
Package Photos. 132
Design Resources. 132
Related Parts. 132

For more information www.analog.com
ABSOLUTE MAXIMUM RATINGS

(Note 1)
Terminal Voltages
$V_{IN_{nn}}$ (Note 4), $SV_{IN_{nn}}$, $I_{IN_{nn}}$, $I_{IN_{nn}}^+$, $I_{IN_{nn}}^–$, $V_{IN_{VBIAS}}$, RUNn .................... $0.3V$ to $16V$ 
$SV_{IN_{nn}}$ – $I_{IN_{nn}}^+$, $I_{IN_{nn}}^+$ – $I_{IN_{nn}}^–$ .................... $–0.3V$ to $0.3V$
$SWn$ .......................... $–1V$ to $16V$, $–5V$ to $16V$ 
Transient INTVCC–$n$, $V_{BIAS}$ .................................... $–0.3V$ to $6V$
$V_{OUTn}$ ........................................ $–0.3V$ to $1.0V$
$V_{OSNSn}^+$ .................................. $–0.3V$ to $1.0V$
$V_{OSNSn}^–$ .................................. $–0.3V$ to $0.3V$
RUNn, SDA–$nn$, SCL–$nn$, ALERT–$nn$ ................. $–0.3V$ to $5.5V$
FSWPH–$nn$–CFG, VOUT–$nn$–CFG, VTRIM–$nn$–CFG, ASEL–$nn$ .................... $–0.3V$ to $2.75V$
FAULTn, SYNC–$nn$, SHARE_CLK–$nn$, WP–$nn$, PGOODn .................................. $–0.3V$ to $3.6V$
COMPna, COMPnb .................................. $–0.3V$ to $2.7V$
$TSNSn$ .................................... $–0.3V$ to $0.8V$

n = 0, 1, 2, 3 and $nn = 01, 23$
$V_{DD_{33}}$–$nn$ and $V_{DD_{25}}$–$nn$ are outputs not to be driven.

Temperatures
Internal Operating Temperature Range
(Notes 2, 13, 15, 16) .................. $–40°C$ to $125°C$
Storage Temperature Range ........... $–55°C$ to $125°C$
Peak Solder Reflow Package Body Temperature ... $245°C$

ORDER INFORMATION

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PAD OR BALL FINISH</th>
<th>PART MARKING</th>
<th>PACKAGE TYPE</th>
<th>MSL RATING</th>
<th>TEMPERATURE RANGE (SEE NOTE 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTM4683YE#PBF</td>
<td>SAC305 (RoHS)</td>
<td>LTM4683Y e1</td>
<td>BGA</td>
<td>4</td>
<td>$–40°C$ to $125°C$</td>
</tr>
<tr>
<td>LTM46831Y#PBF</td>
<td>SAC305 (RoHS)</td>
<td>LTM4683Y e1</td>
<td>BGA</td>
<td>4</td>
<td>$–40°C$ to $125°C$</td>
</tr>
</tbody>
</table>

- Contact the factory for parts specified with wider operating temperature ranges. Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

For more information www.analog.com
## Electrical Characteristics

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). TA = 25°C, VIN, SVIN = 12V, RUN = 3.3V, \(R\text{UNP} = 12V\), FREQUENCY_SWITCH = 425kHz and \(V_{\text{OUT}}\) commanded to 0.5V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

### SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS
--- | --- | --- | --- | --- | --- | ---
\(V_{\text{INmin}}\) | Input DC Voltage | Test Circuit 1 | ● | 5.75 | 14 | V
 | | Test Circuit 2, VIN_OFF < VIN_ON = 4V | ● | 4.5 | 5.75 | V
\(V_{\text{OUTn}}\) | Range of Output Voltage Regulation for Each Channel | \(V_{\text{OUTn}}\) Differentially Sensed on \(V_{\text{OSNS}}\); Pin-Pair, Controlled by Serial Bus or with Resistors Present at Start-Up on \(V_{\text{OUTn}}\)_CFG | ● | 0.3 | 0.7 | V
\(V_{\text{OUTn(OC)}}\) | Output Voltage, Total Variation with Line and Load for Each Channel | Digital Servo Engaged (MFR_PWM_MODE[6]=1b) | ● | 0.4965 | 0.50 | 0.5035 | V
 | | Digital Servo Disengaged (MFR_PWM_MODE[6]=0b) | | | 0.492 | 0.50 | 0.508 | V
\(V_{\text{UVLO}}\) | Undervoltage Lockout Threshold, When VIN < 4.3V | \(V_{\text{INTVCC,n}}\) Falling | 3.55 | | | V
 | | \(V_{\text{INTVCC,n}}\) Rising | 3.90 | | | V

### Input Specifications

\(I_{\text{INRUSH(VINn)}}\) | Input Inrush Current at Start-Up | Test Circuit 1, 0.5V, VIN = 12V, No Load Besides Capacitors; TON_RISEn = 3ms | 200 | | | mA
\(I_{Q(SVINn)}\) | Input Supply Bias Current | Forced Continuous Mode, MFR_PWM_MODE[0]=1b, RUN = RUNC = 3.3V, Shutdown, RUNGn = RUNG = 0V | 40 | | | mA
 | | | | 23 | | | mA
\(I_{S(VINn,PSM)}\) | Input Supply Current in Pulse-Skipping Mode Operation | Pulse-Skipping Mode, MFR_PWM_MODE[0]=0b, \(I_{\text{OUTn}}\) = 100mA | 20 | | | mA
\(I_{S(VINn,FCM)}\) | Input Supply Current in Forced Continuous Mode Operation | Forced Continuous Mode, MFR_PWM_MODE[0]=1b, 12V to 0.5V, \(I_{\text{OUTn}}\) = 31.25A, RUNC = 0V, \(V_{\text{BIAS}}\) = Off | 1.8 | | | A
\(I_{S(VINn,SHUTDOWN)}\) | Input Supply Current in Shutdown | Shutdown, RUNC = 0V, RUNC = 0V, \(V_{\text{BIAS}}\) = Off | 300 | | | μA

### Output Specifications

\(I_{\text{OUTn}}\) | Output Continuous Current Range Each Channel | (Note 6) Utilizing MFR_PWM_MODE[7]=1 and Using \(I_{\text{OUTn}}=40A\) for IOUT_OC_FAULT_LIMIT, Page 96 | 0 | 31.25 | | A
\(\Delta V_{\text{OUTn(LINE)}}/\text{V}_{\text{OUTn}}\) | Line Regulation Accuracy, Each,Channel | Digital Servo Engaged (MFR_PWM_MODE[6]=1b) | ● | 0.03 | | %/V
 | | Digital Servo Disengaged (MFR_PWM_MODE[6]=0b) | | | 0.03 | ±0.2 | %/V
\(\Delta V_{\text{OUTn(LOAD)}}/\text{V}_{\text{OUTn}}\) | Load Regulation Accuracy, Each,Channel | Digital Servo Engaged (MFR_PWM_MODE[6]=1b) | ● | 0.03 | | %
 | | Digital Servo Disengaged (MFR_PWM_MODE[6]=0b) | | | 0.2 | 0.5 | %

\(V_{\text{OUTn(AC)}}\) | Output Voltage Ripple | | 10 | | | mVpp
\(I_{S} (\text{Each Channel})\) | \(V_{\text{OUTn}}\), Ripple Frequency | FREQUENCY_SWITCH Set to 350kHz (0xfABC) | ● | 325 | 350 | 375 | kHz
\(\Delta V_{\text{OUTn(START)}}\) | Turn-On Overshoot | TON_RISEn = 3ms (Note 12) | ● | 8 | | mV
\(I_{\text{START}}\) | Turn-On Start-Up Time | Time from VIN Toggling from 0V to 12V to Rising Edge PGOODn, TON DELAYn = 0ms, TON_RISEn = 3ms | ● | 35 | | ms
\(I_{\text{DELAY(0ms)}}\) | Turn-On Delay Time | Time from First Rising Edge of RUNn to Rising Edge of PGOODn, TON DELAYn = 0ms, TON_RISEn = 3ms, VIN Having Been Established for at Least 70ms | 2.75 | 3.3 | 3.8 | ms
\(\Delta V_{\text{OUTn(LS)}}\) | Peak Output Voltage Deviation for Dynamic Load Step | Load: 10A to 30A and 30A to 10A at 10A/μs, \(V_{\text{OUTn}} = 0.50V, V_{\text{IN}} = 12V\) (Note 12) | ● | 30 | | mV
\(I_{\text{SETTLE}}\) | Settling Time for Dynamic Load Step per Channel | Load: 10A to 30A and 30A to 10A at 10A/μs, \(V_{\text{OUTn}} = 0.50V, V_{\text{IN}} = 12V\), (Note 12) | 18 | | | μs
## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). $T_A = 25^\circ\text{C}$, $V_{\text{IN}}$, $SV_{\text{IN}} = 12\,\text{V}$, $\text{RUNP} = 12\,\text{V}$, FREQUENCY SWITCH = 425kHz and $V_{\text{OUT}}$ commanded to 0.5V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

### SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS
--- | --- | --- | --- | --- | --- | ---
I_{\text{OUT}}(\text{OCL_PK}) | Output Current Limit, Peak High Range per Channel | Cycle-by-Cycle Inductor Peak Current Limit Inception, Utilizing MFR_PWM_MODE[7] = 1, Using $I_{\text{OUT}} = 41.75\,\text{A}$ for IOUT_OC_FAULT_LIMIT, Page 96 | 45 |  |  | A
I_{\text{OUT}}(\text{OCL_AVG}) | Output Current Limit, Time Averaged per Channel | Time-Averaged Output Inductor Current Limit Inception, Commanded by IOUT_OC_FAULT_LIMIT, (Note 12), Utilizing MFR_PWM_MODE[7] = 1, Using $–I_{\text{OUT}} = 41.75\,\text{A}$, Page 96 | 40A |  |  | (See IOUT_RB-ACC Specification (Output Current Readback Accuracy)

### Control Section

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS
--- | --- | --- | --- | --- | --- | ---
$V_{\text{FBCM}}$ | Channel 0 to Channel 3 Feedback Input Common Mode Range | $V_{\text{DSNS}}$ Valid Input Range (Referred to SGND) $V_{\text{DSNS}}$ Valid Input Range (Referred to SGND) | –0.1 | 0.3 |  | V
| $V_{\text{OUT-RNGL}}$ | Full-Scale Command Voltage, Range Low (0.3V to 2.75V) per Channel; Limit to 1V (Note 14) | $V_{\text{OUT}}$, Commanded to 2.750V, MFR_PWM_MODE[1] = 1b Set Point Accuracy Resolution LSB Step Size | –2.7 | 2.8 |  | V
| $R_{\text{VSNS}}^+$ | Impedance to SGND | $0.3\,\text{V} \leq V_{\text{OSNS}}^+ \leq V_{\text{SGND}} \leq 1.0\,\text{V}$ | 50 |  |  | kΩ
| $I_{\text{IGN(MIN)}}$ | Minimum On-Time (Note 8 ) per Channel | 85 |  |  | ns
| $R_{\text{COMP}}$ | Resolution Compensation Resistor $R_{\text{TH(MAX)}}$ Compensation Resistor $R_{\text{TH(MIN)}}$ | MFR_PWM_COMP[4:0] = 0 to 31 (See Figure 1, Note Section) | 5 | 62 |  | Bits
| $R_{\text{MIN}}$ | Resolution Error Amplifier $R_{\text{MIN}}$ (MAX) Error Amplifier $R_{\text{MIN}}$ (MIN) LSB Step Size | $V_{\text{COMP}} = 1.35\,\text{V}$, MFR_PWM_COMP[7:5] = 0 to 7 | 3 | 5.76 | 0.68 | Bits

### Analog OV/UV (Overvoltage/Undervoltage) Output Voltage Supervisor Comparators (VOUT_OV/UV_FAULT_LIMIT and VOUT_OV/UV_WARN_LIMIT Monitors)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS
--- | --- | --- | --- | --- | --- | ---
$N_{\text{OV/UV_COMP}}$ | Resolution, Output Voltage Supervisors (Notes 13, 14) | 9 |  |  | Bits
| $V_{\text{OV-RNG}}$ | Output OV Comparator Threshold Detection Range | High Range Scale Not Used, Low Range Scale, MFR_PWM_MODE[1] = 1b (Note 14) | 0.3 | 2.7 |  | V
| $V_{\text{DUSTP}}$ | Output OV and UV Comparator Threshold Programming LSB Step Size (Note 14), Low Range Scale, MFR_PWM_MODE[1] = 1b | 5.6 |  |  | mV
| $V_{\text{OV-ACC-n}}$ | Output OV Comparator Threshold Accuracy Channel 0 to Channel 3 (Note 13) | $0.3\,\text{V} \leq V_{\text{OSNS}}^+ – V_{\text{OSNS}}^- \leq 0.7\,\text{V}$, MFR_PWM_MODE[1] = 1b |  | ±5 |  | %
| $V_{\text{UV-RNGn}}$ | Output UV Comparator Threshold Detection Range | Low Range Scale, MFR_PWM_MODE[1] = 1b, High Range Scale N/A, Output Limited to 0.7V | 0.3 | 2.7 |  | V
| $V_{\text{UV-ACC-n}}$ | Output UV Comparator Threshold Accuracy Channel 0 to Channel 3 (Note 13) | $0.3\,\text{V} \leq V_{\text{OSNS}}^+ – V_{\text{OSNS}}^- \leq 0.7\,\text{V}$, MFR_PWM_MODE[1] = 1b |  | ±5 |  | %
| $I_{\text{PROP-OV}}$ | Output OV Comparator Response Times | Overdrive to 10% Above Programmed Threshold | 100 |  |  | µs
| $I_{\text{PROP-UV}}$ | Output UV Comparator Response Times | Under Drive to 10% Below Programmed Threshold | 100 |  |  | µs
### ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). $T_a = 25^\circ C$, $V_{IN}$, SVIN = 12V, RUN = 3.3V, RUNP = 12V, FREQUENCY_SWITCH = 425kHz and $V_{OUT}$ commanded to 0.5V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog OV/UV SVIN, Input Voltage Supervisor Comparators (Threshold Detectors for VIN_ON and VIN_OFF)</td>
<td>$N_{SVIN-OV-UV-COMP}$ SVIN_OV/UV Comparator Threshold-Programming Resolution</td>
<td>(Note 14)</td>
<td>9</td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td></td>
<td>$SVIN_{OU-RANGE}$ SVIN_OV/UV Comparator Threshold-Programming Range</td>
<td>Limited to Abs Max = 16V</td>
<td>4.5</td>
<td>16</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$SVIN_{OU-STEP}$ SVIN_OV/UV Comparator Threshold-Programming LSB Step Size</td>
<td>(Note 14)</td>
<td>76</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>$SVIN_{OU-ACC}$ SVIN_OV/UV Comparator Threshold Accuracy</td>
<td>$9V &lt; SVIN \leq 16V$</td>
<td>●</td>
<td>±3</td>
<td>±270</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>$I_{PROP-SVIN-HIGH-VIN}$ SVIN_OV/UV Comparator Response Time, High VIN Operating Configuration</td>
<td>Test Circuit 1, and: VIN_ON = 9V; SVIN Driven from 8.775V to 9.225V VIN_OFF = 9V; SVIN Driven from 9.225V to 8.775V</td>
<td>●</td>
<td>100</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>$I_{PROP-SVIN-LOW-VIN}$ SVIN_OV/UV Comparator Response Time, Low VIN Operating Configuration</td>
<td>Test Circuit 2, and: VIN_ON = 4.5V; SVIN Driven from 4.225V to 4.725V VIN_OFF = 4.5V; SVIN Driven from 4.725V to 4.225V</td>
<td>●</td>
<td>100</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Channel n Output Voltage Readback (READ_VOUT/n)</td>
<td>$N_{O-RB}$ Output Voltage Readback Resolution and LSB Step Size</td>
<td>(Note 14)</td>
<td>16</td>
<td>244</td>
<td></td>
<td>µV</td>
</tr>
<tr>
<td></td>
<td>$V_{O-F/S}$ Output Voltage Full-Scale Digitizable, Range</td>
<td>$V_{RUNP} = 0V$, (Note 14), Limited to 1.0V Max Operating</td>
<td>8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{O-RB-ACC}$ Output Voltage Readback Accuracy</td>
<td>Channel n: $0.3V &lt; V_{VOSNS}^+ - V_{VOSNS}^- &lt; 0.7V$</td>
<td></td>
<td></td>
<td></td>
<td>±3.5mV</td>
</tr>
<tr>
<td></td>
<td>$I_{CONVERT-VO-RB}$ Output Voltage Readback Update, Rate</td>
<td>$MFR_{ADC_CONTROL} = 0x00$, (Notes 9, 14) $MFR_{ADC_CONTROL} = 0x01$ through $0x0C$, (Notes 9, 14), $MFR_{ADC_CONTROL}$ Section</td>
<td>90</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Input Voltage SVIN, Readback (READ_VIN)</td>
<td>$N_{SVIN-RB}$ Input Voltage Readback Resolution and LSB Step Size</td>
<td>(Notes 10, 14), Limited to Abs Max = 16V</td>
<td>10</td>
<td>15.625</td>
<td></td>
<td>Bits mV</td>
</tr>
<tr>
<td></td>
<td>$SVIN_{F/S}$ Input Voltage Full-Scale Digitizable, Range</td>
<td>(Notes 11, 14), Limited to 14V Operating</td>
<td>43</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$SVIN_{RB-ACC}$ Input Voltage Readback Accuracy</td>
<td>$4.5V \leq SVIN \leq 14V$</td>
<td>●</td>
<td></td>
<td>±2%</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>$I_{CONVERT-SVIN-RB}$ Input Voltage Readback Update Rate</td>
<td>$MFR_{ADC_CONTROL} = 0x00$, (Notes 9, 14) $MFR_{ADC_CONTROL} = 0x01$, (Notes 9, 14)</td>
<td>90</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Channel n Output Current (READ_IOUT/n), Duty Cycle (READ_DUTY_CYCLE/n) and Computed Input Current (MFR_READ_IN/n) Readback</td>
<td>$N_{O-RB}$ Output Current Readback Resolution and LSB Step Size</td>
<td>(Notes 10, 14)</td>
<td>10</td>
<td></td>
<td></td>
<td>Bits mA</td>
</tr>
<tr>
<td></td>
<td>$I_{O-RB}$ Output Current Full-Scale Digitizable, Range</td>
<td>(Note 14), Utilizing $MFR_{PWM_MODE[7]} = 1$, Using $I_{OUT_OC_FAULT_LIMIT} = 61A$, Page 96</td>
<td>54</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>$I_{OUT-ACC}$ Output Current, Readback Accuracy</td>
<td>$I_{IOUT}$ Channel 0 to Channel 3, $0 \leq I_{IOUT} \leq 25A$ Forced Continuous Mode, $MFR_{PWM_MODE[7]} = 1b$ See Histograms in Typical Performance Characteristics, (Note 12)</td>
<td>●</td>
<td></td>
<td>1.5A</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{O-RB}$ (31.25A) Full Load Output Current Readback</td>
<td>(Note 12), See Histograms in Typical Performance Characteristics</td>
<td>31.25</td>
<td></td>
<td></td>
<td>A</td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS

The • denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). \( T_A = 25^\circ\text{C}, \ V_{IN}, \ SV_{IN} = 12\text{V}, \ \text{RUNP} = 3.3\text{V}, \ \text{FREQUENCY}\_\text{SWITCH} = 425\text{kHz} \) and \( V_{OUT} \) commanded to 0.5V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICONVERT-IO-RB</td>
<td>Output Current Readback Update, Rate</td>
<td>MFR_ADC_CONTROL = 0x00, (Notes 9, 14) MFR_ADC_CONTROL = 0x06 (CH0.2 IOUT) or 0x0A (CH1.3 IOUT), (Notes 9, 14), See MFR_ADC_CONTROL SECTION</td>
<td>90</td>
<td>8</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

#### Input Current Readback

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>Resolution</td>
<td>(Note 10)</td>
<td>10</td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>VINSTP</td>
<td>LSB Step Size Full-Range = 16mV LSB Step Size Full-Range = 32mV LSB Step Size Full-Range = 64mV Gain = 8, 0V ( \leq</td>
<td>V_{INP}^+ - V_{INP}^-</td>
<td>\leq 5mV ) Gain = 4, 0V ( \leq</td>
<td>V_{INP}^+ - V_{INP}^-</td>
<td>\leq 20mV ) Gain = 2, 0V ( \leq</td>
</tr>
<tr>
<td>IN_TUE</td>
<td>Total Unadjusted Error Gain = 8, 2.5mV ( \leq</td>
<td>V_{INP}^+ - V_{INP}^-</td>
<td>), (Note 7) Gain = 4, 4mV ( \leq</td>
<td>V_{INP}^+ - V_{INP}^-</td>
<td>), (Note 7) Gain = 2, 6mV ( \leq</td>
</tr>
<tr>
<td>VDS</td>
<td>Zero-Code Offset Voltage ( (\text{Note 14}) )</td>
<td>( \pm 50 )</td>
<td></td>
<td></td>
<td>µV</td>
</tr>
<tr>
<td>ICONVERT</td>
<td>Update Rate ( (\text{Note 9, 14}), \ \text{See MFR_ADC_CONTROL SECTION for Faster Update Rates} )</td>
<td>90</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

#### Supply Current Readback (Note 15)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>Resolution</td>
<td>(Note 10)</td>
<td>10</td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>ICHIPSTP</td>
<td>LSB Step Size Full-Range = 256mV</td>
<td>Onboard 1Ω Resistor</td>
<td>244</td>
<td></td>
<td>µV</td>
</tr>
<tr>
<td>ICHIP_RB</td>
<td>ICHIP Readback</td>
<td>SVIN_Ran Current</td>
<td>50</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>ICONVERT</td>
<td>Update Rate ( (\text{Note 9, 14}), \ \text{See MFR_ADC_CONTROL SECTION for Faster Update Rates} )</td>
<td>90</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

#### Temperature Readback (T0, T1)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES-RB</td>
<td>Temperature Readback Resolution Channel ( n ), and Controller, (Note 14)</td>
<td></td>
<td></td>
<td></td>
<td>( ^\circ\text{C} )</td>
</tr>
<tr>
<td>T0_TUE</td>
<td>External Temperature Total Unadjusted Readback Error</td>
<td></td>
<td></td>
<td></td>
<td>( ^\circ\text{C} )</td>
</tr>
<tr>
<td>T1_TUE</td>
<td>Internal TSN6 TUE ( V_{RUNP} = 0V, \ FSYNC = 0kHz, \ (\text{Note 7}) )</td>
<td>( \pm 1 )</td>
<td></td>
<td></td>
<td>( ^\circ\text{C} )</td>
</tr>
<tr>
<td>ICONVERT</td>
<td>Update Rate ( (\text{Note 9}), \ \text{MFR_ADC_CONTROL} = 0x04, \ 0x0C, \ or \ 0x08 \ (\text{Notes 9, 14}) )</td>
<td>90</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

#### INTCGC_ran Regulator, VBias

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VINTGC_ran</td>
<td>Internal ( V_{CC} ) Voltage No Load</td>
<td>( 6V \leq SVIN_ran \leq 14V ) •</td>
<td>5.25</td>
<td>5.5</td>
<td>5.75</td>
</tr>
<tr>
<td>V_LDO INT</td>
<td>INTGC Load Regulation</td>
<td>( I_{CC} = 0mA ) to 50mA, ( 6V \leq SVIN_ran \leq 14V )</td>
<td>0.5</td>
<td></td>
<td>( \pm 2 )</td>
</tr>
<tr>
<td>VINBIA</td>
<td>Input Range for ( VIN_{BIA} )</td>
<td></td>
<td>7</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>RUNP</td>
<td>( V_{BIA} ) Enable</td>
<td>( V_{RUNP} ) Rising</td>
<td>0.8</td>
<td>0.85</td>
<td></td>
</tr>
<tr>
<td>VBIA</td>
<td>5.5V Internal Regulator</td>
<td>( 7V \leq VIN_{BIA} \leq 14V, \ SVIN_{BIA, ran} &gt; 7V )</td>
<td>5.25</td>
<td>5.5</td>
<td>5.75</td>
</tr>
<tr>
<td>SVIN_THR</td>
<td>( V_{SVIN, ran} ) Threshold to Enable ( V_{BIA} ) Switchover</td>
<td>( SVIN_{ran} ) Rising</td>
<td>7</td>
<td>7.5</td>
<td></td>
</tr>
<tr>
<td>SVIN_THF</td>
<td>( V_{SVIN, ran} ) Threshold to Disable ( V_{BIA} ) Switchover</td>
<td>( SVIN_{ran} ) Falling</td>
<td>6.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS** The • denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). $T_A = 25^\circ C$, $V_{IN}$, $SV_{IN}$ = 12V, $RUN = 3.3V$, $RUNP = 12V$, $FREQUENCY\_SWITCH = 425kHz$ and $V_{OUTP}$ commanded to 0.5V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD33_nn}$</td>
<td>Internal $V_{DD33}$ Voltage</td>
<td>$V_{INTVCC_nn} &gt; 4.5V$</td>
<td>3.2</td>
<td>3.3</td>
<td>3.4</td>
<td>V</td>
</tr>
<tr>
<td>$I_{LIM}$</td>
<td>$V_{DD33}$ Current Limit</td>
<td>$V_{DD33_nn} = GND, V_{IN_nn} = INTVCC_nn = 4.5V$</td>
<td>100</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD33_OV}$</td>
<td>$V_{DD33}$ Overvoltage Threshold</td>
<td>(Note 14)</td>
<td>3.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD33_UV}$</td>
<td>$V_{DD33}$ Undervoltage Threshold</td>
<td>(Note 14)</td>
<td>3.1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD25_nn}$</td>
<td>Internal $V_{DD25}$ Voltage</td>
<td></td>
<td>2.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{LIM}$</td>
<td>$V_{DD25}$ Current Limit</td>
<td>$V_{DD25_nn} = GND, V_{IN_nn} = INTVCC_nn = 4.5V$</td>
<td>80</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Oscillator and Phase-Locked Loop (PLL)**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{RANGE}$</td>
<td>PLL SYNC Range</td>
<td>Synchronized with Falling Edge of SYNC, $V_{IN} = 12V$</td>
<td>250</td>
<td>750</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>$I_{OSC}$</td>
<td>Oscillator Frequency Accuracy</td>
<td>Frequency Switch = 250kHz to 1000kHz, (Note 14)</td>
<td>•</td>
<td>±7.5</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$V_{TH(SYNC_nn)}$</td>
<td>SYNC Input Threshold (Note 14)</td>
<td></td>
<td>1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{TH(SYNCC_nn)}$</td>
<td></td>
<td>1.5</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL(SYNC_nn)}$</td>
<td>SYNC Low Output Voltage</td>
<td>$I_{LOAD} = 3mA$, (Note 14)</td>
<td>0.2</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{LEAK(SYNC_nn)}$</td>
<td>SYNC Leakage Current in Subordinate Mode</td>
<td>$0V \leq V_{SYNC_nn} \leq 3.6V$</td>
<td>±5</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$0SYNC\_00,02$:

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_PWM_CONFIG[2:0] = 0.2,3 (Note 14)</td>
<td></td>
<td></td>
<td>0</td>
<td>Deg</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_PWM_CONFIG[2:0] = 5</td>
<td></td>
<td>60</td>
<td>Deg</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_PWM_CONFIG[2:0] = 1</td>
<td></td>
<td>90</td>
<td>Deg</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_PWM_CONFIG[2:0] = 4.6</td>
<td></td>
<td>120</td>
<td>Deg</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$0SYNC\_01,03$:

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_PWM_CONFIG[2:0] = 3 (Note 14)</td>
<td></td>
<td></td>
<td>120</td>
<td>Deg</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_PWM_CONFIG[2:0] = 0</td>
<td></td>
<td>180</td>
<td>Deg</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_PWM_CONFIG[2:0] = 2,4,5</td>
<td></td>
<td>240</td>
<td>Deg</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_PWM_CONFIG[2:0] = 1</td>
<td></td>
<td>270</td>
<td>Deg</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_PWM_CONFIG[2:0] = 6</td>
<td></td>
<td>300</td>
<td>Deg</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**EEPROM Characteristics**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Endurance</td>
<td>(Note 15)</td>
<td>$0^\circ C \leq T_J \leq 85^\circ C$ During EEPROM Write Operations</td>
<td>•</td>
<td>10,000</td>
<td>Cycles</td>
<td></td>
</tr>
<tr>
<td>Retention</td>
<td>(Note 15)</td>
<td>$T_J &lt; 125^\circ C$</td>
<td></td>
<td>10</td>
<td>Years</td>
<td></td>
</tr>
<tr>
<td>Mass_Write</td>
<td></td>
<td>STORE_USER_ALL, $0^\circ C \leq T_J &lt; 85^\circ C$ During EEPROM Write Operation</td>
<td></td>
<td>440</td>
<td>4100</td>
<td>ms</td>
</tr>
</tbody>
</table>

**Leakage Current SDA\_nn, SCL\_nn, ALERT\_nn, RUN\_nn**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{OL}$</td>
<td>Input Leakage Current</td>
<td>$0V \leq V_{PIN} \leq 5.5V$</td>
<td>•</td>
<td>±5</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>Input Leakage Current</td>
<td>$0V \leq V_{PIN} \leq 3.6V$</td>
<td>•</td>
<td>±2</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

**Digital Inputs SCL\_nn, SDA\_nn, RUN\_nn**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Threshold Voltage</td>
<td></td>
<td>1.35</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Threshold Voltage</td>
<td></td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{HYST}$</td>
<td>Input Hysteresis</td>
<td>SCL, SDA</td>
<td>0.08</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{PIN}$</td>
<td>Input Capacitance</td>
<td></td>
<td>10</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Digital Input WP\_nn (Note 14)**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{PUWP}$</td>
<td>Input Pull-Up Current</td>
<td>WP</td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). $T_A = 25^\circ C$, $V_{IN} = 12V$, $V_{OUT} = 3.3V$, $RUNP = 12V$, $FREQUENCY\_SWITCH = 425kHz$ and $V_{OUT}$ commanded to 0.5V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open-Drain Outputs $SCL_nn$, $SDA_nn$, $FAULT_nn$, $ALERT_nn$, $RUN_nn$, $SHARE_CLK_nn$, $PGOOD_nn$</td>
<td>$V_{OL}$ Output Low Voltage</td>
<td>$I_{SINK} = 3mA$</td>
<td>0.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Digital Inputs $SHARE_CLK_nn$, $WP_nn$ (Note 14)</td>
<td>$V_{IH}$ Input High Threshold Voltage</td>
<td>●</td>
<td>1.5</td>
<td>1.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{IL}$ Input Low Threshold Voltage</td>
<td>●</td>
<td>0.6</td>
<td>1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Digital Filtering of $FAULT_nn$ (Note 14)</td>
<td>$I_{FLTG}$ Input Digital Filtering $FAULT_nn$</td>
<td>3</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Digital Filtering of $PGOOD_nn$ (Note 14)</td>
<td>$I_{FLTG}$ Output Digital Filtering $PGOOD_nn$</td>
<td>100</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Digital Filtering of $RUN_nn$ (Note 14)</td>
<td>$I_{FLTG}$ Input Digital Filtering $RUN$</td>
<td>10</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMBus Interface Timing Characteristics (Note 14)</td>
<td>$f_{SCL}$ Serial Bus Operating Frequency</td>
<td>●</td>
<td>10</td>
<td>400</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{BUF}$ Bus Free Time Between Stop and Start</td>
<td>●</td>
<td>1.3</td>
<td></td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{HD(STA)}$ Hold Time After Repeated Start Condition after This Period, the First Clock is Generated</td>
<td>●</td>
<td>0.6</td>
<td></td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{SU(STA)}$ Repeated Start Condition Setup Time</td>
<td>●</td>
<td>0.6</td>
<td>10000</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{SU(STO)}$ Stop Condition Setup Time</td>
<td>●</td>
<td>0.6</td>
<td></td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{HD(DAT)}$ Date Hold Time Receiving Data Transmitting Data</td>
<td>●</td>
<td>0</td>
<td></td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{SU(DAT)}$ Data Setup Time Receiving Data</td>
<td>●</td>
<td>0.3</td>
<td>0.9</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Stuck PMBus Timer Non-Block Reads Stuck PMBus Timer Block Reads</td>
<td>$t_{TIMEOUT_SMB}$ Measured from the Last PMBus Start Event</td>
<td>32</td>
<td>255</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{LOW}$ Serial Clock Low Period</td>
<td>●</td>
<td>1.3</td>
<td>10000</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{HIGH}$ Serial Clock High Period</td>
<td>●</td>
<td>0.6</td>
<td></td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTM4683 is tested under pulsed-load conditions such that $T_J = T_A$. The LTM4683E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4683I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. $T_J$ is calculated from the ambient temperature $T_A$ and the power dissipation $P_D$ according to the following formula: $T_J = T_A + (P_D \times \theta_{JA})$.

**Note 3:** All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

**Note 4:** The power inputs—$V_{IN01}$ and $V_{IN23}$—and their respective power outputs—$V_{OUT}\_1$ and $V_{OUT}\_3$—are tested independently in production. A shorthand notation is used in this document that allows these parameters to be referred to by “$V_{INn}$” and “$V_{OUTn}$”, where $n$ is permitted to take on a value of 0 to 3. This italicized “$n$” notation and convention is extended to encompass all such pin names, and register names with channel-specific, i.e., paged data. For example, $VOUT\_COMMAND\_n$ refers to the $VOUT\_COMMAND$ command code data located in Pages 0 and 1, which in
ELECTRICAL CHARACTERISTICS

turn relate to Channel 0, 2 (VOUT ±2), and Channel 1, 3 (VOUT ±3). Registers containing non-page-specific data, i.e., whose data is “global” to the module, or applies to all of the module’s channels, lack the italicized “n”, e.g., FREQUENCY_SWITCH.

Note 5: VOUT (DC) and line and load regulation tests are performed in production with digital servo disengaged (MFR_PWM_MODE[6] = 0b), and low VOUT range selected MFR_PWM_MODE[1] = 1b. The digital servo control loop is exercised in production (setting MFR_PWM_MODE[6] = 1b). However, the convergence of the output voltage to its final settling value is not necessarily observed in the final test—due to potentially long-time constants involved—and is instead guaranteed by the output voltage readback accuracy specification. Evaluation in application demonstrates capability; see the Typical Performance Characteristics section.

Note 6: See output current derating curves for different VIN, VOUT, and Tª, located in the Applications Information section.

Note 7: Part tested with pulse-width modulation disabled. Evaluation in application demonstrates capability. TUE(%) = analog-to-digital converter (ADC) gain error (%) + 100 (zero code offset + ADC Linearity Error)/Actual Value.

Note 8: Minimum on-time is tested at wafer sort.

Note 9: The data conversion is done by default in a round-robin fashion. All input signals are continuously converted for a typical latency of 90ms. Setting MFR_ADC_CTRL value to be 0 to 12, LTM4683 can do fast data conversion with only 8ms to 10ms. See the PMBus Command Details section.

Note 10: The following telemetry parameters are formatted in PMBus-defined “Linear Data Format”, in which each register contains a word comprised of 5 most significant bits—representing a signed exponent, to be raised to the power of 2—and 11 least significant bits—representing a signed mantissa: input voltage (on SVIN,nn), accessed through the READ_VIN command code; output currents (IOUT,nn), accessed through the READ_IOUTn command codes; module input current (IVIN,nn + IVIN,nn + ISVIN,nn), accessed through the READ_IN command code; channel input currents (IVIN,nn + 1/2 • ISVIN,nn), accessed through the MFR_READ_IINn command codes; and duty cycles of Channel 0 and Channel 1 switching power stages, accessed through the READ_DUTY_CYCLEn command codes. This data format limits the resolution of telemetry readback data to 10 bits, even though the internal ADC is 16 bits and the LTM4683’s internal calculations use 32-bit words.

Note 11: The absolute maximum rating for the SVIN,nn pin is 16V. Input voltage telemetry (READ_VIN) is obtained by digitizing a voltage scaled down from the SVIN,nn pin.

Note 12: These typical parameters are based on bench measurements and are not production tested.

Note 13: Channel 0 to Channel 3 OV/UV comparator threshold accuracy for 0.3V to 0.7V are 5%.

Note 14: Tested at IC-level automatic test equipment (ATE).

Note 15: The LTM4683’s EEPROM temperature range for valid write commands is 0°C to 85°C. To achieve guaranteed EEPROM data retention, execution of the “STORE_USER_ALL” command—i.e., uploading RAM contents to NVM (nonvolatile memory)—outside this temperature range is not recommended. However, if the LTM4683’s EEPROM temperature is less than 130°C, the LTM4683 will obey the STORE_USER_ALL command. Only when EEPROM temperature exceeds 130°C the LTM4683 will not act on any STORE_USER_ALL transactions; instead, the LTM4683 NACKs the serial command and asserts its relevant CML (communications, memory, logic) fault bits. EEPROM temperature can be queried before commanding STORE_USER_ALL; see the Applications Information section.

Note 16: The LTM4683 includes overtemperature (OT) protection intended to protect the device during momentary overload conditions. The junction temperature will exceed 125°C when OT protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Figure 1. Programmable RCOMPn

For more information www.analog.com
TYPICAL PERFORMANCE CHARACTERISTICS  \( T_A = 25^\circ\text{C}, \) unless otherwise noted.

**Single Channel Efficiency, 5V\(_{\text{IN}}\),**  
\( V_{\text{IN}} = SV_{\text{IN}} = INTV_{\text{CC}} = 5\text{V}, \)  
RUNP = 0V, Continuous-Conduction Mode (CCM)

**Single Channel Efficiency, 8V\(_{\text{IN}}\),**  
\( V_{\text{IN}} = SV_{\text{IN}} = V_{\text{IN}}\text{ VB\text{IAS}} = 8\text{V}, \)  
RUNP = 8V, CCM

**Single Channel Efficiency, 12V\(_{\text{IN}}\),**  
\( V_{\text{IN}} = SV_{\text{IN}} = V_{\text{IN}}\text{ VB\text{IAS}} = 12\text{V}, \)  
RUNP = 12V, CCM

**Quad Channel Single Output Efficiency**  
\( V_{\text{IN}} = SV_{\text{IN}} = V_{\text{IN}}\text{ VB\text{IAS}} = \)  
RUNP = 12V, CCM
TYPICAL PERFORMANCE CHARACTERISTICS  \( T_A = 25^\circ \text{C}, \) unless otherwise noted.

Single Channel Load Transient Response (0A) to (10A) Load Step, 10A/µs, \( V_{\text{IN}} = 12\text{V}, \ V_{\text{OUT}} = 0.3\text{V}, \ f_{\text{SW}} = 250\text{kHz} \)

Single Channel Load Transient Response (0A) to (10A) Load Step, 10A/µs, \( V_{\text{IN}} = 12\text{V}, \ V_{\text{OUT}} = 0.6\text{V}, \ f_{\text{SW}} = 500\text{kHz} \)

Single Channel Load Transient Response (0A) to (10A) Load Step, 10A/µs, \( V_{\text{IN}} = 12\text{V}, \ V_{\text{OUT}} = 0.4\text{V}, \ f_{\text{SW}} = 350\text{kHz} \)

Single Channel Load Transient Response (0A) to (10A) Load Step, 10A/µs, \( V_{\text{IN}} = 12\text{V}, \ V_{\text{OUT}} = 0.7\text{V}, \ f_{\text{SW}} = 575\text{kHz} \)
TYPICAL PERFORMANCE CHARACTERISTICS  

**Quad Output Concurrent Rail, Start-Up, Pre-Bias**

$V_{OUT3} = 0.7V$
$V_{OUT2} = 0.6V$
$V_{OUT1} = 0.5V$
$V_{OUT0} = 0.4V$

FIGURE 48 CIRCUIT, $12V_{IN}$, 10A ON $V_{OUT0}$
NO LOAD ON OTHER OUTPUTS AND 180mV PRE-BIAS ON $V_{OUT0}$

**Single Phase Single Output**

12V to 0.5V, No Load
Short-Circuit Protection

$V_{OUT0}, 0.5V$

FIGURE 48 CIRCUIT, $12V_{IN}$
NO LOAD ON $V_{OUT0}$
PRIOR TO APPLICATION OF SHORT-CIRCUIT
USE HIGH RANGE OF I$_{OUT}$ SYSTEM
SHORT-CIRCUIT USING LOW IMPEDANCE COPPER ACROSS OUTPUT (HARD SHORT)

**Quad Output Concurrent Rail, Start-Up, Pre-Bias**

$V_{OUT3} = 0.7V$
$V_{OUT2} = 0.6V$
$V_{OUT1} = 0.5V$
$V_{OUT0} = 0.4V$

FIGURE 48 CIRCUIT, $12V_{IN}$, 10A ON $V_{OUT0}$
NO LOAD ON OTHER OUTPUTS AND 180mV PRE-BIAS ON $V_{OUT0}$

**Single Phase Single Output**

12V to 0.5V, 31.25A Load
Short-Circuit Protection

$V_{OUT0}, 0.5V$

FIGURE 48 CIRCUIT, $12V_{IN}$
31.25A LOAD ON $V_{OUT0}$
PRIOR TO APPLICATION OF SHORT-CIRCUIT
USE HIGH RANGE OF I$_{OUT}$ SYSTEM
SHORT-CIRCUIT USING LOW IMPEDANCE COPPER ACROSS OUTPUT (HARD SHORT)

$V_{IN} = SV_{IN} = 12V$, $V_{OUT} = 0.5V$, FREQ = 425kHz, $I_{OUT} = 31.25A$

I$_{OUT}$ READBACK AT 31.25A

COLOR BY TEMPERATURE
-40°C
+25°C
+125°C

VARIOUS OUTPUT CHANNELS
PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.


VIN01 (A5-A6, B5-B6, C5-C6, D5-D6, E5-E6, F5-F6, G5-G6, H5-H6, J5-J6, K5-K6): Positive Power Input to Channel 0 and Channel 1 Switching Stages. These pins provide sufficient decoupling capacitance in the form of multilayer ceramic capacitors (MLCCs) and low ESR electrolytic (or equivalent) to handle reflected input current ripple from the step-down switching stage. MLCCs should be placed as close to the LTM4683 as physically possible. See the Layout Checklist/Example section in the Applications Information section.

VOUT0_CFG (A8): Output Voltage Select Pin for VOUT0, Coarse Setting. If the VOUT0_CFG and VTRIMO_CFG pins are both left open—or, if the LTM4683 is configured to ignore pin-strap (RCONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1b—then the LTM4683s target VOUT0 output voltage setting (VOUT0_COMMAND) and associated power-good and OV/UV warning and fault thresholds are dictated at SVIN01 power-up according to the LTM4683’s NVM contents. A resistor divider connected to 2.5V and to SGND (see Table 1)—in combination with resistor pin settings on VTRIMO_CFG, and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0b—can be used to configure the LTM4683’s Channel 0 output to power-up to a VOUT_COMMAND value (and associated output voltage monitoring and protection/fault-detection thresholds) different from those of NVM contents. (See the Applications Information section.) Connecting resistor(s) from VOUT0_CFG to SGND and/or VTRIMO_CFG to SGND in this manner allows a convenient way to configure multiple LTM4683s with identical NVM contents for different output voltage settings all without GUI intervention or the need to custom-preprogram module NVM contents. Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that using RCONFIGs on VOUT0_CFG/VTRIMO_CFG can affect the VOUT0 range setting (MFR_PWM_MODE[1]) and loop gain. For addressed ASEL_01, Page 0x00 corresponds to Channel 0, and Page 0x01 corresponds to Channel 1. See PAGE description section.

FSWH01_CFG (A9): Switching Frequency, Channel Phase-Interleaving Angle and Phase Relationship to SYNC Configuration Pin for Channel 0 and Channel 1. If this pin is left open—or, if the LTM4683 is configured to ignore pin-strap (RCONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1b—then LTM4683’s switching frequency (FREQUENCY_SWITCH) and channel phase relationships (with respect to the SYNC clock; MFR_PWM_CONFIG[2:0]) are dictated at SVIN01 power-up according to the LTM4683’s NVM contents for Channel 0 and Channel 1. Default factory values are 425kHz operation, Channel 0 at 0°, and Channel 1 at 180°C (convention throughout this document: a phase angle of 0° means the channel’s switch node rises coincident with the falling edge of the SYNC pulse). Connecting a resistor divider from 2.5V to SGND (and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0b) allows a convenient way to configure multiple LTM4683s with identical NVM contents for different switching frequencies of operation and phase interleaving angle settings of intra- and extra-module-paralleled channels—all, without GUI intervention or the need to custom pre-program module NVM contents. (See the Applications Information section.) Minimizing capacitance ensures accurate detection of the pin state.

FAULT0, FAULT1, FAULT2, and FAULT3 (A11, A10, V10, W10): Digital Programmable FAULT inputs and Outputs. Open-drain output. A pull-up resistor to 3.3V is required in the application.

VOUT0 (A13-A15, B13-B15, C13-C15, D13-D15, E13-E15): Channel 0 Output Voltage. Place recommended output capacitors from this shape to GND. See the Layout Checklist/Example section.
**PIN FUNCTIONS**

**VOUT2_CFG (AA8):** Output Voltage Select Pin for VOUT2. Coarse Setting. If the VOUT2_CFG and VTRIM2_CFG pins are both left open—or, if the LT4683 is configured to ignore pin-strap (R_CONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1b—then the LT4683s target VOUT2 output voltage setting (VOUT_COMMAND) and associated power-good and OV/UV warning and fault thresholds are dictated at SVIN_23 power-up according to the LT4683’s NVM contents. A resistor divider connected to 2.5V and SGND to this pin—in combination with resistor pin settings on VTRIM2_CFG, and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0b—can be used to configure the LT4683’s Channel 2 output to power-up to a VOUT_COMMAND value (and associated output voltage monitoring and protection/fault-detection thresholds) different from those of NVM contents. (See the Applications Information section.) Connecting resistor(s) from VOUT2_CFG to SGND and/or VTRIM2_CFG to SGND in this manner allows a convenient way to configure multiple LT4683s with identical NVM contents for different output voltage settings all without GUI intervention or the need to custom-preprogram module NVM contents. Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that using R_CONFIGs on VOUT2_CFG/VTRIM2_CFG can affect the VOUT2 range setting (MFR_PWM_MODE[0][1]) and loop gain. For addressed ASEL_23, Page 0x00 corresponds to Channel 2, and Page 0x01 corresponds to Channel 3. See PAGE description section.

**FSWH23_CFG (AA9):** Switching Frequency, Channel Phase-Interleaving Angle and Phase Relationship to SYNC Configuration Pin for Channel 2 and Channel 3. If this pin is left open—or, if the LT4683 is configured to ignore pin-strap (R_CONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1b—then LT4683’s switching frequency (FREQUENCY SWITCH) and channel phase relationships (with respect to the SYNC clock; MFR_PWM_CONFIG[2:0]) are dictated at SVIN_23 power-up according to the LT4683’s NVM contents for Channel 2 and Channel 3. Default factory values are 425kHz operation, Channel 2 at 0°, and Channel 3 at 180°C (convention throughout this document: a phase angle of 0° means the channel’s switch node rises coincident with the falling edge of the SYNC pulse). Connecting a resistor divider from 2.5V to SGND (and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0b) allows a convenient way to configure multiple LT4683s with identical NVM contents for different switching frequencies of operation and phase interleaving angle settings of intra- and extra-module-paralleled channels—all, without GUI intervention or the need to custom pre-program module NVM contents. (See the Applications Information section.) Minimize capacitance especially when the pin is left open—to ensure accurate detection of the pin state.

**ASEL_23 (AA10):** Serial Bus Address Configuration Pin for Channel 2 and Channel 3 Controller. On any given I²C/SMBus serial bus segment, every device must have its unique subordinate address. If this pin is left open, the LT4683 powers up to its default subordinate address of 0x0F (hexadecimal), i.e., 1001111b (industry-standard convention is used throughout this document: 7-bit subordinate addressing). The lower four bits of the LT4683’s subordinate address can be altered from this default value by connecting a resistor from this pin to SGND. Minimize capacitance especially when the pin is left open—to ensure accurate detection of the pin state. It is recommended to use a resistor to set the address. The ASEL_23 address will be used to address Channels 2 and 3, and a different ASEL_01 address will be used to address Channel 0 and Channel 1. For addressed ASEL_23, Page 0x00 corresponds to Channel 2, and Page 0x01 corresponds to Channel 3. See PAGE description section. The GUI will represent Channel 2 as U1:B0 and Channel 3 as U1:B1. See Figure 32.

**VOUT3_CFG (AB8):** Output Voltage Select Pin for VOUT3. Coarse Setting. If the VOUT3_CFG and VTRIM3_CFG pins are both left open—or, if the LT4683 is configured to ignore pin-strap (R_CONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1b—then the LT4683s target VOUT3 output voltage setting (VOUT_COMMAND) and associated power-good and OV/UV warning and fault thresholds are dictated at SVIN_23 power-up according to the LT4683’s NVM contents. A resistor divider connected to 2.5V and SGND to this pin—in combination with resistor pin settings on VTRIM3_CFG, and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0b—can be used to
PIN FUNCTIONS

configure the LTM4683’s Channel 3 output to power-up to a VOUT_COMMAND value (and associated output voltage monitoring and protection/fault-detection thresholds) different from those of NVM contents. (See the Applications Information section.) Connecting resistor(s) from VOUT3_CFG to SGND and/or VTRIM3_CFG to SGND in this manner allows a convenient way to configure multiple LTM4683s with identical NVM contents for different output voltage settings all without GUI intervention or the need to custom-preprogram module NVM contents. Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that using RCONFIGs on VOUT3_CFG/VTRIM3_CFG can affect the VOUT3 range setting (MFR_PWM_MODE[1]) and loop gain. For addressed ASEL_23, Page 0x00 corresponds to Channel 2, and Page 0x01 corresponds to Channel 3. See PAGE description section.

VTRIM3_CFG (AB9): Output Voltage Select Pin for VOUT3. Fine Setting. Works in combination with VOUT3_CFG to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 3, at SVIN_23 power-up. (See VOUT3_CFG and the Applications Information section.) A resistor divider from 2.5V to SGND connected to the pin will set the TRIM value. See Table 2. Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that using RCONFIGs on VOUT3_CFG/VTRIM3_CFG can affect the VOUT3 range setting (MFR_PWM_MODE[1]) and loop gain. For addressed ASEL_23, Page 0x00 corresponds to Channel 2, and Page 0x01 corresponds to Channel 3. See PAGE description section.

VTRIM2_CFG (AB10): Output Voltage Select Pin for VOUT2. Fine Setting. Works in combination with VOUT2_CFG to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 2, at SVIN_23 power-up. (See VOUT2_CFG and the Applications Information section.) A resistor divider from 2.5V to SGND connected to the pin will set the TRIM value. See Table 2. Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that using RCONFIGs on VOUT2_CFG/VTRIM2_CFG can affect the VOUT2 range setting (MFR_PWM_MODE[1]) and loop gain. For addressed ASEL_23,
PIN FUNCTIONS

convention is used throughout this document: 7-bit subordinate addressing). The lower four bits of the LTM4683’s subordinate address can be altered from this default value by connecting a resistor from this pin to SGND. Minimize capacitance—especially when the pin is left open—to ensure accurate detection of the pin state. It is recommended to use a resistor to set the address. The ASEL_01 address will be used to address Channels 0 and 1, and a different ASEL_23 address will be used to address Channels 2 and 3. For addressed ASEL_01, Page 0x00 corresponds to Channel 0, and Page 0x01 corresponds to Channel 1. See PAGE description section. The GUI will represent Channel 0 as U0:A0 and Channel 1 as U0:A1. See Figure 32.

RUN0, RUN1 (B10, B11, Respectively): Enable Run Input for Channels 0 and 1, respectively—Open-drain input and output. The logic high on these pins enables the respective outputs of the LTM4683. These open-drain output pins hold the pin low until the LTM4683 is out of reset and SVIN_01 is detected to exceed VIN_ON. A pull-up resistor to 3.3V is required in the application. The LTM4683 pulls RUN0 and/or RUN1 low, as appropriate, when a global fault and/or channel-specific fault occurs whose fault response is configured to latch off and cease regulation, issuing a CLEAR_FAULTS command via I2C or power-cycling SVIN_01 is necessary to restart the module, in such cases. Do not pull RUN logic high with a low impedance source. INTVCC is active when SVIN_01 is above UVLO. This provides power to the VDD33 and VDD25 to allow programming the EEPROM.

SW0 (C1-C2, D1-D2, E1-E2): Switching Node of Channel 0 Step-Down Converter Stage. Used for test purposes or EMI-snubbing. It may be routed a short distance to a local test point to monitor the switching action of Channel 0, if desired, but do not route near any sensitive signals. Otherwise, leave it electrically isolated (open).

VDD25_01 (C8): Internally Generated 2.5V Power Supply Output Pin for Channel 0 and Channel 1 Circuits. Do not load this pin with the external current; it is used strictly to bias internal logic and provides current for the internal pull-up resistors connected to the configuration-programming pins. No external decoupling is required.

VTRIM1_CFG (C9): Output Voltage Select Pin for VOUT1. Fine Setting. Works in combination with VOUT1_CFG to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 1, at SVIN_01 power-up. (See VOUT1_CFG and the Applications Information section.) A resistor divider from 2.5V to SGND connected to the pin will set the TRIM value. See Table 2. Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that using RCONFIG on VOUT1_CFG/VTRIM1_CFG can affect the VOUT1 range setting (MFR_PWM_MODE1[1]) and loop gain. For addressed ASEL_01, Page 0x00 corresponds to Channel 0, and Page 0x01 corresponds to Channel 1. See PAGE description section.

SDA_01, SDA_23 (C10, V8): Serial Bus Data Open-Drain Input and Output. A pull-up resistor to 3.3V is required in the application. SDA_01 is for Channel 0 and Channel 1, and SDA_23 is for Channel 2 and Channel 3.

ALERT_01, ALERT_23 (C11, W8): Open-Drain Digital Output. A pull-up resistor to 3.3V is required in the application only if SMBALERT interrupt detection is implemented in one’s SMBus system.

SHARE_CLK_01, SHARE_CLK_23 (D8, AA11): Share Clock, Bidirectional Open-Drain Clock Sharing Pins. Nominally 100kHz. They are used for synchronizing the time base between multiple LTM4683s (and any other Analog Devices products with a SHARE_CLK pin) to realize well-defined rail sequencing and rail tracking. Connect the SHARE_CLK pins of all such devices together; all devices with a SHARE_CLK pin will synchronize to the fastest clock. A pull-up resistor to 3.3V is only required when synchronizing the time base between devices.

VTRIMO_CFG (D9): Output Voltage Select Pin for VOUT0. Fine Setting. Works in combination with VOUT0_CFG to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 0, at SVIN_01 power-up. (See VOUT0_CFG and the Applications Information section.) A resistor divider from 2.5V to SGND connected to the pin will set the TRIM value. See Table 2. Minimize capacitance especially when the pin is left open to ensure accurate detection
PIN FUNCTIONS

of the pin state. Note that using $R_{\text{CONFIG}}$ on VOUT0_CFG/VTRIMO_CFG can affect the VOUT range setting (MFR_PWM_MODE0[1]) and loop gain. For addressed ASEL_01, Page 0x00 corresponds to Channel 0, and Page 0x01 corresponds to Channel 1. See PAGE command description section.

SCL_01, SCL_23 (D10, W9): Serial Bus Clock Open-Drain Input (Can Be an Input and Output, if Clock Stretching is Enabled). A pull-up resistor to 3.3V is required in the application for digital communication to the SMBus main device(s) that nominally drive this clock. The LTM4683 will never encounter scenarios where it would need to engage clock stretching unless serial clock line (SCL) communication speeds exceed 100kHz—and even then, LTM4683 will not clock stretch unless clock stretching is enabled by using the setting MFR_CONFIG_ALL[1] = 1b. The factory-default NVM configuration setting has MFR_CONFIG_ALL[1] = 0b: clock stretching disabled. If communication on the bus at clock speeds above 100kHz is required, the user’s SMBus main device(s) needs to implement clock stretching support to ensure solid serial bus communications, and only, then should MFR_CONFIG_ALL[1] be set to 1b. When clock stretching is enabled, SCL becomes a bidirectional, open-drain output pin on the LTM4683.

SYNC_01, SYNC_23 (D11, V9): External Clock Synchronization Input and Open-Drain Output Pin. If an external clock is present at this pin, the switching frequency will be synchronized to the external clock. If the main clock mode is enabled, this pin will pull low at the switching frequency with a 500ns pulse to the ground. A resistor pull-up to 3.3V is required in the application if the LTM4683 is the main device.

VDD33_01 (E8): Internally Generated 3.3V Power Supply Output Pin for Channel 0 and Channel 1 Circuits. This pin should only be used to provide external current for the pull-up resistors required for FAULTn, SHARE_CLK_n, and SYNC_n, and may be used to provide current for pull-up resistors on RUNn, SDA_n, SCL_n, ALERT_n and PGOODn. Where n is either 0,1 or 2,3 channels, and n is the actual channel. No external decoupling is required. VDD33_01 is powered from VBIAS, that programming RUNn improves efficiency.

WP_01, WP_23 (E9, Y11): Write Protect Pin, Active High. An internal 10µA current source pulls this pin to VDD33. If WP is open circuit or logic high, only I²C writes to PAGE, OPERATION, CLEAR_FAULTS, MFR_CLEAR_PEAKS and MFR_EE_UNLOCK are supported. Additionally, Individual faults can be cleared by writing 1b’s to bits of interest in registers prefixed with STATUS. If WP is low, I²C writes are unrestricted.

TSNS0, TSNS1, TSNS2, TSNS3 (E11, E10, U8, U9): Power stage temperature monitors for the four channels. See the Applications Information section.

VOSNS1– (F8): Channel 1 Negative Differential Voltage Sense Input. See VOSNS1+.

SGND01, SGND23 (F10-F11, U10-U11): SGND is the signal ground return path of the LTM4683 internal controllers. SGND is not internally connected to GND. Connect SGND to GND local to the LTM4683. See the Layout Checklist/Example section.

VOUT1 (F13-F15, G13-G15, H13-H15, J13-J15, K13-K15): Channel 1 Output Voltage. Place recommended output capacitors from this output copper shape to GND. See the Layout Checklist/Example section.

SW1 (G1-G2, H1-H2, J1-J2): Switching Node of Channel 1 Step-Down Converter Stage. Used for test purposes or EMI-snubbing. It may be routed a short distance to a local test point to monitor the switching action of channel 1, if desired, but do not route near any sensitive signals. Otherwise, leave it open.

VOSNS1+ (G8): Channel 1 Positive Differential Voltage Sense Input. Together, VOSNS1+ and VOSNS1– serve to Kelvin-sense the VOUT1 output voltage at VOUT1’s point-of-load (POL) and provide the differential feedback signal directly to channel 1’s feedback loop. Command VOUT1’s target regulation voltage by serial bus. Its initial command value at SVIN_01 power-up is dictated by NVM contents (factory default: 0.5V)—or, optionally, may be set by configuration resistors; see VOUT1_CFG, VTRIM1_CFG and the Applications Information section.

COMP0b, COMP1b, COMP2b, COMP3b (G10, F9, T9, W11): Current Control Threshold and Error Amplifier Compensation Nodes. Each associated channel’s current...
PIN FUNCTIONS

comparator tripping threshold increases with its compensation voltage. Each channel has a 22pF to SGND.

COMP0a, COMP1a, COMP2a, COMP3a (G11, G9, T8, V11): Loop Compensation Nodes. The internal PWM loop compensation resistors R_{COMP} of the LTM4683 can be adjusted using bit[4:0] of the MFR_PWM_COMP command. The transconductance of the LTM4683 PWM error amplifier can be adjusted using bit[7:5] of the MFR_PWM_COMP command. These two loop compensation parameters can be programmed when the device is in operation. See the Programmable Loop Compensation subsection in the Applications Information section for further details. See Figure 1.

PGOOD0, PGOOD1, PGOOD2, PGOOD3 (H9, H8, R10, T10): Power Good Indicator Outputs. The open-drain logic output is pulled to the ground when the output exceeds the UV and OVP regulation window. The output is de-glitched by an internal 100µs filter. A pull-up resistor to 3.3V is required in the application.

I_{IN} (H10): Positive Current Sense Amplifier Input. If the input current sense amplifier is not used, this pin must be shorted to the I_{IN} and SV_{IN} pins. See the Applications Information section for more details about the input current sensing.

V_{OSNSO} (H11): Channel 0 Negative Differential Voltage Sense Input. See V_{OSNSO}+.

SV_{IN} (J8): Input Supply for LTM4683’s Internal Control IC for Channel 0 and Channel 1. In most applications, it connects to V\textsubscript{IN01}. SV_{IN} can be operated from an auxiliary supply separate from V\textsubscript{IN01} for powering the V\textsubscript{IN01} from a lower supply like 6V. The SV_{IN} pin requires 1Ω and 1µF decoupling capacitor to measure the actual control chip current. See MFR_READ_ICHP and MFR_ADC_CONTROL command section. When operating from 4.5V to 5.75V with no auxiliary bias supply, then the main device input supply should connect to SV_{IN} and INTV_{CC,01}. See Test Circuit 2 for an example. In this configuration, the I_{CHIP} current will not be relevant since INTV_{CC,01} is connected to SV_{IN}. See Input Voltage and Limits to update low V_{IN} operation parameters.

INTV_{CC,01} (J9): Internal Regulator, 5.5V Output. When operating the LTM4683 from 5.75V ≤ SV_{IN} ≤ 14V, an internal low dropout (LDO) generates INTV_{CC,01} to bias internal control circuits and the MOSFET drivers of the LTM4683’s Channel 0 and Channel 1. An external 4.7µF ceramic decoupling capacitor is required. INTV_{CC,01} is on regulated regardless of the RUNP pin state. When operating the LTM4683 with 4.5V ≤ SV_{IN} < 5.75V, INTV_{CC,01} must be electrically shorted to SV_{IN}, and the RUNP pin must be pulled to GND. V_{BIAS} takes over after startup when the input voltage is greater than 7V.

I_{IN}+ (J10): Negative Current Sense Amplifier Input. If the input current sense amplifier is not used, this pin must be shorted to the I_{IN} and SV_{IN} pins. See the Applications Information section for more details about the input current sensing.

V_{OSNSO}+ (J11): Channel 0 Positive Differential Voltage Sense Input. Together, V_{OSNSO}+ and V_{OSNSO}− serve to Kelvin-sense the V\textsubscript{OUT0} output voltage at V\textsubscript{OUT0}’s point-of-load (POL) and provide the differential feedback signal directly to Channel 0’s feedback loop. Command V\textsubscript{OUT0}’s target regulation voltage by serial bus. Its initial command value at SV_{IN} power-up is dictated by NVM contents (factory default: 0.5V)—or, optionally, may be set by configuration resistors; see VOUT0_CFG, VTRIM0_CFG and the Applications Information section.

V_{IN23} (N5-N6, P5-P6, R5-R6, T5-T6, U5-U6, V5-V6, W5-W6, Y5-Y6, AA5-AA6, AB5-AB6): Positive Power Input to Channel 2 and Channel 3 Switching Stages. Provide sufficient decoupling capacitance in the form of MLCCs and low ESR electrolytic (or equivalent) to handle reflected input current ripple from the step-down switching stage. MLCCs should be placed as close to the LTM4683 as physically possible. See the Layout Checklist/Example section in the Applications Information section.

V_{IN}_{BIAS} (N9): Input pin to the internal step-down regulator that produces 5.5V (V_{BIAS} pin) to power both internal controllers to reduce power dissipation after power up. Each internal controller has an INTV_{CC,01} or INTV_{CC,23} regulator that is powered from SV_{IN} or SV_{IN}.

www.analog.com
eliminate this power loss through these linear regulators, the $V_{BIAS}$ powers both at very high efficiency.

$V_{BIAS}$ (N10): 5.5V step-down output that powers both internal controllers to reduce power loss. Provide a 22µF ceramic bypass capacitor on this pin to GND. $SV_{IN_01}$ and $SV_{IN_23}$ must be higher than 7V for this $V_{BIAS}$ to supply the controllers. When the input voltage is between 4.5V to 5.75V, pull the RUNP pin to GND, and connect $SV_{IN_01}$ and $SV_{IN_23}$ to $INTV_{CC_01}$ and $INTV_{CC_23}$, respectively. Powering up the $V_{BIAS}$ regulator with the $SV_{IN_01}$ and $SV_{IN_23}$ greater than 7V will power the $INTV_{CC_01}$, $INTV_{CC_23}$, $V_{DD33_{01}}$, $V_{DD33_{23}}$, $V_{DD25_{01}}$, and $V_{DD25_{23}}$ from $V_{BIAS}$. Otherwise, these sources will get their power from $SV_{IN_01}$ and $SV_{IN_23}$. This will allow programming each internal controller’s EEPROM with the power regulator channels in the off position.

RUNP (N11): This pin enables the Internal 5.5V $V_{BIAS}$ Step-Down Regulator. Pulling this pin above 0.85V will enable the Internal regulator. The pin is rated to $V_{IN}$, so connect to $V_{IN}$ to enable, and connect to GND to disable. When the input voltage is between 4.5V to 5.75V, pull the RUNP pin to GND, and connect $SV_{IN_01}$ and $SV_{IN_23}$ to $INTV_{CC_01}$ and $INTV_{CC_23}$, respectively.

$V_{OUT2}$ (N13-N15, P13-P15, R13-R15, T13-T15, U13-U15): Channel 2 Output Voltage. Place recommended output capacitors from this shape to GND. See the Layout Checklist/Example section.

SW2 (P1-P2, R1-R2, T1-T2): Switching Node of Channel 2 Step-Down Converter Stage. Used for test purposes or EMI-snubbing. It may be routed a short distance to a local test point to monitor the switching action of Channel 2, if desired, but do not route near any sensitive signals. Otherwise, leave it open.

$V_{OSNS2^+}$ (P8): Channel 2 Positive Differential Voltage Sense Input. Together, $V_{OSNS2^+}$ and $V_{OSNS2^-}$ serve to Kelvin-sense the $V_{OUT2}$ output voltage at $V_{OUT2}$’s point-of-load (POL) and provide the differential feedback signal directly to Channel 2’s feedback loop. Command $V_{OUT2}$’s target regulation voltage by serial bus. Its initial command value at $SV_{IN_23}$ power-up is dictated by NVM (nonvolatile memory) contents (factory default: 0.5V)—or, optionally, may be set by configuration resistors; see VOUT2_CFG, VTRIM2_CFG and the Applications Information section.

$V_{IN_{23}^-}$ (P9): Negative Current Sense Amplifier Input. If the input current sense amplifier is not used, this pin must be shorted to the $I_{IN_{23}^+}$ and $SV_{IN_{23}}$ pins. See the Applications Information section for more details about the input current sensing.

$INTV_{CC_{23}}$ (P10): Internal Regulator, 5.5V Output. When operating the LTM4683 from 5.75V $\leq SV_{IN_{23}} \leq 14$V, an internal LDO generates $INTV_{CC_{23}}$ from $SV_{IN_{23}}$ to bias internal control circuits and the MOSFET drivers of the LTM4683’s Channel 2 and Channel 3. An external 4.7µF ceramic decoupling capacitor is required. $INTV_{CC_{23}}$ is regulated regardless of the RUNn pin state. When operating the LTM4683 with 4.5V $\leq SV_{IN_{23}} < 5.75$V, $INTV_{CC_{23}}$ must be electrically shorted to $SV_{IN_{23}}$, and the RUNP pin must be pulled to GND. $V_{BIAS}$ takes over after start-up when the input voltage is greater than 7V.

$SV_{IN_{23}}$ (P11): Input Supply for LTM4683’s Internal Control IC for Channel 2 and Channel 3. In most applications, $SV_{IN_{23}}$ connects to $V_{IN_{23}}$. $SV_{IN_{23}}$ can be operated from an auxiliary supply separate from $V_{IN_{23}}$ for powering the $IN_{23}$ from a lower supply like 6V. The $SV_{IN_{23}}$ pin requires 1Ω and 1µF decoupling capacitor to measure the actual control chip current. See MFR_READ_ICHIP and MFR_ADC_CONTROL command section. When operating from 4.5V to 5.75V with no auxiliary bias supply, then the main device input supply should connect to $SV_{IN_{23}}$ and $INTV_{CC_{23}}$. See Test Circuit 2 for an example. In this configuration, the $I_{CHIP}$ current will not be relevant since $INTV_{CC_{23}}$ is connected to $SV_{IN_{23}}$. See Input Voltage and Limits to update low $V_{IN}$ operation parameters.

$V_{OSNS2^-}$ (R8): Channel 2 Negative Differential Voltage Sense Input. See $V_{OSNS2^+}$.

$I_{IN_{23}^+}$ (R9): Positive Current Sense Amplifier Input. If the input current sense amplifier is not used, this pin must be shorted to the $I_{IN_{23}^-}$ and $SV_{IN_{23}}$ pins. See the Applications Information section for more details about the input current sensing.
PIN FUNCTIONS

$V_{OSNS3^+} (R11)$: Channel 3 Positive Differential Voltage Sense Input. Together, $V_{OSNS3^+}$ and $V_{OSNS3^-}$ serve to Kelvin-sense the $V_{OUT3}$ output voltage at $V_{OUT3}$’s point-of-load (POL) and provide the differential feedback signal directly to Channel 3’s feedback loop. Command $V_{OUT3}$’s target regulation voltage by serial bus. Its initial command value at $SV_{IN_23}$ power-up is dictated by NVM contents (factory default: 0.5V)—or, optionally, may be set by configuration resistors; see $VOUT3_{CFG}$, $VTRI3_{CFG}$ and the Applications Information section.

$V_{OSNS3^-} (T11)$: Channel 3 Negative Differential Voltage Sense Input. See $V_{OSNS3^+}$.

$SW3$ ($V1-V2$, $W1-W2$, $Y1-Y2$): Switching Node of Channel 3 Step-Down Converter Stage. Used for test purposes or EMI-snubbing. It may be routed a short distance to a local test point to monitor the switching action of Channel 3, if desired, but do not route near any sensitive signals. Otherwise, leave it open.

$V_{OUT3}$ ($V13-V15$, $W13-W15$, $Y13-Y15$, $AA13-AA15$, $AB13-AB15$): Channel 3 Output Voltage. Place recommended output capacitors from this output copper shape to GND. See the Layout Checklist/Example section.

$RUN2$, $RUN3$ ($Y9$, $Y8$): Enable Run Input for Channels 2 and 3, respectively. Open-drain input and output. The logic high on these pins enables the respective outputs of the LTM4683. These open-drain output pins hold the pin low until the LTM4683 is out of reset and $SV_{IN_23}$ is detected to exceed $V_{IN_{ON}}$. A pull-up resistor to 3.3V is required in the application. The LTM4683 pulls RUN2 and/or RUN3 low, as appropriate, when a global fault and/or channel-specific fault occurs whose fault response is configured to latch off and cease regulation, issuing a CLEAR_FAULTS command via $I^2C$ or power-cycling $SV_{IN_23}$ is necessary to restart the module, in such cases. Do not pull RUN logic high with a low impedance source. $INTV_{CC}$ is active when $SVIN_{23}$ is above UVLO. This provides power to the $V_{DD33}$ and $V_{DD25}$ to allow the programming of the EEPROM.

$V_{DD33_{23}} (Y10)$: Internally Generated 3.3V Power Supply Output Pin for Channel 2 and Channel 3 Circuits. This pin should only be used to provide external current for the pull-up resistors required for $FAULT_n$, $SHARE_CLK_{nn}$, and $SYNC_{nn}$, and may be used to provide external current for pull-up resistors on $RUN_n$, $SDA_{nn}$, $SCL_{nn}$, $ALERT_{nn}$ and $PGOOD_n$. Where $nn$ is either 0, 1 or 2, 3 channels, and $n$ is the actual channel. No external decoupling is required. $V_{DD33_{23}}$ can be powered from $V_{BIAS}$, so this controller 2 can be programmed with $RUN_n$ low.
Figure 2. Simplified LTM4683 Block Diagram of the 1/2 Function

**Decoupling Requirements**

\[ T_A = 25^\circ \text{C. Using Figure 2 configuration.} \]

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{\text{INH}} )</td>
<td>External High-Frequency Input Capacitor Requirement (5.75V ≤ ( V_{\text{IN}} ) ≤ 14V, ( V_{\text{OUT}} ) Commanded to 0.5V)</td>
<td>( I_{\text{OUT}} = 31.25A )</td>
<td>100</td>
<td>100</td>
<td>( \mu \text{F} )</td>
<td>( \mu \text{F} )</td>
</tr>
<tr>
<td>( C_{\text{OUTH}} )</td>
<td>External High-Frequency Output Capacitor Requirement (5.75V ≤ ( V_{\text{IN}} ) ≤ 14V, ( V_{\text{OUT}} ) Commanded to 0.5V)</td>
<td>( I_{\text{OUT}} = 31.25A )</td>
<td>800</td>
<td>800</td>
<td>( \mu \text{F} )</td>
<td>( \mu \text{F} )</td>
</tr>
</tbody>
</table>
Figure 3. Functional LTM4683 Block Diagram
Test Circuit 1.
Test Circuit 2.
OPERATION

POWER MODULE INTRODUCTION

The LT4683 is a highly configurable quad 31.25A output standalone nonisolated switching mode step-down DC/DC power supply with built-in EEPROM NVM with ECC and I²C-based PMBus/ SMBus 2-wire serial communication interface capable of 400kHz SCL bus speed. Four output voltages can be regulated (V\textsubscript{OUT0}, V\textsubscript{OUT1}, V\textsubscript{OUT2}, V\textsubscript{OUT3}) with a few external input and output capacitors and pull-up resistors. Readback telemetry data of input and output voltages, input and output currents, and module temperatures are continually digitized cyclically by an integrated 16-bit ADC (analog-to-digital converter). Many fault thresholds and responses are customizable. Data can be autonomously saved to EEPROM when a fault occurs, and the resulting fault log can be retrieved over I²C later, for analysis. See Figure 2 and Figure 3 for Block Diagrams. One controller for Channels 0 and 1, 2nd for controller Channels 2 and 3.

POWER MODULE MAJOR FEATURES OVERVIEW

Major Features Include:

- Dedicated Power Good Indicators
- Direct Input and Chip Current Sensing
- Programmable Loop Compensation Parameters
- T\textsubscript{INIT} Start-Up Time: 30ms
- PWM Synchronization Circuit (See theSwitching Frequency and Phase Section)
- MFR_ADC\_CONTROL for Fast ADC Sampling of One Parameter (as Fast as 8ms) (See the PMBus Command Details Section)
- Fully Differential Output Sensing for All Four Channels; V\textsubscript{OUT0}/V\textsubscript{OUT1}/V\textsubscript{OUT2}/V\textsubscript{OUT3} All Programmable Up to 0.8V
- Power-Up and Program EEPROM with V\textsubscript{BIAS}
- Input Voltage Up to 14V
- ΔV\textsubscript{BE} Temperature Sensing
- SYNC Contention Circuit (See the Switching Frequency and Phase Section for Details)
- Fault Logging
- Programmable Output Voltage
- Programmable Input Voltage On/Off Threshold Voltage
- Programmable Current Limit
- Programmable Switching Frequency
- Programmable OV/UV Threshold Voltage
- Programmable ON/Off Delay Times
- Programmable Output Rise/Fall Times
- Phase-Locked Loop for Synchronous PolyPhase Operation (2, 3, 4 or 6 Phases)
- Nonvolatile Configuration Memory with ECC
- Optional External Configuration Resistors for Key Operating Parameters
- Optional Time Base Interconnect for Synchronization Between Multiple Controllers
- WP Pin to Protect Internal Configuration
- Standalone Operation After User Factory Configuration
- PMBus, Version 1.2, 400kHz-Compliant Interface

The PMBus interface provides access to important power management data during system operation, including:

- Internal Controller Temperature
- Internal Power Channel Temperature
- Average Output Current
- Average Output Voltage
- Average Input Voltage
- Average Input Current
- Average Chip Input Current from V\textsubscript{IN}
- Configurable, Latched and Unlatched Individual Fault and Warning Status

Individual channels are accessed through the PMBus using the PAGE command, i.e., PAGE 0 or 1.
Fault reporting and shutdown behavior are fully configurable. Four individual FAULT0, FAULT1, FAULT2, and FAULT3, outputs are provided. Each FAULTn can be masked independently.

Six dedicated pins for ALERT_01, ALERT_23, PGOOD0, PGOOD1, PGOOD2, and PGOOD3 functions are provided. The shutdown operation also allows all faults to be individually masked and can be operated in either unlatched (hiccup) or latched modes.

Individual status commands enable fault reporting over the serial bus to identify the specific fault event. Fault or warning detection includes the following:

- Output Undervoltage/Overvoltage
- Input Undervoltage/Overvoltage
- Input and Output Overcurrent
- Internal Overtemperature
- Communication, Memory or Logic (CML) Fault

**EEPROM WITH ECC**

The LTM4683 contains internal EEPROM with error correction coding (ECC) to store user configuration settings and fault log information for Channels 0 and 1 and Channels 2 and 3. EEPROM endurance retention and mass write operation time are specified in the Electrical Characteristics and Absolute Maximum Ratings sections. Write operations above TJ = 85°C are possible, although the Electrical Characteristics are not guaranteed, and the EEPROM will be degraded. Read operations performed at temperatures between -40°C and 125°C will not degrade the EEPROM. Writing to the EEPROM above 85°C will result in degrading retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 85°C, the slight degradation in the data retention characteristics of the fault log will not take away from the usefulness of the function.

It is recommended that the EEPROM not to be written when the die temperature is greater than 85°C. If the die temperature exceeds 130°C, the LTM4683 will disable all EEPROM write operations. All EEPROM write operations will be re-enabled when the die temperature drops below 125°C. (The controller will also disable all the switching when the die temperature exceeds the internal overtemperature fault limit of 160°C with a 10°C hysteresis).

The degradation in EEPROM retention for temperatures >125°C can be approximated by calculating the dimensionless acceleration factor using Equation 1.

\[
AF = e^{\left(\frac{E_a}{k}\left(\frac{1}{T_{USE} + 273} - \frac{1}{T_{STRESS} + 273}\right)\right)}
\]

where:

- AF = acceleration factor
- \(E_a\) = activation energy = 1.4eV
- \(k = 8.617 \times 10^{-5}\) eV/K
- \(T_{USE} = 125°C\) specified junction temperature
- \(T_{STRESS} = \) actual junction temperature in °C

Example: Calculate the effect on retention when operating at a junction temperature of 130°C for 10 hours.

\[
T_{STRESS} = 130°C
\]
\[
T_{USE} = 125°C
\]

\[
AF = e^{\left(\frac{1.4}{8.617 \times 10^{-5}} \cdot \left(\frac{1}{130} - \frac{1}{125}\right)\right)} = 1.66
\]

The equivalent operating time at 125°C = 16.6 hours.

Thus, the overall retention of the EEPROM was degraded by 6.6 hours as a result of operating at a junction temperature of 130°C for 10 hours. The effect of the overstress is negligible when compared to the overall EEPROM retention rating of 87,600 hours at a maximum junction temperature of 125°C.

The integrity of the entire onboard EEPROM is checked with a CRC calculation each time its data is to be read, such as after a power-on reset or execution of a RESTORE_USER_ALL command. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the EEPROM CRC Error bit in the STATUS_MFR_SPECIFIC command is set, and the ALERT and RUN pins pulled low (PWM channels off). At that point, the device will only respond at a special address 0x7C, which is activated
OPERATION

only after an invalid CRC has been detected. The chip will also respond at the global addresses 0x5A and 0x5B, but using these addresses when attempting to recover from a CRC issue is not recommended. All power supply rails associated with either PWM channel of a device reporting an invalid CRC should remain disabled until the issue is resolved. See the Applications Information section or contact the factory for details on efficient in-system EEPROM programming, including bulk EEPROM programming, which the LTM4683 also supports.

The LTM4683 contains two dual internal constant frequency current mode control buck regulators (Channels 0 and 1 and Channels 2 and 3) whose power MOSFETs are capable of fast switching speed. Reference to the signal pins will be Name\_nn, where n is either 01 or 23, or with Namen when referring to signal pins that are related to the actual channel. The factory NVM-default switching frequency clocks SYNC\_nn at 425kHz, to which the regulators synchronize their switching frequency. The default phase-interleaving angle between the channels is 180°. A pin-strapping resistor on FSWPH\_nn\_CFG configures the frequency of the SYNC\_nn clock (switching frequency) and the channel phase relationship of the channels to each other and for the falling edge of the SYNC\_nn signal. (Most possible combinations of switching frequency and phase-angle assignments are settleable by resistor pin programming; see Table 3. Configure the LTM4683’s NVM to implement settings not available by resistor-pin strapping.) When an FSWPH\_nn\_CFG pin-strap resistor sets the channel phase relationship of the LTM4683’s channels, the SYNC\_nn clock is not driven by the module; instead, SYNC\_nn becomes strictly a high-impedance input, and the channel switching frequency is then synchronized to SYNC\_nn provided by an externally-generated clock or sibling LTM4683 with a pull-up resistor to VDD33\_nn. The switching frequency and the phase relationship can be altered via the I\(^2\)C interface, but only when the switching action is off, i.e., when the module is not regulating the outputs. See the Applications Information section for details.

Programmable analog feedback loop compensation for Channel 0 to Channel 3 is accomplished with a capacitor connection from COMPn\_a to SGND and a capacitor from COMPn\_b to SGND.) The COMPn\_b pin is for the high-frequency gain roll-off and is the g\textsubscript{m} amplifier output that has a programmable range, and the COMPn\_a pin has the programmable resistor range along with a capacitor to SGND that sets the frequency compensation. See the Programmable Loop Compensation section. The LTM4683 module has sufficient stability margins and good transient performance with a wide range of output capacitors—even all-ceramic MLCCs. Table 13 provides guidance on input and output capacitors recommended for many common operating conditions, along with the programmable compensation settings. The Analog Devices LTpowerCAD® tool is available for transient and stability analysis, and experienced users who prefer to adjust the module’s feedback loop compensation parameters can use this tool.

POWER-UP AND INITIALIZATION

The LTM4683 is designed to provide standalone supply sequencing and controlled turn-on and turn-off operation. It operates from a single input supply (4.5V to 14V) while three on-chip linear regulators generate internal 2.5V, 3.3V, and 5.5V per controller. If V\textsubscript{IN\_nn} does not exceed 5.75V, and the V\textsubscript{BIAS} pin is turned off, the INTV\_CC, V\textsubscript{IN\_nn}, and SV\textsubscript{IN\_nn} pins must be connected together. The controller configuration is initialized by an internal threshold-based UVLO where V\textsubscript{IN\_nn} must be approximately 4V, and the 5.5V, 3.3V, and 2.5V linear regulators must be within approximately 20% of the regulated values. In addition to the power supply, a PMBus RESTORE\_USER\_ALL or MFR\_RESET command can initialize the part too.

The V\textsubscript{BIAS} pin is the output of an internal 5.5V buck regulator to improve the efficiency of the circuit and minimize power loss on the LTM4683. The V\textsubscript{BIAS} pin must exceed approximately 4.8V, and the V\textsubscript{IN} must exceed 7V before the INTV\_CC LDO operates from the V\textsubscript{BIAS} pin. The V\textsubscript{BIAS} regulator is powered from V\textsubscript{IN\_VBIAS} and enabled with RUNP.

During initialization, the external configuration resistors are identified and/or contents of the NVM are read into the controller’s commands, and the power train is held off. The RUN\_nn and FAULT\_nn, and PGOOD\_nn are held low. The LTM4683 will use the contents of Table 1—Table 5 to determine the resistor-defined parameters. See the R\textsubscript{CON}\_FF (Resistor
### OPERATION

Configuration) Pins section for more details. The resistor configuration pins only control some of the preset values of the controller. The remaining values are programmed in NVM either at the factory or by the user.

If the configuration resistors are not inserted or if the ignore RCONFIG bit is asserted (bit 6 of the MFR_CONFIG_ALL configuration command), the LTM4683 will use only the contents of NVM to determine the DC/DC characteristics. The ASEL_nn value read at power-up or reset is always respected unless the pin is open. The ASEL_nn will set the bottom 4LSBs, and the MSBs are set by NVM. See the Applications Information section for more details.

After the part has initialized, an additional comparator monitors VIN through the SVIN_nn pins. The VIN_ON threshold must be exceeded before the output power sequencing can begin. After VIN is initially applied, the part will typically require 30ms to initialize and begin the TON_DELAY timer. The readback of voltages and currents may require an additional 0ms to 90ms.

### SOFT-START

The method of start-up sequencing described below is time-based. The part must enter the run state before soft-start. The run pins are released by the LTM4683 after the part is initialized, and SVIN_nn is greater than the VIN_ON threshold. If multiple LTM4683s are used in an application, they all hold their respective run pins low until all devices are initialized, and SVIN_nn exceeds the VIN_ON threshold for every device. The SHARE_CLK_nn pin assures all the devices connected to the signal use the same time base. The SHARE_CLK_nn pin is held low until the part has been initialized after VIN is applied. The LTM4683 can be set to turn-off (or remain off) if SHARE_CLK_nn is low (set bit 2 of MFR_CHAN_CONFIG to 1). This allows the user to ensure synchronization across numerous Analog Devices ICs, even if the RUNn pins cannot be connected together due to board constraints. In general, if the user cares about synchronization between chips, it is best not only to connect all the respective RUNn pins together but also to connect all the respective SHARE_CLK_nn pins together and pulled up to VDD33_nn with a 10k resistor. This assures that all chips begin sequencing simultaneously and use the same time base.

After the RUNn pins release and before entering a constant output voltage regulation state, the LTM4683 performs a monotonic initial ramp or “soft-start”. Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set-point. Once the LTM4683 is commanded to turn on (after power up and initialization), the controller waits for the user-specified turn-on delay (TON_DELAY) before initiating this output voltage ramp. The rise time of the voltage ramp can be programmed using the TON_RISE command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting the value of TON_RISE to any value less than 0.25ms. The LTM4683 PWM always uses discontinuous mode during the TON_RISE operation. In discontinuous mode, the bottom MOSFET is turned off as soon as reverse current is detected in the inductor. This will allow the regulator to start up into a pre-biased load. When the TON_MAX_FAULT_LIMIT is reached, the part transitions to continuous mode, if so programmed. If TON_MAX_FAULT_LIMIT is set to zero, there is no time limit, and the part transitions to the desired conduction mode after TON_RISE completes and VOUTn has exceeded the VOUT_UV_FAULT_LIMIT and IOUT_OC is not present. However, setting TON_MAX_FAULT_LIMIT to a value of 0 is not recommended.

### TIME-BASED SEQUENCING

The default mode for sequencing the outputs on and off is time-based. Each output is enabled after waiting a TON_DELAY amount of time following either a RUN pin going high, a PMBus command to turn on or the VIN rising above a preprogrammed voltage. Off-sequencing is handled similarly. To ensure proper sequencing, ensure all ICs connect the SHARE_CLK_nn pin together and RUNn pins together. If the RUNn pins cannot be connected together for some reasons, set bit 2 of MFR_CHAN_CONFIG to 1. This bit requires the SHARE_CLK_nn pin to be clocking before the power supply output can start. When the RUNn pin is pulled low, the LTM4683 will hold the pin low for the MFR_RESTART_DELAY. The minimum MFR_RESTART_DELAY is TOFF_DELAY + TOFF_FALL + 136ms. This delay assures proper sequencing of all rails. The LTM4683 calculates this delay internally and will not process a shorter delay.
**OPERATION**

However, a longer commanded MFR_RESTART_DELAY can be used by the part. The maximum allowed value is 65.52 seconds.

**VOLTAGE-BASED SEQUENCING**

The sequence can also be voltage-based. As shown in Figure 4, The PGOODn pin is asserted when the UV threshold is exceeded for each output. It is possible to feed the PGOODn pin from one LTM4683 channel into the RUNn pin of the next LTM4683 channel in the sequence, especially across multiple LTM4683s. The PGOODn has a 100µs filter. If the VOUTn voltage bounces around the UV threshold for a long period of time, it is possible for the PGOODn output to toggle more than once. To minimize this problem, set the TON_RISE time under 100ms.

If a fault in the string of rails is detected, only the faulted rail and downstream rails will fault off. The rails in the string of devices in front of the faulted rail will remain on unless commanded off.

![Light-Load Current Operation Diagram](image)

**SHUTDOWN**

The LTM4683 supports two shutdown modes. The first mode is a closed-loop shutdown response with a user-defined turn-off delay (TOFF_DELAY) and ramp-down rate (TOFF_FALL). The controller will maintain the mode of operation for TOFF_FALL. The second mode is discontinuous conduction mode, the controller will not draw current from the load, and the fall time will be set by the output capacitance, and load current, instead of TOFF_FALL.

The shutdown occurs in response to a fault condition or loss of SHARE_CLK_nn (if bit 2 of MFR_CHAN_CONFIG is set to a 1), or VINn falling below the VIN_OFF threshold or FAULT pulled low externally (if the MFR_FAULT_RESPONSE is set to inhibit). Under these conditions, the power stage is disabled in order to stop the transfer of energy to the load as quickly as possible. The shutdown state can be entered from the soft-start or active regulation states or through user intervention.

There are two ways to respond to faults, retry mode and latched-off mode. In retry mode, the controller responds to a fault by shutting down and entering the in-active state for a programmable delay time (MFR_RETRY_DELAY). This delay minimizes the duty cycle associated with autonomous retries if the fault that causes the shutdown disappears once the output is disabled. The retry delay time is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. If multiple outputs are controlled by the same FAULTn pin, the decay time of the faulted output determines the retry delay. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG. Alternatively, latched-off mode means the controller remains latched-off following a fault, and clearing requires user intervention, such as toggling RUNn or commanding the part OFF and then ON.

**LIGHT-LOAD CURRENT OPERATION**

The LTM4683 has two modes of operation: high-efficiency discontinuous-conduction mode or forced continuous conduction mode. Mode selection is done using the MFR_PWM_MODE command (discontinuous-conduction is always the start-up mode, and forced continuous is the default running mode).

If a controller is enabled for discontinuous operation, the inductor current is not allowed to reverse. The reverse current comparator’s output turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative.
OPERATION

In forced continuous mode operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined solely by the voltage on the COMPn pins. In this mode, the efficiency at light loads is lower than in discontinuous mode operation. However, continuous mode exhibits lower output ripple and less interference with audio circuitry but may result in reverse inductor current, which can cause the input supply to boost. The VIN_OV_FAULT_LIMIT can detect this and turn off the offending channel. However, this fault is based on an ADC read and can take up to t_CONVERT to detect. If there is concern about the input supply boosting, keep the part in discontinuous conduction mode.

If the part is set to discontinuous mode operation, as the inductor average current increases, the controller will automatically modify the operation from discontinuous mode to continuous mode.

SWITCHING FREQUENCY AND PHASE

The switching frequency of the PWM can be established with an internal oscillator or an external time base. The internal phase-locked loop (PLL) synchronizes the PWM control to this timing reference with proper phase relation, whether the clock is provided internally or externally. The device can also be configured to provide the main clock to other devices through the PMBus command, NVM setting, or external configuration resistors, as outlined in Table 3.

As a main clock, the LTM4683 will drive its open-drain SYNC_nn pin at the selected rate with a pulse width of 500ns. An external pull-up resistor between SYNC_nn and VDD3_nn is required in this case. Only one device connected to SYNC_nn should be designated to drive the pin. The LTM4683 will automatically revert to an external SYNC_nn input, disabling its own SYNC_nn, as long as the external SYNC_nn frequency is greater than 80% of the programmed SYNC_nn frequency. The external SYNC input shall have a duty cycle between 20% and 80%.

Whether configured to drive SYNC_nn or not, the LTM4683 can continue PWM operation using its own internal oscillator if an external clock signal is subsequently lost.

The device can also be programmed to always require an external oscillator for PWM operation by setting bit 4 of MFR_CONFIG_ALL. The status of the SYNC driver circuit is indicated by bit 10 of MFR_PADS.

The MFR_PWM_CONFIG command can be used to configure the phase of each channel. The desired phase can also be set from EEPROM or external configuration resistors, as outlined in Table 3. The designated phase is the relationship between the falling edge of SYNC and the internal clock edge that sets the PWM latch to turn on the top power switch. Additional small propagation delays to the PWM control pins will also apply. Both channels must be off before the FREQUENCY_SWITCH and MFR_PWM_CONFIG commands can be written to the LTM4683.

The phase relationships and frequency options provide for numerous application options. Multiple LTM4683 modules can be synchronized to realize a PolyPhase array. In this case, the phases should be separated by 360/n degrees, where n is the number of phases driving the output voltage rail.

PWM LOOP COMPENSATION

The internal PWM loop compensation resistors R_COMP of the LTM4683 can be adjusted using bit[4:0] of the MFR_PWM_CONFIG command for each controller.

The transconductance (gm) of the LTM4683 PWM error amplifier can be adjusted using bit[7:5] of the MFR_PWM_CONFIG command. These two loop compensation parameters can be programmed when the device is in operation. See the Programmable Loop Compensation subsection in the Applications Information section for further details.

OUTPUT VOLTAGE SENSING

All four channels in LTM4683 have differential amplifiers, which allow the remote sensing of the load voltage between V+ and V− pins. The telemetry ADC is also fully differential and makes measurements between VO_SNS+n and VO_SNS–n voltages for both channels at the V+ and V− pins, respectively. The maximum allowed is 1V, but the LTM4683 design is limited to 0.7V.

For more information www.analog.com
**OPERATION**

**INTVCC/VBIAS POWER**

Power for the internal top and bottom MOSFET drivers and most other internal circuitry is derived from the INTVCC pin. When the RUNP pin is shorted to GND and the VBIAS is off, an internal 5.5V linear regulator INTVCC supplies power from SVIN. When enabling VBIAS at 5.5V output and SVIN exceeds 7.0V, an internal switch is turned on to source power from VBIAS instead of the INTVCC regulator. Using the VBIAS allows the INTVCC power to be derived from a high-efficiency internal source. VBIAS can provide power to the internal 3.3V linear regulators when SVIN is present, which allows the LTM4683 controllers to be initialized and programmed, even with channels off.

The INTVCC pin regulator is powered from the SVIN pin; the power through the IC is equal to SVIN - INTVCC. The gate charge current is dependent on the operating frequency. The typical INTVCC current for the LTM4683 is ~50mA. A 12V input voltage would equate to a difference of 7V per controller drop across the internal controller, when multiplied by 50mA, equals a 350mW power loss. This loss can be eliminated by utilizing the VBIAS regulator.

Do not connect INTVCC on the LTM4683 to an external supply because INTVCC will attempt to pull the external supply high and hit the current limit, significantly increasing the die temperature.

For applications where VIN is 5V, tie the SVIN and INTVCC pins together to the 5V input through a 1Ω resistor, as shown in Test Circuit 2.

**OUTPUT CURRENT SENSING AND SUB MILLIOHM DCR CURRENT SENSING**

The LTM4683 uses a unique sub-milliohm inductor current-sensing technique that provides a high-level signal-to-noise ratio while sensing very low signals in current mode operation. This enables higher conversion efficiencies using the internal sub-milliohm inductors in heavy load applications. The current limit threshold can be accurately set with the MFR_PWM_MODE[7] for the High and Low range (see the IOUT_OC_FAULT_LIMIT in the PMBus Command Details section for the high and the low details.

The internal direct current resistance (DCR) sensing network, thus the current limit, is calculated based on the DCR of the inductor at room temperature. The DCR of the inductor has a large temperature coefficient, approximately 3900ppm/°C. The temperature coefficient of the inductor is written to the MFR_IOUT_CAL_GAIN_TC register. The external temperature is sensed near the inductor and used to modify the internal current limit circuit to maintain an essentially constant current limit with temperature. The current sensed is then digitized by the LTM4683’s telemetry ADC with an input range of ±128mV, a noise floor of 7µVRMS, and a peak-peak noise of approximately 46.5µV. The LTM4683 computes the inductor current using the DCR value stored in the IOUT_CAL_GAIN command and the temperature coefficient stored in the command MFR_IOUT_CAL_GAIN_TC. The resulting current value is returned by the READ_IOUT command.

**INPUT CURRENT SENSING**

To sense the total input current consumed by the LTM4683’s power stages, a sense resistor is placed between the supply voltage and the drain of the top N-channel MOSFET. The IIN33+ and IIN33− pins are connected to the sense resistor. The filtered voltage is amplified by the internal high-side current sense amplifier and digitized by the LTM4683’s telemetry ADC. The input current sense amplifier has three gain settings of 2x, 4x, and 8x set by the bit [6:5] of the MFR_PWM_CONFIG command. The maximum input sense voltage for the three gain settings is 50mV, 25mV, and 10mV, respectively. The LTM4683 computes the input current using the internal RSENSE value stored in the IIN33_CAL_GAIN command. The resulting measured power stage current is returned by the READ_IIN command. IIN01+, IIN01− for controller 1 (Channels 0 and 1), and IIN23+, IIN23− for controller 2 (Channels 2 and 3).

The LTM4683 uses a 1Ω resistor to measure the SVIN pin supply current being consumed by each LTM4683 internal controller. This value is returned by the MFR_READ_ICHIP command. The chip current is calculated by using the 1Ω value stored in the MFR_ICHIP_CAL_GAIN command. See the Input Current Sense Amplifier subsection in the Applications Information section for further details.
OPERATION

PolyPhase LOAD SHARING
Multiple LTM4683s can be arrayed to provide a balanced load-share solution by bussing the necessary pins. Figure 50 illustrates an 8-phase design sharing connection required for load sharing.

If an external oscillator is not provided, the SYNC_\(nn\) pins should only be enabled on one of the LTM4683s controllers. The other(s) should be programmed to disable SYNC_\(nn\) controllers using bit 4 of MFR_CONFIG_ALL. If an external oscillator is present, the chip with the SYNC\(nn\) pin enabled will detect the presence of the external clock and disable its output.

Multiple channels need to tie all the \(V_{OSNSn}\) pins together and all the \(V_{OSNSn^-}\) pins together, \(\text{COMP}_{Rn}\) and \(\text{COMP}_{Pn}\) pins together as well. Do not assert bit[4] of MFR_CONFIG_ALL except in a PolyPhase® application.

The user must share the SYNC_\(nn\), SHARE_CLK_\(nn\), FAULT\(nn\), and ALERT\(nn\) pins of these parts. Use pull-up resistors on SYNC_\(nn\), FAULT\(nn\), SHARE_CLK_\(nn\), and ALERT\(nn\). See the Typical Applications figures.

INTERNAL TEMPERATURE SENSE
Temperature is measured using the internal diode-connected PNP transistors, and the outputs are connected to TSNS0 to TSNS3 pins corresponding to Channels 0 to 3. These outputs are used for testing. Two different currents are applied to the diode (nominally \(2\mu\text{A}\) and \(32\mu\text{A}\)), and the temperature is calculated from a \(\Delta V_{BE}\) measurement made with the internal 16-bit monitor ADC (see Figure 2 Simplified Block Diagram).

The LTM4683 will only implement \(\Delta V_{BE}\) temperature sensing; therefore MFR_PWM_MODE bit [5] is reserved.

\(\text{R}_{\text{CONFIG}}\) (RESISTOR CONFIGURATION) PINS
There are twelve input pins utilizing 1% resistors between these pins to select key operating parameters. The pins are ASEL_01, ASEL_23, FSWPH_01_CFG, FSWPH_23_CFG, VOUT0_CFG, VOUT1_CFG, VOUT2_CFG, VOUT3_CFG, VTRIM0_CFG, VTRIM1_CFG, VTRIM2_CFG, and VTRIM3_CFG. If pins are floated, the value stored in the corresponding NVM command is used. If bit 6 of the MFR_CONFIG_ALL configuration command is asserted in NVM, the resistor input is ignored upon power-up except for ASEL, which is always respected. The resistor configuration pins are only measured during a power-up reset or, after a MFR_RESET, or after a RESTORE_USER_ALL command is executed.

The VOUT\(_n\)_CFG pin settings are described in Table 1. These pins set the LTM4683 VOUT0 to VOUT3 output voltage coarse settings. If the pin is open, the VOUT_COMMAND command is loaded from NVM to determine the output voltage. The default setting is to have the switcher off unless the voltage configuration pins are installed. The VTRIM\(_n\)_CFG pins in Table 2 are used to set the output voltage fine adjustment setting. Both combine to offer several distinct output voltages.

The following parameters are set as a percentage of the output voltage if the \(\text{R}_{\text{CONFIG}}\) pins are used to determine the output voltage.

- \(\text{VOUT}_0\text{V_FAULT_LIMIT}\)..............................\(+10\%\)
- \(\text{VOUT}_0\text{V_WARN_LIMIT}\)..............................\(+7.5\%\)
- \(\text{VOUT}\_MAX\)........................................\(+7.5\%\)
- \(\text{VOUT}\_MARGIN\_HIGH\)..............................\(+5\%\)
- \(\text{VOUT}\_MARGIN\_LOW\)..............................\(-5\%\)
- \(\text{VOUT}\_UV\_FAULT\_LIMIT\).........................\(-7\%\)

The FSWPH_CFG_\(nn\) pin settings are described in Table 3. This pin selects the switching frequency and phase of each channel. The phase relationships between the two channels and the SYNC_\(nn\) pin are determined in Table 3. To synchronize to an external clock, the part should be put into external clock mode (SYNC_\(nn\) output disabled, but frequency set to the nominal value). If no external clock is supplied, the part will clock at the programmed frequency. If the application is multiphase and the SYNC_\(nn\) signal between chips is lost, the parts will not operate at the designed phase, even if they are programmed and trimmed to the same frequency. This can increase the ripple voltage on the output, possibly producing undesirable operation. If the external SYNC_\(nn\) signal is being generated internally and external SYNC_\(nn\) is not selected, bit 10 of MFR_PADS will be asserted. If no frequency is selected and the external SYNC_\(nn\) frequency is not present, a PLL_FAULT
will occur. If the user does not wish to see the ALERT from a PLL_FAULT, even if there is a valid synchronization signal at power-up, the ALERT mask for PLL_FAULT must be written. See the description on SMBALERT_MASK for more details. If the SYNC_{nn} pin is connected between multiple ICs, only one of the ICs should have the SYNC_{nn} pin enabled using the MFR_CONFIG_ALL[4] = 0, and all other ICs should be configured to have the SYNC pin disabled with MFR_CONFIG_ALL[4] = 1.

The ASEL_{nn} pin settings are described in Table 4. ASEL_{nn} selects the subordinate address for the LTM4683 internal controller. For more details, see Table 5.

NOTE: Per the PMBus specification, pin-programmed parameters can be overridden by commands from the digital interface, with the exception of ASEL_{nn}, which is always honored. Do not set any part address to 0x5A or 0x5B because these are global addresses, and all parts will respond to them.

Table 1. VOUT_{nn} CFG Pin Strapping Look-Up Table for the LTM4683’s Output Voltage, Coarse Setting (Not Applicable if MFR_CONFIG_ALL[6] = 1b) Top Resistor = 14.3k

<table>
<thead>
<tr>
<th>R_{VOUT_{nn} CFG} (kΩ)</th>
<th>V_{OUT_{nn}} (V)</th>
<th>MFR_PWM_MODE/11 BIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open</td>
<td>NVM</td>
<td>NVM</td>
</tr>
<tr>
<td>32.4</td>
<td>NVM</td>
<td>NVM</td>
</tr>
<tr>
<td>0.787</td>
<td>0.7</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0.5</td>
<td>1</td>
</tr>
</tbody>
</table>

*V_{VOUT_{nn} CFG} value indicated is nominal. Select R_{VOUT_{nn} CFG} from a resistor vendor such that its value is always within 3% of the value indicated in the table. Consider resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity), and other effects (depending on one’s specific application) could also affect R_{VOUT_{nn} CFG}’s value over time. All such effects must be considered in order for resistor pin strapping to yield the expected result at every SVIN_{nn} power-up and/or every execution of MFR_RESET or RESTORE_USER_ALL over the lifetime of one’s product. R_{TOP} = 14.3k is external to the part. Example:

\[ \text{V}_{\text{DD25}_{nn}} \]
\[ \text{R}_{\text{TOP}} \]
\[ \text{V}_{\text{OUT}_{nn} \_CFG} \]
\[ \text{R}_{\text{VOUT}_{nn} \_CFG} \]
\[ \text{SIN}_{\text{D} \_nn} \]

Table 2. VTRIM_{nn} CFG Pin Strapping Look-Up Table for the LTM4683’s Output Voltage, Fine Adjustment Setting (Not Applicable if MFR_CONFIG_ALL[6] = 1b) Top Resistor = 14.3k

<table>
<thead>
<tr>
<th>R_{VTRIM_{nn} CFG} (kΩ)</th>
<th>V_{TRIM} (mV) FINE ADJUSTMENT TO V_{OUT_{nn}} SETTING WHEN RESPECTIVE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open</td>
<td>0</td>
</tr>
<tr>
<td>32.4</td>
<td>99</td>
</tr>
<tr>
<td>22.6</td>
<td>86.625</td>
</tr>
<tr>
<td>18.0</td>
<td>74.25</td>
</tr>
<tr>
<td>15.4</td>
<td>61.875</td>
</tr>
<tr>
<td>12.7</td>
<td>49.5</td>
</tr>
<tr>
<td>10.7</td>
<td>37.125</td>
</tr>
<tr>
<td>9.09</td>
<td>24.75</td>
</tr>
<tr>
<td>7.68</td>
<td>12.375</td>
</tr>
<tr>
<td>6.34</td>
<td>–12.375</td>
</tr>
<tr>
<td>5.23</td>
<td>–24.75</td>
</tr>
<tr>
<td>4.22</td>
<td>–37.125</td>
</tr>
<tr>
<td>3.24</td>
<td>–49.5</td>
</tr>
<tr>
<td>2.43</td>
<td>–61.875</td>
</tr>
<tr>
<td>1.65</td>
<td>–74.25</td>
</tr>
<tr>
<td>0.787</td>
<td>–86.625</td>
</tr>
<tr>
<td>0</td>
<td>–99</td>
</tr>
</tbody>
</table>

*R_{VTRIM_{nn} CFG} value indicated is nominal. Select R_{VTRIM_{nn} CFG} from a resistor vendor such that its value is always within 3% of the value indicated in the table. Consider resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity), and other effects (depending on one’s specific application) could also affect R_{VTRIM_{nn} CFG}’s value over time. All such effects must be considered in order for resistor pin strapping to yield the expected result at every SVIN_{nn} power-up and/or every execution of MFR_RESET, or RESTORE_USER_ALL over the lifetime of one’s product. R_{TOP} = 14.3k is external to the part. Example:
### Table 3. FSWPH\_nn\_CFG Pin Strapping Look-Up Table to Set the LTM4683’s Switching Frequency and Channel Phase-Interleaving Angle (Not Applicable if MFR\_CONFIG\_ALL[6] = 1b), nn = 01 or 23 Channels, Set Top Resistor to 14.3k.

<table>
<thead>
<tr>
<th>$R_{FSWPH\text{_nn_CFG}}$ (kΩ)</th>
<th>SWITCHING FREQUENCY (kHz)</th>
<th>$θ$ SYNC TO $θ_{0,2}$</th>
<th>$θ$ SYNC TO $θ_{1,3}$</th>
<th>BITS [2:0] OF MFR_PWM_CONFIG</th>
<th>BIT [4] OF MFR_CONFIG_ALL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open</td>
<td>NVM; LTM4683 Default = 425</td>
<td>NVM; LTM4683 Default = 0°</td>
<td>NVM; LTM4683 Default = 180°</td>
<td>NVM; LTM4683 Default = 000b</td>
<td>NVM; LTM4683 Default = 0b</td>
</tr>
<tr>
<td>32.4</td>
<td>250</td>
<td>0°</td>
<td>180°</td>
<td>000b</td>
<td>0b</td>
</tr>
<tr>
<td>22.6</td>
<td>350</td>
<td>0°</td>
<td>180°</td>
<td>000b</td>
<td>0b</td>
</tr>
<tr>
<td>18.0</td>
<td>425</td>
<td>0°</td>
<td>180°</td>
<td>000b</td>
<td>0b</td>
</tr>
<tr>
<td>15.4</td>
<td>575</td>
<td>0°</td>
<td>180°</td>
<td>000b</td>
<td>0b</td>
</tr>
<tr>
<td>12.7</td>
<td>650</td>
<td>0°</td>
<td>180°</td>
<td>000b</td>
<td>0b</td>
</tr>
<tr>
<td>10.7</td>
<td>750</td>
<td>0°</td>
<td>180°</td>
<td>000b</td>
<td>0b</td>
</tr>
<tr>
<td>7.68</td>
<td>500</td>
<td>120°</td>
<td>240°</td>
<td>100b</td>
<td>0b</td>
</tr>
<tr>
<td>6.34</td>
<td>500</td>
<td>90°</td>
<td>270°</td>
<td>001b</td>
<td>0b</td>
</tr>
<tr>
<td>5.23</td>
<td>External**</td>
<td>0°</td>
<td>240°</td>
<td>010b</td>
<td>1b</td>
</tr>
<tr>
<td>4.22</td>
<td>External**</td>
<td>0°</td>
<td>120°</td>
<td>011b</td>
<td>1b</td>
</tr>
<tr>
<td>3.24</td>
<td>External**</td>
<td>60°</td>
<td>240°</td>
<td>101b</td>
<td>1b</td>
</tr>
<tr>
<td>2.43</td>
<td>External**</td>
<td>120°</td>
<td>300°</td>
<td>110b</td>
<td>1b</td>
</tr>
<tr>
<td>1.65</td>
<td>External**</td>
<td>90°</td>
<td>270°</td>
<td>001b</td>
<td>1b</td>
</tr>
<tr>
<td>0.787</td>
<td>External**</td>
<td>0°</td>
<td>180°</td>
<td>000b</td>
<td>1b</td>
</tr>
<tr>
<td>0</td>
<td>External**</td>
<td>120°</td>
<td>240°</td>
<td>100b</td>
<td>1b</td>
</tr>
</tbody>
</table>

* $R_{FSWPH\text{\_nn\_CFG}}$ value indicated is nominal. Select $R_{FSWPH\text{\_nn\_CFG}}$ from a resistor vendor such that its value is always within 3% of the value indicated in the table. Consider resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity) and other effects (depending on one’s specific application) could also affect $R_{FSWPH\text{\_nn\_CFG}}$’s value over time. All such effects must be considered in order for resistor pin-strapping to yield the expected result at every SVIN power-up and/or every execution of MFR\_RESET or RESTORE\_USER\_ALL, over the lifetime of one’s product.

**External setting corresponds to FREQUENCY\_SWITCH (Register 0x33) value set to 0x0000; the device synchronizes its switching frequency to that of the clock provided on the SYNC\_nn pin, provided MFR\_CONFIG\_ALL[4] = 1b. $R_{TOP}$ = 14.3k is external to the part.

Example:

![Diagram](image-url)
**OPERATION**

Table 4. ASEL \_nn Pin Strapping Look-Up Table to Set the LTM4683’s Subordinate Address (Applicable Regardless of MFR \_CONFIG \_ALL[6] Setting)

<table>
<thead>
<tr>
<th>( R_{\text{ASEL}} ) *(kΩ)</th>
<th>SUBORDINATE ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open</td>
<td>100_1111_R/W</td>
</tr>
<tr>
<td>32.4</td>
<td>100_1111_R/W</td>
</tr>
<tr>
<td>22.6</td>
<td>100_1110_R/W</td>
</tr>
<tr>
<td>18.0</td>
<td>100_1101_R/W</td>
</tr>
<tr>
<td>15.4</td>
<td>100_1100_R/W</td>
</tr>
<tr>
<td>12.7</td>
<td>100_1011_R/W</td>
</tr>
<tr>
<td>10.7</td>
<td>100_1010_R/W</td>
</tr>
<tr>
<td>9.09</td>
<td>100_1001_R/W</td>
</tr>
<tr>
<td>7.68</td>
<td>100_1000_R/W</td>
</tr>
<tr>
<td>6.34</td>
<td>100_0111_R/W</td>
</tr>
<tr>
<td>5.23</td>
<td>100_0110_R/W</td>
</tr>
<tr>
<td>4.22</td>
<td>100_0101_R/W</td>
</tr>
<tr>
<td>3.24</td>
<td>100_0100_R/W</td>
</tr>
<tr>
<td>2.43</td>
<td>100_0011_R/W</td>
</tr>
<tr>
<td>1.65</td>
<td>100_0010_R/W</td>
</tr>
<tr>
<td>0.787</td>
<td>100_0001_R/W</td>
</tr>
<tr>
<td>0</td>
<td>100_0000_R/W</td>
</tr>
</tbody>
</table>

Where:
- \( R/W \) = Read/Write bit in the control byte
- All PMBus device addresses listed in the specification are 7 bits wide unless otherwise noted.

NOTE: The LTM4683 will always respond to subordinate addresses 0x5A and 0x5B, regardless of the NVM or ASEL resistor configuration values.

*\( R_{\text{CFG}} \) value indicated is nominal. Select \( R_{\text{CFG}} \) from a resistor vendor such that its value is always within 3% of the value indicated in the table. Consider resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock cycling, moisture (humidity), and other effects (depending on one’s specific application) could also affect \( R_{\text{CFG}} \)’s value over time. All such effects must be considered in order for resistor pin-strapping to yield the expected result at every SV \_IN power-up and/ or every execution of MFR \_RESET or RESTORE \_USER \_ALL, over the lifetime of one’s product.

Example:

![ASEL \_nn PIN](image)

Table 5. LTM4683 MFR \_ADDRESS Command Examples Expressed in 7- and 8-Bit Addressing

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>HEX DEVICE ADDRESS</th>
<th>BIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>7-BIT</td>
<td>8-BIT</td>
</tr>
<tr>
<td>Rail (^4)</td>
<td>0x5A</td>
<td>0x84</td>
</tr>
<tr>
<td>Global (^4)</td>
<td>0x5B</td>
<td>0x86</td>
</tr>
<tr>
<td>Default</td>
<td>0x4F</td>
<td>0x9E</td>
</tr>
<tr>
<td>Example 1</td>
<td>0x40</td>
<td>0x80</td>
</tr>
<tr>
<td>Example 2</td>
<td>0x41</td>
<td>0x82</td>
</tr>
<tr>
<td>Disabled (^2) (^3)</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

1 This table can be applied to the MFR \_RAIL \_ADDRESS \_nn commands, but not the MFR \_ADDRESS command.

2 A disabled value in one command does not disable the device, nor does it disable the global address.

3 A disabled value in one command does not inhibit the device from responding to device addresses specified in other commands.

4 It is not recommended to write the value 0x00, 0x0C (7-bit), 0x5A (7-bit), 0x5B (7-bit), or 0x7C (7-bit) to the MFR \_CHANNEL \_ADDRESS \_nn or the MFR \_RAIL \_ADDRESS \_nn commands.

**FAULT DETECTION AND HANDLING**

A variety of fault and warning reporting and handling mechanisms are available, including the following fault and warning detection capabilities.

- Input OV Fault Protection and UV Warning
- Average Input Overcurrent Warn
- Output OV/UV Fault and Warn Protection
- Output OC Fault and Warn Protection
- Internal Control Die and Internal Module Overtemperature Fault and Warn Protection
- Internal Undertemperature Fault and Warn Protection
- CML Fault (Communication, Memory or Logic)
- External Fault Detection via the Bidirectional FAULT \_nn Pins

In addition, the LTM4683 can map any combination of fault indicators to their respective FAULT \_nn pin using the propagate FAULT \_nn response commands, MFR \_FAULT \_PROPAGATE. Typical usage of a FAULT \_nn pin is as a driver for an external crowbar device, overtemperature alert, overvoltage (OV) alert or as an interrupt to cause a
**OPERATION**

Microcontroller to poll the fault commands. Alternatively, the FAULT \( n \) pins can be used as inputs to detect external faults downstream of the controller that require an immediate response.

Any fault or warning event will always cause the ALERT \( nn \) pin to assert low unless the fault or warning is masked by the SMBALERT_MASK. The pin will remain asserted low until the CLEAR_FAULTS command is issued, the fault bit is written to a 1 or, bias power is cycled, or an MFR_RESET command is issued, or the RUN\( n \) pins are toggled Off/On, or the part is commanded Off/On via PMBus, or an alert response address (ARA) command operation is performed. The MFR_FAULT_PROPAGATE command determines if the FAULT \( n \) pins are pulled low when a fault is detected.

Output and input fault event handling is controlled by the corresponding fault response byte as specified in Table 17 ——Table 21. Shutdown recovery from these types of faults can either be autonomous or latched. For autonomous recovery, the faults are not latched, so if the fault conditions are not present after the retry interval has elapsed, a new soft-start is attempted.

If the fault persists, the controller will continue to retry. The retry interval is specified by the MFR_RETRY_DELAY command and prevents damage to the regulator components by repetitive power cycling, assuming the fault condition itself is not immediately destructive. The MFR_RETRY_DELAY must be greater than 120ms. It can not exceed 83.88 seconds.

**Status Registers and ALERT Masking**

Figure 5 summarizes the internal LTM4683 status registers accessible by the PMBus command. These contain indications of various faults, warnings and other important operating conditions. As shown, the STATUS_BYTE and STATUS_WORD commands also summarize the contents of other status registers. See the PMBus Command Details for specific information.

NONE OF THE ABOVE in the STATUS_BYTE indicates that one or more of the bits in the most significant nibble of STATUS_WORD are also set.

Generally, any asserted bit in a STATUS_x register also pulls the ALERT\( nn \) pin low. Once set, the ALERT\( nn \) pin will remain low until one of the following occurs.

- A CLEAR_FAULTS or MFR_RESET Command Is Issued
- The Related Status Bit Is Written to a One
- The Faulted Channel Is Properly Commanded Off and Back On
- The LTM4683 Successfully Transmits Its Address During a PMBus Alert Response Address (ARA)
- Bias Power Is Cycled

With some exceptions, the SMBALERT_MASK command can be used to prevent the LTM4683 from asserting ALERT\( nn \) for bits in these registers on a bit-by-bit basis. These mask settings are promoted to STATUS_WORD and STATUS_BYTE in the same fashion as the status bits themselves. For example, if ALERT\( nn \) is masked for all bits in Channel \( n \) STATUS_VOUT, then ALERT\( nn \) is effectively masked for the VOUT bit in STATUS_WORD for PAGE\( n \). The BUSY bit in STATUS_BYTE also asserts ALERT\( nn \) low and cannot be masked. This bit can be set as a result of various internal interactions with the PMBus communication. This fault occurs when a command is received that it cannot be safely executed with one or both channels enabled. As discussed in the Applications Information section, BUSY faults can be avoided by polling MFR_COMMON before executing some commands.

If masked faults occur immediately after power up, ALERT\( nn \) may still be pulled low because there has not been time to retrieve all of the programmed masking information from EEPROM.

Status information contained in MFR_COMMON and MFR_PADS can be used to further debug or clarify the contents of STATUS_BYTE or STATUS_WORD as shown, but the contents of these registers do not affect the state of the ALERT\( nn \) pin and may not directly influence bits in STATUS_BYTE or STATUS_WORD.
**OPERATION**

**Figure 5. LTM4683 Status Register Summary per Controller**

<table>
<thead>
<tr>
<th>STATUS_VOUT*</th>
<th>STATUS_WORD</th>
<th>STATUS_INPUT</th>
<th>STATUS_MFR_SPECIFIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 VOUT_OV Fault</td>
<td>15 VOUT</td>
<td>7 VIN_OV Fault</td>
<td>15 VOUT_OV Fault</td>
</tr>
<tr>
<td>6 VOUT_OV Warning</td>
<td>14 IOUT</td>
<td>6 VIN_OV Warning</td>
<td>6 VIN_OV Warning</td>
</tr>
<tr>
<td>5 VOUT_UV Warning</td>
<td>13 MFR_SPECIFIC</td>
<td>5 VOUT_UV Warning</td>
<td>5 VOUT_UV Warning</td>
</tr>
<tr>
<td>4 VOUT_UV Fault</td>
<td>12 POWER_GOOD#</td>
<td>4 VOUT_UV Warning</td>
<td>4 VOUT_UV Warning</td>
</tr>
<tr>
<td>3 VOUT_MAX Warning</td>
<td>10 (reads 0)</td>
<td>3 Unit Off for Insufficient VIN</td>
<td>3 Unit Off for Insufficient VIN</td>
</tr>
<tr>
<td>2 TON_MAX Warning</td>
<td>9 (reads 0)</td>
<td>2 (reads 0)</td>
<td>2 (reads 0)</td>
</tr>
<tr>
<td>1 TOFF_MAX Warning</td>
<td>8 (reads 0)</td>
<td>1 (reads 0)</td>
<td>1 (reads 0)</td>
</tr>
<tr>
<td>0 (reads 0)</td>
<td></td>
<td>0 (reads 0)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STATUS_IOUT</th>
<th>STATUS_BYTE</th>
<th>MFR_COMMON</th>
<th>MFR_PADS</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 IOUT_OC Fault</td>
<td>7 BUSY</td>
<td>7 Chip Not Driving ALERT Low</td>
<td>15 VDD33 UV or OV Fault</td>
</tr>
<tr>
<td>6 (reads 0)</td>
<td>6 OFF</td>
<td>6 Chip Not Busy</td>
<td>14 VDD33 UV or OV Fault</td>
</tr>
<tr>
<td>5 VOUT_OV</td>
<td>5 VOUT_OV</td>
<td>5 Internal Calculations Not Pending</td>
<td>13 (reads 0)</td>
</tr>
<tr>
<td>4 IOUT_OC</td>
<td>4 IOUT_OC</td>
<td>4 Output Not In Transition</td>
<td>12 (reads 0)</td>
</tr>
<tr>
<td>3 (reads 0)</td>
<td>3 (reads 0)</td>
<td>3 EEPROM Initialized</td>
<td>11 Invalid ADC Result(s)</td>
</tr>
<tr>
<td>2 TEMPERATURE</td>
<td>2 TEMPERATURE</td>
<td>2 SHARE_CLK_LOW</td>
<td>10 SYNC Clocked by External Source</td>
</tr>
<tr>
<td>1 CML</td>
<td>1 CML</td>
<td>1 WP Pin High</td>
<td>9 (reads 0)</td>
</tr>
<tr>
<td>0 NONE OF THE ABOVE</td>
<td>0 NONE OF THE ABOVE</td>
<td></td>
<td>8 (reads 0)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STATUS_TEMPERATURE</th>
<th>MFR_INFO</th>
<th>STATUS_MFR_SPECIFIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 OT Fault</td>
<td>15 Reserved</td>
<td>7 Internal Temperature Fault</td>
</tr>
<tr>
<td>6 OT Warning</td>
<td>14 Reserved</td>
<td>6 Internal Temperature Warning</td>
</tr>
<tr>
<td>5 (reads 0)</td>
<td>13 Reserved</td>
<td>5 EEPROM CRC Error</td>
</tr>
<tr>
<td>4 OT Fault</td>
<td>12 Reserved</td>
<td>4 Internal PLL Unlocked</td>
</tr>
<tr>
<td>3 (reads 0)</td>
<td>11 Reserved</td>
<td>3 Fault Log Present</td>
</tr>
<tr>
<td>2 (reads 0)</td>
<td>10 Reserved</td>
<td>2 VDD33 UV or OV Fault</td>
</tr>
<tr>
<td>1 (reads 0)</td>
<td>9 Reserved</td>
<td>1 VOUT Short Cycled</td>
</tr>
<tr>
<td>0 (reads 0)</td>
<td>8 Reserved</td>
<td>0 FAULT Pulled Low By External Device</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STATUS_CML</th>
<th>MFR_PADS</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 Invalid/Unsupported Command</td>
<td>15 VDD33 Fault</td>
</tr>
<tr>
<td>6 Invalid/Unsupported Data</td>
<td>14 VDD33 UV Fault</td>
</tr>
<tr>
<td>5 Packet Error Check Failed</td>
<td>13 (reads 0)</td>
</tr>
<tr>
<td>4 Memory Fault Detected</td>
<td>12 (reads 0)</td>
</tr>
<tr>
<td>3 Processor Fault Detected</td>
<td>11 (reads 0)</td>
</tr>
<tr>
<td>2 (reads 0)</td>
<td>10 (reads 0)</td>
</tr>
<tr>
<td>1 Other Communication Fault</td>
<td>9 (reads 0)</td>
</tr>
<tr>
<td>0 Other Memory or Logic Fault</td>
<td>8 (reads 0)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>MASKABLE</th>
<th>GENERATES ALERT</th>
<th>BIT CLEARABLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>General Fault or Warning Event</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>General Non-Maskable Event</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Dynamic</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Status Derived from Other Bits</td>
<td>No</td>
<td>Not Directly</td>
<td>No</td>
</tr>
</tbody>
</table>

For more information [www.analog.com](http://www.analog.com)
Mapping Faults to **FAULT** Pins

Channel-to-channel fault (including channels from multiple LTM4683s) dependencies can be created by connecting **FAULT** pins together. In the event of an internal fault, one or more of the channels is configured to pull the bussed **FAULT** pins low. The other channels are configured to shut down when the **FAULT** pins are pulled low. For autonomous group retry, the faulted channel is configured to let go of the **FAULT** pin(s) after a retry interval, assuming the original fault has cleared. All the channels in the group, then begins a soft-start sequence. If the fault response is LATCH_OFF, the **FAULT** pin remains asserted low until either the RUNn pin is toggled Off/On or the part is commanded Off/On. Either toggling of the RUNn pin or Off/On command will clear faults associated with the channel. If it is desired to have all faults cleared when either the RUNn pin is toggled or set bit 0 of MFR_CONFIG_ALL to a 1.

The status of all faults and warnings is summarized in the STATUS_WORD and STATUS_BYTE commands.

Additional fault detection and handling capabilities include power good pins and cyclic redundancy check (CRC).

Power Good Pins

The PGOODn pins of the LTM4683 are connected to the open drains of internal MOSFETs. The MOSFET turns on and pulls the PGOODn pin low when the channel output voltage is not within the channel’s UV and OV voltage threshold ranges. During TON_DELAY and TON_RISE sequencing, the PGOODn pin is held low. The PGOODn pin is also pulled low when the respective RUNn pin is low. The PGOODn pin response is deglitched by an internal 100µs digital filter. The PGOODn pin and PGOOD status can be different at times due to communication latency of up to 10µs.

CRC Protection

The integrity of the NVM memory is checked after a power on reset. A CRC error will prevent the controller from leaving the inactive state. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the ALERT_n pin will be pulled low. NVM repair can be attempted by writing the desired configuration to the controller and executing a STORE_USER_ALL command followed by a CLEAR_FAULTS command.

The LTM4683 manufacturing section of the NVM is mirrored. If both copies are corrupted, the “NVM CRC Fault” in the STATUS_MFR_SPECIFIC command is set. If this bit remains set after being cleared by issuing a CLEAR_FAULTS or writing a 1 to this bit, an irrecoverable internal fault has occurred. The user is cautioned to disable both output power supply rails associated with this specific part. There are no provisions for field repair of NVM faults in the manufacturing section.

SERIAL INTERFACE

The LTM4683 serial interface is a PMBus-compliant subordinate device and can operate at any frequency between 10kHz and 400kHz. The address is configurable using either the NVM or an external resistor. In addition, the LTM4683 always responds to the global broadcast address of 0x5A (7-bit) or 0x5B (7-bit).

The serial interface supports the following protocols defined in the PMBus specifications: 1) send command, 2) write byte, 3) write word, 4) group, 5) read byte, 6) read word, and 7) read block. 8) write block. All read operations will return a valid PEC if the PMBus main device requests it. If the PEC_REQUIRED bit is set in the MFR_CONFIG_ALL command, the PMBus write operations will not be acted upon until a valid PEC has been received by the LTM4683.

Communication Protection

PEC write errors (if PEC_REQUIRED is active), attempts to access unsupported commands, or writing invalid data to supported commands will result in a CML fault. The CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_CML command, and the ALERT pin is pulled low.
OPERATION

DEVICE ADDRESSING

The LTM4683 offers five different types of addressing over the PMBus interface, specifically: 1) global, 2) device, 3) rail addressing and 4) alert response address (ARA).

Global addressing provides a means for the PMBus main device to address all LTM4683 devices on the bus. The LTM4683 global address is fixed 0x5A (7-bit) or 0xB4 (8-bit) and cannot be disabled. Commands sent to the global address act the same as if PAGE is set to a value of 0xFF. Commands sent are written to both channels simultaneously. Global command 0x5B (7-bit) or 0xB6 (8-bit) is paged and allows channel-specific command of all LTM4683 devices on the bus. Other Analog Devices ICs may respond at one or both of these global addresses. Reading from global addresses is strongly discouraged.

Device addressing provides the standard means of the PMBus main device communicating with a single instance of an LTM4683. The value of the device address is set by a combination of the ASEl nn configuration pin and the MFR_ADDRESS command. When this addressing means is used, the PAGE command determines the channel being acted upon. Device addressing can be disabled by writing a value of 0x80 to the MFR_ADDRESS.

Rail addressing provides a means for the bus main device to simultaneously communicate with all channels connected together to produce a single output voltage (PolyPhase). While similar to global addressing, the rail address can be dynamically assigned with the paged MFR_RAIL_ADDRESS command, allowing for any logical grouping of channels that might be required for reliable system control. Reading from rail addresses is also strongly discouraged.

All four means of PMBus addressing require the user to employ disciplined planning to avoid addressing conflicts. Communication to LTM4683 devices at global and rail addresses should be limited to command write operations.

RESPONSES TO VOUT AND IIN/IOUT FAULTS

VOUT OV and UV conditions are monitored by comparators. The OV and UV limits are set in the following three ways.

- As a Percentage of the VOUT if Using the Resistor Configuration Pins
- In NVM, if Either Programmed at the Factory or Through the GUI
- By PMBus Command

The IIN and IOUT overcurrent monitors are performed by ADC readings and calculations. Thus, these values are based on average currents and can have a time latency of up to tCONVERT. The IOUT calculation accounts for the DCR and their temperature coefficient. The input current equals the voltage measured across the RSENSE resistor divided by the resistor value as set with the MFR_IIN_CAL_GAIN command. If this calculated input current exceeds the IN_OC_WARN_LIMIT, the ALERT nn pin is pulled low, and the IIN_OC_WARN bit is asserted in the STATUS_INPUT command.

The digital processor within the LTM4683 provides the ability to ignore the fault, shut down and latch off, or shut down and retry indefinitely (hiccup). The retry interval is set in MFR_RETRY_DELAY and can be from 120ms to 83.88 seconds in 10µs increments. The shutdown for OV/UV and OC can be done immediately or after a user-selectable de-glitch time.

Output Overvoltage Fault Response

A programmable overvoltage (OV) comparator guards against transient overshoots and long-term overvoltages at the output. In such cases, the top MOSFET is turned off, and the bottom MOSFET is turned on. However, the reverse output current is monitored while the device is in OV fault. When it reaches the limit, both top and bottom MOSFETs are turned off. The top and bottom MOSFETs will keep their state until the overvoltage condition is cleared, regardless of the PMBus VOUT_OV_FAULT_RESPONSE command.
OPERATION

byte value. This hardware-level fault response delay is typically 2µs from the overvoltage condition to BG asserted high. Using the VOUT_OV_FAULT_RESPONSE command, the user can select any of the following behaviors:

- OV Pull-Down Only (OV Cannot Be Ignored)
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

Either the Latch Off or Retry fault responses can be deglitched in increments of (0–7) • 10µs. See Table 17.

Output Undervoltage Response

The response to an undervoltage (UV) comparator output can be the following:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

The UV responses can be deglitched. See Table 18.

Peak Output Overcurrent Fault Response

Due to the current mode control algorithm, peak output current across the inductor is always limited on a cycle-by-cycle basis. The value of the peak current limit is specified in the Electrical Characteristics table. The current limit circuit operates by limiting the COMPn maximum voltage. Since internal DCR sensing is used, the COMPn maximum voltage has a temperature dependency directly proportional to the TC of the DCR of the inductor. The LT4683 automatically monitors the external temperature sensors and modifies the maximum allowed COMPn to compensate for this term. See the IOUT_OC_FAULT_LIMIT in the PMBus Command Details section for IOUT limiting details.

The overcurrent fault processing circuitry can execute the following behaviors.

- Current Limit Indefinitely
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

The overcurrent responses can be deglitched in increments of (0–7) • 16ms. See Table 19.

RESPONSES TO TIMING FAULTS

TON_MAX_FAULT_LIMIT is the time allowed for VOUT to rise and settle at start-up. The TON_MAX_FAULT_LIMIT condition is predicated upon detecting the VOUT_UV_FAULT_LIMIT as the output is undergoing a SOFT_START sequence. The TON_MAX_FAULT_LIMIT time is started after TON_DELAY has been reached, and a SOFT_START sequence is started. The resolution of the TON_MAX_FAULT_LIMIT is 10µs. If the VOUT_UV_FAULT_LIMIT is not reached within the TON_MAX_FAULT_LIMIT time, the response of this fault is determined by the value of the TON_MAX_FAULT_RESPONSE command value. This response may be one of the following:

- Ignore
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

This fault response is not deglitched. A value of 0 in TON_MAX_FAULT_LIMIT means the fault is ignored. The TON_MAX_FAULT_LIMIT should be set longer than the TON_RISE time. It is recommended that TON_MAX_FAULT_LIMIT always be set to a non-zero value; otherwise, the output may never come up, and no flag will be set for the user. See Table 21.

RESPONSES TO V_IN_OV FAULTS

V_IN overvoltage is measured with the ADC. The response is naturally deglitched by the 100ms typical response time of the ADC. The fault responses:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY. See Table 21.
OPERATION

RESPONSES TO OT/UT FAULTS

Internal Overtemperature Fault Response

An internal temperature sensor protects against NVM damage. Above 85°C, no writes to NVM are recommended. Above 130°C, the internal overtemperature warns threshold is exceeded, and the part disables the NVM and does not re-enable until the temperature has dropped to 125°C. When the die temperature exceeds 160°C, the internal temperature fault response is enabled, and the PWM is disabled until the die temperature drops below 150°C. Temperature is measured by the ADC. Internal temperature faults cannot be ignored. Internal temperature limits cannot be adjusted by the user. See Table 20.

Overtemperature and Undertemperature Fault Response

Four internal temperature sensors are used to sense the temperature of critical circuit elements like inductors and power MOSFETs on each channel. The OT_FAULT_RESPONSE and UT_FAULT_RESPONSE commands are used to determine the appropriate response to an overtemperature and under temperature conditions, respectively. If no external sense elements are used (not recommended), set the UT_FAULT_RESPONSE to ignore—and set the UT_FAULT_LIMIT to 275°C. The fault responses:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY. See Table 21.

RESPONSES TO INPUT OVERCURRENT AND OUTPUT UNDERCURRENT FAULTS

Input overcurrent and output undercurrent are measured with the ADC. The fault responses:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

RESPONSES TO EXTERNAL FAULTS

When either FAULTn pin is pulled low, the OTHER bit is set in the STATUS_WORD command, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the ALERT_nn pin is pulled low. Responses are not deglitched. Each channel can be configured to ignore or shut down, then retry in response to its FAULTn pin going low by modifying the MFR_FAULT_RESPONSE command. To avoid the ALERT_nn pin asserting low when FAULTn is pulled low, assert bit 1 of MFR_CHAN_CONFIG or mask the ALERT using the SMBALERT_MASK command.

FAULT LOGGING

The LTM4683 has the fault-logging capability. Data is logged into memory in the order shown in Table 23. The data is stored in a continuously updated buffer in RAM. When a fault event occurs, the fault log buffer is copied from the RAM buffer into the NVM. Fault logging is allowed at temperatures above 85°C; however, retention of 10 years is not guaranteed. When the die temperature exceeds 130°C, the fault logging is delayed until the die temperature drops below 125°C. The fault log data remains in NVM until an MFR_FAULT_LOG_CLEAR command is issued. Issuing this command re-enables the fault log feature. Before re-enabling the fault log, be sure no faults are present, and a CLEAR_FAULTS command has been issued.

When the LTM4683 powers up or exits its reset state, it checks the NVM for a valid fault log. If a valid fault log exists in NVM, the “Valid Fault Log” bit in the STATUS_MFR_SPECIFIC command will be set, and an ALERT event will be generated. Also, fault logging will be blocked until the LTM4683 has received an MFR_FAULT_LOG_CLEAR command before fault logging will be re-enabled.

The information is stored in EEPROM in the event of any fault that disables the controller on either channel. A FAULTn being externally pulled low will not trigger a fault logging event.
OPERATION

BUS TIMEOUT PROTECTION

The LT4683 implements a timeout feature to avoid persistent faults on the serial interface. The data packet timer begins at the first START event before the device address byte write. Data packet information must be completed within 30ms, or the LT4683 will three-state the bus and ignore the given data packet. If more time is required, assert bit 3 of MFR_CONFIG_ALL to allow typical bus timeouts of 255ms. Data packet information includes the device address byte write, command byte, repeat start event (if a read operation), device address byte read (if a read operation), all data bytes and the PEC byte if applicable.

The LT4683 allows longer PMBus timeouts for block-read data packets. This timeout is proportional to the length of the block read. The additional block read timeout applies primarily to the MFR_FAULT_LOG command. The timeout period defaults to 32ms.

The user is encouraged to use as high a clock rate as possible to maintain efficient data packet transfer between all devices sharing the serial bus interface. The LT4683 supports the full PMBus frequency range from 10kHz to 400kHz.

SIMILARITY BETWEEN PMBus, SMBus AND I²C 2-WIRE INTERFACE

The PMBus 2-wire interface is an incremental extension of the SMBus. SMBus is built upon I²C with some minor differences in timing, DC parameters and protocol. The PMBus/SMBus protocols are more robust than simple I²C byte commands because PMBus/SMBus provide timeouts to prevent persistent bus errors and optional packet error checking (PEC) to ensure data integrity. In general, a main device that can be configured for I²C communication can be used for PMBus communication with little or no change to hardware or firmware. Repeat start (restart) is not supported by all I²C controllers but is required for SMBus/PMBus reads. If a general-purpose I²C controller is used, check that repeat start is supported.

The LT4683 supports the maximum SMBus clock speed of 100kHz and is compatible with the higher speed PMBus specification (between 100kHz and 400kHz) if MFR_COMMON polling or clock stretching is enabled. For robust communication and operation, see the Note section in the PMBus command summary table (See Table 7). Clock stretching is enabled by asserting bit 1 of MFR_CONFIG_ALL.

For a description of the minor extensions and exceptions PMBus makes to SMBus, Refer to PMBus Specification Part 1 Revision 1.2: Paragraph 5: Transport.

To describe the differences between SMBus and I²C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B—Differences Between SMBus and I²C.

PMBus SERIAL DIGITAL INTERFACE

The LT4683 communicates with a host (main) device using the standard PMBus serial bus interface. The timing diagram, Figure 6, shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines. The LT4683 is a subordinate device. The main device can communicate with the LT4683 using the following formats:

- The Main Transmitter, Subordinate Receiver
- The Main Receiver, Subordinate Transmitter

The following PMBus protocols are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read, Block Write
- Alert Response Address

Figure 7—Figure 24 illustrate the aforementioned PMBus protocols. All transactions support PEC and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the PMBus timeout may be extended when reading the fault log.

Figure 7 is the key to the protocol diagrams in this section. PEC is optional.

A value shown below a field in Figure 7—Figure 24 is a mandatory value for that field.
The following data formats are implemented by PMBus.

- The main transmitter transmits to a subordinate receiver. The transfer direction, in this case is not changed.

- The main transmitter reads the subordinate receiver immediately after the first byte. At the moment of the first acknowledgement (provided by the subordinate receiver), the main transmitter becomes the main receiver, and the subordinate receiver becomes a subordinate transmitter.

- Combined format. During a change of direction within a transfer, the main device repeats both a start condition and the subordinate device address but with the R/W bit reversed. In this case, the main receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

See Figure 7 for a legend.

Handshaking features are included to ensure robust system communication. See the PMBus Communication and Command Processing subsection of the Applications Information section for further details.

**FIGURE 7—FIGURE 24 PMBus PROTOCOLS**
Figure 7. PMBus Packet Protocol Diagram Element Key

Figure 8. Quick Command Protocol

Figure 9. Send Byte Protocol

Figure 10. Send Byte Protocol with PEC

Figure 11. Write Byte Protocol

Figure 12. Write Byte Protocol with PEC

Figure 13. Write Word Protocol

Figure 14. Write Word Protocol with PEC
Figure 15. Read Byte Protocol

Figure 16. Read Byte Protocol with PEC

Figure 17. Read Word Protocol

Figure 18. Read Word Protocol with PEC

Figure 19. Block Read Protocol

Figure 20. Block Read Protocol with PEC
Figure 21. Block Write – Block Read Process Call

Figure 22. Block Write – Block Read Process Call with PEC

Figure 23. Alert Response Address Protocol

Figure 24. Alert Response Address Protocol with PEC
PMBus COMMAND SUMMARY

PMBus COMMANDS

Table 7 lists supported PMBus commands and manufacturer-specific commands. A complete description of these commands can be found in the “PMBus Power System Management Protocol Specification – Part II – Revision 1.2”. Users are encouraged to reference this specification. Exceptions or manufacturer-specific implementations are listed in Table 7. Floating point values listed in the “DEFAULT VALUE” column are either Linear 16-bit signed (PMBus Section 8.3.1) or Linear_5s_11s (PMBus Section 7.1) format, whichever is appropriate for the command. All commands from 0x00 through 0xFF not listed in Table 7 are implicitly reserved by the manufacturer. Users should avoid blind writes within this range of commands to avoid the undesired operation of the part. All commands from 0x00 through 0xCF not listed in Table 7 are implicitly not supported by the manufacturer. Attempting to access non-supported or reserved commands may result in a CML command fault event. All output voltage settings and measurements are based on the VOUT_MODE setting of 0x14. This translates to an exponent of $2^{-12}$.

If PMBus commands are received faster than they are being processed, the part may become too busy to handle new commands. In these circumstances, the part follows the protocols defined in the PMBus Specification v1.2, Part II, Section 10.8.7, to communicate that it is busy. The part includes handshaking features to eliminate busy errors and simplify error-handling software while ensuring robust communication and system behavior. See the PMBus Communication and Command Processing subsection in the Applications Information section for further details.

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PAGE</td>
<td>0x00</td>
<td>Provides integration with multi-page PMBus devices.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td></td>
<td></td>
<td>0x00</td>
<td>83</td>
</tr>
<tr>
<td>OPERATION</td>
<td>0x01</td>
<td>Operating mode control. On/off, margin high and margin low.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td></td>
<td>0x80</td>
<td>87</td>
</tr>
<tr>
<td>ON_OFF_CONFIG</td>
<td>0x02</td>
<td>RUN pin and PMBus bus on/off command configuration.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0x1E</td>
<td></td>
<td>87</td>
</tr>
<tr>
<td>CLEAR_FAULTS</td>
<td>0x03</td>
<td>Clear any fault bits that have been set.</td>
<td>Send Byte</td>
<td>N</td>
<td></td>
<td>NA</td>
<td></td>
<td></td>
<td>112</td>
</tr>
<tr>
<td>PAGE_PLUS_WRITE</td>
<td>0x05</td>
<td>Write a command directly to a specified page.</td>
<td>W Block</td>
<td>N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>83</td>
</tr>
<tr>
<td>PAGE_PLUS_READ</td>
<td>0x06</td>
<td>Read a command directly from a specified page.</td>
<td>Block R/W</td>
<td>N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>83</td>
</tr>
<tr>
<td>WRITE_PROTECT</td>
<td>0x10</td>
<td>Level of protection provided by the device against accidental changes.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>0x00</td>
<td></td>
<td>84</td>
</tr>
<tr>
<td>STORE_USER_ALL</td>
<td>0x15</td>
<td>Store user operating memory to EEPROM.</td>
<td>Send Byte</td>
<td>N</td>
<td></td>
<td>NA</td>
<td></td>
<td></td>
<td>122</td>
</tr>
<tr>
<td>RESTORE_USER_ALL</td>
<td>0x16</td>
<td>Restore user operating memory from EEPROM.</td>
<td>Send Byte</td>
<td>N</td>
<td></td>
<td>NA</td>
<td></td>
<td></td>
<td>122</td>
</tr>
<tr>
<td>CAPABILITY</td>
<td>0x19</td>
<td>Summary of PMBus optional communication protocols supported by this device.</td>
<td>R Byte</td>
<td>N</td>
<td>Reg</td>
<td></td>
<td></td>
<td>0xB0</td>
<td>111</td>
</tr>
<tr>
<td>SMBALERT_MASK</td>
<td>0x1B</td>
<td>Mask ALERT activity</td>
<td>Block R/W</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>See CMD</td>
<td></td>
<td>112</td>
</tr>
<tr>
<td>VOUT_MODE</td>
<td>0x20</td>
<td>Output voltage format and exponent ($2^{-12}$).</td>
<td>R Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td></td>
<td>$2^{-12}$</td>
<td>93</td>
</tr>
<tr>
<td>VOUT_COMMAND</td>
<td>0x21</td>
<td>Nominal output voltage set point.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.5</td>
<td>94</td>
</tr>
<tr>
<td>VOUT_MAX</td>
<td>0x24</td>
<td>The upper limit on the commanded output voltage, including VOUT_MARGIN_HI.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>1.1</td>
<td>93</td>
</tr>
</tbody>
</table>

Table 7. PMBus Commands Summary (NOTE: The Data Format Abbreviations are Detailed in Table 8)
Table 7. PMBus Commands Summary (NOTE: The Data Format Abbreviations are Detailed in Table 8)

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT_MARGIN_HIGH</td>
<td>0x25</td>
<td>Margin high output voltage set point. It must be greater than VOUT_COMMAND.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.525 0x0866</td>
<td>94</td>
</tr>
<tr>
<td>VOUT_MARGIN_LOW</td>
<td>0x26</td>
<td>Margin low output voltage set point. It must be less than VOUT_COMMAND.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.475 0x079A</td>
<td>94</td>
</tr>
<tr>
<td>VOUT_TRANSITION_RATE</td>
<td>0x27</td>
<td>Rate the output changes when VOUT is commanded to a new value.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>V/ms</td>
<td>Y</td>
<td>0.25 0xAA00</td>
<td>100</td>
</tr>
<tr>
<td>FREQUENCY_SWITCH</td>
<td>0x33</td>
<td>Switching frequency of the controller.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>kHz</td>
<td>Y</td>
<td>425kHz 0xFB52</td>
<td>91</td>
</tr>
<tr>
<td>VIN_ON (SVIN_XX)</td>
<td>0x35</td>
<td>Input voltage at which the unit should start power conversion.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>V</td>
<td>Y</td>
<td>4.75 0xC6A0</td>
<td>92</td>
</tr>
<tr>
<td>VIN_OFF (SVIN_XX)</td>
<td>0x36</td>
<td>Input voltage at which the unit should stop power conversion.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>V</td>
<td>Y</td>
<td>4.5 0xCA40</td>
<td>92</td>
</tr>
<tr>
<td>VOUT_OV_FAULT_LIMIT</td>
<td>0x40</td>
<td>Output overvoltage fault limit.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.55 0x08CD</td>
<td>93</td>
</tr>
<tr>
<td>VOUT_OV_FAULT_RESPONSE</td>
<td>0x41</td>
<td>Action to be taken by the device when an output overvoltage fault is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td>Y</td>
<td>0xB8</td>
<td>102</td>
</tr>
<tr>
<td>VOUT_OV_WARN_LIMIT</td>
<td>0x42</td>
<td>Output overvoltage warning limit.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.537 0x089A</td>
<td>93</td>
</tr>
<tr>
<td>VOUT_UV_WARN_LIMIT</td>
<td>0x43</td>
<td>Output undervoltage warning limit.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.462 0x0766</td>
<td>94</td>
</tr>
<tr>
<td>VOUT_UV_FAULT_LIMIT</td>
<td>0x44</td>
<td>Output undervoltage fault limit.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.450 0x0733</td>
<td>94</td>
</tr>
<tr>
<td>VOUT_UV_FAULT_RESPONSE</td>
<td>0x45</td>
<td>Action to be taken by the device when an output undervoltage fault is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td>Y</td>
<td>0xB8</td>
<td>103</td>
</tr>
<tr>
<td>IOUT_OC_FAULT_LIMIT</td>
<td>0x46</td>
<td>Output overcurrent fault limit.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>A</td>
<td>Y</td>
<td>40.00 0xE280</td>
<td>96</td>
</tr>
<tr>
<td>IOUT_OC_FAULT_RESPONSE</td>
<td>0x47</td>
<td>Action to be taken by the device when an output overcurrent fault is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td>Y</td>
<td>0x00</td>
<td>105</td>
</tr>
<tr>
<td>IOUT_OC_WARN_LIMIT</td>
<td>0x4A</td>
<td>Output overcurrent warning limit.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>A</td>
<td>Y</td>
<td>34.0 0xE220</td>
<td>97</td>
</tr>
<tr>
<td>OT_FAULT_LIMIT</td>
<td>0x4F</td>
<td>External overtemperature fault limit.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>C</td>
<td>Y</td>
<td>128.0 0xF200</td>
<td>98</td>
</tr>
<tr>
<td>OT_FAULT_RESPONSE</td>
<td>0x50</td>
<td>Action to be taken by the device when an external overtemperature fault is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td>Y</td>
<td>0xB8</td>
<td>107</td>
</tr>
<tr>
<td>OT_WARN_LIMIT</td>
<td>0x51</td>
<td>External overtemperature warning limit.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>C</td>
<td>Y</td>
<td>125.0 0xE8B8</td>
<td>98</td>
</tr>
<tr>
<td>UT_FAULT_LIMIT</td>
<td>0x53</td>
<td>External undertemperature fault limit.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>C</td>
<td>Y</td>
<td>–45.0 0xE530</td>
<td>99</td>
</tr>
<tr>
<td>UT_FAULT_RESPONSE</td>
<td>0x54</td>
<td>Action to be taken by the device when an external undertemperature fault is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td>Y</td>
<td>0xB8</td>
<td>107</td>
</tr>
<tr>
<td>VIN_OV_FAULT_LIMIT</td>
<td>0x55</td>
<td>Input supply overvoltage fault limit.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>V</td>
<td>Y</td>
<td>15.5 0xD3E0</td>
<td>91</td>
</tr>
<tr>
<td>VIN_OV_FAULT_RESPONSE</td>
<td>0x56</td>
<td>Action to be taken by the device when an input overvoltage fault is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td>Y</td>
<td>0x80</td>
<td>102</td>
</tr>
</tbody>
</table>
### Table 7. PMBus Commands Summary (NOTE: The Data Format Abbreviations are Detailed in Table 8)

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN_UV_WARN_LIMIT</td>
<td>0x58</td>
<td>Input supply undervoltage warning limit.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>V</td>
<td>Y</td>
<td>4.65 0xCA54</td>
<td>92</td>
</tr>
<tr>
<td>IIN_OC_WARN_LIMIT</td>
<td>0x5D</td>
<td>Input supply overcurrent warning limit.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>A</td>
<td>Y</td>
<td>10.0 0xD280</td>
<td>97</td>
</tr>
<tr>
<td>TON_DELAY</td>
<td>0x60</td>
<td>Time from RUN and/or operation on to output rail turn-on.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>0.0 0x8000</td>
<td>99</td>
</tr>
<tr>
<td>TON_RISE</td>
<td>0x61</td>
<td>Time from when the output starts to rise until the output voltage reaches the VOUT commanded value.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>3.0 0xC300</td>
<td>99</td>
</tr>
<tr>
<td>TON_MAX_FAULT_LIMIT</td>
<td>0x62</td>
<td>Maximum time from the start of TON_RISE for VOUT to cross the VOUT_UV_FAULT_LIMIT.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>5.0 0xCA80</td>
<td>100</td>
</tr>
<tr>
<td>TON_MAX_FAULT_RESPONSE</td>
<td>0x63</td>
<td>Action to be taken by the device when a TON_MAX_FAULT event is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td>Y</td>
<td>0x88</td>
<td>105</td>
</tr>
<tr>
<td>TOFF_DELAY</td>
<td>0x64</td>
<td>Time from RUN and/or operation off to the start of TOFF_FALL ramp.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>0.0 0x8000</td>
<td>100</td>
</tr>
<tr>
<td>TOFF_FALL</td>
<td>0x65</td>
<td>Time from when the output starts to fall until the output reaches zero volts.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>3.0 0xC300</td>
<td>100</td>
</tr>
<tr>
<td>TOFF_MAX_WARN_LIMIT</td>
<td>0x66</td>
<td>Maximum allowed time, after TOFF_FALL is completed, for the unit to decay below 12.5%.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>0 0x8000</td>
<td>101</td>
</tr>
<tr>
<td>STATUS_BYTE</td>
<td>0x78</td>
<td>One-byte summary of the unit’s fault condition.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td></td>
<td>NA</td>
<td>113</td>
</tr>
<tr>
<td>STATUS_WORD</td>
<td>0x79</td>
<td>Two-byte summary of the unit’s fault condition.</td>
<td>R/W Word</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td></td>
<td>NA</td>
<td>114</td>
</tr>
<tr>
<td>STATUS_VOUT</td>
<td>0x7A</td>
<td>Output voltage fault and warning status.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td></td>
<td>NA</td>
<td>114</td>
</tr>
<tr>
<td>STATUS_IOUT</td>
<td>0x7B</td>
<td>Output current fault and warning status.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td></td>
<td>NA</td>
<td>115</td>
</tr>
<tr>
<td>STATUS_INPUT</td>
<td>0x7C</td>
<td>Input supply fault and warning status.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td></td>
<td></td>
<td>NA</td>
<td>115</td>
</tr>
<tr>
<td>STATUS_TEMPERATURE</td>
<td>0x7D</td>
<td>External temperature fault and warning status for READ_TEMPERATURE_1.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td></td>
<td>NA</td>
<td>116</td>
</tr>
<tr>
<td>STATUS_CML</td>
<td>0x7E</td>
<td>Communication and memory fault and warning status.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td></td>
<td></td>
<td>NA</td>
<td>116</td>
</tr>
<tr>
<td>STATUS_MFR_SPCIFIC</td>
<td>0x80</td>
<td>Manufacturer-specific fault and state information.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td></td>
<td>NA</td>
<td>117</td>
</tr>
<tr>
<td>READ_VIN</td>
<td>0x88</td>
<td>Measured input supply voltage.</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>V</td>
<td></td>
<td>NA</td>
<td>119</td>
</tr>
<tr>
<td>READ_IIN</td>
<td>0x89</td>
<td>Measured input supply current.</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>A</td>
<td></td>
<td>NA</td>
<td>119</td>
</tr>
<tr>
<td>READ_VOUT</td>
<td>0x8B</td>
<td>Measured output voltage.</td>
<td>R Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td></td>
<td>NA</td>
<td>119</td>
</tr>
<tr>
<td>READ_IOUT</td>
<td>0x8C</td>
<td>Measured output current.</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>A</td>
<td></td>
<td>NA</td>
<td>119</td>
</tr>
<tr>
<td>READ_TEMPERATURE_1</td>
<td>0x8D</td>
<td>External temperature sensor temperature. This is the value used for all temperature-related processing, including IOUT_CAL_GAIN.</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>C</td>
<td></td>
<td>NA</td>
<td>119</td>
</tr>
<tr>
<td>READ_TEMPERATURE_2</td>
<td>0x8E</td>
<td>Internal die junction temperature. Does not affect any other commands.</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>C</td>
<td></td>
<td>NA</td>
<td>119</td>
</tr>
</tbody>
</table>
## PMBus COMMAND SUMMARY

Table 7. PMBus Commands Summary (NOTE: The Data Format Abbreviations are Detailed in Table 8)

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ_FREQUENCY</td>
<td>0x95</td>
<td>Measured PWM switching frequency.</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>Hz</td>
<td>NA</td>
<td></td>
<td>119</td>
</tr>
<tr>
<td>READ_POUT</td>
<td>0x96</td>
<td>Measured output power.</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>W</td>
<td>N/A</td>
<td></td>
<td>119</td>
</tr>
<tr>
<td>READ_PIN</td>
<td>0x97</td>
<td>Calculated input power.</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>W</td>
<td>N/A</td>
<td></td>
<td>120</td>
</tr>
<tr>
<td>PMBus_REVISION</td>
<td>0x98</td>
<td>PMBus revision is supported by this device. The current revision is 1.2.</td>
<td>R Byte</td>
<td>N</td>
<td>Reg</td>
<td></td>
<td>0x22</td>
<td></td>
<td>111</td>
</tr>
<tr>
<td>MFR_ID</td>
<td>0x99</td>
<td>The manufacturer ID of the LTM4683 in ASCII.</td>
<td>R String</td>
<td>N</td>
<td>ASC</td>
<td></td>
<td>LTC</td>
<td></td>
<td>111</td>
</tr>
<tr>
<td>MFR_MODEL</td>
<td>0x9A</td>
<td>Manufacturer part number is in ASCII.</td>
<td>R String</td>
<td>N</td>
<td>ASC</td>
<td></td>
<td></td>
<td></td>
<td>111</td>
</tr>
<tr>
<td>MFR_VOUT_MAX</td>
<td>0xA5</td>
<td>Maximum allowed output voltage including VOUT_OV_FAULT_LIMIT.</td>
<td>R Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>2.75</td>
<td>0x2C00</td>
<td>95</td>
</tr>
<tr>
<td>MFR_PIN_ACCURACY</td>
<td>0xAC</td>
<td>Returns the accuracy of the READ_PIN command</td>
<td>R Byte</td>
<td>N</td>
<td>%</td>
<td></td>
<td>5.0%</td>
<td></td>
<td>120</td>
</tr>
<tr>
<td>USER_DATA_00</td>
<td>0xB0</td>
<td>OEM RESERVED. Typically used for part serialization.</td>
<td>R/W Word</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>NA</td>
<td></td>
<td>111</td>
</tr>
<tr>
<td>USER_DATA_01</td>
<td>0xB1</td>
<td>Manufacturer reserved for LTpowerPlay.</td>
<td>R/W Word</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>NA</td>
<td></td>
<td>111</td>
</tr>
<tr>
<td>USER_DATA_02</td>
<td>0xB2</td>
<td>OEM RESERVED. Typically used for part serialization</td>
<td>R/W Word</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>NA</td>
<td></td>
<td>111</td>
</tr>
<tr>
<td>USER_DATA_03</td>
<td>0xB3</td>
<td>An NVM word available for the user.</td>
<td>R/W Word</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0x0000</td>
<td></td>
<td>111</td>
</tr>
<tr>
<td>USER_DATA_04</td>
<td>0xB4</td>
<td>An NVM word available for the user.</td>
<td>R/W Word</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>0x0000</td>
<td></td>
<td>111</td>
</tr>
<tr>
<td>MFR_EE_UNLOCK</td>
<td>0xBD</td>
<td>Contact factory.</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>127</td>
</tr>
<tr>
<td>MFR_EE_ERASE</td>
<td>0xBE</td>
<td>Contact factory.</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>127</td>
</tr>
<tr>
<td>MFR_EE_DATA</td>
<td>0xBF</td>
<td>Contact factory.</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>127</td>
</tr>
<tr>
<td>MFR_CHAN_CONFIG</td>
<td>0xD0</td>
<td>The configuration bits that are channel-specific.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0x1D</td>
<td></td>
<td>85</td>
</tr>
<tr>
<td>MFR_CONFIG_ALL</td>
<td>0xD1</td>
<td>General configuration bits.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>0x21</td>
<td></td>
<td>86</td>
</tr>
<tr>
<td>MFR_FAULT_PROPAGATE</td>
<td>0xD2</td>
<td>Configuration that determines which faults are propagated to the FAULT pin.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0x6993</td>
<td></td>
<td>108</td>
</tr>
<tr>
<td>MFR_PWM_COMP</td>
<td>0xD3</td>
<td>PWM loop compensation configuration.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0x48</td>
<td></td>
<td>89</td>
</tr>
<tr>
<td>MFR_PWM_MODE</td>
<td>0xD4</td>
<td>Configuration for the PWM engine.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0xC7</td>
<td></td>
<td>88</td>
</tr>
<tr>
<td>MFR_FAULT_RESPONSE</td>
<td>0xD5</td>
<td>Action to be taken by the device when the FAULT pin is externally asserted low.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0xC0</td>
<td></td>
<td>110</td>
</tr>
<tr>
<td>MFR_OT_FAULT_RESPONSE</td>
<td>0xD6</td>
<td>Action to be taken by the device when an internal overtemperature fault is detected.</td>
<td>R Byte</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>0xC0</td>
<td></td>
<td>106</td>
</tr>
<tr>
<td>MFR_IOUT_PEAK</td>
<td>0xD7</td>
<td>Report the maximum measured value of READ_IOUT since the last MFR_CLEAR_PEAKS.</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>A</td>
<td>NA</td>
<td></td>
<td>120</td>
</tr>
<tr>
<td>MFR_ADC_CONTROL</td>
<td>0xD8</td>
<td>ADC telemetry parameter selected for repeated fast ADC read back</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>0x00</td>
<td></td>
<td>121</td>
</tr>
<tr>
<td>MFR_RETRY_DELAY</td>
<td>0xDB</td>
<td>Retry interval during FAULT retry mode.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>250.0 0x2E8</td>
<td>101</td>
</tr>
<tr>
<td>MFR_RESTART_DELAY</td>
<td>0xDC</td>
<td>The minimum time the RUN pin is held low by the LTM4683.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>150.0 0xF258</td>
<td>101</td>
</tr>
</tbody>
</table>
# PMBus Command Summary

## Table 7. PMBus Commands Summary (NOTE: The Data Format Abbreviations are Detailed in Table 8)

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_VOUT_PEAK</td>
<td>0xDD</td>
<td>The maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.</td>
<td>R Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>NA</td>
<td></td>
<td>120</td>
</tr>
<tr>
<td>MFR_VIN_PEAK</td>
<td>0xDE</td>
<td>The maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>V</td>
<td>NA</td>
<td></td>
<td>120</td>
</tr>
<tr>
<td>MFR_TEMPERATURE_1_PEAK</td>
<td>0xDF</td>
<td>The maximum measured value of external Temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>C</td>
<td>NA</td>
<td></td>
<td>120</td>
</tr>
<tr>
<td>MFR_READ_IIN_PEAK</td>
<td>0xE1</td>
<td>The maximum measured value of READ_IIN command since last MFR_CLEAR_PEAKS.</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>A</td>
<td>NA</td>
<td></td>
<td>120</td>
</tr>
<tr>
<td>MFR_CLEAR_PEAKS</td>
<td>0xE3</td>
<td>Clears all peak values.</td>
<td>Send Byte</td>
<td>N</td>
<td>NA</td>
<td></td>
<td>NA</td>
<td></td>
<td>113</td>
</tr>
<tr>
<td>MFR_READ_ICHIP</td>
<td>0xE4</td>
<td>Measured supply current of the SVIN pin</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>A</td>
<td>NA</td>
<td></td>
<td>121</td>
</tr>
<tr>
<td>MFR_PADS</td>
<td>0xE5</td>
<td>Digital status of the I/O pads.</td>
<td>R Word</td>
<td>N</td>
<td>Reg</td>
<td></td>
<td>NA</td>
<td></td>
<td>117</td>
</tr>
<tr>
<td>MFR_ADDRESS</td>
<td>0xE6</td>
<td>Sets the 7-bit I2C address byte, Ch 0 and 1</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>0x4F</td>
<td></td>
<td>85</td>
</tr>
<tr>
<td>MFR_ADDRESS</td>
<td>0xE6</td>
<td>Sets the 7-bit I2C address byte, Ch 2 and 3</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>0x4E</td>
<td></td>
<td>85</td>
</tr>
<tr>
<td>MFR_SPECIAL_ID</td>
<td>0xE7</td>
<td>Manufacturer code representing the LTM4683 and revision</td>
<td>R Word</td>
<td>N</td>
<td>Reg</td>
<td></td>
<td>0x4191</td>
<td></td>
<td>111</td>
</tr>
<tr>
<td>MFR_IIN_CAL_GAIN</td>
<td>0xE8</td>
<td>The resistance value of the input current sense element in mΩ.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>mΩ</td>
<td>Y</td>
<td>2.0</td>
<td>97</td>
</tr>
<tr>
<td>MFR_FAULT_LOG_STORE</td>
<td>0xEA</td>
<td>Command a transfer of the fault log from RAM to EEPROM.</td>
<td>Send Byte</td>
<td>N</td>
<td>NA</td>
<td></td>
<td></td>
<td></td>
<td>123</td>
</tr>
<tr>
<td>MFR_INFO</td>
<td>0x</td>
<td>Contact factory.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>127</td>
</tr>
<tr>
<td>MFR_IOUT_CAL_GAIN</td>
<td>0xDA</td>
<td>SET AT FACTORY. Typical 0.36mΩ</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>mΩ</td>
<td></td>
<td>0.360 Typical 0x017</td>
<td>95</td>
</tr>
<tr>
<td>MFR_FAULT_LOG_CLEAR</td>
<td>0xEC</td>
<td>Initialize the EEPROM block reserved for fault logging.</td>
<td>Send Byte</td>
<td>N</td>
<td>NA</td>
<td></td>
<td></td>
<td></td>
<td>127</td>
</tr>
<tr>
<td>MFR_FAULT_LOG</td>
<td>0xEE</td>
<td>Fault log data bytes.</td>
<td>R Block</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>NA</td>
<td></td>
<td>123</td>
</tr>
<tr>
<td>MFR_COMMON</td>
<td>0xEF</td>
<td>Manufacturer status bits that are common across multiple ADI chips.</td>
<td>R Byte</td>
<td>N</td>
<td>Reg</td>
<td></td>
<td>NA</td>
<td></td>
<td>118</td>
</tr>
<tr>
<td>MFR_COMPARE_USER_ALL</td>
<td>0xF0</td>
<td>Compares current command contents with NVM.</td>
<td>Send Byte</td>
<td>N</td>
<td>NA</td>
<td></td>
<td></td>
<td></td>
<td>122</td>
</tr>
<tr>
<td>MFR_TEMPERATURE_2_PEAK</td>
<td>0xF4</td>
<td>Peak internal die temperature since last MFR_CLEAR_PEAKS.</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>C</td>
<td>NA</td>
<td></td>
<td>121</td>
</tr>
<tr>
<td>MFR_PWM_CONFIG</td>
<td>0xF5</td>
<td>Set numerous parameters for the DC/DC controller, including phasing.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>0x10</td>
<td></td>
<td>90</td>
</tr>
<tr>
<td>MFR_IOUT_CAL_GAIN_TC</td>
<td>0xF6</td>
<td>Temperature coefficient of the current sensing element.</td>
<td>R/W Word</td>
<td>Y</td>
<td>CF</td>
<td>ppm/˚C</td>
<td>Y</td>
<td>3900 0x0F3C</td>
<td>95</td>
</tr>
<tr>
<td>MFR_RVIN_CAL_GAIN</td>
<td>0xF7</td>
<td>The resistance value of the VIN pin filter element in mΩ.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>mΩ</td>
<td>Y</td>
<td>1000 0x03E8</td>
<td>92</td>
</tr>
<tr>
<td>MFR_TEMP_1_GAIN</td>
<td>0xF8</td>
<td>Sets the slope of the external temperature sensor.</td>
<td>R/W Word</td>
<td>Y</td>
<td>CF</td>
<td></td>
<td>Y</td>
<td>0.995 0x3FAE</td>
<td>98</td>
</tr>
</tbody>
</table>

For more information [www.analog.com](http://www.analog.com)
## PMBus COMMAND SUMMARY

**Table 7. PMBus Commands Summary (NOTE: The Data Format Abbreviations are Detailed in Table 8)**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_TEMP_1_OFFSET</td>
<td>0xF9</td>
<td>Sets the offset of the external temperature sensor with respect to –273.1°C</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>C</td>
<td>Y</td>
<td>0.0</td>
<td>98</td>
</tr>
<tr>
<td>MFR_RAIL_ADDRESS</td>
<td>0xFA</td>
<td>Common address for PolyPhase outputs to adjust common parameters.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0x80</td>
<td>85</td>
<td></td>
</tr>
<tr>
<td>MFR_REAL_TIME</td>
<td>0xFB</td>
<td>48-bit share-clock counter value.</td>
<td>R Block</td>
<td>N</td>
<td>CF</td>
<td>NA</td>
<td>124</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_RESET</td>
<td>0xFD</td>
<td>Commanded reset without requiring a power down.</td>
<td>Send Byte</td>
<td>N</td>
<td>NA</td>
<td>87</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Commands indicated with Y in the NVM column indicate that these commands are stored and restored using the STORE_USER_ALL and RESTORE_USER_ALL commands, respectively.

**Note 2:** Commands with a default value of NA indicate “not applicable”. Commands with a default value of FS indicate “factory set on a per part basis”.

**Note 3:** The LTM4683 contains additional commands not listed in Table 7. Reading these commands is harmless to the operation of the IC; however, the contents and meaning of these commands can change without notice.

**Note 4:** Some unpublished commands are read-only and will generate a CML bit 6 fault if written.

**Note 5:** Writing to commands not published in Table 7 is not permitted.

**Note 6:** The user should not assume compatibility of commands between different parts based on command names. Always refer to the manufacturer’s data sheet for each part for a complete definition of a command’s function. Analog Devices, Inc., strives to keep command functionality compatible between all Analog Devices, Inc’s ICs. Differences may occur to address specific product requirements.

### Table 8. Data Format Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>L11</td>
<td>PMBus data field b[15:0]</td>
</tr>
</tbody>
</table>
| Linear_5s_11s| Value = \(Y \cdot 2^N\)  
where \(N = b[15:11]\) is a 5-bit two's complement integer and \(Y = b[10:0]\) is an 11-bit two's complement integer  |
|              | Example:                                                                    |
|              | For \(b[15:0] = 0x9807\) = 'b10011_000_0000_0111                           |
|              | Value = 7 \(\cdot 2^{-13}\) = 854 \(\cdot 10^{-6}\)                      |
|              | From “PMBus Spec Part II: Paragraph 7.1”                                     |
| L16          | PMBus data field b[15:0]                                                     |
| Linear_16u   | Value = \(Y \cdot 2^N\)  
where \(Y = b[15:0]\) is an unsigned integer and \(N = VOUT MODE PARAMETER\) is a 5-bit two's complement exponent that is hardwired to –12 decimal |
|              | Example:                                                                    |
|              | For \(b[15:0] = 0x9803\) = 'b10011_1000_0000_0000                           |
|              | Value = 19456 \(\cdot 2^{-12}\) = 4.75 From “PMBus Spec Part II: Paragraph 8.2” |
| Reg          | PMBus data field b[15:0] or b[7:0]. Bit field meaning is defined in detailed PMBus Command Description. |
| L16          | PMBus data field b[15:0]                                                     |
| Integer Word | Value = \(Y\)  
where \(Y = b[15:0]\) is a 16-bit unsigned integer |
|              | Example:                                                                    |
|              | For \(b[15:0] = 0x9807\) = 'b10011_1000_0000_0111                           |
|              | Value = 38919 (decimal)                                                     |
| CF           | Value is defined in detailed PMBus Command Description.                     |
|              | This is often an unsigned or two's complement integer scaled by an MFR specific constant. |
| ASC          | ASCII Format  
A variable length string of text characters conforming to ISO/IEC 8859-1 standard. |
APPLICATIONS INFORMATION

V<sub>IN</sub> TO V<sub>OUT</sub> STEP-DOWN RATIOS

There are restrictions in the maximum V<sub>IN</sub> and V<sub>OUT</sub> step-down ratio that can be achieved for a given input voltage. Each output of the LT4683 is capable of a 95% duty cycle at 500kHz, but the V<sub>IN</sub> to V<sub>OUT</sub> minimum dropout is still a function of its load current and will limit output current capability related to the high duty cycle on the topside switch.

Minimum on-time t<sub>ON(MIN)</sub> is another consideration in operating at a specified duty cycle while operating at a certain frequency since t<sub>ON(MIN)</sub> < D/f<sub>SW</sub>, where D is the duty cycle and f<sub>SW</sub> is the switching frequency. t<sub>ON(MIN)</sub> is specified in the electrical parameters as 85ns. See Note 6 in the Electrical Characteristics section for output current guideline.

INPUT CAPACITORS

The LT4683 module should be connected to a low AC-impedance DC source. For the regulator input, four 22µF input ceramic capacitors are used to handle the RMS ripple current. A 47µF to 150µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low-impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated with Equation 2.

\[
D_n = \frac{V_{OUT,n}}{V_{IN,n}}
\]

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated with Equation 3.

\[
I_{CIN,n}(RMS) = \frac{I_{OUT,n(MAX)}}{\eta}\sqrt{D_n \cdot (1 - D_n)}
\]

In Equation 3, \(\eta\)% is the estimated efficiency of the module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor or a polymer capacitor. Analog Devices, Inc’s Application Note 77 can be utilized to help calculate ripple current cancellation for multiphase applications.

OUTPUT CAPACITORS

The LT4683 is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as C<sub>OUT</sub> are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. The C<sub>OUT</sub> can be a low ESR tantalum capacitor, a low ESR polymer, or a ceramic capacitor. The typical output capacitance range for each output is from 400µF to 1000µF. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spikes is required. Table 13 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 10A to 20A step, with a 10A/µs transient in each channel. Table 13 optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 13 matrix, and the LTpowerCAD design tool will be provided for stability analysis. Multiphase operation reduces effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The LTpowerCAD design tool can calculate the output ripple reduction as the number of implemented phases increases by N times. A small value 10Ω resistor can be placed in series from V<sub>OUT</sub>n to the V<sub>OSNS0</sub> pin to allow for a bode plot analyzer to inject a signal into the control loop and validate the regulator stability. The LT4683’s stability compensation can be adjusted using two external capacitors (COMP<sub>a</sub>, COMP<sub>b</sub>) and the MFR_PWM_COMP commands.

LIGHT LOAD CURRENT OPERATION

The LT4683 has two modes of operation, including high efficiency, discontinuous-conduction mode (DCM) or forced continuous mode (FCM). The mode of operation is configured by bit 0 of the MFR_PWM_MODE<sub>n</sub> command (discontinuous-conduction mode is always the
APPLICATIONS INFORMATION

start-up mode, forced continuous mode is the default running mode).

If a channel is enabled for discontinuous-conduction mode operation, the inductor current is not allowed to reverse. The reverse current comparator, \( I_{\text{REV}} \), turns off the bottom MOSFET (Mbn) just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller can operate in discontinuous (pulse-skipping) operation. In forced continuous mode operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined solely by the voltage on the \( \text{COMPn} \) pin. In this mode, the efficiency at light loads is lower than in discontinuous mode operation. However, continuous mode exhibits lower output ripple and less interference with audio circuitry. Forced continuous mode may result in a reverse inductor current, which can cause the input supply to boost. The \( \text{VIN}_{\text{OV}}_{\text{FAULT\_LIMIT}} \) can detect this (if \( \text{SVIN}_{\text{nn}} \) is connected to \( \text{VIN01} \) and/or \( \text{VIN23} \)) and turn off the offending channel. However, this fault is based on an ADC read and can nominally take up to 100ms to detect. If there is a concern about the input supply boosting, keep the part in discontinuous conduction operation.

SWITCHING FREQUENCY AND PHASE

The switching frequency of the LTM4683’s channels is established by its analog phase-locked-loop (PLL) locking on to the clock present at the module’s \( \text{SYNC\_nn} \) pin. The clock waveform on the \( \text{SYNC\_nn} \) pin can be generated by the LTM4683’s internal circuitry when an external pull-up resistor to 3.3V (e.g., \( \text{VDD33} \)) is provided, in combination with the LTM4683 control IC’s FREQUENCY_SWITCH command being set to one of the following supported values: 250kHz, 350kHz, 425kHz, 500kHz, 575kHz, 650kHz, 750kHz. In this configuration, the module is called a “sync main” (using the factory-default setting of MFR_CONFIG_ALL[4] = 0b), \( \text{SYNC\_nn} \) becomes a bidirectional open-drain pin, and the LTM4683 pulls \( \text{SYNC} \) logic low for nominally 500ns at a time, at the prescribed clock rate. The \( \text{SYNC} \) signal can be bused to other LTM4683 modules (configured as “sync subordinates”) for purposes of synchronizing switching frequencies of multiple modules within a system—but only one LTM4683 internal controller should be configured as a “sync main”; the other LTM4683(s) should be configured as “sync subordinates”.

The most straightforward way is to set its FREQUENCY_SWITCH command to 0x0000 and MFR_CONFIG_ALL[4] = 1b. This can be easily implemented with resistor pin-strap settings on the FSWPH_nn_CFG pin (see Table 3). Using MFR_CONFIG_ALL[4] = 1b, the LTM4683’s \( \text{SYNC} \) pin becomes a high impedance input only—i.e., it does not drive \( \text{SYNC} \) low. The LTM4683 module synchronizes its frequency to the clock applied to its \( \text{SYNC} \) pin. The only shortcoming of this approach is that in the absence of an externally applied clock, the switching frequency of the module will default to the low end of its frequency-synchronization capture range (~225kHz).

If fault-tolerance to the loss of an externally applied \( \text{SYNC} \) clock is desired, the FREQUENCY_SWITCH command of a “sync subordinate” can be left at the nominal target switching frequency of the application and not 0x0000. However, it is still necessary to configure MFR_CONFIG_ALL[4] = 1b. With this combination of configurations, the LTM4683’s \( \text{SYNC\_nn} \) pins become a high-impedance input, and the module synchronizes its frequency to that of the externally applied clock, provided that the frequency of the externally applied clock exceeds \( \frac{1}{2} \) of the target frequency (FREQUENCY_SWITCH). If the \( \text{SYNC} \) clock is absent, the module responds by operating at its target frequency, indefinitely. If and when the \( \text{SYNC} \) clock is restored, the module automatically phase-locks to the \( \text{SYNC} \) clock as normal. The only shortcoming of this approach is that the EEPROM must be configured per above guidance; resistor pin-strap options on the FSWPH_nn_CFG pin alone cannot provide fault-tolerance to the absence of the \( \text{SYNC} \) clock.

The FREQUENCY_SWITCH register can be altered via \( \text{I}^2\text{C} \) commands, but only when the switching action is disengaged, i.e., the module’s outputs are turned off. The FREQUENCY_SWITCH command takes on the value stored in NVM at \( \text{SVIN} \) power-up, but is overridden according to a resistor pin-strap applied between the FSWPH_nn_CFG pin and \( \text{SGND} \) only if the module is configured to respect resistor pin-strap settings (MFR_CONFIG_ALL[6] = 0b).
APPLICATIONS INFORMATION

Table 3 highlights the available resistor pin-strap and corresponding FREQUENCY_SWITCH settings.

The relative phasing of all active channels in a PolyPhase rail should be optimally phased. The relative phasing of each rail is $360^\circ/n$, where $n$ is the number of phases in the rail. MFR_PWM_CONFIG[2:0] configures channel relative phasing with respect to the SYNC_nn pin. Phase relationship values are indicated in $0^\circ$ corresponding to the falling edge of SYNC being coincident with the turn-on of the top MOSFETs.

The MFR_PWM_CONFIG command can be altered via I^2C commands, but only when the switching action is disengaged, i.e., the module’s outputs are turned off. The MFR_PWM_CONFIG command takes on the value stored in NVM at SV_IN_nn power-up, but is overridden according to a resistor pin-strap applied between the FSWPH_nn_CFG pin and SGND only if the module is configured to respect resistor pin-strap settings (MFR_CONFIG_ALL[6] = 0b). Table 3 highlights the available resistor pin-strap and corresponding MFR_PWM_CONFIG[2:0] settings.

Some combinations of FREQUENCY_SWITCH and MFR_PWM_CONFIG[2:0] are not available by resistor pin-strapping the FSWPH_nn_CFG pin. All combinations of supported values for FREQUENCY_SWITCH and MFR_PWM_CONFIG[2:0] can be configured by NVM programming—or I^2C transactions, provided switching action is disengaged, i.e., the module’s outputs are turned off.

Care must be taken to minimize capacitance on SYNC to ensure that the pull-up resistor versus the capacitor load has a low enough time constant for the application to form a “clean” clock. (See Open-Drain Pins section.)

When an LTM4683 is configured as a sync subordinate, it is permissible for external circuitry to drive the SYNC_nn pin from a current-limited source (less than 10mA), rather than using a pull-up resistor. Any external circuitry must not drive high with arbitrarily low impedance at SV_IN_nn power-up, because the SYNC_nn output can be low impedance until NVM contents have been downloaded to RAM.

Recommended LTM4683 switching frequencies of operation for many common VIN-to-VOUT applications are indicated in Table 9. When the two channels of an LTM4683 are stepping input voltage(s) down to output voltages whose recommended switching frequencies are significantly different, operation at the higher of the two recommended switching frequencies is preferable, but minimum on-time must be considered. (See Minimum On-Time Considerations section.)

### Table 9. Recommended Switching Frequency for Various VIN-to-VOUT Step-Down Scenarios

<table>
<thead>
<tr>
<th>5VIN</th>
<th>8VIN</th>
<th>12VIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3VOUT</td>
<td>350kHz</td>
<td>250kHz</td>
</tr>
<tr>
<td>0.4VOUT</td>
<td>575kHz</td>
<td>350kHz</td>
</tr>
<tr>
<td>0.5VOUT</td>
<td>650kHz</td>
<td>425kHz</td>
</tr>
<tr>
<td>0.6VOUT</td>
<td>650kHz</td>
<td>500kHz</td>
</tr>
<tr>
<td>0.7VOUT</td>
<td>650kHz</td>
<td>575kHz</td>
</tr>
</tbody>
</table>

#### OUTPUT CURRENT LIMIT PROGRAMMING

The cycle-by-cycle current limit (VSENSE/DCR) is proportional to COMPnb, which can be programmed from 1.45V to 2.2V using the PMBus command IOUT_OC_FAULT_LIMIT. The LTM4683 uses only the sub-milliokhm sensing to detect current levels. See IOUT_OC_FAULT_LIMIT details in the PMBus Command Details section. The LTM4683 has two ranges of current limit programming. The value of MFR_PWM_MODE[2] is reserved, and the MFR_PWM_MODE[7], and IOUT_OC_FAULT_LIMIT are used to set the current limit level, see the PMBus Commands section, the device can regulate output voltage with the peak current under the value of IOUT_OC_FAULT_LIMIT in normal operation. In case the output current exceeds that current limit, an OC fault will be issued. Each of the IOUT_OC_FAULT_LIMIT ranges will affect the loop gain, and subsequently affect the loop stability, so setting the range of current limiting is a part of loop design.

The LTpowerCAD design tool can be used to look at the loop stability changes if current limit range is adjusted. The LTM4683 will automatically update the current limit as the inductor temperature changes. Keep in mind this operation is on a cycle-by-cycle basis and is only a function of the peak inductor current. The average inductor current is monitored by the ADC converter and can provide a warning if too much average output current is detected.
## APPLICATIONS INFORMATION

The overcurrent fault is detected when the COMP_nb voltage hits the maximum value. The digital processor within the LTM4683 can either ignore the fault, shut down and latch off or shut down and retry indefinitely (hiccup). See the overcurrent portion of the Operation section for more detail. The Read_POUT can be used to readback calculated output power.

### MINIMUM ON-TIME CONSIDERATIONS

Minimum on-time, t_{ON(MIN)}, is the smallest time duration that the LTM4683 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low-duty cycle applications may approach this minimum on-time limit, and care should be taken to ensure Equation 4.

$$t_{ON(MIN)} < \frac{V_{OUTn}}{V_{INn} \cdot f_{OSC}}$$

(4)

If the duty cycle falls below what can be accommodated by the minimum on time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTM4683 is 85ns.

### VARIABLE DELAY TIME, SOFT-START AND OUTPUT VOLTAGE RAMPING

The LTM4683 must enter its run state before soft-start. The RUNn pins are released after the part initializes and SV_{IN,nn} exceeds the VIN_ON threshold. If multiple LTM4683s are used in an application, they should be configured to share the same RUNn pins. They all hold their respective RUNn pins low until all devices initialize and SV_{IN} exceeds the VIN_ON threshold for all devices. The SHARE_CLK_{nn} pin assures that all the devices connected to the signal use the same time base.

After the RUNn pin is released, the controller waits for the user-specified turn-on delay (TON_DELAYn) before initiating an output voltage ramp. Multiple LTM4683s and other Analog Devices ICs can be configured to start with variable delay times. To work correctly, all devices use the same timing clock (SHARE_CLK), and all devices must share the RUNn pin.

This allows the relative delay of all parts to be synchronized. The actual variation in the delay will be dependent on the highest clock rate of the devices connected to the SHARE_CLK pin (all Analog Devices ICs are configured to allow the fastest SHARE_CLK signal to control the timing of all devices). The SHARE_CLK signal can be ±10% in frequency. Thus, the actual time delays will have some variance.

Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set point. The rise time of the voltage ramp can be programmed using the TON_RISEn command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting TON_RISEn to any value less than 0.250ms. The LTM4683 performs the necessary math internally to ensure that the voltage ramp is controlled to the desired slope. However, the voltage slope can not be any faster than the V_{OUTn} fundamental limits of the power stage. The number of t_{ON(MIN)} steps in the ramp is equal to TON_RISE/0.1ms. Therefore, the shorter the TON_RISEn time setting, the more discrete steps in the soft-start ramp appear.

The LTM4683 PWM always operates in discontinuous-conduction mode during the TON_RISEn operation. In discontinuous-conduction mode, the bottom MOSFET (MBn) is turned off as soon as reverse current is detected in the inductor. This allows the regulator to start up into a pre-biased load.

There is no analog tracking feature in the LTM4683; however, two outputs can be given the same TON_RISEn and TON_DELAYn times to achieve ratiometric rail tracking. Because the RUNn pins are released simultaneously, and both units use the same time base (SHARE_CLK), the outputs track very closely. If the circuit is in a PolyPhase configuration, all timing parameters must be the same.

### DIGITAL SERVO MODE

For maximum accuracy in the regulated output voltage, enable the digital servo loop by asserting bit 6 of the MFR_PWM_MODE command. In digital servo mode, the LTM4683 will adjust the regulated output voltage based on the ADC voltage reading. Every 90ms, the digital servo...
APPLICATIONS INFORMATION

loop will step the LSB of the DAC (nominally 1.375mV or 0.6875mV depending on the voltage range bit) until the output is at the correct ADC reading. At power-up, this mode engages after TON_MAX_FAULT_LIMIT unless the limit is set to 0 (infinite). If the TON_MAX_FAULT_LIMIT is set to 0 (infinite), the servo begins after TON_RISE is complete and $V_{OUT}$ has exceeded the VOUT_UV_FAULT_LIMIT. This same point in time is when the output changes from discontinuous to the programmed mode, as indicated in MFR_PWM_MODE bit 0. See Figure 25 for details on the $V_{OUT}$ waveform under time-based sequencing. If the TON_MAX_FAULT_LIMIT is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE is set to ignore 0x00, the servo begins:

1. After the TON_RISE sequence is complete
2. After the TON_MAX_FAULT_LIMIT time is reached; and
3. After the VOUT_UV_FAULT_LIMIT has been exceeded or the IOUT_OC_FAULT_LIMIT is no longer active.

If the TON_MAX_FAULT_LIMIT is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE is not set to ignore 0x00, the servo begins:

1. After the TON_RISE sequence is complete; and
2. After the TON_MAX_FAULT_LIMIT time has expired and both VOUT_UV_FAULT and IOUT_OC_FAULT are not present.

The maximum rise time is limited to 1.3 seconds.

In a PolyPhase configuration, it is recommended only one of the control loops have the digital servo mode enabled. This will assure that the various loops do not work against each other due to slight differences in the reference circuits.

SOFT OFF (SEQUENCED OFF)

In addition to a controlled start-up, the LTM4683 also supports controlled turn-off. The TOFF_DELAY and TOFF_FALL functions are shown in Figure 26. TOFF_FALL is processed when the RUNn pin goes low or if the part is commanded off. If the part faults off or FAULTn is pulled low externally, and the part is programmed to respond to this, the output will be three-state rather than exhibiting a controlled ramp. The output will decay as a function of the load. The output voltage will operate as shown in Figure 26 as long as the part is in forced continuous mode and the TOFF_FALL time is sufficiently slow that the power stage can achieve the desired slope. The TOFF_FALL time can only be met if the power stage and controller can sink sufficient current to ensure the output is at zero volts by the end of the fall time interval. If the TOFF_FALL time is set shorter than the time required to discharge the load capacitance, the output will not reach the desired zero-volt state. At the end of TOFF_FALL, the controller will cease to sink current, and $V_{OUT}$ will decay.

Figure 25. Timing Controlled $V_{OUT}$ Rise

Figure 26. TOFF_DELAY and TOFF_FALL
APPLICATIONS INFORMATION

at the natural rate determined by the load impedance. If the controller is in discontinuous-conduction mode, the controller will not pull a negative current, and the output will be pulled low by the load, not the power stage. The maximum fall time is limited to 1.3 seconds. The shorter the TOFF_FALL time is set, the larger the discrete steps in the TOFF_FALL ramp will appear. The number of steps in the ramp is equal to TOFF_FALL/0.1ms.

UNDERVOLTAGE LOCKOUT

The LTM4683 is initialized by an internal threshold-based UVLO where VIN must be approximately 4V and INTVCC_{nn}, VDD33_{nn}, and VDD25_{nn} must be within approximately 20% of their regulated values. In addition, VDD33_{nn} must be within approximately 7% of the targeted value before the RUNnn pin is released. After the part has initialized, an additional comparator monitors VIN. The VIN_ON threshold must be exceeded before the power sequencing can begin. When the VIN drops below the VIN_OFF threshold, the SHARE_CLK_{nn} pin will be pulled low, and the VIN must increase above the VIN_ON threshold before the controller will restart. The normal start-up sequence will be allowed after the VIN_ON threshold is crossed. If FAULT_{nn} is held low when VIN is applied, ALERT_{nn} will be asserted low even if the part is programmed not to assert ALERT_{nn} when FAULT_{nn} is held low. If I^2C communication occurs before the LTM4683 is out of reset and only a portion of the command is seen by the part, this can be interpreted as a CML fault. If a CML fault is detected, ALERT_{nn} is asserted low.

It is possible to program the contents of the NVM in the application if the VDD33_{nn} supply is externally driven directly to VDD33_{nn} or through VBIAS. This will activate the digital portion of the LTM4683 without engaging the high voltage sections. PMBus communications are valid in this supply configuration. If VIN has not been applied to the LTM4683, bit 3 (NVM Not Initialized) in MFR_COMMON will be asserted low. If this condition is detected, the part will only respond to addresses 5A and 5B. To initialize the part issue, the following set of commands: global address 0x5B command 0xBD data 0x2B followed by global address 5B command 0xBD and data 0xC4. The part will now respond to the correct address. Configure the part as desired, then issue a STORE_USER_ALL. When VIN is applied, an MFR_RESET command must be issued to allow the PWM to be enabled and valid ADC conversions to be read.

FAULT DETECTION AND HANDLING

The LTM4683 FAULT_{nn} pins are configurable to indicate a variety of faults, including overvoltage (OV), undervoltage (UV), overcurrent (OC), overtemperature (OT), timing faults, and peak overcurrent faults. In addition, the FAULT_{nn} pins can be pulled low by external sources, indicating a fault in some other portion of the system. The fault response is configurable and allows the following options:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

See the PMBus Command Summary and the PMBus Command Details sections and refer to the PMBus specification for more details.

The OV response is automatic. If an OV condition is detected, TG_{nn} goes low, and BG_{nn} is asserted.

Fault logging is available on the LTM4683. The fault logging is configurable to automatically store data when a fault occurs that causes the unit to fault off. The header portion of the fault logging table contains peak values. It is possible to read these values at any time. This data will be useful while troubleshooting the fault.

If the LTM4683 internal temperature is in excess of 85°C, writes into the NVM (other than fault logging) are not recommended. The data will still be held in RAM, unless the 3.3V supply UVLO threshold is reached. If the die temperature exceeds 130°C, all NVM communication is disabled until the die temperature drops below 120°C.

For more information www.analog.com
APPLICATIONS INFORMATION

OPEN-DRAIN PINS

The LT4683 has the following open-drain pins:

3.3V Pins
1. FAULTn
2. SYNC_nn
3. SHARE_CLK_nn
4. PGOODn

5.5V Pins (5.5V pins operate correctly when pulled to 3.3V.)
1. RUNn
2. ALERT_nn
3. SCL_nn
4. SDA_nn

All the above open-drain pins have on-chip pull-down transistors that can sink 3mA at 0.4V. The low threshold on the pins is 0.8V; thus, there is plenty of margin on the digital signals with 3mA of current. For 3.3V pins, 3mA of current is a 1.1k resistor. Unless there are transient speed issues associated with the RC time constant of the resistor pull-up and parasitic capacitance to ground, a 10k resistor or larger is generally recommended.

For high-speed signals such as the SDA, SCL, and SYNC, a lower-value resistor may be required. The RC time constant should be set to 1/3 to 1/5 of the required rise time to avoid timing issues. For a 100pF load and a 400kHz PMBus communication rate, the rise time must be less than 300ns. The resistor pull-up on the SDA_nn and SCL_nn pins with the time constant set to 1/3 of the rise time is given by Equation 5.

\[ R_{PULLUP} = \frac{t_{RISE}}{3 \times 100pF} = 1k \]  

(5)

The closest 1% resistor value is 1k. Be careful to minimize parasitic capacitance on the SDA and SCL pins to avoid communication problems. To estimate the loading capacitance, monitor the signal in question and measure how long it takes for the desired signal to reach approximately 63% of the output value. This is a one-time constant. The SYNC_nn pin has an on-chip pull-down transistor with the output held low for nominally 500ns. If the internal oscillator is set for 500kHz, the load is 100pF, and a 3x time constant is required, the resistor calculation is given by Equation 6.

\[ R_{PULLUP} = \frac{2 \mu s - 500ns}{3 \times 100pF} = 5k \]  

(6)

The closest 1% resistor is 4.99k.

If timing errors occur or if the SYNC frequency is not as fast as desired, monitor the waveform and determine if the RC time constant is too long for the application. If possible, reduce the parasitic capacitance. If not, reduce the pull-up resistor sufficiently to ensure proper timing. The SHARE_CLK_nn pull-up resistor has a similar equation with a period of 10μs and a pull-down time of 1μs. The RC time constant should be approximately 3μs or faster.

PHASE-LOCKED LOOP AND FREQUENCY SYNCHRONIZATION

The LT4683 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. The PLL is locked to the falling edge of the SYNC_nn pin. The phase relationship between the PWM controller and the falling edge of SYNC is controlled by the lower 3 bits of the MFR_PWM_CONFIG command. For PolyPhase applications, it is recommended that all the phases be spaced evenly. Thus, for a 2-phase system, the signals should be 180° out of phase, and a 4-phase system should be spaced 90°.

The phase detector is an edge-sensitive digital type that provides a known phase shift between the external and internal oscillators. This type of phase detector does not exhibit a false lock to the harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. The PLL lock range is guaranteed between 250kHz and 1MHz. Nominal parts will have a range beyond this; however, the operation to a wider frequency range is not guaranteed.

The PLL has a lock detection circuit. If the PLL should lose lock during the operation, bit 4 of the
APPLICATIONS INFORMATION

STATUS_MFR_SPECIFIC command is asserted, and the ALERT_nn pin is pulled low. The fault can be cleared by writing a 1 to the bit. If the user does not wish to see the ALERT_nn pin assert if a PLL_FAULT occurs, the SMBALERT_MASK command can be used to prevent the alert.

If the SYNC signal is not clocking in the application, the nominal programmed frequency will control the PWM circuitry. However, if multiple parts share the SYNC_nn pins and the signal is not clocking, the parts will not be synchronized, and excess voltage ripple on the output may be present. Bit 10 of MFR_PADS will be asserted low if this condition exists.

If the PWM signal appears to be running at too high a frequency, monitor the SYNC_nn pin. Extra transitions on the falling edge will result in the PLL trying to lock on to noise versus the intended signal. Review the routing of digital control signals and minimize crosstalk to the SYNC signal to avoid this problem. Multiple LTM4683s are required to share one SYNC_nn pin in PolyPhase configurations. For other configurations, connecting the SYNC_nn pins to form a single SYNC signal is optional. If the SYNC_nn pin is shared between LTM4683s, only one LTM4683 controller can be programmed with frequency output. All the other LTM4683s should be programmed to disable the SYNC_nn output. However, their frequency should be programmed to the nominal desired value.

INPUT CURRENT SENSE AMPLIFIER

The LTM4683 input current sense amplifier can sense the supply current into the VIN01 and VIN23 power stages pins using an external sense resistor, as shown in Figure 2 Simplified Block Diagram. The RSENSE value can be programmed using the MFR_IIN_CAL_GAIN command. Kelvin sensing is recommended across the RSENSE resistor to eliminate errors. The MFR_PWM_CONFIG [6:5] sets the input current sense amplifier gain. See the MFR_PWM_CONFIG section. The IIN_OC_WARN_LIMIT command sets the value of the input current measured by the ADC in amperes, which causes a warning indicating the input current is high. The READ_IIN value will be used to determine if this limit has been exceeded. The READ_IIN command returns the input current, in Amperes, as measured across the input current sense resistor.

There is an IR voltage drop from the supply to the SVIN_nn pin due to the current flowing into the SVIN_nn pin. To compensate for this voltage drop, the MFR_RVIN will be automatically set to the 1Ω internal sense resistor in the Figure 2 Simplified Block Diagram. The LTM4683 will multiply the MFR_READ_ICHIP measurement value by this 1Ω resistor and add this voltage to the measured voltage at the SVIN_nn pin. Therefore, READ_VIN = VSVIN_PIN + (MFR_READ_ICHIP • 1Ω). The MFR_READ_ICHIP command is used to measure the internal controller current. Using the READ_PIN command allows for reading calculated input power.

PROGRAMMABLE LOOP COMPENSATION

The LTM4683 offers programmable loop compensation to optimize the transient response without hardware change. The error amplifier gain gm varies from 1.0mS to 5.76mS, and the compensation resistor RCOMPa varies from 0kΩ to 62kΩ inside the controller. Two compensation capacitors, COMPna and COMPrb, are required in the design, and the typical ratio between COMPna and COMPrb is 10. Also, see Figure 2 Simplified Block Diagram and Figure 27.

By adjusting the gm and RCOMPa only, the LTM4683 can provide a flexible Type II compensation network to optimize the loop over a wide range of output capacitors. Adjusting the gm will change the gain of the compensation over the whole frequency range without moving the pole and zero location, as shown in Figure 28.

Adjusting the RCOMP will change the pole and zero location, as shown in Figure 29. It is recommended that the user determines the appropriate value for the gm and RCOMP using the LTpowerCAD tool.

CHECKING TRANSIENT RESPONSE

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, VOUT shifts by an amount equal to ΔILOAD • ESR, where ESR is the effective
APPLICATIONS INFORMATION

Figure 27. Programmable Loop Compensation

Figure 28. Error Amp g_m Adjust

Figure 29. R_COMP Adjust

series resistance of C_OUT. ΔI_LOAD also begins to charge or discharge C_OUT generating, the feedback error signal that forces the regulator to adapt to the current change and return V_OUT to its steady-state value. During this recovery time, V_OUT can be monitored for excessive overshoot or ringing, indicating a stability problem. The availability of the COMP pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling time at this test point truly reflect the closed-loop response. Assuming a predominantly second-order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The COMPna external capacitor shown in the Typical Application circuits will provide an adequate starting point for most applications. The programmable parameters that affect loop gain are the output voltage range bit[1] of the MFR_PWM_MODE command, the current range bit[7] of the MFR_PWM_MODE command, the g_m of the PWM channel amplifier bits[7:5] of MFR_PWM_COMP, and the internal R_COMP compensation resistor bits[4:0] of MFR_PWM_COMP. Be sure to establish these settings before compensation calculation.

The COMPna series internal R_COMP/n and external C_COMP na filter sets the dominant pole-zero loop compensation. The internal R_COMP/n value can be modified (from 0Ω to 62kΩ) using bits[4:0] of the MFR_PWM_COMP command. Adjust the value of R_COMP/n to optimize transient response once the final PCB layout is done and the particular C_COMP filter capacitor and output capacitor type and value have been determined. The output capacitors must be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and COMP pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET with a resistor to ground directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a load step. The MOSFET + R_SERIES will produce output currents approximately equal to V_OUT/R_SERIES. R_SERIES values from 0.1Ω to 2Ω are valid depending on the current limit settings and the programmed output voltage. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine the phase margin. This is why it is better to look at the COMP pin signal, which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_COMP, and the bandwidth of the loop will be...
increased by decreasing $C_{COMP}$. If $R_{COMP}$ is increased by the same factor that $C_{COMP}$ is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The gain of the loop will be proportional to the transconductance of the error amplifier, $g_m$, which is set using bits[7:5] of the MFR_PWM_COMP command.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with $C_{OUT}$, causing a rapid drop in $V_{OUT}$. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and if it is driven quickly. If the ratio of $C_{LOAD}$ to $C_{OUT}$ is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately $25 \times C_{LOAD}$. Thus, a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

**PolyPhase Configuration**

When configuring a PolyPhase rail with multiple LTM4683s, the user must share the SYNC, COMP, SHARE_CLK, FAULT, and ALERT pins of these parts. Be sure to use pull-up resistors on FAULT, SHARE_CLK and ALERT. One of the part’s SYNC pins must be set to the desired switching frequency, and all other FREQUENCY_SWITCH commands must be set to External Clock. If an external oscillator is provided, set the FREQUENCY_SWITCH command to External Clock for all parts. The relative phasing of all the channels should be spaced equally. The MFR_RAIL_ADDRESS of all the devices should be set to the same value.

Multiple channels need to tie all the $V_{SENSE^n+}$ pins together, and all the $V_{SENSE^n–}$ pins together, COMP^n and $\text{COMPb}$ pins together as well. Do not assert bit[4] of MFR_CONFIG_ALL except in a PolyPhase application. See the Typical Applications section (Figure 50).

**CONNECTING THE USB TO I²C/SMBus/PMBus CONTROLLER TO THE LTM4683 IN SYSTEM**

The ADI USB-to-I²C/SMBus/PMBus adapter (DC1613A or equivalent) can be interfaced with the LTM4683 on the user’s board for programming, telemetry, and system debugging. The adapter, when used in conjunction with LTpowerPlay, provides a powerful way to debug an entire power system. Faults are quickly diagnosed using telemetry, fault status commands and the fault log. The

![Figure 30. Controller Connection](image-url)
APPLICATIONS INFORMATION

final configuration can be quickly developed and stored in the LTM4683 EEPROM. Figure 30 illustrates the application schematic for powering, programming and communication with one or more LTM4683s via the ADI I²C/ SMBus/PMBus adapter regardless of whether or not system power is present. If system power is not present, the dongle will power the LTM4683 through the V_{DD33, nn} supply pin. To initialize the part when V_{IN} is not applied, and the V_{DD33, nn} pin is powered, use global address 0x5B command 0x0D data 0x2B followed by address 0x5B command 0x0D data 0xC4. The LTM4683 can now communicate with the internal EEPROM and read the project file. To write the updated project file to the NVM, issue a STORE_USER_ALL command. When V_{IN} is applied, an MFR_RESET must be issued to allow the PWM POWER to be enabled and valid ADCs to be read.

Because of the adapter’s limited current sourcing capability, only the LTM4683s, their associated pull-up resistors, and the I²C pull-up resistors should be powered from the V_{DD33} 3.3V supply. In addition, any device sharing the I²C bus connections with the LTM4683 should not have body diodes between the SDA/SCL pins and their respective V_{DD} node because this will interfere with bus communication without system power. If V_{IN} is applied, the DC1613A will not supply the power to the LTM4683s on the board. It is recommended that the RUN n pins be held low or no voltage configuration resistors inserted to avoid providing power to the load until the part is fully configured.

The LTM4683 is fully isolated from the host PC’s ground by the DC1613A. The 3.3V from the adapter and the LTM4683 V_{DD33, nn} pin must be driven to each LTM4683 internal controller with a separate PFET. If both V_{IN} and V_{BIAS} are not on, the V_{DD33, nn} pins can be in parallel because the on-chip LDO is off. The controller’s 3.3V current limit is 100mA, but typical V_{DD33, nn} currents are under 15mA. The V_{DD33, nn} also back drive the INTVCC/ V_{BIAS} pin. Normally, this is not an issue if V_{IN} is open.

LTPowerPlay: AN INTERACTIVE GUI FOR DIGITAL POWER

The LTPowerPlay (see Figure 31) is a powerful Windows-based development environment that supports Analog Devices, Inc's digital power system management ICs, including the LTM4683. The software supports a variety of different tasks. LTPowerPlay can evaluate Analog Devices, Inc's ICs by connecting to a demo board or the user application. LTPowerPlay can also be used in an offline mode (with no hardware present) to build multiple IC configuration files that can be saved and reloaded later. LTPowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program or tweak the power system or to diagnose power issues when bring up rails. LTPowerPlay utilizes Analog Devices, Inc’s USB-to-I²C/ SMBus/PMBus adapter to communicate with one of the many potential targets, including the DC2924A, DC3082A demo boards, or a customer target system. The software also provides an automatic update feature to keep the revisions current with the latest set of device drivers and documentation.

A great deal of context-sensitive help is available with LTPowerPlay, along with several tutorial demos.

PMBus COMMUNICATION AND COMMAND PROCESSING

The LTM4683 internal controllers have a one-deep buffer to hold the last data written for each supported command before processing, as shown in Figure 32, write command data processing. When the part receives a new command from the bus, it copies the data into the write command data buffer, indicates to the internal processor that this command data needs to be fetched, and converts the command to its internal format so that it can be executed. Two distinct parallel blocks manage command buffering and command processing (fetch, convert, and execute) to ensure the last data written to any command is never lost. Command data buffering handles incoming PMBus writes by storing the command data in the write command data buffer and marking these commands for future processing. The internal processor runs in parallel and handles the sometimes slower task of fetching, converting and executing commands marked for processing. Some computationally intensive commands (e.g., timing parameters, temperatures, voltages and currents) have internal processor execution times that may be long.
Figure 31. LTpowerPlay Screen Shot

Figure 32. Write Command Data Processing
relative to PMBus timing. If the part is busy processing a command, and new command(s) arrive, execution may be delayed or processed in a different order than received. The part indicates when internal calculations are in process through bit 5 of MFR_COMMON (“calculations not pending”). When the part is busy calculating, bit 5 is cleared. When this bit is set, the part is ready for another command. An example polling loop is provided in Figure 33, which ensures that commands are processed in order while simplifying error-handling routines.

```
// wait until chip is not busy
while(!partReady)
{
  mfrCommonValue = PMBUS_READ_BYTE(0xEF);
  partReady = (mfrCommonValue & 0x68) == 0x68;
}

// now the part is ready to receive the next command
PMBUS_WRITE_WORD(0x21, 0x2000); //write VOUT_COMMAND to 2V
```

Figure 33. Example of a Command Write of VOUT_COMMAND

When the part receives a new command while busy, it will communicate this condition using standard PMBus protocol. Depending on the part configuration, it may either NACK the command or return all ones (0xFF) for reads. It may also generate a BUSY fault and ALERT notification, or stretch the SCL clock low. For more information, refer to PMBus Specification v1.1, Part II, Section 10.8.7 and SMBus v2.0, section 4.3.3. Clock stretching can be enabled by asserting bit 1 of MFR_CONFIG_ALL. Clock stretching will only occur if enabled, and the bus communication speed exceeds 100kHz.

PMBus protocols are well-accepted standards, but can make writing system-level software somewhat complex. The part provides three “hand shaking” status bits, which reduce complexity while enabling robust system-level communication.

The three hand shaking status bits are in the MFR_COMMON register. When the part is busy executing an internal operation, it will clear bit 6 of MFR_COMMON (“chip not busy”). When the part is busy specifically because it is in a transitional V_OUT state (margining hi/lo, power off/on, moving to a new output voltage set point, etc.), it will clear bit 4 of MFR_COMMON (“output not in transition”). When internal calculations are in process, the part will clear bit 5 of MFR_COMMON (“calculations not pending”). These three status bits can be polled with a PMBus read byte of the MFR_COMMON register until all three bits are set. A command immediately following the status bits being set will be accepted without NACKing or generating a BUSY fault(ALERT notification. The part can NACK commands for other reasons, however, as required by the PMBus spec (for instance, an invalid command or data). An example of a robust command write algorithm for the VOUT_COMMAND register is provided in Figure 33.

It is recommended that all command writes (write byte, write word, etc.) be preceded with a polling loop to avoid the extra complexity of dealing with busy behavior and unwanted ALERT notification. A simple way to achieve this is to create a SAFE_WRITE_BYTE() and SAFE_WRITE_WORD() subroutine. The above polling mechanism allows your software to remain clean and simple while robustly communicating with the part. For a detailed discussion of these topics and other special cases, refer to the Analog Devices Application Note section.

When communicating using bus speeds at or below 100kHz, the polling mechanism shown here provides a simple solution that ensures robust communication without clock stretching. At bus speeds in excess of 100kHz, it is strongly recommended that the part be configured to enable clock stretching. This requires a PMBus main device that supports clock stretching. System software that detects and properly recovers from the standard PMBus NACK/BUSY faults as described in the PMBus Specification v1.1, Par II, Section 10.8.7 is required to communicate. The LTM4683 is not recommended in applications with bus speeds in excess of 400kHz.

THERMAL CONSIDERATIONS AND OUTPUT CURRENT DERATING

The thermal resistances reported in the Pin Configuration section of this data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation.
APPLICATIONS INFORMATION

performed on a µModule package mounted to a hardware test board defined by JESD51-9 (“Test Boards for Area Array Surface Mount Package Thermal Measurements”). The motivation for providing these thermal coefficients is found in JESD51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may opt to use laboratory equipment and a test vehicle, such as the demo board, to predict the µModule regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance on thermal performance; instead, the derating curves provided later in this data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below.

1. $\theta_{JA}$, the thermal resistance from the junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in one cubic foot sealed enclosure. This environment is sometimes referred to as “still air”, although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.

2. $\theta_{JCbottom}$, the thermal resistance from the junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In a typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don’t generally match the user’s application.

3. $\theta_{JCtop}$, the thermal resistance from the junction to the top of the product case, is determined with nearly all component power dissipation flowing through the top of the package. As the electrical connections of a typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages, but the test conditions don’t generally match the user’s application.

4. $\theta_{JB}$, the thermal resistance from the junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured at a specified distance from the package, using a two-sided, two-layer board. This board is described in JESD51-9.

Figure 34. Graphical Representation of JESD51-12 Thermal Coefficients
APPLICATIONS INFORMATION

A graphical representation of the aforementioned thermal resistances is shown in Figure 34; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device’s total power loss (heat) thermally conduct exclusively through the top or exclusively through the bottom of the µModule package—as the standard defines for $\theta_{J\text{Top}}$ and $\theta_{J\text{Bottom}}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4683, be aware that there are multiple power devices and components dissipating power, with the consequence that the thermal resistances relative to different junctions of components or die are not exactly linear to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4683 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 and JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4683 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss, which was simulated. The outcome of this process and due diligence yields the set of derating curves provided in later sections of this data sheet, along with well-correlated JESD51-12-defined $\theta$ values provided in the Pin Configuration section of this data sheet.

The 5V, 8V, and 12V power loss curves in Figure 35, Figure 36, and Figure 37, respectively, can be used in coordination with the load current derating curves in Figure 41 through Figure 46 for calculating an approximate $\theta_{JA}$ thermal resistance for the LTM4683 with various airflow conditions and without heat sinks. These thermal resistances represent demonstrated performance of the LTM4683 on hardware, a 8-layer FR4 PCB measuring 215mm × 160mm × 1.6mm using 2oz copper on all layers. The power loss curves are taken at room temperature, and are increased with multiplicative factors of 1.35 when the junction temperature reaches 125°C. The derating curves are plotted with the LTM4683’s paralleled outputs initially sourcing up to 120A and the ambient temperature at 25°C. The output voltages are 0.4V, 0.6V and 0.7V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber, along with thermal modeling analysis. The junction temperatures are monitored while the ambient temperature is increased with and without airflow.

The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 125°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current decreases the internal module loss as the ambient temperature is increased. The monitored junction temperature of 125°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 43, the load current is derated to ~84A at ~76°C ambient with no air or heat sink, and the room temperature (25°C) power loss for this 12VIN to 0.6VOUT at 84AOUT condition is ~9.3W. A 12.56W loss is calculated by multiplying the ~9.3W room temperature loss from the 12VIN to 0.6VOUT.
APPLICATIONS INFORMATION

power loss curve at 84A (See Figure 37), with the 1.35 multiplying factor. If the 76°C ambient temperature is subtracted from the 125°C junction temperature, then the difference of °C divided by 12.56W yields a thermal resistance, $\theta_{JA}$, of -4°C/W—in good agreement with the value derived from thermal simulation shown in the Pin Configuration section. Table 10–Table 12 provide equivalent thermal resistances for 0.4V, 0.6V and 0.7V outputs with and without airflow.

Table 10. 0.4V Output

<table>
<thead>
<tr>
<th>DERATING CURVE</th>
<th>$V_{IN}$ (V)</th>
<th>POWER LOSS CURVE</th>
<th>AIRFLOW (LFM)</th>
<th>HEAT SINK</th>
<th>$\theta_{JA}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 38 to 40</td>
<td>5, 8, 12</td>
<td>Figure 35 to 37</td>
<td>0</td>
<td>None</td>
<td>4.25</td>
</tr>
<tr>
<td>Figure 38 to 40</td>
<td>5, 8, 12</td>
<td>Figure 35 to 37</td>
<td>200</td>
<td>None</td>
<td>4</td>
</tr>
<tr>
<td>Figure 38 to 40</td>
<td>5, 8, 12</td>
<td>Figure 35 to 37</td>
<td>400</td>
<td>None</td>
<td>3</td>
</tr>
</tbody>
</table>

Table 11. 0.6V Output

<table>
<thead>
<tr>
<th>DERATING CURVE</th>
<th>$V_{IN}$ (V)</th>
<th>POWER LOSS CURVE</th>
<th>AIRFLOW (LFM)</th>
<th>HEAT SINK</th>
<th>$\theta_{JA}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 41 to 43</td>
<td>5, 8, 12</td>
<td>Figure 35 to 37</td>
<td>0</td>
<td>None</td>
<td>4.25</td>
</tr>
<tr>
<td>Figure 41 to 43</td>
<td>5, 8, 12</td>
<td>Figure 35 to 37</td>
<td>200</td>
<td>None</td>
<td>4</td>
</tr>
<tr>
<td>Figure 41 to 43</td>
<td>5, 8, 12</td>
<td>Figure 35 to 37</td>
<td>400</td>
<td>None</td>
<td>3</td>
</tr>
</tbody>
</table>

Table 12. 0.7V Output

<table>
<thead>
<tr>
<th>DERATING CURVE</th>
<th>$V_{IN}$ (V)</th>
<th>POWER LOSS CURVE</th>
<th>AIRFLOW (LFM)</th>
<th>HEAT SINK</th>
<th>$\theta_{JA}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 44 to 46</td>
<td>5, 8, 12</td>
<td>Figure 35 to 37</td>
<td>0</td>
<td>None</td>
<td>4.25</td>
</tr>
<tr>
<td>Figure 44 to 46</td>
<td>5, 8, 12</td>
<td>Figure 35 to 37</td>
<td>200</td>
<td>None</td>
<td>4</td>
</tr>
<tr>
<td>Figure 44 to 46</td>
<td>5, 8, 12</td>
<td>Figure 35 to 37</td>
<td>400</td>
<td>None</td>
<td>3</td>
</tr>
</tbody>
</table>
Table 13. Single Channel Output Voltage vs Capacitor Selection, 10A to 20A Load Step with 10A/µs Slew Rate

<table>
<thead>
<tr>
<th>V&lt;sub&gt;IN&lt;/sub&gt; (V)</th>
<th>V&lt;sub&gt;OUT&lt;/sub&gt; (V)</th>
<th>I&lt;sub&gt;LM&lt;/sub&gt; RANGE</th>
<th>V&lt;sub&gt;OUT&lt;/sub&gt; RANGE</th>
<th>C&lt;sub&gt;OUT&lt;/sub&gt; (CER CAP)</th>
<th>C&lt;sub&gt;OUT&lt;/sub&gt; (BULK CAP)</th>
<th>C&lt;sub&gt;COMP&lt;/sub&gt; (µF)</th>
<th>C&lt;sub&gt;COMP&lt;/sub&gt; (nF)</th>
<th>R&lt;sub&gt;COMP&lt;/sub&gt; (kΩ)</th>
<th>E&lt;sub&gt;A&lt;/sub&gt;-g&lt;sub&gt;m&lt;/sub&gt; (mS)</th>
<th>f&lt;sub&gt;SW&lt;/sub&gt; (kHz)</th>
<th>LOAD STEP (A)</th>
<th>V&lt;sub&gt;OUT&lt;/sub&gt; DROOP (mV)</th>
<th>PK-PK DEVIATION (mV)</th>
<th>RECOVERY TIME (μs)</th>
<th>PHASE MARGIN CROSS OVER FREQ (kHz)</th>
<th>PHASE MARGIN (DEG)</th>
<th>GAIN MARGIN CROSS OVER FREQ (kHz)</th>
<th>GAIN MARGIN (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>0.3</td>
<td>High</td>
<td>Low</td>
<td>*100µF x4</td>
<td>**560µF x4</td>
<td>150</td>
<td>4.7</td>
<td>15</td>
<td>3.02</td>
<td>250</td>
<td>10 to 20</td>
<td>15</td>
<td>30</td>
<td>35</td>
<td>35</td>
<td>41</td>
<td>35</td>
<td>41</td>
</tr>
<tr>
<td>12</td>
<td>0.3</td>
<td>High</td>
<td>Low</td>
<td>*100µF x4</td>
<td>**560µF x4</td>
<td>150</td>
<td>4.7</td>
<td>9</td>
<td>3.02</td>
<td>250</td>
<td>10 to 20</td>
<td>15</td>
<td>30</td>
<td>50</td>
<td>30</td>
<td>41</td>
<td>30</td>
<td>41</td>
</tr>
<tr>
<td>5</td>
<td>0.4</td>
<td>High</td>
<td>Low</td>
<td>*100µF x4</td>
<td>**560µF x4</td>
<td>150</td>
<td>4.7</td>
<td>15</td>
<td>3.02</td>
<td>425</td>
<td>10 to 20</td>
<td>15</td>
<td>30</td>
<td>35</td>
<td>35</td>
<td>41</td>
<td>30</td>
<td>41</td>
</tr>
<tr>
<td>12</td>
<td>0.4</td>
<td>High</td>
<td>Low</td>
<td>*100µF x4</td>
<td>**560µF x4</td>
<td>150</td>
<td>4.7</td>
<td>13</td>
<td>3.02</td>
<td>250</td>
<td>10 to 20</td>
<td>20</td>
<td>40</td>
<td>45</td>
<td>28</td>
<td>62</td>
<td>28</td>
<td>62</td>
</tr>
<tr>
<td>5</td>
<td>0.5</td>
<td>High</td>
<td>Low</td>
<td>*100µF x4</td>
<td>**560µF x3</td>
<td>150</td>
<td>4.7</td>
<td>13</td>
<td>3.02</td>
<td>575</td>
<td>10 to 20</td>
<td>16</td>
<td>32</td>
<td>30</td>
<td>45</td>
<td>65</td>
<td>30</td>
<td>45</td>
</tr>
<tr>
<td>12</td>
<td>0.5</td>
<td>High</td>
<td>Low</td>
<td>*100µF x4</td>
<td>**560µF x3</td>
<td>150</td>
<td>4.7</td>
<td>13</td>
<td>3.02</td>
<td>425</td>
<td>10 to 20</td>
<td>15</td>
<td>30</td>
<td>40</td>
<td>45</td>
<td>60</td>
<td>40</td>
<td>45</td>
</tr>
<tr>
<td>5</td>
<td>0.6</td>
<td>High</td>
<td>Low</td>
<td>*100µF x4</td>
<td>**560µF x2</td>
<td>150</td>
<td>4.7</td>
<td>13</td>
<td>3.02</td>
<td>575</td>
<td>10 to 20</td>
<td>20</td>
<td>40</td>
<td>30</td>
<td>56</td>
<td>60</td>
<td>30</td>
<td>56</td>
</tr>
<tr>
<td>12</td>
<td>0.6</td>
<td>High</td>
<td>Low</td>
<td>*100µF x4</td>
<td>**560µF x2</td>
<td>150</td>
<td>4.7</td>
<td>13</td>
<td>3.02</td>
<td>425</td>
<td>10 to 20</td>
<td>13</td>
<td>26</td>
<td>35</td>
<td>54</td>
<td>56</td>
<td>26</td>
<td>54</td>
</tr>
<tr>
<td>5</td>
<td>0.7</td>
<td>High</td>
<td>Low</td>
<td>*100µF x4</td>
<td>**560µF x2</td>
<td>150</td>
<td>4.7</td>
<td>13</td>
<td>3.02</td>
<td>650</td>
<td>10 to 20</td>
<td>20</td>
<td>40</td>
<td>30</td>
<td>57</td>
<td>60</td>
<td>30</td>
<td>57</td>
</tr>
<tr>
<td>12</td>
<td>0.7</td>
<td>High</td>
<td>Low</td>
<td>*100µF x4</td>
<td>**560µF x2</td>
<td>150</td>
<td>4.7</td>
<td>13</td>
<td>3.02</td>
<td>575</td>
<td>10 to 20</td>
<td>20</td>
<td>40</td>
<td>30</td>
<td>57</td>
<td>57</td>
<td>20</td>
<td>57</td>
</tr>
</tbody>
</table>

* TDK C3225X5R0J107M, 100µF, 6.3V, X5R.
** Panasonic EEFGX0D561R, 560µF, 2.0V, 3mΩ.

These values should be check with a BODE Analyzer.
Table 14. Single Channel Output Voltage vs Capacitor Selection, All Ceramic Configuration, 10A to 20A Load Step with 10A/μs Slew Rate

| $V_{IN}$ (V) | $V_{OUT}$ (V) | $I_{UM}$ RANGE | $V_{OUT}$ RANGE | $C_{OUT}$ (CER CAP) | $C_{OUT}$ (BULK CAP) | $C_{COMP}$ (pF) | $C_{COMP}$ (nF) | $R_{COMP}$ (kΩ) | $E_{A-gm}$ (mS) | $f_{SW}$ (kHz) | LOAD STEP (A) | $V_{OUT}$ DROOP (mV) | PK-PK DEVIATION (mV) | RECOVERY TIME (μs) | PHASE MARGIN CROSS OVER FREQ (kHz) | GAIN MARGIN CROSS OVER FREQ (kHz) | PHASE MARGIN (DEG) | GAIN MARGIN (dB) | PHASE MARGIN CROSS OVER FREQ (kHz) |
|--------------|--------------|----------------|-----------------|---------------------|---------------------|-------------------|-----------------|-----------------|-----------------|-----------------|----------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| 5            | 0.3          | High           | Low             | *220μF x12         | None                | 150               | 4.7             | 8               | 3.02            | 350             | 10 to 20       | 22                  | 44                  | 50                  | 22                  | 56                  | –14                 | 85                  |
| 12           | 0.3          | High           | Low             | *220μF x12         | None                | 150               | 4.7             | 8               | 3.02            | 250             | 10 to 20       | 22                  | 44                  | 50                  | 22                  | 56                  | –14                 | 85                  |
| 5            | 0.4          | High           | Low             | *220μF x12         | None                | 150               | 4.7             | 9               | 3.02            | 350             | 10 to 20       | 20                  | 40                  | 40                  | 26                  | 58                  | –15                 | 108                 |
| 12           | 0.4          | High           | Low             | *220μF x12         | None                | 150               | 4.7             | 8               | 3.02            | 250             | 10 to 20       | 15                  | 30                  | 50                  | 22                  | 56                  | –14                 | 84                  |
| 5            | 0.5          | High           | Low             | *220μF x12         | None                | 150               | 4.7             | 13              | 3.02            | 500             | 10 to 20       | 15                  | 30                  | 40                  | 35                  | 51                  | –15                 | 121                 |
| 12           | 0.5          | High           | Low             | *220μF x12         | None                | 150               | 4.7             | 13              | 3.02            | 425             | 10 to 20       | 15                  | 30                  | 35                  | 35                  | 50                  | –13.5               | 102                 |
| 5            | 0.6          | High           | Low             | *220μF x12         | None                | 150               | 4.7             | 13              | 3.02            | 500             | 10 to 20       | 15                  | 30                  | 35                  | 35                  | 52                  | –15                 | 123                 |
| 12           | 0.6          | High           | Low             | *220μF x12         | None                | 150               | 4.7             | 13              | 3.02            | 500             | 10 to 20       | 15                  | 30                  | 35                  | 35                  | 50                  | –14                 | 106                 |
| 5            | 0.7          | High           | Low             | *220μF x12         | None                | 150               | 4.7             | 13              | 3.02            | 500             | 10 to 20       | 20                  | 40                  | 30                  | 35                  | 57                  | 60                  | –14                 | 230                 |
| 12           | 0.7          | High           | Low             | *220μF x12         | None                | 150               | 4.7             | 13              | 3.02            | 500             | 10 to 20       | 15                  | 30                  | 40                  | 35                  | 52                  | –16                 | 125                 |

*Murata GRM32EC80E227ME05L, 220μF, 2.5V, X6S.

These values should be check with a BODE Analyzer.
Table 15. Dual Connected Channels Output Voltage vs Capacitor Selection, Bulk and Ceramic Cap Configuration, 10A to 30A Load Step with 20A/µs Slew Rate

<table>
<thead>
<tr>
<th>$V_{IN}$</th>
<th>$V_{OUT}$</th>
<th>$I_{LIM}$</th>
<th>$V_{OUT}$</th>
<th>$C_{OUT}$</th>
<th>$C_{COMPb}$</th>
<th>$C_{COMPa}$</th>
<th>$R_{COMP}$</th>
<th>$E_{A GM}$</th>
<th>$f_{SW}$</th>
<th>LOAD STEP</th>
<th>$V_{OUT}$</th>
<th>PK-PK</th>
<th>RECOVERY</th>
<th>PHASE</th>
<th>GAIN</th>
<th>CROSSOVER</th>
<th>PHASE</th>
<th>GAIN</th>
<th>CROSSOVER</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V)</td>
<td>(V)</td>
<td>RANGE</td>
<td>RANGE</td>
<td>(CER CAP)</td>
<td>(BULK CAP)</td>
<td>(pF)</td>
<td>(nF)</td>
<td>(kΩ)</td>
<td>(mS)</td>
<td>(kHz)</td>
<td>(mV)</td>
<td>(mV)</td>
<td>(µs)</td>
<td>(º)</td>
<td>(dB)</td>
<td>(kHz)</td>
<td>(º)</td>
<td>(dB)</td>
<td>(kHz)</td>
</tr>
<tr>
<td>12</td>
<td>0.3</td>
<td>High</td>
<td>Low</td>
<td>*100µF 8</td>
<td>**560µF 4</td>
<td>150</td>
<td>4.7</td>
<td>8</td>
<td>2.35</td>
<td>250</td>
<td>10 to 30</td>
<td>22</td>
<td>44</td>
<td>30</td>
<td>28</td>
<td>78</td>
<td>–15</td>
<td>137</td>
<td>–10</td>
</tr>
<tr>
<td>12</td>
<td>0.4</td>
<td>High</td>
<td>Low</td>
<td>*100µF 8</td>
<td>**560µF 4</td>
<td>150</td>
<td>4.7</td>
<td>11</td>
<td>2.35</td>
<td>350</td>
<td>10 to 30</td>
<td>18</td>
<td>36</td>
<td>30</td>
<td>39</td>
<td>76</td>
<td>–10</td>
<td>169</td>
<td>–10</td>
</tr>
<tr>
<td>12</td>
<td>0.5</td>
<td>High</td>
<td>Low</td>
<td>*100µF 8</td>
<td>**560µF 4</td>
<td>150</td>
<td>4.7</td>
<td>11</td>
<td>2.35</td>
<td>425</td>
<td>10 to 30</td>
<td>20</td>
<td>40</td>
<td>25</td>
<td>40</td>
<td>78</td>
<td>–13</td>
<td>196</td>
<td>–13</td>
</tr>
<tr>
<td>12</td>
<td>0.6</td>
<td>High</td>
<td>Low</td>
<td>*100µF 8</td>
<td>**560µF 4</td>
<td>150</td>
<td>4.7</td>
<td>15</td>
<td>2.35</td>
<td>525</td>
<td>10 to 30</td>
<td>15</td>
<td>30</td>
<td>20</td>
<td>56</td>
<td>72</td>
<td>–12</td>
<td>211</td>
<td>–12</td>
</tr>
<tr>
<td>12</td>
<td>0.7</td>
<td>High</td>
<td>Low</td>
<td>*100µF 8</td>
<td>**560µF 4</td>
<td>150</td>
<td>4.7</td>
<td>15</td>
<td>2.35</td>
<td>575</td>
<td>10 to 30</td>
<td>15</td>
<td>30</td>
<td>20</td>
<td>56</td>
<td>72</td>
<td>–12</td>
<td>227</td>
<td>–12</td>
</tr>
</tbody>
</table>

*TDK C3225X5R0J107M, 100µF, 6.3V, X5R.
**Panasonic EEFGX0D561R, 560µF, 2.0V, 3mΩ.
These values should be checked with a BODE Analyzer.
Table 16. Quad Connected Channels Output Voltage vs Capacitor Selection, Bulk and Ceramic Cap Configuration, 10A to 40A Load Step with 15A/μs Slew Rate

<table>
<thead>
<tr>
<th>V&lt;sub&gt;IN&lt;/sub&gt; (V)</th>
<th>V&lt;sub&gt;OUT&lt;/sub&gt; (V)</th>
<th>I&lt;sub&gt;LIM&lt;/sub&gt; RANGE</th>
<th>V&lt;sub&gt;OUT&lt;/sub&gt; RANGE</th>
<th>C&lt;sub&gt;OUT&lt;/sub&gt; (CER CAP)</th>
<th>C&lt;sub&gt;OUT&lt;/sub&gt; (BULK CAP)</th>
<th>C&lt;sub&gt;COMPb&lt;/sub&gt; (pF)</th>
<th>C&lt;sub&gt;COMPa&lt;/sub&gt; (nF)</th>
<th>R&lt;sub&gt;COMP&lt;/sub&gt; (kΩ)</th>
<th>f&lt;sub&gt;S0&lt;/sub&gt; (MHz)</th>
<th>LOAD STEP (A)</th>
<th>V&lt;sub&gt;OUT&lt;/sub&gt; DROOP (mV)</th>
<th>PK-PK DEVIATION (mV)</th>
<th>RECOVERY TIME (μs)</th>
<th>PHASE MARGIN CROSS OVER FREQ (MHz)</th>
<th>PHASE MARGIN (DEG)</th>
<th>GAIN MARGIN CROSS OVER FREQ (kHz)</th>
<th>GAIN MARGIN (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>0.5</td>
<td>High</td>
<td>Low</td>
<td>*100μF x12</td>
<td>**560μF x4</td>
<td>220</td>
<td>2.7</td>
<td>11</td>
<td>2.35</td>
<td>425</td>
<td>10 to 40</td>
<td>14</td>
<td>28</td>
<td>20</td>
<td>55</td>
<td>64</td>
<td>–10</td>
</tr>
<tr>
<td>12</td>
<td>0.6</td>
<td>High</td>
<td>Low</td>
<td>*100μF x12</td>
<td>**560μF x4</td>
<td>220</td>
<td>2.7</td>
<td>11</td>
<td>2.35</td>
<td>500</td>
<td>10 to 40</td>
<td>13</td>
<td>26</td>
<td>20</td>
<td>56</td>
<td>66</td>
<td>–11</td>
</tr>
<tr>
<td>12</td>
<td>0.7</td>
<td>High</td>
<td>Low</td>
<td>*100μF x12</td>
<td>**560μF x4</td>
<td>220</td>
<td>2.7</td>
<td>13</td>
<td>2.35</td>
<td>575</td>
<td>10 to 40</td>
<td>13</td>
<td>26</td>
<td>20</td>
<td>70</td>
<td>68</td>
<td>–10</td>
</tr>
</tbody>
</table>

* TDK C3225X5R0J107M, 100μF, 6.3V, X5R.
** EEFGX0D561R, 560μF, 2.0V, 3mΩ.

These values should be check with a BODE Analyzer.
APPLICATIONS INFORMATION

EMI PERFORMANCE

The SWn pin provides access to the midpoint of the power MOSFETs in the LTM4683’s power stages.

Connecting an optional series RC network from SWn to GND can dampen high-frequency (~30MHz+) switch node ringing caused by parasitic inductances and capacitances in the switched-current paths. The RC network is called a snubber circuit because it dampens (or “snubs”) the resonance of the parasitics at the expense of higher power loss. To use a snubber, first choose how much power to allocate to the task and how much PCB real estate is available to implement the snubber. For example, if PCB space allows a low inductance 0.5W resistor to be used, then the capacitor in the snubber network (C_SW) is computed by Equation 7.

\[
C_{SW} = \frac{P_{SNUB}}{V_{INn(MAX)}^2 \cdot f_{SW}}
\]  

(7)

where \(V_{INn(MAX)}\) is the maximum input voltage that the input to the power stage (\(V_{INn}\)) will see in the application, and \(f_{SW}\) is the DC/DC converter’s switching frequency of operation. C_SW should be NPO, COG or X7R-type (or better) material.

The snubber resistor (\(R_{SW}\)) value is then given by Equation 8.

\[
R_{SW} = \sqrt{\frac{5nH}{C_{SW}}}
\]  

(8)

The snubber resistor should be low ESL and capable of withstanding the pulsed currents present in snubber circuits. A value between 0.7Ω and 4.2Ω is normal.

A 2.2nF snubber capacitor is a good value to start with in series with the snubber resistor to ground. The no-load input quiescent current can be monitored while selecting different RC series snubber components to get an increased power loss versus switch node ringing attenuation.

SAFETY CONSIDERATIONS

The LTM4683 modules do not provide galvanic isolation from \(V_{IN}\) to \(V_{OUT}\). There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current must be provided to protect each unit from catastrophic failure.

The fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage; thus the internal bottom MOSFET will turn on indefinitely, trying to protect the load. Under this fault condition, the input voltage will source very large currents to ground through the failed internal top MOSFET and enabled internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation. The device does support overcurrent and overtemperature protection.

LAYOUT CHECKLIST/EXAMPLE

The high integration of LTM4683 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some of the following layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including \(V_{INn}\), GND and \(V_{OUTn}\). It helps to minimize the PCB conduction loss and thermal stress.
- Place high-frequency ceramic input and output capacitors next to the \(V_{INn}\), GND and \(V_{OUTn}\) pins to minimize high-frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between the top layer and other power layers.
APPLICATIONS INFORMATION

- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4683.
- Use Kelvin sense connections across the input RSENSE resistor if input current monitoring is used.

For parallel modules, tie the $V_{OUTn}$, $V_{OSNSn+}/V_{OSNSn-}$ voltage-sense differential pair lines, $RUNn$, $COMPna$, and $COMPnb$ pins together.

- The user must share the $SYNC_{nn}$, $SHARE_CLK_{nn}$, $FAULTn$, and $ALERT_{nn}$ pins of these parts. Be sure to use pull-up resistors on $FAULTn$, $SHARE_CLK_{nn}$ and $ALERT_{nn}$.

- Bring out test points on the signal pins for monitoring. Figure 47 gives a good example of the recommended layout.

Figure 47. Recommended PCB Layout Package, Top View
Figure 48. Quad 31.25A DC/DC µModule Regulator with I²C/SMBus/PMBus Serial Interface
Figure 49. 0.6V and 0.4V Outputs at 60A with Providing I2C/SMBus/PMBus Serial Interface
Figure 50. Two Paralleled LTM4683 Producing 0.7VOUT at 250A. Integrated Power System Management Features Accessible Over 2-Wire I²C/SMBus/PMBus Serial Interface
TYPICAL APPLICATIONS

Figure 51. 0.45V at 60A and 0.7V at 60A Outputs Generated from 5V Power Input and Providing I2C/SMBus/PMBus Serial Interface
Figure 52. 6-Phase Operation Producing 0.7V at 185A, 0.6V at 30A, and 0.5V at 30A. Power System Management Features Accessible through LTM4683 Over 2-Wire I²C/SMBus/PMBus Serial Interface

Rev. 0

For more information www.analog.com
**PMBus COMMAND DETAILS**

**ADDRESSING AND WRITE PROTECT**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PAGE</td>
<td>0x00</td>
<td>Provides integration with multi-page PMBus devices.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td></td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>PAGE_PLUS_WRITE</td>
<td>0x05</td>
<td>Write a supported command directly to a PWM channel.</td>
<td>W Block</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PAGE_PLUS_READ</td>
<td>0x06</td>
<td>Read a supported command directly from a PWM channel.</td>
<td>Block</td>
<td>N</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WRITE_PROTECT</td>
<td>0x10</td>
<td>Level of protection provided by the device against accidental changes.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>MFR_ADDRESS</td>
<td>0x6E</td>
<td>Sets the 7-bit I²C address byte.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td></td>
<td>0x4F</td>
</tr>
<tr>
<td>MFR_RAIL_ADDRESS</td>
<td>0xFA</td>
<td>Common address for PolyPhase outputs to adjust common parameters.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td></td>
<td>0x80</td>
</tr>
</tbody>
</table>

**PAGE**

The PAGE command provides the ability to configure, control and monitor both PWM channels through only one physical address, either the MFR_ADDRESS or GLOBAL device address. Each PAGE contains the operating commands for one PWM channel.

Pages 0x00 and 0x01 correspond to Channel 0 and Channel 1, respectively, in this device.

ASEL_01 sets the address for Channel 0 and Channel 1, and ASEL_23 sets the address for Channel 2 and Channel 3. Each of the ASEL pins will have a different programmed address.

Setting PAGE to 0xFF applies any following paged commands to both outputs. With PAGE set to 0xFF, the LTM4683 will respond to read commands as if PAGE were set to 0x00 (Channel 0 results).

This command has one data byte.

**PAGE_PLUS_WRITE**

The PAGE_PLUS_WRITE command provides a way to set the page within a device, send a command, and then send the data for the command, all in one communication packet. Commands allowed by the present write protection level may be sent with PAGE_PLUS_WRITE.

The value stored in the PAGE command is not affected by PAGE_PLUS_WRITE. If PAGE_PLUS_WRITE is used to send a non-paged command, the Page Number byte is ignored.

This command uses the Write Block protocol. An example of the PAGE_PLUS_WRITE command with PEC sending a command with two data bytes is shown in Figure 53.

![Figure 53. Example of PAGE_PLUS_WRITE](image)

**PAGE_PLUS_READ**

The PAGE_PLUS_READ command provides the ability to set the page within a device, send a command, and then read the data returned by the command, all in one communication packet.
The value stored in the PAGE command is not affected by PAGE_PLUS_READ. If PAGE_PLUS_READ is used to access data from a non-paged command, the Page Number byte is ignored.

This command uses the process call protocol. An example of the PAGE_PLUS_READ command with PEC is shown in Figure 54.

![Figure 54. Example of PAGE_PLUS_READ](image)

NOTE: PAGE_PLUS commands cannot be nested. A PAGE_PLUS command cannot be used to read or write another PAGE_PLUS command. If this is attempted, the LTM4683 will NACK the entire PAGE_PLUS packet and issue a CML fault for Invalid/Unsupported Data.

**WRITE_PROTECT**

The WRITE_PROTECT command is used to control writing to the LTM4683 device. This command does not indicate the status of the WP pin, which is defined in the MFR_COMMON command. The WP pin takes precedence over the value of this command.

<table>
<thead>
<tr>
<th>BYTE</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x80</td>
<td>Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, and STORE_USER_ALL commands.</td>
</tr>
<tr>
<td>0x40</td>
<td>Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, STORE_USER_ALL, OPERATION and CLEAR_FAULTS command. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.</td>
</tr>
<tr>
<td>0x20</td>
<td>Disable all writes except to the WRITE_PROTECT, OPERATION, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, CLEAR_FAULTS, PAGE, ON_OFF_CONFIG, VOUT_COMMAND and STORE_USER_ALL. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.</td>
</tr>
<tr>
<td>0x10</td>
<td>Reserved, must be 0</td>
</tr>
<tr>
<td>0x08</td>
<td>Reserved, must be 0</td>
</tr>
<tr>
<td>0x04</td>
<td>Reserved, must be 0</td>
</tr>
<tr>
<td>0x02</td>
<td>Reserved, must be 0</td>
</tr>
<tr>
<td>0x01</td>
<td>Reserved, must be 0</td>
</tr>
</tbody>
</table>

Enable writes to all commands when WRITE_PROTECT is set to 0x00.

If the WP pin is high, PAGE, OPERATION, MFR_CLEAR_PEAKS, MFR_EE_UNLOCK, WRITE_PROTECT and CLEAR_FAULTS commands are supported. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.
**PMBus COMMAND DETAILS**

**MFR_ADDRESS**
The MFR_ADDRESS command byte sets the 7 bits of the PMBus subordinate address for this device.

Setting this command to a value of 0x80 disables device addressing. The GLOBAL device address, 0x5A and 0x5B, cannot be deactivated. If \( R_{CONFIG} \) is set to ignore, the ASEL\(_{nn}\) pins are still used to determine the LSB of the channel address. If the ASEL\(_01\) and ASEL\(_23\) pins are both open, the LTM4683 will use the address value stored in NVM. If the ASEL\(_{nn}\) pins are open, the LTM4683 will use the lower 4 bits of the MFR_ADDRESS value stored in NVM to construct the effective address of the part.

This command has one data byte.

**MFR_RAIL_ADDRESS**
The MFR_RAIL_ADDRESS command enables direct device address access to the PAGE-activated channel. The value of this command should be common to all devices attached to a single power supply rail.

The user should only perform command writes to this address. If a read is performed from this address and the rail devices do not respond with EXACTLY the same value, the LTM4683 will detect bus contention and may set a CML communications fault.

Setting this command to a value of 0x80 disables rail device addressing for the channel.

This command has one data byte.

**GENERAL CONFIGURATION COMMANDS**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_CHAN_CONFIG</td>
<td>0x00</td>
<td>Configuration bits that are channel-specific</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0x1D</td>
<td></td>
</tr>
<tr>
<td>MFR_CONFIG_ALL</td>
<td>0x01</td>
<td>General configuration bits</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>0x21</td>
<td></td>
</tr>
</tbody>
</table>

**MFR_CHAN_CONFIG**
General-purpose configuration command common to multiple ADI products.

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
</tr>
<tr>
<td>6</td>
<td>Reserved</td>
</tr>
<tr>
<td>5</td>
<td>Reserved</td>
</tr>
<tr>
<td>4</td>
<td>Disable ( \text{RUN Low} ). When asserted, the ( \text{RUN} ) pin is not pulsed low if commanded Off.</td>
</tr>
<tr>
<td>3</td>
<td>Enable ( \text{Short Cycle} ) recognition if this bit is set to a 1.</td>
</tr>
<tr>
<td>2</td>
<td>( \text{SHARE_CLOCK} ) control. If ( \text{SHARE_CLOCK} ) is held low, the output is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>No ( \text{FAULT ALERT} ), ( \text{ALERT} ) is not pulled low if ( \text{FAULT} ) is pulled low externally. Assert this bit if either ( \text{POWER_GOOD} ) or ( \text{VOUT_UVUF} ) are propagated on ( \text{FAULT} ).</td>
</tr>
<tr>
<td>0</td>
<td>Disables the ( \text{V_OUT} ) decay value requirement for ( \text{MFR_RETRY_TIME} ) and ( \text{t_OFF(MIN)} ) processing. When this bit is set to a 0, the output must decay to less than 12.5% of the programmed value for any action that turns off the rail, including a fault, an Off/On command, or a toggle of ( \text{RUN} ) from high to low to high.</td>
</tr>
</tbody>
</table>

This command has one data byte.
**PMBus Command Details**

A ShortCycle event occurs whenever the PWM channel is commanded back On or reactivated, after the part has been commanded Off and is processing either the TOFF_DELAY or the TOFF_FALL states. The PWM channel can be turned On/Off through the RUN pin or the PMBus OPERATION command.

If the PWM channel is reactivated during the TOFF_DELAY, the part will perform the following:

1. Immediately tri-state the PWM channel output.
2. Start the retry delay timer as specified by the t_{OFF(MIN)}.
3. After the t_{OFF(MIN)} value has expired, the PWM channel will proceed to the TON_DELAY state and the STATUS_MFR_SPECIFIC bit #1 will assert.

If the PWM channel is reactivated during the TOFF_FALL, the part will perform the following:

1. Stop ramping down the PWM channel output.
2. Immediately tri-state the PWM channel output.
3. Start the retry delay timer as specified by the t_{OFF(MIN)}.
4. After the t_{OFF(MIN)} value has expired, the PWM channel will proceed to the TON_DELAY state, and the STATUS_MFR_SPECIFIC bit #1 will assert.

If the ShortCycle event occurs and the ShortCycle MFR_CHAN_CONFIG bit is not set, the PWM channel state machine will complete its TOFF_DELAY and TOFF_FALL operations as previously commanded by the user.

**MFR_CONFIG_ALL**

General-purpose configuration command common to multiple ADI products.

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Enable fault logging</td>
</tr>
<tr>
<td>6</td>
<td>Ignore resistor configuration pins</td>
</tr>
<tr>
<td>5</td>
<td>Mask PMBus, Part II, Section 10.9.1 Violations</td>
</tr>
<tr>
<td>4</td>
<td>Disable SYNC output</td>
</tr>
<tr>
<td>3</td>
<td>Enable 255ms PMBus timeout</td>
</tr>
<tr>
<td>2</td>
<td>A valid PEC is required for PMBus writes to be accepted. If this bit is not set, the part will accept commands with invalid PEC.</td>
</tr>
<tr>
<td>1</td>
<td>Enable the use of PMBus clock stretching</td>
</tr>
<tr>
<td>0</td>
<td>Execute CLEAR_FAULTS on the rising edge of either RUN pin</td>
</tr>
</tbody>
</table>

This command has one data byte.

**ON/OFF/MARGIN**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON_OFF_CONFIG</td>
<td>0x02</td>
<td>RUN pin and PMBus bus on/off command configuration.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0x1E</td>
<td></td>
</tr>
<tr>
<td>OPERATION</td>
<td>0x01</td>
<td>Operating mode control. On/off, margin high, and margin low.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0x80</td>
<td></td>
</tr>
<tr>
<td>MFR_RESET</td>
<td>0xFD</td>
<td>Commanded reset without requiring a power-down.</td>
<td>Send Byte</td>
<td>N</td>
<td></td>
<td></td>
<td>NA</td>
<td></td>
</tr>
</tbody>
</table>
PMBus COMMAND DETAILS

ON_OFF_CONFIG

The ON_OFF_CONFIG command specifies the combination of the RUN\textsubscript{n} pin input state and PMBus commands needed to turn the PWM channel on and off.

Supported Values

<table>
<thead>
<tr>
<th>VALUE</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Margin low</td>
</tr>
<tr>
<td>0x08</td>
<td>Margin high</td>
</tr>
<tr>
<td>0x40*</td>
<td>Soft off (with sequencing)</td>
</tr>
<tr>
<td>0x00*</td>
<td>Immediate off (no sequencing)</td>
</tr>
</tbody>
</table>

Programming an unsupported ON_OFF_CONFIG value will generate a CML fault, and the command will be ignored. This command has one data byte.

OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the input from the RUN\textsubscript{n} pins. It is also used to cause the unit to set the output voltage to the upper or lower MARGIN VOL TAGEs. The unit stays in the commanded operating mode until a subsequent OPERATION command or change in the state of the RUN\textsubscript{n} pin instructs the device to change to another mode. If the part is stored in the MARGIN_LOW/HIGH state, the next RESET or POWER_ON cycle will ramp to that state. If the OPERATION command is modified, for example, On is changed to MARGIN_LOW, the output will move at a fixed slope set by the VOUT_TRANSITION_RATE. The default operation command is sequence off. If $V_{IN}$ is applied to a part with factory default programming and the VOUT_CONFIG resistor configuration pins are not installed, the outputs will be commanded off.

The part defaults to the Sequence Off state.

This command has one data byte.

Supported Values

<table>
<thead>
<tr>
<th>VALUE</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA8</td>
<td>Margin high</td>
</tr>
<tr>
<td>0x98</td>
<td>Margin low</td>
</tr>
<tr>
<td>0x80</td>
<td>On ($V_{OUT}$ back to nominal even if bit 3 of ON_OFF_CONFIG is not set).</td>
</tr>
<tr>
<td>0x40*</td>
<td>Soft off (with sequencing)</td>
</tr>
<tr>
<td>0x00*</td>
<td>Immediate off (no sequencing)</td>
</tr>
</tbody>
</table>

*Device does not respond to these commands if bit 3 of ON_OFF_CONFIG is not set.

Programming an unsupported OPERATION value will generate a CML fault, and the command will be ignored. This command has one data byte.

MFR_RESET

This command provides a means to reset the LTM4683 from the serial bus. This forces the LTM4683 to turn off both PWM channels, load the operating memory from internal EEPROM, clear all faults and then perform a soft-start of both PWM channels, if enabled.

This write-only command has no data bytes.
**PWM CONFIGURATION**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_PWM_COMP</td>
<td>0xD3</td>
<td>PWM loop compensation configuration</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0x48</td>
</tr>
<tr>
<td>MFR_PWM_MODE</td>
<td>0xD4</td>
<td>Configuration for the PWM engine.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0xC7</td>
</tr>
<tr>
<td>MFR_PWM_CONFIG</td>
<td>0xF5</td>
<td>Set numerous parameters for the DC/DC controller,</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>0x10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>including phasing.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FREQUENCY_SWITCH</td>
<td>0x33</td>
<td>Switching frequency of the controller.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>kHz</td>
<td>425 0xFB52</td>
</tr>
</tbody>
</table>

**MFR_PWM_MODE**

The MFR_PWM_MODE command sets important PWM controls for each channel.

The MFR_PWM_MODE command allows the user to program the PWM controller to use discontinuous (pulse-skipping mode), or forced continuous conduction mode.

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Use high range of I\textsubscript{LIMIT}</td>
</tr>
<tr>
<td>0b</td>
<td>Low current range</td>
</tr>
<tr>
<td>1b</td>
<td>High current range</td>
</tr>
<tr>
<td>6</td>
<td>Enable servo mode</td>
</tr>
<tr>
<td>5</td>
<td>External temperature sense:</td>
</tr>
<tr>
<td>0</td>
<td>∆V\textsubscript{BE} measurement. No reserved, ∆V\textsubscript{BE} only supported.</td>
</tr>
<tr>
<td>4</td>
<td>Page 0 Only: Use of TSNS\textsubscript{n}-Sensed Temperature Telemetry</td>
</tr>
<tr>
<td>0</td>
<td>Temperature sensed through TSNS1,3 is used to temperature-correct the current-sense information digitized by Channel 1,3's power stage.</td>
</tr>
<tr>
<td>1</td>
<td>Temperature sensed through TSNS0,2 is used to temperature-correct the current-sense information digitized by Channel 0,2's power stage.</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>V\textsubscript{OUT} range</td>
</tr>
<tr>
<td>1b</td>
<td>The maximum output voltage is 2.75V.</td>
</tr>
<tr>
<td>0b</td>
<td>The maximum output voltage is 3.6V, NOT NEEDED.</td>
</tr>
<tr>
<td>Bit[0]</td>
<td>Mode</td>
</tr>
<tr>
<td>0b</td>
<td>Discontinuous-conduction mode</td>
</tr>
<tr>
<td>1b</td>
<td>Forced continuous mode</td>
</tr>
</tbody>
</table>

Bit [7] of this command determines if the part is in the high range or low range of the I\textsubscript{OUT OC_FAULT LIMIT} command. Changing this bit value changes the PWM loop gain and compensation. This bit value should not be changed when the channel output is active. Writing this bit when the channel is active will generate a CML fault.

Bit [6] The LTM4683 will not servo while the part is Off, ramping on or ramping off. When set to one, the output servo is enabled. The output set point DAC will be slowly adjusted to minimize the difference between the READ_VOUT_ADC and the VOUT_COMMAND (or the appropriate margined value).

The LTM4683 computes temperature in °C from ∆V\textsubscript{BE} measured by the ADC at the TSNS\textsubscript{n} pin as:

\[
T = \left( G \cdot \Delta V_{BE} \cdot q/(K \cdot \ln(16)) \right) - 273.15 + O
\]

For both equations,
**PMBus COMMAND DETAILS**

G = MFR_TEMP_1_GAIN • 2^{-14}, and
O = MFR_TEMP_1_OFFSET

Bit[1] of this command determines if the part is in a high range or low voltage range. Changing this bit value changes the PWM loop gain and compensation. This bit value should not be changed when the channel output is active. Writing this bit when the channel is active will generate a CML fault.

Bit[0] determines if the PWM mode of operation is discontinuous (pulse-skipping mode), or forced continuous conduction mode. Whenever the channel is ramping on, the PWM mode will be discontinuous, regardless of the value of this bit. This command has one data byte.

**MFR_PWM_COMP**

The MFR_PWM_COMP command sets the $g_m$ of the PWM channel error amplifiers and the value of the internal $R_{COMP}$ compensation resistors. This command affects the loop gain of the PWM output, which may require modifications to the external compensation network.

<table>
<thead>
<tr>
<th>BIT [7:5]</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>000b</td>
<td>1.00</td>
</tr>
<tr>
<td>001b</td>
<td>1.68</td>
</tr>
<tr>
<td>010b</td>
<td>2.35</td>
</tr>
<tr>
<td>011b</td>
<td>3.02</td>
</tr>
<tr>
<td>100b</td>
<td>3.69</td>
</tr>
<tr>
<td>101b</td>
<td>4.36</td>
</tr>
<tr>
<td>110b</td>
<td>5.04</td>
</tr>
<tr>
<td>111b</td>
<td>5.76</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>BIT [4:0]</th>
<th>$R_{COMP}$ (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000b</td>
<td>0</td>
</tr>
<tr>
<td>00001b</td>
<td>0.25</td>
</tr>
<tr>
<td>00010b</td>
<td>0.5</td>
</tr>
<tr>
<td>00011b</td>
<td>0.75</td>
</tr>
<tr>
<td>00100b</td>
<td>1</td>
</tr>
<tr>
<td>00101b</td>
<td>1.25</td>
</tr>
<tr>
<td>00110b</td>
<td>1.5</td>
</tr>
<tr>
<td>00111b</td>
<td>1.75</td>
</tr>
<tr>
<td>01000b</td>
<td>2</td>
</tr>
<tr>
<td>01001b</td>
<td>2.5</td>
</tr>
<tr>
<td>01010b</td>
<td>3</td>
</tr>
<tr>
<td>01011b</td>
<td>3.5</td>
</tr>
<tr>
<td>01100b</td>
<td>4</td>
</tr>
<tr>
<td>01101b</td>
<td>4.5</td>
</tr>
<tr>
<td>01110b</td>
<td>5</td>
</tr>
<tr>
<td>01111b</td>
<td>5.5</td>
</tr>
<tr>
<td>10000b</td>
<td>6</td>
</tr>
<tr>
<td>10001b</td>
<td>7</td>
</tr>
</tbody>
</table>
PMBus COMMAND DETAILS

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>10010b</td>
<td>8</td>
</tr>
<tr>
<td>10011b</td>
<td>9</td>
</tr>
<tr>
<td>10100b</td>
<td>11</td>
</tr>
<tr>
<td>10101b</td>
<td>13</td>
</tr>
<tr>
<td>10110b</td>
<td>15</td>
</tr>
<tr>
<td>10111b</td>
<td>17</td>
</tr>
<tr>
<td>11000b</td>
<td>20</td>
</tr>
<tr>
<td>11001b</td>
<td>24</td>
</tr>
<tr>
<td>11010b</td>
<td>28</td>
</tr>
<tr>
<td>11011b</td>
<td>32</td>
</tr>
<tr>
<td>11100b</td>
<td>38</td>
</tr>
<tr>
<td>11101b</td>
<td>46</td>
</tr>
<tr>
<td>11110b</td>
<td>54</td>
</tr>
<tr>
<td>11111b</td>
<td>62</td>
</tr>
</tbody>
</table>

This command has one data byte.

*MFR_PWM_CONFIG*

The MFR_PWM_CONFIG command sets the switching frequency phase offset to the falling edge of the SYNC signal. The part must be in the Off state to process this command. The RUN pins must be low, or the channels must be commanded off. If either channel is in the RUN state and this command is written, the command will be NACK’d and a BUSY fault will be asserted.

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

[6:5] Input current sense gain
00b  2x gain. 0mV to 50mV range
01b  4x gain. 0mV to 25mV range
10b  8x gain. 0mV to 10mV range
11b  Reserved

4 Share Clock Enable: If this bit is 1, the SHARE_CLK pin will not be released until \( V_{IN} > V_{IN\_ON} \). The SHARE_CLK pin will be pulled low when \( V_{IN} < V_{IN\_OFF} \). If this bit is 0, the SHARE_CLK pin will not be pulled low when \( V_{IN} < V_{IN\_OFF} \) except for the initial application of \( V_{IN} \).

3 Reserved

<table>
<thead>
<tr>
<th>BIT [2:0]</th>
<th>CHANNEL 0 (DEGREES)</th>
<th>CHANNEL 1 (DEGREES)</th>
</tr>
</thead>
<tbody>
<tr>
<td>000b</td>
<td>0</td>
<td>180</td>
</tr>
<tr>
<td>001b</td>
<td>90</td>
<td>270</td>
</tr>
<tr>
<td>010b</td>
<td>0</td>
<td>240</td>
</tr>
<tr>
<td>011b</td>
<td>0</td>
<td>120</td>
</tr>
<tr>
<td>100b</td>
<td>120</td>
<td>240</td>
</tr>
<tr>
<td>101b</td>
<td>60</td>
<td>240</td>
</tr>
<tr>
<td>110b</td>
<td>120</td>
<td>300</td>
</tr>
</tbody>
</table>
The FREQUENCY_SWITCH command sets the switching frequency, in kHz, of the LTM4683.

### Supported Frequencies

<table>
<thead>
<tr>
<th>VALUE [15:0]</th>
<th>RESULTING FREQUENCY (TYP) (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000</td>
<td>External Oscillator</td>
</tr>
<tr>
<td>0xF3E8</td>
<td>250</td>
</tr>
<tr>
<td>0xFABC</td>
<td>350</td>
</tr>
<tr>
<td>0xFB52</td>
<td>425</td>
</tr>
<tr>
<td>0xFBE8</td>
<td>500</td>
</tr>
<tr>
<td>0x023F</td>
<td>575</td>
</tr>
<tr>
<td>0x028A</td>
<td>650</td>
</tr>
<tr>
<td>0x02EE</td>
<td>750</td>
</tr>
<tr>
<td>0x03E8</td>
<td>1000</td>
</tr>
</tbody>
</table>

The part must be in the Off state to process this command. The RUN pin must be low, or both channels must be commanded off. If the part is in the RUN state and this command is written, the command will be NACK’d and a BUSY fault will be asserted. When the part is commanded off, and the frequency is changed, a PLL_UNLOCK status may be detected as the PLL locks onto the new frequency.

This command has two data bytes and is formatted in Linear_5s_11s format.

### VOLTAGE

#### Input Voltage and Limits

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN_OV_FAULT_LIMIT</td>
<td>0x55</td>
<td>Input supply overvoltage fault limit.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>V</td>
<td>Y</td>
<td>15.5 0xD3E0</td>
</tr>
<tr>
<td>VIN_UV_WARN_LIMIT</td>
<td>0x58</td>
<td>Input supply undervoltage warning limit.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>V</td>
<td>Y</td>
<td>4.65 0xCA54</td>
</tr>
<tr>
<td>VIN_ON</td>
<td>0x35</td>
<td>Input voltage at which the unit should start power conversion.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>V</td>
<td>Y</td>
<td>4.75 0xCA60</td>
</tr>
<tr>
<td>VIN_OFF</td>
<td>0x36</td>
<td>Input voltage at which the unit should stop power conversion.</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>V</td>
<td>Y</td>
<td>4.50 0xCA40</td>
</tr>
<tr>
<td>MFR_ICHIP_CAL_GAIN</td>
<td>0xF7</td>
<td>The resistance value of the ( V_{IN} ) pin filter element in milliohms</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>mΩ</td>
<td>Y</td>
<td>1000 0x03E8</td>
</tr>
</tbody>
</table>

**VIN_OV_FAULT_LIMIT**

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured by the ADC, in volts, that causes an input overvoltage fault.

This command has two data bytes in Linear_5s_11s format.
**PMBus COMMAND DETAILS**

**VIN_UV_WARN_LIMIT**
The VIN_UV_WARN_LIMIT command sets the value of input voltage measured by the ADC that causes an input under-voltage warning. This warning is disabled until the input exceeds the input startup threshold value set by the VIN_ON command and the unit has been enabled. If the $V_{IN}$ voltage drops below the VIN_UV_WARN_LIMIT, the device:

- Sets the INPUT Bit Is the STATUS_WORD
- Sets the $V_{IN}$ Undervoltage Warning Bit in the STATUS_INPUT Command
- Notifies the Host by Asserting ALERT, unless Masked

**VIN_ON**
The VIN_ON command sets the input voltage, in volts, at which the unit starts power conversion. This command has two data bytes and is formatted in Linear_5s_11s format.

**VIN_OFF**
The VIN_OFF command sets the input voltage, in volts, at which the unit stops power conversion. This command has two data bytes and is formatted in Linear_5s_11s format.

**MFR_ICHIP_CAL_GAIN**
The MFR_ICHIP_CAL_GAIN command is used to set the resistance value of the $V_{IN}$ pin filter element in milliohms. (See also READ_VIN). Set MFR_RVIN equal to 0 if no filter element is used.

This command has two data bytes and is formatted in Linear_5s_11s format.

**Output Voltage and Limits**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT_MODE</td>
<td>0x20</td>
<td>Output voltage format and exponent $(2^{-12})$</td>
<td>R Byte</td>
<td>Y</td>
<td>Reg</td>
<td></td>
<td></td>
<td>$2^{-12}$ 0x14</td>
</tr>
<tr>
<td>VOUT_MAX</td>
<td>0x24</td>
<td>The upper limit on the output voltage the unit can command regardless of any other commands.</td>
<td>R/W</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>1.1V 0x119A</td>
</tr>
<tr>
<td>VOUT_OV_FAULT_LIMIT</td>
<td>0x40</td>
<td>Output overvoltage fault limit</td>
<td>R/W</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.55V 0x08CD</td>
</tr>
<tr>
<td>VOUT_OV_WARN_LIMIT</td>
<td>0x42</td>
<td>Output overvoltage warning limit</td>
<td>R/W</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.538 0x089A</td>
</tr>
<tr>
<td>VOUT_MARGIN_HIGH</td>
<td>0x25</td>
<td>Margin high output voltage set point. It must be greater than VOUT_COMMAND.</td>
<td>R/W</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.525 0x0866</td>
</tr>
<tr>
<td>VOUT_COMMAND</td>
<td>0x21</td>
<td>Nominal output voltage set point</td>
<td>R/W</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.5 0x0800</td>
</tr>
<tr>
<td>VOUT_MARGIN_LOW</td>
<td>0x26</td>
<td>Margin low output voltage set point. It must be less than VOUT_COMMAND.</td>
<td>R/W</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.475 0x079A</td>
</tr>
<tr>
<td>VOUT_UV_WARN_LIMIT</td>
<td>0x43</td>
<td>Output undervoltage warning limit</td>
<td>R/W</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.462 0x0766</td>
</tr>
<tr>
<td>VOUT_UV_FAULT_LIMIT</td>
<td>0x44</td>
<td>Output undervoltage fault limit</td>
<td>R/W</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>Y</td>
<td>0.45 0x0733</td>
</tr>
<tr>
<td>MFR_VOUT_MAX</td>
<td>0xA5</td>
<td>Maximum allowed output voltage</td>
<td>R Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td></td>
<td>2.75 0x2C00</td>
</tr>
</tbody>
</table>
**PMBus COMMAND DETAILS**

**VOUT_MODE**

The data byte for the VOUT_MODE command, used for commanding and reading output voltage, consists of a 3-bit mode (only linear format is supported) and a 5-bit parameter representing the exponent used in output voltage Read/Write commands.

This read-only command has one data byte.

**VOUT_MAX**

The VOUT_MAX command sets an upper limit on any voltage, including VOUT_MARGIN_HIGH. The unit can command regardless of any other commands or combinations. The maximum allowed value of this command is 1.0V. The maximum output voltage the LTM4683 can produce is 0.8V, including VOUT_MARGIN_HIGH. However, the VOUT_OV_FAULT_LIMIT can be commanded as high as 0.85V.

This command has two data bytes and is formatted in Linear_16u format.

**VOUT_OV_FAULT_LIMIT**

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage measured by the overvoltage supervisor comparator at the sense pins, in volts, which causes an output overvoltage fault.

If the VOUT_OV_FAULT_LIMIT is modified and the part is in the RUN state, allow 10ms after the command is modified to ensure the new value is being honored. The part indicates if it is busy making a calculation. Monitor bits 5 and 6 of MFR_COMMON. Either bit is low if the part is busy. If this wait time is not honored and the VOUT_COMMAND is modified above the old overvoltage limit, an overvoltage condition might temporarily be detected, resulting in undesirable behavior and possible damage to the switcher.

If VOUT_OV_FAULT_RESPONSE is set to OV_PULLDOWN or 0x00, the FAULT pin will not assert if VOUT_OV_FAULT is propagated. The LTM4683 will pull the TG low and assert the BG bit as soon as the overvoltage condition is detected.

This command has two data bytes and is formatted in Linear_16u format.

**VOUT_OV_WARN_LIMIT**

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage measured by the ADC at the sense pins, in volts, which causes an output voltage high warning. The MFR_VOUT_PEAK value can be used to determine if this limit has been exceeded.

In response to the VOUT_OV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT Overvoltage Warning bit in the STATUS_VOUT command
- Notifies the host by asserting ALERT pin, unless masked

This condition is detected by the ADC so the response time may be up to t\_CONVERT. This command has two data bytes and is formatted in Linear_16u format.
PMBus COMMAND DETAILS

**VOUT_MARGIN_HIGH**
The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output will be changed, in volts, when the OPERATION command is set to “Margin High”. The value should be greater than VOUT_COMMAND. The maximum guaranteed value on VOUT_MARGIN_HIGH is 0.55V.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

**VOUT_COMMAND**
The VOUT_COMMAND consists of two bytes and is used to set the output voltage, in volts. The maximum guaranteed value on VOUT is 0.8V.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

**VOUT_MARGIN_LOW**
The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output will be changed, in volts, when the OPERATION command is set to “Margin Low”. The value must be less than VOUT_COMMAND.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

**VOUT_UV_WARN_LIMIT**
The VOUT_UV_WARN_LIMIT command reads the value of the output voltage measured by the ADC at the sense pins, in volts, which causes an output voltage low warning.

In response to the VOUT_UV_WARN_LIMIT being exceeded, the device:

• Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
• Sets the VOUT bit in the STATUS_WORD
• Sets the VOUT Undervoltage Warning bit in the STATUS_VOUT command
• Notifies the host by asserting ALERT pin, unless masked

This command has two data bytes and is formatted in Linear_16u format.

**VOUT_UV_FAULT_LIMIT**
The VOUT_UV_FAULT_LIMIT command reads the value of the output voltage measured by the UV supervisor comparator at the sense pins, in volts, which causes an output undervoltage fault.

This command has two data bytes and is formatted in Linear_16u format.
**PMBus COMMAND DETAILS**

**MFR_VOUT_MAX**

The MFR_VOUT_MAX command is the maximum output voltage in volts for each channel, including VOUT_OV_FAULT_LIMIT. If the output voltages are set to a high range (Bit 1 of MFR_PWM_MODE set to 0), MFR_VOUT_MAX is 3.6V. The (Bit 6 of MFR_PWM_CONFIG set to a 0) MFR_VOUT_MAX of 3.6V is not used since the outputs are limited to 0.7V. If the output voltage is set to a low range (Bit 1 of MFR_PWM_MODE set to a 1), the MFR_VOUT_MAX is 2.75V. Entering a VOUT_COMMAND value greater than this will result in a CML fault, and the output voltage setting will be clamped to the maximum level. This will also result in Bit 3 VOUT_MAX_Warning in the STATUS_VOUT command being set.

This read-only command has 2 data bytes and is formatted in Linear_16u format.

**OUTPUT CURRENT AND LIMITS**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_IOUT_CAL_GAIN</td>
<td>0xDA</td>
<td>The ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the resistance value in mΩ.</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>mΩ</td>
<td></td>
<td>Factory Only NVM: 0.360 0xD017</td>
</tr>
<tr>
<td></td>
<td>0xF6</td>
<td>Temperature coefficient of the current sensing element</td>
<td>R/W Word</td>
<td>Y</td>
<td>CF</td>
<td></td>
<td></td>
<td>3900 0xF3C</td>
</tr>
<tr>
<td>IOUT_OC_FAULT_LIMIT</td>
<td>0x46</td>
<td>Output overcurrent fault limit</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>A</td>
<td>Y</td>
<td>40.0 0xE280</td>
</tr>
<tr>
<td>IOUT_OC_WARN_LIMIT</td>
<td>0x4A</td>
<td>Output overcurrent warning limit</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>A</td>
<td>Y</td>
<td>34.0 0xE220</td>
</tr>
</tbody>
</table>

**MFR_IOUT_CAL_GAIN**

The MFR_IOUT_CAL_GAIN command is used to set the resistance value of the current sense resistor in milliohms. (see also MFR_IOUT_CAL_GAIN_TC). The default typical value is 0.360mΩ.

This command has two data bytes and is formatted in Linear_5s_11s format.

**MFR_IOUT_CAL_GAIN_TC**

The MFR_IOUT_CAL_GAIN_TC command allows the user to program the temperature coefficient of the IOUT_CAL_GAIN sense resistor or inductor DCR in ppm/°C.

This command has two data bytes and is formatted in 16-bit 2’s complement integer ppm. $N = -32768$ to $32767 \cdot 10^{-6}$. The nominal temperature is 27°C. The IOUT_CAL_GAIN is multiplied by:

$$[1.0 + \text{MFR}_\text{IOUT}_\text{CAL_GAIN}_\text{TC} \cdot (\text{READ_TEMPERATURE}_1-27)].$$

DCR sensing will have a typical value of 3900.

The IOUT_CAL_GAIN and MFR_IOUT_CAL_GAIN_TC impact all current parameters, including: READ_IOUT, MFR_IOUT_PEAK, IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT.
The IOUT_OC_FAULT_LIMIT command sets the value of the peak output current limit, in Amperes. When the controller is in the current limit, the overcurrent detector will indicate an overcurrent fault condition. The following table lists the programmable peak output current limit value in mV between ISENSE⁺ and ISENSE⁻. The actual value of the current limit is (ISENSE⁺ – ISENSE⁻)/IOUT_CAL_GAIN in Amperes.

Based on Peak-to-Peak Inductor Current = 50% of 30A for Worse Case, These are Approximates, So use Guardband and Check.

<table>
<thead>
<tr>
<th>MFR_PWM_MODE[7] = 1</th>
<th>~Iₚ (A)</th>
<th>~IOUT (A)</th>
<th>MFR_PWM_MODE[7] = 0</th>
<th>~Iₚ (A)</th>
<th>~IOUT (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIGH CURRENT RANGE (mV)</td>
<td></td>
<td></td>
<td>LOW CURRENT RANGE (mV)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17.73</td>
<td>49.95</td>
<td>41.75</td>
<td>9.85</td>
<td>27.36</td>
<td>19.50</td>
</tr>
<tr>
<td>18.86</td>
<td>52.38</td>
<td>44.88</td>
<td>10.48</td>
<td>29.11</td>
<td>21.61</td>
</tr>
<tr>
<td>20.42</td>
<td>NA</td>
<td>NA</td>
<td>11.34</td>
<td>31.5</td>
<td>24</td>
</tr>
<tr>
<td>21.14</td>
<td>NA</td>
<td>NA</td>
<td>11.74</td>
<td>32.61</td>
<td>25.11</td>
</tr>
<tr>
<td>22.27</td>
<td>NA</td>
<td>NA</td>
<td>12.37</td>
<td>34.36</td>
<td>28.86</td>
</tr>
<tr>
<td>23.41</td>
<td>NA</td>
<td>NA</td>
<td>13.01</td>
<td>36.13</td>
<td>28.63</td>
</tr>
<tr>
<td>24.55</td>
<td>NA</td>
<td>NA</td>
<td>13.64</td>
<td>37.88</td>
<td>30.38</td>
</tr>
</tbody>
</table>

NOTE: This is the peak of the current waveform. The READ_IOUT command returns the average current. The peak output current limits are adjusted with temperature based on the MFR_IOUT_CAL_GAIN_TC using the equation:

\[ \text{Peak Current Limit} = \text{IOUT_CAL_GAIN} \times (1 + \text{MFR_IOUT_CAL_GAIN_TC} \times (\text{READ_TEMPERATURE}_1-27.0)) \]

The LTM4683 automatically convert currents to the appropriate internal bit value.

The IOUT range is set with bit 7 of the MFR_PWM_MODE command.
The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.
If the IOUT_OC_FAULT_LIMIT is exceeded, the device:

- Sets the IOUT bit in the STATUS word
- Sets the IOUT Overcurrent fault bit in the STATUS_IOUT
- Notifies the host by asserting ALERT, unless masked

This command has two data bytes and is formatted in Linear_5s_11s format.
**PMBus COMMAND DETAILS**

**IOUT_OC_WARN_LIMIT**
This command sets the value of the output current measured by the ADC that causes an output overcurrent warning in Amperes. The READ_IOUT value will be used to determine if this limit has been exceeded.

In response to the IOUT_OC_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT Overcurrent Warning bit in the STATUS_IOUT command
- Notifies the host by asserting ALERT pin, unless masked

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

This command has two data bytes and is formatted in Linear_5s_11s format.

### Input Current and Limits

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_IIN_CAL_GAIN</td>
<td>0xE8</td>
<td>The resistance value of the input current sense element in mΩ.</td>
<td>R/W Word</td>
<td>L11</td>
<td>mΩ</td>
<td>Y</td>
<td>1.000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0E010</td>
</tr>
</tbody>
</table>

**MFR_IIN_CAL_GAIN**
The MFR_IIN_CAL_GAIN command is used to set the resistance value of the input current sense resistor in milliohms. (see also READ_IIN).

This command has two data bytes and is formatted in Linear_5s_11s format.

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>IIN_OC_WARN_LIMIT</td>
<td>0x5D</td>
<td>Input overcurrent warning limit</td>
<td>R/W Word</td>
<td>N</td>
<td>L11</td>
<td>A</td>
<td>Y</td>
<td>10.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xD280</td>
</tr>
</tbody>
</table>

**IIN_OC_WARN_LIMIT**
The IIN_OC_WARN_LIMIT command sets the value of the input current measured by the ADC, in amperes, which causes a warning indicating the input current is high. The READ_IIN value will be used to determine if this limit has been exceeded.

In response to the IIN_OC_WARN_LIMIT being exceeded, the device:

- Sets the OTHER bit in the STATUS_BYTE
- Sets the INPUT bit in the upper byte of the STATUS_WORD
- Sets the IIN Overcurrent Warning bit[1] in the STATUS_INPUT command
- Notifies the host by asserting the ALERT pin

This command has two data bytes and is formatted in Linear_5s_11s format.
**PMBus COMMAND DETAILS**

**TEMPERATURE**

### Power Stage DCR Temperature Calibration

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_TEMP_1_GAIN</td>
<td>0xF8</td>
<td>Sets the slope of the external temperature sensor.</td>
<td>R/W Word</td>
<td>Y</td>
<td>CF</td>
<td>Y</td>
<td>Y</td>
<td>0.995 0x3FAE</td>
</tr>
<tr>
<td>MFR_TEMP_1_OFFSET</td>
<td>0xF9</td>
<td>Sets the offset of the external temperature sensor.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>C</td>
<td>Y</td>
<td>0.0 0x8000</td>
</tr>
</tbody>
</table>

*MFR_TEMP_1_GAIN*

The MFR_TEMP_1_GAIN command will modify the slope of the power stage sensor to account for non-idealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in 16-bit 2’s complement integer. The effective gain adjustment is $N \cdot 2^{-14}$. The nominal value is $N = 8192$ to $32767$.

*MFR_TEMP_1_OFFSET*

The MFR_TEMP_1_OFFSET command will modify the offset of the power stage temperature sensor to account for non-idealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in Linear_5s_11s format. The part starts the calibration with a $-273.15$, so the default adjustment is zero.

### Power Stage Temperature Limits

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>OT_FAULT_LIMIT</td>
<td>0x4F</td>
<td>Power stage overtemperature fault limit.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>C</td>
<td>Y</td>
<td>128.0 0xF200</td>
</tr>
<tr>
<td>OT_WARN_LIMIT</td>
<td>0x51</td>
<td>Power stage overtemperature warning limit.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>C</td>
<td>Y</td>
<td>125.0 0xEBE8</td>
</tr>
<tr>
<td>UT_FAULT_LIMIT</td>
<td>0x53</td>
<td>Power stage undertemperature fault limit.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>C</td>
<td>Y</td>
<td>-45.0 0xE530</td>
</tr>
</tbody>
</table>

*OT_FAULT_LIMIT*

The OT_FAULT_LIMIT command sets the value of the power stage temperature measured by the ADC, in degrees Celsius, which causes an overtemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

This command has two data bytes and is formatted in Linear_5s_11s format.

*OT_WARN_LIMIT*

The OT_WARN_LIMIT command sets the value of the power stage temperature measured by the ADC, in degrees Celsius, which causes an overtemperature warning. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.
**PMBus COMMAND DETAILS**

In response to the OT_WARN_LIMIT being exceeded, the device:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the Overtemperature Warning bit in the STATUS_TEMPERATURE command
- Notifies the host by asserting the ALERT pin, unless masked

This command has two data bytes and is formatted in Linear_5s_11s format.

**UT_FAULT_LIMIT**

The UT_FAULT_LIMIT command sets the value of the power stage temperature measured by the ADC, in degrees Celsius, which causes an undertemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

**NOTE:** If the temp sensors are not installed, the UT_FAULT_LIMIT can be set to $-275^\circ C$ and the UT_FAULT_LIMIT response set to ignore to avoid ALERT being asserted.

This command has two data bytes and is formatted in Linear_5s_11s format.

**TIMING**

**Timing—On Sequence/Ramp**

<table>
<thead>
<tr>
<th>COMMAND_NAME</th>
<th>CMD_CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TON_DELAY</td>
<td>0x60</td>
<td>Time from RUN and/or Operation on to output rail turn-on.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>0.0</td>
</tr>
<tr>
<td>TON_RISE</td>
<td>0x61</td>
<td>Time from when the output starts to rise until the output voltage reaches the $V_{OUT}$ commanded value.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>3.0</td>
</tr>
<tr>
<td>TON_MAX_FAULT_LIMIT</td>
<td>0x62</td>
<td>Maximum time from the start of TON_RISE for $V_{OUT}$ to cross the $V_{OUT_UV_FAULT_LIMIT}$.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>5.0</td>
</tr>
<tr>
<td>VOUT_TRANSITION_RATE</td>
<td>0x27</td>
<td>Rate the output changes when $V_{OUT}$ is commanded to a new value.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>V/ms</td>
<td>Y</td>
<td>0.250</td>
</tr>
</tbody>
</table>

**TON_DELAY**

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received until the output voltage starts to rise. Values from 0ms to 83 seconds are valid. The resulting turn-on delay will have a typical delay of 270µs for TON_DELAY = 0 and an uncertainty of ±50µs for all values of TON_DELAY.

This command has two data bytes and is formatted in Linear_5s_11s format.

**TON_RISE**

The TON_RISE command sets the time, in milliseconds, from the time the output starts to rise to the time the output enters the regulation band. Values from 0 to 1.3 seconds are valid. The part will be in discontinuous mode during TON_RISE events. If TON_RISE is less than 0.25ms, the LTM4683 digital slope will be bypassed, and the output voltage transition will only be controlled by the analog performance of the PWM switcher. The number of steps in TON_RISE is equal to TON_RISE (in ms)/0.1ms with an uncertainty of ±0.1ms.

This command has two data bytes and is formatted in Linear_5s_11s format.
**PMBus COMMAND DETAILS**

**TON_MAX_FAULT_LIMIT**

The TON_MAX_FAULT_LIMIT command sets the value, in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit.

A data value of 0ms means there is no limit, and the unit can attempt to bring up the output voltage indefinitely. The maximum limit is 83 seconds.

This command has two data bytes and is formatted in Linear_5s_11s format.

**VOUT_TRANSITION_RATE**

When a PMBus device receives either a VOUT_COMMAND or OPERATION (Margin High, Margin Low) that causes the output voltage to change, this command sets the rate in V/ms at which the output voltage changes. The commanded rate of change does not apply when the unit is commanded On or Off. The maximum allowed slope is 4V/ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

**Timing—Off Sequence/Ramp**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOFF_DELAY</td>
<td>0x64</td>
<td>Time from RUN and/or Operation off to the start of TOFF_FALL ramp.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>0.0 0x8000</td>
</tr>
<tr>
<td>TOFF_FALL</td>
<td>0x65</td>
<td>Time from when the output starts to fall until the output reaches zero volts.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>3.0 0xC300</td>
</tr>
<tr>
<td>TOFF_MAX_WARN_LIMIT</td>
<td>0x66</td>
<td>Maximum allowed time, after TOFF_FALL completed, for the unit to decay below 12.5%.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>0 0x8000</td>
</tr>
</tbody>
</table>

**TOFF_DELAY**

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received until the output voltage starts to fall. Values from 0 to 83 seconds are valid. The resulting turn-off delay will have a typical delay of 270µs for TOFF_DELAY = 0 and an uncertainty of ±50µs for all values of TOFF_DELAY. TOFF_DELAY is not applied when a fault event occurs.

This command has two data bytes and is formatted in Linear_5s_11s format.

**TOFF_FALL**

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-off delay time until the output voltage is commanded to zero. It is the ramp time of the VOUT_DAC. When the VOUT_DAC is zero, the PWM output will be set to a high impedance state.

The part will maintain the mode of operation programmed. For defined TOFF_FALL times, the user should set the part to continuous conduction mode. Loading the max value indicates that the part will ramp down at the slowest possible rate. The minimum supported fall time is 0.25ms. A value less than 0.25ms will result in a 0.25ms ramp. The maximum fall time is 1.3 seconds. The number of steps in TOFF_FALL is equal to TOFF_FALL (in ms)/0.1ms with an uncertainty of ±0.1ms.

In discontinuous conduction mode, the controller will not draw current from the load, and the fall time will be set by the output capacitance and load current.

This command has two data bytes and is formatted in Linear_5s_11s format.
**PMBus COMMAND DETAILS**

**TOFF_MAX_WARN_LIMIT**

The TOFF_MAX_WARN_LIMIT command sets the value, in milliseconds, on how long the output voltage exceeds 12.5% of the programmed voltage before a warning is asserted. The output is considered off when the V\text{OUT} voltage is less than 12.5% of the programmed V\text{OUT}\_COMMAND value. The calculation begins after TOFF_FALL is complete.

A data value of 0ms means there is no limit, and the output voltage exceeds 12.5% of the programmed voltage indefinitely. Other than 0, values from 120ms to 524 seconds are valid.

This command has two data bytes and is formatted in Linear_5s_11s format.

**Precondition for Restart**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_RESTART_DELAY</td>
<td>0xDC</td>
<td>Minimum time the RUN pin is held low by the LTM4683.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>150</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xF258</td>
</tr>
</tbody>
</table>

**MFR\_RESTART\_DELAY**

This command specifies the minimum RUN off time in milliseconds. This device will pull the RUN pin low for this length of time once a falling edge of RUN has been detected. The minimum recommended value is 136ms.

NOTE: The restart delay is different from the retry delay. The restart delay pulls RUN low for the specified time, after which a standard start-up sequence is initiated. The minimum restart delay should be equal to TOFF\_DELAY + TOFF\_FALL + 136ms. Valid values are from 136ms to 65.52 seconds in 16ms increments. To ensure a minimum off time, set the MFR\_RESTART\_DELAY 16ms longer than the desired time. The output rail can be off longer than the MFR\_RESTART\_DELAY after the RUN pin is pulled high if the output decay bit 0 is enabled in MFR\_CHAN\_CONFIG and the output takes a long time to decay below 12.5% of the programmed value.

This command has two data bytes and is formatted in Linear_5s_11s format.

**FAULT RESPONSE**

**Fault Responses All Faults**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_RETRY_DELAY</td>
<td>0xDB</td>
<td>Retry interval during FAULT retry mode.</td>
<td>R/W Word</td>
<td>Y</td>
<td>L11</td>
<td>ms</td>
<td>Y</td>
<td>250</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xF3E8</td>
</tr>
</tbody>
</table>

**MFR\_RETRY\_DELAY**

This command sets the time in milliseconds between retries if the fault response is to retry the controller at specified intervals. This command value is used for all fault responses that require retry. The retry time starts once the fault has been detected by the offending channel. Valid values are from 120ms to 83.88 seconds in 10\mu s increments.

NOTE: The retry delay time is determined by the length of the MFR\_RETRY\_DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR\_RETRY\_DELAY command by asserting bit 0 of MFR\_CHAN\_CONFIG.

This command has two data bytes and is formatted in Linear_5s_11s format.
Fault Responses Input Voltage

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN_OV_FAULT_RESPONSE</td>
<td>0x56</td>
<td>Action to be taken by the device when an input supply overvoltage fault is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>Y</td>
<td>0x80</td>
</tr>
</tbody>
</table>

**VIN_OV_FAULT_RESPONSE**

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. The data byte is in the format as shown in Table 21.

The device also:
- Sets the NONE_OF_THE ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD
- Sets the VIN Overvoltage Fault bit in the STATUS_INPUT command
- Notifies the host by asserting ALERT pin, unless masked

This command has one data byte.

Fault Responses Output Voltage

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT_OV_FAULT_RESPONSE</td>
<td>0x41</td>
<td>Action to be taken by the device when an output overvoltage fault is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>Y</td>
<td>0xB8</td>
</tr>
<tr>
<td>VOUT_UV_FAULT_RESPONSE</td>
<td>0x45</td>
<td>Action to be taken by the device when an output undervoltage fault is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>Y</td>
<td>0xB8</td>
</tr>
<tr>
<td>TON_MAX_FAULT_RESPONSE</td>
<td>0x63</td>
<td>Action to be taken by the device when a TON_MAX_FAULT event is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>Y</td>
<td>0xB8</td>
</tr>
</tbody>
</table>

**VOUT_OV_FAULT_RESPONSE**

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. The data byte is in the format given in Table 17.

The device also:
- Sets the VOUT_OV bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT Overvoltage Fault bit in the STATUS_VOUT command
- Notifies the host by asserting ALERT pin, unless masked

The only values recognized for this command are:
- 0x00 Part performs OV pull down only, or OV_PULLDOWN.
- 0x80 The device shuts down (disables the output), and the unit does not attempt to retry. (PMBus, Part II, Section 10.7).
**PMBus COMMAND DETAILS**

0xB8  The device shuts down (disables the output) and device attempts to retry continuously, without limitation, until it is commanded Off (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.

0x4n  The device shuts down, and the unit does not attempt to retry. The output remains disabled until the part is commanded Off, then On, or the RUN pin is asserted low, then high or RESET through the command or removal of $V_{IN}$. The overvoltage fault must remain active for a period of $n \times 10\mu s$, where $n$ is a value from 0 to 7.

0x78n  The device shuts down, and the unit attempts to retry continuously until either the fault condition is cleared or the part is commanded Off, then On or the RUN pin is asserted low, then high or RESET through the command or removal of $V_{IN}$. The overvoltage fault must remain active for a period of $n \times 10\mu s$, where $n$ is a value from 0 to 7.

Any other value will result in a CML fault, and the write will be ignored.

This command has one data byte.

**Table 17. VOUT_OV_FAULT_RESPONSE Data Byte Contents**

<table>
<thead>
<tr>
<th>BITS</th>
<th>DESCRIPTION</th>
<th>VALUE</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:6</td>
<td>Response</td>
<td>00</td>
<td>Part performs OV pull-down only or OV_PULLDOWN. (i.e., turns off the top MOSFET and turns on lower MOSFET while $V_{OUT}$ is $&gt; V_{OUT_OV_FAULT}$).</td>
</tr>
<tr>
<td></td>
<td>For all values of bits [7:6], the LTM4683:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Sets the corresponding fault bit in the status commands and</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Notifies the host by asserting ALERT pin, unless masked.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>The fault bit, once set, is cleared only when one or more of the</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>following events occurs:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• The device receives a CLEAR_FAULTS command,</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• The output is commanded through the RUN pin, the OPERATION command, or</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>the combined action of the RUN pin and OPERATION command, to turn off and</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>then to turn back on, or</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Bias power is removed and reapplied to the LTM4683.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>01</td>
<td>The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
<td>Not supported. Writing this value will generate a CML fault.</td>
</tr>
<tr>
<td>5:3</td>
<td>Retry Setting</td>
<td>000</td>
<td>The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>111</td>
<td>The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. NOTE: The retry interval is set by the MFR_RETRY_DELAY command.</td>
</tr>
<tr>
<td>2:0</td>
<td>Delay Time</td>
<td>000-111</td>
<td>The delay time in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. Only valid for deglitched off state.</td>
</tr>
</tbody>
</table>

**VOUT_UV_FAULT_RESPONSE**

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output undervoltage fault. The data byte is in the format as shown in Table 18.

The device also:

• Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE

• Sets the VOUT bit in the STATUS_Word

• Sets the VOUT undervoltage fault bit in the STATUS_VOUT command

• Notifies the host by asserting ALERT pin, unless masked

For more information [www.analog.com](http://www.analog.com)
The UV fault and warn are masked until the following criteria are achieved:

1. The TON_MAX_FAULT_LIMIT has been reached.
2. The TON_DELAY sequence has been completed.
3. The TON_RISE sequence has been completed.
4. The VOUT_UV_FAULT_LIMIT threshold has been reached.
5. The IOUT_OC_FAULT_LIMIT is not present.

The UV fault and warning are masked whenever the channel is not active.

The UV fault and warning are masked during TON_RISE and TOFF_FALL sequencing.

This command has one data byte.

### Table 18. VOUT_UV_FAULT_RESPONSE Data Byte Contents

<table>
<thead>
<tr>
<th>BITS</th>
<th>DESCRIPTION</th>
<th>VALUE</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:6</td>
<td>Response</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>For all values of bits [7:6], the LTM4683:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Sets the corresponding fault bit in the status commands and</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Notifies the host by asserting ALERT pin, unless masked.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>The fault bit, once set, is cleared only when one or more of the</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>following events occurs:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• The device receives a CLEAR_FAULTS command,</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• The output is commanded through the RUN pin, the OPERATION</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>command, or the combined action of the RUN pin and</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OPERATION command, to turn off and then to turn back on, or</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• The device receives a RESTORE_USER_ALL command,</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• The device receives a MFR_RESET command,</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• The device supply power is cycled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>00</td>
<td>The PMBus device continues operation without interruption. (Ignores the fault functionally)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01</td>
<td>The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
<td>Not supported. Writing this value will generate a CML fault.</td>
</tr>
<tr>
<td>5:3</td>
<td>Retry Setting</td>
<td>000</td>
<td>The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>111</td>
<td>The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. NOTE: The retry interval is set by the MFR_RETY_DELAY command.</td>
</tr>
<tr>
<td>2:0</td>
<td>Delay Time</td>
<td>000-111</td>
<td>The delay time in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. Only valid for deglitched off state.</td>
</tr>
</tbody>
</table>
**PMBus COMMAND DETAILS**

*TON_MAX_FAULT_RESPONSE*

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to a TON_MAX fault. The data byte is in the format as shown in Table 21.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the TON_MAX_FAULT bit in the STATUS_VOUT command
- Notifies the host by asserting ALERT pin, unless masked

A value of 0 disables the TON_MAX_FAULT_RESPONSE. It is not recommended to use 0.

**NOTE:** The PWM channel remains in discontinuous-conduction mode until the TON_MAX_FAULT_LIMIT has been exceeded.

This command has one data byte.

**Fault Responses Output Current**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOUT_OC_FAULT_RESPONSE</td>
<td>0x47</td>
<td>Action to be taken by the device when an output overcurrent fault is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>Y</td>
<td>0x00</td>
</tr>
</tbody>
</table>

*IOUT_OC_FAULT_RESPONSE*

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an output overcurrent fault. The data byte is in the format as shown in Table 19.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the IOUT_OC bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT Overcurrent Fault bit in the STATUS_IOUT command
- Notifies the host by asserting ALERT pin, unless masked

This command has one data byte.
## PMBus Command Details

### Table 19. IOUT_OC_FAULT_RESPONSE Data Byte Contents

<table>
<thead>
<tr>
<th>BITS</th>
<th>DESCRIPTION</th>
<th>VALUE</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:6</td>
<td>Response</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>For all values of bits [7:6], the LTM4683:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Sets the corresponding fault bit in the status commands and</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Notifies the host by asserting ALERT pin, unless masked.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>The fault bit, once set, is cleared only when one or more of the following events occurs:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• The device receives a CLEAR_FAULTS command,</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• The device receives a RESTORE_USER_ALL command,</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• The device receives a MFR_RESET command,</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• The device supply power is cycled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5:3</td>
<td>Retry Setting</td>
<td>000</td>
<td>The unit does not attempt to restart. The output remains disabled until the fault is cleared by cycling the RUN pin or removing bias power.</td>
</tr>
<tr>
<td></td>
<td>111</td>
<td>The device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. <strong>NOTE:</strong> The retry interval is set by the MFR_RETRY_DELAY command.</td>
<td></td>
</tr>
<tr>
<td>2:0</td>
<td>Delay Time</td>
<td>000-111</td>
<td>The number of delay time units in 16ms increments. This delay time is used to determine the amount of time a unit is to continue operating after a fault is detected before shutting down. Only valid for deglitched off response.</td>
</tr>
</tbody>
</table>

### Fault Responses IC Temperature

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_OT_FAULT_RESPONSE</td>
<td>0xD6</td>
<td>Action to be taken by the device when an internal overtemperature fault is detected.</td>
<td>R Byte</td>
<td>N</td>
<td>Reg</td>
<td></td>
<td></td>
<td>0xC0</td>
</tr>
</tbody>
</table>

**MFR_OT_FAULT_RESPONSE**

The MFR_OT_FAULT_RESPONSE command byte instructs the device on what action to take in response to an internal overtemperature fault. The data byte is in the format as shown in Table 20.

The LTM4683 also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the MFR bit in the STATUS_WORD, and
- Sets the Overtemperature Fault bit in the STATUS_MFR_SPECIFIC command
- Notifies the host by asserting ALERT pin, unless masked

This command has one data byte.
PMBus COMMAND DETAILS

Table 20. Data Byte Contents MFR_OT_FAULT_RESPONSE

<table>
<thead>
<tr>
<th>BITS</th>
<th>DESCRIPTION</th>
<th>VALUE</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:6</td>
<td>Response</td>
<td>00</td>
<td>Not supported. Writing this value will generate a CML fault.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01</td>
<td>Not supported. Writing this value will generate a CML fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
<td>The device’s output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.</td>
</tr>
<tr>
<td>5:3</td>
<td>Retry Setting</td>
<td>000</td>
<td>The unit does not attempt to restart. The output remains disabled until the fault is cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>001-111</td>
<td>Not supported. Writing this value will generate a CML fault.</td>
</tr>
<tr>
<td>2:0</td>
<td>Delay Time</td>
<td>XXX</td>
<td>Not supported. Value ignored</td>
</tr>
</tbody>
</table>

Fault Responses External Temperature

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>OT_FAULT_RESPONSE</td>
<td>0x50</td>
<td>Action to be taken by the device when an external overtemperature fault is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0xB8</td>
<td></td>
</tr>
<tr>
<td>UT_FAULT_RESPONSE</td>
<td>0x54</td>
<td>Action to be taken by the device when an external undertemperature fault is detected.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0xB8</td>
<td></td>
</tr>
</tbody>
</table>

**OT_FAULT_RESPONSE**

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an external overtemperature fault on the external temp sensors. The data byte is in the format as shown in Table 21.

The device also:
- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the Overtemperature Fault bit in the STATUS_TEMPERATURE command
- Notifies the host by asserting ALERT pin, unless masked

This command has one data byte.

**UT_FAULT_RESPONSE**

The UT_FAULT_RESPONSE command instructs the device on what action to take in response to an external undertemperature fault on the external temp sensors. The data byte is in the format as shown in Table 15.

The device also:
- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the Undertemperature Fault bit in the STATUS_TEMPERATURE command, and
- Notifies the host by asserting ALERT pin, unless masked
PMBus COMMAND DETAILS

This condition is detected by the ADC so the response time may be up to $t_{\text{convert}}$.

This command has one data byte.

Table 21. Data Byte Contents: TON_MAX_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE, OT_FAULT_RESPONSE, UT_FAULT_RESPONSE

<table>
<thead>
<tr>
<th>BITS</th>
<th>DESCRIPTION</th>
<th>VALUE</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:6</td>
<td>Response</td>
<td>00</td>
<td>The PMBus device continues operation without interruption.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01</td>
<td>Not supported. Writing this value will generate a CML fault.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
<td>Not supported. Writing this value will generate a CML fault.</td>
</tr>
<tr>
<td>5:3</td>
<td>Retry Setting</td>
<td>000</td>
<td>The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>111</td>
<td>The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. NOTE: The retry interval is set by the MFR_RETRY_DELAY command.</td>
</tr>
<tr>
<td>2:0</td>
<td>Delay Time</td>
<td>XXX</td>
<td>Not supported. Values ignored</td>
</tr>
</tbody>
</table>

FAULT SHARING

Fault Sharing Propagation

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_FAULT_PROPAGATE</td>
<td>0x0D2</td>
<td>Configuration that determines which faults are propagated to the FAULT pins.</td>
<td>R/W Word</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td></td>
<td>0x6993</td>
</tr>
</tbody>
</table>

MFR_FAULT_PROPAGATE

The MFR_FAULT_PROPAGATE command enables the faults that can cause the FAULT$n$ pin to assert low. The command is formatted as shown in Table 22. Faults can only be propagated to the FAULT$n$ pin if they are programmed to respond to faults.

This command has two data bytes.
### Table 22. FAULTn Propagate Fault Configuration

The FAULT0 and FAULT1 pins are designed to provide electrical notification of selected events to the user. Some of these events are common to both output channels. Others are specific to an output channel. They can also be used to share faults between channels.

<table>
<thead>
<tr>
<th>BIT(S)</th>
<th>SYMBOL</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>B[15]</td>
<td>VOUT disabled while not decayed.</td>
<td>This is used in a PolyPhase configuration when bit 0 of the MFR_CHAN_CONFIG_LTM4683 is a zero. If the channel is turned off, by toggling the RUN pin, or commanding the part OFF, and then the RUN is reasserted, or the part is commanded back on before the output has decayed, VOUT will not restart until the 12.5% decay is honored. The FAULT pin is asserted during this condition if bit 15 is asserted.</td>
</tr>
<tr>
<td>B[14]</td>
<td>Mfr_fault_propagate_short_CMD_cycle</td>
<td>0: No action 1: Asserts low if commanded off then on before the output has sequenced off. Re-asserts high if OFF(MIN) after sequence off.</td>
</tr>
<tr>
<td>b[13]</td>
<td>Mfr_fault_propagate_ton_max_fault</td>
<td>0: No action if a TON_MAX_FAULT fault is asserted 1: Associated output will be asserted low if a TON_MAX_FAULT fault is asserted FAULT0 is associated with page 0 TON_MAX_FAULT faults FAULT1 is associated with page 1 TON_MAX_FAULT faults</td>
</tr>
<tr>
<td>b[12]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>b[11]</td>
<td>Mfr_fault0_propagate_int_ot, Mfr_fault1_propagate_int_ot</td>
<td>0: No action if the MFR_OT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the MFR_OT_FAULT_LIMIT fault is asserted</td>
</tr>
<tr>
<td>b[10]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>b[9]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>b[8]</td>
<td>Mfr_fault0_propagate_ut, Mfr_fault1_propagate_ut</td>
<td>0: No action if the UT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the UT_FAULT_LIMIT fault is asserted FAULT0 is associated with page 0 UT faults FAULT1 is associated with page 1 UT faults</td>
</tr>
<tr>
<td>b[7]</td>
<td>Mfr_fault0_propagate_ot, Mfr_fault1_propagate_ot</td>
<td>0: No action if the OT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the OT_FAULT_LIMIT fault is asserted FAULT0 is associated with page 0 OT faults FAULT1 is associated with page 1 OT faults</td>
</tr>
<tr>
<td>b[6]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>b[5]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>b[4]</td>
<td>Mfr_fault0_propagate_input_ov, Mfr_fault1_propagate_input_ov</td>
<td>0: No action if the VIN_OV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VIN_OV_FAULT_LIMIT fault is asserted</td>
</tr>
<tr>
<td>b[3]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>b[2]</td>
<td>Mfr_fault0_propagate_iout_oc, Mfr_fault1_propagate_iout_oc</td>
<td>0: No action if the IOOUT_OC_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the IOOUT_OC_FAULT_LIMIT fault is asserted FAULT0 is associated with page 0 OC faults FAULT1 is associated with page 1 OC faults</td>
</tr>
<tr>
<td>b[1]</td>
<td>Mfr_fault0_propagate_vout_uv, Mfr_fault1_propagate_vout_uv</td>
<td>0: No action if the VOUT UV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VOUT UV_FAULT_LIMIT fault is asserted FAULT0 is associated with page 0 UV faults FAULT1 is associated with page 1 UV faults</td>
</tr>
<tr>
<td>b[0]</td>
<td>Mfr_fault0_propagate_vout_ov, Mfr_fault1_propagate_vout_ov</td>
<td>0: No action if the VOUT OV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VOUT OV_FAULT_LIMIT fault is asserted FAULT0 is associated with page 0 OV faults FAULT1 is associated with page 1 OV faults</td>
</tr>
</tbody>
</table>
Fault Sharing Response

**COMMAND NAME** | **CMD CODE** | **DESCRIPTION** | **TYPE** | **PAGED** | **DATA FORMAT** | **UNITS** | **NVM** | **DEFAULT VALUE**
--- | --- | --- | --- | --- | --- | --- | --- | ---
MFR_FAULT_RESPONSE | 0xD5 | Action to be taken by the device when the FAULT pin is asserted low. | R/W Byte | Y | Reg | Y | 0xC0

**MFR_FAULT_RESPONSE**

The MFR_FAULT_RESPONSE command instructs the device on what action to take in response to the FAULT pin being pulled low by an external source.

**Supported Values**

<table>
<thead>
<tr>
<th>VALUE</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xC0</td>
<td>FAULT_INHIBIT The LTM4683 will three-state the output in response to the FAULT pin pulled low.</td>
</tr>
<tr>
<td>0x00</td>
<td>FAULT_IGNORE The LTM4683 continues operation without interruption.</td>
</tr>
</tbody>
</table>

The device also:

- Sets the MFR Bit in the STATUS_WORD.
- Sets Bit 0 in the STATUS_MFR_SPECIFIC Command to Indicate FAULT Is Being Pulled Low
- Notifies the Host by Asserting ALERT, Unless Masked

This command has one data byte.

**SCRATCHPAD**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>USER_DATA_00</td>
<td>0xB0</td>
<td>OEM reserved. Typically used for part serialization.</td>
<td>R/W Word</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>USER_DATA_01</td>
<td>0xB1</td>
<td>Manufacturer reserved for LTpowerPlay.</td>
<td>R/W Word</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>USER_DATA_02</td>
<td>0xB2</td>
<td>OEM reserved. Typically used for part serialization.</td>
<td>R/W Word</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>USER_DATA_03</td>
<td>0xB3</td>
<td>A NVM word available for the user.</td>
<td>R/W Word</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>0x0000</td>
<td></td>
</tr>
<tr>
<td>USER_DATA_04</td>
<td>0xB4</td>
<td>A NVM word available for the user.</td>
<td>R/W Word</td>
<td>N</td>
<td>Reg</td>
<td>Y</td>
<td>0x0000</td>
<td></td>
</tr>
</tbody>
</table>
**PMBus COMMAND DETAILS**

**USER_DATA_00 through USER_DATA_04**

These commands are nonvolatile memory locations for customer storage. The customer can write any value to the USER_DATA_\(_nn\) at any time. However, the LTpowerPlay software and contract manufacturers use some of these commands for inventory control. Modifying the reserved USER_DATA_\(_nn\) commands may lead to undesirable inventory control and incompatibility with these products.

These commands have 2-data bytes and are in a register format.

### IDENTIFICATION

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMBus_REVISION</td>
<td>0x98</td>
<td>PMBus revision is supported by this device. The current revision is 1.2.</td>
<td>R Byte</td>
<td>N</td>
<td>Reg</td>
<td>FS</td>
<td></td>
<td>0x22</td>
</tr>
<tr>
<td>CAPABILITY</td>
<td>0x19</td>
<td>Summary of PMBus optional communication protocols supported by this device.</td>
<td>R Byte</td>
<td>N</td>
<td>Reg</td>
<td>0x80</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_ID</td>
<td>0x99</td>
<td>The manufacturer ID of the LTM4683 is in ASCII.</td>
<td>R String</td>
<td>N</td>
<td>ASC</td>
<td>LTC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_MODEL</td>
<td>0xA</td>
<td>Manufacturer part number is in ASCII.</td>
<td>R String</td>
<td>N</td>
<td>ASC</td>
<td>LTM4683</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_SPECIAL_ID</td>
<td>0xE7</td>
<td>Manufacturer code representing the LTM4683.</td>
<td>R Word</td>
<td>N</td>
<td>Reg</td>
<td>0x900X</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**PMBus_REVISION**

The PMBUS_REVISION command indicates the revision of the PMBus to which the device is compliant. The LTM4683 is PMBus Version 1.2 compliant in both Part I and Part II.

This read-only command has one data byte.

**CAPABILITY**

This command provides a way for a host system to determine some key capabilities of a PMBus device.

The LTM4683 supports packet error checking, 400kHz bus speeds, and an ALERT pin.

This read-only command has one data byte.

**MFR_ID**

The MFR_ID command indicates the manufacturer ID of the LTM4683 using ASCII characters.

This read-only command is in block format.

**MFR_MODEL**

The MFR_MODEL command indicates the manufacturer’s part number of the LTM4683 using ASCII characters.

This read-only command is in block format.

**MFR_SPECIAL_ID**

The 16-bit word represents the part name and revision. 0x414 denotes the part is an LTM4683, and X is adjustable by the manufacturer.

This read-only command has two data bytes.
**PMBus COMMAND DETAILS**

**FAULT WARNING AND STATUS**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLEAR_FAULTS</td>
<td>0x03</td>
<td>Clear any fault bits that have been set</td>
<td>Send Byte</td>
<td>N</td>
<td>NA</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBALERT_MASK</td>
<td>0x1B</td>
<td>Mask activity</td>
<td>Block R/W</td>
<td>Y</td>
<td>Reg</td>
<td>Y</td>
<td>See CMD Details</td>
<td></td>
</tr>
<tr>
<td>MFR_CLEAR_PEAKS</td>
<td>0xE3</td>
<td>Clears all peak values</td>
<td>Send Byte</td>
<td>Y</td>
<td>NA</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STATUS_BYTE</td>
<td>0x78</td>
<td>One-byte summary of the unit’s fault condition.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STATUS_WORD</td>
<td>0x79</td>
<td>Two-byte summary of the unit’s fault condition.</td>
<td>R/W Word</td>
<td>Y</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STATUS_VOUT</td>
<td>0x7A</td>
<td>Output voltage fault and warning status.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STATUS_IOUT</td>
<td>0x7B</td>
<td>Output current fault and warning status.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STATUS_INPUT</td>
<td>0x7C</td>
<td>Input supply fault and warning status.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STATUS_TEMPERATURE</td>
<td>0x7D</td>
<td>External temperature fault and warning status for READ_TEMPERATURE_1.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STATUS_CML</td>
<td>0x7E</td>
<td>Communication and memory fault and warning status.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STATUS_MFR_SPECIFIC</td>
<td>0x80</td>
<td>Manufacturer-specific fault and state information.</td>
<td>R/W Byte</td>
<td>Y</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_PADS</td>
<td>0xE5</td>
<td>Digital status of the I/O pads</td>
<td>R Word</td>
<td>N</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR/Common</td>
<td>0xEF</td>
<td>Manufacturer status bits that are common across multiple ADI chips.</td>
<td>R Byte</td>
<td>N</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CLEAR_FAULTS**

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status commands simultaneously. At the same time, the device negates (clears, releases) its ALERT pin signal output if the device is asserting the ALERT pin signal. If the fault is still present when the bit is cleared, the fault bit will remain set, and the host will be notified by asserting the ALERT pin low. CLEAR_FAULTS can take up to 10µs to process. If a fault occurs within that time frame, it may be cleared before the status register is set.

This write-only command has no data bytes.

The CLEAR_FAULTS does not cause a unit that has latched off for a fault condition to restart. Units that have shut down for a fault condition are restarted when:

- The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or
- MFR_RESET command is issued.
- Bias power is removed and reapplied to the integrated circuit

**SMBALERT_MASK**

The SMBALERT_MASK command can be used to prevent a particular status bit or bits from asserting ALERT as they are asserted.

Figure 55 shows an example of the Write Word format used to set an ALERT mask, in this case, without PEC. The bits in the mask byte align with bits in the specified status register. For example, if the STATUS_TEMPERATURE command code is sent in the first data byte, and the mask byte contains 0x40, then a subsequent External Overtemperature Warning...
**PMBus Command Details**

would still set bit 6 of STATUS_TEMPERATURE but not assert ALERT. All other supported STATUS_TEMPERATURE bits would continue to assert ALERT if set.

Figure 55 and Figure 56 show an example of the Block Write – Block Read Process Call protocol used to read back the present state of any supported status register, again without PEC.

SMBALERT_MASK cannot be applied to STATUS_BYTE, STATUS_WORD, MFR_COMMON or MFR_PADS_LTM4683. Factory default masking for applicable status registers is shown below. Providing an unsupported command code to SMBALERT_MASK will generate a CML for Invalid/Unsupported Data.

**SMBALERT_MASK Default Setting: (Also see Figure 2)**

<table>
<thead>
<tr>
<th>STATUS RESISTER</th>
<th>ALERT MASK VALUE</th>
<th>MASKED BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>STATUS_VOUT</td>
<td>0x00</td>
<td>None</td>
</tr>
<tr>
<td>STATUS_IOUT</td>
<td>0x00</td>
<td>None</td>
</tr>
<tr>
<td>STATUS_TEMPERATURE</td>
<td>0x00</td>
<td>None</td>
</tr>
<tr>
<td>STATUS_CML</td>
<td>0x00</td>
<td>None</td>
</tr>
<tr>
<td>STATUS_INPUT</td>
<td>0x00</td>
<td>None</td>
</tr>
<tr>
<td>STATUS_MFR_SPECIFIC</td>
<td>0x11</td>
<td>Bit 4 (internal PLL unlocked), bit 0 (FAULT pulled low by external device)</td>
</tr>
</tbody>
</table>

**Figure 55. Example of Writing SMBALERT_MASK**

**Figure 56. Example of Reading SMBALERT_MASK**

**MFRCLEAR_PEAKS**

The MFR_CLEAR_PEAKS command clears the MFR_* PEAK data values. A MFR_RESET command will also clear the MFR_* PEAK data values.

This write-only command has no data bytes.

**STATUS_BYTE**

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults. This is the lower byte of the status word.
PMBus COMMAND DETAILS

STATUS_BYTE Message Contents

<table>
<thead>
<tr>
<th>BIT</th>
<th>STATUS BIT NAME</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7*</td>
<td>BUSY</td>
<td>A fault was declared because the LTM4683 was unable to respond.</td>
</tr>
<tr>
<td>6</td>
<td>OFF</td>
<td>This bit is set if the channel is not providing power to its output, regardless of the reason, including simply not being enabled.</td>
</tr>
<tr>
<td>5</td>
<td>VOUT_OV</td>
<td>An output overvoltage fault has occurred.</td>
</tr>
<tr>
<td>4</td>
<td>IOUT_OC</td>
<td>An output overcurrent fault has occurred.</td>
</tr>
<tr>
<td>3</td>
<td>VIN_UV</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
<tr>
<td>2</td>
<td>TEMPERATURE</td>
<td>A temperature fault or warning has occurred.</td>
</tr>
<tr>
<td>1</td>
<td>CML</td>
<td>A communications, memory or logic fault has occurred.</td>
</tr>
<tr>
<td>0*</td>
<td>NONE_OF_THE_ABOVE</td>
<td>A fault Not listed in bits[7:1] has occurred.</td>
</tr>
</tbody>
</table>

*ALERT can be asserted if either of these bits is set. They may be cleared by writing a 1 to their bit position in the STATUS_BYTE, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_WORD

The STATUS_WORD command returns a two-byte summary of the channel's fault condition. The low byte of the STATUS_WORD is the same as the STATUS_BYTE command.

STATUS_WORD High Byte Message Contents

<table>
<thead>
<tr>
<th>BIT</th>
<th>STATUS BIT NAME</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>VOUT</td>
<td>An output voltage fault or warning has occurred.</td>
</tr>
<tr>
<td>14</td>
<td>IOUT</td>
<td>An output current fault or warning has occurred.</td>
</tr>
<tr>
<td>13</td>
<td>INPUT</td>
<td>An input voltage fault or warning has occurred.</td>
</tr>
<tr>
<td>12</td>
<td>MFR_SPECIFIC</td>
<td>A fault or warning specific to the LTM4683 has occurred.</td>
</tr>
<tr>
<td>11</td>
<td>POWER_GOOD#</td>
<td>The POWER_GOOD state is false if this bit is set.</td>
</tr>
<tr>
<td>10</td>
<td>FANS</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
<tr>
<td>9</td>
<td>OTHER</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
<tr>
<td>8</td>
<td>UNKNOWN</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
</tbody>
</table>

If any of the bits in the upper byte are set, NONE_OF_THE_ABOVE is asserted.

This command has two data bytes.

STATUS_VOUT

The STATUS_VOUT command returns one byte of VOUT status information.

STATUS_VOUT Message Contents

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>VOUT overvoltage fault</td>
</tr>
<tr>
<td>6</td>
<td>VOUT overvoltage warning</td>
</tr>
<tr>
<td>5</td>
<td>VOUT undervoltage warning</td>
</tr>
<tr>
<td>4</td>
<td>VOUT undervoltage fault</td>
</tr>
<tr>
<td>3</td>
<td>VOUT max warning</td>
</tr>
<tr>
<td>2</td>
<td>TON max fault</td>
</tr>
<tr>
<td>1</td>
<td>TOFF max fault</td>
</tr>
<tr>
<td>0</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
</tbody>
</table>
The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an ALERT event.

This command has one data byte.

**STATUS_IOUT**

The STATUS_IOUT command returns one byte of I\textsubscript{OUT} status information.

### STATUS_IOUT Message Contents

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>I\textsubscript{OUT} overcurrent fault</td>
</tr>
<tr>
<td>6</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
<tr>
<td>5</td>
<td>I\textsubscript{OUT} overcurrent warning</td>
</tr>
<tr>
<td>4:0</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
</tbody>
</table>

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an ALERT event. This command has one data byte.

**STATUS_INPUT**

The STATUS_INPUT command returns one byte of V\textsubscript{IN} status information.

### STATUS_INPUT Message Contents

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>V\textsubscript{IN} overvoltage fault</td>
</tr>
<tr>
<td>6</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
<tr>
<td>5</td>
<td>V\textsubscript{IN} undervoltage warning</td>
</tr>
<tr>
<td>4</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
<tr>
<td>3</td>
<td>Unit off for insufficient V\textsubscript{IN}</td>
</tr>
<tr>
<td>2</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
<tr>
<td>1</td>
<td>I\textsubscript{IN} overcurrent warning</td>
</tr>
<tr>
<td>0</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
</tbody>
</table>

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an ALERT event. Bit 3 of this command is not latched and will not generate an ALERT even if it is set. This command has one data byte.
**PMBus COMMAND DETAILS**

**STATUS_TEMPERATURE**

The STATUS_TEMPERATURE command returns one byte with status information on temperature. This is a paged command and is related to the respective READ_TEMPERATURE_1 value.

**STATUS_TEMPERATURE Message Contents**

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>External overtemperature fault</td>
</tr>
<tr>
<td>6</td>
<td>External overtemperature warning</td>
</tr>
<tr>
<td>5</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
<tr>
<td>4</td>
<td>External undertemperature fault</td>
</tr>
<tr>
<td>3:0</td>
<td>Not supported (LTM4683 returns 0)</td>
</tr>
</tbody>
</table>

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

This command has one data byte.

**STATUS_CML**

The STATUS_CML command returns one byte of status information on received commands, internal memory and logic.

**STATUS_CML Message Contents**

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Invalid or unsupported command received</td>
</tr>
<tr>
<td>6</td>
<td>Invalid or unsupported data received</td>
</tr>
<tr>
<td>5</td>
<td>The packet error check failed</td>
</tr>
<tr>
<td>4</td>
<td>Memory fault detected</td>
</tr>
<tr>
<td>3</td>
<td>Processor fault detected</td>
</tr>
<tr>
<td>2</td>
<td>Reserved (LTM4683 returns 0)</td>
</tr>
<tr>
<td>1</td>
<td>Other communication faults</td>
</tr>
<tr>
<td>0</td>
<td>Other memory or logic faults</td>
</tr>
</tbody>
</table>

If either bit 3 or bit 4 of this command is set, a serious and significant internal error has been detected. Continued operation of the part is not recommended if these bits are continuously set.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an ALERT event.

This command has one data byte.
**PMBus COMMAND DETAILS**

**STATUS_MFR_SPECIFIC**

The STATUS_MFR_SPECIFIC commands return one byte with the manufacturer-specific status information.

The format for this byte is:

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Internal Temperature Fault Limit Exceeded</td>
</tr>
<tr>
<td>6</td>
<td>Internal Temperature Warn Limit Exceeded</td>
</tr>
<tr>
<td>5</td>
<td>Factory Trim Area NVM CRC Fault</td>
</tr>
<tr>
<td>4</td>
<td>PLL is Unlocked</td>
</tr>
<tr>
<td>3</td>
<td>Fault Log Present</td>
</tr>
<tr>
<td>2</td>
<td>( V_{DD33} ) UV or OV Fault</td>
</tr>
<tr>
<td>1</td>
<td>ShortCycle Event Detected</td>
</tr>
<tr>
<td>0</td>
<td>FAULT Pin Asserted Low by External Device</td>
</tr>
</tbody>
</table>

If any of these bits are set, the MFR bit in the STATUS_WORD will be set, and ALERT may be asserted.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command. However, the fault log present bit can only be cleared by issuing the MFR_FAULT_LOG_CLEAR command.

Any supported fault bit in this command will initiate an ALERT event.

This command has one data byte.

**MFR_PADS**

This command provides the user with a means of directly reading the digital status of the I/O pins of the device. The bit assignments of this command are as follows:

<table>
<thead>
<tr>
<th>BIT</th>
<th>ASSIGNED DIGITAL PIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>( V_{DD33} ) OV Fault</td>
</tr>
<tr>
<td>14</td>
<td>( V_{DD33} ) UV Fault</td>
</tr>
<tr>
<td>13</td>
<td>Reserved</td>
</tr>
<tr>
<td>12</td>
<td>Reserved</td>
</tr>
<tr>
<td>11</td>
<td>ADC values invalid, occurs during start-up. May occur briefly on current measurement channels during normal operation.</td>
</tr>
<tr>
<td>10</td>
<td>SYNC clocked by an external device (when LTM4683 configured to drive SYNC pin).</td>
</tr>
<tr>
<td>9</td>
<td>Channel 1 Power Good</td>
</tr>
<tr>
<td>8</td>
<td>Channel 0 Power Good</td>
</tr>
<tr>
<td>7</td>
<td>LTM4683 Driving RUN1 Low</td>
</tr>
<tr>
<td>6</td>
<td>LTM4683 Driving RUN0 Low</td>
</tr>
<tr>
<td>5</td>
<td>RUN1 Pin State</td>
</tr>
<tr>
<td>4</td>
<td>RUN0 Pin State</td>
</tr>
<tr>
<td>3</td>
<td>LTM4683 Driving FAULT1 Low</td>
</tr>
<tr>
<td>2</td>
<td>LTM4683 Driving FAULT0 Low</td>
</tr>
<tr>
<td>1</td>
<td>FAULT1 Pin State</td>
</tr>
<tr>
<td>0</td>
<td>FAULT0 Pin State</td>
</tr>
</tbody>
</table>

A 1 indicates the condition is true.

This read-only command has two data bytes.
**LTM4683**

**PMBus COMMAND DETAILS**

**MFR_COMMON**

The MFR_COMMON command contains bits that are common to all ADI digital power and telemetry products.

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Module Not Driven ALERT Low</td>
</tr>
<tr>
<td>6</td>
<td>LTM4683 Not Busy</td>
</tr>
<tr>
<td>5</td>
<td>Calculations Not Pending</td>
</tr>
<tr>
<td>4</td>
<td>LTM4683 Outputs Not in Transition</td>
</tr>
<tr>
<td>3</td>
<td>NVM Initialized</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>SHARE_CLK Timeout</td>
</tr>
<tr>
<td>0</td>
<td>WP Pin Status</td>
</tr>
</tbody>
</table>

This read-only command has one data byte.

**TELEMETRY**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ_VIN</td>
<td>0x88</td>
<td>Measured input supply voltage</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>V</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>READ_IIN</td>
<td>0x89</td>
<td>Measured input supply current</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>A</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>READ_VOUT</td>
<td>0x8B</td>
<td>Measured output voltage</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>V</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>READ_IOUT</td>
<td>0x8C</td>
<td>Measured current</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>A</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>READ_TEMPERATURE_1</td>
<td>0x8D</td>
<td>Power stage temperature sensor. This is the value used for all temperature-related processing, including IOUT_CAL_GAIN.</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>C</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>READ_TEMPERATURE_2</td>
<td>0x8E</td>
<td>Internal junction temperature. Does not affect any other controller commands.</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>C</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>READ_FREQUENCY</td>
<td>0x95</td>
<td>Measured PWM switching frequency.</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>Hz</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>READ_POUT</td>
<td>0x96</td>
<td>Calculated output power</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>W</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>READ_PIN</td>
<td>0x97</td>
<td>Calculated input power</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>W</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>MFR_PIN_ACCURACY</td>
<td>0xAC</td>
<td>Returns the accuracy of the READ_PIN command</td>
<td>R Byte</td>
<td>N</td>
<td>%</td>
<td>5.0%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_IOUT_PEAK</td>
<td>0xD7</td>
<td>Report the maximum measured value of READ_IOUT since the last MFR_CLEAR_PEAKS.</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>A</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>MFR_VOUT_PEAK</td>
<td>0xDD</td>
<td>The maximum measured value of READ_VOUT since the last MFR_CLEAR_PEAKS</td>
<td>R Word</td>
<td>Y</td>
<td>L16</td>
<td>V</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>MFR_VIN_PEAK</td>
<td>0xDE</td>
<td>The maximum measured value of READ_VIN since the last MFR_CLEAR_PEAKS</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>V</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>MFR_TEMPERATURE_1_PEAK</td>
<td>0xDF</td>
<td>The maximum measured value of external Temperature (READ_TEMPERATURE_1) since the last MFR_CLEAR_PEAKS.</td>
<td>R Word</td>
<td>Y</td>
<td>L11</td>
<td>C</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>MFR_READ_IIN_PEAK</td>
<td>0xE1</td>
<td>The maximum measured value of the READ_IIN command since the last MFR_CLEAR_PEAKS.</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>A</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>MFR_READ_ICHIP</td>
<td>0xE4</td>
<td>Measured current used by the LTM4683.</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>A</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>MFR_TEMPERATURE_2_PEAK</td>
<td>0xF4</td>
<td>Peak internal die temperature since the last MFR_CLEAR_PEAKS.</td>
<td>R Word</td>
<td>N</td>
<td>L11</td>
<td>C</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>MFR_ADC_CONTROL</td>
<td>0xD8</td>
<td>ADC telemetry parameter selected for repeated fast ADC read back.</td>
<td>R/W Byte</td>
<td>N</td>
<td>N</td>
<td>Reg</td>
<td>NA</td>
<td></td>
</tr>
</tbody>
</table>
**PMBus COMMAND DETAILS**

**READ_VIN**
The READ_VIN command returns the measured \( V_{IN} \) pin voltage, in volts added to \( \text{READ_ICHIP} \cdot MFR_{RVIN} \). This compensates for the IR voltage drop across the \( V_{IN} \) filter element due to the supply current of the LTM4683.
This read-only command has two data bytes and is formatted in Linear_5s_11s format.

**READ_VOUT**
The READ_VOUT command returns the measured output voltage by the VOUT_MODE command.
This read-only command has two data bytes and is formatted in Linear_16u format.

**READ_IIN**
The READ_IIN command returns the input current, in Amperes, as measured across the input current sense resistor (see also MFR_IIN_CAL_GAIN).
This read-only command has two data bytes and is formatted in Linear_5s_11s format.

**READ_IOUT**
The READ_IOUT command returns the average output current in amperes. The \( I_{OUT} \) value is a function of:
1. The differential voltage measured across the \( I_{SENSE} \) pins.
2. The \( IOUT_{CAL\_GAIN} \) value.
3. The MFR_IOUT_CAL_GAIN_TC value.
4. \( \text{READ\_TEMPERATURE}_1 \) value.
5. The MFR_TEMP_1_GAIN and the MFR_TEMP_1_OFFSET.
This read-only command has two data bytes and is formatted in Linear_5s_11s format.

**READ_TEMPERATURE_1**
The READ_TEMPERATURE_1 command returns the temperature, in degrees Celsius, of the power stage sense element.
This read-only command has two data bytes and is formatted in Linear_5s_11s format.

**READ_TEMPERATURE_2**
The READ_TEMPERATURE_2 command returns the LTM4683’s die temperature, in degrees Celsius, of the internal sense element.
This read-only command has two data bytes and is formatted in Linear_5s_11s format.

**READ_FREQUENCY**
The READ_FREQUENCY command is a reading of the PWM switching frequency in kHz.
This read-only command has 2-data bytes and is formatted in Linear_5s_11s format.

**READ_POUT**
The READ_POUT command is a reading of the DC/DC converter output power in Watts. \( P_{OUT} \) is calculated based on the most recent correlated output voltage and current reading.
This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.
PMBus COMMAND DETAILS

READ_PIN
The READ_PIN command is a reading of the DC/DC converter input power in Watts. The PIN is calculated based on the most recent input voltage and current reading.
This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

MFR_PIN_ACCURACY
The MFR_PIN_ACCURACY command returns the accuracy, in percent, of the value returned by the READ_PIN command.
There is one data byte. The value is 0.1% per bit, which gives a range of ±0.0% to ±25.5%.
This read-only command has one data byte and is formatted as an unsigned integer.

MFR_IOUT_PEAK
The MFR_IOUT_PEAK command reports the highest current, in amperes, reported by the READ_IOUT measurement.
This command is cleared using the MFR_CLEAR_PEAKS command.
This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_VOUT_PEAK
The MFR_VOUT_PEAK command reports the highest voltage, in volts, reported by the READ_VOUT measurement.
This command is cleared using the MFR_CLEAR_PEAKS command.
This read-only command has two data bytes and is formatted in Linear_16u format.

MFR_VIN_PEAK
The MFR_VIN_PEAK command reports the highest voltage, in volts, reported by the READ_VIN measurement.
This command is cleared using the MFR_CLEAR_PEAKS command.
This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_TEMPERATURE_1_PEAK
The MFR_TEMPERATURE_1_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_1 measurement.
This command is cleared using the MFR_CLEAR_PEAKS command.
This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_READ_IIN_PEAK
The MFR_READ_IIN_PEAK command reports the highest current, in Amperes, reported by the READ_IIN measurement.
This command is cleared using the MFR_CLEAR_PEAKS command.
This command has two data bytes and is formatted in Linear_5s_11s format.
**PMBus COMMAND DETAILS**

**MFR_READ_ICHIP**
The MFR_READ_ICHIP command returns the measured input current, in Amperes, used by the LTM4683. This command has two data bytes and is formatted in Linear_5s_11s format.

**MFR_TEMPERATURE_2_PEAK**
The MFR_TEMPERATURE_2_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_2 measurement. This command is cleared using the MFR_CLEAR_PEAKS command. This read-only command has two data bytes and is formatted in Linear_5s_11s format.

**MFR_ADC_CONTROL**
The MFR_ADC_CONTROL command determines the ADC read-back selection. A default value of 0 in the command runs the standard telemetry loop with all parameters updated in a round-robin fashion with a typical latency of t\text{CONVERT}. The user can command a non-zero value to monitored a single parameter with an approximate update rate of 8ms. This command has a latency of up to 2 ADC conversions or approximately 16ms (external temperature conversions may have a latency of up to 3 ADC conversions or approximately 24ms). It is recommended the part remain in standard telemetry mode except for special cases where fast ADC updates of a single parameter are required. The part should be commanded to monitor the desired parameter for a limited period of time (less than 1 second), then set the command back to standard round-robin mode. If this command is set to any value except standard round-robin telemetry (0), all warnings and faults associated with telemetry other than the selected parameter are effectively disabled, and voltage servoing is disabled. When round-robin is reasserted, all warnings and faults and servo mode are re-enabled.

<table>
<thead>
<tr>
<th>COMMANDED VALUE</th>
<th>TELEMETRY COMMAND NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0F</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x0E</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x0D</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x0C</td>
<td>READ_TEMPERATURE_1</td>
<td>Channel 1 external temperature</td>
</tr>
<tr>
<td>0x0B</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x0A</td>
<td>READ_IOUT</td>
<td>Channel 1 measured output current</td>
</tr>
<tr>
<td>0x09</td>
<td>READ_VOUT</td>
<td>Channel 1 measured output voltage</td>
</tr>
<tr>
<td>0x08</td>
<td>READ_TEMPERATURE_1</td>
<td>Channel 0 external temperature</td>
</tr>
<tr>
<td>0x07</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x06</td>
<td>READ_IOUT</td>
<td>Channel 0 measured output current</td>
</tr>
<tr>
<td>0x05</td>
<td>READ_VOUT</td>
<td>Channel 0 measured output voltage</td>
</tr>
<tr>
<td>0x04</td>
<td>READ_TEMPERATURE_2</td>
<td>Internal junction temperature</td>
</tr>
<tr>
<td>0x03</td>
<td>READ_IIN</td>
<td>Measured input supply current</td>
</tr>
<tr>
<td>0x02</td>
<td>MFR_READ_ICHIP</td>
<td>Measured supply current of the LTM4683</td>
</tr>
<tr>
<td>0x01</td>
<td>READ_VIN</td>
<td>Measured input supply voltage</td>
</tr>
<tr>
<td>0x00</td>
<td>Standard ADC Round-Robin Telemetry</td>
<td></td>
</tr>
</tbody>
</table>

If a reserved command value is entered, the telemetry will default to Internal IC Temperature and issue a CML fault. CML faults will continue to be issued by the LTM4683 until a valid command value is entered. The accuracy of the measured input supply voltage is only guaranteed if the MFR_ADC_CONTROL command is set to standard round-robin telemetry. This write-only command has one data byte and is formatted in a register format.
## PMBus COMMAND DETAILS

### NVM MEMORY COMMANDS

#### Store/Restore

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>STORE_USER_ALL</td>
<td>0x15</td>
<td>Store user operating memory to EEPROM.</td>
<td>Send Byte</td>
<td>N</td>
<td>NA</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESTORE_USER_ALL</td>
<td>0x16</td>
<td>Restore user operating memory from EEPROM.</td>
<td>Send Byte</td>
<td>N</td>
<td>NA</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFRCOMPARE_USER_ALL</td>
<td>0xF0</td>
<td>Compares current command contents with NVM.</td>
<td>Send Byte</td>
<td>N</td>
<td>NA</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**STORE_USER_ALL**

The STORE_USER_ALL command instructs the PMBus device to copy the nonvolatile user contents of the Operating Memory to the matching locations in the nonvolatile User NVM memory.

If the die temperature exceeds 85°C or is below 0°C, executing this command is not recommended, and the data retention of 10 years cannot be guaranteed. If the die temperature exceeds 130°C, the STORE_USER_ALL command is disabled. The command is re-enabled when the IC temperature drops below 125°C.

Communication with the LTM4683 and programming of the NVM can be initiated when EXTVCC or VDD33 is available, and VIN is not applied. To enable the part in this state, using global address 0x5B, write MFR_EE_UNLOCK to 0x2B followed by 0xC4. The LTM4683 will now communicate normally, and the project file can be updated. To write the updated project file to the NVM issue a STORE_USER_ALL command. When VIN is applied, an MFR_RESET must be issued to allow the PWM to be enabled and valid ADCs to be read.

This write-only command has no data bytes.

**RESTORE_USER_ALL**

The RESTORE_USER_ALL command instructs the LTM4683 to copy the contents of the nonvolatile User memory to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the user commands. The LTM4683 ensures both channels are off, loads the operating memory from the internal EEPROM, clears all faults, reads the resistor configuration pins, and then performs a soft-start of both PWM channels if applicable.

STORE_USER_ALL, MFR_COMPARE_USER_ALL and RESTORE_USER_ALL commands are disabled if the die exceeds 130°C and are not re-enabled until the die temperature drops below 125°C.

This write-only command has no data bytes.

**MFR_COMPARE_USER_ALL**

The MFR_COMPARE_USER_ALL command instructs the PMBus device to compare current command contents with what is stored in nonvolatile memory. If the compare operation detects differences, a CML bit 0 fault will be generated.

This write-only command has no data bytes.
**PMBus COMMAND DETAILS**

**Fault Logging**

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_FAULT_LOG</td>
<td>0xEE</td>
<td>Fault log data bytes.</td>
<td>R Block</td>
<td>N</td>
<td>CF</td>
<td>Y</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>MFR_FAULT_LOG_STORE</td>
<td>0xEA</td>
<td>Command a transfer of the fault log from RAM to EEPROM.</td>
<td>Send Byte</td>
<td>N</td>
<td></td>
<td></td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>MFR_FAULT_LOG_CLEAR</td>
<td>0xEC</td>
<td>Initialize the EEPROM block reserved for fault logging.</td>
<td>Send Byte</td>
<td>N</td>
<td></td>
<td></td>
<td>NA</td>
<td></td>
</tr>
</tbody>
</table>

**MFR_FAULT_LOG**

The MFR_FAULT_LOG command allows the user to read the contents of the FAULT_LOG after the first fault occurrence since the last MFR_FAULT_LOG_CLEAR command was written. The contents of this command are stored in nonvolatile memory, and are cleared by the MFR_FAULT_LOG_CLEAR command. The length and content of this command are listed in Table 15. If the user accesses the MFR_FAULT_LOG command and the no-fault log is present, the command will return a data length of 0. If a fault log is present, the MFR_FAULT_LOG will return a block of data 147 bytes long. If a fault occurs within the first second of applying power, some of the earlier pages in the fault log may not contain valid data.

**NOTE:** The approximate transfer time for this command is 3.4ms using a 400kHz clock.

This read-only command is in block format.

**MFR_FAULT_LOG_STORE**

The MFR_FAULT_LOG_STORE command forces the fault log operation to be written to NVM just as if a fault event occurred. This command will set bit 3 of the STATUS_MFR_SPECIFIC fault if bit 7, “Enable Fault Logging”, is set in the MFR_CONFIG_ALL command.

If the die temperature exceeds 130°C, the MFR_FAULT_LOG_STORE command is disabled until the IC temperature drops below 125°C.

This write-only command has no data bytes.
### Table 23. Fault Logging

This table outlines the format of the block data from a read block data of the MFR_FAULT_LOG command.

<table>
<thead>
<tr>
<th>DATA</th>
<th>BITS</th>
<th>DATA FORMAT</th>
<th>BYTE NUM</th>
<th>BLOCK READ COMMAND</th>
</tr>
</thead>
<tbody>
<tr>
<td>Block Length</td>
<td>BYTE</td>
<td>147</td>
<td></td>
<td>The MFR_FAULT_LOG command is a fixed length of 147 bytes.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The block length will be zero if a data log event has not been captured.</td>
</tr>
</tbody>
</table>

**HEADER INFORMATION**

| Fault Log Preface         | [7:0] | ASC         | 0        | Returns LTxx beginning at byte 0 if a partial or complete fault log exists.     |
|                          | [7:0] |             | 1        | Word xx is a factory identifier that may vary from part to part.               |
|                          | [15:8]| Reg         | 2        |                                                                                |
|                          | [7:0] |             | 3        |                                                                                |
| Fault Source             | [7:0] | Reg         | 4        | See Table 19.                                                                  |
| MFR_REAL_TIME            | [7:0] | Reg         | 5        | 48-bit share-clock counter value when the fault occurred (200µs resolution).   |
|                          | [15:8]|             | 6        |                                                                                |
|                          | [23:16]|            | 7        |                                                                                |
|                          | [31:24]|            | 8        |                                                                                |
|                          | [39:32]|            | 9        |                                                                                |
|                          | [47:40]|            | 10       |                                                                                |
| MFR_VOUT_PEAK (PAGE 0)   | [15:8]| L16        | 11       | Peak READ_VOUT on Channel 0 since the last power-on or CLEAR_PEAKS command.      |
|                          | [7:0] |             | 12       |                                                                                |
| MFR_VOUT_PEAK (PAGE 1)   | [15:8]| L16        | 13       | Peak READ_VOUT on Channel 1 since the last power-on or CLEAR_PEAKS command.      |
|                          | [7:0] |             | 14       |                                                                                |
| MFR_IOUT_PEAK (PAGE 0)   | [15:8]| L11        | 15       | Peak READ_IOUT on Channel 0 since the last power-on or CLEAR_PEAKS command.      |
|                          | [7:0] |             | 16       |                                                                                |
| MFR_IOUT_PEAK (PAGE 1)   | [15:8]| L11        | 17       | Peak READ_IOUT on Channel 1 since the last power-on or CLEAR_PEAKS command.      |
|                          | [7:0] |             | 18       |                                                                                |
| MFR_VIN_PEAK             | [15:8]| L11        | 19       | Peak READ_VIN since the last power-on or CLEAR_PEAKS command.                    |
|                          | [7:0] |             | 20       |                                                                                |
| READ_TEMPERATURE1 (PAGE 0)| [15:8]| L11       | 21       | Power stage temperature sensor 0 during the last event.                         |
|                          | [7:0] |             | 22       |                                                                                |
| READ_TEMPERATURE1 (PAGE 1)| [15:8]| L11       | 23       | Power stage temperature sensor 1 during the last event.                         |
|                          | [7:0] |             | 24       |                                                                                |
| READ_TEMPERATURE2        | [15:8]| L11       | 25       | LTM4683 die temperature sensor during the last event.                            |
|                          | [7:0] |             | 26       |                                                                                |
### PMBus COMMAND DETAILS

**Table 23. Fault Logging**

This table outlines the format of the block data from a read block data of the MFR_FAULT_LOG command.

#### CYCLICAL DATA

<table>
<thead>
<tr>
<th>EVENT n</th>
<th>(Data at Which Fault Occurred, Most Recent Data)</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ_VOUT (PAGE 0)</td>
<td>[15:8] LIN 16 27</td>
</tr>
<tr>
<td></td>
<td>[7:0] LIN 16 28</td>
</tr>
<tr>
<td>READ_VOUT (PAGE 1)</td>
<td>[15:8] LIN 16 29</td>
</tr>
<tr>
<td></td>
<td>[7:0] LIN 16 30</td>
</tr>
<tr>
<td>READ_IOUT (PAGE 0)</td>
<td>[15:8] LIN 11 31</td>
</tr>
<tr>
<td></td>
<td>[7:0] LIN 11 32</td>
</tr>
<tr>
<td>READ_IOUT (PAGE 1)</td>
<td>[15:8] LIN 11 33</td>
</tr>
<tr>
<td></td>
<td>[7:0] LIN 11 34</td>
</tr>
<tr>
<td>READ_VIN</td>
<td>[15:8] LIN 11 35</td>
</tr>
<tr>
<td></td>
<td>[7:0] LIN 11 36</td>
</tr>
<tr>
<td>READ_IIN</td>
<td>[15:8] LIN 11 37</td>
</tr>
<tr>
<td></td>
<td>[7:0] LIN 11 38</td>
</tr>
<tr>
<td>STATUS_VOUT (PAGE 0)</td>
<td>BYTE 39</td>
</tr>
<tr>
<td>STATUS_VOUT (PAGE 1)</td>
<td>BYTE 40</td>
</tr>
<tr>
<td>STATUS_WORD (PAGE 0)</td>
<td>[15:8] WORD 41</td>
</tr>
<tr>
<td></td>
<td>[7:0] WORD 42</td>
</tr>
<tr>
<td>STATUS_WORD (PAGE 1)</td>
<td>[15:8] WORD 43</td>
</tr>
<tr>
<td></td>
<td>[7:0] WORD 44</td>
</tr>
<tr>
<td>STATUS_MFR_SPECIFIC (PAGE 0)</td>
<td>BYTE 45</td>
</tr>
<tr>
<td>STATUS_MFR_SPECIFIC (PAGE 1)</td>
<td>BYTE 46</td>
</tr>
</tbody>
</table>

Event "n" represents one complete cycle of ADC reads through the MUX at the time of the fault. Example: If the fault occurs when the ADC is processing step 15, it will continue to take readings through step 25 and then store the header and all 6-event pages to EEPROM.
### Table 23. Fault Logging
This table outlines the format of the block data from a read block data of the MFR_FAULT_LOG command.

<table>
<thead>
<tr>
<th>EVENT n-1</th>
<th>READ_VOUT (PAGE 0)</th>
<th>READ_VOUT (PAGE 1)</th>
<th>READ_IOUT (PAGE 0)</th>
<th>READ_IOUT (PAGE 1)</th>
<th>READ_VIN</th>
<th>READ_IIN</th>
<th>STATUS_VOUT (PAGE 0)</th>
<th>STATUS_VOUT (PAGE 1)</th>
<th>STATUS_WORD (PAGE 0)</th>
<th>STATUS_WORD (PAGE 1)</th>
<th>STATUS_MFR_SPECIFIC (PAGE 0)</th>
<th>STATUS_MFR_SPECIFIC (PAGE 1)</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>EVENT n-5</th>
<th>READ_VOUT (PAGE 0)</th>
<th>READ_VOUT (PAGE 1)</th>
<th>READ_IOUT (PAGE 0)</th>
<th>READ_IOUT (PAGE 1)</th>
<th>READ_VIN</th>
<th>READ_IIN</th>
<th>STATUS_VOUT (PAGE 0)</th>
<th>STATUS_VOUT (PAGE 1)</th>
<th>STATUS_WORD (PAGE 0)</th>
<th>STATUS_WORD (PAGE 1)</th>
<th>STATUS_MFR_SPECIFIC (PAGE 0)</th>
<th>STATUS_MFR_SPECIFIC (PAGE 1)</th>
</tr>
</thead>
</table>
PMBus COMMAND DETAILS

Table 24. Explanation of Position_Fault Values

<table>
<thead>
<tr>
<th>POSITION_FAULT_VALUE</th>
<th>SOURCE OF FAULT LOG</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xFF</td>
<td>MFR_FAULT_LOG_STORE</td>
</tr>
<tr>
<td>0x00</td>
<td>TON_MAX_FAULT</td>
</tr>
<tr>
<td>0x01</td>
<td>VOUT_OV_FAULT</td>
</tr>
<tr>
<td>0x02</td>
<td>VOUT_UV_FAULT</td>
</tr>
<tr>
<td>0x03</td>
<td>IOUT_OC_FAULT</td>
</tr>
<tr>
<td>0x05</td>
<td>TEMP_OT_FAULT</td>
</tr>
<tr>
<td>0x06</td>
<td>TEMP_UT_FAULT</td>
</tr>
<tr>
<td>0x07</td>
<td>VIN_OV_FAULT</td>
</tr>
<tr>
<td>0x0A</td>
<td>MFR_TEMP_2_OT_FAULT</td>
</tr>
</tbody>
</table>

MFR_INFO
Contact the factory for details.

MFR_IOUT_CAL_GAIN
Contact the factory for details.

MFR_FAULT_LOG_CLEAR
The MFR_FAULT_LOG_CLEAR command will erase the fault log file stored values. It will also clear bit 3 in the STATUS_MFR_SPECIFIC command. After a clear is issued, the status can take up to 8ms to clear.
This write-only command is to send bytes.

Block Memory Write/Read

<table>
<thead>
<tr>
<th>COMMAND NAME</th>
<th>CMD CODE</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
<th>PAGED</th>
<th>DATA FORMAT</th>
<th>UNITS</th>
<th>NVM</th>
<th>DEFAULT VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFR_EE_UNLOCK</td>
<td>0xBD</td>
<td>Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_EE_ERASE</td>
<td>0xBE</td>
<td>Initialize user EEPROM for bulk programming by MFR_EE_DATA.</td>
<td>R/W Byte</td>
<td>N</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFR_EE_DATA</td>
<td>0xBF</td>
<td>Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.</td>
<td>R/W Word</td>
<td>N</td>
<td>Reg</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

All the NVM commands are disabled if the die temperature exceeds 130°C. NVM commands are re-enabled when the die temperature drops below 125°C.

MFR_EE_xxxx
The MFR_EE_xxxx commands facilitate bulk programming of the LTM4683 internal EEPROM. Contact the factory for details.
## PACKAGE DESCRIPTION

**PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.**

Table 25. LTM4683 BGA Pinout

<table>
<thead>
<tr>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>GND</td>
<td>B1</td>
<td>GND</td>
<td>C1</td>
<td>SW0</td>
<td>D1</td>
<td>SW0</td>
<td>E1</td>
<td>SW0</td>
<td>F1</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>GND</td>
<td>B2</td>
<td>GND</td>
<td>C2</td>
<td>SW0</td>
<td>D2</td>
<td>SW0</td>
<td>E2</td>
<td>SW0</td>
<td>F2</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A3</td>
<td>GND</td>
<td>B3</td>
<td>GND</td>
<td>C3</td>
<td>GND</td>
<td>D3</td>
<td>GND</td>
<td>E3</td>
<td>GND</td>
<td>F3</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A4</td>
<td>GND</td>
<td>B4</td>
<td>GND</td>
<td>C4</td>
<td>GND</td>
<td>D4</td>
<td>GND</td>
<td>E4</td>
<td>GND</td>
<td>F4</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A5</td>
<td>VIN01</td>
<td>B5</td>
<td>VIN01</td>
<td>C5</td>
<td>VIN01</td>
<td>D5</td>
<td>VIN01</td>
<td>E5</td>
<td>VIN01</td>
<td>F5</td>
<td>VIN01</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A6</td>
<td>VIN01</td>
<td>B6</td>
<td>VIN01</td>
<td>C6</td>
<td>VIN01</td>
<td>D6</td>
<td>VIN01</td>
<td>E6</td>
<td>VIN01</td>
<td>F6</td>
<td>VIN01</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A7</td>
<td>GND</td>
<td>B7</td>
<td>GND</td>
<td>C7</td>
<td>GND</td>
<td>D7</td>
<td>GND</td>
<td>E7</td>
<td>GND</td>
<td>F7</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A8</td>
<td>VOUT0_CFG</td>
<td>B8</td>
<td>VOUT1_CFG</td>
<td>C8</td>
<td>VDD25_01</td>
<td>D8</td>
<td>SHARE_CLK_01</td>
<td>E8</td>
<td>VDD33_01</td>
<td>F8</td>
<td>VOSNS1**</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A9</td>
<td>FSWPH_01_CFG</td>
<td>B9</td>
<td>ASEL_01</td>
<td>C9</td>
<td>VTRIM1_CFG</td>
<td>D9</td>
<td>VTRIMO_CFG</td>
<td>E9</td>
<td>WP_01</td>
<td>F9</td>
<td>COMP1b</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A10</td>
<td>FAULT1</td>
<td>B10</td>
<td>RUN0</td>
<td>C10</td>
<td>SDA_01</td>
<td>D10</td>
<td>SCL_01</td>
<td>E10</td>
<td>TSN1</td>
<td>F10</td>
<td>SGND01</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A11</td>
<td>FAULT0</td>
<td>B11</td>
<td>RUN1</td>
<td>C11</td>
<td>ALERT_01</td>
<td>D11</td>
<td>SYNC_01</td>
<td>E11</td>
<td>TSN0</td>
<td>F11</td>
<td>SGND01</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A12</td>
<td>GND</td>
<td>B12</td>
<td>GND</td>
<td>C12</td>
<td>GND</td>
<td>D12</td>
<td>GND</td>
<td>E12</td>
<td>GND</td>
<td>F12</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A13</td>
<td>VOUT0</td>
<td>B13</td>
<td>VOUT0</td>
<td>C13</td>
<td>VOUT0</td>
<td>D13</td>
<td>VOUT0</td>
<td>E13</td>
<td>VOUT0</td>
<td>F13</td>
<td>VOUT1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A14</td>
<td>VOUT0</td>
<td>B14</td>
<td>VOUT0</td>
<td>C14</td>
<td>VOUT0</td>
<td>D14</td>
<td>VOUT0</td>
<td>E14</td>
<td>VOUT0</td>
<td>F14</td>
<td>VOUT1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A15</td>
<td>VOUT0</td>
<td>B15</td>
<td>VOUT0</td>
<td>C15</td>
<td>VOUT0</td>
<td>D15</td>
<td>VOUT0</td>
<td>E15</td>
<td>VOUT0</td>
<td>F15</td>
<td>VOUT1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G1</td>
<td>SW1</td>
<td>H1</td>
<td>SW1</td>
<td>J1</td>
<td>SW1</td>
<td>K1</td>
<td>GND</td>
<td>L1</td>
<td>GND</td>
<td>M1</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G2</td>
<td>SW1</td>
<td>H2</td>
<td>SW1</td>
<td>J2</td>
<td>SW1</td>
<td>K2</td>
<td>GND</td>
<td>L2</td>
<td>GND</td>
<td>M2</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G3</td>
<td>GND</td>
<td>H3</td>
<td>GND</td>
<td>J3</td>
<td>GND</td>
<td>K3</td>
<td>GND</td>
<td>L3</td>
<td>GND</td>
<td>M3</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G4</td>
<td>GND</td>
<td>H4</td>
<td>GND</td>
<td>J4</td>
<td>GND</td>
<td>K4</td>
<td>GND</td>
<td>L4</td>
<td>GND</td>
<td>M4</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G5</td>
<td>VIN01</td>
<td>H5</td>
<td>VIN01</td>
<td>J5</td>
<td>VIN01</td>
<td>K5</td>
<td>VIN01</td>
<td>L5</td>
<td>GND</td>
<td>M5</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G6</td>
<td>VIN01</td>
<td>H6</td>
<td>VIN01</td>
<td>J6</td>
<td>VIN01</td>
<td>K6</td>
<td>VIN01</td>
<td>L6</td>
<td>GND</td>
<td>M6</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G7</td>
<td>GND</td>
<td>H7</td>
<td>GND</td>
<td>J7</td>
<td>GND</td>
<td>K7</td>
<td>GND</td>
<td>L7</td>
<td>GND</td>
<td>M7</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G8</td>
<td>VOSNS1++</td>
<td>H8</td>
<td>PGOOD1</td>
<td>J8</td>
<td>SVIN_01</td>
<td>K8</td>
<td>GND</td>
<td>L8</td>
<td>GND</td>
<td>M8</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G9</td>
<td>COMP1a</td>
<td>H9</td>
<td>PGOOD0</td>
<td>J9</td>
<td>INTVCC_01</td>
<td>K9</td>
<td>GND</td>
<td>L9</td>
<td>GND</td>
<td>M9</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G10</td>
<td>COMP0b</td>
<td>H10</td>
<td>IIN_01++</td>
<td>J10</td>
<td>IIN_01++</td>
<td>K10</td>
<td>GND</td>
<td>L10</td>
<td>GND</td>
<td>M10</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G11</td>
<td>COMP0a</td>
<td>H11</td>
<td>VOSNS0--</td>
<td>J11</td>
<td>VOSNS0++</td>
<td>K11</td>
<td>GND</td>
<td>L11</td>
<td>GND</td>
<td>M11</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G12</td>
<td>GND</td>
<td>H12</td>
<td>GND</td>
<td>J12</td>
<td>GND</td>
<td>K12</td>
<td>GND</td>
<td>L12</td>
<td>GND</td>
<td>M12</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G13</td>
<td>VOUT1</td>
<td>H13</td>
<td>VOUT1</td>
<td>J13</td>
<td>VOUT1</td>
<td>K13</td>
<td>VOUT1</td>
<td>L13</td>
<td>GND</td>
<td>M13</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G14</td>
<td>VOUT1</td>
<td>H14</td>
<td>VOUT1</td>
<td>J14</td>
<td>VOUT1</td>
<td>K14</td>
<td>VOUT1</td>
<td>L14</td>
<td>GND</td>
<td>M14</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G15</td>
<td>VOUT1</td>
<td>H15</td>
<td>VOUT1</td>
<td>J15</td>
<td>VOUT1</td>
<td>K15</td>
<td>VOUT1</td>
<td>L15</td>
<td>GND</td>
<td>M15</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 25. LTM4683 BGA Pinout

<table>
<thead>
<tr>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1</td>
<td>GND</td>
<td>P1</td>
<td>SW2</td>
<td>R1</td>
<td>SW2</td>
<td>T1</td>
<td>SW2</td>
<td>U1</td>
<td>GND</td>
<td>V1</td>
<td>SW3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N2</td>
<td>GND</td>
<td>P2</td>
<td>SW2</td>
<td>R2</td>
<td>SW2</td>
<td>T2</td>
<td>SW2</td>
<td>U2</td>
<td>GND</td>
<td>V2</td>
<td>SW3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N3</td>
<td>GND</td>
<td>P3</td>
<td>GND</td>
<td>R3</td>
<td>GND</td>
<td>T3</td>
<td>GND</td>
<td>U3</td>
<td>GND</td>
<td>V3</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N4</td>
<td>GND</td>
<td>P4</td>
<td>GND</td>
<td>R4</td>
<td>GND</td>
<td>T4</td>
<td>GND</td>
<td>U4</td>
<td>GND</td>
<td>V4</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N5</td>
<td>VIN23</td>
<td>P5</td>
<td>VIN23</td>
<td>R5</td>
<td>VIN23</td>
<td>T5</td>
<td>VIN23</td>
<td>U5</td>
<td>VIN23</td>
<td>V5</td>
<td>VIN23</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N6</td>
<td>VIN23</td>
<td>P6</td>
<td>VIN23</td>
<td>R6</td>
<td>VIN23</td>
<td>T6</td>
<td>VIN23</td>
<td>U6</td>
<td>VIN23</td>
<td>V6</td>
<td>VIN23</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N7</td>
<td>GND</td>
<td>P7</td>
<td>GND</td>
<td>R7</td>
<td>GND</td>
<td>T7</td>
<td>GND</td>
<td>U7</td>
<td>GND</td>
<td>V7</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N8</td>
<td>VIN_VBIAS</td>
<td>P8</td>
<td>V_GNS2*</td>
<td>R8</td>
<td>V_GNS2*</td>
<td>T8</td>
<td>COMP2a</td>
<td>U8</td>
<td>TSNS2</td>
<td>V8</td>
<td>SDA_23</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N9</td>
<td>VIN_VBIAS</td>
<td>P9</td>
<td>I_IN,23^</td>
<td>R9</td>
<td>I_IN,23^</td>
<td>T9</td>
<td>COMP2b</td>
<td>U9</td>
<td>TSNS3</td>
<td>V9</td>
<td>SYNC_23</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N10</td>
<td>VIN_BIAS</td>
<td>P10</td>
<td>INTVCC,23</td>
<td>R10</td>
<td>PGOOD2</td>
<td>T10</td>
<td>PGOOD3</td>
<td>U10</td>
<td>SGND23</td>
<td>V10</td>
<td>FAULT2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N11</td>
<td>RUNP</td>
<td>P11</td>
<td>SVIN,23</td>
<td>R11</td>
<td>V_GNS3*</td>
<td>T11</td>
<td>V_GNS3*</td>
<td>U11</td>
<td>SGND23</td>
<td>V11</td>
<td>COMP3a</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N12</td>
<td>GND</td>
<td>P12</td>
<td>GND</td>
<td>R12</td>
<td>GND</td>
<td>T12</td>
<td>GND</td>
<td>U12</td>
<td>GND</td>
<td>V12</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N13</td>
<td>VOUT2</td>
<td>P13</td>
<td>VOUT2</td>
<td>R13</td>
<td>VOUT2</td>
<td>T13</td>
<td>VOUT2</td>
<td>U13</td>
<td>VOUT2</td>
<td>V13</td>
<td>VOUT3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N14</td>
<td>VOUT2</td>
<td>P14</td>
<td>VOUT2</td>
<td>R14</td>
<td>VOUT2</td>
<td>T14</td>
<td>VOUT2</td>
<td>U14</td>
<td>VOUT2</td>
<td>V14</td>
<td>VOUT3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N15</td>
<td>VOUT2</td>
<td>P15</td>
<td>VOUT2</td>
<td>R15</td>
<td>VOUT2</td>
<td>T15</td>
<td>VOUT2</td>
<td>U15</td>
<td>VOUT2</td>
<td>V15</td>
<td>VOUT3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
<th>PIN ID</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>W1</td>
<td>SW3</td>
<td>Y1</td>
<td>SW3</td>
<td>AA1</td>
<td>GND</td>
<td>AB1</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W2</td>
<td>SW3</td>
<td>Y2</td>
<td>SW3</td>
<td>AA2</td>
<td>GND</td>
<td>AB2</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W3</td>
<td>GND</td>
<td>Y3</td>
<td>GND</td>
<td>AA3</td>
<td>GND</td>
<td>AB3</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W4</td>
<td>GND</td>
<td>Y4</td>
<td>GND</td>
<td>AA4</td>
<td>GND</td>
<td>AB4</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W5</td>
<td>VIN23</td>
<td>Y5</td>
<td>VIN23</td>
<td>AA5</td>
<td>VIN23</td>
<td>AB5</td>
<td>VIN23</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W6</td>
<td>VIN23</td>
<td>Y6</td>
<td>VIN23</td>
<td>AA6</td>
<td>VIN23</td>
<td>AB6</td>
<td>VIN23</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W7</td>
<td>GND</td>
<td>Y7</td>
<td>GND</td>
<td>AA7</td>
<td>GND</td>
<td>AB7</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W8</td>
<td>ALERT_23</td>
<td>Y8</td>
<td>RUN3</td>
<td>AA8</td>
<td>VOUT2_CFG</td>
<td>AB8</td>
<td>VOUT3_CFG</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W9</td>
<td>SCL_23</td>
<td>Y9</td>
<td>RUN2</td>
<td>AA9</td>
<td>FSWPH_23_CFG</td>
<td>AB9</td>
<td>VTRIM3_CFG</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W10</td>
<td>FAULT3</td>
<td>Y10</td>
<td>VDD33,23</td>
<td>AA10</td>
<td>ASEL_23</td>
<td>AB10</td>
<td>VTRIM2_CFG</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W11</td>
<td>COMP3b</td>
<td>Y11</td>
<td>WP_23</td>
<td>AA11</td>
<td>SHARE_CLK_23</td>
<td>AB11</td>
<td>VDD25,23</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W12</td>
<td>GND</td>
<td>Y12</td>
<td>GND</td>
<td>AA12</td>
<td>GND</td>
<td>AB12</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W13</td>
<td>VOUT3</td>
<td>Y13</td>
<td>VOUT3</td>
<td>AA13</td>
<td>VOUT3</td>
<td>AB13</td>
<td>VOUT3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W14</td>
<td>VOUT3</td>
<td>Y14</td>
<td>VOUT3</td>
<td>AA14</td>
<td>VOUT3</td>
<td>AB14</td>
<td>VOUT3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W15</td>
<td>VOUT3</td>
<td>Y15</td>
<td>VOUT3</td>
<td>AA15</td>
<td>VOUT3</td>
<td>AB15</td>
<td>VOUT3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**BGA Package**

330-Lead (22mm × 15mm × 5.71mm)

*(Reference DWG # BC-330-2 Rev Ø)*

**DIMENSIONS**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>5.58</td>
<td>5.71</td>
<td>6.00</td>
<td></td>
</tr>
<tr>
<td>A1</td>
<td>0.40</td>
<td>0.50</td>
<td>0.60</td>
<td>BALL HT</td>
</tr>
<tr>
<td>A2</td>
<td>1.72</td>
<td>1.82</td>
<td>1.92</td>
<td></td>
</tr>
<tr>
<td>b</td>
<td>0.50</td>
<td>0.60</td>
<td>0.70</td>
<td>BALL DIM</td>
</tr>
<tr>
<td>b1</td>
<td>0.47</td>
<td>0.50</td>
<td>0.53</td>
<td>PAD DIM</td>
</tr>
<tr>
<td>D</td>
<td>15.00</td>
<td>22.00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>1.00</td>
<td>21.00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>14.00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>H1</td>
<td>0.27</td>
<td>0.32</td>
<td>0.37</td>
<td>SUBSTRATE THK</td>
</tr>
<tr>
<td>H2</td>
<td>1.45</td>
<td>1.50</td>
<td>1.55</td>
<td>MOLD CAP HT</td>
</tr>
<tr>
<td>H3</td>
<td>3.50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>aaa</td>
<td>0.15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bbb</td>
<td>0.10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ccc</td>
<td>0.20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ddd</td>
<td>0.25</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>eee</td>
<td>0.10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fff</td>
<td>0.35</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY
<table>
<thead>
<tr>
<th>REV</th>
<th>DATE</th>
<th>DESCRIPTION</th>
<th>PAGE NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>10/23</td>
<td>Initial Release.</td>
<td></td>
</tr>
</tbody>
</table>
LTM4683

PACKAGE PHOTOS Part marking is either ink mark or laser mark

DESIGN RESOURCES

<table>
<thead>
<tr>
<th>SUBJECT</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>µModule Design and Manufacturing Resources</td>
<td>Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools</td>
<td>Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability</td>
</tr>
<tr>
<td>µModule Regulator Products Search</td>
<td>1. Sort table of products by parameters and download the result as a spreadsheet. 2. Search using the Quick Power Search parametric table.</td>
<td></td>
</tr>
<tr>
<td>Digital Power System Management</td>
<td>Analog Devices’ family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.</td>
<td></td>
</tr>
</tbody>
</table>

RELATED PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTM4675</td>
<td>Dual 9A or Single 18A Step-Down µModule Regulator, Digital Power System Management (PSM)</td>
<td>4.5V ≤ VIN ≤ 17V, 0.5V ≤ VOUT ≤ 5.5V, 11.9mm × 16mm × 3.51mm BGA</td>
</tr>
<tr>
<td>LTM4673</td>
<td>Dual 12A and Dual 5A, Quad µModule Regulator, Digital PSM</td>
<td>4.5V ≤ VIN ≤ 16V, 0.6V ≤ VOUT ≤ 3.3V or 5.5V, 16mm × 16mm × 4.72mm BGA</td>
</tr>
<tr>
<td>LTM4686/LM4686-1</td>
<td>Ultrathin Dual 10A or Single 20A µModule Regulator, Digital PSM</td>
<td>4.5V ≤ VIN ≤ 17V, 0.5V ≤ VOUT ≤ 3.6V (LTM4686), 2.375V ≤ VIN ≤ 17V (LTM4686-1) 11.9mm × 16mm × 1.82mm LGA</td>
</tr>
<tr>
<td>LTM4688B</td>
<td>Ultrathin Dual 14A or Single 28A µModule Regulator, Digital PSM, Low VOUT, Higher iOUT Version of LTM4686/LM4686-1</td>
<td>4.5V ≤ VIN ≤ 5.75V, 0.5V ≤ VOUT ≤ 3.6V, 11.9mm × 16mm × 1.82mm LGA</td>
</tr>
<tr>
<td>LTM4676A</td>
<td>Dual 13A or Single 26A Step-Down µModule Regulator, Digital PSM</td>
<td>4.5V ≤ VIN ≤ 26.5V, 0.5V ≤ VOUT ≤ 5.5V, 16mm × 16mm × 5.01mm BGA</td>
</tr>
<tr>
<td>LTM4677</td>
<td>Dual 18A or Single 36A Step-Down µModule Regulator, Digital PSM</td>
<td>4.5V ≤ VIN ≤ 16V, 0.5V ≤ VOUT ≤ 1.8V, 16mm × 16mm × 5.01mm BGA</td>
</tr>
<tr>
<td>LTM4678</td>
<td>Dual 25A or Single 50A µModule Regulator with Digital PSM</td>
<td>4.5V ≤ VIN ≤ 16V, 0.5V ≤ VOUT ≤ 3.4V, 16mm × 16mm × 5.86mm BGA</td>
</tr>
<tr>
<td>LTM4664</td>
<td>54VIN, Dual 25A or Single 50A µModule Regulator with Digital PSM</td>
<td>30V ≤ VIN ≤ 58V, 0.5V ≤ VOUT ≤ 1.5V, 16mm × 16mm × 7.72mm BGA</td>
</tr>
<tr>
<td>LTM4680</td>
<td>Dual 30A or Single 60A µModule Regulator with Digital PSM</td>
<td>4.5V ≤ VIN ≤ 16V, 0.5V ≤ VOUT ≤ 3.3V, 16mm × 16mm × 8.72mm BGA</td>
</tr>
<tr>
<td>LTM4681</td>
<td>Quad 31.25A or Single 125A, µModule Regulator with Digital PSM, Higher VOUT Version of LTM4683</td>
<td>4.5V ≤ VIN ≤ 16V, 0.5V ≤ VOUT ≤ 3.3V, 15mm × 22mm × 7.87mm BGA</td>
</tr>
<tr>
<td>LTM4700</td>
<td>Dual 50A or Single 100A µModule Regulator with Digital PSM</td>
<td>4.5V ≤ VIN ≤ 16V, 0.5V ≤ VOUT ≤ 1.8V, 15mm × 22mm × 7.87mm BGA</td>
</tr>
</tbody>
</table>