55V, 300W Source/Sink Hybrid Step-Down Non-Isolated µModule Bus Converter

FEATURES

- Input voltage range: 20V to 55V (57V abs. max.)
- Wide output voltage range: 4.5V to 18V ($V_{OUT} < V_{IN}/2$)
- 96.7% efficiency (9V at ±15A output, $48V_{IN}$)
- ±3% maximum total DC output error
- Up to 300W output power (source/sink)
- Scalable for higher power applications
- Fixed-frequency current mode control
- Phase-lockable external synchronization from 200kHz to 1MHz
- Low startup inrush current with voltage-balancing of C_{FLY} and C_{MID} before the DC-to-DC switching action
- Output voltage tracking with soft start
- Short-circuit protection with adjustable retry-timer
- Overcurrent and overtemperature protection
- Onboard diode temperature monitor
- Optional external reference input
- Power good and $\overline{FAULT}$ output indicators
- *120-Lead, 16mm × 16mm × 8.96mm, BGA* package

APPLICATIONS

- Non-isolated intermediate bus power architectures
- Telecom, networking, test, and measurement equipment
- Industrial applications

GENERAL DESCRIPTION

The *LTM4654* is a complete 300W output source/sink switching mode hybrid-topology step-down DC-to-DC power µModule® (micromodule) bus converter. The LTM4654's exposed power inductor resides on the top of the package, providing an intrinsic path for the heat to dissipate
up-and-out of the power module—away from the printed circuit board (PCB). The package includes the switching controller IC, the power MOSFETs, and the supporting components. Only flying (charge-pump) capacitors, bulk input and output bypass capacitors, and a few passive components for configurations are needed.

The LTM4654 features bidirectional operation, frequency synchronization, Burst Mode® operation, output voltage soft start, and tracking. An onboard temperature diode is available for temperature monitoring. The LTM4654 is designed for scalability. In higher power applications, multiple LTM4654 power modules can be paralleled.

The LTM4654 protects against short-circuit, overcurrent (OC), and overtemperature (OT) faults. The LTM4654 is offered in a BGA package with a RoHS-compliant terminal finish.

TYPICAL APPLICATION

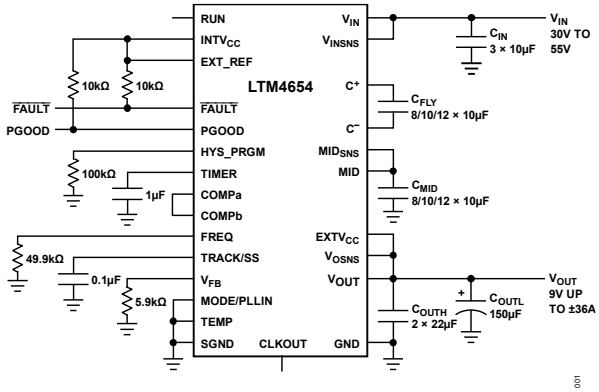


Figure 1. 9V, ±36A DC-to-DC µModule Non-Isolated Bus Converter

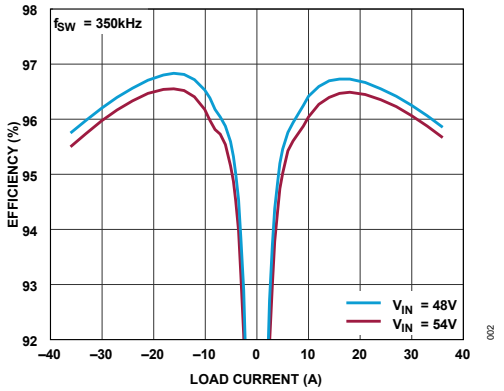


Figure 2. Efficiency vs. Load Current, V_{OUT} = 9V

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

TABLE OF CONTENTS

REVISION HISTORY

04/2025 - Rev. 0, Initial Release.

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C[1], V_{IN} = V_{INSNS} = 48V, RUN = open circuit, $EXTV_{CC}$ = 9V[2], configured per the *Block Diagram* circuit with no output load unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Input DC voltage	$V_{IN(DC)}$	–40°C ≤ T_J ≤ 125°C	20		55	V
Output voltage, supported range of regulation[3]	$V_{OUT(RANGE)}$	–40°C ≤ T_J ≤ 125°C	4.5		18	V
Output voltage, total variation with line and load[4]	$V_{OUT(DC)}$	–20A ≤ I_{OUT} ≤ 20A	8.7	9	9.3	V
Minimum input voltage	$V_{IN(DC,MIN)}$	V_{OUT} = 9V, I_{OUT} = 0A[6]		20		V
		V_{OUT} = 9V, I_{OUT} = 10A[6]		22		
		V_{OUT} = 12V, I_{OUT} = 0A[6]		26		
		V_{OUT} = 12V, I_{OUT} = 10A[6]		29		
		V_{OUT} = 18V, I_{OUT} = 0A[6]		38		
		V_{OUT} = 18V, I_{OUT} = 10A[6]		42		
Input Specifications						
Undervoltage lockout threshold	$V_{IN(UVLO)}$	V_{IN} rising; –40°C ≤ T_J ≤ 125°C		8.8	9.4	V
		Hysteresis		0.45		
Input supply power current in Forced continuous mode (FCM)	$I_{S(VIN, FCM)}$	MODE/PLLIN = 0V, I_{OUT} = 0A[5]		88		mA
		MODE/PLLIN = 0V, I_{OUT} = 0.5A		185		
Input supply power current in Pulse-skipping mode (PSM)	$I_{S(VIN, PS)}$	MODE/PLLIN = $INTV_{CC}$, I_{OUT} = 0.5A		170		mA
Input supply power current in Burst Mode (BM) operation	$I_{S(VIN, BM)}$	MODE/PLLIN = open circuit, I_{OUT} = 0.5A		105		mA

(T_A = 25°C[1], V_{IN} = V_{INSNS} = 48V, RUN = open circuit, $EXTV_{CC}$ = 9V[2], configured per the *Block Diagram* circuit with no output load unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Input supply power current in shutdown	$I_{S(VIN,SHUTDOWN)}$	Shutdown, RUN = GND		300		µA
Output Specifications						
Output continuous current range	$I_{OUT(DC)}$	[4]			±36	A
Line regulation accuracy	$\Delta V_{OUT(LINE)}/V_{OUT}$	24V ≤ V_{IN} ≤ 55V, I_{OUT} = 0A		0.003	0.2	%/V
Load regulation accuracy	$\Delta V_{OUT}/V_{OUT}$	−20A ≤ I_{OUT} ≤ 20A, V_{OUT} = 9V, R_{FREQ} = 61.9kΩ	−3	1.5	3	%
		−36A ≤ I_{OUT} ≤ 36A, V_{OUT} = 9V[6]		0.5		
Output voltage ripple	$V_{OUT(AC)}$	C_{OUT} = 2 × 150µF, 3 × 10µF[6]		110		mV_{P-P}
V_{OUT} ripple frequency	f_S	R_{FREQ} = 61.9kΩ		450		kHz
Turn-on start-up time	t_{START}	Delay measured from the MID pin reaching V_{IN}/2 to PGOOD exceeding 3V above GND, $C_{TRACK/SS}$ = 0.1µF		7		ms
Peak output voltage deviation for dynamic load step	$\Delta V_{OUT(LS)}$	Load: 0W to 150W in 1µs and 150W to 0W in 1µs, C_{OUT} = 2 × 150µF, 3 × 10µF[6]		0.2		V
Settling time for dynamic load step	t_{SETTLE}	Load: 0W to 150W in 1µs and 150W to 0W in 1µs, C_{OUT} = 2 × 150µF, 3 × 10µF[6]		250		µs
Control Section						
Regulated V_{FB} pin feedback voltage	V_{VFB}	I_{OUT} = 0A, V_{OUT} = 9V; −40°C ≤ T_J ≤ 125°C	0.792	0.8	0.808	V
V_{FB} pin leakage current	I_{VFB}	[7]		±10	±50	nA
Soft start charge current	$I_{TRACK/SS}$	$V_{TRACK/SS}$ = 0V	−9	−10	−11	µA
Monitors						
V_{INSNS} bias current	I_{VINSNS}	V_{RUN} = 5V, normal mode		1		µA
		V_{RUN} = 0V, shutdown		35		

(T_A = 25°C[1], V_{IN} = V_{INSNS} = 48V, RUN = open circuit, $EXTV_{CC}$ = 9V[2], configured per the *Block Diagram* circuit with no output load unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
RUN Enable Pins							
RUN turn-on threshold	V_{RUN}	V_{RUN} rising	–40°C ≤ T_J ≤ 125°C	1.1	1.3	1.6	V
RUN hysteresis	$V_{RUN,HYS}$				100		mV
RUN pull-up current	I_{RUN}	V_{RUN} = 0V			1		µA
Capacitor Voltage-Balancing							
The voltage at TIMER pin to start capacitor balancing	V_{TIMER_LOW}				0.5		V
The voltage at TIMER pin to stop capacitor balancing	V_{TIMER_HIGH}				1.25		V
TIMER pin charge current	I_{TIMER}	V_{TIMER} = 0.9V	–40°C ≤ T_J ≤ 125°C	–6	–7		µA
		V_{TIMER} = 2.8V	–40°C ≤ T_J ≤ 125°C	–3	–3.5	–4	
Capacitor balancing window comparator threshold	V_{HYS_PRGM}	V_{HYS_PRGM} = 0V			±0.3		V
		V_{HYS_PRGM} = 1.2V			±1.2		
		V_{HYS_PRGM} = $INTV_{CC}$			±0.8		
HYS_PRGM pin current	I_{HYS_PRGM}	V_{HYS_PRGM} = 0V	–40°C ≤ T_J ≤ 125°C	–9	–10	–11	µA
$\overline{FAULT}$ pin voltage low	$V_{\overline{FAULT}}$	$I_{\overline{FAULT}}$ = 0.6mA			0.2	0.4	V
$\overline{FAULT}$ leakage current	$I_{\overline{FAULT}}$	$V_{\overline{FAULT}}$ = 20V				1	µA
Current out of C^+ during capacitor balancing	$I_{C^+(SOURCE)}$	$V_{C^+} - V_{C^-} < V_{IN}/2$, V_{C^-} = 12V[7]			40		mA
Current into C^+ during capacitor balancing	$I_{C^+(SINK)}$	$V_{C^+} - V_{C^-} < V_{IN}/2$, V_{C^-} = 12V[7]			6		mA

(T_A = 25°C[1], V_{IN} = V_{INSNS} = 48V, RUN = open circuit, $EXTV_{CC}$ = 9V[2], configured per the *Block Diagram* circuit with no output load unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Current into C⁻ during capacitor balancing	$I_{C^-(SINK)}$	$V_{C^+} - V_{C^-} < V_{IN}/2$, V_{C^-} = 12V[7]		40		mA
Current out of C⁻ during capacitor balancing	$I_{C^-(SOURCE)}$	$V_{C^+} - V_{C^-} < V_{IN}/2$, V_{C^-} = 12V[7]		6		mA
Current out of MID during capacitor balancing	$I_{MID(SOURCE)}$	$V_{MID} < V_{IN}/2$, $V_{MID} = V_{MIDSNS}$ = 23V, $V_{C^+} - V_{C^-} \geq 27V$, V_{C^-} = 12V[7]		60		mA
Current into MID during capacitor balancing	$I_{MID(SINK)}$	$V_{MID} > V_{IN}/2$, $V_{MID} = V_{MIDSNS}$ = 31V, $V_{C^+} - V_{C^-} \geq 27V$, V_{C^-} = 12V[7]		40		mA
Oscillator and Timer Circuits						
Oscillator synchronization frequency range	$f_{SYNC(RANGE)}$		200		1000	kHz
Nominal switching frequency	f_{NOM}	R_{FREQ} = 61.9kΩ		450		kHz
FREQ setting current	I_{FREQ}	V_{FREQ} = 0V[7]	–9.5	–10	–10.5	µA
Power Good						
PGOOD pull-down resistance	$R_{PGOOD(LOW)}$	I_{PGOOD} = 0.6mA		600		Ω
PGOOD leakage current	I_{PGOOD_LEAK}	V_{PGOOD} = 20V			±1	µA
$INTV_{CC}$ Regulator and $EXTV_{CC}$ Circuits						
$INTV_{CC}$ voltage no load	V_{INTVCC_INT}	10V ≤ V_{IN} ≤ 55V, V_{EXTVCC} = 0V	5.65	5.8	5.95	V
$INTV_{CC}$ load regulation	V_{INTVCC_INT}	I_{INTVCC} = 0 to 50mA, V_{EXTVCC} = 0V		0.8	±2	%
$INTV_{CC}$ voltage no load with EXTVCC bias	V_{INTVCC_EXT}	8V < V_{EXTVCC} < 20V[7]	5.65	5.8	5.95	V
$INTV_{CC}$ load regulation with EXTVCC bias		I_{INTVCC} = 0 to 50mA, V_{EXTVCC} = 9V		0.5	±2	%

(T_A = 25°C[1], V_{IN} = V_{INSNS} = 48V, RUN = open circuit, $EXTV_{CC}$ = 9V[2], configured per the *Block Diagram* circuit with no output load unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
$EXTV_{CC}$ switchover voltage		$EXTV_{CC}$ ramping positive	6.7	7	7.3	V
$EXTV_{CC}$ hysteresis				220		mV
Temperature Sensor						
Temperature sensor-forward voltage, $V_{TEMP}^+ - V_{TEMP}^-$	ΔV_{TEMP}	I_{TEMP}^+ = 100µA and I_{TEMP}^- = –100µA at T_A = 25°C		0.587		V
ΔV_{TEMP} temperature coefficient	$TC_{\Delta V(TEMP)}$			–2		mV/°C

1 The LTM4654, including the E-grade and I-grade parts (see *Table 12*), is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4654E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4654I is guaranteed to meet specifications over the full internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

2 To reduce the internal power module temperature rise, it is recommended to bias $EXTV_{CC}$ with 7.5VDC or higher (ideally 8VDC for additional safety margin). For applications where $V_{OUT} \geq 8V$, connect V_{OUT} to $EXTV_{CC}$. For applications where $V_{OUT} < 8V$, drive $EXTV_{CC}$ to 8V (or higher) with an external bias supply.

3 For LTM4654 with this hybrid topology, V_{OUT} is always lower than $V_{IN}/2$. The minimum required differential voltage between $V_{IN}/2$ and V_{OUT} is determined by operating conditions and guaranteed by design. See the *Maximum Duty Cycle Considerations* and *Negative Output Voltage Configuration* in the *Applications Information* section for more details.

4 See the derating curves, *Figure 33* through *Figure 38*, for different V_{IN}, V_{OUT}, and T_A conditions in the *Applications Information* section.

5 The dynamic supply current is higher because of the gate charge being delivered at the switching frequency in the FCM operation. See the *Applications Information* section for more details.

6 Guaranteed by design. Validated from bench measurements.

7 Automatic test equipment (ATE) test performed at the wafer sort level only.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C[1] unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
Terminal Voltages[2]	
V_{IN}, V_{INSNS}	–0.3V to 57V
V_{OUT}, V_{OSNS}, $EXTV_{CC}$, PGOOD, $\overline{FAULT}$	–0.3V to 20V
MID, MID_{SNS}	–0.3V to 28.5V
C^+	–0.3V to V_{IN} + 0.3V
C^-	–0.3V to MID + 0.3V
RUN, FREQ, HYS_PRGM, TEMP, V_{FB}, TRACK/SS, TIMER, MODE_PLLIN, EXT_REF, COMPa, COMPb	–0.3V to $INTV_{CC}$
Terminal Currents	
$TEMP^+$	–1mA to 1mA
$TEMP^-$	–1mA to 1mA
Temperatures	
Internal operating temperature range[1]	–40°C to 125°C
Storage temperature range	–55°C to 125°C
Peak package body temperature during reflow	245°C

1 The LTM4654, including the E-grade and I-grade parts (see *Table 12*), is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4654E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4654I is guaranteed to meet specifications over the full internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

2 All voltages relative to GND unless otherwise indicated.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Field induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

Table 3. LTM4654 ESD Ratings

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±2500	2
CDM	±1250	C3

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

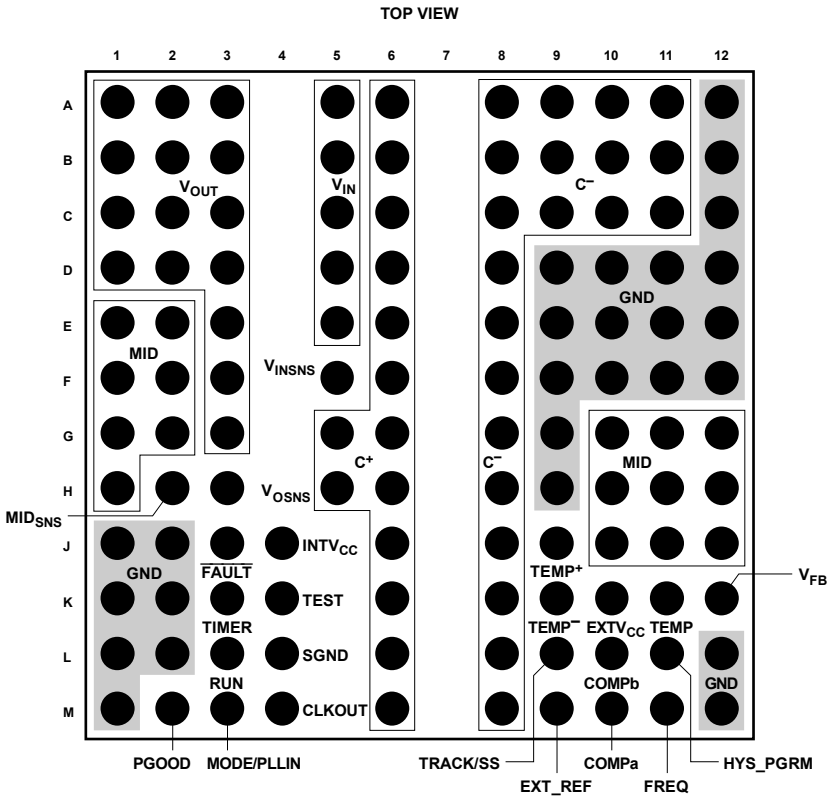


Figure 3. Pin Configuration

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Table 4. Pin Descriptions

PIN	NAME	DESCRIPTION
A1-A3, B1-B3, C1-C3, D1-D3, E3, F3, G3	V_{OUT}	Output Voltage. Bypass this pin to GND with capacitors that are appropriate to the application. See the *Decoupling Requirements* table. An internal 49.9Ω resistor between V_{OUT} and V_{OSNS} protects the output from an open V_{OSNS} scenario.
A5, B5, C5, D5, E5	V_{IN}	The Main Input Supply. Bypass this pin to GND with at least 3 × 10µF X7R- or X7S-type capacitors with the appropriate voltage rating.

A6, B6, C6, D6, E6, F6, G5, G6, H5, H6, J6, K6, L6, M6	C^+	Switch Node Connection to One Terminal of the Flying Capacitor. The voltage swing at this pin is from $V_{IN}/2$ voltage to V_{IN}.
A8-A11, B8-B11, C8-C11, D8, E8, F8, G8, H8, J8, K8, L8, M8	C^-	Switch Node Connection to the Internal Power Inductor and to One Terminal of the Flying Capacitor. The voltage swing at this pin is from slightly below ground to $V_{IN}/2$.
A12, B12, C12, D9-D12, E9-E12, F9-F12, G9, H9, J1, J2, K1, K2, L1, L2, L12, M1, M12	GND	Power Ground. Connect all the power modules' GND pins to the application's power ground plane.
E1, E2, F1, F2, G1, G2, G10-G12, H1, H10-H12, J10-J12	MID	Half Supply from V_{IN}. Do not use these pins to source current. Connect MLCC bypass capacitors from this node to GND. A minimum of 8 × 10µF X7R or X7S MLCC capacitors are recommended. Higher efficiency can be achieved with 12 × 10µF X7R or X7S MLCC capacitors. All MID pins are internally connected within the power module, but for the best possible efficiency, it is necessary to connect all MID pins together with the large copper plane(s) external to the power module. See the *Applications Information* section for more details.
F5	V_{INSNS}	The V_{IN} Kelvin Sensing Input. Allow an internal $V_{IN}/2$ to be generated for the power module control circuit usage. Connect to V_{IN}, under the power module.
H2	MID_{SNS}	Half Supply Monitor. Provides Kelvin sensing input for the comparator that monitors the voltage between MID_{SNS} and ground. Connect to MID, under the power module.
H3	V_{OSNS}	Output Voltage Sensing Pin. This pin is connected to the top of the internal feedback resistor (60.4kΩ). This pin must be connected to V_{OUT}, either locally to the power module, or to the remote sense point of V_{OUT}. An internal 49.9Ω resistor between V_{OUT} and V_{OSNS} protects the output from an open V_{OSNS} scenario.
J3	$\overline{FAULT}$	Open-Drain Output Pin. When the signal goes low, it indicates one of the following conditions: 1) In the capacitor balancing phase, capacitors C_{FLY} or C_{MID} are not charged to $V_{IN}/2$ (see the *Typical Applications* section for more details). A low FAULT indicates an abnormal condition that is preventing C_{FLY} or C_{MID} from being charged up to $V_{IN}/2$.

		2) During normal operation, the voltage deviates from $V_{IN}/2$ by a window amount set by the voltage on the HYS_PRGM pin. 3) The die temperature exceeds its internally set limit, or the positive temperature coefficient (PTC) resistor connected as the lower leg of a resistor divider (if used) trips the TEMP pin threshold. 4) During these conditions, the TRACK/SS pin is also pulled low.
J4	$INTV_{CC}$	Internal Regulator Output. The gate drivers and the control circuits are powered by this regulator. Do not use the $INTV_{CC}$ pin for any other purpose that is not described in this datasheet.
J9	$TEMP^+$	Temperature Sensor Positive Input. The emitter of a 2N3906-genre PNP bipolar junction transistor (BJT). Working together with $TEMP^-$ pin, optionally apply DC current as $I_{TEMP}{}^+ = 100\mu A$ and $I_{TEMP}{}^- = -100\mu A$, and the differential voltage across $TEMP^+$ and $TEMP^-$ represents the internal temperature of the module. It is recommended adding a filter capacitor between $TEMP^+$ and $TEMP^-$ for the measurement. See the *Applications Information* section for more details. Otherwise, leave electrically open.
K3	TIMER	Charge Balancing Timer Input. A capacitor connected from this pin to ground sets the amount of time allocated to charge C_{FLY} and C_{MID} to $V_{IN}/2$ during the capacitor balancing phase. It also sets the auto-retry timeout, should the capacitors fail to reach this voltage within the set time. The charging of the capacitors, C_{FLY} and C_{MID}, is enabled when the TIMER voltage is between 0.5V and 1.2V. If the capacitor is balanced before the TIMER voltage reaches 1.2V, this voltage is reset to ground, and normal operation starts. However, if the balance is not reached when the voltage reaches 1.2V, then the charging of the capacitors stops, and the auto-retry timeout period starts. The TIMER capacitor is now slew at half of the rate until it reaches 4V, then resets to zero and starts to slew at 1× rate. Once it reaches 0.5V, the C_{FLY} and C_{MID} starts to charge again, and the process repeats.
K4	TEST	Test Pin. Used in ATE test only. Leave this pin open.
K9	$TEMP^-$	Temperature Sensor Negative Input. Collector and base of a 2N3906-genre PNP bipolar junction transistor (BJT). Working together with the $TEMP^+$ pin, optionally apply DC current as $I_{TEMP}{}^+ = 100\mu A$ and $I_{TEMP}{}^- = -100\mu A$, and the differential voltage across $TEMP^+$ and $TEMP^-$ represents the internal temperature of the module. It is recommended to add a filter capacitor between $TEMP^+$ and $TEMP^-$ for the measurement. See the *Applications Information* section for more details. Otherwise, leave electrically open.
K10	$EXTV_{CC}$	External Power Input to an Internal LDO connected to the $INTV_{CC}$. This LDO supplies the $INTV_{CC}$ power, bypassing the internal LDO powered by V_{IN} whenever $EXTV_{CC}$ is higher than 7V (typical). Do not float or exceed the absolute maximum of 20V on this pin. Connect $EXTV_{CC}$ to GND if the feature is not used. To reduce the internal power module temperature rise, it is strongly recommended to bias $EXTV_{CC}$ with 7.5VDC (ideally 8VDC for additional safety margin) or higher. For applications where $V_{OUT} \geq 8V$, connect V_{OUT} to $EXTV_{CC}$. For applications where $V_{OUT} < 8V$, drive $EXTV_{CC}$ to 8V (or higher) with an external bias supply. When driving $EXTV_{CC}$ externally, take precautions to ensure that $EXTV_{CC} \leq V_{IN}$ and $EXTV_{CC} \leq 20V$ at all times.
K11	TEMP	Temperature Sensing Input. Using a PTC resistor as the lower leg of a resistor divider, connect the TEMP pin to the common point of the divider. The PTC resistor monitors a hot spot on the printed circuit board (PCB). Once it reaches the TEMP threshold of

		1.22V, the LTM4654 stops switching for 100ms before retrying. Ground this pin if not used.
K12	V_{FB}	Error Amplifier Feedback Input. Connect the resistor R_{VFB} from this pin to SGND to configure the V_{OUT} output voltage setting. The R_{VFB} is given by: $$R_{VFB}(k\Omega) = \frac{60.4k\Omega}{\frac{V_{OUT}}{V_{VFB}} - 1}$$ When EXT_REF is connected to $INTV_{CC}$, the power module regulates the V_{FB} pin at 0.8V, nominal. If EXT_REF is used or TRACK/SS is externally driven to influence the V_{FB} target servo voltage, the value of R_{VFB} must be computed accordingly. (See the *Applications Information* section for more details.)
L3	RUN	RUN Control Input. Floating this pin or applying a voltage above 1.3V turns the controller ON. There is a 1µA pull-up current on this pin when its voltage is below 1.3V.
L4	SGND	Signal Ground. All small-signal components and external compensation components (if used) should connect to this signal ground, which connects to the GND internal to the power module. Externally connecting SGND to GND is not required.
L9	TRACK/SS	Output Voltage Tracking and Soft Start Input. The LTM4654 regulates the V_{FB} voltage to the lowest of three voltages: 0.8V, the voltage on the EXT_REF pin, or the voltage on the TRACK/SS pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage. Alternatively, a resistor divider from another voltage supply connected to this pin allows the LTM4654 output voltage to track the other supply during startup.
L10	COMPb	Default Loop Compensation Network. Connect COMPa to COMPb for default loop compensation.
L11	HYS_PRGM	There is a 10µA current flowing out of this pin. A voltage created by connecting a resistor from this pin to ground sets an equal amount of window threshold around $V_{IN}/2$ to a window comparator. When the voltage at MID_{SNS} is not within this window threshold, $\overline{FAULT}$ is pulled low, and switching stops. C_{FLY} and C_{MID} are rebalanced to half of V_{IN} before resuming normal operation.
M2	PGOOD	Power Good Pin. This is an open drain output. PGOOD is pulled to ground when the voltage of the V_{FB} pin falls below 7.5% or rises above 8.5% of its set point after an internal 50µs mask timer expires. It is also pulled low when $\overline{FAULT}$ is tripped.
M3	MODE/PLLIN	Mode Selection or External Synchronization Input to Phase Detector. When external synchronization is not used, this pin selects the operating modes and can connect to SGND, to $INTV_{CC,}$ or be left open. If the pin is connected to SGND, it enables FCM, while a connection to $INTV_{CC}$ enables PSM. Floating the pin enables Burst Mode operation. For external SYNC, apply a clock signal to this pin. The integrated PLL and its internal compensation network synchronizes the internal oscillator to this clock. The FCM is enabled when a clock is applied.
M4	CLKOUT	Clock Output Pin. This pin outputs a clock of 180° out-of-phase with the main operating clock of the LTM4654.
M9	EXT_REF	External Reference Input. A voltage applied to this pin forces the V_{FB} to be regulated to this voltage. Internal clamps set at 0.4V and 0.93V limit the lower and upper bounds of

		V_{FB} regulation that EXT_REF can command. Connecting this pin to $INTV_{CC}$ will cause the internal reference to be used for output voltage regulation.
M10	COMPa	Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with its COMPa control voltage. Connect COMPa to COMPb for default loop compensation—or alternatively, connect a series R-C network from COMPa to SGND, to apply application-specific loop compensation.
M11	FREQ	Frequency Set Pin. There is a 10µA current flowing out of this pin. A resistor to ground sets a voltage, which in turn programs the switching frequency of the power module.

Table 5. LTM4654 Component BGA Pinout (Sorted by Pin Number)

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1–C12					
A1	V_{OUT}	B1	V_{OUT}	C1	V_{OUT}
A2	V_{OUT}	B2	V_{OUT}	C2	V_{OUT}
A3	V_{OUT}	B3	V_{OUT}	C3	V_{OUT}
A4	(No Pin)	B4	(No Pin)	C4	(No Pin)
A5	V_{IN}	B5	V_{IN}	C5	V_{IN}
A6	C^+	B6	C^+	C6	C^+
A7	(No Pin)	B7	(No Pin)	C7	(No Pin)
A8	C^-	B8	C^-	C8	C^-
A9	C^-	B9	C^-	C9	C^-
A10	C^-	B10	C^-	C10	C^-
A11	C^-	B11	C^-	C11	C^-
A12	GND	B12	GND	C12	GND
D1–F12					
D1	V_{OUT}	E1	MID	F1	MID
D2	V_{OUT}	E2	MID	F2	MID
D3	V_{OUT}	E3	V_{OUT}	F3	V_{OUT}
D4	(No Pin)	E4	(No Pin)	F4	(No Pin)
D5	V_{IN}	E5	V_{IN}	F5	V_{INSNS}
D6	C^+	E6	C^+	F6	C^+
D7	(No Pin)	E7	(No Pin)	F7	(No Pin)
D8	C^-	E8	C^-	F8	C^-
D9	GND	E9	GND	F9	GND
D10	GND	E10	GND	F10	GND
D11	GND	E11	GND	F11	GND
D12	GND	E12	GND	F12	GND

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1–J12					
G1	MID	H1	MID	J1	GND
G2	MID	H2	MID_{SNS}	J2	GND
G3	V_{OUT}	H3	V_{OSNS}	J3	$\overline{FAULT}$
G4	(No Pin)	H4	(No Pin)	J4	$INTV_{CC}$
G5	C^+	H5	C^+	J5	(No Pin)
G6	C^+	H6	C^+	J6	C^+
G7	(No Pin)	H7	(No Pin)	J7	(No Pin)
G8	C^-	H8	C–	J8	C^-
G9	GND	H9	GND	J9	$TEMP^+$
G10	MID	H10	MID	J10	MID
G11	MID	H11	MID	J11	MID
G12	MID	H12	MID	J12	MID
K1–M12					
K1	GND	L1	GND	M1	GND
K2	GND	L2	GND	M2	PGOOD
K3	TIMER	L3	RUN	M3	MODE/PLLIN
K4	TEST	L4	SGND	M4	CLKOUT
K5	(No Pin)	L5	(No Pin)	M5	(No Pin)
K6	C^+	L6	C^+	M6	C^+
K7	(No Pin)	L7	(No Pin)	M7	(No Pin)
K8	C^-	L8	C^-	M8	C^-
K9	$TEMP^-$	L9	TRACK/SS	M9	EXT_REF
K10	$EXTV_{CC}$	L10	COMPb	M10	COMPa
K11	TEMP	L11	HYS_PRGM	M11	FREQ
K12	V_{FB}	L12	GND	M12	GND

TYPICAL PERFORMANCE CHARACTERISTICS

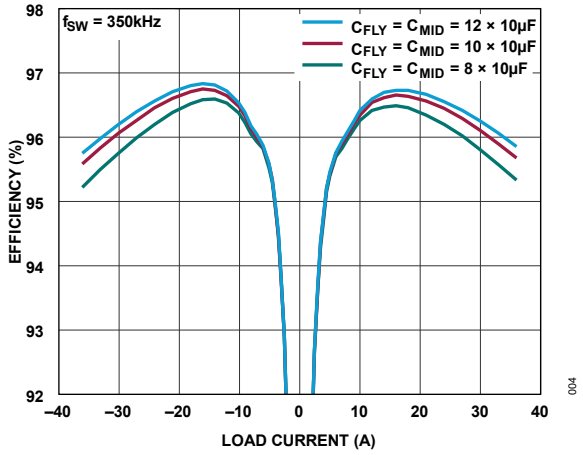


Figure 4. Efficiency vs. Load Current, V_{IN} = 48V, V_{OUT} = 9V

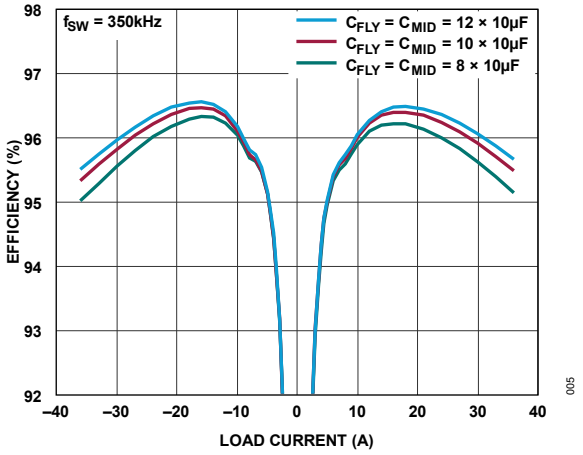


Figure 5. Efficiency vs. Load Current, V_{IN} = 54V, V_{OUT} = 9V

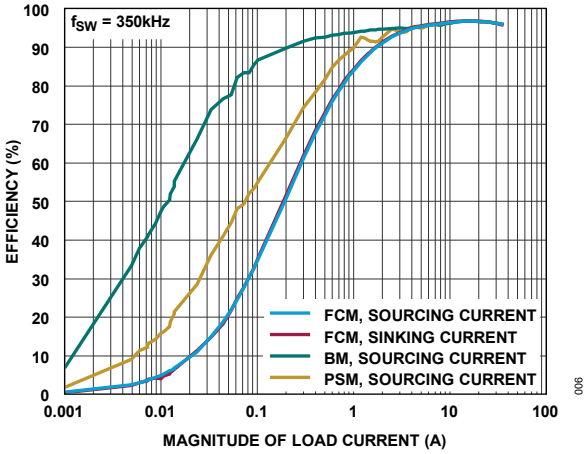


Figure 6. Efficiency vs. Load Current, V_{IN} = 48V, V_{OUT} = 9V

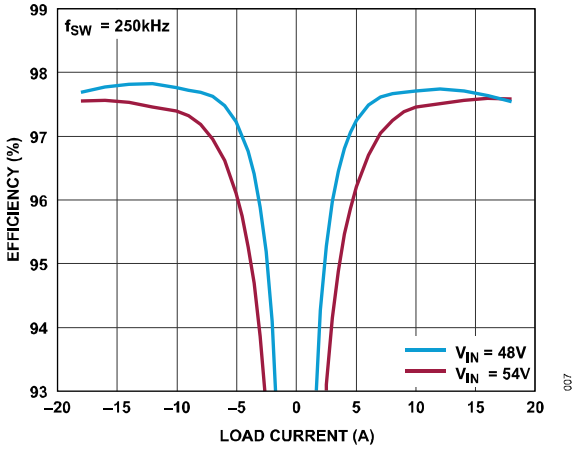


Figure 7. Efficiency vs. Load Current, V_{OUT} = 18V

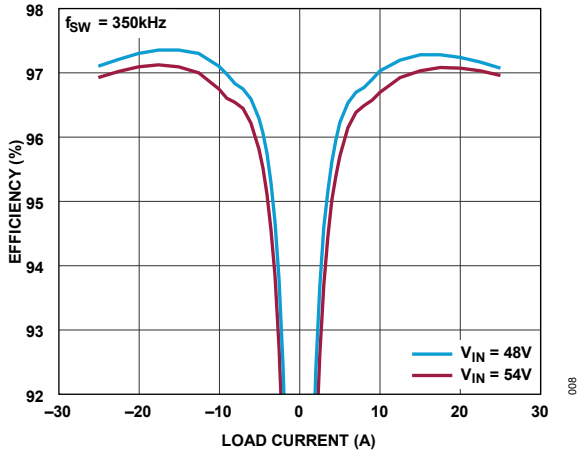


Figure 8. Efficiency vs. Load Current, V_{OUT} = 12V

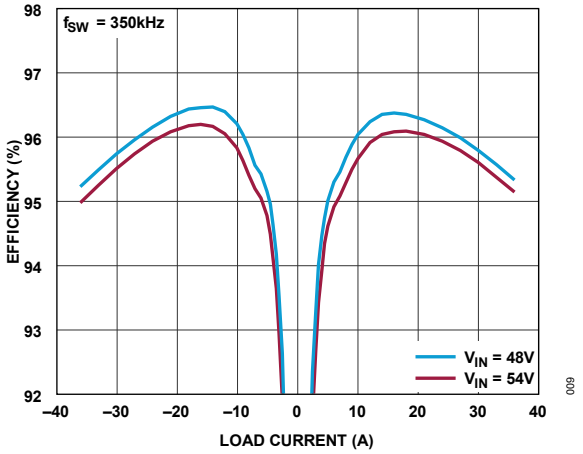


Figure 9. Efficiency vs. Load Current, V_{OUT} = 7.5V

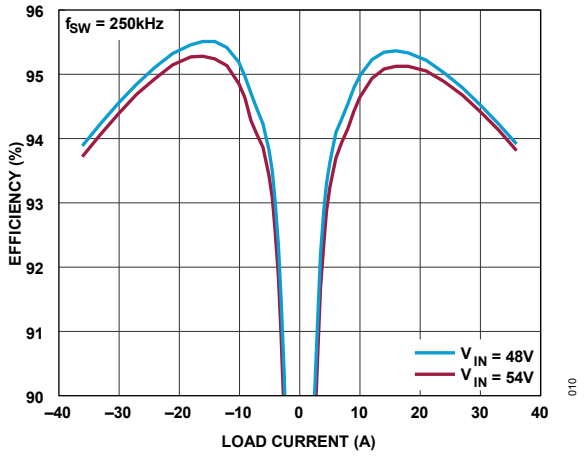


Figure 10. Efficiency vs. Load Current, V_{OUT} = 5V, $EXTV_{CC}$ = 8V

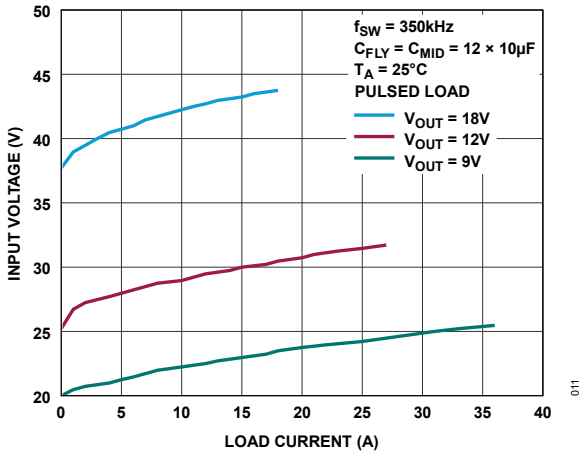


Figure 11. Minimum V_{IN} for Typical V_{OUT} Applications

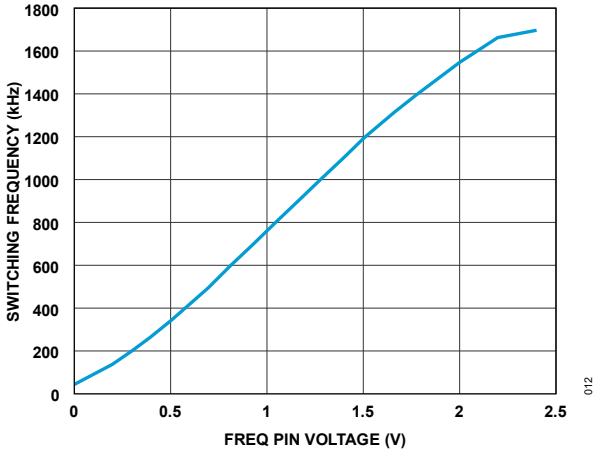


Figure 12. Switching Frequency vs. Voltage at FREQ Pin

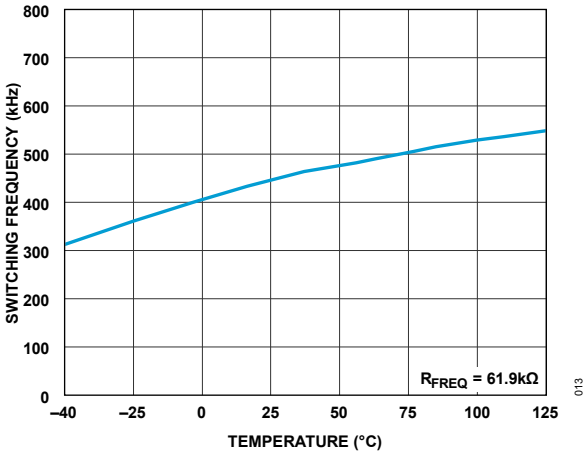


Figure 13. Oscillator Frequency vs. Temperature

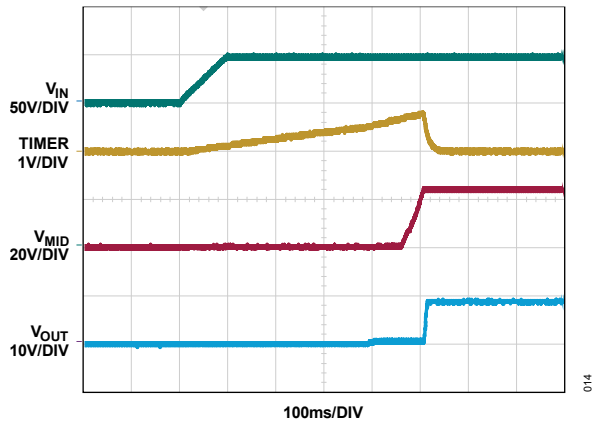


Figure 14. Startup Characteristics, V_{IN} = 48V, V_{OUT} = 9V

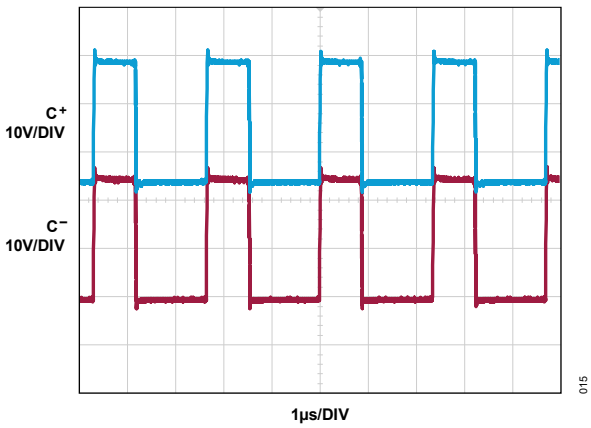
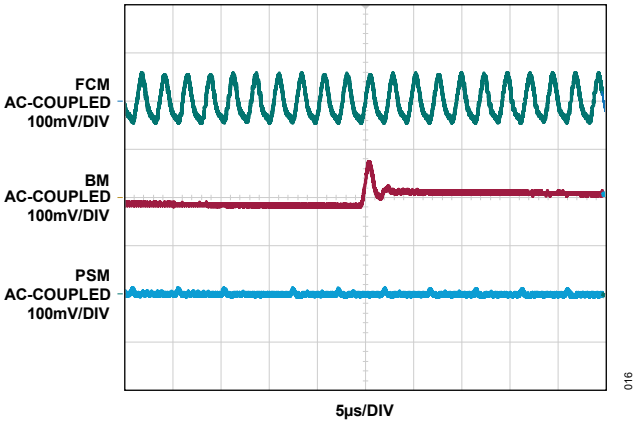
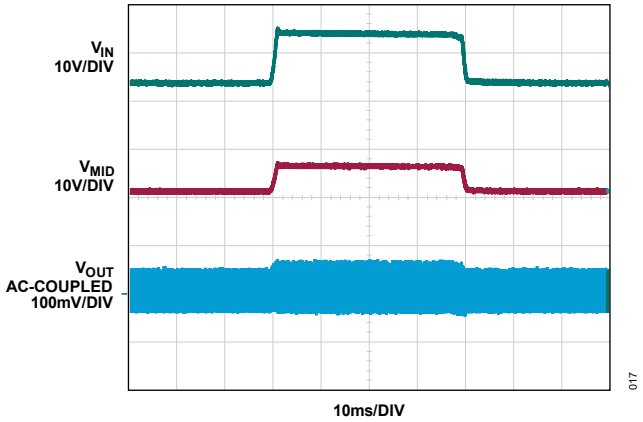


Figure 15. Steady-State Waveforms, V_{IN} = 48V, V_{OUT} = 9V, FCM



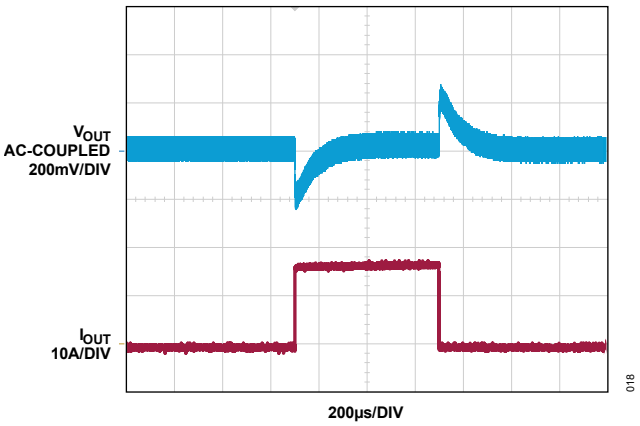
V_{IN} = 48V
V_{OUT} = 9V
I_{OUT} = 50mA
C_{OUT} = 2 × 150µF + 3 × 10µF

Figure 16. Steady–State Output Voltage Ripple



V_{IN} = 44V TO 54V TO 44V
V_{OUT} = 9V
P_{OUT} = 300W
C_{OUT} = 2 × 150µF + 3 × 10µF

Figure 17. Line Transient, V_{IN} Slew Rate = 10V/ms



V_{IN} = 48V
V_{OUT} = 9V
C_{OUT} = 2 × 150µF + 3 × 10µF
COMPa CONNECTED TO COMPb

Figure 18. Load Transient, 150W to 300W to 150W

THEORY OF OPERATION

LTM4654 Power µModule Overview

The LTM4654 is a high-efficiency, bidirectional (source/sink), intermediate bus converter (IBC) utilizing a hybrid-switched capacitor topology. Four power switches and the capacitor banks, C_{FLY} and C_{MID}, form a switched capacitor stage, dividing the input voltage by two at MID. The voltage at MID is further stepped down through a power inductor and an output capacitor, like a step-down switching converter. The LTM4654 employs peak current mode control of the inductor current for pulse-width modulation (PWM) of the switches and to maintain accurate output regulation. Soft switching of the power switches results in excellent efficiency and electromagnetic interference (EMI) performance.

The current mode control enables fast cycle-by-cycle current limiting of the inductor current and hence protects the internal components of LTM4654 during short-circuit conditions. With current mode control, the LTM4654 exhibits good transient performance and stability margins for a wide range of output capacitors. An internal compensation network included inside the LTM4654 is sufficient for most typical applications. The V_{FB} pin is used to program the output voltage with a single resistor to ground.

The switching frequency can be programmed by a single resistor connected between the FREQ pin and SGND. The typical switching frequency range for IBC applications with the LTM4654 is 300kHz to 500kHz. A phase-locked loop inside the power module enables synchronizing the switching frequency to an external clock.

Pulling the RUN pin below 1.1V forces the regulator into a shutdown state by turning off all the switching and all the internal circuits. The TRACK/SS pin is used to program the output voltage ramp and the voltage tracking during startup. The internal bandgap reference of 0.8V can be overridden by applying a suitable voltage at the EXT_REF pin. See the *Applications Information* section for more details.

A general-purpose temperature diode is included to monitor the internal temperature of the power module. In addition, the TEMP pin is used to program the overtemperature (OT) protection trip point. Internal overvoltage (OV) and undervoltage (UV) comparators pull the open-drain PGOOD output low if the output feedback voltage exits the regulation window.

The capacitor banks C_{FLY} and C_{MID}, externally connected to the power module, are also part of the energy transfer elements. The LTM4654 utilizes these capacitor banks to efficiently deliver energy from input to output. These capacitors are initially charged in the capacitor balancing phase using Analog Devices' proprietary control techniques. This balancing eliminates large transient currents seen in similar switched capacitor-based topologies. The voltages of capacitor banks are continuously monitored and balanced by the LTM4654. Dedicated pins, TIMER and HYS_PRGM, are provided to set the balancing time interval and the voltage window and can be adjusted for each application of the LTM4654. Following the balancing phase, regular switching action starts. During each switching cycle, the capacitor C_{FLY} is connected either in series with or parallel to C_{MID}. See the *Applications Information* section for more information.

Block Diagram

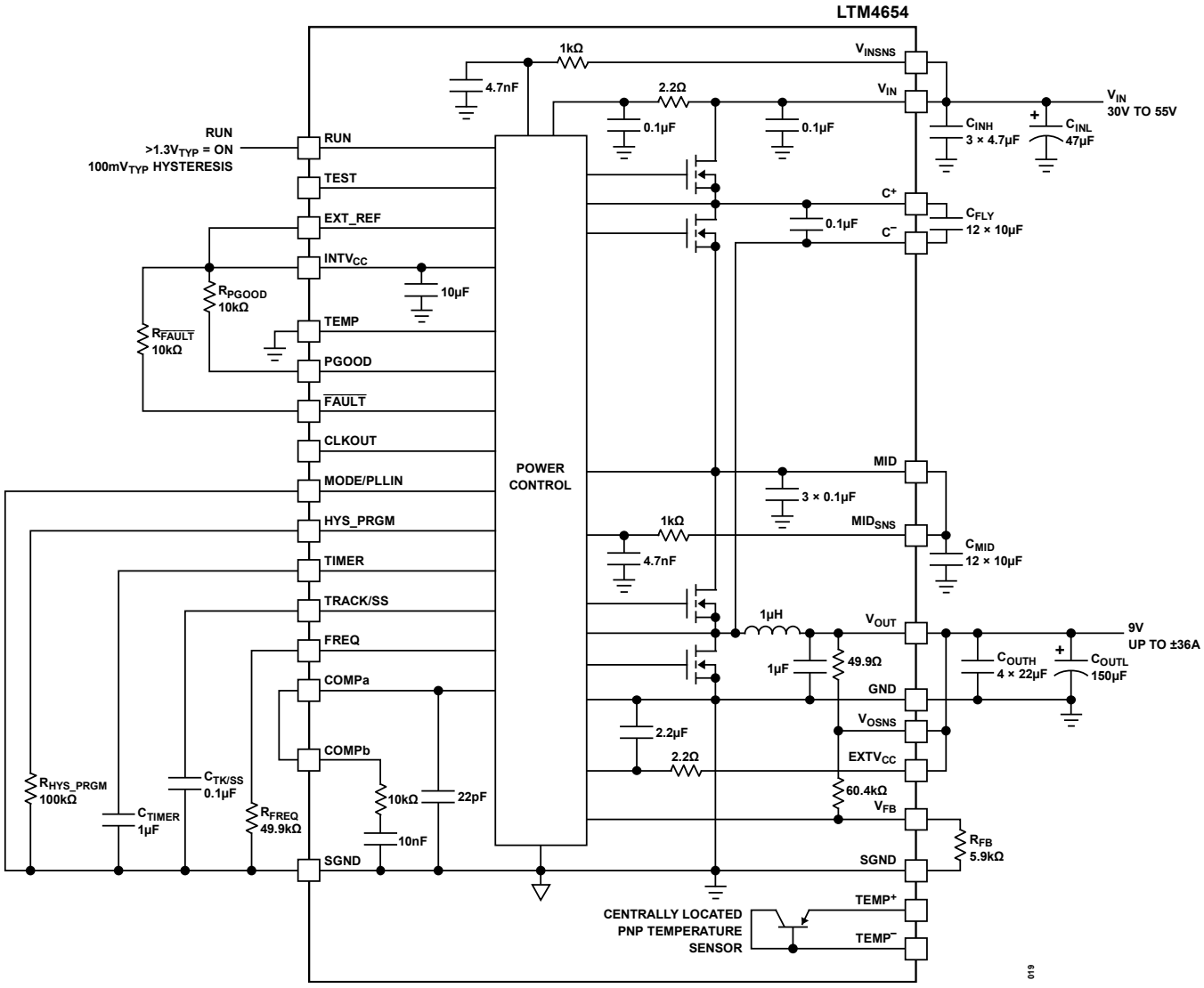


Figure 19. Simplified Block Diagram

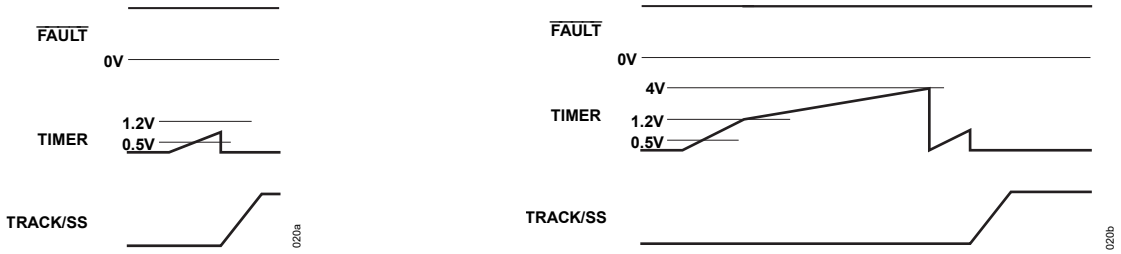
Table 6. Decoupling Requirements

T_A = 25°C. See *Figure 19* (Block Diagram).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{FLY}	External flying capacitor requirement, 30V ≤ V_{IN} ≤ 55V, V_{OUT} = 9V	P_{OUT} = 300W[4]	80	100	120	µF
C_{MID}	External midpoint capacitor requirement, 30V ≤ V_{IN} ≤ 55V, V_{OUT} = 9V	P_{OUT} = 300W[4]	80	100	120	µF
C_{OUT}	External output capacitor requirement, 30V ≤ V_{IN} ≤ 55V, V_{OUT} = 9V	P_{OUT} = 300W[4]		150		µF

Capacitor Balancing Phase

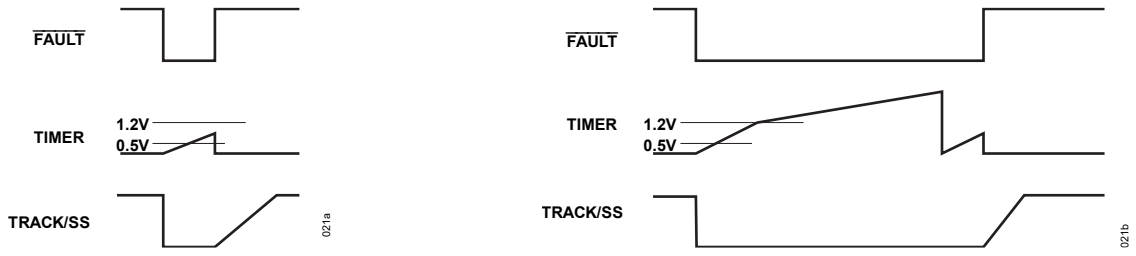
During the initial power-up, the voltage across the flying capacitors, C_{FLY} and C_{MID}, are measured. If either of these voltages are not at $V_{IN}/2$, the TIMER's capacitor is allowed to charge up. When the TIMER capacitor's voltage reaches 0.5V, the internal current sources are turned ON to bring the C_{FLY} voltage to $V_{IN}/2$. After the C_{FLY} voltage has reached $V_{IN}/2$, C_{MID} is then charged to $V_{IN}/2$. The TRACK/SS pin is pulled low during this phase. The $\overline{FAULT}$ pin does no pull low during this initial power-up. If the voltages across C_{FLY} and C_{MID} reach $V_{IN}/2$ before the TIMER capacitor's voltage reaches 1.2V, the TRACK/SS is released and allowed to charge up. The TIMER pin resets to ground and remains there. Normal operation starts (see *Figure 20*a). If, however, the C_{FLY} and the C_{MID} voltage are not at $V_{IN}/2$ when the V_{TIMER} reaches 1.2V, the internal current sources are turned OFF, and the TIMER capacitor is charged at half the initial rate until it reaches 4V. The TIMER then resets to zero, and the LTM4654 repeats the above process until the C_{FLY} and C_{MID} are at $V_{IN}/2$ (see *Figure 20*b).



(a) Completed Within One Timer Period ***(b) Completed in More Than One Timer Period***

Figure 20. Charge Balancing During Power-Up

During normal operation, only the C_{MID} is monitored for deviation away from $V_{IN}/2$ by a window amount set by a resistor connected from HYS_PRGM to ground. The voltage across this resistor sets the same amount of window threshold above and below the $V_{IN}/2$. If the V_{CMID} leaves this voltage window, all the switching stops, and the TRACK/SS pin is pulled low. The corresponding internal current sources are turned ON to bring the C_{FLY} and C_{MID} voltages back to $V_{IN}/2$. The $\overline{FAULT}$ pin is pulled low and released once the balancing is complete. During this balancing period, PGOOD is also pulled low. The TRACK/SS pin is also allowed to charge up after the completion of the balancing (see *Figure 21*a and *Figure 21*b). Connecting the HYS_PRGM to $INTV_{CC}$ sets the window threshold to ±0.8V around $V_{IN}/2$.



(a) Completed Within One Timer Period ***(b) More Than One Timer Period***

Figure 21. Charge Balancing During Normal Operation

Main Control Loop

Once the capacitor balancing phase is complete, the normal operation starts. Power switches are turned ON/OFF based on the peak current in the power inductor. The peak inductor current is controlled by the voltage on the COMPa pin, which is the output of a transconductance error amplifier. The V_{FB} pin receives the voltage feedback signal from V_{OUT}, which is compared to the internal reference voltage by the error amplifier. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference voltage, which in turn causes the COMPa voltage to increase until the average inductor current matches the new load current.

During each switching cycle, capacitor C_{FLY} is connected in series with or parallel to C_{MID}. The voltage at C^+ alternates between V_{IN} and $V_{IN}/2$, whereas voltage at C^- alternates between $V_{IN}/2$ and ground. The voltage at MID and across C_{FLY} each is approximately at $V_{IN}/2$.

APPLICATIONS INFORMATION

The Typical Application shown in *Figure 1* is a basic LTM4654 application circuit.

$INTV_{CC}/EXTV_{CC}$ Power

The power for the power switch drivers and for most of the internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is grounded or connected to a voltage less than 7V (typical), an internal 5.8V linear regulator supplies $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is taken above 7V (typical), this linear regulator is turned OFF, and another 5.8V linear regulator turns ON to provide the $INTV_{CC}$ power from $EXTV_{CC}$. The $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high-efficiency external source, resulting in an overall increase in the LTM4654 efficiency. For the LTM4654 applications where V_{OUT} is no lower than 7.5V (ideally 8V for additional safety margin), $EXTV_{CC}$ can be directly connected to V_{OUT}.

Shutdown and Startup

When the RUN pin is below 1.1V, the $INTV_{CC}$ linear regulator and all the internal circuitry, including the main control loop, enter shutdown mode. Releasing the RUN pin allows an internal 1µA current source to pull the RUN pin up, thus enabling the LTM4654. The RUN pin can also be driven directly by logic if this voltage does not exceed the absolute maximum rating of 6V.

The slew rate of the output voltage V_{OUT} can be controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the internal reference voltage of 0.8V (or EXT_REF if this feature is utilized), the LTM4654 regulates the V_{FB} voltage to the TRACK/SS voltage instead of to the reference voltage. This allows the TRACK/SS pin to be used to program the soft start period by connecting an external capacitor from the TRACK/SS pin to SGND. After the capacitor balancing phase of the LTM4654 completes, an internal 10µA pull-up current charges the soft start capacitor, creating a voltage ramp. As the voltage on this pin rises linearly from 0V to the reference voltage (and beyond), the output voltage V_{OUT} rises smoothly from zero to the final set value. Note that the soft start is achieved not by limiting the maximum output current of the LTM4654, but by controlling the output ramp voltage according to the ramp rate at the TRACK/SS pin. The total soft start time can be calculated using Equation *1*.

$$t_{SOFT\ START} = (0.8V\ or\ V_{EXT\_REF}) \times \frac{C_{SS}}{10\mu A} \qquad (1)$$

A 0.1µF capacitor connected between TRACK/SS pin and SGND would be sufficient for most typical IBC applications using the LTM4654.

Output Voltage Tracking

Alternatively, the TRACK/SS pin allows the startup of the V_{OUT} to track that of another supply. Typically, this requires connecting the TRACK/SS pin to an external resistor divider from the other supply to ground. Tracking can be configured to be either coincident or ratio-metric, as shown in *Figure 22*a and Figure 22b. In the following discussions, V_{OUT1} refers to another supply's output while V_{OUT2} refers to the LTM4654 output that tracks V_{OUT1}. To implement the coincident tracking in *Figure 22*a, connect the resistor dividers, R1 and R2, between the external supply V_{OUT1} and ground, and connect their midpoint to the TRACK/SS pin of the LTM4654 (see Figure 22a). The ratio of this divider should be the same as that of the subordinate channel's feedback divider, which is given by Equation *2*. In this tracking mode, V_{OUT1} must be higher than V_{OUT2}. This ensures that the final voltage on the TRACK/SS pin exceeds 0.8V.

$$\frac{R_1}{R_2} = \frac{60.4k\Omega}{R_{VFB}} \qquad (2)$$

Similarly, to implement the ratio-metric tracking shown in *Figure 22*b, connect the resistor dividers, R1 and R2, from the external supply to the TRACK/SS pin of the LTM4654 (see *Figure 23*b). Select R1 and R2 so that when the external

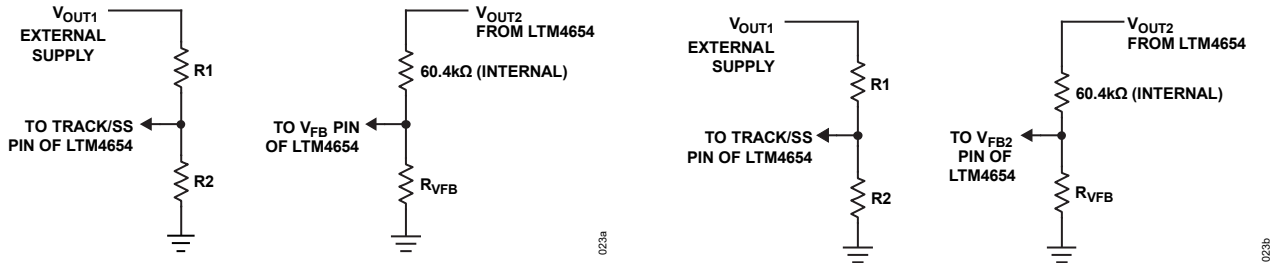
supply reaches the steady state, the final voltage on the TRACK/SS pin does not exceed 0.8V. Use this final voltage to select the FB resistor, R_{VFB}. The output voltage V_{OUT2} of the LTM4654 which ratiometrically tracks the external supply voltage V_{OUT1} is given by Equation 3.

$$V_{OUT2} = V_{OUT1} \frac{1 + \frac{60.4k\Omega}{R_{VFB}}}{1 + \frac{R_1}{R_2}} \quad (3)$$

To track down another supply after soft start has reached 82.5% of 0.8V or V_{EXT_REF}, it is recommended to set the LTM4654 into FCM operation by setting the MODE/PLLIN pin to 0V. By selecting different resistors, the LTM4654 can achieve different modes of tracking, including the two shown in *Figure 22*a and *Figure 22*b. The ratio-metric mode has a lesser output accuracy on V_{OUT2} but is fully coupled to any variations in V_{OUT1}. In both tracking modes, there is an error in the output voltage setting caused by the pin current of TRACK/SS. To minimize this error, use smaller resistor values in the divider.

Coincident Tracking ***Ratio-Metric Tracking***

Figure 22. Two Different Methods of Output Voltage Tracking



Coincident Tracking Setup ***Ratio-Metric Tracking Setup***

Figure 23. Setup for Coincident and Ratio-Metric Tracking

Burst Mode Operation, Pulse-Skipping Mode, or Forced Continuous Mode

The LTM4654 can be enabled to enter high-efficiency Burst Mode operation, pulse-skipping mode (PSM), or forced continuous mode (FCM). To select FCM operation, connect the MODE/PLLIN pin to SGND. To select the PSM of operation, connect the MODE/PLLIN pin to $INTV_{CC}$. To select the Burst Mode operation, float the MODE/PLLIN pin.

When the controller is enabled for the Burst Mode operation, and if the average inductor current is higher than the load current, the error amplifier decreases the voltage on the COMPa pin. When the COMPa voltage drops below 0.5V, the internal sleep signal goes high (enabling sleep mode), and the switching is turned off. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the voltage on the COMPa pin rises. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the power switches in the next cycle of the internal oscillator. When a controller is enabled for the Burst Mode operation, the controller operates in discontinuous operation.

In FCM operation, the peak inductor current is determined by the voltage on the COMPa pin. Switching frequency is constant as set by the R_{FREQ} resistor, and the inductor current remains continuous through the switching period. In this mode, the efficiency at light loads is lower than in the Burst Mode operation. However, the continuous mode has the advantages of a faster response to load transients and lower output ripple noise.

When the MODE/PLLIN pin is connected to $INTV_{CC}$, the LTM4654 operates in pulse-skipping mode (PSM) at light loads. At very light loads, switching is off for a few numbers of cycles (i.e., skipping pulses), and the inductor current is not allowed to reverse (discontinuous operation). This mode, like FCM, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to the Burst Mode operation. At light loads, PSM provides higher efficiency than FCM, but not as high as the Burst Mode operation. Regardless of which mode is selected by the MODE/PLLIN pin, the LTM4654 always operates in PSM during startup.

Frequency Selection and Phase-Locked Loop

The switching frequency of the LTM4654 can be selected using the FREQ pin. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 200kHz to 1MHz. There is a 10µA current flowing out of the FREQ pin, so that the user can program the controller's switching frequency with a single resistor to SGND. *Figure 24* shows the variation of switching frequency versus a resistor connected from the FREQ pin to SGND. For a typical data center IBC application of the LTM4654 with V_{IN} = 48V or 54V bus voltage and with V_{OUT} = 9V or 12V, choose the FREQ resistor to be 40kΩ to 60kΩ for maximum efficiency.

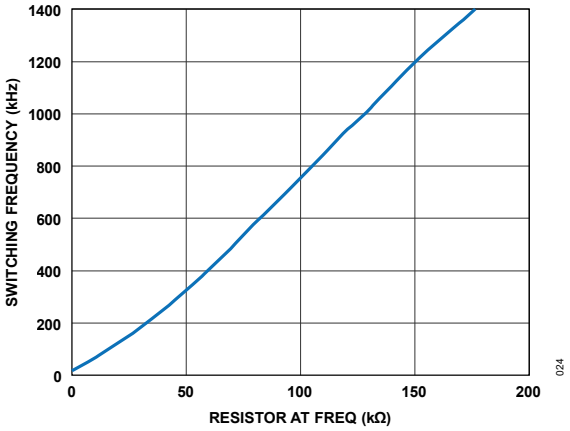


Figure 24. Variation of Switching Frequency vs. Resistor Connected from FREQ Pin to SGND

A phase-locked loop (PLL) is integrated on the LTM4654 to synchronize the internal oscillator to an external clock source that is connected to the MODE/PLLIN pin. The rising edge of the C^- pin synchronizes to the rising edge of the

external clock source. The controller operates in FCM when it is synchronized. The phase-locked loop is capable of locking any frequency within the range of 200kHz to 1MHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock.

Temperature Monitoring

The LTM4654 can provide hotspot monitoring through the TEMP pin. By using a positive temperature coefficient (PTC) thermistor as the lower leg of a resistor divider and connecting the common point of this divider to the TEMP pin, the voltage increases drastically when the temperature reaches beyond the Curie point of the PTC thermistor, as shown in *Figure 25*. The characteristics of the PTC thermistor are shown in *Figure 26*. When the TEMP pin reaches 1.22V, all switching stops for 100ms.

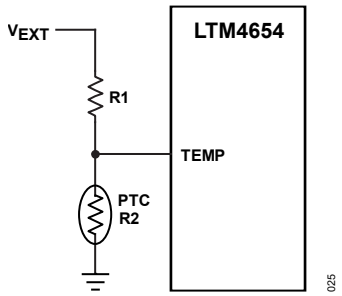


Figure 25. Temperature Monitoring Setup

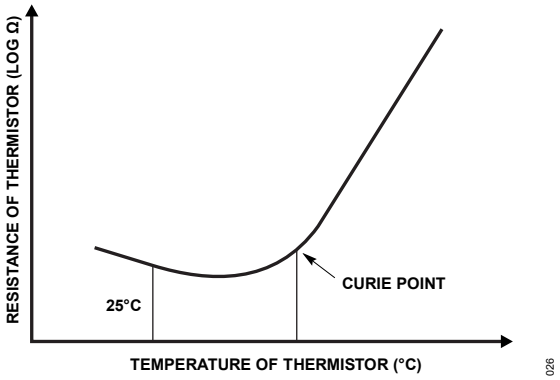


Figure 26. Characteristics of a Thermistor

The voltage on the TRACK/SS pin and $\overline{\text{FAULT}}$ pin is pulled low and is released after 100ms (see *Figure 27*), if the voltage on the TEMP pin goes below 1.1V during this 100ms timeout. If the TEMP pin voltage remains above 1.1V, the timeout period is extended until the voltage drops below 1.1V. The temperature that triggers the hotspot protection determines the thermistor selection. This temperature is the Curie point of the thermistor, which is often defined as having two times its resistance at 25°C. With the Curie point resistance of the thermistor known, $R2_{CURIE}$, the upper resistance, R1, can be selected by Equation *4*.

$$R1 = R2_{CURIE} \frac{V_{EXT} - 1.22V}{1.22V} \qquad (4)$$

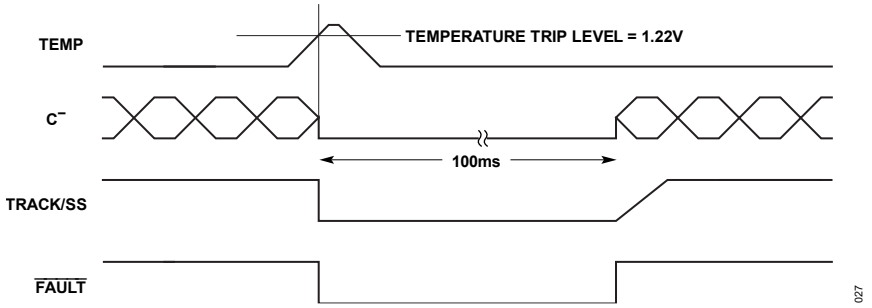


Figure 27. Temperature Trip Characteristics

A diode-connected PNP transistor is connected internally between the $TEMP^+$ and $TEMP^-$ pins. The transistor is centrally located inside the LTM4654, near the hotspot. The voltage measured across the $TEMP^+$ and $TEMP^-$ pins provides a close estimate of the internal temperature of the LTM4654. For accurate temperature sensing in this way, it is recommended to apply a DC current as I_{TEMP^+} = 100µA (sinking into $TEMP^+$ pin) and I_{TEMP^-} = –100µA (sourcing out of $TEMP^-$ pin) and measure the differential voltage across these two pins. A filter capacitor is also recommended between these two pins. The typical differential voltage across these two pins is around 0.6V at room temperature, with a -2mV/°C typical temperature coefficient.

Power Good

When the V_{FB} pin voltage falls below 7.5% or rises above 8.5% of the internal 0.8V reference or the reference set by EXT_REF, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when the RUN pin is below 1.1V or when the LTM4654 is in the soft start or tracking phase. The PGOOD pin flags power good immediately when the V_{FB} pin is within the reference window. However, there is an internal 50µs power bad mask when V_{FB} goes out this window. The PGOOD pin can be pulled up by an external resistor to sources of up to 20V.

$\overline{\text{FAULT}}$

During the initial power-up of the LTM4654 or when enabling the part through the RUN pin, the $\overline{\text{FAULT}}$ pin does not pull low even when C_{FLY} and/or C_{MID} need to be rebalanced to $V_{IN}/2$. But during normal operation, when rebalancing is needed, the $\overline{\text{FAULT}}$ is pulled low. Another condition that causes the $\overline{\text{FAULT}}$ to go low is thermal shutdown, either caused by the internal temperature reaching 150°C or the voltage at the TEMP pin reaching 1.22V. The $\overline{\text{FAULT}}$ pin can be pulled up by an external resistor to sources of up to 20V.

Stability Compensation

The LTM4654 module employs the peak current mode control for the PWM of the power switches. This method of control simplifies the compensation design by eliminating the dynamics of the power inductor contributing to the closed-loop response. A Type-II network is sufficient to compensate the LTM4654 feedback loop. Such a network comprises of a resistor in series with a capacitor connected at the COMPa pin—the output of a transconductance error amplifier inside the LTM4654, to SGND. A high-frequency roll-off capacitor of 22pF, as part of the Type-II network, is already connected at the COMPa pin internal to the LTM4654.

Component selection of the Type-II network depends on the desired output response for line and load variations and loop stability parameters—phase margin and gain margin of the feedback loop. In general, selecting a low capacitance and a high resistance for the Type-II network at the COMPa pin leads to a fast transient response, but it may adversely affect the loop stability.

A resistor-capacitor network of 10kΩ in series with 10nF is connected from the COMPb pin to SGND internal to the LTM4654. For most LTM4654's applications, it is sufficient to connect all the COMPa and COMPb pins together to

ensure closed-loop stability across line and load variations. Refer to the LTM4654 model in the LTspice® design tool to fine tune and optimize the Type-II network for each application circuit with the LTM4654.

Input Capacitor Selection

The LTM4654 module should be connected to a low AC-impedance DC source. For the regulator input, three 10µF input ceramic capacitors are required for the root mean square (RMS) ripple current up to full load. A 33µF or 47µF surface-mounted aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitance is only needed if the input source impedance is compromised by long inductive leads. If low-impedance power planes are used, then this bulk capacitor is not needed. For IBC applications with 48V or 54V bus, choose input capacitors rated to at least 100V. Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated with Equation 5.

$$I_{CIN(RMS)} = \frac{I_{OUTMAX}}{2 \times \eta\%} \sqrt{D \times D'} \quad (5)$$

where D is $2 \times V_{OUT}/V_{IN}$ and D' = 1 – D

In Equation 5, η% is the estimated ratio of the output power to the input power of the module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor or Polymer capacitor.

Output Capacitor Selection

The LTM4654 is designed to achieve good transient response and low output voltage ripple. Choose C_{OUT} with a low Equivalent series resistance (ESR) to meet the output ripple and transient performance requirements. Place at least three 10µF output ceramic capacitors close to the V_{OUT} and GND pins. This lowers the output ripple by lowering the total ESR of the C_{OUT}. Aluminum electrolytic capacitors of at least 150µF can be placed further away as bulk output capacitors. Choose enough bulk capacitance to meet the transient specification demanded by the downstream loads. When choosing the C_{OUT}, be aware of the impact of its ESR on loop stability. Refer to LTM4654 model in the LTspice design tool to optimize and fine tune the combination of C_{OUT} for each LTM4654 application.

C_{FLY} and C_{MID} Selection

For the LTM4654 module, capacitor banks C_{FLY} and $_{CMID}$, externally connected to the module, are part of the energy transfer elements. Therefore, ceramic capacitors are attractive since they have the lowest ESR. However, care should be taken when choosing this type of capacitors. During operation, the DC voltage across C_{FLY} and C_{MID} is approximately half the V_{IN} supply; therefore, the voltage rating of the capacitors should be greater than that. As a general rule, select the voltage rating of the capacitor to be twice the operating voltage of the capacitor. For the same voltage rating and capacitance, a larger case size has a lower failure rate.

In addition, the operating temperature of the capacitors must be considered. For operating temperatures above 85°C, capacitors with the X7R dielectric need to be used, while X5R dielectric is adequate for operation below 85°C. For long-term reliability of the capacitor, keep the temperature rise of the capacitor below 20°C, preferably 10°C. The temperature rise of the capacitor is dependent on the amount of RMS current through the capacitor and the operating frequency.

Ceramic capacitors also have a large voltage coefficient, losing close to half their capacitance when the DC bias across a given capacitor is half its rated voltage. The DC bias effect on a capacitor is greater when the case size is smaller. Factor in these effects when deciding on the capacitance. The ripple voltage on C_{FLY} and C_{MID} is given by Equation 6.

$$V_{RIPPLE} = \frac{I_{OUT}}{C_{BANK} \times f_{SW}} \times \frac{2V_{OUT}}{V_{IN}} \quad (6)$$

where C_{BANK} is either C_{FLY} or C_{MID}, I_{OUT} is the output current, and f_{SW} is the switching frequency.

The ripple voltage on C_{FLY} and C_{MID} contributes significantly to the power dissipated in the LTM4654 (see *Figure 4* through *Figure 11* in the *Typical Performance Characteristics* section). As a good starting point, select enough capacitance so that the ripple on each capacitor is less than 2% of the DC bias voltage of the capacitor. For example, if the DC bias voltage of the capacitor is 24V, keep the ripple to be less than 480mV. To achieve the lowest loss in the LTM4654, select the capacitance of CMID to be the same as that of C_{FLY}.

The LTM4654 is designed to deliver 300W of output power at $9V_{OUT}$. For maximum efficiency at 300W, use eight to twelve 10µF ceramic capacitors for each C_{MID} and C_{FLY}. Considering the voltage derating of the ceramic capacitors, for bus voltages in a range of $48V_{IN}$ to $54V_{IN}$, choose ceramic capacitors rated to at least 50V.

Timer and Capacitor Balancing Phase

The LTM4654 module uses a switched capacitor hybrid topology where the switched capacitor stage consists of the C_{FLY} and the C_{MID} capacitor banks connected, alternately, in series or in parallel through the power switches inside the LTM4654. During startup, C_{FLY} and C_{MID} capacitors are completely discharged. Starting switching with the capacitors discharged may lead to undesirably high currents through the power switches. To circumvent this phenomenon, the LTM4654 uses a patented technology to balance the charge across the C_{FLY} and C_{MID} to half of the V_{IN} during startup.

A capacitor connected at the TIMER pin to SGND defines the time-period during which LTM4654 enters the capacitor balancing phase. An internal current source at the pin charges the TIMER capacitor, generating a voltage ramp. Capacitor balancing is initiated when the voltage at this pin is between 0.5V and 1.2V. Choose this capacitor based on the maximum input voltage and the capacitance of the capacitor banks C_{FLY} and C_{MID}. Higher input voltage and higher capacitance indicate more time necessary for LTM4654 to complete capacitor balancing, hence requiring a larger TIMER capacitor. Choosing a smaller TIMER capacitor leads to LTM4654 using multiple TIMER cycles to complete capacitor charge balancing, leading to longer start-up times. A TIMER capacitor of 1µF is sufficient for V_{IN} of up to 55V and $C_{MID} = C_{FLY} = 10µF \times 12$.

For applications with strict start-up timing requirements, it is possible to speed up the process of charging the TIMER capacitor to 0.5V by applying a pre-bias voltage on the TIMER capacitor. This is achieved by adding a resistive voltage divider between $INTV_{CC}$ and SGND and connecting the TIMER capacitor between the TIMER pin and the midpoint of the voltage divider, as shown in *Figure 28*. For the voltage divider, lower resistance increases the power consumption from $INTV_{CC}$, while higher resistance gets the pre-bias voltage, more impacted by the internal current source, at the TIMER pin. A divider with 110kΩ and 10kΩ resistance values is a good design for balancing these two aspects, which provide about 0.45V pre-bias voltage on the TIMER capacitor, saving 90% of the time needed for charging this capacitor to 0.5V.

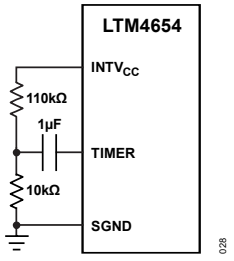


Figure 28. Reference Circuit for Speeding Up TIMER Capacitor Charging to 0.5V

HYS_PRGM Voltage

The voltage on the HYS_PRGM pin sets a window centered on $V_{IN}/2$ for fault protection purposes. During operation, if the voltage at MIDSNS deviates beyond this window, a fault is indicated, and capacitor balancing starts. Therefore, setting the correct window is important as it adds another layer of protection to the LTM4654 application circuit.

During normal operation, the voltage at MID may settle to a voltage higher or lower than $V_{IN}/2$, depending on the impedance looking into MID and the output current. In general, the higher the I_{OUT}, the higher would be the deviation of MID from VIN/2. Similarly, the lower the C_{MID} and the switching frequency, the higher the impedance looking into the MID. In addition to the DC offset of MID relative to $V_{IN}/2$, the AC ripple on CMID is also to be considered (see Equation 6 in the *CFLY and CMID Selection* section) when choosing the HYS_PRGM window.

For most LTM4654 applications, a hysteresis window of ±1V is sufficient to ensure proper operation. To set the window to ±1V, connect a 100kΩ resistor from HYS_PRGM to SGND.

Output Voltage Setting

The LTM4654 uses its internal reference of 0.8V when EXT_REF is connected to $INTV_{CC}$. The output voltage is given by Equation 7, where R_{VFB} is the feedback resistor connected from V_{FB} to SGND. Always set V_{OUT} to be less than half of the minimum expected input voltage.

$$V_{OUT} = 0.8V \times \left(1 + \frac{60.4k\Omega}{R_{VFB}}\right) \quad (7)$$

Applying a voltage on the EXT_REF pin between 0.45V and 0.9V allows the LTM4654's output to track the EXT_REF voltage, indicated by the characteristic in *Figure 29*.

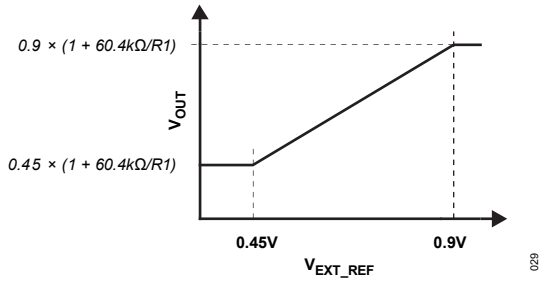


Figure 29. Output Voltage Set by EXT_REF Pin

Because of its unique architecture, the optimal efficiency for the LTM4654 is when $V_{OUT} = V_{IN}/4$. Efficiency for step-down ratios higher or lower than 4:1 may be lower. For applications that demand optimal efficiency within a range of V_{IN}, the EXT_REF pin could be used to track this V_{IN} variation while maintaining a 4:1 step-down ratio at the output. In this type of setup, the output voltage also changes with the input. *Figure 30* shows a 48V to 12V setup that accounts for the V_{IN} variation between 36V to 55V.

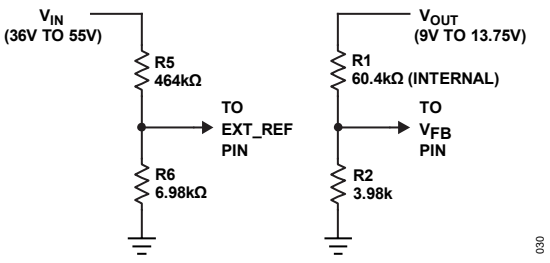


Figure 30. Output Voltage to Track V_{IN} in a 4:1 Ratio

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTM4654 can turn on its power switches. Low-duty cycle applications may approach the minimum on-time limit, and care should be taken to ensure the results given by Equation 8.

$$\frac{2V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} > t_{ON(MIN)} \quad (8)$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTM4654 starts to skip cycles. The output voltage continues to be regulated, but the ripple voltage and the current increases. The $t_{ON(MIN)}$ for the LTM4654 is approximately 210ns. To avoid running into the minimum on-time of the LTM4654 switching, it is recommended that the switching frequency be reduced between 200kHz to 400kHz for input and output step-down ratios greater than 6:1.

Maximum Duty Cycle Considerations

For stable operation, the charge balance of C_{FLY} and C_{MID} must be met for each switching cycle. To maintain such a charge balance cycle-by-cycle in the LTM4654, it requires some minimum amount of off-time for each switching cycle, which determines the maximum duty cycle of the LTM4654 for a given switching frequency. Because the existence of parasitic resistance and inductance in the charge balance loop, it usually requires longer off-time for each switching cycle as load increases, which is dependent on the layout of the circuit board on which the LTM4654 is mounted and it might be different in a case by case basis. Lower switching frequency helps to extend the maximum duty cycle.

Figure 11 include the recommended minimum V_{IN}, which represents the maximum duty cycle, based on the bench verification using the standard *DC2879A* evaluation board, with the LTM4654 mounted, covering its various typical V_{OUT} applications. It should be noted that these data were tested under pulsed load conditions with a duration of much less than 1 second. To ensure normal operation in continuously running loaded applications, consider the impact of load current and the impact of junction temperature rise on the charge balance in the LTM4654. It is recommended to further reduce the duty cycle properly.

Table 7 shows the recommended minimum V_{IN} for various typical V_{OUT} applications for the LTM4654, up to full load (300W output power or 36A DC inductor current, whichever comes first) sustained operation, validated on bench using the standard *DC2879A* evaluation board, with the ambient temperature being the room temperature. Combining with *Figure 11*, for V_{OUT} applications not listed here, interpolation is a good way to estimate the minimum V_{IN}.

Table 7. Recommended Minimum V_{IN} to Handle Full Load Sustained Operation (T_A = 25°C)

V_{OUT} (TYPICAL APPLICATION)	5V	9V	12V	18V
Recommended minimum V_{IN}	20V	30V	36V	48V

Dual Phase Operation

For higher output power applications, two LTM4654s can be paralleled to create a dual phase single output configuration. *Figure 43* shows the key signal connections between the two LTM4654 modules.

Bidirectional (Sourcing/Sinking) Power Flow

All the previously mentioned operation principles and application information are applicable to both sourcing and sinking power transfer applications.

In the sinking power transfer applications, if the input power source cannot sink power coming from the output side, then it is required to add a resistor in parallel with the input power source to sink such an amount of power. Choose a suitable resistor considering the power rating.

Negative Output Voltage Configuration

The LTM4654 can be configured in a similar way as an inverting buck-boost converter to provide a negative output voltage, which is especially beneficial to industrial applications such as ATE.

In this configuration, the positive and the negative terminals of the input voltage source are connected to the V_{IN} pin and the V_{OUT} pin of the LTM4654, respectively; the load is connected across the V_{OUT} pin and the GND pin of the LTM4654. The negative output voltage is referenced to the negative terminal of the input voltage source, meaning that the output side, the GND pin, of the LTM4654 can get a voltage level that is lower than the negative terminal of the input voltage source.

In such a configuration, define $V_{IN(NV)}$ as the voltage level at the V_{IN} pin of the LTM4654, and define $V_{OUT(NV)}$ as the voltage level at the GND pin of the LTM4654. Both definitions are referenced to the V_{OUT} pin of the LTM4654, meaning that $V_{IN(NV)}$ is positive and that $V_{OUT(NV)}$ is negative. With such definitions, the voltage stress seen by the LTM4654 from the V_{IN} pin to the GND pin in this configuration is ($V_{IN(NV)}$ + $|V_{OUT(NV)}|$), which is recommended to stay no higher than 55V. The voltage stress across the capacitors C_{FLY} and C_{MID} is ($V_{IN(NV)}$ + $|V_{OUT(NV)}|$)/2.

Theoretically, the operation in the LTM4654 in such configuration is equivalent to a positive–V_{OUT} hybrid converter with ($V_{IN(NV)}$ + $|V_{OUT(NV)}|$) as the input voltage, and $|V_{OUT(NV)}|$ as the output voltage, referenced to the GND pin of the LTM4654, thus having the identical inductor current in both cases. Therefore, the duty cycle D (NV) is determined by Equation *9*.

$$D(NV) = \frac{2\left|V_{OUT(NV)}\right|}{V_{IN(NV)} + \left|V_{OUT(NV)}\right|} \qquad (9)$$

Comparing with a positive–V_{OUT} hybrid converter, the main difference is the location of the input voltage source, making the inductor current in such a configuration equal to the summation of the input current and the load current. Therefore, the relation between the load current and the DC inductor current, in this case, is determined by the Equation *10*, where η% is the ratio of the output power to the input power of the power module.

$$I_{OUT} = I_{L(DC)} \times \frac{V_{IN(NV)} \times \eta\%}{V_{IN(NV)} \times \eta\% + \left|V_{OUT(NV)}\right|} \qquad (10)$$

In this configuration, the load current is lower than the DC inductor current, dependent on the input voltage, output voltage, and efficiency of the power module, because part of the inductor current serves as the circulating current. The efficiency data in the *Typical Performance Characteristics* section at various (positive) output voltage and load current conditions are good references to make an estimation about the efficiency in the negative output voltage configuration.

It is recommended that the current and output power load, in such a configuration, meet the following two conditions simultaneously. First, the DC inductor current must not exceed ±36A. Second, the product of the DC inductor current and the output voltage (an equivalent power) must not exceed ±300W.

Similar considerations about the maximum duty cycle are also applicable to this configuration. Note that the load current mentioned in the *Maximum Duty Cycle Considerations* section is equivalent to the DC inductor current in this configuration.

Based on *Table 7* and *Typical Performance Characteristics*, Table 8 shows the equivalent recommended minimum $V_{IN(NV)}$ and maximum load current for various typical $V_{OUT(NV)}$ applications for the LTM4654, up to full load (300W abovementioned equivalent power or 36ADC inductor current, whichever comes first) sustained operation, with the ambient temperature being the room temperature. Similarly, for $V_{OUT(NV)}$ applications not listed here, interpolation is a good way to make an estimation of the minimum $V_{IN(NV)}$ and the maximum load current.

Table 8. Recommended Minimum $V_{IN(NV)}$ to Handle Full Load Sustained Operation (T_A = 25°C)

VOUT(NV) (TYPICAL APPLICATION)	–5V	–9V	–12V	–18V
Recommended minimum $V_{IN(NV)}$	15V	21V	24V	30V
Recommended maximum $\|I_{OUT}\|$	26A	22A	16A	11A

With $V_{IN(NV)}$ = 30V to $V_{OUT(NV)}$ = –7V being taken as an example, *Figure 44*a shows the typical application circuit for a single-phase operation. *Figure 44*b shows the corresponding efficiency and power loss data. Similarly, bidirectional operation and multiphase parallel operation are also applicable in such a negative output voltage configuration.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the *Pin Configurations and Function Descriptions* section, which are consistent with those parameters defined by the JESD51-9. They are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a power module package mounted to a hardware test board—also defined by JESD51-9 (Refer to the Test Boards for Area Array Surface Mount Package Thermal Measurements). The motivation for providing these thermal coefficients is found in JESD51-12 (Refer to the Guidelines for Reporting and Using Electronic Package Thermal Information).

Many designers may use laboratory equipment and a test vehicle, such as the evaluation board, to anticipate the power module regulator's thermal performance in their application at various electrical and environmental operating conditions to complement any FEA activities. Without FEA software, the thermal resistances reported in the *Pin Configurations and Function Descriptions* section are in-and-of themselves not relevant to providing guidance on the thermal performance; instead, the derating curves in *Figure 33* through *Figure 38* are used in a manner that yields insight and guidance pertaining to the user's application-usage, and they can be adapted to correlate thermal performance to the user's application.

The *Pin Configurations and Function Descriptions* section typically gives three thermal coefficients explicitly defined in the JESD51-12. The following list quotes or paraphrases these three coefficients.

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. θ_{JCbot}, the thermal resistance from the junction to the bottom of the product case, is the junction-to-board thermal resistance with all the component power dissipation flowing through the bottom of the package. In a typical power module, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don't generally match the user's application.
3. θ_{JCtop}, the thermal resistance from the junction to the top of the product case, is determined with nearly all the component power dissipation flowing through the top of the package. As the electrical connections of the typical power module are at the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot}, this value may be useful for comparing packages, but the test conditions don't generally match the user's application.

A graphical representation of the thermal resistances is shown in *Figure 31*; blue resistances are contained within the power module regulator, whereas green resistances are external to the power module.

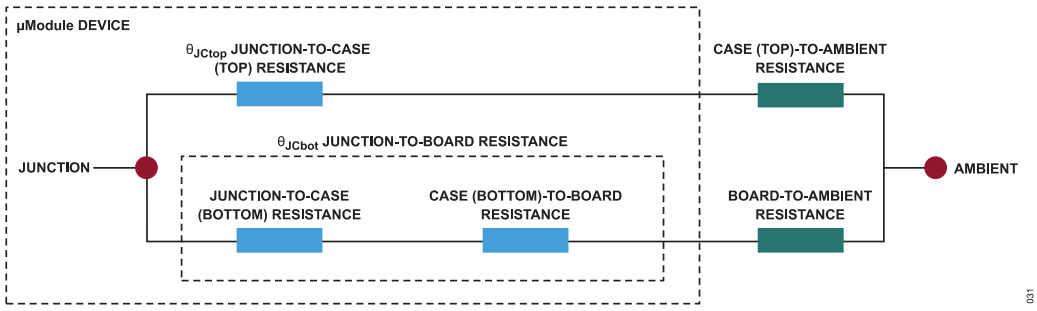


Figure 31. Graphical Representation of JESD51-12 Thermal Coefficients

As a practical matter, it should be clear to the user that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the *Pin Configurations and Function Descriptions* section replicates or conveys normal operating conditions of the power module. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the power module—as the standard defines for θ_{JCtop} and θ_{JCbot}, respectively. In practice, power loss is thermally dissipated in both directions away from the package granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, note that there are multiple power devices and components dissipating power with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to the total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using the FEA software modeling and the laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values provided in this data sheet: (1) Initially, FEA software accurately builds the mechanical geometry of the power module and the specified PCB with all of the correct material coefficients and the accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED51-9 to predict power loss heat flow.

The LTM4654 package has been designed so that the inductor on the top also doubles as a heat sink, removing heat from the power switches below. The bottom substrate material has very low thermal resistance to the printed circuit board (PCB). An external heat sink can be applied to the top of the device for excellent heat sinking with airflow.

Figure 32 shows a thermal capture of LTM4654 with 48V input, 9V output at 33A, 350kHz, 21°C ambient temperature, without heat sink and 400LFM airflow condition.

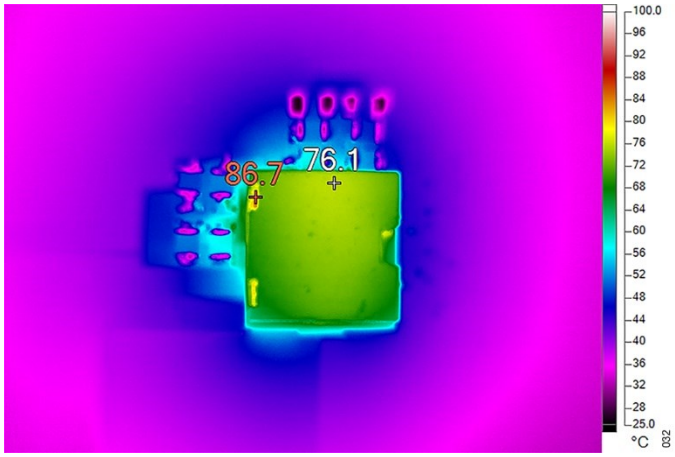


Figure 32. Thermal Image 48V to 9V, 33A, 400LFM Airflow, No Heat Sink (Based on 6-Layer PCB with 2oz Copper on All Layers)

Derating Curves

Derating curves in *Figure 33* to *Figure 38* can be used to calculate approximate values of θ_{JA} thermal resistance with various airflow conditions. Unless otherwise specified, $C_{FLY} = C_{MID} = 12 \times 10\mu F$.

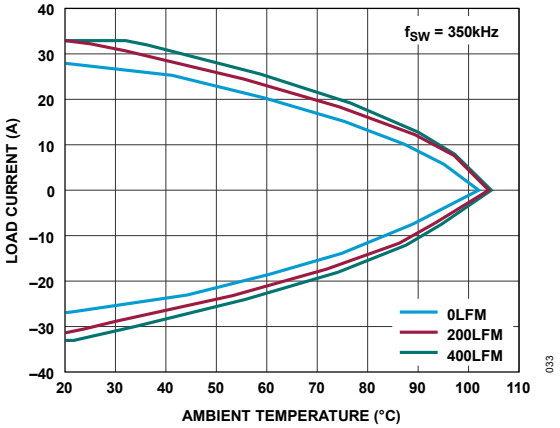


Figure 33. 48V to 9V Derating Curve, No Heat Sink

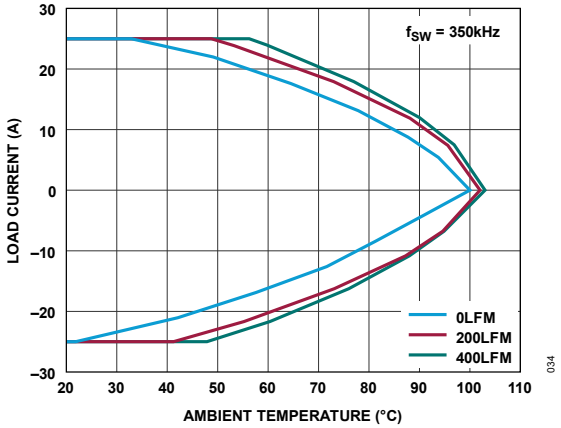


Figure 34. 48V to 12V Derating Curve, No Heat Sink

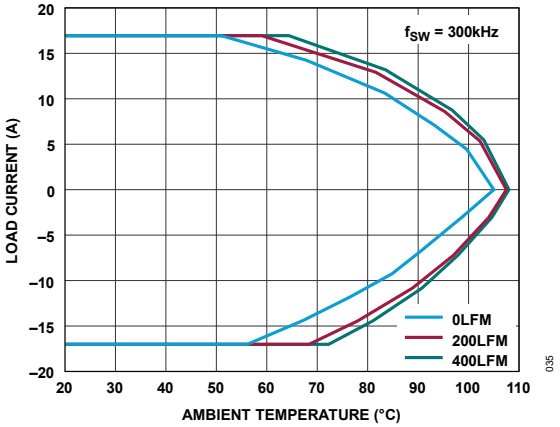


Figure 35. 48V to 18V Derating Curve, No Heat Sink

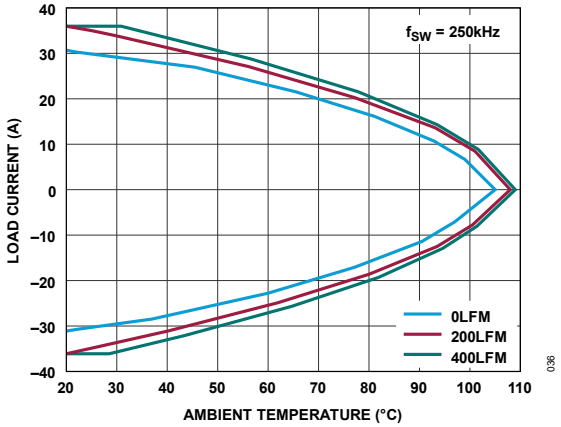


Figure 36. 48V to 5V Derating Curve, No Heat Sink

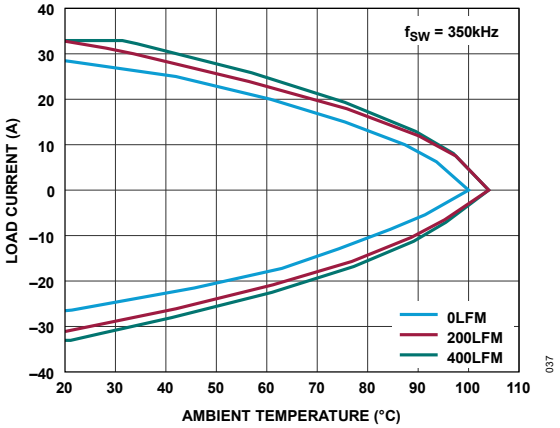


Figure 37. 48V to 9V Derating Curve, No Heat Sink, $C_{FLY} = C_{MID} = 10 \times 10\mu F$

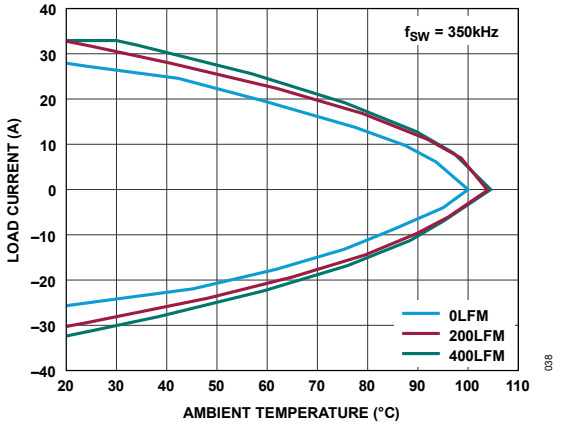


Figure 38. 48V to 9V Derating Curve, No Heat Sink, $C_{FLY} = C_{MID} = 8 \times 10\mu F$

Capacitor Selection Considerations

Table 9. Bulk and Ceramic Capacitor Manufacturers

VENDOR	VALUE	PART NUMBER	VENDOR	VALUE	PART NUMBER
C_{IN} (Bulk)			**C_{IN} (Ceramic)**		
Panasonic	33µF, 80V	EEHZA1K330	Murata	2.2µF, 100V, 1210, X7R	GRM32DR72A225KA12
			TDK		C3225X7R2A225K230AB
C_{OUT} (Bulk)			**C_{OUT} (Ceramic)**		
Panasonic	150µF, 16V	16SVPC150	Murata	10µF, 35V, 1210, X7S	GCM32EC7YA106KA03
Panasonic	120µF, 25V	25SVPK120	TDK	10µF, 25V, 1210, X7R	C3225X7R1E106K250AC
C_{FLY}, C_{MID}					
Murata	10µF, 100V, 1210, X7S	GRM32EC72A106KE05			
TDK	10µF, 100V, 1210, X7R	C3225X7R2A106K250AC			
Murata	10µF, 50V, 1210, X7S	GCM32EC71H106KA03			
TDK	10µF, 50V, 1210, X5R	C3225X5R1H106K250AB			

Table 10.Component Selection Table for Typical LTM4654 Applications

V_{IN} (V)	V_{OUT} (V)*	C_{IN} BULK (µF)	C_{IN} CERAMIC (µF)	C_{OUT} BULK (µF)	C_{OUT} CERAMIC (µF)	C_{FLY} (µF)	C_{MID} (µF)	R_{VFB} (kΩ)	R_{FREQ} (kΩ)	R_{HYS_PRGM} (kΩ)	TIMER (µF)
48	12	33	10	2 × 150	3 × 10	10 ×10	10 ×10	4.32	49.9	100	1
54	12	33	10	2 × 150	3 × 10	12 ×10	12 ×10	4.32	49.9	100	1
48	5	33	10	2 × 150	3 × 10	12 ×10	12 ×10	11.5	36.5	100	1
54	9	33	10	2 × 150	3 × 10	10 ×10	10 ×10	5.9	49.9	100	1

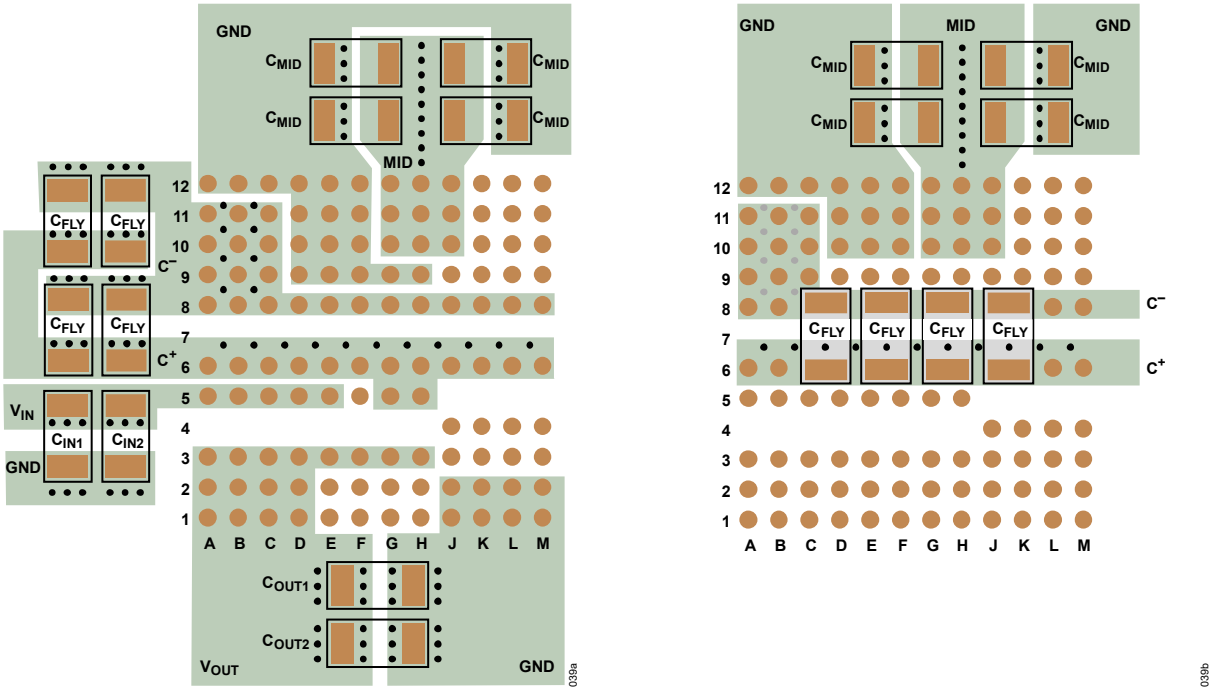
* I_{OUT} up to ±36A or P_{OUT} up to ±300W, whichever comes first.

Recommendations for PCB Layout

The high integration of the LTM4654 makes the PCB board layout simple and easy to implement. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

1. Use large PCB copper areas for high current paths, including V_{IN}, GND, and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
2. Place the high-frequency ceramic input and output capacitors next to the V_{IN}, MID, GND, and V_{OUT} pins to minimize high-frequency noise.
3. Use short loops to route C_{FLY} capacitors from C^+ to C^-. Reduce the parasitic trace inductance and resistance in this loop.
4. Place a dedicated power ground layer underneath the unit.
5. To minimize the via conduction loss and reduce the power module thermal stress, use multiple vias for interconnection between the top layer and the other power layers.
6. Do not put vias directly on the pad unless they are capped or plated over.
7. Use a separated SGND ground copper area for components that are connected to the signal pins. The SGND is connected to GND internal to the power module.
8. For parallel power modules, connect all the V_{OUT}, V_{FB}, and COMPa pins together. Use an internal layer to closely connect these pins. The TRACK/SS pin can be connected to a common capacitor for regulating the soft start.
9. Bring out test points on the signal pins for monitoring.

Figure 39 shows a recommended example for the PCB layout for input, output, C_{FLY}, and C_{MID} capacitors on the top layer. The pinout of the LTM4654 is designed so that the C_{FLY} capacitors can be conveniently placed on the bottom layer, right underneath of the power module, with minimal impact on the total PCB area.



(a) Top Layer *(b) Bottom Layer*

Figure 39.Recommended PCB Layout

Safety Considerations

The LTM4654 does not provide galvanic isolation between the input and output. There is no internal fuse. If required, a slow blow fuse with a rating of twice the maximum input current must be provided to protect each unit from catastrophic failure. The device supports overcurrent protection. The temperature diode and the TEMP pin can detect the need for a thermal shutdown, which can be done by controlling the RUN pin. The BGA pinout of the LTM4654 is such that the high voltage pins (V_{IN} and C^+) have a clearance of one BGA ball from adjacent lower voltage pins.

Radiated EMI Noise

The potential for electromagnetic interference (EMI) is inherent to all switching regulators. Fast switching turn-on and turn-off of the power MOSFETs—necessary for achieving high efficiency—creates high frequency (~30MHz +) dI/dt changes within DC-to-DC converters. This activity tends to be the dominant source of high-frequency EMI radiation in such systems. The high-level device integration within LTM4654, along with the soft switching of the power MOSFETs, deliver low radiated EMI noise performance. The EMI graph in *Figure 40* shows an example of the LTM4654 meeting radiation emission limits established by the CISPR22 Class B.

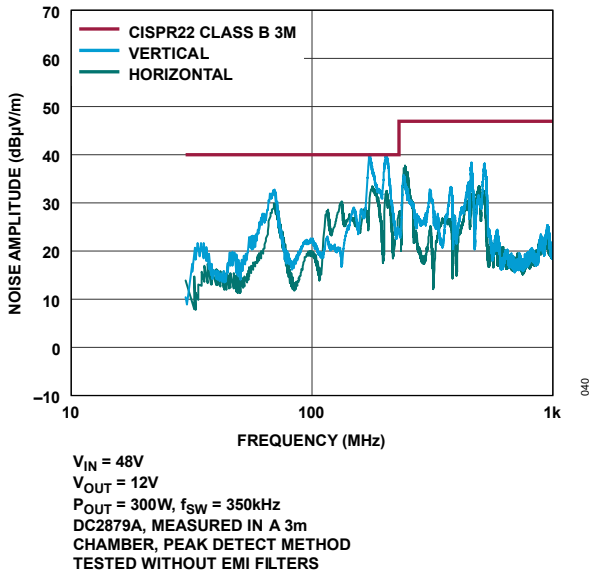
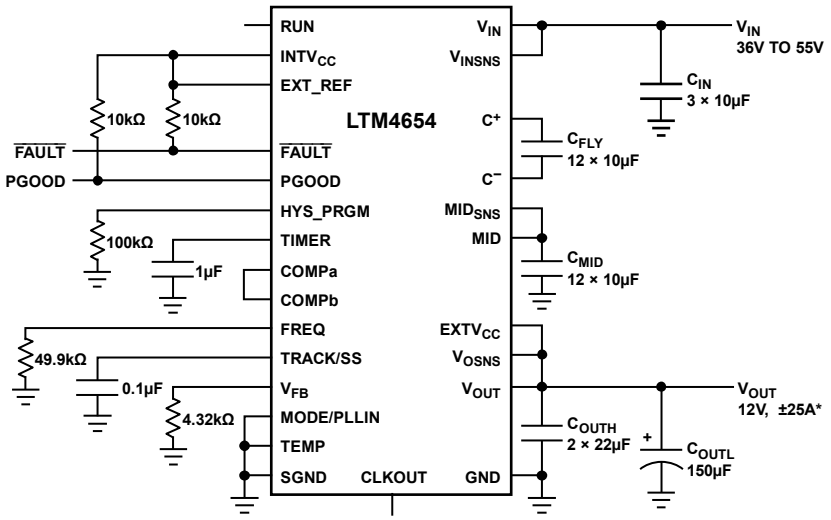


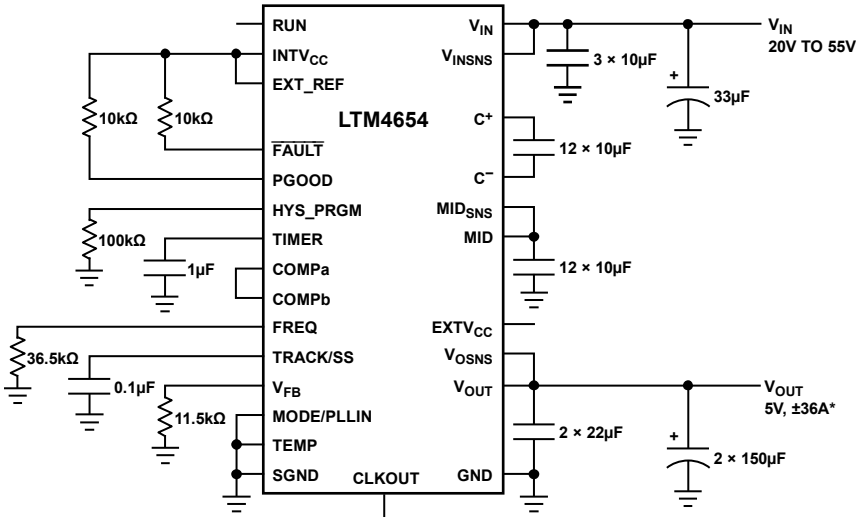
Figure 40. Radiated EMI Performance (CISPR22 Radiated Emission Test with Class B 3m Limits)

Typical Applications



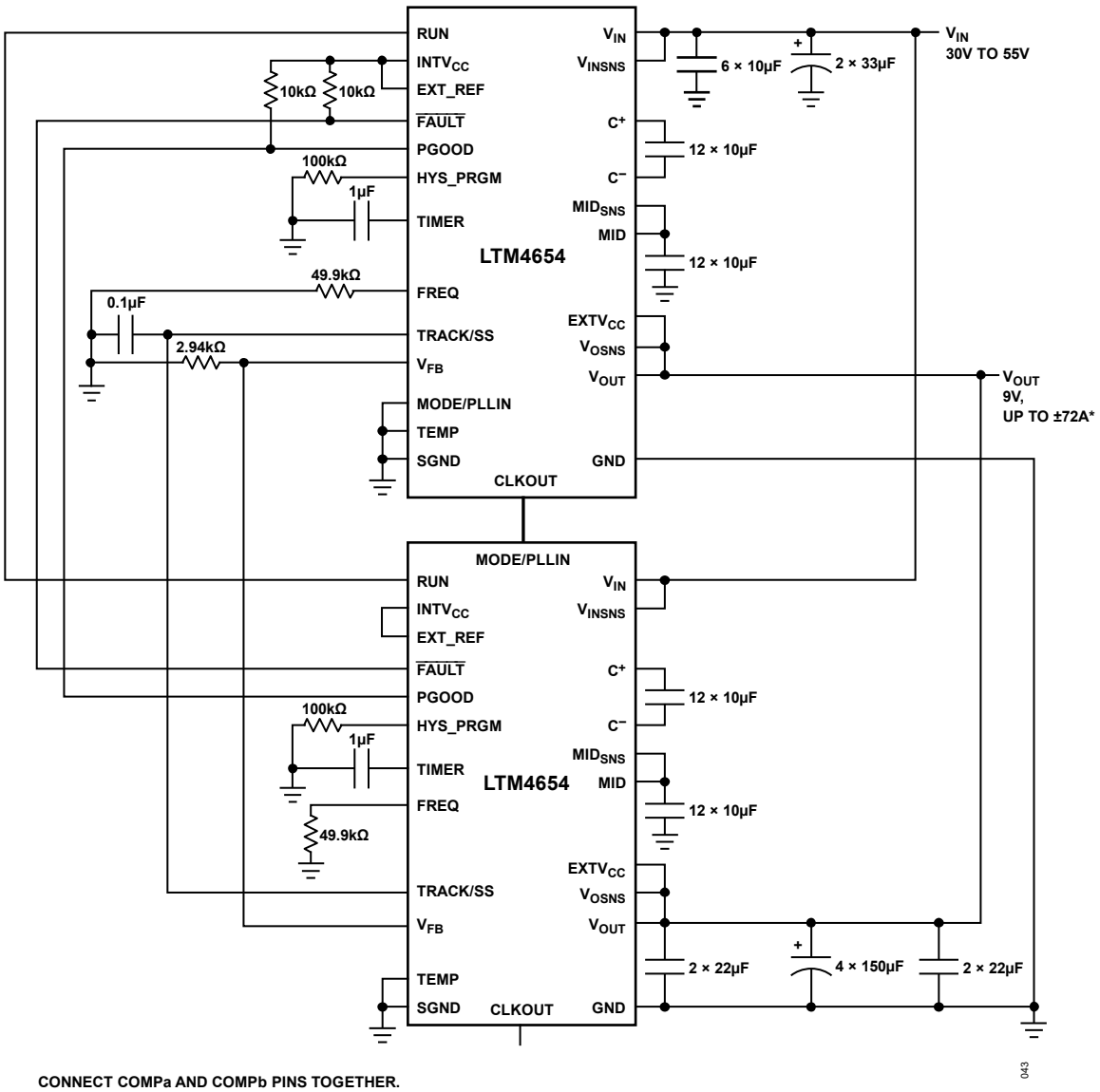
*CURRENT UP TO ±36A PEAK (NON-SUSTAINED), SUBJECT TO THERMAL CONSTRAINTS OF USER'S ENVIRONMENT AND APPLICATION. SEE THE DERATING CURVES IN THE APPLICATIONS INFORMATION SECTION.

Figure 41. 12V_{OUT}, 25A Intermediate Bus Converter



*CURRENT UP TO ±36A PEAK, SUBJECT TO THERMAL CONSTRAINTS OF USER'S ENVIRONMENT AND APPLICATION. SEE THE DERATING CURVES IN THE APPLICATIONS INFORMATION SECTION.

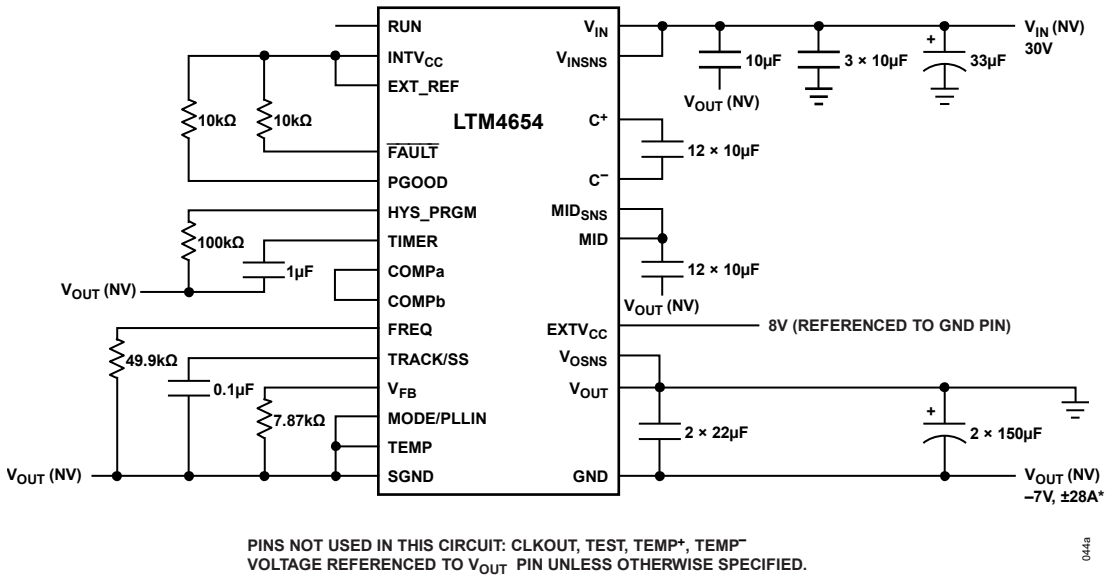
Figure 42. 5V_{OUT}, 36A Intermediate Bus Converter



CONNECT COMPa AND COMPb PINS TOGETHER.

*CURRENT UP TO ±72A PEAK (NON-SUSTAINED), SUBJECT TO THERMAL CONSTRAINTS OF USER'S ENVIRONMENT AND APPLICATION. SEE THE DERATING CURVES IN THE APPLICATIONS INFORMATION SECTION.

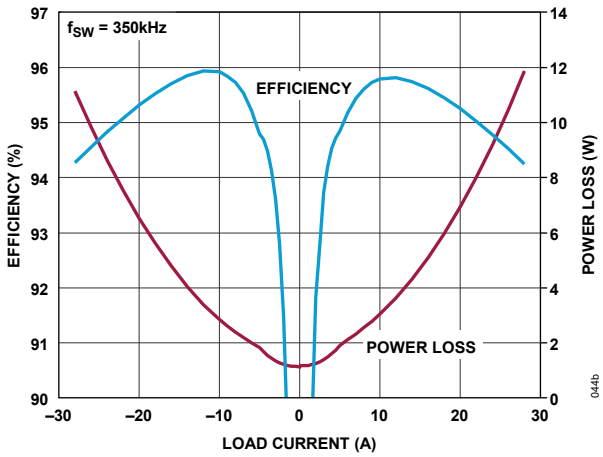
Figure 43. LTM4654 Configured for Dual Phase Operation: 9V_{OUT}, 72A Intermediate Bus Converter



PINS NOT USED IN THIS CIRCUIT: CLKOUT, TEST, TEMP+, TEMP–
VOLTAGE REFERENCED TO V_{OUT} PIN UNLESS OTHERWISE SPECIFIED.

*CURRENT UP TO ±28A PEAK (NON-SUSTAINED), SUBJECT TO THERMAL CONSTRAINTS OF USER'S ENVIRONMENT AND APPLICATION. SEE THE DERATING CURVES IN THE APPLICATIONS INFORMATION SECTION.

(a) Single-Phase Operation Negative Voltage Output



(b) Efficiency vs. Load Current, $EXTV_{CC}$ = 8V (Referenced to GND pin)

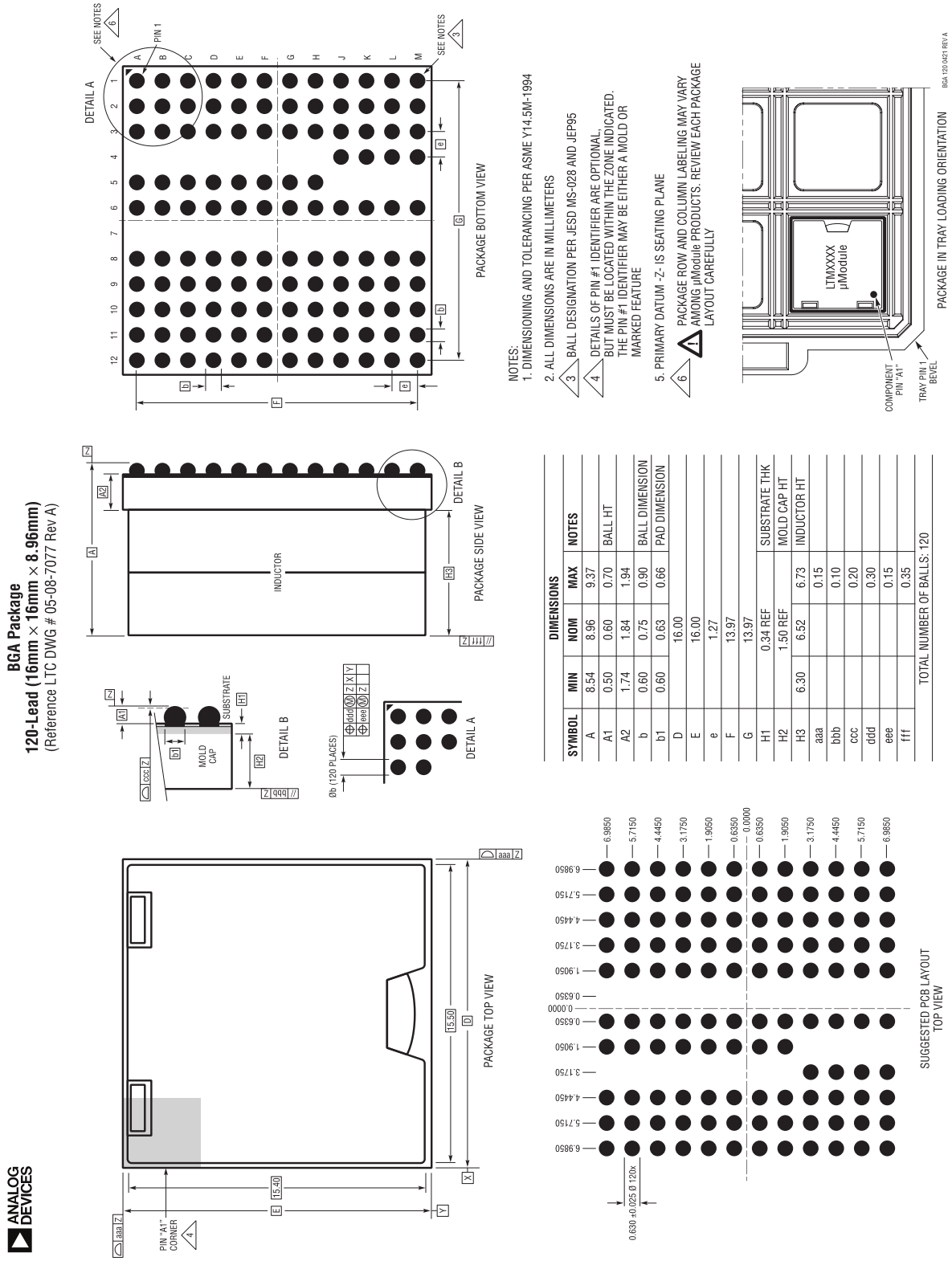
Figure 44. LTM4654 Configured for Negative V_{OUT} Operation, 30V_{IN}, –7V_{OUT}, 28A Intermediate Bus Converter

Related Parts

Table 11.Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LTM4652	Sink and source, dual ±25A or single ±50A µModule regulator	4.5V ≤ V_{IN} ≤ 18V, 0.6V ≤ V_{OUT} ≤ 7.5V, 16mm × 16mm × 4.92mm BGA
LTM4660	60V, 300W hybrid step-down µModule bus converter	30V ≤ V_{IN} ≤ 60V, 4.5V ≤ V_{OUT} ≤ 18V, 16mm × 16mm × 10.34mm BGA
LTM4664	54V_{IN} dual 25A or single 50A µModule regulator with PMBus interface	30V ≤ V_{IN} ≤ 58V, 0.5V ≤ V_{OUT} ≤ 1.5V, 16mm × 16mm × 7.72mm BGA
LTM4664A	54V_{IN} dual 30A or single 60A µModule regulator with PMBus interface	30V ≤ V_{IN} ≤ 58V, 0.5V ≤ V_{OUT} ≤ 1.5V, 16mm × 16mm × 7.72mm BGA
LTM4681	Quad 31.25A to single 125A µModule regulator with PMBus interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.3V, 15mm × 22mm × 8.17mm BGA
LTM4682	Quad 31.25A to single 125A µModule regulator with PMBus interface	4.5V ≤ V_{IN} ≤ 16V, 0.7V ≤ V_{OUT} ≤ 1.35V, 15mm × 22mm × 5.71mm BGA
LTM4683	Low profile, low V_{OUT}, quad 31.25A to single 125A µModule regulator with PMBus interface	4.5V ≤ V_{IN} ≤ 14V, 0.3V ≤ V_{OUT} ≤ 0.7V, 15mm × 22mm × 5.71mm BGA
LTM4700	Dual 50A or single 100A µModule regulator with PMBus interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 1.8V, 15mm × 22mm × 7.87mm BGA
LTM4680	Dual 30A or single 60A µModule regulator with PMBus interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.3V, 16mm × 16mm × 7.72mm BGA
LTM4678	Dual 25A or single 50A µModule regulator with PMBus interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.3V, 16mm × 16mm × 5.86mm BGA
LTM4650	Dual 25A or single 50A µModule regulator	4.5V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 1.8V, 16mm × 16mm × 5.01mm BGA
LTM4650A	Wide V_{OUT} range, dual 25A or single 50A µModule regulator	4.5V ≤ V_{IN} ≤ 16V, 0.6V ≤ V_{OUT} ≤ 5.5V, 16mm × 16mm × 5.01mm BGA, 16mm × 16mm × 4.41mm LGA

OUTLINE DIMENSIONS



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	8.54	8.96	9.37	
A1	0.50	0.60	0.70	BALL HT
A2	1.74	1.84	1.94	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		16.00		
E		16.00		
e		1.27		
F		13.97		
G		13.97		
H1		0.34 REF		SUBSTRATE THK
H2		1.50 REF		MOLD CAP HT
H3	6.30	6.52	6.73	INDUCTOR HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
fff			0.35	
TOTAL NUMBER OF BALLS: 120				

Figure 45.120-Lead, 16mm × 16mm × 8.96mm, BGA

ORDERING GUIDE

Table 12.Ordering Guide

MODEL	TEMPERATURE RANGE [1]	PACKAGE DESCRIPTION	PACKAGE OPTION
LTM4654EY#PBF	–40°C to 125°C	LTM4654Y part marking SAC305 (RoHS) pad finish* E1 finish code Moisture sensitivity level 4 (MSL 4) rated device	*120-Lead, 16mm × 16mm × 8.96mm, BGA*
LTM4654IY#PBF	–40°C to 125°C	LTM4654Y part marking SAC305 (RoHS) pad finish E1 finish code Moisture sensitivity level 4 (MSL 4) rated device	*120-Lead, 16mm × 16mm × 8.96mm, BGA*

[1] The LTM4654, including the E-grade and I-grade parts, is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4654E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4654I is guaranteed to meet specifications over the full internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

Contact the factory for parts specified with wider operating temperature ranges. *Pad finish code is per IPC/JEDEC J-STD-609. Device temperature grade is indicated by a label on the shipping container. This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to *Recommended LGA and BGA PCB assembly and manufacturing procedures.*

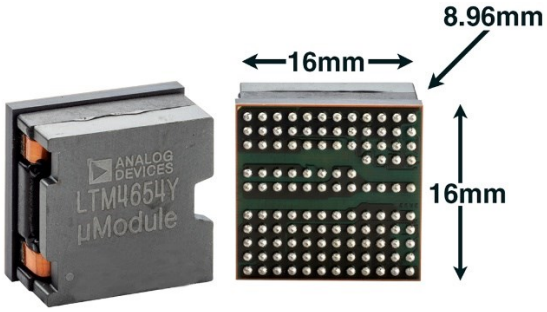
LGA and BGA package and tray drawings.

Table 13. Evaluation Boards

PART NUMBER	DESCRIPTION
EVAL-LTM4654-AZ	55V, 300W Step-Down µModule Regulator evaluation (demo) board.

SELECTOR GUIDE

Package Photos



(Part Marking Is Laser Mark)

Design Resources

Table 14.Design Resources

	SUBJECT	DESCRIPTION
µModule Design and Manufacturing Resources	**Design** ▶ Selector guides ▶ Evaluation guide boards and Gerber files ▶ Free design tools, including LTspice® and LTpowerCAD®	**Manufacturing** ▶ Quick start guide ▶ PCB design, assembly, and manufacturing guidelines ▶ Package and board level reliability
µModule Regulator Products Search	▶ Sort table of products by parameters and download the result as a spread sheet. ▶ Search using the Quick Power Search parametric table. Quick Search Input V_{in} (Min) V V_{in} (Max) V Output V_{out} V I_{out} A Features ☐ Low EMI ☐ Ultrathin ☐ Internal Heat Sink Multiple Outputs	
Digital Power System Management	The Analog Devices family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	