Data Sheet

LTM3360B

5V_{IN}, 33A High-Density Step-Down DC-to-DC µModule Regulator with I^2C and Integrated Capacitors

FEATURES

- Highest Output Current to Total Solution Footprint (1A/mm²), Integrates all C_{INs}, C_{OUTs}, and Inductors
- Fast Transient Response
- V_{IN} Range: 2.9V to 5.5V
- V_{OUT} Range: 0.3V to 1V
- Remote Differential Output Sense Pins
- V_{OUT}^+ DC accuracy: ±1%
- I^2C Serial Interface—Telemetry Readback Includes V_{OUT}, I_{OUT}, V_{IN}, and Die Temperature
- Analog IMON pin for Output Current Monitoring
- Fixed Clock Frequency of 5MHz, External SYNC from 4.5MHz to 5.5MHz
- Parallel Operation: Multiphase up to 12 phases and Stackable to > 1000A
- Advanced Thermally Enhanced *160-Lead, 6.55mm × 5mm × 3.31mm, BGA* Package

APPLICATIONS

- Data Centers xPU Core, Application-Specific Integrated Circuit (ASIC), Field-Programmable Gate Array (FPGA) Supplies
- Optical Modules
- Industrial and Communications
- Distributed DC Point-of-Load (POL) Power Systems

GENERAL DESCRIPTION

The **LTM®3360B** is a high-current, high-density, low-voltage buck power µModule® (micromodule) regulator optimized for high-output current applications. The 2.9V to 5.5V input voltage range accommodates an intermediate bus voltage (IBV) of 5V ±10% or 3.3V ±10%. The current output capability of 33A can be paralleled to provide >1000A in a multiphase, stacked from a main-to-subordinate device configuration. Regulated output voltages down to 0.3V are achieved using a current mode architecture, which is capable of small on-time at very high frequencies. Select an appropriate feedback resistor divider to configure the output voltage. The 0.3V (default) feedback voltage is 8-bit adjustable through an I^2C for margining or dynamic voltage scaling. Keep the feedback voltage close to 0.3V for the best phase-margin voltage regulation loop. The high fixed clock frequency of 5MHz which is double the switching frequency of 2.5MHz each phase permits integration of input and output capacitors and a power inductor, resulting in the highest density of output current-to-board footprint achievable in the industry today with minimal external components required. The LTM3360B is offered in a ball grid array (BGA) package, 0.4mm ball pitch, with excellent thermal performance and integrated inductors, input, and output capacitors. The LTM3360B is lead(Pb)-free and RoHS-compliant.

TYPICAL APPLICATION

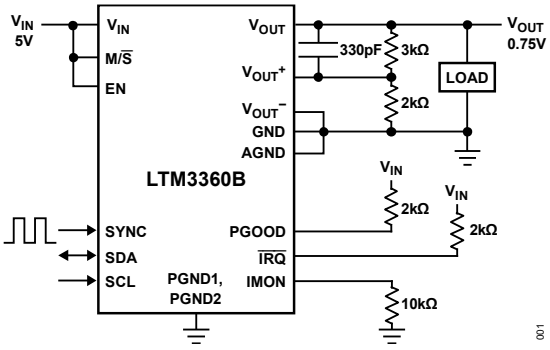

Figure 1. 5V to 0.75V at 33A, No Additional Capacitors

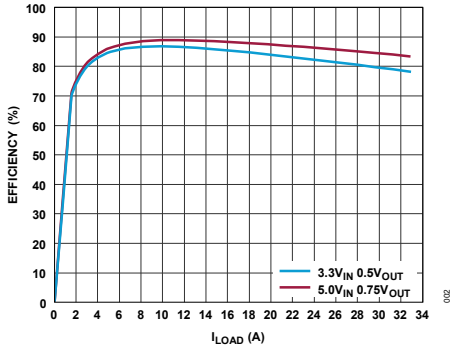

Figure 2. Efficiency vs. Current

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	11/25	Initial Release.	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{IN} = 5V and –40°C ≤ T_J ≤ 105°C unless otherwise noted. [1,2])

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Operating supply voltage (V_{IN})		2.9		5.5	V
V_{IN} undervoltage lockout	V_{IN} rising	2.70	2.75	2.80	V
V_{IN} hysteresis	T_A = 25°C		110		mV
V_{IN} quiescent current	Shutdown (not switching, V_{EN} = 0V), T_A = 25°C		5		mA
EN threshold	V_{EN} rising	1.0	1.2	1.4	V
EN hysteresis	T_A = 25°C		250		mV
EN pin leakage current	0V ≤ V_{EN} ≤ 5.5V, T_A = 25°C			±6	µA
Output Voltage Regulation					
Regulated output feedback voltage	V_{OUT}^+ = 0.3V, V_{OUT}^- = 0V, I_{OUT} = 0A, T_A = 25°C	0.297	0.3	0.303	V
Output voltage range		0.3		1	V
Continuous output current range	V_{OUT} = 0.75V, T_A = 25°C			33	A
	V_{IN} = 3.3V, V_{OUT} = 0.5V, T_A = 25°C. See *Figure 13* for different T_A values			33	A
Output current limit, peak high range	V_{OUT} = 0.75V, T_A = 25°C, average load current		46		A
Turn-on startup time	From EN high to PGOOD high, V_{OUT} = 0.75V		800		µs
V_{OUT}^+ pin input current	V_{OUT} = 0.75V, T_A = 25°C			±100	nA
V_{OUT}^- pin input current	V_{OUT}^- = 0V, T_A = 25°C	–300	–150		µA
Feedback Voltage Programmability					
Feedback voltage digital-to-analog (DAC) resolution	T_A = 25°C		8		bits
LSB step size	T_A = 25°C		4		mV
Default startup feedback voltage	OPT_VOUT = 0x4b, T_A = 25°C, I_{OUT} = 0A		300		mV
Feedback voltage programmability range	T_A = 25°C	300		1000	mV
Output programmability differential nonlinearity	Monotonicity guaranteed	–0.2		0.2	LSB

(V_{IN} = 5V and –40°C ≤ T_J ≤ 105°C unless otherwise noted. [1,2])

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input supply voltage rejection	V_{IN} = 2.9V to 5.5V, V_{OUT} = 0.75V, I_{OUT} = 0A	–4		4	mV
Oscillator					
Default clock frequency		4.5	5	5.5	MHz
Minimum synchronization frequency	Through the SYNC pin		4.5		MHz
Maximum synchronization frequency	Through the SYNC pin		5.5		MHz
SYNC input level (main device only)	V_{SYNC} high	1.5			V
	V_{SYNC} low			0.6	V
Minimum SYNC input pulse width	T_A = 25°C	20			ns
SYNC input leakage current to GND	V_{SYNC} = 6V, T_A = 25°C			±1	µA
CLK out rise/fall time (main device only)	C_{CLK} = 50pF, rising: 10% to 90%, falling: 90% to 10%, T_A = 25°C			16	ns
CLK low output voltage (main device only)	I_{CLK} = 1mA, T_A = 25°C			0.2	V
CLK high output voltage (main device only)	I_{CLK} = –1mA, T_A = 25°C	V_{IN} – 0.2			V
CLK out duty cycle (main device only)	T_A = 25°C		50		%
CLK input level (subordinate device only)	V_{CLK} high	1.5			V
	V_{CLK} low			0.6	V
Minimum CLK input pulse width (subordinate device only)	T_A = 25°C	20			ns
CLK input leakage current to GND	V_{CLK} = 6V ,T_A = 25°C			±1	µA
Main/Subordinate Device Communication Pins: ITH					
ITH pull-up current (main device only)	V_{OUT} at –10% out of regulation, V_{ITH} = 1.2V, T_A = 25°C		–10		mA
ITH pull-down current (main device only)	V_{OUT} at +10% out of regulation, V_{ITH} = 1.2V, T_A = 25°C		10		mA
ITH input leakage current (subordinate device only)	V_{ITH} = 2.0V, T_A = 25°C			±100	nA

(V_{IN} = 5V and –40°C ≤ T_J ≤ 105°C unless otherwise noted. [1,2])

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current Monitor					
IMON voltage at 33A	R_{IMON} = 10kΩ, V_{OUT} = 0.75V, T_A = 25°C	0.91	0.96	1.01	V
IMON voltage at no load	R_{IMON} = 10kΩ, V_{OUT} = 0.75V, T_A = 25°C		0		V
IMON gain	I_{IMON}/I_{OUT}, V_{IMON} = 0.96V, T_A = 25°C		2.91		µA/A
Output current error	V_{IMON} = 0V to 0.96V, R_{IMON} = 10kΩ, T_A = 25°C			±5	µA
IMON Over Current Alert Through $\overline{IRQ}$					
IMON rising threshold overvoltage	OPT_IMON_TH bits 00 to 103% (I_{OUT} = 34A)	0.96	0.99	1.02	V
	OPT_IMON_TH bits 01 to 93% (I_{OUT} = 30.6A)	0.86	0.89	0.92	V
IMON rising threshold overvoltage	OPT_IMON_TH bits 10 to 82% (I_{OUT} = 27.1A)	0.76	0.79	0.82	V
	OPT_IMON_TH bits 11 to 72% (I_{OUT} = 23.7A)	0.66	0.69	0.72	V
Hysteresis		40	50	60	mV
IMON overvoltage to $\overline{IRQ}$ delay	V_{IMON} rising edge = 0.90V to 1.04V, OPT_IMON_TH = 00, 2kΩ to V_{IN} and 10pF on $\overline{IRQ}$ pin, T_A = 25°C		1	2	µs
REF Pin					
REF voltage (main device only)	I_{OUT} = 0A		300		mV
REF input leakage current (subordinate device only)	T_A = 25°C			±100	nA
PGOOD (Main Device Only), $\overline{IRQ}$ Pins, and Soft Start					
PGOOD UV (undervoltage) rising threshold		–30	–18.75	–7.5	mV
Hysteresis		1.88	3.75	5.63	mV
PGOOD OV (overvoltage) rising threshold		7.5	18.75	30	mV
Hysteresis		1.88	3.75	5.63	mV
PGOOD delay/deglitch time	V_{OUT}: 110% to 100% or 90% to 100% to PGOOD rising edge, 2kΩ pull-up to V_{IN}, T_A = 25°C		20		µs

(V_{IN} = 5V and –40°C ≤ T_J ≤ 105°C unless otherwise noted. [1,2])

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD, $\overline{IRQ}$ leakage current	V_{PIN} = 5V, T_A = 25°C			±1	µA
PGOOD, $\overline{IRQ}$ pull-down current	V_{PIN} = 0.4V, T_A = 25°C	5	15		mA
Soft start slew rate	T_A = 25°C		2		mV/µs
M/$\overline{S}$, I²C, PH[3:0] (Digital/Programming Pins)					
Input level for pins M/$\overline{S}$ SDA, SCL (main device only) PH[3:0] (subordinate device only)	V_{PIN} high	1.4			V
	V_{PIN} low			0.6	V
Input leakage current to GND	For pins M/$\overline{S}$, SDA, SCL, PH[3:0], V_{PIN} = 5V, T_A = 25°C			±1	µA
SDA pull-down current	V_{PIN} = 0.4V, T_A = 25°C	5	20		mA
I²C Timing Characteristics					
I²C address			7'b1101001		
SCL clock frequency	f_{SCL}			400	kHz
SCL pulse width low		1.3			µs
SCL pulse width high		0.6			µs
Bus free time start to stop	t_{BUF}	1.3			µs
Hold time after repeated start	$t_{HD(STA)}$	0.6			µs
Setup time after repeated start	$t_{SU(STA)}$	0.6			µs
Stop the setup time	$t_{SU(STO)}$	0.6			µs
Data hold time	$t_{HD(DAT)}$	0		900	ns
Data setup time	$t_{SU(DAT)}$	100			ns
Input spike suppression pulse width	t_{SP}			50	ns
IMON-Average Current Readback Through I²C					
Output current resolution	T_A = 25°C		8		bits
LSB	I_{MON} to LSB, T_A = 25°C		4.7		mV
Analog-to-digital converter (ADC) full-scale input voltage	T_A = 25°C		1.2		V
Full-scale I_{MON} output code	I_{MON} voltage = 1V, T_A = 25°C		0xd5		
Total unadjusted readback error[3]	I_{MON} voltage = 1V, output valid 25°C ≤ T_J ≤ 105°C	–1		1	%
Conversion time	T_A = 25°C		3.3		ms

(V_{IN} = 5V and –40°C ≤ T_J ≤ 105°C unless otherwise noted. [1,2])

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Monitor Readback[4]					
Temperature least-significant bit (LSB)	T_A = 25°C		2.6		°C
Monitor code (room temperature)	T_A = 25°C	–3	01010101	3	LSB
Total unadjusted readback error[3]	T_A = 25°C	–7.8		7.8	°C
Conversion time	T_A = 25°C		3.3		ms
Input Voltage Monitor Readback[4]					
LSB	T_A = 25°C		23		mV
V_{IN} output code	V_{IN} = 3.3V, T_A = 25°C		10001101		
Total unadjusted readback error[3]	Output valid 25°C ≤ T_J ≤ 105°C	–5		5	%
Differential Feedback Voltage Monitor Readback[4]					
LSB	T_A = 25°C		4.7		mV
V_{OUT}^+ output code	T_A = 25°C, V_{OUT}^+ = 0.3V		01001011		
V_{OUT}^- output code	T_A = 25°C, V_{OUT}^- = 0V		00000000		
Total unadjusted $V_{OUT}^{\pm}$ readback error[3]	Output valid 25°C ≤ T_J ≤ 105°C	–2		2	LSB

1 The LTM3360B is tested under conditions such that $T_J \approx T_A$. The LTM3360B is guaranteed to meet specifications from –40°C to 105°C junction temperature. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the following formula: $T_J = T_A + (P_D \times \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

2 All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

3 Total unadjusted error includes gain, integral nonlinearity (INL), differential nonlinearity (DNL), as well as offset.

4 The ADC output is valid for 25°C ≤ T_J ≤ 105°C and is ADC tested with pulse-width modulation (PWM) disabled. Comparable capability demonstrated by the in-circuit evaluations.

5 This module includes overtemperature protection that is intended to protect the switching device during momentary overload conditions. Junction temperature exceeds 105°C when overtemperature protection is active. Continuous operation above the specified maximum junction temperature may impair device reliability or permanently damage the device.

I²C Digital Interface

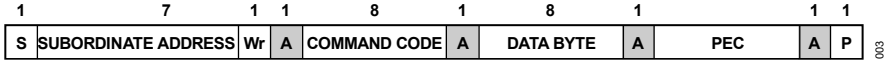


Figure 3. Write Byte Protocol

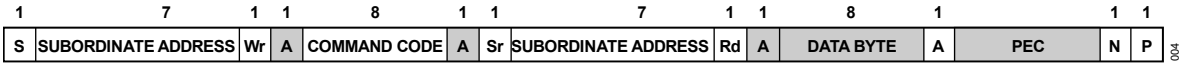


Figure 4. Read Byte Protocol

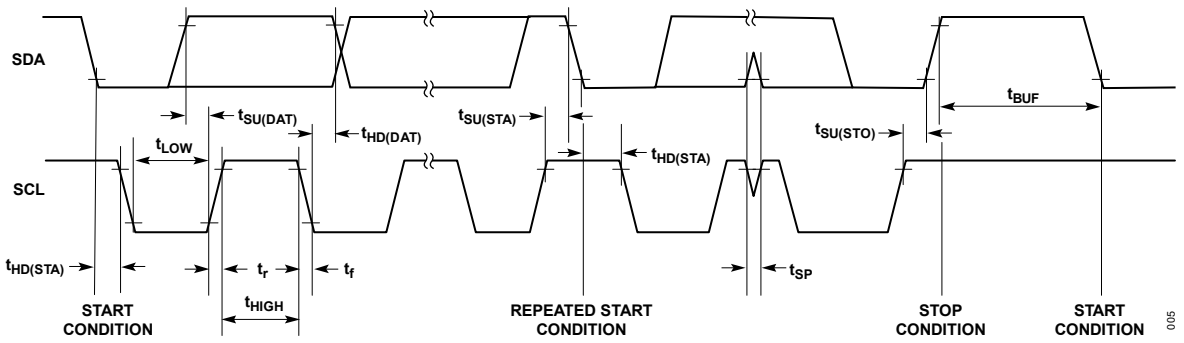


Figure 5. I²C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings [1]

PARAMETER	RATING
$V_{IN1,2}$ voltage	–0.3V to 6V
SDA, SCL, $\overline{IRQ}$ voltage	–0.3V to Min (V_{IN}, 6V)
EN, M/$\overline{S}$, SYNC, PGOOD voltage	–0.3V to Min (V_{IN}, 6V)
PH[3:0] voltage	–0.3V to Min (V_{IN}, 6V)
IMON, REF voltage	–0.3V to 1.5V
V_{OUT}^+, V_{OUT}^- voltage	–0.3V to 1.5V
Operating junction temperature range	–40°C to 105°C
Storage temperature range	–55°C to 125°C
Max reflow (package body) temperature	250°C

1 The LTM3360B is tested under conditions such that $T_J \approx T_A$. The LTM3360B is guaranteed to meet specifications from –40°C to 105°C junction temperature.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to the PCB thermal design is required. Using enhanced heat removal like the PCB, heat sink, and airflow techniques improve the thermal resistance values.

Thermal Coefficients Definition

1. θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.
2. θ_{JCtop} is the junction-to-case top thermal resistance.
3. $\theta_{JCbottom}$ is the junction-to-case bottom thermal resistance.

Table 3. Thermal Resistance for LTM3360B Evaluation Board in "Still Air"

θ_{JA}	θ_{JCtop}	$\theta_{JCbottom}$	UNIT
15.5	12.7	4.2	°C/W

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only. Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Field-induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002. International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2. Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings

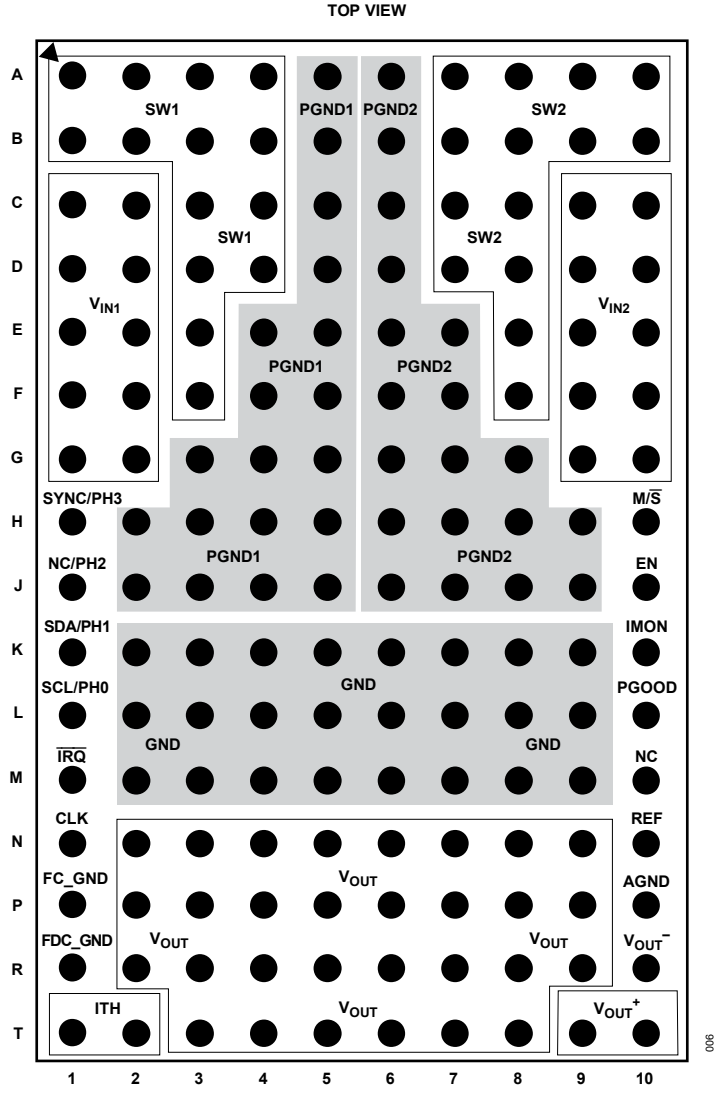
Table 4. LTM3360B ESD Ratings

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±4000	3A
CDM	±1250	C3

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



BGA PACKAGE
160-PIN (6.55mm × 5mm × 3.31mm)
T_{JMAX} = 105°C, θ_{JA} = 15.5°C/W, 0.4mm BALL PITCH
θ_{JCtop} = 12.7°C/W, $\theta_{JCbottom}$ = 4.2°C/W
WEIGHT = 0.31g

θ VALUES DETERMINED PER JESD5 112

Figure 6. Pin Configuration

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Pin Descriptions

Table 5. Pin Descriptions

PIN	NAME	DESCRIPTION
A1-B1, A2-B2, A3-F3, A4-D4; A7-D7, A8-F8, A9-B9, A10-B10	SW1, SW2	Switch Pins. These pins are the switching outputs of the internal power switches connected to the internal power inductors. High dV/dt waveforms are present in these pins. Leave these pins open to minimize electromagnetic interference (EMI).
A5-J5, E4-J4, G3-J3, H2-J2	PGND1	Power Ground 1. PGND1 pins are the return path of the internal bottom-side power switch 1 (SW1). Connect the negative terminal of any additional input capacitors as close to the PGND1 pins as possible (half between V_{IN1} and PGND1, and the other half between V_{IN2} and PGND2). The PGND1 node is one of the primary thermal highways at the bottom of the package and should be connected to a large PCB ground plane with several thermal vias.
A6-J6, E7-J7, G8-J8, H9-J9	PGND2	Power Ground 2. PGND2 pins are the return path of the internal bottom-side power switch 2 (SW2). Connect the negative terminal of any additional input capacitors as close to the PGND2 pins as possible (half between V_{IN1} and PGND1, and the other half between V_{IN2} and PGND2). The PGND2 node is one of the primary thermal highways at the bottom of the package and should be connected to a large PCB ground plane with several thermal vias.
C1-G1, C2-G2; C9-G9, C10-G10	V_{IN1}, V_{IN2}	Input Voltage Supply. The V_{IN1} and V_{IN2} pins supply current to the internal circuitry and top-side power switches. The V_{IN1} and V_{IN2} pins must be connected to the same power source potential. Internally connected to bypass capacitors to GND.
H1[2]	SYNC	Synchronization Input Pin. The SYNC pin allows the power switches to synchronize to an external clock between 4.5MHz and 5.5MHz.
H1, J1, K1, L1[3]	PH3, PH2, PH1, PH0	Phase Setting Pins. For each subordinate device, one of 16-phase delays (in degrees) is selectable, allowing for the implementation of an evenly spaced 1-, 2-, 3-, 4-, 6-, 8-, or 12-phase system. For the main device, the phase is set to 0°. On the main device, these pins' functions are replaced by SYNC, NC, SDA, and SCL pins, respectively. See the *Applications Information* section for more details.
H10	M/$\overline{S}$	Main/Subordinate Select Input Pin. Connect this pin to V_{IN} to set the LTM3360B to the main mode. Similarly, connect this pin to GND to set the LTM3360B to the subordinate mode.
J1[2]	NC	No Connect Pin. Leave the NC pin open in the main configuration.
J10	EN	Enable Input Pin. Pull the EN pin above its rising threshold to enable the switching converter. If this pin is not used, directly connect the pin to V_{IN} to automatically enable the switching converter as V_{IN} rises. Connecting this pin to GND ensures that the switching converter remains disabled with no power

PIN	NAME	DESCRIPTION
		delivered to V_{OUT} as V_{IN} rises. When connected in the main configuration, use the I^2C ports to overwrite this pin, allowing the enable/disable of the switching converter independent of the state of this pin. When connected as a subordinate, connect the EN pin to the main EN pin. See the *Applications Information* section for details on subordinate operation in a multiphase system when the main is disabled through I^2C.
K1[2, 5]	SDA	I^2C Data Pin. When writing data to the LTM3360B, the SDA pin is a high impedance input pin. When reading data from the LTM3360B, the SDA pin is an open-drain, active-low pin. Connect a 2kΩ pull-up resistor to the I^2C supply or V_{IN}. See the *I2C Communication* section for more details.
K2-K9, L2-L9, M2-M9	GND	Power Ground. The GND pins are the return path of the internal output bulk capacitors. Connect the negative terminal of any additional output capacitors between V_{OUT} and GND. The GND node is one of the primary thermal highways at the bottom of the package and should be connected to a large PCB ground plane with several thermal vias.
K10	IMON	Current Monitor Pin. The IMON pin outputs a current proportional to the output current. Connect an appropriate resistor to ground to convert IMON current to an equivalent voltage. At 34A load current at V_{OUT} , the IMON pin outputs 100µA (typical) of current.
L1[2, 5]	SCL	I^2C Clock Input Pin. The SCL pin is a high impedance input pin. See the *I2C Communication* section for more details.
L10 [2]	PGOOD	Power Good Output. Open-drain active low output. This pin is driven low when the regulated output voltage falls below its PGOOD threshold or rises above its overvoltage threshold. Connect a 2kΩ pull-up resistor to V_{IN} in a typical application.
M1	$\overline{IRQ}$	Interrupt Request Output. Open-drain active low output. This pin pulls low when there is an overcurrent event (IMON pin goes above the overcurrent alert threshold) or an overtemperature event.
M10	NC	Do Not Connect Pin. Leave this pin open.
N1[4]	CLK	Clock Pin. In the main, this is the clock reference output for the multiphase operation. On a subordinate, it is an input. Connect the main and subordinate CLK pins in a multiphase operation. When connected as a subordinate, the converter is disabled when there is no edge on the CLK pin.
N2-N9, P2-P9, R2-R9, T3-T8	V_{OUT}	Output Voltage Pins. Connect the appropriate feedback resistor divider to V_{OUT}^+ and V_{OUT}^- to set the desired output voltage. The V_{OUT} pins deliver the inductor output current up to a maximum of 33A in steady state. Ensure that short, wide traces or several thermal vias (in a vertical construction) with sufficient current density ratings connect these pins to the point-of-load. Internally connected to bypass capacitors to GND.
N10 [4]	REF	Reference Pin. The REF pin from the main drives all the subordinate REF pins to ensure a common reference voltage for proper operation. The buffer driving the main REF pin has a 100Ω (typical) output impedance. Ensure that only the

PIN	NAME	DESCRIPTION
		subordinate REF pins are connected to the main REF pin. Do not connect this pin to other circuits that source or sink current, or near any noise source.
P1	FC_GND	Test purpose only. Suggested to be connected to ground.
P10	AGND	Analog Ground. The AGND pin is the return path for all the internal sensitive analog circuits. Connect the AGND pin directly to any of the GND pins (K2-K9, L2-L9, M2-M9) for a kelvin connection to the negative terminal of the internal bypass V_{OUT} capacitors.
R1	FDC_GND	Test purpose only. Suggested to be connected to ground.
R10, T9-T10[2]	V_{OUT}^+, V_{OUT}^-	Output Voltage Differential Remote Sense Pins. Voltage across these pins is regulated to 0.3V by default. Connect an appropriate feedback resistor divider from V_{OUT} to V_{OUT}^+ and from V_{OUT}^+ to V_{OUT}^- to set the desired output voltage at V_{OUT}. See the *Applications Information* section for details on selecting the feedback network.
T1-T2[4]	ITH	Current Threshold Control Pin. On the main, this is an output. On a subordinate, it is an input. Connect the main and subordinate ITH pins in a multiphase operation. When connected in the main, the ITH pin is driven to 0V when the device is disabled (through the EN pin or I^2C).

1 See *Figure 38* in the *Applications Information* section for the main and the subordinate devices' pin configurations.

2 Main device only.

3 Subordinate devices only.

4 Output for main device, input for subordinate devices.

5 The LTM3360B's method of implementing ESD protection on these pins is I^2C-compliant but not SMBus-compliant. The V_{IN} power should not be removed from the device when the I^2C bus is active to avoid loading the I^2C bus lines through the internal ESD protection diodes.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

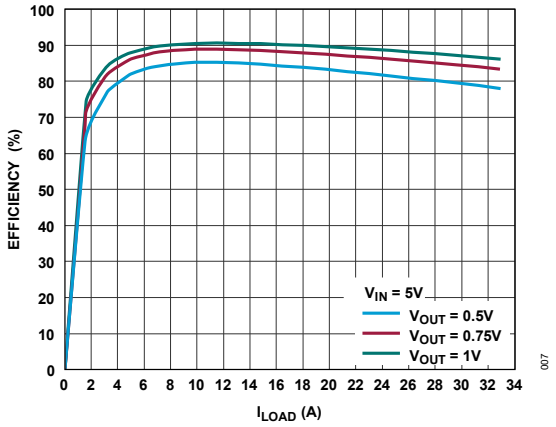


Figure 7. Efficiency vs. I_{LOAD} at Different V_{OUT}

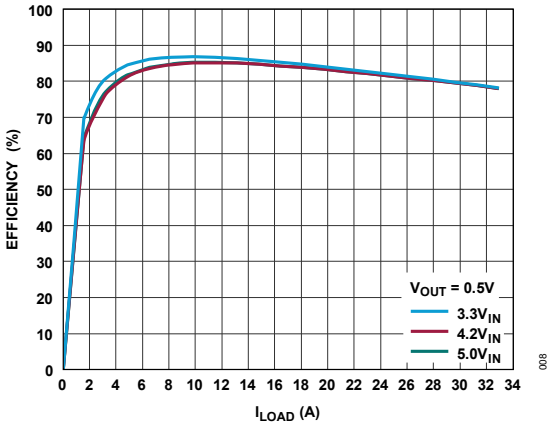


Figure 8. Efficiency vs. I_{LOAD} at Different V_{IN}

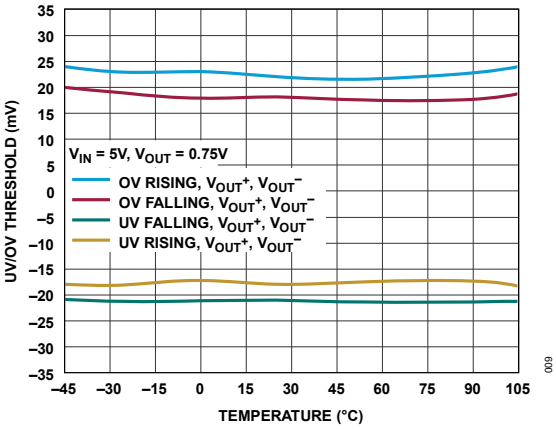


Figure 9. PGOOD UV/OV Rise and Fall

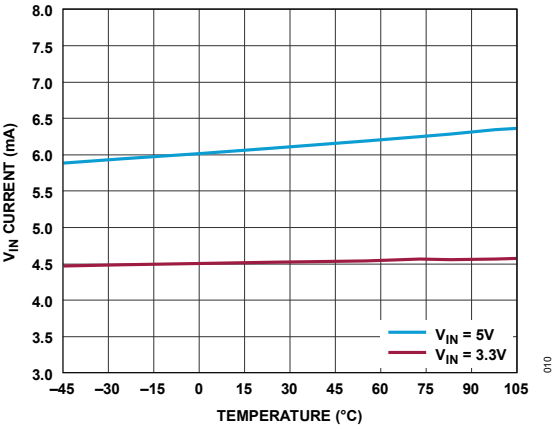


Figure 10. V_{IN} Shutdown Current vs. Temperature

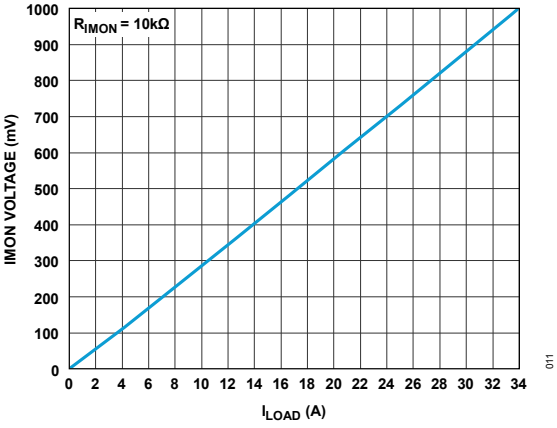


Figure 11. IMON Voltage vs. I_{LOAD}

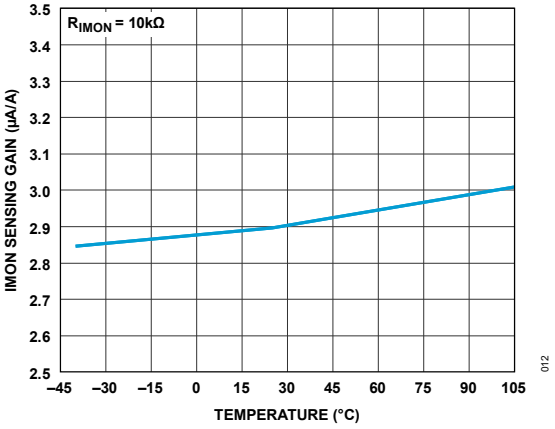


Figure 12. IMON Sensing Gain vs. Temperature

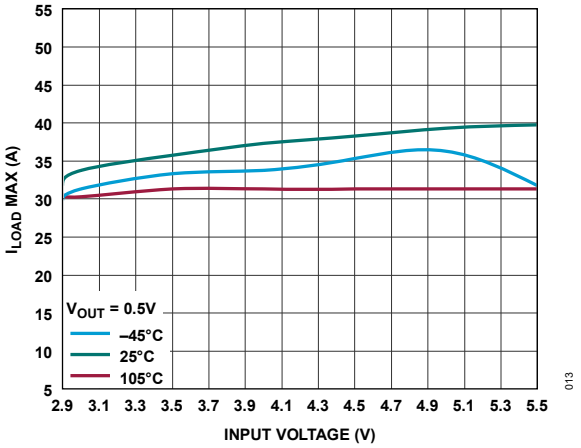


Figure 13. Maximum I_{LOAD} vs. V_{IN}

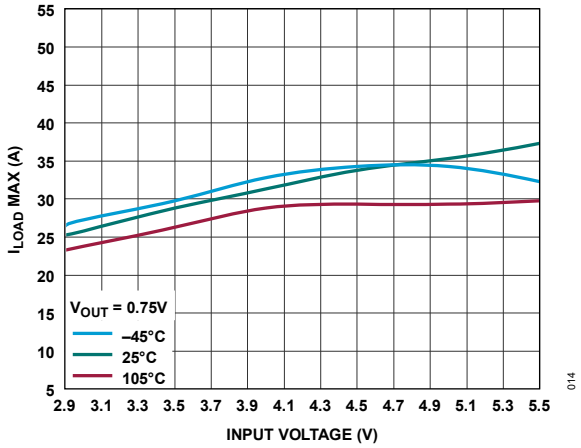


Figure 14. Maximum I_{LOAD} vs. V_{IN}

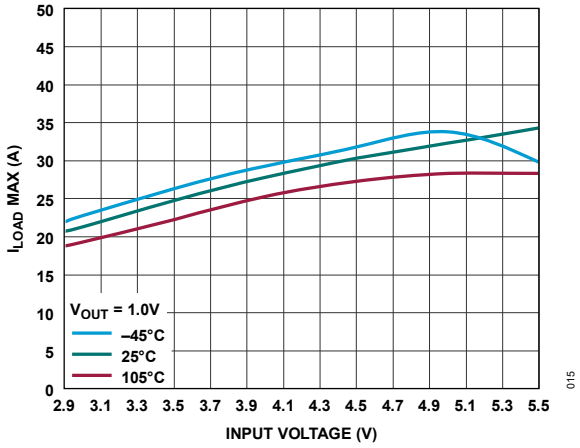


Figure 15. Maximum I_{LOAD} vs. V_{IN}

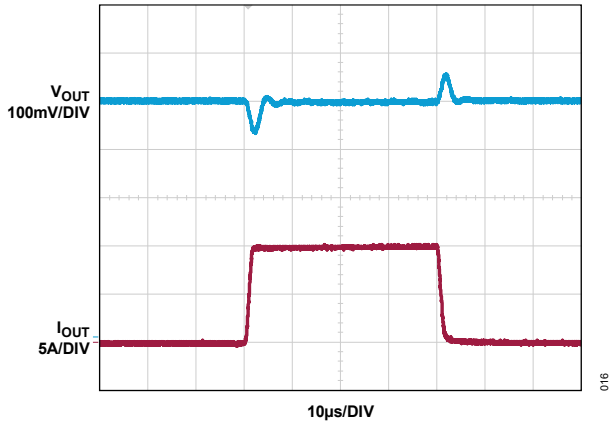


Figure 16. Load Step Up/Down Waveforms

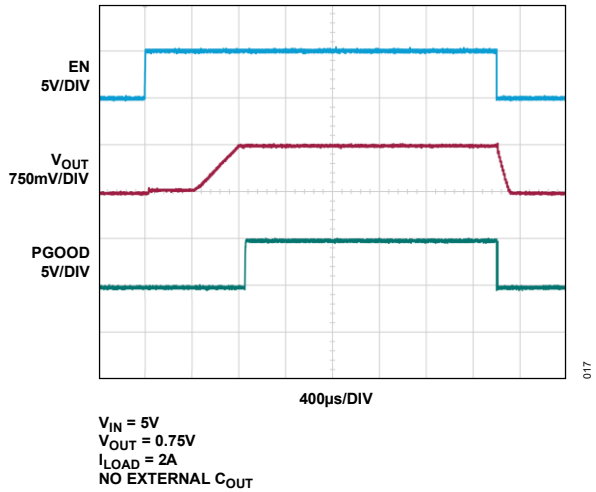


Figure 17. Startup and Shutdown Waveforms

I²C COMMUNICATION

Overview

When connected as the main device, the LTM3360B's I²C port allows communication with the LTM3360B for configuration and readback telemetry data. The communication protocol is compatible with the SMBus read-byte and write-byte protocols. The input thresholds for the ports are fixed at 1.1V (typical).

The registers, accessible through this port, are organized on an 8-bit address bus, and each register is 8 bits wide. The "command code" (or subordinate address) of the SMBus read/write word formats is the 8-bit address of each of these registers. The address of the LTM3360B is 7'b1101001(Wr), where Wr is 1 for write and 0 for read.

See the *Register Summary: LTM3360B Register Map* section for more details on the registers accessible through this interface. For the I²C main devices unable to create the repeated start needed for the read and write word protocols, a stop followed by a start may be substituted.

The serial clock line (SCL) has no output driver and does not stretch clock cycles.

The I²C port is disabled in subordinate mode.

Register Summary: LTM3360B Register Map

Table 6. LTM3360B Register Summary

ADDRESS	NAME	DESCRIPTION	RESET	ACCESS
0x1	EN_IMON_CTRL	Enable and IMON control	0x00	R/W
0x3	VOUT+_SETTING	Feedback voltage setting	0x4b	R/W
0x4	ADC_SELECT	ADC input selection	0x00	R/W
0x5	ADC_CTRL	ADC setup	0x00	R/W
0x6	ADC_OUTPUT	ADC output	0x00	R

Enable and IMON Control Register

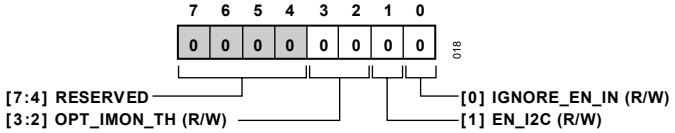


Figure 18. Address: 0x1, Reset: 0x00, Name: EN_IMON_CTRL

Table 7. Bit Descriptions for EN_IMON_CTRL

BITS	BIT NAME	DESCRIPTION	RESET	ACCESS
[7:4]	RESERVED	Reserved	0x0	R
[3:2]	OPT_IMON_TH	IMON threshold setting: 00 to 99% 01 to 89% 10 to 79% 11 to 69%	0x0	R/W
1	EN_I2C	Writing this bit high enables the device regardless of the state of the enable pin.	0x0	R/W
0	IGNORE_EN_IN	Writing this bit high ignores the enable pin.	0x0	R/W

V_{OUT}+ Setting Register

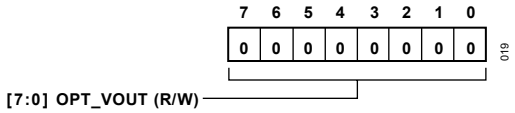


Figure 19. Address: 0x3, Reset: 0x4b, Name: VOUT+_SETTING

Table 8. Bit Descriptions for VOUT_SETTING

BITS	BIT NAME	DESCRIPTION	RESET	ACCESS
[7:0]	OPT_VOUT	Feedback Voltage setting – range 300mV to 1000mV, LSB ~ 4mV: 11111111 (0xff – 255): 1000mV 10111011 (0x4b – 75): 300mV (factory program default at power-up) 01000111 (0x4a – 74): 297mV (minimum allowable programmed code)	0x4b	R/W

ADC Input Selection Register

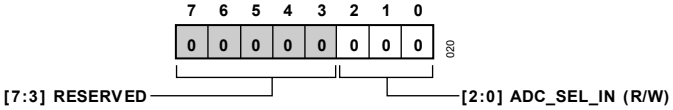


Figure 20. Address: 0x4, Reset: 0x00, Name: ADC_SELECT

Table 9. Bit Descriptions for ADC_SELECT

BITS	BIT NAME	DESCRIPTION	RESET	ACCESS
[7:3]	RESERVED	Reserved	0x0	R
[2:0]	ADC_SEL_IN	3-bit input select for ADC. Write to this register to initiate a new conversion cycle. 000: IMON 001: Temperature monitor 010: V_{OUTP} monitor 011: V_{OUTN} monitor 100: V_{IN} monitor 101 to 111: IMON (redundant)	0x0	R/W

ADC Setup Register

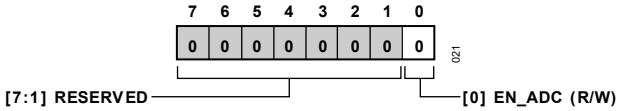


Figure 21. Address: 0x5, Reset: 0x00, Name: ADC_CTRL

Table 10.Bit Descriptions for ADC_CTRL

BITS	BIT NAME	DESCRIPTION	RESET	ACCESS
[7:1]	RESERVED	Reserved	0x0	R
0	EN_ADC	Writing this bit high enables the ADC.	0x0	R/W

ADC Output Register

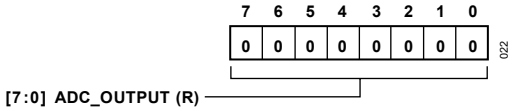


Figure 22. Address: 0x6, Reset: 0x00, Name: ADC_OUTPUT

Table 11. Bit Descriptions for ADC_OUTPUT

BITS	BIT NAME	DESCRIPTION	RESET	ACCESS
[7:0]	ADC_OUTPUT	ADC output.	0x0	R

THEORY OF OPERATION

LTM3360B Overview

The LTM3360B is a power µModule DC-to-DC regulator with high-current, high-density, constant-frequency, and current-mode architecture, which is capable of efficiently delivering 33A at output voltages as low as 300mV. The I^2C interface allows for programmability of various features as well as readback of output current. The high-fixed switching frequency of 5MHz permits the integration of not only the input and the output capacitors, but also the integration of the power inductor, resulting in the highest density of output current to total board footprint achievable in the industry, with minimal external components required. The high-density and small footprint, with the ability to synchronize the switching frequency to an external clock, enable systems using the LTM3360B to easily mantain a low-noise/EMI profile. Some of the features of the LTM3360B include internal compensation to optimize transient response, soft start to manage inrush current, an output power good function to report when V_{OUT} is within regulation, and an $\overline{IRQ}$ pin to signal status change. For higher current applications, multiple LTM3360Bs are easily paralleled with the clock (CLK) and current threshold control (ITH) pins, along with the REF pins. In multi-device applications, one device acts as the main controller, and the other devices operate as subordinate devices. The devices are subordinate if the M/$\overline{S}$ pin is connected to GND.

Simplified Block Diagram

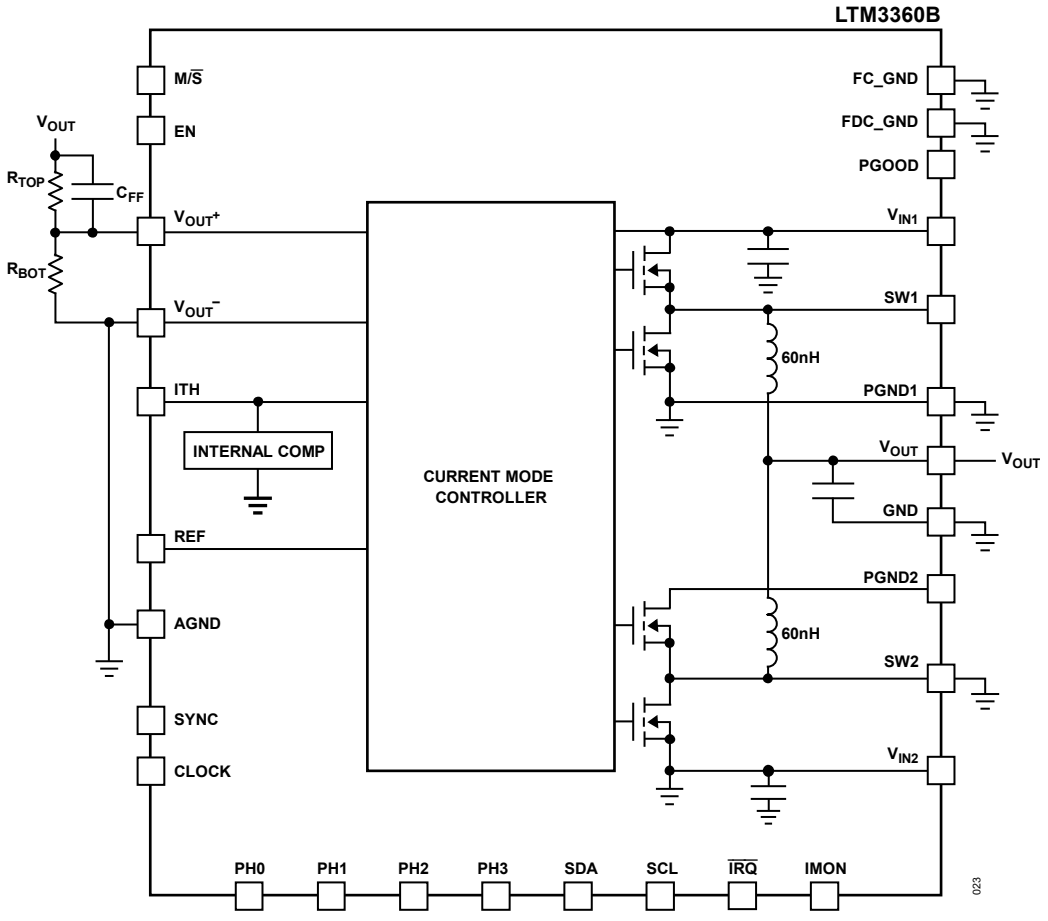


Figure 23. LTM3360B Simplified Block Diagram

Power-On

The LTM3360B uses the EN pin and the EN_I2C bit in the EN_IMON_CTRL register to enable and disable the device. The device can only be enabled if the input supply at V_{INn} is above the UVLO rising threshold.

Setting the EN_I2C bit high enables the device regardless of the state of the EN pin. And if the IGNORE_EN_IN bit in the same EN_IMON_CTRL register is low, once the EN pin exceeds the input threshold, the device is enabled.

To disable the device, both the EN_I2C bit and the EN pin must be low if the IGNORE_EN_IN bit is low. However, if the IGNORE_EN_IN bit is high, setting the EN_I2C bit disables the device regardless of the state of the EN pin.

The LOGIC Equation *1* determines the state of the internal enable signal (INT_EN).

$$INT_{EN} = [\overline{IGNORE\_EN\_IN} \times EN\_PIN] + ENI^2C \quad (1)$$

When the internal enable signal is high, the device is enabled and starts switching after 100µs (typical). On the other hand, when the internal enable signal is low, the device powers down, and all the internal logic states are reset to their default values.

Voltage Regulation

The internal bottom power switch is turned on at the beginning of each clock cycle. Current in the inductor then decreases until the inductor current comparator trips and turns off the bottom power switch. The valley inductor current at which the bottom switch turns off is controlled by the voltage on the internal ITH node. The error amplifier servos this ITH node by comparing the differential voltage on the V_{OUT} sense pins (V_{OUT}^+, V_{OUT}^-) with a factory-programmed reference of 0.3V.

When the load current increases, it causes a reduction in the V_{OUT} sense pins voltage relative to the reference voltage, leading the error amplifier to raise the ITH voltage until the average inductor current matches the new load current. When the bottom power switch turns off, the synchronous top power switch turns on until the next clock cycle begins or inductor current rises to the top switch current limit.

If overload conditions result in excessive current flowing through the bottom switch, the next clock cycle is delayed (pulse-skipped) until the switch current returns to a safe level.

Forced Continuous Mode Operation

The LTM3360B operates in forced continuous mode (FCM). In FCM, the oscillator operates continuously. The bottom switch turns on every cycle, and regulation is maintained by allowing the inductor current to reverse at light load. This mode allows the buck regulator to run at a fixed frequency with minimal output ripple. With this FCM of operation, if the inductor current reaches the negative current limit (into the SW pin), the bottom switch turns off for the remainder of the cycle to limit the reverse current.

Soft Start and Output Power Good

Soft-starting the output during startup prevents a current surge on the input supply and/or output voltage overshoot. During the soft start, the output voltage proportionally tracks the internal reference voltage ramp. The soft start rate is set to a default (typ 2mV/µs) on feedback in the internal one-time programmable (OTP) memory and cannot be changed through I^2C. Consult with the factory for startup rates other than the programmed default.

In the case of a fault condition, the soft start voltage is reset to 0V. The ramp restarts when the fault is cleared, and the output returns to its default value. Fault conditions that initiate the soft start ramp include disabling the device, V_{INn} is undervoltage, or thermal shutdown.

When operating as a main device, the power good status is indicated on the PGOOD pin. If the output voltage is within the specified power good voltage window, the output is considered good, and the open-drain PGOOD pin becomes high impedance. The PGOOD output is typically pulled high with an external resistor (2kΩ recommended).

If the output voltage is outside the specified power good voltage window, the output is considered NOT good, and the internal pull-down device pulls the PGOOD pin low. The PGOOD pin is also pulled low under the following conditions: the device is disabled, V_{INn} is undervoltage, or thermal shutdown is active. To filter noise and short-duration output voltage transients, the threshold has built-in hysteresis and a 20µs time delay to report PGOOD. *Figure 24* shows the timing relationship between EN, V_{OUT}, and PGOOD. If a device is acting as a subordinate (M/$\overline{S}$ = 0V), the PGOOD function is disabled since only the main device power good comparators are enabled to detect if regulation is within the power good window.

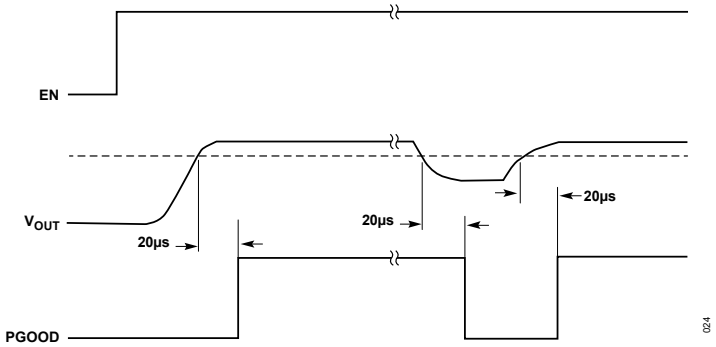


Figure 24. Output Power Good (PGOOD) Timing

Output Dynamic Voltage Scaling (DVS) Rate

When the output voltage regulation target is changed through the OPT_VOUT bits in the VOUT_SETTING register, the dynamic voltage scaling (DVS) rate is similarly set to a default (typical 2mV/µs) in the internal OTP memory and cannot be changed through I²C. Consult with the factory for DVS rates other than the programmed default. The PGOOD pin is driven LOW before the DVS starts and then released HIGH after the DVS process completes. *Figure 25* shows the timing relationship between V_{OUT} and PGOOD. The PGOOD DVS function can be disabled by I²C communication by setting the register at address 0x7 from x0 to x1.

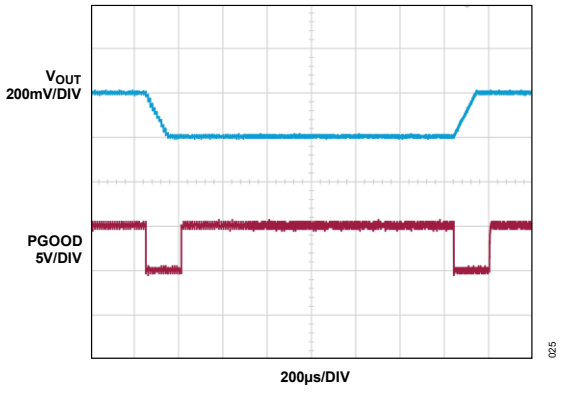


Figure 25. Output Dynamic Voltage Scaling (DVS)

Power-Down

When the device is disabled (INT_EN = 0), the inductor current returns to zero, and the output discharge resistor (typical 1kΩ) is turned on. Much of the internal circuitry is disabled when the internal enable signal (INT_EN) is set

low to reduce shutdown current. Disabling the internal circuitry also results in all the registers being reset to their default programmed values in preparation for the next restart.

Overtemperature Protection

To prevent thermal damage to the LTM3360B, the device incorporates an overtemperature (OT) function. When the die temperature reaches 150°C (typical, not tested), the switcher is shut down and remains in shutdown until the die temperature falls below 140°C (typical, not tested).

When an OT event occurs, the $\overline{IRQ}$ pin pulls low to indicate an overtemperature fault condition. Note that multiple devices can assert the $\overline{IRQ}$ pin.

For systems with subordinate devices, if the $\overline{IRQ}$ pins of the subordinate devices are connected to the main device $\overline{IRQ}$ pin, then all the $\overline{IRQ}$ pins are low anytime one or more of the devices are above the over temperature threshold (typical 160°C, not tested).

Overcurrent Warning

The average current of the inductor is represented as a pull-up current at the IMON pin. The average inductor current to the IMON output current gain is set to typically 1/340,000, with 100µA IMON output current representing 34A average inductor current. When a resistor is connected to this IMON pin, the average inductor current is then translated to a voltage.

The voltage on the IMON pin is monitored by an overcurrent warning comparator. By default (at power-up), this comparator threshold is set to 0.99V. However, this threshold is adjustable through I^2C from 0.69V to 0.99V in 0.1V increments.

When the IMON voltage exceeds this overcurrent warning threshold, the $\overline{IRQ}$ pin pulls low.

For systems with subordinate devices, typically, the IMON pins of the subordinate devices are connected to the main device IMON pin. Then all the pull-up currents of the devices are summed together. Each of the device IMON output current gain to its own output current is typically 1/340,000. Therefore, by scaling the resistor value connected to this common IMON node, the real-time total average inductor current of all the LTM3360B (main and subordinates included) is translated to a single voltage on this common IMON node.

If the $\overline{IRQ}$ pins of the subordinate devices are also connected to the main device $\overline{IRQ}$ pin, then all the $\overline{IRQ}$ pins are low any time the total system current exceeds the overcurrent warning threshold set in the main LTM3360B.

Output Short-Circuit Operation

As described in the *Voltage Regulation* subsection, the valley inductor current at which the bottom switch turns off (and therefore turning on the top switch) is controlled by the voltage on the internal ITH node.

If the output current increases, the error amplifier raises the ITH pin voltage (allowing the top switch to turn on earlier in the clock cycle and therefore for a longer period) until the average inductor current matches the load current. The LTM3360B clamps the maximum ITH pin voltage, thereby limiting the maximum valley inductor current. This clamp point is set to the bottom switch's maximum valley current limit.

To ensure safe operations of the top switch under all conditions, the current through the top switch is monitored whenever it is turned on. The maximum current through the top switch is set to the top switch's maximum peak current limit.

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle because the voltage across the inductor is low. If the inductor current measured through the bottom power switch

is greater than the bottom switch's max valley current limit, then the bottom switch is held on and the top power switch is held off. Subsequent switching cycles are skipped until the inductor current is reduced below the bottom switch’s max valley current limit.

Synchronization

When operating as the main, the LTM3360B internal oscillator is synchronized through an internal phase-locked loop (PLL) circuit to an external frequency by applying a square wave clock signal to the SYNC pin. When synchronized, the bottom power switch’s turn-on is locked to the rising edge of the external frequency source.

The slope compensation is automatically adapted to the external clock frequency. After detecting an external clock on the first rising edge of the SYNC pin, the internal PLL gradually adjusts its operating frequency to match the frequency and phase of the signal on the SYNC pin.

When the external clock is abruptly removed, the LTM3360B detects the absence of the external clock within approximately 10µs (typical). During this detection time, the PLL continues to provide clock cycles at a gradually decreasing frequency to a minimum of 4.5MHz (typical). Once the external clock removal has been detected, the oscillator gradually adjusts its operating frequency back to the default frequency of 5MHz (typical).

When operating as subordinates, the main LTM3360B provides a reference clock through its CLK pin. This is to ensure that any external synchronization source only needs to drive the main’s SYNC pin without worrying about the capacitive loading of multiple subordinates. To ensure correct phasing and synchronization of the subordinates, their CLK pins need to be connected to each other and to the main CLK pin.

Identical to the main synchronization of its internal clock to the SYNC pin, the subordinates’ internal PLL synchronizes its internal clock to the CLK pin.

APPLICATIONS INFORMATION

The LTM3360B is designed to be a highly integrated complete step-down DC-to-DC converter solution maximizing output current density per unit board surface area. See *Figure 23* (LTM3360B Simplified Block Diagram) as a reference for the following sections.

Output Voltage Programming/Sensing

The LTM3360B has an internal reference voltage of 0.3V. When operating as the main device, the internal error amplifier (EA) compares the output sense voltage (V_{OUT}^+ and V_{OUT}^-) to the internal reference voltage. A buffered version of this internal reference voltage is accessible on the REF pin.

The output voltage level of the LTM3360B can be changed by selecting the appropriate resistor dividers, R_{TOP} and R_{BOT}, between V_{OUT}, V_{OUT}^+, and V_{OUT}^- as shown in *Figure 26*. Use values of less than 2kΩ (0.1% tolerance) for R_{BOT}. Calculate R_{TOP} based on the desired output voltage using Equation *2*. See *Table 13* for the recommended values for R_{TOP} and R_{BOT}.

$$V_{OUT} = \left(1 + \frac{R_{TOP}}{R_{BOT}}\right) \times 300mV \qquad (2)$$

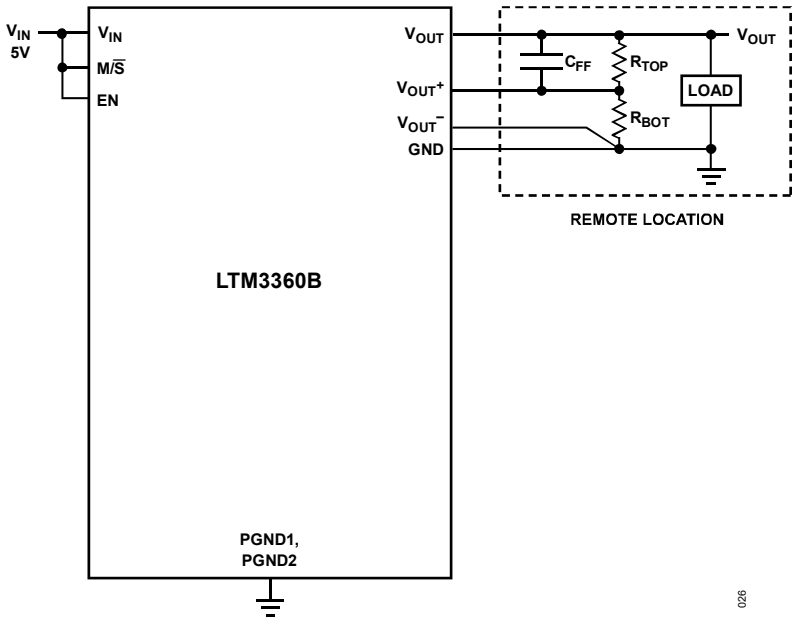


Figure 26. Resistor Divider for Setting the Output Voltage

Place the resistor dividers, R_{TOP} and R_{BOT}, as close to the load where the voltage needs to be sensed. The V_{OUT}^+ and V_{OUT}^- should always be connected directly across R_{BOT}, near the desired sense location. Minimize impedance between the V_{OUT} and GND pins of the device, and sense locations for maximum accuracy. Thought should be given to inaccuracies that occur due to large currents in the output ground (GND) plane when selecting the V_{OUT} location.

The LTM3360B AGND pin is the ground reference for the internal analog circuitry. For proper functioning of the device, connect the AGND pin to the GND pins as close to the device as possible. All the signal components, such as the IMON resistor, should be referenced to the AGND node. The AGND node carries very little current and can therefore be a minimal-size trace. See the *PC Board Layout Considerations* section for more information.

Setting the Output Overcurrent Warning Threshold

The IMON pin sources a current that is proportional to the average output current. At 34A of load current at V_{OUT}, the IMON pin outputs 100µA (typical) of current. By connecting a resistor on this pin, a voltage representing the average output current is obtained according to Equation *3*.

$$V_{IMON} = \frac{I_{OUT}(A) \times R_{IMON}}{340{,}000} \quad (3)$$

For example, with a 10kΩ resistor connected between IMON and GND, the IMON voltage gain to the output voltage is 29.1mV/A with a voltage of 0.99V for a 34A output current.

As discussed in the *Theory of Operation* section, the voltage on the IMON pin is monitored by an overcurrent warning comparator. The output overcurrent warning threshold has four different thresholds, whose default is programmed at the factory. Beyond the default value, this threshold can be programmed over through I²C. This threshold can be changed by setting the OPT_IMON_TH bit field, as shown in *Table 12*.

Table 12. OPT_IMON_TH Bit Field Settings

OPT_IMON_TH (BITS)	PERCENTAGE OVER 33A (%)	VOLTAGE (V)
00 (default)	103	0.99
01	93	0.89
10	82	0.79
11	72	0.69

By default (at power-up), this comparator threshold is set to 0.99V. However, this threshold is adjustable through I²C from 0.69V to 0.99V in 0.1V increments.

When the IMON pin voltage goes above the overcurrent alert threshold, the $\overline{IRQ}$ pin pulls low.

Reverse Output Current Limit

The LTM3360B operates in forced continuous mode, allowing the current in the inductor to go negative. To prevent damage to the device, the reverse inductor current is limited by internal circuitry. The limit is set to –7A (typical).

Output Pull-Down

When the LTM3360B is disabled, a resistive pull-down is connected between V_{OUT} and GND (typical 1kΩ).

Synchronization

The switching regulator clock source may be switched from the internal oscillator to a clock on the SYNC pin. The LTM3360B can sync to an externally applied clock in the range of 4.5MHz to 5.5MHz at the appropriate logic levels.

As discussed in the *Theory of Operation* section, when operating as the main, the LTM3360B has an edge detector on the SYNC pin. When detecting an external clock on the first rising edge of the SYNC pin, the internal PLL gradually adjusts its operating frequency to match the frequency and phase of the signal on the SYNC pin.

Identical to the main synchronization of its internal clock to the SYNC pin, the subordinates synchronize their internal clocks to the CLK pin. In *Typical Applications*, the CLK pin of the main is connected to a clock bus for all the subordinates to ensure an identical clock reference for accurate phase programming of each of the subordinates

with respect to the main. Furthermore, the CLK pin output buffer of the main has been sized to be able to drive multiple subordinates while maintaining the integrity of the clock signal edges.

Care must be taken in routing this clock signal. With the clock fast edges at frequencies in the range of 4.5MHz to 5.5MHz, this clock routing is a high-frequency noise source. This clock route should also be kept to a minimum to ensure the smallest parasitic capacitance and inductance.

Analog-to-Digital Converter (ADC)

The LTM3360B has an integrated 8-bit sigma-delta ADC. The ADC processes a single sample at a time and is reset before each new conversion cycle. Any ADC_SEL_IN I^2C write triggers a single conversion. Each conversion takes approximately 3.3ms. At the end of a conversion, the ADC result is stored in the ADC_OUTPUT register 0x6. To continuously monitor an ADC input, the user must continually write to the appropriate ADC_SEL_IN register address.

To readback the IMON pin voltage, first enable the ADC by writing 0x1 to the ADC_CTRL register 0x5 to enable the ADC, followed by writing 0x0 to the ADC_SELECT register 0x4. After a 3.3ms conversion time, the output of the ADC is written to the ADC_OUTPUT register 0x6. The pin voltage can then be calculated using Equation 4.

$$IMON\ Voltage = 4.7mV\ \times (ADC\_OUTPUT) \qquad (4)$$

For example, an ADC output of 10010101 is equal to 149 in base 10, which gives an IMON voltage = 700mV per Equation 4.

To read the die temperature, write 0x1 to the ADC_CTRL register 0x5 to enable the ADC, followed by writing 0x1 to the ADC_SELECT register 0x4. After completing the conversion, the output of the ADC is written to the ADC_OUTPUT register 0x6. The die temperature can then be calculated using Equation 5.

$$Die\ Temperature = 2.6°C\ \times (ADC\_OUTPUT - 75) \qquad (5)$$

For example, an ADC output of 01010101 is equal to 85 in base 10, which gives a die temperature of 26°C per Equation 5.

To read the input supply voltage (V_{IN}), write 0x1 to the ADC_CTRL register 0x5 to enable the ADC, followed by writing 0x4 to the ADC_SELECT register 0x4. After completing the conversion, the output of the ADC is written to the ADC_OUTPUT register 0x6. The input voltage can then be calculated using Equation 6.

$$Input\ Voltage = 23mV\ \times (ADC\_OUTPUT) \qquad (6)$$

For example, an ADC output of 10001101 is equal to 141 in base 10, which gives an input voltage of 3.3V per Equation 6.

To read the output voltage on the differential sense pins (V_{OUT}^+, V_{OUT}^-), first write 0x0 to the ADC_CTRL register 0x5 to enable the ADC, followed by writing 0x2 to the ADC_SELECT register 0x4. After completing the conversion, the output of the ADC is written to the ADC_OUTPUT register 0x6. Then write 0x3 to the ADC_SELECT register 0x4. After completing the conversion, the output of the ADC is written to the ADC_OUTPUT register 0x6. The V_{OUT}^+ and V_{OUT}^- voltages can then be calculated using Equation 7.

$$\begin{aligned} V_{OUT}{}^+ &= 4.7mV\ \times (ADC\_OUTPUT) \\ V_{OUT}{}^- &= 4.7mV\ \times (ADC\_OUTPUT) \end{aligned} \qquad (7)$$

For example, an ADC output of 10100000 for V_{OUT}^+ and 0000001 for V_{OUT}^- is equal to 160 and 1 in base 10, which gives (V_{OUT}^+, V_{OUT}^-) = 0.75V per Equation 7.

Transient Response and Loop Compensation

The LTM3360B has been designed to operate at a high bandwidth for fast transient response capability. Operating at a high loop bandwidth reduces the output capacitance required to meet transient response requirements.

Add a feedforward capacitor, C_{FF}, in parallel with the feedback resistor R_{TOP} (see *Figure 26*). Choose C_{FF} according to the Equation *8*, so that the resulting phase boost is maximum at crossover frequency f_{BW}, typically 200kHz to 300kHz for LTM3360B. See *Table 13* for the recommended values for C_{FF} at different output voltages.

$$C_{FF} = \frac{1}{2\pi f_{BW}} \sqrt{\frac{1}{R_{TOP}(R_{TOP}||R_{BOT})}} \quad (8)$$

Table 13. Typical Values for the Feedback Resistor Divider and the Feedforward Capacitor

V_{OUT} (V)	R_{TOP} (Ω)	R_{BOT} (kΩ)	C_{FF} (F)
0.5	667Ω	1	1n
0.6	1k	1	1n
0.75	3k	2	330p
0.8	1.69k	1.02	470p
1	2.7k	1.15	330p

Applying a load transient and monitoring the response of the system, or using a network analyzer to measure the actual loop response, are two ways of verifying the control loop frequency response and stability.

The LTM3360B also has special nonlinear transient response circuitry that helps to improve transient response time. During large load steps or load releases, this nonlinear transient response circuitry provides another assurance that the output voltage excursions are limited. Various peak and valley current limits are continuously observed even during nonlinear operations to ensure safe operations of the internal power switches. This function is disabled by default. Consult with the factory for enabling the nonlinear control.

V_{OUT} Overvoltage/Undervoltage Monitoring

When operating as the main device, the LTM3360B monitors the voltage difference between the V_{OUT}^+ and the V_{OUT}^- pins. This monitoring is done using the overvoltage (OV) and undervoltage (UV) comparators. The OV threshold is set at +18.75mV (rising typical) and the UV threshold is set at –18.75mV (falling typical) with respect to the target regulation point.

As discussed in the *Theory of Operation* section, if the output voltage is outside the specified power-good voltage window, the output is considered NOT good, and the internal pull-down device pulls the PGOOD pin low. The PGOOD pin is also pulled low under the following conditions: EN pin is low, V_{INn} is undervoltage, or thermal shutdown is active.

On the other hand, if the output voltage is within the specified power good voltage window, the output is considered good, and the open-drain PGOOD pin goes to high impedance. The PGOOD output is typically pulled high with an external resistor (2kΩ recommended). This output voltage monitoring is disabled when operating as a subordinate.

Additional Input Capacitors

In a typical buck DC-to-DC converter, the input power supply (V_{INn}) and the power ground pins (PGND(n)) have extremely high-frequency pulsatile current changes; whereas, the switching node current (SW(n)) does not contain much energy beyond the switching frequency and the first few harmonics. Therefore, the supply and power ground terminals require the utmost attention.

To combat supply noise, the LTM3360B package includes bulk and high-frequency input capacitors to filter the hot loop formed by the V_{INn} pins, PGND(n) pins, and the input capacitors. These input capacitors are sufficient for providing bulk charge as well as filtering high-frequency noise for most applications.

For the most sensitive input rail supply voltages (connected to V_{INn}), additional bulk capacitance in the form of 0603, or larger, ceramic capacitors, close to the supply pins on the package, can be added. See the *PC Board Layout Considerations* section for the required PCB layout topology. The X7R or X5R ceramic capacitors are recommended for best performance across temperature and input voltage variations. Note that, in general, the larger input bulk capacitances are typically required when a lower switching frequency is used.

Additional Output Capacitor, Output Ripple, and Transient Response

In a typical buck DC-to-DC converter, the output capacitor connections of the buck regulator are not as critical as the input capacitors because the frequency content of the inductor current waveform is generally much more benign compared to the input current. Nonetheless, the output capacitors' position and orientation may introduce additional parasitic inductance and resistance that can affect the output noise performance.

The LTM3360B also integrates the bulk output capacitor inside its package to ensure minimum output ripple as well as optimum output voltage droop and overshoot performance during load steps and load releases, respectively. In most applications where the LTM3360B can be placed very close to the point-of-loads, no additional output capacitor is necessary. However, in some applications where the location of the point-of-loads is unavoidably distributed and cannot be placed optimally as close as to the LTM3360B, additional output capacitor(s) can be added close to these locations to provide high frequency decoupling closer to the loads.

Care should still be taken to ensure the shortest route from the LTM3360B's V_{OUT} pins to the point-of-loads locations to reduce additional parasitic resistances and inductances. These parasitic components not only affect the overall efficiency but could also affect the overall frequency response of the closed-loop regulation if the V_{OUT}+ and V_{OUT}⁻ sensing is done at any one of these points.

Sensing at points, including the parasitic components, adds secondary high-frequency dynamics to the overall frequency response that may degrade the overall step response of the LTM3360B's load steps and load releases. Note that adding output capacitance generally results in lower ripple output voltage but also a slower transient response.

When additional output capacitors are necessary, X7R or X5R ceramic capacitors are recommended for the best performance across temperature and input voltage variations.

Multiphase Operation

The LTM3360B is designed for easy multiphase operation. One LTM3360B acts as the main control unit, while all other devices should be programmed as subordinates by connecting the M/$\overline{S}$ pins to ground.

The main and subordinate(s) REF, CLK, ITH, AGND, V_{OUT}^+, and V_{OUT}^- pins should be connected to each other. The CLK pins connection ensures that all devices operate at the same frequency with an accurate phase relation.

Table 14 indicates the phase selection for subordinate devices (M/$\overline{S}$ = 0V). The main device always has a phase of 0 degrees. The subordinate phase is set by the states of the PH3, PH2, PH1, and PH0 pins as shown in *Table 14*. Note that the I^2C pins on the subordinate devices are disabled.

The phase selections for the subordinates are designed for simple even spacing for an 8-phase operation (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°) or simple even spacing for a 12-phase operation (0°, 30°, 60°, 90°, 120°, 150°, 180°, 210°, 240°, 270°, 300°, and 330°). With these phasing relations, systems using the LTM3360Bs can also have simple even spacing for any 2-, 3-, 4-, or 6-phase operation. Note that the number of subordinates connected in a multiphase operation is not limited to 11 (+1 main in a 12-phase operation). There can be multiple subordinate devices operating at the same phase. For example, a system using 24 devices can be configured as a 2 × 12-phase system with each of the 12 pairs of LTM3360Bs sharing the same phase.

Table 14. Subordinate Phase Pins Programming

SUBORDINATE PHASE SELECTION				
PH3	**PH2**	**PH1**	**PH0**	**PHASE (DEG)**
0	0	0	0	0
0	0	0	1	30
0	0	1	0	45
0	0	1	1	60
0	1	0	0	90
0	1	0	1	120
0	1	1	0	135
0	1	1	1	150
1	0	0	0	180
1	0	0	1	210
1	0	1	0	225
1	0	1	1	240
1	1	0	0	270
1	1	0	1	300
1	1	1	0	315
1	1	1	1	330

The number of LTM3360B subordinates connected to a single main LTM3360B is only limited by the output buffer capability of the main LTM3360B on the shared pins: REF, ITH, CLK, and AGND. The CLK bus carries the clock signal, which requires its fast edges to maintain integrity for the phase relation between the main and its subordinates to be accurate. Furthermore, capacitive loading and extra delay on the ITH bus degrades the overall multiphase system transient response.

Enabling and Disabling Subordinates in a Multiphase Operation

As described in the *Pin Configurations and Function Descriptions* section, the EN pin(s) of the subordinate(s) should be tied to the main EN pin. Connecting all these pins together ensures that all the parts in a multiphase system turn on and turn off together depending on the state of the EN pin(s). Note, however, that the I^2C port is disabled in the subordinate(s). Therefore, if the main is disabled through I^2C, the effect on the subordinate(s) is delivered through the ITH pin by driving the pin to 0V. The converter is disabled in the subordinate(s) if there is no edge on the CLK pin.

Low Supply Operation

The LTM3360B is designed to operate down to an input supply voltage of 2.9V. See the *Typical Performance Characteristics* section for more details.

Thermal Consideration for Output Short-Circuit and Overload Condition

The LTM3360B is designed to sustain output short-circuit and an overload condition, but it is critical to manage the surface temperature of the device to prevent overheating. Proper heat sinking is essential, and if that is not possible because of other constraints, additional external circuitry, shown in *Figure 27* and *Figure 28*, is recommended to help maintain the LTM3360B's operating temperature.

The $\overline{IRQ}$ pin is tied to the EN pin, which shuts down the device temporarily when the load current exceeds the programmed IMON overcurrent threshold (see the overcurrent warning sections). The resistor (100kΩ) and capacitor (1µF) sets the time delay that allows the device to turn back on once the LTM3360B turns off and its output current falls below the overcurrent threshold. This RC time constant should be carefully chosen based on the $\overline{IRQ}$ maximum pull-down current rating and the surrounding thermal conditions in the application. Such on-off attempts at operation are referred to as a hiccup mode.

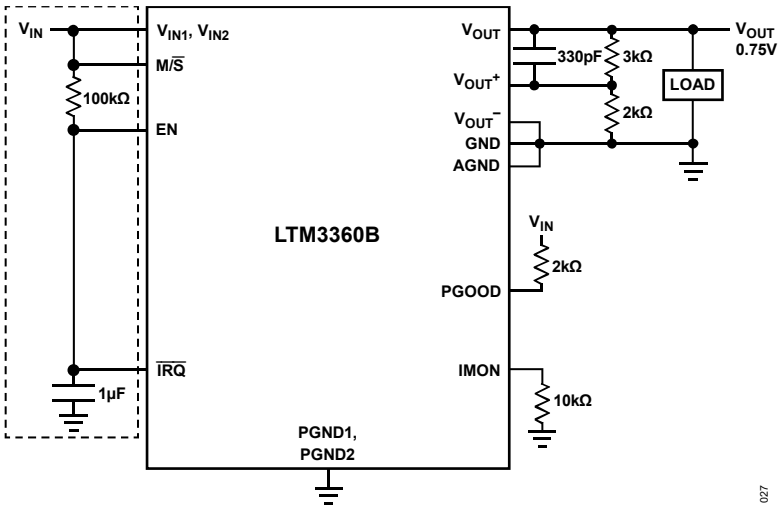


Figure 27. Single Hiccup Mode Application Circuit

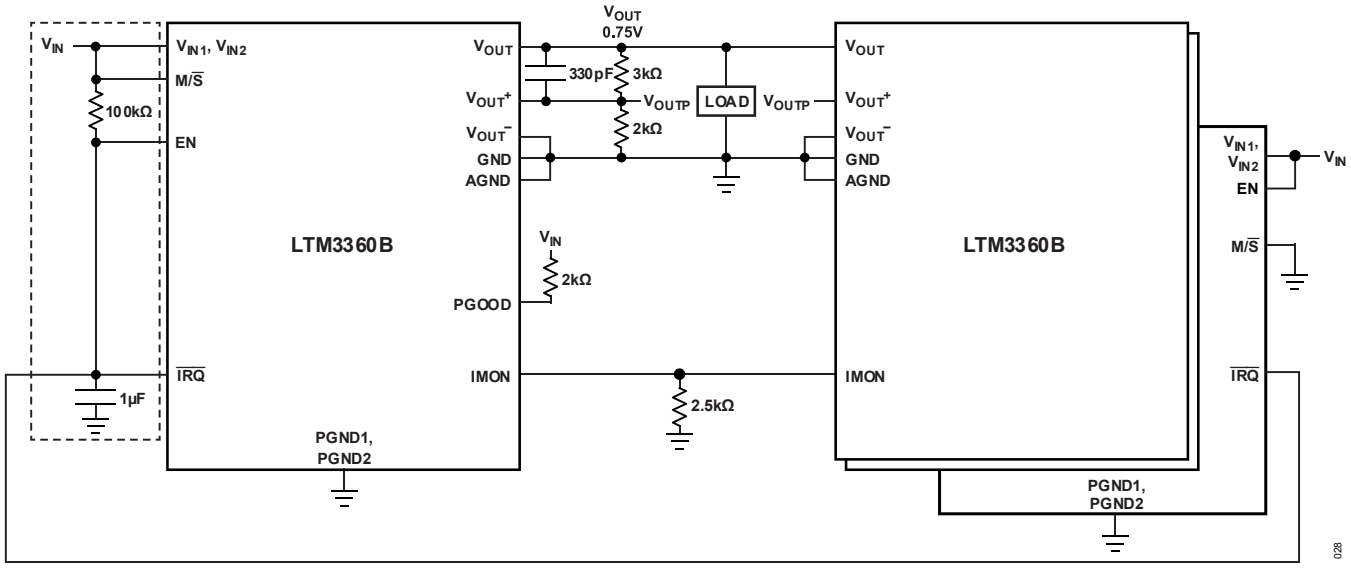


Figure 28. Four × LTM3360B Hiccup Mode Application Circuit

Thermal Derating Curves

The thermal derating curves in *Figure 31* through *Figure 36* can be used to calculate approximate values of θ_{JA} thermal resistance with various airflow conditions.

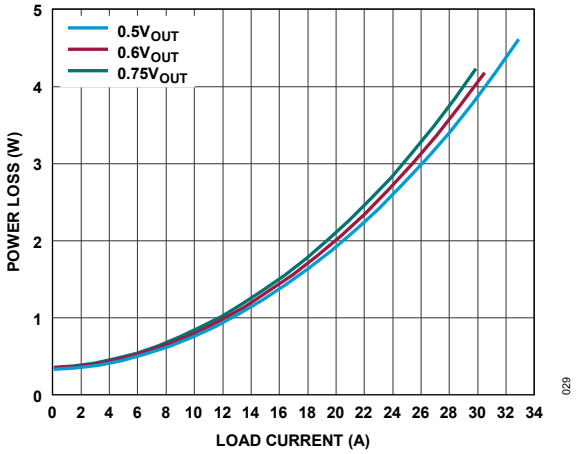


Figure 29. Thermal Derating, Power Loss vs. Load, V_{IN} = 3.3V, V_{OUT} = 0.5V, f_{SW} = 2.5MHz

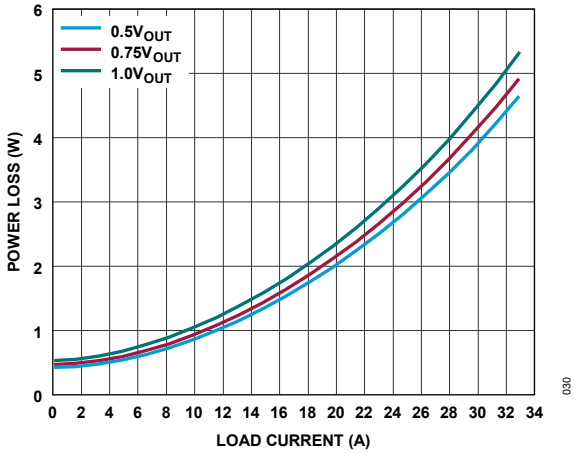


Figure 30. Thermal Derating, Power Loss vs. Load, V_{IN} = 5V, V_{OUT} = 0.5V, f_{SW} = 2.5MHz

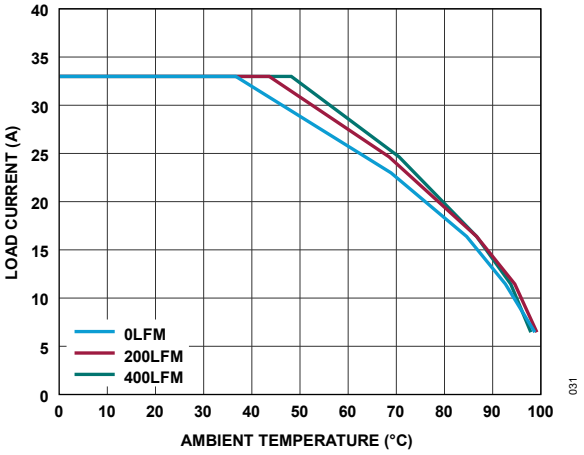


Figure 31. Thermal Derating,
V_{IN} = 3.3V, V_{OUT} = 0.5V, f_{SW} = 2.5MHz

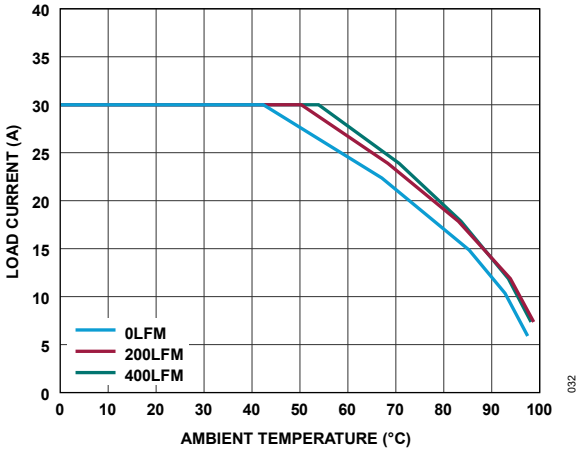


Figure 32. Thermal Derating,
V_{IN} = 3.3V, V_{OUT} = 0.6V, f_{SW} = 2.5MHz

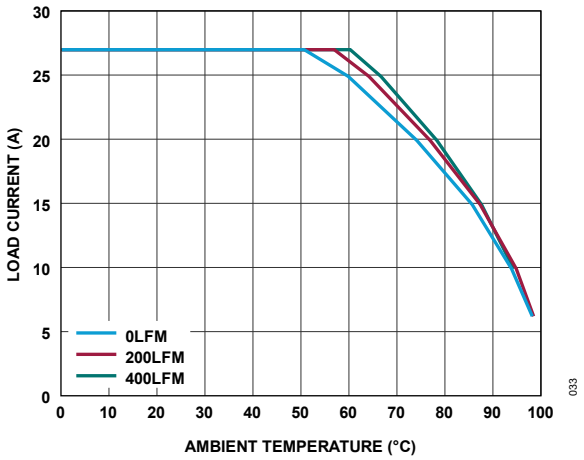


Figure 33. Thermal Derating,
V_{IN} = 3.3V, V_{OUT} = 0.75V, f_{SW} = 2.5MHz

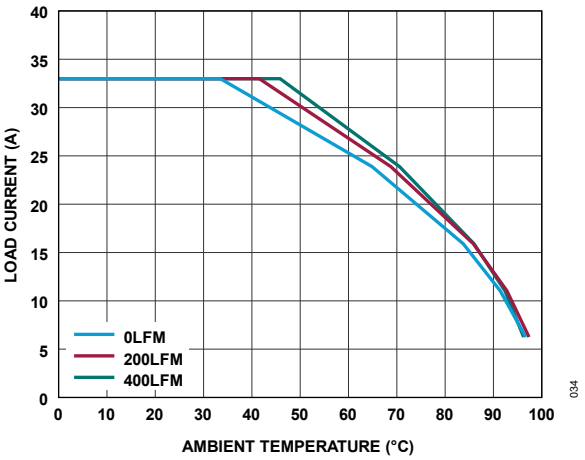


Figure 34. Thermal Derating,
V_{IN} = 5V, V_{OUT} = 0.5V, f_{SW} = 2.5MHz

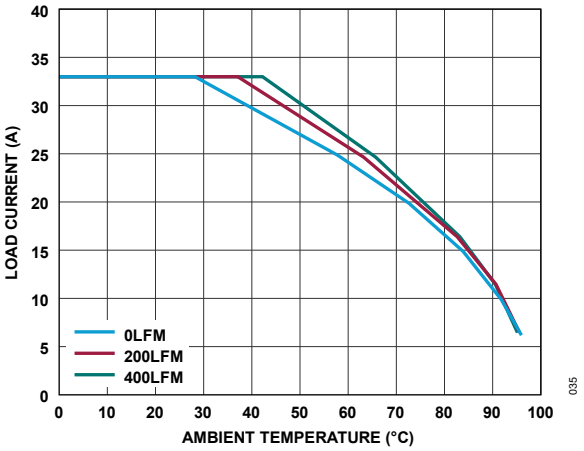


Figure 35. Thermal Derating,
V_{IN} = 5V, V_{OUT} = 0.75V, f_{SW} = 2.5MHz

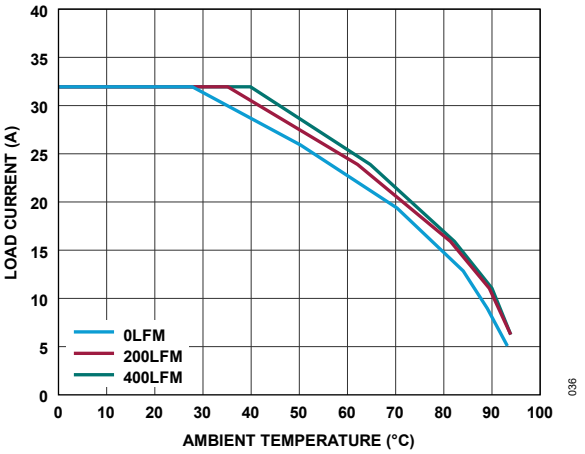
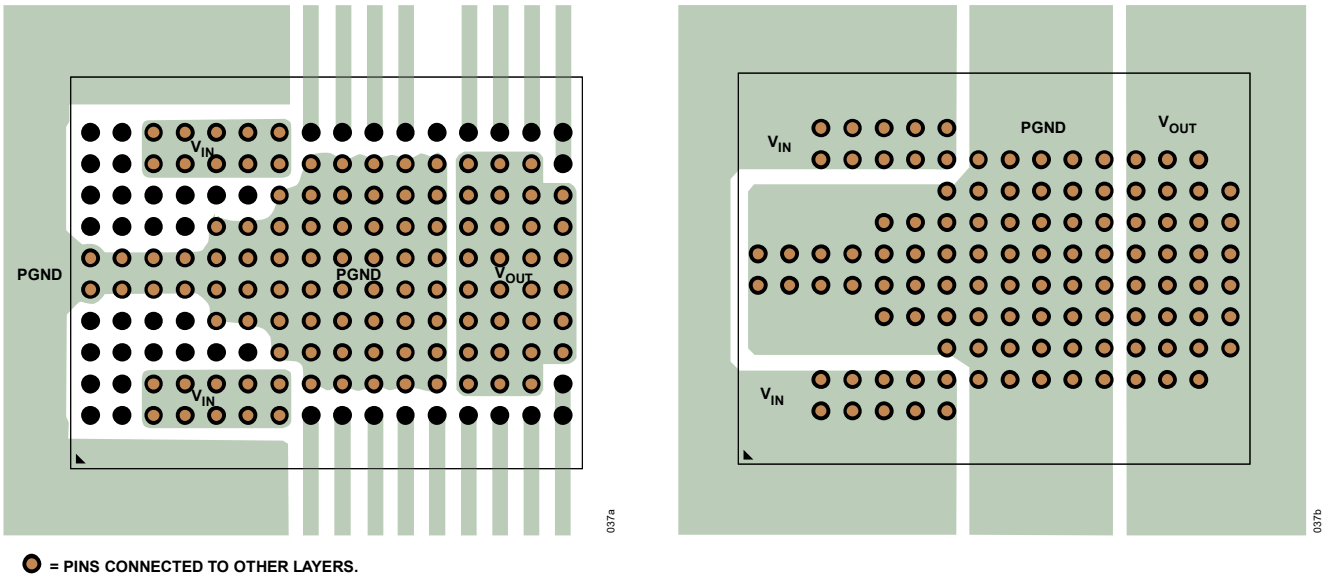


Figure 36. Thermal Derating,
V_{IN} = 5V, V_{OUT} = 1V, f_{SW} = 2.5MHz

PC Board Layout Considerations

The LTM3360B is specifically designed to minimize the electromagnetic interference and the electromagnetic compatibility (EMI/EMC) emissions and to maximize efficiency when switching at high frequencies. For optimal performance, the LTM3360B includes in-package ceramic capacitors to filter out high-frequency switching noise.

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LTM3360B (*Figure 37)*. The PGND(n) and GND pins on the bottom of the package should be soldered to a ground plane. This ground plane should be connected to large copper layers with many thermal vias; these layers spread heat dissipated by the LTM3360B. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating.



(a) Layer One *(b) Internal Layer*

Figure 37. Recommended PCB Layout for the LTM3360B

Typical Applications

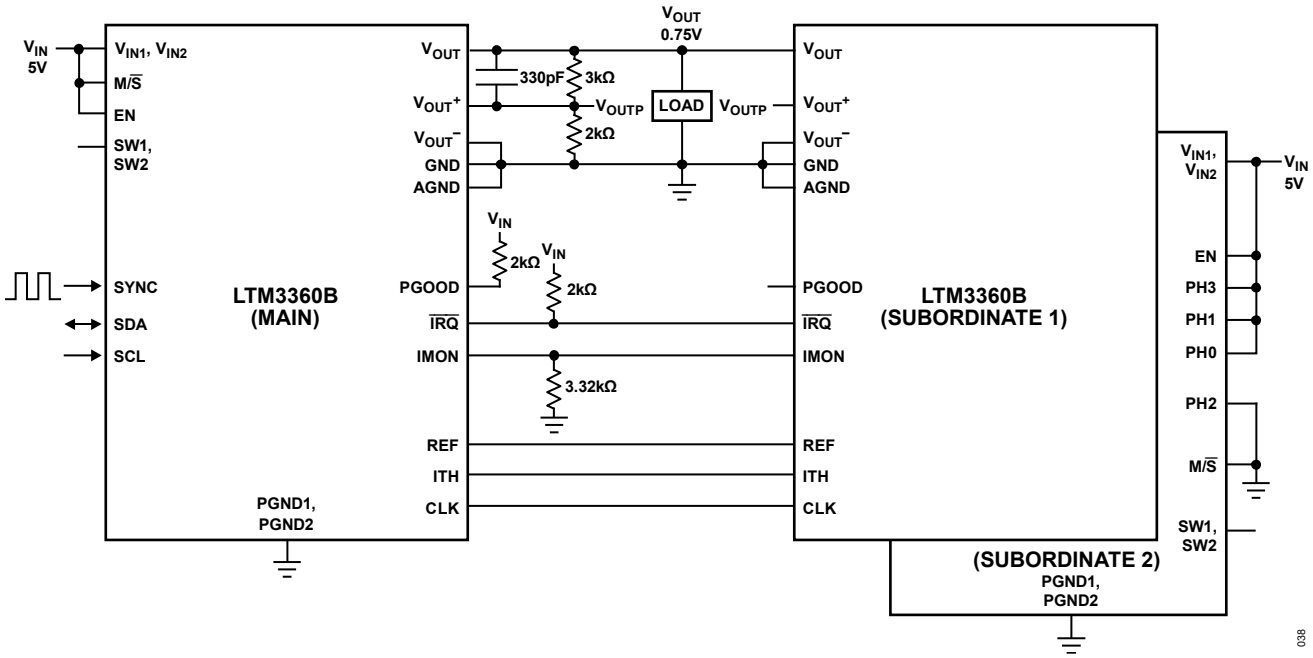


Figure 38. Three × LTM3360B (5V to 0.75V, 99A)

Table 15. Phase Selection

DESIGNATION	PH3	PH2	PH1	PH0	PHASE (DEGREES)
Main	N/A	N/A	N/A	N/A	0
Subordinate 1	GND	V_{IN}	GND	V_{IN}	120
Subordinate 2	V_{IN}	GND	V_{IN}	V_{IN}	240

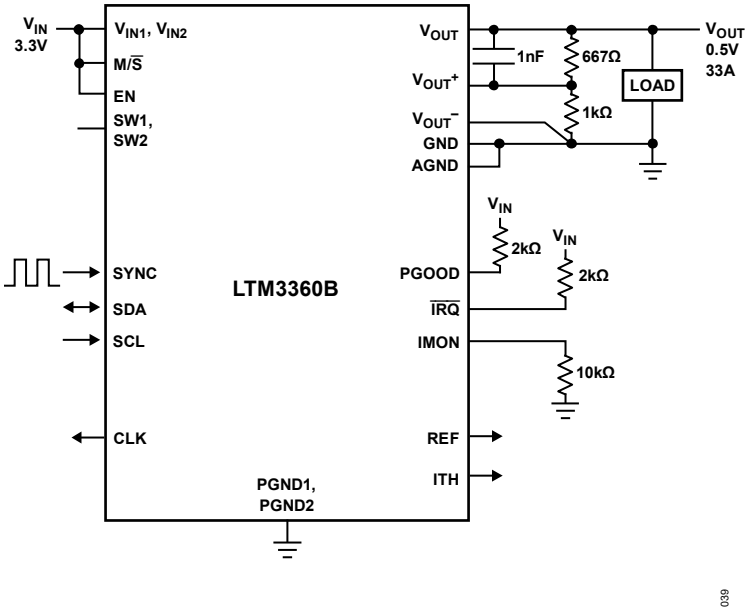


Figure 39. Single LTM3360B (3.3V to 0.5V, 33A)

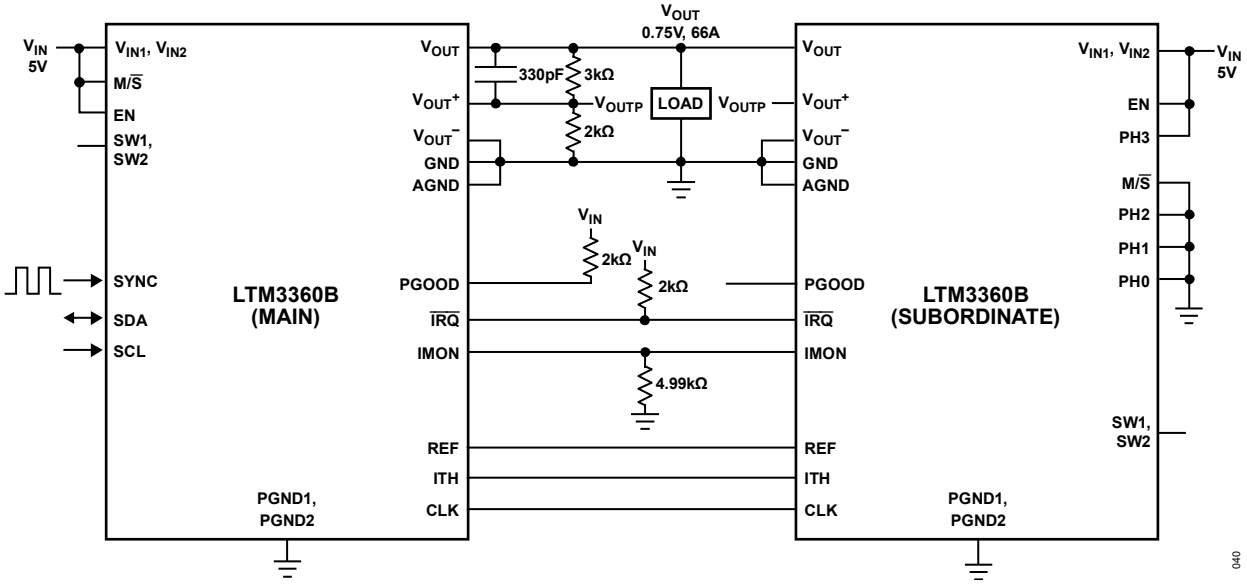


Figure 40. Dual LTM3360B (5V to 0.75V, 66A)

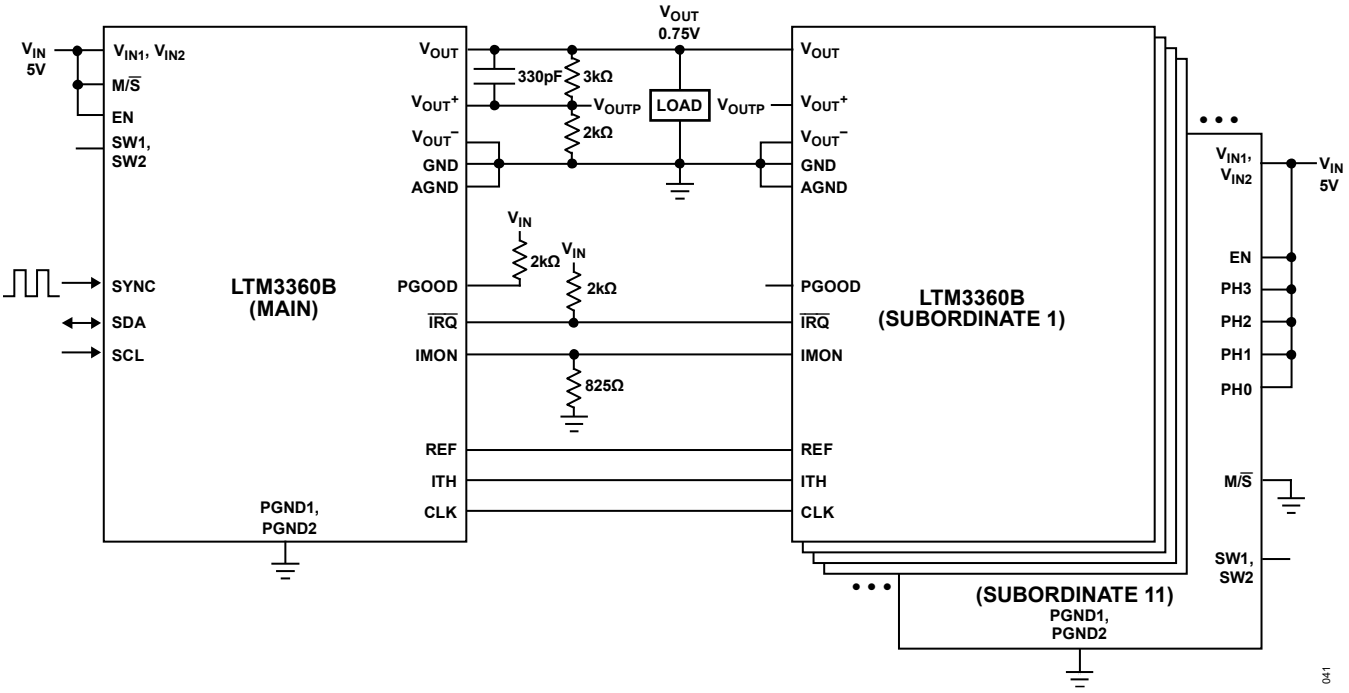


Figure 41. 12× LTM3360B (5V to 0.75V, 396A)

Table 16. Phase Selection

DESIGNATION	PH3	PH2	PH1	PH0	PHASE (DEG)
Main	N/A	N/A	N/A	N/A	0
Subordinate 1	GND	GND	GND	V_{IN}	30
Subordinate 2	GND	GND	V_{IN}	V_{IN}	60
Subordinate 3	GND	V_{IN}	GND	GND	90
Subordinate 4	GND	V_{IN}	GND	V_{IN}	120
Subordinate 5	GND	V_{IN}	V_{IN}	V_{IN}	150
Subordinate 6	V_{IN}	GND	GND	GND	180
Subordinate 7	V_{IN}	GND	GND	V_{IN}	210
Subordinate 8	V_{IN}	GND	V_{IN}	V_{IN}	240
Subordinate 9	V_{IN}	V_{IN}	GND	GND	270
Subordinate 10	V_{IN}	V_{IN}	GND	V_{IN}	300
Subordinate 11	V_{IN}	V_{IN}	V_{IN}	V_{IN}	330

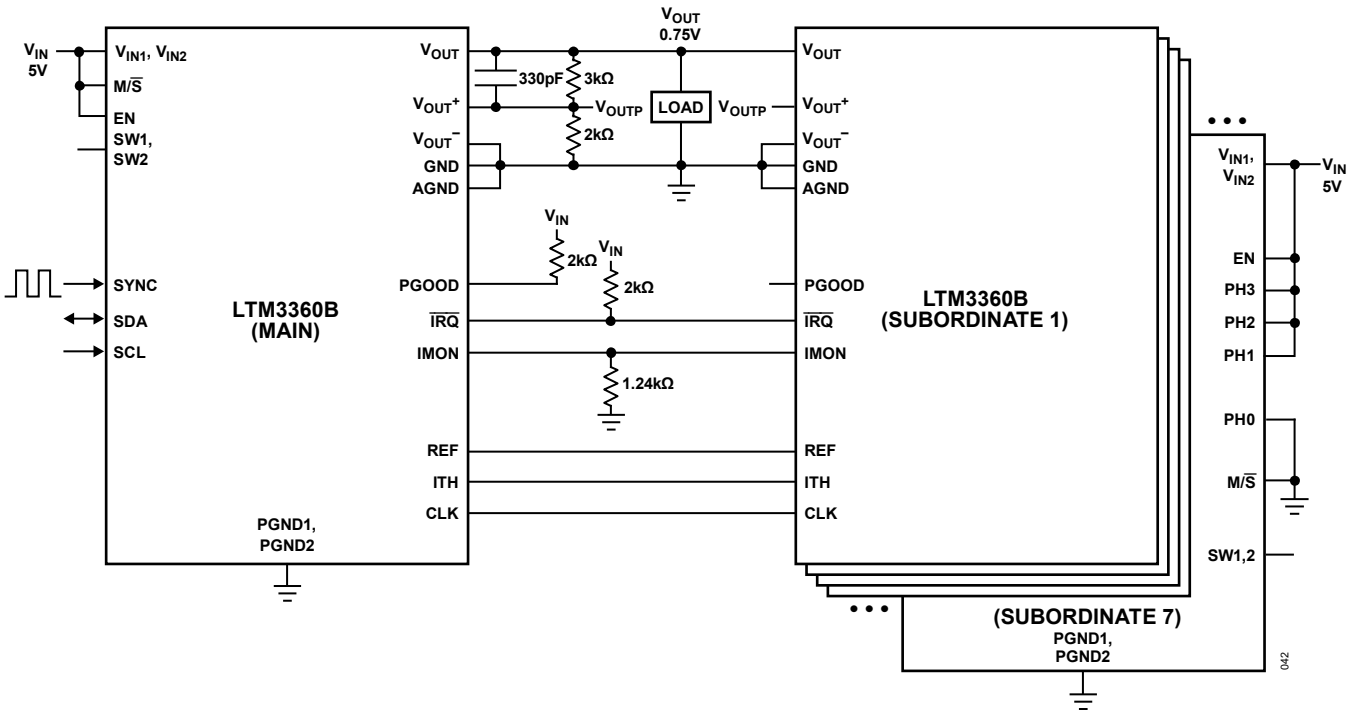


Figure 42. 8 × LTM3360B (5V to 0.75V, 264A)

Table 17. Phase Selection

DESIGNATION	PH3	PH2	PH1	PH0	PHASE (DEG)
Main	N/A	N/A	N/A	N/A	0
Subordinate 1	GND	GND	V_{IN}	GND	45
Subordinate 2	GND	V_{IN}	GND	GND	90
Subordinate 3	GND	V_{IN}	V_{IN}	GND	135
Subordinate 4	V_{IN}	GND	GND	GND	180
Subordinate 5	V_{IN}	GND	V_{IN}	GND	225
Subordinate 6	V_{IN}	V_{IN}	GND	GND	270
Subordinate 7	V_{IN}	V_{IN}	V_{IN}	GND	315

Related Parts

Table 18. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LTM4658	Low V_{IN}, High Efficiency 10A Step-Down DC/DC µModule Regulator	2.25V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ V_{IN}, 4mm × 4mm × 4.32mm LGA, 4mm × 4mm × 4.62mm BGA
LTM4659	Ultrathin, Low V_{IN} 10A Step-Down DC/DC µModule Regulator	2.25V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ V_{IN}, 4mm × 4mm × 1.43mm LGA
LTM4691	Low V_{IN}, High Efficiency, ultrathin, Dual 2A Step-Down DC/DC µModule Regulator	2.25V ≤ V_{IN} ≤ 3.6V, 0.5V ≤ V_{OUT} ≤ 2.5V, 3mm × 4mm × 1.18mm LGA 3mm × 4mm × 1.48mm BGA
LTM4710-1	Low V_{IN}, Quad 8A Silent Switcher® µModule Regulator	2.5V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ 3.6V, 6mm × 12mm × 3.54mm LGA with presolder package
LTM4693	Low V_{IN}, Ultrathin, 2A Buck-Boost µModule Regulator	2.6V ≤ V_{IN} ≤ 5.5V, 1.8V ≤ V_{OUT} ≤ 5.5V, 3.5mm × 4mm × 1.25mm LGA
LTM4611	Ultralow V_{IN}, 15A DC/DC µModule (Power Module) Regulator	1.5V ≤ V_{IN} ≤ 5.5V, 0.8V ≤ V_{OUT} ≤ 5V, 15mm × 15mm × 4.32mm LGA
LTM4670	Low V_{IN}, Quad µModule Regulator with Configurable 10A Output Array	2.25V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ V_{IN}, 7.5mm × 15mm × 4.65mm BGA

OUTLINE DIMENSIONS

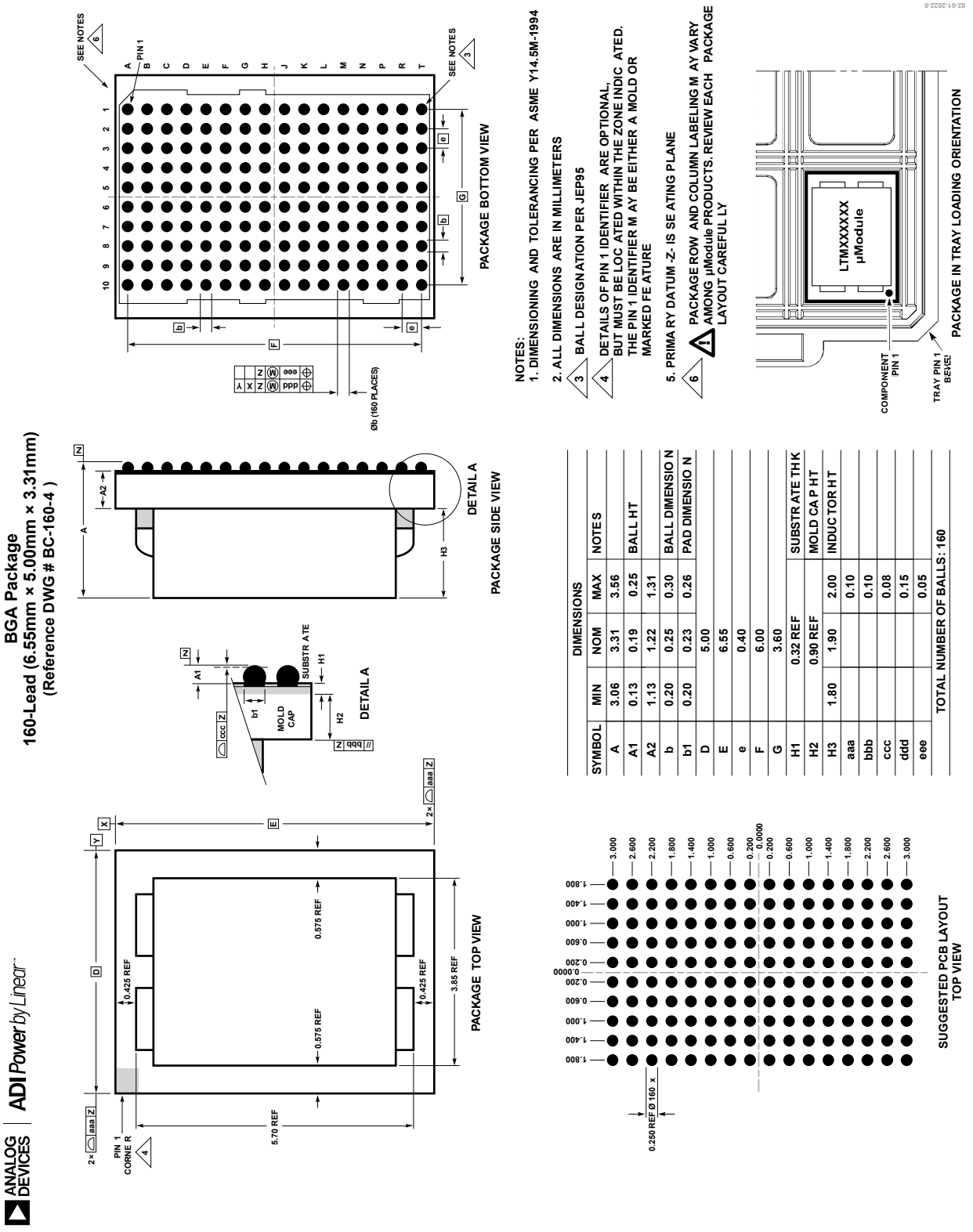


Figure 43. 160-Lead, 6.55mm × 5mm × 3.31mm, BGA

ORDERING GUIDE

Table 19. LTM3360B Ordering Information

MODEL	TEMPERATURE RANGE[1, 2]	PACKAGE DESCRIPTION	PACKAGE OPTION[5]
LTM3360BIY#PBF	–40°C to 105°C	LTM3360B device marking SAC305 (RoHS) pad finish [3] e1 finish code Moisture sensitivity level 4 (MSL 4) rated device[4]	*160-Lead, 6.55mm × 5mm × 3.31mm, BGA*

1 The LTM3360B is tested under conditions such that $T_J \approx T_A$. The LTM3360B is guaranteed to meet specifications from 0°C to 105°C junction temperature. Specifications over the –40°C to 105°C operating junction temperature are assured by design, characterization, and correlation with statistical process controls. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and from the power dissipation (P_D, in Watts) according to the following formula: $T_J = T_A + (P_D \times \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

2 Contact the factory for parts specified with wider operating temperature ranges.

3 The pad finish code is per IPC/JEDEC J-STD-609.

4 This product is not recommended for second-side reflow and is sensitive to moisture. For more information, refer to the Analog Devices *µModule LGA and BGA Packaging Care and Assembly Instructions* document.

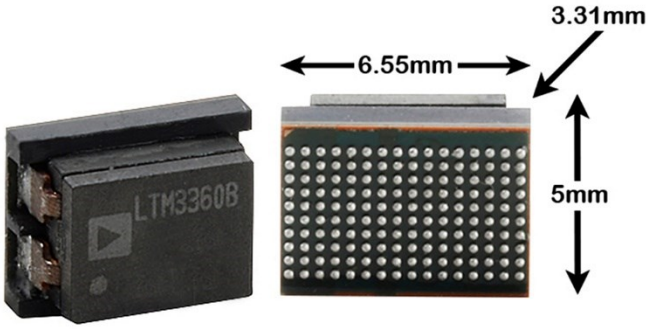
5 The BGA package should follow assembly and manufacturing procedures. For more information, refer to the Analog Devices *Assembly Considerations for the µModule BGA and LGA Packages* guidelines.

Table 20. Evaluation Board Ordering Information

MODEL	DESCRIPTION
EVAL-LTM3360B-AZ	LTM3360B evaluation board.

SELECTOR GUIDE

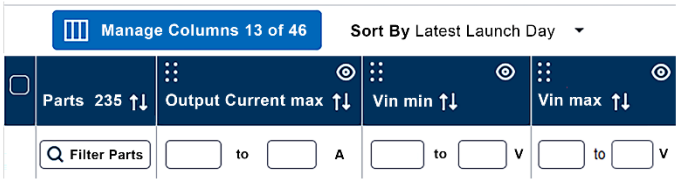
Package Photos



(Part marking is laser mark)

Design Resources

Table 21. µModule Power Technology

RESOURCES	DESCRIPTION	
µModule Design, Manufacturing, and Assembly	**Design** ▶ Evaluation guide boards and Gerber files ▶ Free design tools, including LTspice® and LTpowerCAD® ▶ Circuit simulations	**Manufacturing** ▶ Quick start guides ▶ PCB design, assembly, and manufacturing guidelines ▶ Package and board level reliability
µModule Regulator Products Search	▶ Manage columns and sort table of products by parameters and download the result as a spread sheet. 	
Digital Power System Management	The Analog Devices family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	