LTC7899

140V, Low I_Q, Negative to Positive Synchronous Boost Controller with 10V Gate Drive

FEATURES

- Converts Negative Input to Positive Output Regulated with Respect to Ground
- Wide $|V_{IN}^-|+V_{OUT}$ Range: 4V to 135V (140V ABS MAX)
- Internal Feedback Level Shifter for Easy Output Voltage Programming with Two Resistors
- Adjustable Gate Drive Level: 5V to 10V (OPTI-DRIVE, 14V ABS MAX)
- Adjustable Driver Voltage UVLO
- Adaptive or Resistor-Adjustable Dead Times
- Split-Output Gate Drivers for Adjustable Turn-On and Turn-Off Driver Strengths
- Supports Positive Input to Positive Output Boost Up to 135V with Pass-Through
- Operation Down to 1V after Start-Up
- CLK Output for High Power PolyPhase Operation
- Spread Spectrum Frequency Modulation
- Programmable Frequency (100kHz to 2.5MHz)
- Phase-Lockable Frequency (100kHz to 2.5MHz)
- 28-Pin (4mm x 5mm) QFN Package

APPLICATIONS

- Industrial Power Systems
- Military/Avionics
- Telecommunications Power Systems

GENERAL DESCRIPTION

The *LTC®7899* is a high performance DC/DC negative to positive switching regulator controller that drives all N-channel synchronous MOSFET stages and can operate from input voltages up to 135V. The positive output voltage can easily be programmed with only two resistors by using the integrated feedback level shifter. The LTC7899 can alternatively be configured as a step-up (Boost) operation with pass-through.

The gate drive voltage for the LTC7899 can be programmed from 5V to 10V to allow the use of logic or standard-level MOSFETs to maximize efficiency.

The low no-load quiescent current extends operating run time in battery-powered systems. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The user can adjust the dead times of the LTC7899 with external resistors for margin or to tailor the application for higher efficiency and allow for high frequency operation.

The LTC7899 additionally features spread spectrum operation, which significantly reduces the peak radiated and conducted noise on both the input and output supplies, making it easier to comply with electromagnetic interference (EMI) standards.

TYPICAL APPLICATION

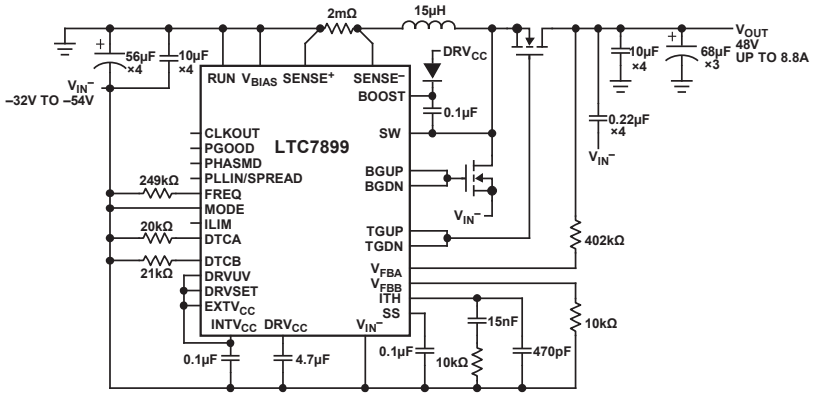

Figure 1. High Power -48V Input to 48V Output Converter

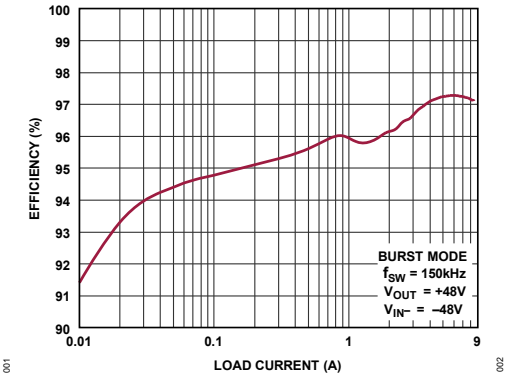

Figure 2. V_{OUT} Efficiency for Figure 1

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	7/25	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are for T_J = -40°C to +150°C for the minimum and maximum values, T_A = 25°C for the typical values, all voltages are with respect to V_{IN}^- unless otherwise noted. (GND to V_{IN}^-) = 12V, RUN = 5V, $EXTV_{CC}$ = $INTV_{CC}$, DRVSET = 0V, DRVUV = 0V, TGUP = TGDN = TGxx, BGUP = BGDN = BGxx, and DTCA and DTCB = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Input Supply (V_{IN})						
Bias Input Supply Operating Range	V_{BIAS}		4		135	V
Input Supply Operating Range	$\lvert V_{IN}^- \rvert$	$V_{BIAS} \geq 4V$	1		135	V
Regulated Output Voltage Set Point	V_{OUT}	with respect to V_{IN}^-	1.2		135	V
Controller Operation						
Regulated Feedback Voltage with respect to V_{IN}^- [2]	V_{FBB}	V_{BIAS} = 4V to 135V, ITH Voltage = 0.6V to 1.2V	1.188	1.2	1.212	V
Regulated Feedback Voltage with respect to $SENSE^+$	V_{FBA}	V_{BIAS} = 4V to 135V, ITH Voltage = 0.6V to 1.2V	-50	0	50	mV
V_{FBB} Feedback Current[2]		$V_{FBA} = (V_{SENSE}^+ + 100mV)$	-50	0	+50	nA
Feedback Overvoltage Threshold		Relative to V_{FBB}, T_A = 25°C	7	10	13	%
Transconductance Amplifier g_m[2]	g_m	ITH = 1.2V, Sink and Source = 5µA		1.8		mmho
Maximum Current Sense Threshold	$V_{SENSE(MAX)}$	V_{FBB} = 1.1V, $SENSE^+$ = 12V ILIM = 0V ILIM = floating ILIM = $INTV_{CC}$	 21 45 67	 25 50 75	 29 55 83	 mV mV mV
$SENSE^-$ Pin Current	I_{SENSE}^-	$SENSE^-$ = 3.3V, T_A = 25°C	-1		+1	µA
$SENSE^+$ Pin Current	I_{SENSE}^+	$SENSE^+ < 3V$ $3.2V \leq SENSE^+ < INTV_{CC} - 0.5V$ $SENSE^+ > INTV_{CC} + 0.5V$		1 80 700		µA µA µA

(Specifications are for T_J = -40°C to +150°C for the minimum and maximum values, T_A = 25°C for the typical values, all voltages are with respect to V_{IN}^- unless otherwise noted. (GND to V_{IN}^-) = 12V, RUN = 5V, $EXTV_{CC}$ = $INTV_{CC}$, DRVSET = 0V, DRVUV = 0V, TGUP = TGDN = TGxx, BGUP = BGDN = BGxx, and DTCA and DTCB = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Soft-Start Charge Current		SS = 0V	7	9	11	µA
RUN Pin ON Threshold RUN Pin Hysteresis		RUN Rising	1.15	1.20 120	1.25	V mV
DC Supply Current						
V_{BIAS} Shutdown Current		RUN = 0V		1		µA
V_{BIAS} Sleep Mode Current		$SENSE^+$ < 3.2V, $EXTV_{CC}$ = $INTV_{CC}$		15		µA
Sleep Mode Current[3] V_{BIAS} Current V_{BIAS} Current $EXTV_{CC}$ Current $SENSE^+$ Current		 $SENSE^+$ ≥ 3.2V, $EXTV_{CC}$ = $INTV_{CC}$ $SENSE^+$ ≥ 3.2V, $EXTV_{CC}$ ≥ 12V $SENSE^+$ ≥ 3.2V, $EXTV_{CC}$ ≥ 12V $SENSE^+$ ≥ 3.2V		 5 1 10 10		 µA µA µA µA
Pulse-Skipping or Forced Continuous Mode (FCM), V_{BIAS} or $EXTV_{CC}$ Current[3]				2.5		mA
Gate Drivers						
TGxx or BGxx On-Resistance		DRVSET = $INTV_{CC}$ Pull-up Pull-down		 2.0 1.0		 Ω Ω
TGxx or BGxx Transition Time[4] Rise Time Fall Time		 C_{LOAD} = 3300pF C_{LOAD} = 3300pF		 25 15		 ns ns
TGxx Off to BGxx On Adaptive Delay Time[5]		DTCA = 0V DTCA = $INTV_{CC}$		80 30		ns ns
BGxx Off to TGxx On Adaptive Delay Time[5]		DTCB = 0V DTCB = $INTV_{CC}$		80 30		ns ns

(Specifications are for T_J = -40°C to +150°C for the minimum and maximum values, T_A = 25°C for the typical values, all voltages are with respect to V_{IN}^- unless otherwise noted. (GND to V_{IN}^-) = 12V, RUN = 5V, $EXTV_{CC}$ = $INTV_{CC}$, DRVSET = 0V, DRVUV = 0V, TGUP = TGDN = TGxx, BGUP = BGDN = BGxx, and DTCA and DTCB = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
BGxx Off to TGxx On Open-Loop Delay[5]		DTCA = 10k DTCA = 50k DTCA = 100k		13 50 100		ns ns ns
TGxx Off to BGxx On Open-Loop Delay[5]		DTCB = 10k DTCB = 50k DTCB = 100k		13 50 100		ns ns ns
BG Minimum On-Time[6]	$t_{ON(MIN)}$			120		ns
Maximum Duty Cycle for BGx		FREQ = 0V		93		%
Charge Pump for BST-SW Supply						
Charge Pump Output Current		V_{BST-SW} = 7V, V_{SW} = 0V V_{SW} = 12V		-120 -80		µA µA
Charge Pump Output Voltage	V_{BST-SW}	I_{BST} = −1µA, V_{SW} = 0V and 12V	10	11	12	V
Low Dropout (LDO) Linear Regulators						
DRV_{CC} Voltage for V_{BIAS} and $EXTV_{CC}$ LDOs		$EXTV_{CC}$ = $INTV_{CC}$ for V_{BIAS} LDO, $EXTV_{CC}$ = 12V for $EXTV_{CC}$ LDO DRVSET = $INTV_{CC}$ DRVSET = 64.9kΩ DRVSET = 0V	 9.5 5.8 5.8	 9.77 6.5 6.0	 10.0 7.0 6.2	 V V V
DRV_{CC} Load Regulation		DRV_{CC} load current = 0mA to 100mA, T_A = 25°C		1	3	%
Undervoltage Lockout	UVLO	DRV_{CC} Rising DRVUV = $INTV_{CC}$ DRVUV = floating DRVUV = 0V	 7.1 5.2 3.8	 7.4 5.35 3.93	 7.6 5.5 4.0	 V V V
		DRV_{CC} Falling DRVUV = $INTV_{CC}$ DRVUV = floating DRVUV = 0V	 6.4 4.9 3.6	 6.64 5.05 3.71	 6.8 5.2 3.8	 V V V

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PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
$EXTV_{CC}$ LDO Switchover Voltage $EXTV_{CC}$ Rising		DRVUV = $INTV_{CC}$, T_A = 25°C DRVUV = floating, T_A = 25°C DRVUV = 0V, T_A = 25°C	7.5 5.9 4.6	7.7 6.1 4.8	8.0 6.4 5.1	V V V
$EXTV_{CC}$ Switchover Hysteresis $EXTV_{CC}$ Falling				250		mV
$INTV_{CC}$ Regulation Point				4.5		V
Spread Spectrum Oscillator and Phase-Locked Loop						
Fixed Frequency	f_{OSC}	PLLIN/SPREAD = 0V FREQ = 0V, T_A = 25°C FREQ = $INTV_{CC}$ FREQ = 374kΩ FREQ = 75kΩ, T_A = 25°C FREQ = 14.7kΩ	 320 2.0 450 	 370 2.25 100 500 2.5	 420 2.5 550 	 kHz MHz kHz kHz MHz
Synchronizable Frequency Range	f_{SYNC}	PLLIN/SPREAD = External Clock	0.1		2.5	MHz
PLLIN Input High Level			2.2			V
PLLIN Input Low Level					0.5	V
Spread Spectrum Frequency Range (Relative to f_{OSC})		PLLIN/SPREAD = $INTV_{CC}$ Minimum Frequency Maximum Frequency		 0 20		 % %
PGOOD Output						
PGOOD Voltage Low		I_{PGOOD} = 2mA, T_A = 25°C		0.2	0.4	V
PGOOD Leakage Current		PGOOD = 5V, T_A = 25°C	-1		+1	µA
PGOOD Trip Level V_{FBB} with Respect to Set Regulated Voltage		T_A = 25°C V_{FBB} Rising Hysteresis V_{FBB} Falling Hysteresis	 7 -13 	 10 2.5 -10 2.5	 13 -7 	 % % % %

(Specifications are for T_J = -40°C to +150°C for the minimum and maximum values, T_A = 25°C for the typical values, all voltages are with respect to V_{IN}^- unless otherwise noted. (GND to V_{IN}^-) = 12V, RUN = 5V, $EXTV_{CC}$ = $INTV_{CC}$, DRVSET = 0V, DRVUV = 0V, TGUP = TGDN = TGxx, BGUP = BGDN = BGxx, and DTCA and DTCB = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
PGOOD Delay for Reporting a Fault				25		µs

1 This specification is not tested in production.

2 The LTC7899 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FBB}.

3 Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

4 Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

5 TGxx falling to BGxx rising and BGxx falling to TGxx rising delay times are measured at rising/falling thresholds on TGxx and BGxx of approximately 1.5V. See *Figure 37* and *Figure 38* .

6 The minimum on-time condition specified for inductor peak-to-peak ripple current is >40% of the maximum load current (I_{MAX}) (see the *Minimum On-Time Considerations* section).

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified. All pins are with respect to V_{IN}^- unless otherwise noted.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
Bias Input Supply (V_{BIAS})	–0.3V to 140V
RUN	–0.3V to 140V
BOOST	–0.3V to 150V
SW	–5V to 150V
BOOST to SW	–0.3V to 15V
TGUP, TGDN, BGUP, BGDN[1]	Not applicable
$EXTV_{CC}$	–0.3V to 30V
DRV_{CC}	–0.3V to 14V
$EXTV_{CC}$ to DRV_{CC}	-6V to 30V
$INTV_{CC}$	–0.3V to 6V
V_{FBB}	–0.3V to 6V
PLLIN/SPREAD, FREQ, PHASMD	–0.3V to 6V
SS, ITH, ILIM	–0.3V to 6V
DRVSET, DRVUV, PGOOD	–0.3V to 6V
DTCA, DTCB, MODE, CLKOUT	–0.3V to 6V
V_{FBA}	–0.3V to 140V
V_{FBA} to $SENSE^-$	–0.3V to 0.3V
$SENSE^+$, $SENSE^-$	–0.3V to 140V
$SENSE^+$ to $SENSE^-$ Continuous	–0.3V to 6V
$SENSE^+$ to $SENSE^-$ < 1ms	-100mA to 100mA
Operating Junction Temperature Range[2]	–40°C to 150°C
Storage Temperature Range	–65°C to 150°C

[1] Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only. Otherwise, permanent damage can occur.

[2] The LTC7899 is specified over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with the board layout, rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the following formula: $T_J = T_A + (P_D \times \theta_{JA})$, where θ_{JA} is the package thermal impedance and equals 43°C/W for the 28-lead (4mm × 5mm), quad flat no lead (QFN) package.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

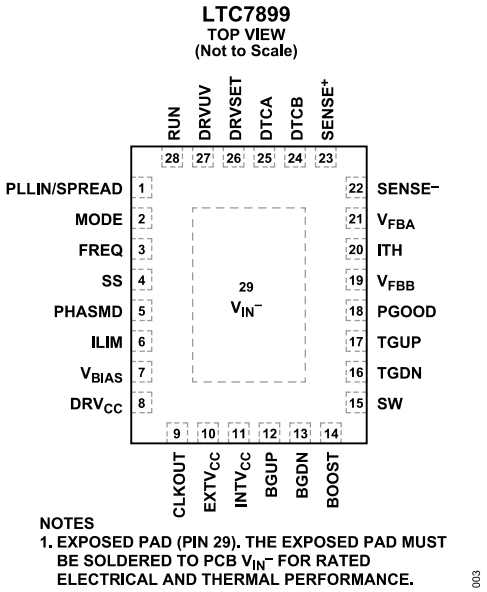


Figure 3. Pin Configuration

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	PLLIN/ SPREAD	External Synchronization Input to Phase Detector and Spread Spectrum Enable. When an external clock is applied to this pin, the phase-locked loop will force the rising BG signal to be synchronized with the rising edge of the external clock. When not synchronizing to an external clock, tie this input to $INTV_{CC}$ to enable spread spectrum dithering of the oscillator or to V_{IN}^- to disable spread spectrum.
2	MODE	Mode Select Input. This input determines how the LTC7899 operates at light loads. Connect MODE to V_{IN}^- to select the Burst Mode operation. An internal 100kΩ resistor to V_{IN}^- also invokes Burst Mode operation when MODE is floating. Connect MODE to $INTV_{CC}$ to force continuous inductor current operation. Tying MODE to $INTV_{CC}$ through a 100kΩ resistor selects the pulse-skipping operation.
3	FREQ	Frequency Control Pin for the Internal Voltage Controlled Oscillator (VCO). Connect FREQ to V_{IN}^- for a fixed frequency of 370kHz. Connect FREQ to $INTV_{CC}$ for a fixed frequency of 2.25MHz. Program frequencies between 100kHz and 2.5MHz by using a resistor between FREQ and V_{IN}^-. Minimize the capacitance on FREQ.
4	SS	External Soft Start Input. SS regulates the V_{FBB} voltage to the lesser of 1.2V or the voltage on the SS pin. An internal 9µA pull-up current source is connected to SS. A capacitor to V_{IN}^- at SS sets the ramp time to the final regulated output voltage. The ramp time is equal to 1 ms for every 7.5nF of capacitance.
5	PHASMD	Control Input to Phase Selector. This determines the CLKOUT phase relationships with respect to BG. Pulling this pin to V_{IN}^- forces CLKOUT to be out of phase 90° with respect to BG. Connecting this pin to $INTV_{CC}$ forces CLKOUT to be out of phase 120° with

		respect to BG. Floating this pin forces CLKOUT to be out of phase 180° with respect to BG.
6	ILIM	Current Comparator Sense Voltage Range Input. Tying this pin to V_{IN}^- or $INTV_{CC}$ or floating it sets the maximum current sense threshold to one three different levels (25mV, 75mV, and 50mV, respectively).
7	V_{BIAS}	Main Supply Pin. A bypass capacitor should be tied between this pin and V_{IN}^-. For Negative to Positive converters this pin is typically tied to GND.
8	DRV_{CC}	Gate Driver Output of the internal LDO regulator from V_{BIAS} or $EXTV_{CC}$. The gate drivers and the $INTV_{CC}$ internal LDO are powered from DRV_{CC}. A low ESR 4.7µF ceramic bypass capacitor should be connected between DRV_{CC} and V_{IN}^-, as close as possible to the IC.
9	CLKOUT	Output Clock Signal. This signal is available to daisy-chain other controller ICs for additional MOSFET driver stages/phases. The output levels swing from $INTV_{CC}$ to V_{IN}^-.
10	$EXTV_{CC}$	External Power Input to an Internal LDO Regulator Connected to DRV_{CC}. This LDO regulator supplies $INTV_{CC}$ power, bypassing the internal V_{BIAS} LDO regulator whenever $EXTV_{CC}$ is higher than the $EXTV_{CC}$ switchover voltage. See the $EXTV_{CC}$ connection in the *Power and Bias Supplies (VBIAS, EXTVCC, DRVCC, and INTVCC)* section. Do not exceed 30V on $EXTV_{CC}$. Connect $EXTV_{CC}$ to $INTV_{CC}$ if the $EXTV_{CC}$ LDO regulator is not used.
11	$INTV_{CC}$	Output of the Internal 4.5V Low Dropout Regulator from DRV_{CC}. The internal analog and digital circuits are powered from this pin. A low ESR 0.1µF ceramic bypass capacitor should be connected between $INTV_{CC}$ and V_{IN}^-, as close as possible to the IC.
12	BGUP	High Current Gate Driver Pull-Up for Bottom MOSFET. BGUP pulls up to DRV_{CC}. Tie BGUP directly to the bottom MOSFET gate for maximum gate drive transition speed on the gate rising edge. Tie a resistor between BGUP and the bottom MOSFET gate to adjust the gate rising slew rate. BGUP also serves as the Kelvin sense of the bottom MOSFET gate during turn-off.
13	BGDN	High Current Gate Driver Pull-Down for Bottom MOSFET. BGDN pulls down to V_{IN}^-. Tie BGDN directly to the bottom MOSFET gate for maximum gate drive transition speed on the gate falling edge. Tie a resistor between BGDN and the bottom MOSFET gate to adjust the gate falling slew rate. BGDN also serves as the Kelvin sense of the bottom MOSFET gate during turn-on.
14	BOOST	Bootstrapped Supply to the Top Side Floating Driver. Connect a capacitor between the BOOST and SW pins. Also connect a Schottky diode between the BOOST and DRV_{CC} pins. The differential voltage swing at the BOOST pin is $(V_{OUT} + \lvert V_{IN}^- \rvert)$.
15	SW	Switch Node Connection to Inductor.
16	TGDN	High Current Gate Driver Pull-Down for Top MOSFET. TGDN pulls down to SW. Tie TGDN directly to the top MOSFET gate for maximum gate drive transition speed on the gate falling edge. Tie a resistor between TGDN and the top MOSFET gate to adjust the gate falling slew rate.
17	TGUP	High Current Gate Driver Pull-Up for Top MOSFET. TGUP pulls up to BOOST. Tie TGUP directly to the top MOSFET gate for maximum gate drive transition speed on the gate rising edge. Tie a resistor between TGUP and the top MOSFET gate to adjust the gate rising slew rate.

18	PGOOD	Power Good Open-Drain Logic Output. PGOOD is pulled to V_{IN}^- when the voltage on V_{FBB} is not within ±10% of its set point.
19	V_{FBB}	Receives the remotely sensed feedback voltage for controller from an external resistor to V_{IN}^-. This is the input to the Error Amplifier.
20	ITH	Error Amplifier Output and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage.
21	V_{FBA}	Input Power Supply Voltage Sense Pin. An external feedback resistor is tied from the V_{FBA} to V_{OUT}. The pin voltage is regulated to the $SENSE^+$ voltage.
22	$SENSE^-$	The Negative (–) Input to the Differential Current Comparator. The ITH pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} set the current trip threshold.
23	$SENSE^+$	The Positive (+) Input to the Differential Current Comparator. The $SENSE^+$ pin supplies current to the current comparator when it is greater than $INTV_{CC}$. When $SENSE^+$ is 3.2V or greater, it supplies the majority of the sleep mode quiescent current instead of V_{BIAS}, further reducing the input-referred quiescent current.
24	DTCB	Dead Time Control Pin for TG Off to BG On Delay. Connect to V_{IN}^- to program an adaptive TG falling to BG rising dead time delay of approximately 50ns. Connect to $INTV_{CC}$ to program and adaptive TG falling to BG rising delay of approximately 30ns. Connect a resistor between DTCB and V_{IN}^- to add additional delay (from 13ns to 100ns) between the time TG falling and BG rising.
25	DTCA	Dead Time Control Pin for BG Off to TG On Delay. Connect to V_{IN}^- to program an adaptive BG falling to TG rising dead time delay of approximately 50ns. Connect to $INTV_{CC}$ to program an adaptive BG falling to TG rising dead time delay of approximately 30ns. Connect a resistor between DTCA and V_{IN}^- to add additional delay (from 13ns to 100ns) between the time BG falling and TG rising.
26	DRVSET	DRV_{CC} Regulation Program pin. This pin sets the regulation point for the DRV_{CC} low dropout (LDO) linear regulator. Connect to V_{IN}^- to set DRV_{CC} to 6.0V. Connect to $INTV_{CC}$ to set DRV_{CC} to 9.7V. Program voltages between 5V and 10V by placing a resistor (50k to 100k) between DRVSET and V_{IN}^-. The resistor and an internal 20µA source current create a voltage used by the DRV_{CC} LDO regulator to set the regulation point.
27	DRVUV	DRV_{CC} UVLO and $EXTV_{CC}$ Switchover Program Pin. DRVUV determines the DRV_{CC} UVLO and $EXTV_{CC}$ switchover rising and falling thresholds, as listed in *Table 1*.
28	RUN	Run Control Input for the Controller. Forcing the RUN pin below 1.1V disables control, while forcing the RUN pin below 0.7V shuts down the entire LTC7899, reducing quiescent current to approximately 1µA. Tie the RUN pin to V_{BIAS} for always-on operation.
29	V_{IN}^- (EPAD)	Negative Input Voltage. The exposed pad must be soldered to PCB V_{IN}^- for rated electrical and thermal performance.

BLOCK DIAGRAM

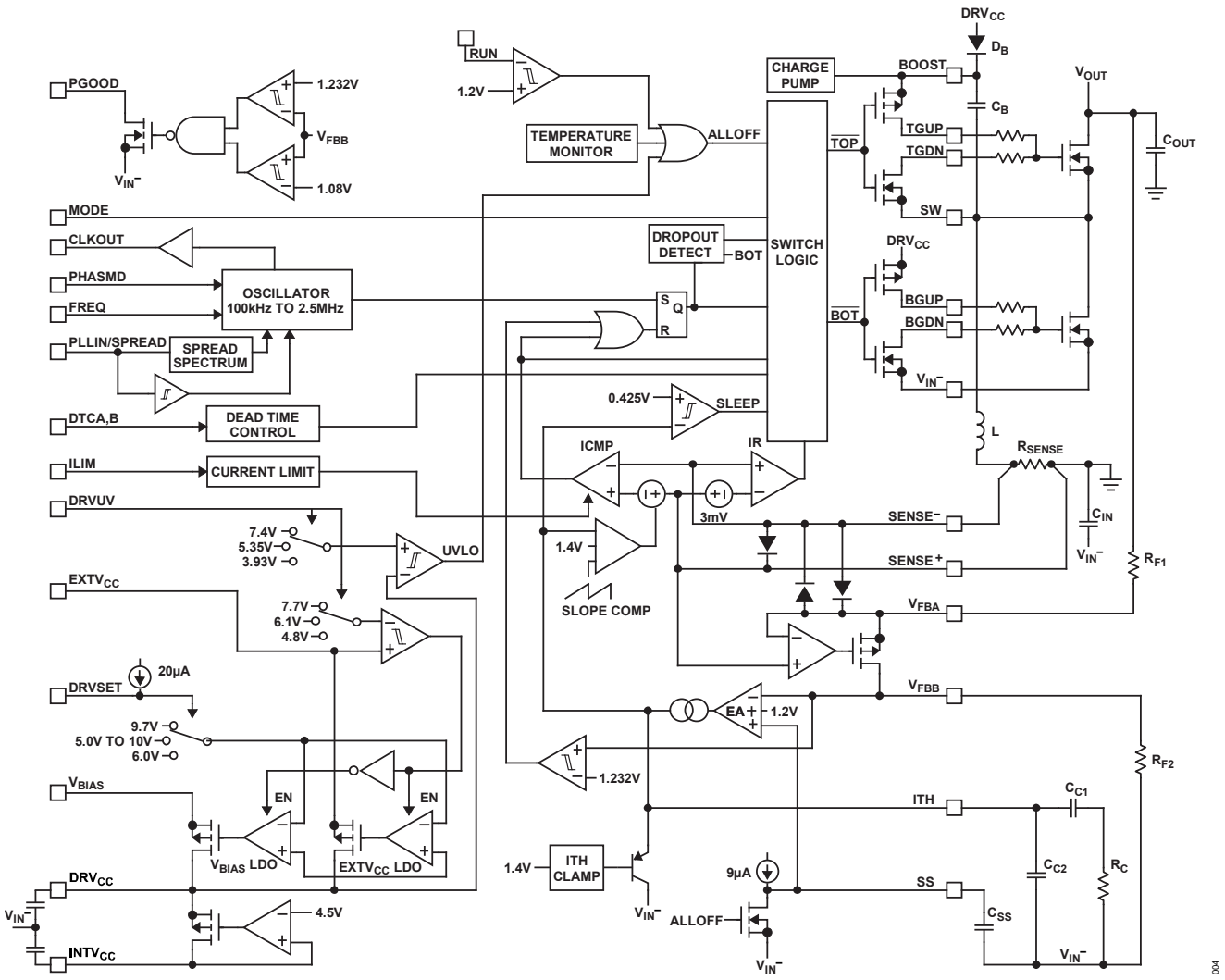


Figure 4. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

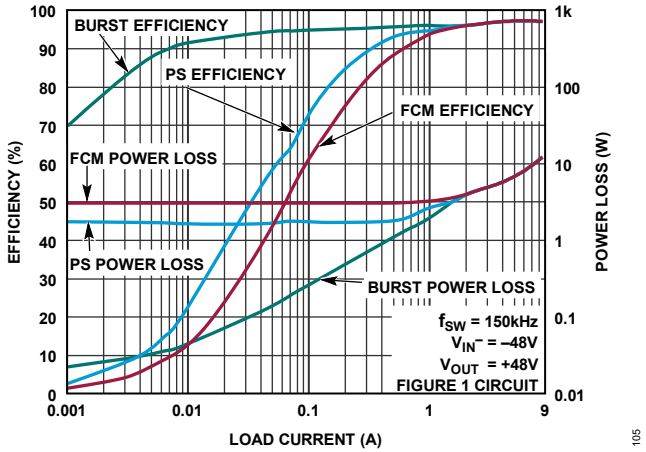


Figure 5. Efficiency and Power Loss vs. Load Current

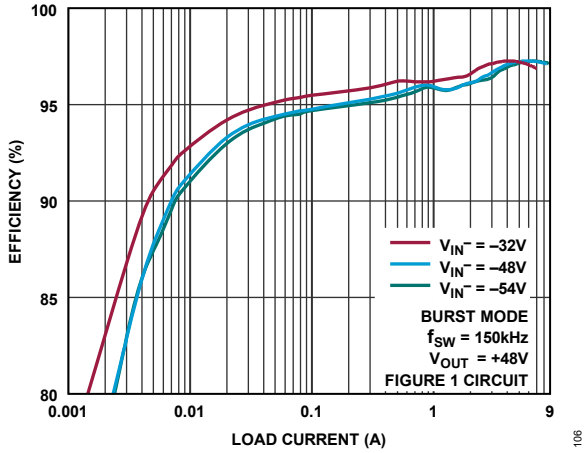


Figure 6. Efficiency vs. Load Current

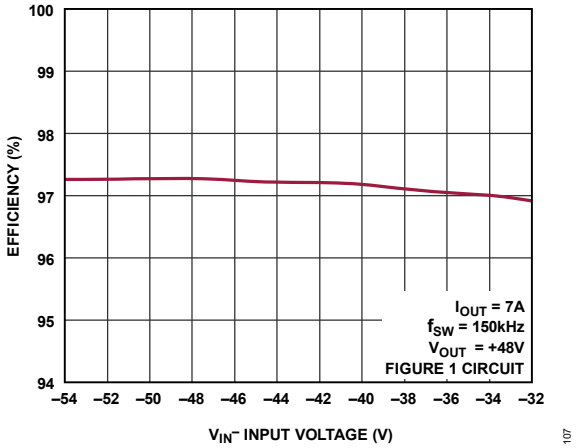


Figure 7. Efficiency vs. Input Voltage

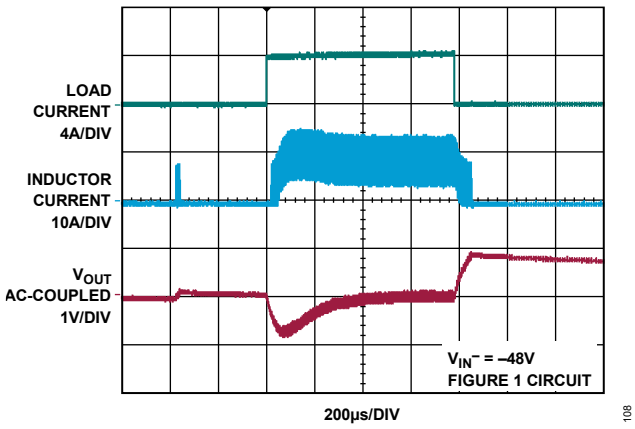


Figure 8. Load Step Burst Mode Operation

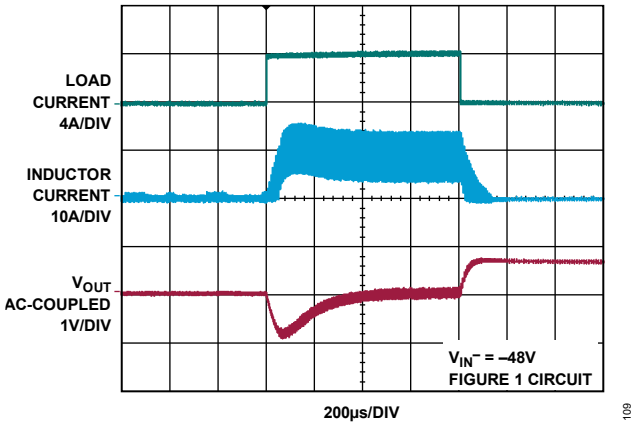


Figure 9. Load Step Pulse-Skipping Mode

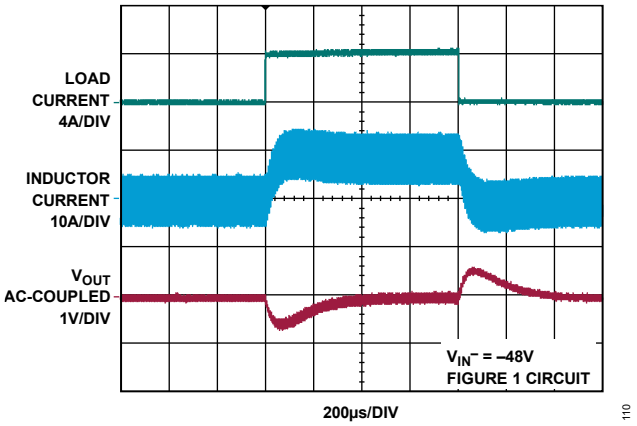


Figure 10. Load Step Forced Continuous Mode

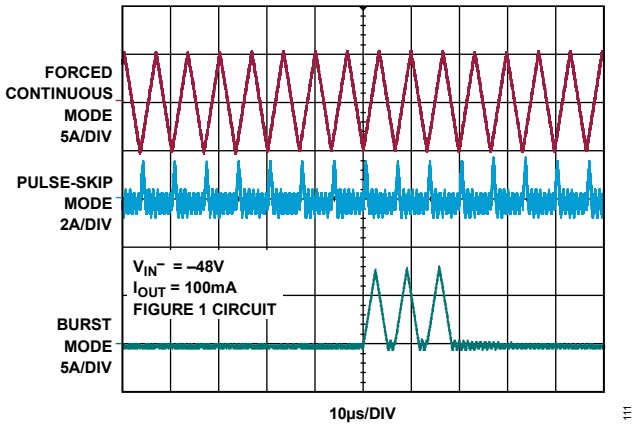


Figure 11. Inductor Current at Light Load

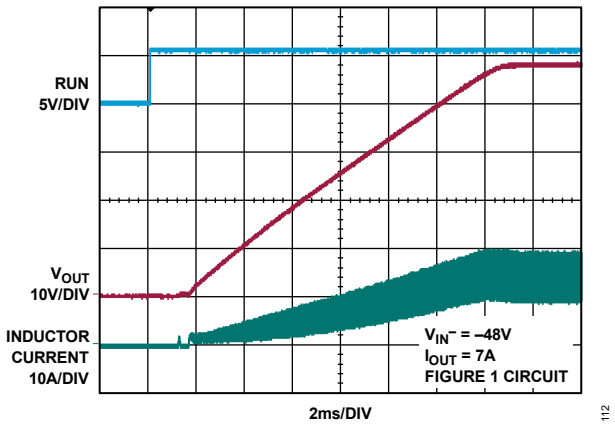


Figure 12. Soft Start-up

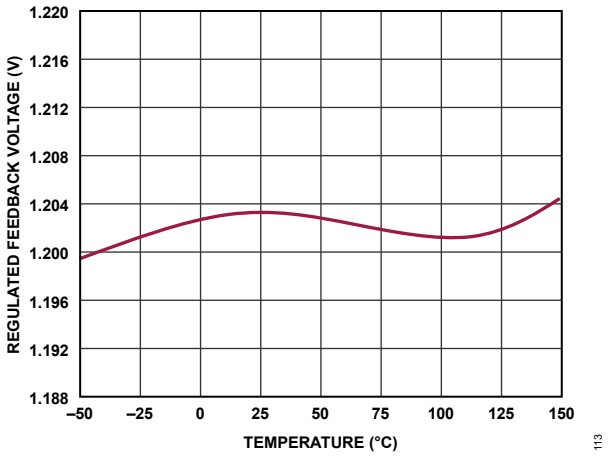


Figure 13. Regulated Feedback Voltage vs. Temperature

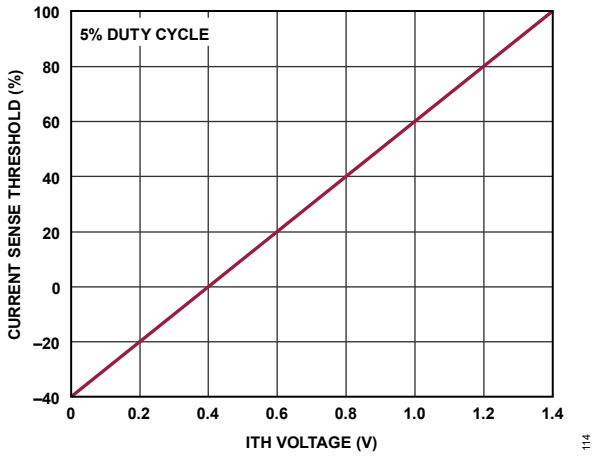


Figure 14. Maximum Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs. V_{ITH} in Forced Continuous Mode

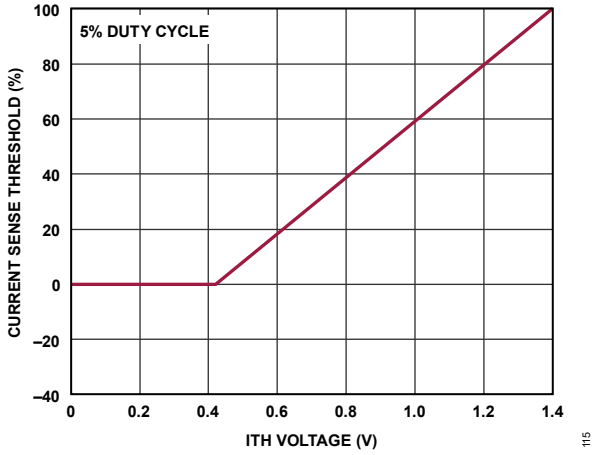


Figure 15. Maximum Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs. V_{ITH} in Pulse-Skipping Mode

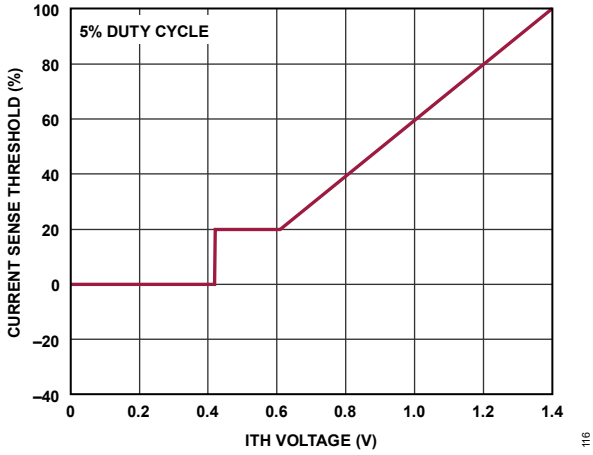


Figure 16. Maximum Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs. V_{ITH} in Burst Mode

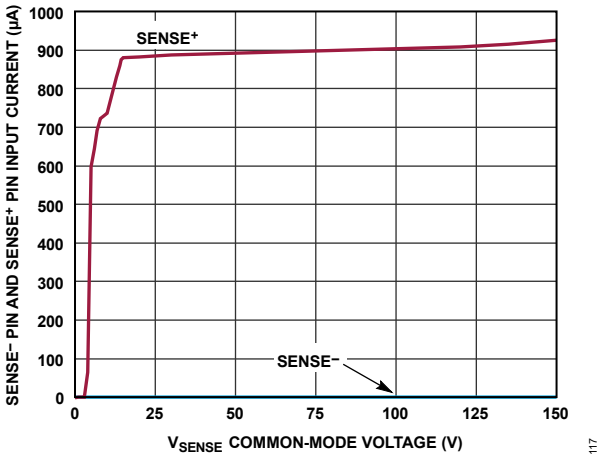


Figure 17. SENSE Input Current vs. V_{SENSE} Voltage

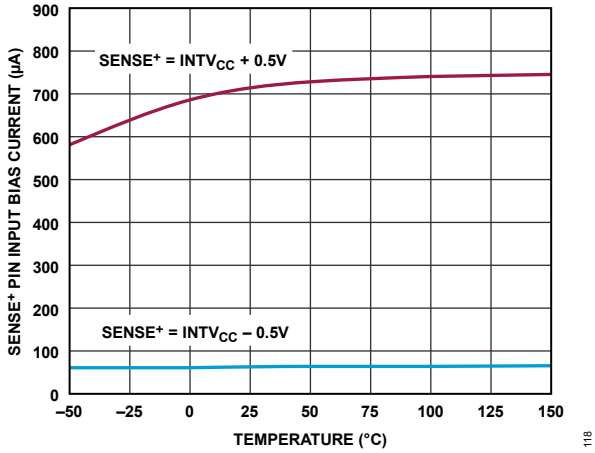


Figure 18. SENSE⁺ Input Current vs. Temperature

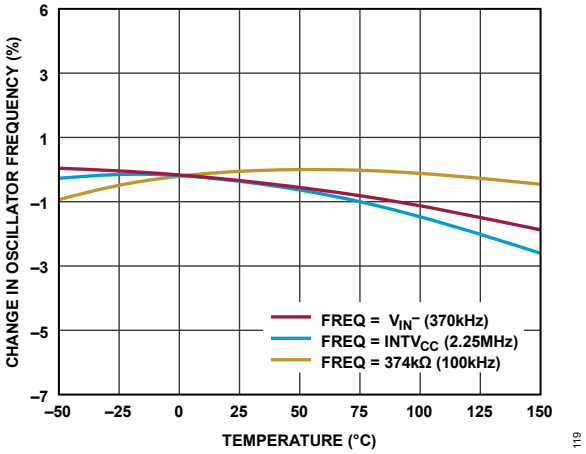


Figure 19. Oscillator Frequency vs. Temperature

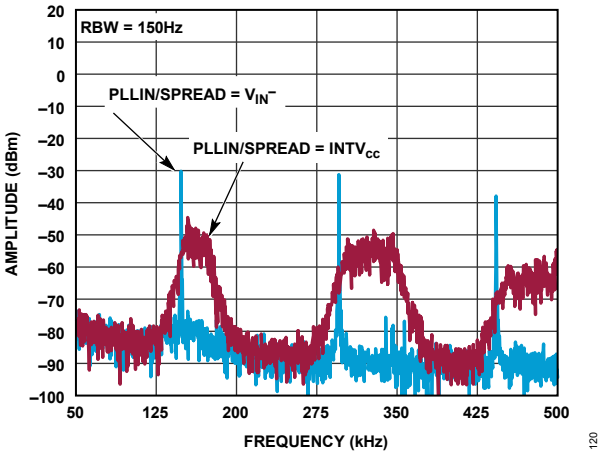


Figure 20. Output Voltage Noise Spectrum

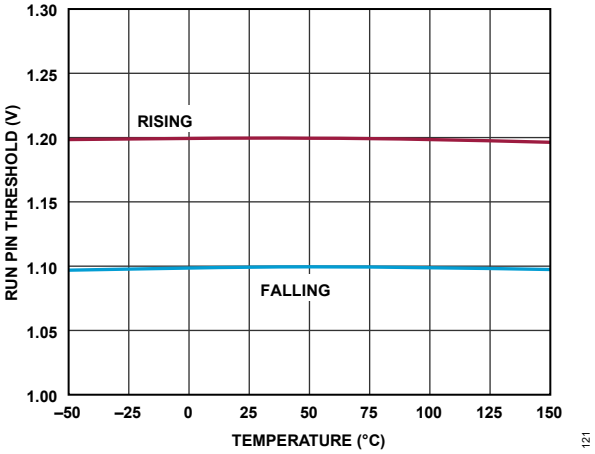


Figure 21. RUN Pin Thresholds vs. Temperature

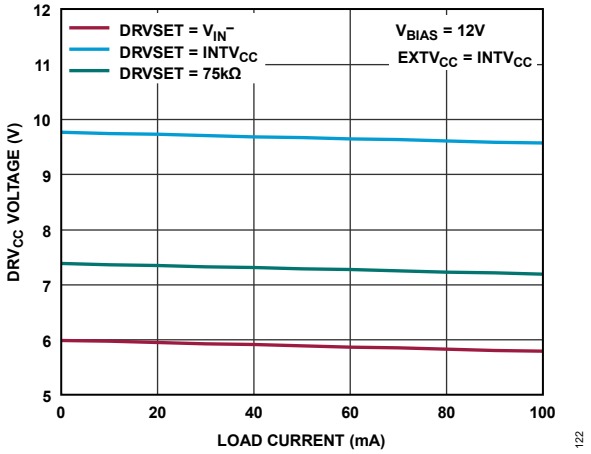


Figure 22. DRV_{CC} Voltage vs. Load Current

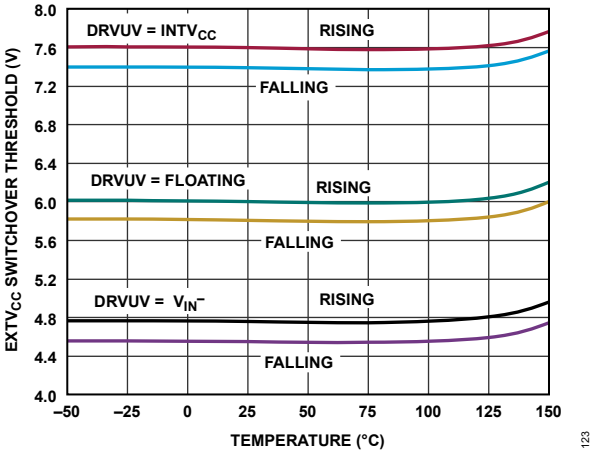


Figure 23. $EXTV_{CC}$ Switchover Voltage vs. Temperature

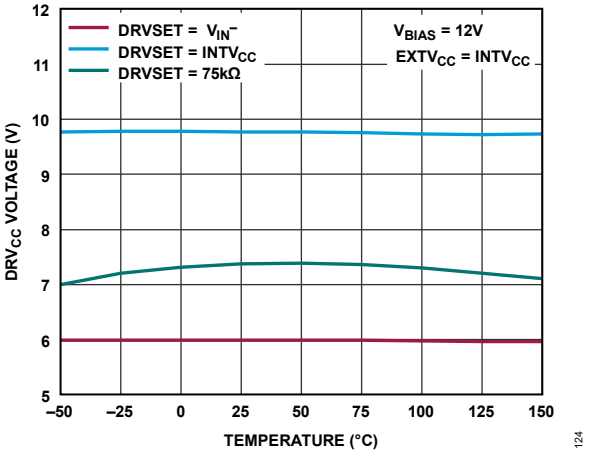


Figure 24. DRV_{CC} Voltage vs. Temperature

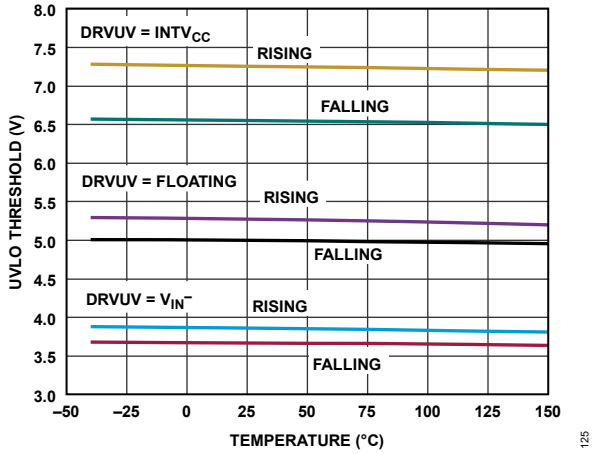


Figure 25. DRV_{CC} Undervoltage Lockout Thresholds vs. Temperature

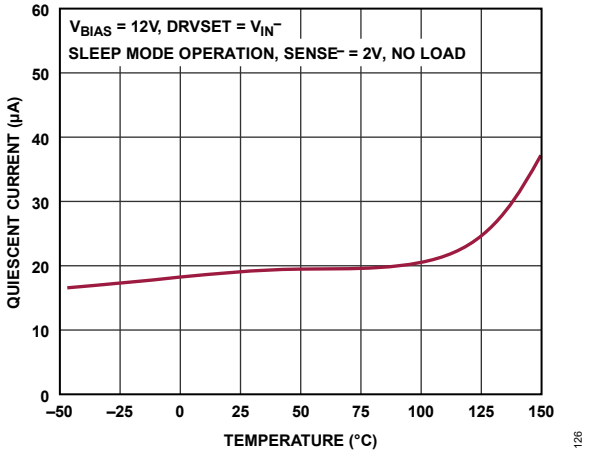


Figure 26. Quiescent Current vs. Temperature

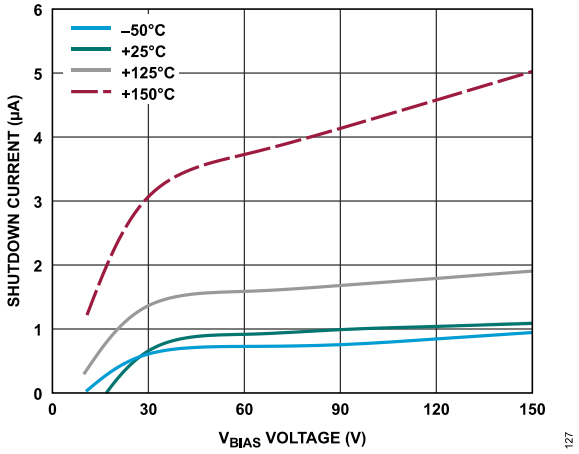


Figure 27. Shutdown Current vs. V_{BIAS} Voltage

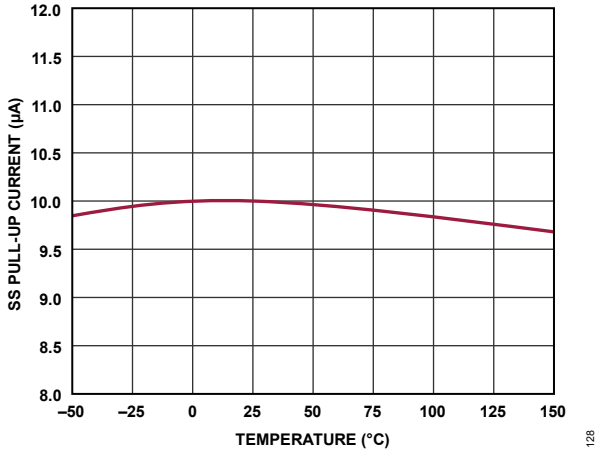


Figure 28. SS Pull-up Current vs. Temperature

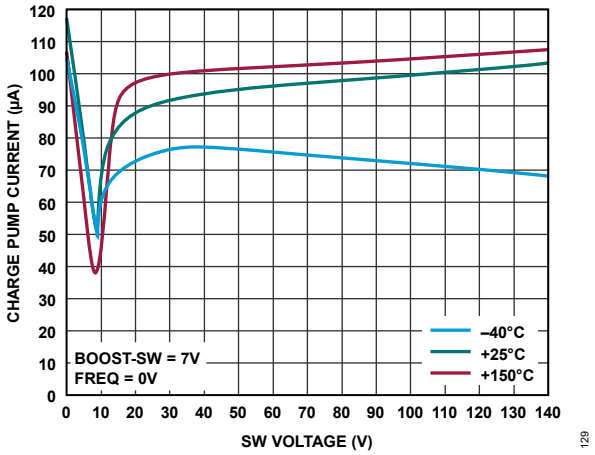


Figure 29. Charge Pump Output Current vs. SW Voltage

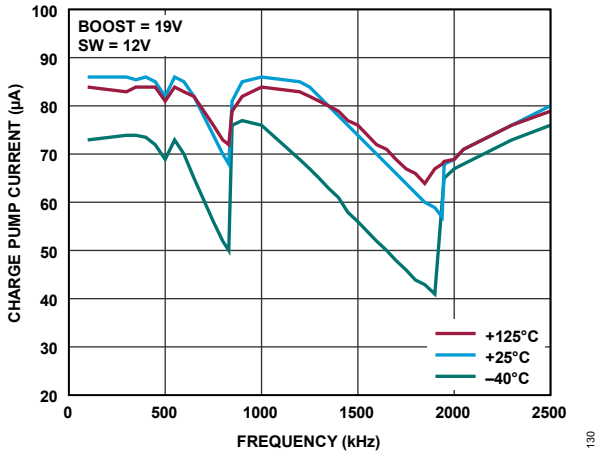


Figure 30. Charge Pump Output Current vs. Frequency

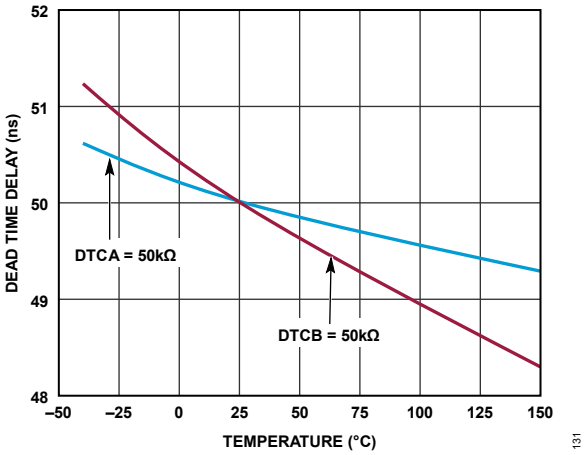


Figure 31. Dead Time Delay vs. Temperature

THEORY OF OPERATION

Main Control Loop

The LTC7899 is a synchronous controller utilizing a constant frequency, peak current mode architecture. During normal operation, the external bottom MOSFET turns on when the clock sets the RS latch, causing the inductor current to increase. The main switch turns off when the main current comparator, ICMP, resets the RS latch. After the bottom MOSFET is turned off each cycle, the top MOSFET turns on, which causes the inductor current to decrease until either the inductor current starts to reverse, as indicated by the current comparator (IR), or the beginning of the next clock cycle.

The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier (EA). The error amplifier compares the output voltage feedback signal at the V_{FBB} pin (which is generated with an external resistor connected to V_{IN}^-) to the internal 1.2V reference voltage. When the load current increases, it causes a slight decrease in V_{FBB} relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current meets the new load current.

After the bottom MOSFET is turned off each cycle, the top MOSFET turns on until either the inductor current starts to reverse, as indicated by the current comparator (IR), or the beginning of the next clock cycle.

Power and Bias Supplies (V_{BIAS}, $EXTV_{CC}$, DRV_{CC}, and $INTV_{CC}$)

Power for the top and bottom MOSFET drivers is derived from the DRV_{CC} pin. LDOs (low dropout linear regulators) are available from both the V_{BIAS} and $EXTV_{CC}$ pins to provide power to DRV_{CC}, which can be programmed from 5V to 10V through control of the DRVSET pin. When the $EXTV_{CC}$ pin is tied to a voltage below its switchover voltage, the V_{BIAS} LDO supplies power to DRV_{CC}. If $EXTV_{CC}$ is taken above its switchover voltage (4.8V, 6.1V or 7.7V depending on the DRVUV pin), the V_{BIAS} LDO is turned off and the $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies power to DRV_{CC}. Using the $EXTV_{CC}$ pin allows the DRV_{CC} power to be derived from a high efficiency external source.

The $INTV_{CC}$ supplies power for most of the internal circuits in the LTC7899. The $INTV_{CC}$ LDO regulates to a fixed value of 4.5V and its power is derived from the DRV_{CC} supply.

High-Side Bootstrap Capacitor

The top MOSFET driver is biased from the floating bootstrap capacitor (C_B), which normally recharges during each cycle through an external diode between BOOST and DRV_{CC} whenever the switch voltage goes low. The LTC7899 also has an internal charge pump that keeps the required bias on BOOST. The charge pump always operates in both forced continuous mode and pulse-skipping mode. In burst mode operation, the charge pump is turned off during sleep and enabled when the chip wakes up. The internal charge pump can nominally supply a charging current of 80µA.

If the input voltage GND to V_{IN}^- decreases to a voltage close to its output (V_{OUT}), the loop may enter dropout and attempt to turn on the top MOSFET continuously. In forced continuous mode or pulse-skipping mode, the internal charge pump enables the top MOSFET to be turned on continuously, resulting in a 100% duty cycle.

Dead Time Control (DTCA and DTCB Pins)

The LTC7899 dead time delays can be programmed from 13ns to 100ns through configuration of the DTCA and DTCB pins. The DTCA pin programs the dead time associated with the bottom MOSFET turning off (BG falling) and the top MOSFET turning on (TG rising). The DTCB pin programs the dead time associated with the top MOSFET turning off (TG falling) and the bottom MOSFET turning on (BG rising).

Tying the DTCx pin to V_{IN}^- or $INTV_{CC}$ programs adaptive dead time control, which means the driver logic waits for one MOSFET to turn off before deciding to turn on the other MOSFET. Adaptive dead time control results in dead times between BG/(TG) falling to TG/(BG) rising of approximately 80ns with DTCx = V_{IN}^- and 30ns with DTCx = $INTV_{CC}$. Placing a resistor between the DTC pin and V_{IN}^- programs the open-loop delay between one MOSFET turning off and the other turning on. This delay can be programmed between 13ns and 100ns. See the *Applications Information* section on dead time control for more information.

Start-Up and Shutdown (RUN and SS Pins)

The LTC7899 can be shut down using the RUN pin. Pulling the RUN pin below 1.1V shuts down the main control loop. Pulling the RUN pin below 0.7V disables the controller and most internal circuits, including the DRV_{CC} and $INTV_{CC}$ LDOs. In this shutdown state, the LTC7899 draws only 1µA of quiescent current.

The RUN pin needs to be externally pulled up or driven directly by logic. The RUN pin can tolerate up to 140V (absolute maximum), so it can be conveniently tied to V_{BIAS} in always-on applications where the controller is enabled continuously and never shut down. Additionally, a resistive divider between V_{BIAS} and V_{IN}^- with a tap to the RUN pin can be used to set a precise input undervoltage lockout so that the power supply does not operate below a user adjustable level.

The start-up of the output voltage V_{OUT} with respect to ground is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 1.2V internal reference voltage, the LTC7899 regulates the V_{FBB} voltage to the SS pin voltage instead of the 1.2V reference voltage. This allows the SS pin to be used as a soft-start, which smoothly ramps the output voltage on start-up. An external capacitor from the SS pin to V_{IN}^- is charged by an internal 9µA pull-up current, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.2V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value.

Light Load Operation: Burst Mode Operation, Pulse-Skipping Mode, or Forced Continuous Mode (MODE Pin)

The LTC7899 can be enabled to enter high efficiency burst mode operation, constant frequency pulse-skipping mode or forced continuous conduction mode at low load currents.

To select burst mode operation, tie the MODE pin to V_{IN}^-. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V. An internal 100k resistor to V_{IN}^- invokes burst mode operation when the MODE pin is floating and pulse-skipping mode when the MODE pin is tied to $INTV_{CC}$ through an external 100k resistor.

When the controller is enabled for burst mode operation, the minimum peak current in the inductor is set to approximately 25% of its maximum value, even though the voltage on the ITH pin may indicate a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, decreases the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.45V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC7899 draws to 15µA. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases with respect to ground, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the bottom MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for burst mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the top MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous operation or clocked by an external clock source to use the phase-locked loop, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in burst mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

When the MODE pin is connected for pulse-skipping mode, the LTC7899 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of the designed maximum output current. At light loads, the current comparator, ICMP, can remain tripped for several cycles and force the bottom MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference, as compared to burst mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as burst mode operation.

Unlike forced continuous mode and pulse-skipping mode, burst mode operation cannot be synchronized to an external clock. Therefore, if burst mode operation is selected and the switching frequency is synchronized to an external clock applied to the PLLIN/SPREAD pin, the LTC7899 switches from burst mode operation to forced continuous mode.

Frequency Selection, Spread Spectrum, and Phase-Locked Loop (FREQ and PLLIN/SPREAD Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The free running switching frequency of the LTC7899 controller is selected using the FREQ pin. If the PLLIN/SPREAD pin is not being driven by an external clock source, the FREQ pin can be tied to V_{IN}^-, tied to $INTV_{CC}$ or programmed through an external resistor. Tying FREQ to V_{IN}^- selects 370kHz, while tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and V_{IN}^- allows the frequency to be programmed between 100kHz and 2.5MHz.

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI, the LTC7899 can operate in spread spectrum mode, which is enabled by tying the PLLIN/SPREAD pin to $INTV_{CC}$. This feature varies the switching frequency within typical boundaries of the frequency set by the FREQ pin and +20%.

A phase-locked loop (PLL) is available on the LTC7899 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. The LTC7899's PLL aligns the turn-on of the controllers external bottom MOSFET to the rising edge of the synchronizing signal.

The PLL frequency is prebiased to the free running frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL only needs to make slight changes to synchronize the rising edge of the external clock to the rising edge of BG. For more rapid lock-in to the external clock, use the FREQ pin to set the internal oscillator to approximately the frequency of the external clock. The LTC7899's PLL is guaranteed to lock to an external clock source whose frequency is between 100kHz and 2.5MHz.

The PLLIN/SPREAD pin is TTL compatible with thresholds of 1.6V (rising) and 1.1V (falling) and is guaranteed to operate with a clock signal swing of 0.5V to 2.2V.

PolyPhase Applications (CLKOUT and PHASMD Pins)

The LTC7899 features two pins (CLKOUT and PHASMD) that allow other controller ICs to be daisy-chained with the LTC7899 in PolyPhase applications. The clock output signal on the CLKOUT pin can be used to synchronize additional power stages in a multiphase power supply solution feeding a single, high current output or multiple separate outputs. The PHASMD pin is used to adjust the phase of the CLKOUT signal. Pulling this pin to V_{IN}^- forces CLKOUT to be out-of-phase 90° with respect to BG. Connecting this pin to $INTV_{CC}$ forces CLKOUT to be out-of-phase 120° with respect to BG. Floating this pin forces CLKOUT to be out-of-phase 180° with respect to BG.

Output Overvoltage Protection

An overvoltage comparator that guards against transient overshoots as well as other more serious conditions that can overvoltage the output. When the V_{FBB} pin rises more than 10% above its regulation point of 1.2V, the top MOSFET turns off and the inductor current is not allowed to reverse.

Operation at Low Input Voltage

The LTC7899 features a rail-to-rail current comparator, which functions down to zero volts with respect to V_{IN}^-. The minimum converter input voltage ($|V_{IN}^-|$) is therefore determined by the practical limitations of the converter architecture.

BOOST Supply Refresh

The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each cycle through an external diode when the bottom MOSFET turns on. During start-up, if the bottom MOSFET is not turned on within 100µs after UVLO goes low, the bottom MOSFET will be forced to turn on for a cumulative on time of ~400ns. This forced refresh generates enough BOOST-SW voltage to allow the top MOSFET to be fully enhanced instead of waiting for the initial few cycles to charge the bootstrap capacitor, C_B.

Power Good

The controller has a PGOOD pin that is connected to an open-drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{FBB} voltage is not within ±10% of the 1.2V reference. The PGOOD pin is also pulled low when the RUN pin is low (shutdown). When the V_{FBB} voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V, such as $INTV_{CC}$.

APPLICATIONS INFORMATION

The typical application on the first page is a basic LTC7899 application circuit. External component selection is largely driven by the load requirement and begins with the selection of the inductor, current sense components, operating frequency, and light load operating mode. The remaining power stage components, consisting of the input and output capacitors, and power MOSFETs can then be chosen. Next, feedback resistors are selected to set the desired output voltage. Then, the remaining external components are selected, such as for soft-start, biasing, and loop compensation.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So, why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on the ripple current and low current operation must also be considered. The inductor value has a direct effect on the ripple current.

The maximum average inductor current in continuous conduction is equal to the maximum average output current multiplied by a factor ($1 + V_{OUT}/|V_{IN}^-|$) or $I_{OUT(MAX)} = I_{L(MAX)} \bullet |V_{IN}^-|/(V_{OUT} + |V_{IN}^-|)$, where V_{OUT} is referenced to ground. Be aware that the maximum output current from this regulator decreases with decreasing $|V_{IN}^-|$. The choice of $I_{L(MAX)}$ therefore depends on the maximum load current for a regulated V_{OUT} at the minimum normal operating $|V_{IN}^-|$. If the load current for a given $|V_{IN}^-|$ is exceeded, V_{OUT} will decrease until the $I_{OUT(MAX)} = I_{L(MAX)} \bullet |V_{IN}^-|/(V_{OUT} + |V_{IN}^-|)$ equation is satisfied.

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \bullet I_{L(MAX)}$. The maximum ΔI_L occurs at $|V_{IN}^-| = V_{OUT}$ given by Equation 1, as follows:

$$\Delta I_L = \frac{|V_{IN-}|}{(f)(L)}\left(\frac{V_{OUT}}{V_{OUT}+|V_{IN-}|}\right) \quad (1)$$

The inductor value also has secondary effects. The transition to burst mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) cause this transition to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In burst mode operation, lower inductance values cause the burst frequency to decrease.

Inductor Core Selection

When the value for L is known, select the type of inductor. High efficiency regulators generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. The actual core loss is independent of core size for a fixed inductor value, but it is dependent on the inductance value selected. As inductance increases, core losses decrease. However, because increased inductance requires more turns of wire, copper losses increase.

Ferrite designs have low core loss and are preferred for high switching frequencies. Therefore, design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This collapse results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate. The inductor saturation design margin should account for the tolerance and temperature effects of the saturation current.

Current Sense Selection

The LTC7899 can be configured to use either inductor DC resistance (DCR) sensing or low value resistor sensing. The choice between the two current sensing schemes is a design trade-off between cost, power consumption, and accuracy. DCR sensing is popular because it saves expensive current sensing resistors and is more power efficient, particularly in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. The selection of other external components is driven by the load requirement and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and the inductor value.

The SENSE$^+$ and SENSE$^-$ pins are the inputs to the current comparator. The common mode voltage range on these pins is 0V to 140V (absolute maximum), enabling the LTC7899 to operate with a wide input voltage range up to a maximum of 135V. The SENSE$^-$ pin is high impedance, drawing less than ≈1µA. This high impedance allows the current comparator to be used in inductor DCR sensing. The impedance of the SENSE$^+$ pin changes depending on the common mode voltage. When less than $INTV_{CC}$ – 0.5V, the SENSE$^+$ pin is relatively high impedance, drawing ≈1µA. When the SENSE$^+$ pin is above $INTV_{CC}$ + 0.5V, a higher current (≈700µA) flows into the pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current. The SENSE$^+$ pin has an additional ≈70µA current when its voltage is above 3.2V to bias internal circuitry from V_{BIAS}.

Filter components mutual to the sense lines must be placed close to the LTC7899, and the sense lines must run close together to a Kelvin connection underneath the current sense element (shown in *Figure 32*). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (*Figure 34*), the R1 resistor must be placed close to the switching node to prevent noise from coupling into sensitive small signal nodes.

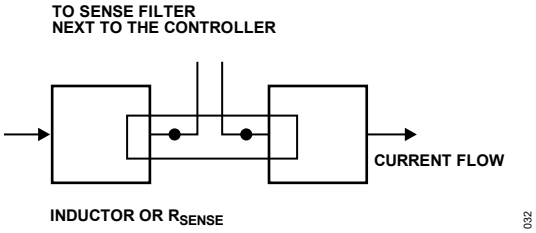


Figure 32. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

Figure 33 shows a typical sensing circuit using a discrete resistor. R_{SENSE} is chosen based on the required output current. The current comparator of the controller has a $V_{SENSE(MAX)}$ of 25mV, 50mV, or 75mV, as determined by the state of the ILIM pin. The current comparator threshold voltage sets the peak inductor current.

Using the maximum inductor current ($I_{L(MAX)}$) and ripple current (ΔI_L) (as described in the *Inductor Value Calculation* section), the target sense resistor value is given by Equation 2, as follows:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (2)$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the *Table 1*.

The parasitic inductance (ESL) of the sense resistor introduces significant error in the current sense signal for lower inductor value (3µH) or higher current (5A) applications. This error is proportional to the input voltage and can degrade line regulation or cause loop instability. Placing an RC filter (R_F) into the sense pins, as shown in *Figure 33*, can be used to compensate for this error. For optimal cancellation of the ESL, set the RC filter time constant to $R_F \times C_F = ESL/R_{SENSE}$ (C_F is the filter capacitor). In general, select C_F to be in the range of 1nF to 10nF and calculate the corresponding R_F. Surface-mount sense resistors in low ESL, wide footprint geometries are recommended to minimize this error. If not specified in the data sheet of the manufacturer, the ESL can be approximated as 0.4nH for a resistor with a 1206 footprint, and 0.2nH for a resistor with a 1225 footprint.

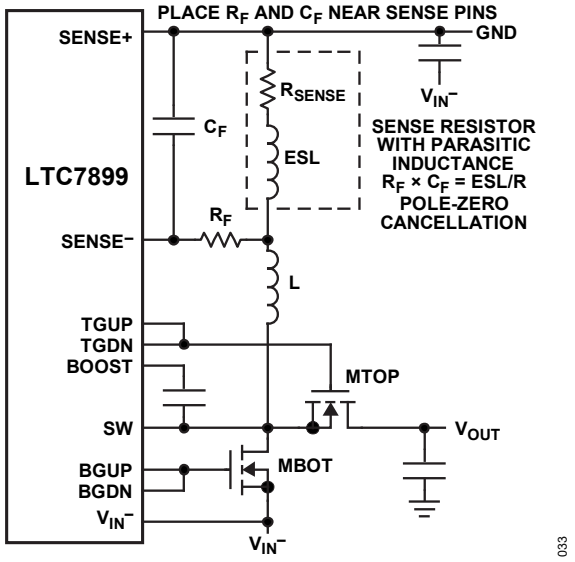


Figure 33. Current Sensing Methods-Using a Resistor to Sense Current

Inductor DCR Current Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7899 is capable of sensing the voltage drop across the inductor DCR, as shown in *Figure 34.* The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor costs several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2) × C1 time constant is chosen to be equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. The DCR can be measured using an inductance, capacitance, and resistance (LCR) meter. However, the DCR tolerance is not always the same and varies with temperature. Consult the data sheet of the manufacturer for detailed information.

Using $I_{L(MAX)}$ and ΔI_L (as described in the *Inductor Value Calculation* section), the target sense resistor value is given by Equation 3, as follows:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (3)$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in *Table 1*.

Next, determine the DCR of the inductor. When provided, use the maximum value noted by the manufacturer, typically given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for the maximum inductor temperature ($T_{L(MAX)}$) is 100°C. To scale the maximum inductor DCR (DCR_{MAX}) to the desired sense resistor (R_D) value, use the divider ratio given by Equation 4, as follows:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}} \quad (4)$$

C1 is typically selected to be in the range of 0.1µF to 0.47µF. This range forces the equivalent resistance (R1||R2) to around 2kΩ, reducing the error that can result from the ≈1µA current of $SENSE^+$ pin.

R1||R2 is scaled to the room temperature inductance and the maximum DCR given by Equation 5, as follows:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \cdot C1} \quad (5)$$

The sense resistor values are given by Equation 6 and Equation 7, as follows:

$$R1 = \frac{R1||R2}{R_D} \quad (6)$$

$$R2 = \frac{R1 \cdot R_D}{1 - R_D} \quad (7)$$

The maximum power loss (P_{LOSS}) in R1 is related to duty cycle and occurs in continuous mode at $|V_{IN}^-| = V_{OUT}$ given by Equation 8, as follows:

$$P_{LOSS} \text{ in } R1 = \frac{|V_{IN}-| \cdot V_{OUT}}{R1} \quad (8)$$

Ensure that R1 has a power rating higher than P_{LOSS} in R1. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses, and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

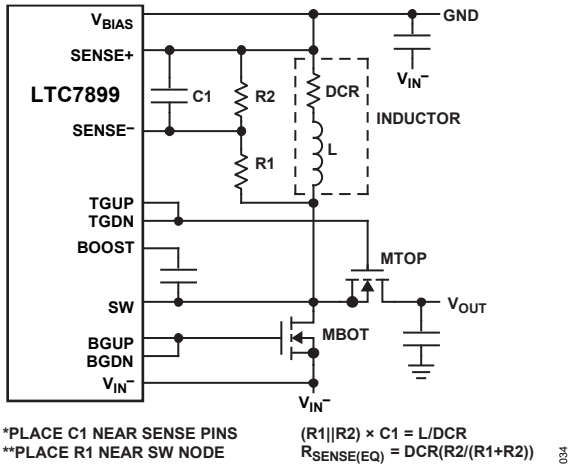


Figure 34. Current Sensing Methods-Using the Inductor DCR to Sense Current

Setting the Operating Frequency

Selecting the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing gate charge and transition losses, but requires larger inductance values and/or more output capacitance to maintain low output ripple voltage.

In higher voltage applications, transition losses contribute more significantly to power loss, and a proper balance between size and efficiency is achieved with a switching frequency between 300kHz and 900kHz. Lower voltage applications benefit from lower switching losses, and can operate at switching frequencies up to 2.5MHz, if desired. The switching frequency is set using the FREQ and PLLIN/SPREAD pins, as shown in *Table 4*.

Table 4. Setting the Switching Frequency Using FREQ and PLLIN/SPREAD

FREQ PIN	PLLIN/SPREAD PIN	FREQUENCY
V_{IN}^-	V_{IN}^-	370kHz
$INTV_{CC}$	V_{IN}^-	2.25MHz
Resistor to V_{IN}^-	V_{IN}^-	100kHz to 2.5MHz
Any of the above	External Clock 100kHz to 2.5MHz	Phase-Locked to External lock
Any of the above	$INTV_{CC}$	Spread Spectrum f_{OSC} Modulated 0% to +20%

Tying the FREQ pin to V_{IN}^- selects 370kHz, whereas tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and V_{IN}^- allows the frequency to be programmed anywhere between 100kHz and 2.5MHz. Choose a FREQ pin resistor (R_{FREQ}) from *Figure 35* or equation 9, as follows:

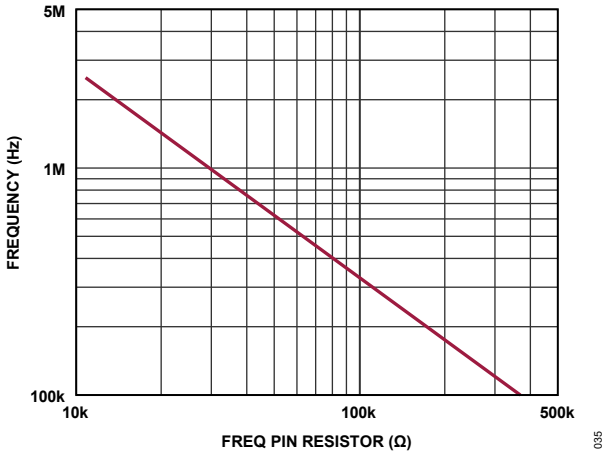


Figure 35. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{f_{osc}} \quad (9)$$

A further constraint on the operating frequency is due to the maximum duty cycle of the converter. The maximum duty cycle, which can be approximated as $DC_{MAX} = V_{OUT}/(V_{OUT}+|V_{IN(MIN)}^-|) \bullet 100\%$ where V_{OUT} is referenced to ground, is limited as shown in *Figure 36*. At low frequencies, the output will lose regulation if the required duty cycle is higher than 93%. At high frequencies, the maximum duty cycle available to maintain constant frequency operation is reduced further. In this region, if a higher duty cycle is required to keep the output voltage in regulation, the controller will skip the top MOSFET (TG) turn-on and keep the bottom MOSFET (BG) on for more than one clock cycle

to achieve the higher duty cycle at an effectively lower frequency. Choose a frequency that limits the maximum duty cycle to a value lower than the curve shown in *Figure 36*.

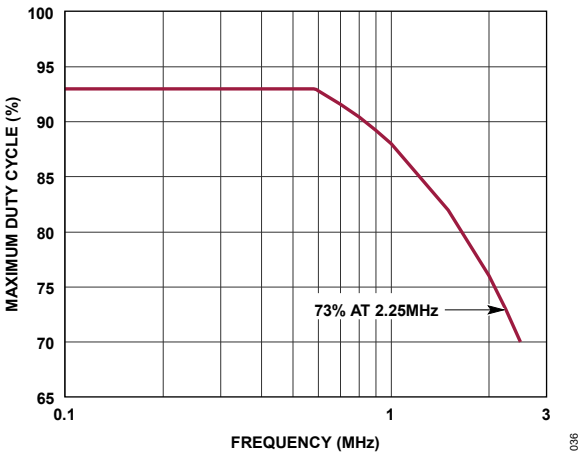


Figure 36. Relationship between Maximum Duty Cycle and Operating Frequency

To improve EMI performance, spread spectrum mode can be selected by tying the PLLIN/SPREAD pin to $INTV_{CC}$. When spread spectrum mode is enabled, the switching frequency modulates within the frequency selected by the FREQ pin and +20%. Spread spectrum mode can be used in any operating mode selected by the MODE pin (burst mode, pulse-skipping mode, or forced continuous mode).

A PLL is also available on the LTC7899 to synchronize the internal oscillator to an external clock source connected to the PLLIN/ SPREAD pin. After the PLL locks, BGxx is synchronized to the rising edge of the external clock signal. See the *Phase-Locked Loop and Frequency Synchronization* section for details.

Selecting the Light Load Operating Mode

The LTC7899 can be set to enter high efficiency burst mode operation, constant frequency pulse-skipping mode or forced continuous conduction mode at light load currents. To select burst mode operation, tie the MODE pin to V_{IN}^-. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to $INTV_{CC}$ through a 100k resistor. An internal 100k resistor from the MODE pin to V_{IN}^- selects burst mode if the pin is floating. When synchronized to an external clock through the PLLIN/SPREAD pin, the LTC7899 operates in pulse-skipping mode if it is selected, or in forced continuous mode otherwise. *Table 5* summarizes the use of the MODE pin to select the light load operating mode.

Table 5. Using the MODE Pin to Select Light Load Operating Mode

MODE PIN	LIGHT LOAD OPERATING MODE	MODE WHEN SYNCHRONIZED
V_{IN}^- or Floating	Burst Mode	Forced Continuous
100k to $INTV_{CC}$	Pulse-Skipping	Pulse-Skipping
$INTV_{CC}$	Forced Continuous	Forced Continuous

In general, the requirements of each application will dictate the appropriate choice for light load operating mode. In burst mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the top MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the regulator operates in discontinuous operation. In addition, when the load current is very light, the inductor current will begin bursting at frequencies lower than the switching frequency and enter a low current sleep mode when not switching. As a result, burst mode operation has the highest possible efficiency at light load.

In forced continuous mode, the inductor current is allowed to reverse at light loads and switches at the same frequency regardless of load. In this mode, the efficiency at light loads is considerably lower than in burst mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

In pulse-skipping mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the PWM comparator can remain tripped for several cycles and force the bottom MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to burst mode operation. It provides higher light load efficiency than forced continuous mode, but not nearly as high as burst mode operation. Consequently, pulse-skipping mode represents a compromise between light load efficiency, output ripple, and EMI.

In some applications, it may be desirable to change light load operating mode based on the conditions present in the system. For example, if a system is inactive, the user can select high efficiency burst mode operation by keeping the MODE pin set to V_{IN}^-. When the system wakes, the user can send an external clock to PLLIN/SPREAD, or tie MODE to $INTV_{CC}$ to switch to low noise forced continuous mode. These on-the-fly mode changes can allow an individual application to benefit from the advantages of each light load operating mode.

Dead Time Control (DTCA and DTCB Pins)

The dead time delays of the LTC7899 can be adjusted from 13ns to 100ns by configuring the DTCA pin and DTCB pin. See *Figure 37* and *Figure 38*, which show the TG minus SW, BG, and SW waveforms for each DTCx pin setting. In the DTCx pins tied to V_{IN}^- (Adaptive Dead Time Control), DTCx pins tied to $INTV_{CC}$, and DTCx pins connected with a resistor to V_{IN}^- sections, TG represents the voltage sensed at the top MOSFET gate (the threshold for TG falling is sensed at the TGUP pin), and BG represents the voltage sensed at the bottom MOSFET gate (the thresholds for BG rising and falling are sensed at the BGDN and BGUP pins, respectively). The SW waveforms represent operation in continuous conduction mode with positive inductor current. The DTCA pin programs the dead time associated with the bottom MOSFET turning off and the top MOSFET turning on (SW transitioning from low to high). The DTCB pin programs the dead time associated with top MOSFET turning off and the bottom MOSFET turning on (SW transitioning from high to low).

DTCx Pins Tied to $INTV_{CC}$ or V_{IN}^- (Adaptive Dead Time Control)

Adaptive dead time control is programmed by tying the DTCx pin to $INTV_{CC}$ or V_{IN}^-. In adaptive control (*Figure 37*), the driver logic waits for one MOSFET to turn off (~1.5V falling threshold on the BGUP/TGUP pins) before turning on the other MOSFET. Tying the DTCA pin to $INTV_{CC}$ programs an adaptive delay between BG going low and TG-SW going high to approximately 30ns. Tying the DTCA pin to V_{IN}^- programs an adaptive delay between BG going low and TG-SW going high to approximately 80ns. Tying the DTCB pin to $INTV_{CC}$ programs an adaptive delay between TG-SW going low and BG going high to approximately 30ns. Tying the DTCB pin to V_{IN}^- programs an adaptive delay between TG-SW going low and BG going high to approximately 80ns.

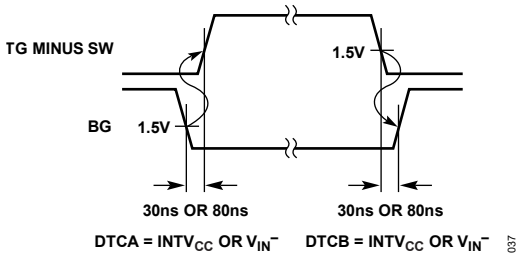


Figure 37. DTCx Pin Tied to $INTV_{CC}$ or V_{IN}^-–Adaptive Dead Time Control

DTCx pin connected with a resistor to V_{IN}^-:

Connecting a resistor between the DTCx pins and V_{IN}^- programs an additional delay from 13ns to 100ns between the TG and BG edges (see *Figure 38*). A resistor tied to the DTCA pin inserts additional delay between BG falling and TG rising.

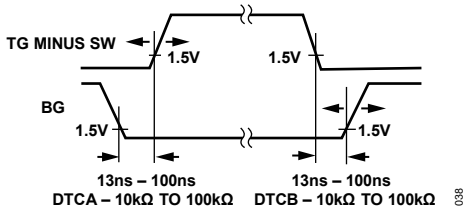


Figure 38. DTCx Pin with Resistor to V_{IN}^-–Adjustable Dead Time Control

A resistor tied to the DTCB pin to V_{IN}^- inserts additional delay between TG falling and BG rising. *Figure 39* shows the relationship between the DTCx pin resistor value and the programmed delay between BG and TG edges. This resistor must not be less than 10kΩ.

With a resistor on the DTCx pins, the maximum delay between one MOSFET turning off and the other MOSFET turning on is set to approximately 60ns beyond the programmed delay time. For the DTCA transition (SW from low to high), this timeout can be reached if the bottom MOSFET turns off with negative inductor current (for example, light load currents in forced continuous mode), such that SW slews high immediately after the bottom MOSFET turns off.

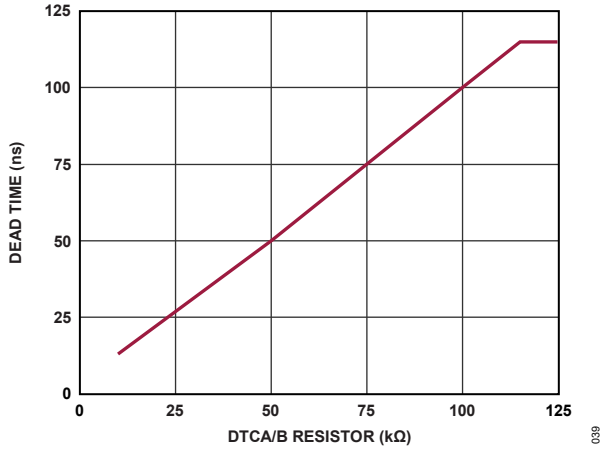


Figure 39. Relationship between Dead Time Delay and Resistor Value at DTCx Pins

Setting wide dead times can be useful in applications where the MOSFETs are not well defined and an extra safety margin is required to prevent shoot-through.

Power MOSFET Selection

Two external power MOSFETs must be selected for the LTC7899: one N-channel MOSFET for the bottom (main) switch and one N-channel MOSFET for the top (synchronous) switch. The peak-to-peak drive levels are set by the DRV_{CC} regulation point (5V to 10V). Therefore, both logic-level and standard-level threshold MOSFETs can be used in most applications depending on the programmed DRV_{CC} voltage. Pay close attention to the breakdown voltage (BVD_{SS}) specification for the MOSFETs as well. The BVD_{SS} of the MOSFETs must be greater than $V_{OUT}+|V_{IN(MIN)}^-|$.

The LTC7899's ability to adjust the gate drive level between 5V to 10V (OPTI-DRIVE) allows an application circuit to be precisely optimized for efficiency. When adjusting the gate drive level, the final arbiter is the total input current

for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Selection criteria for the power MOSFETs include the on resistance ($R_{DS(ON)}$), miller capacitance (C_{MILLER}), input voltage, and maximum output current. C_{MILLER} can be approximated from the gate charge curve typically provided in the data sheet of the MOSFET manufacturer. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat, divided by the specified change in the voltage difference between the drain and source terminals of the MOSFET (V_{DS}). This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode, the duty cycles for the top and bottom FETs are given by Equation 10 and Equation 11, as follows:

$$\text{MAIN SWITCH DUTY CYCLE} = \frac{V_{OUT}}{|V_{IN}^-|+V_{OUT}} \tag{10}$$

$$\text{SYNCHRONOUS SWITCH DUTY CYCLE} = \frac{|V_{IN}^-|}{|V_{IN}^-|+V_{OUT}} \tag{11}$$

The MOSFET power dissipations at maximum output current are given by Equation 12 and Equation 13, as follows:

$$P_{MAIN} = \frac{(|V_{IN}^-|+V_{OUT})V_{OUT}}{|V_{IN}^-|^2}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)} + \left(\frac{(|V_{IN}^-|+V_{OUT})^3}{|V_{IN}^-|}\right)\left(\frac{I_{OUT(MAX)}}{2}\right)(R_{DR})(C_{MILLER}) \cdot \left[\frac{1}{V_{DRVCC}-V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f) \tag{12}$$

$$P_{SYNC} = \frac{|V_{IN}^-|+V_{OUT}}{|V_{IN}^-|}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)} \tag{13}$$

where:

P_{MAIN} is the power dissipation from the main switch.

V_{DRVCC} is the DRV_{CC} voltage.

P_{SYNC} is the power dissipation from the synchronous switch.

δ is the temperature dependency of $R_{DS(ON)}$ ($\delta \approx 0.005/°C$).

R_{DR} is the effective driver resistance at the Miller threshold voltage of the MOSFET ($R_{DR} \approx 2\ \Omega$).

V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses (I^2R is the power loss equation of the MOSFETs), whereas the main N-channel equations include an additional term for transition losses, which are highest at low input voltages. For high V_{IN} the high current efficiency generally improves with larger MOSFETs, while for low V_{IN} the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} provides higher efficiency. The synchronous MOSFET losses are greatest at low $|V_{IN}^-|$ voltage when the bottom switch duty factor is low.

C_{IN} and C_{OUT} Selection

The input ripple current in this type of converter is relatively low (compared to the output ripple current) because this current is continuous. The input capacitor C_{IN} voltage rating should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

The output current in this type of converter is discontinuous, so C_{OUT} should be selected to meet output voltage ripple requirements. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The ripple due to charging and discharging the bulk capacitance of C_{OUT} is given by Equation 14.:

$$V_{RIPPLE} = \frac{I_{OUT(MAX)} \cdot V_{OUT}}{C_{OUT} \cdot (|V_{IN(MIN)}^{-}| + V_{OUT}) \cdot f} \quad (14)$$

The ripple due to the voltage drop across the ESR is given by Equation 15.

$$\Delta V_{ESR} = \left(I_{L(MAX)} + \frac{1}{2}\Delta I_L\right) \bullet ESR \quad (15)$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings such as OS-CON and POSCAP.

Setting the Output Voltage

The LTC7899 output voltages are each set by external resistors carefully placed across the output and the V_{FBA} and V_{FBB} pins, as shown in *Figure 40*. The regulated output voltage is determined by Equation 16.

$$V_{OUT} = 1.2V\left(\frac{R_A}{R_B}\right) \quad (16)$$

Place resistors R_A and R_B very close to the V_{FBA} and V_{FBB} pins to minimize PCB trace length and noise on the sensitive V_{FB} nodes. Great care should be taken to route the V_{FBX} traces away from noise sources, such as the inductor or the SW trace. To improve frequency response, a feedforward capacitor (C_{FF}) can be used.

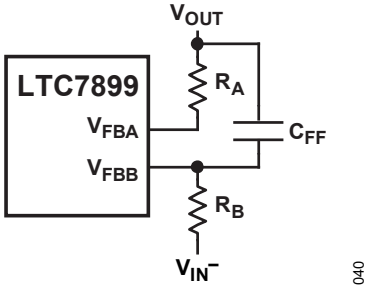


Figure 40. Setting the Output Voltage

RUN Pin and Undervoltage Lockout

The LTC7899 is enabled using the RUN pin. The RUN pin has a rising threshold of 1.2V with 100mV of hysteresis. Pulling the RUN pin below 1.1V shuts down the main control loop and resets the soft-start. Pulling the RUN pin below 0.7V disables the controller and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC7899 draws only ≈1µA of quiescent current.

The RUN pin is high impedance and must be externally pulled up/down or driven directly by logic. The RUN pin can tolerate up to 140V (absolute maximum), so it can be conveniently tied to GND (V_{BIAS}) in always-on applications where the controller is enabled continuously and never shut down. Do not float the RUN pin.

The RUN pin can also be configured as precise undervoltage lockouts (UVLOs) on the input supply with a resistor divider from V_{BIAS} to V_{IN}^{-}, as shown in *Figure 41*.

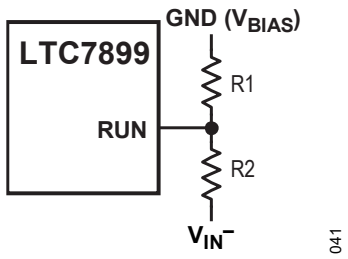


Figure 41. Using the RUN Pin as Undervoltage Lockouts

The V_{IN} UVLO threshold can be computed using the equation 17 and 18.

$$\text{UVLO RISING} = 1.2\text{V} \cdot (1 + \frac{\text{R1}}{\text{R2}}) \quad (17)$$

$$\text{UVLO FALLING} = 1.08 \cdot (1 + \frac{\text{R1}}{\text{R2}}) \quad (18)$$

The current that flows through the R1-R2 divider directly adds to the shutdown, sleep, and active current of the LTC7899, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the MΩ range may be required to keep the impact on quiescent shutdown and sleep currents low.

Soft-Start (SS Pin)

The start-up for V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 1.2V reference, the LTC7899 regulates the V_{FBB} pin voltage to the voltage on the SS pin instead of the internal reference.

Soft-start is enabled by connecting a capacitor from the SS pin to V_{IN}^-. An internal 9µA current source charges the capacitor, providing a linear ramping voltage at the SS pin. The LTC7899 regulates its feedback voltage (and hence V_{OUT} referenced to ground) according to the voltage on the SS pin, allowing V_{OUT} to rise smoothly to its final regulated value. For a desired soft-start time, t_{SS}, select a soft-start capacitor $C_{SS} = t_{SS} \bullet 7.5\text{nF/msec}$.

DRV_{CC} and $INTV_{CC}$ Regulators (OPTI-DRIVE)

The LTC7899 features two separate internal LDO linear regulators that supply power at the DRV_{CC} pin from either the V_{BIAS} pin or the $EXTV_{CC}$ pin, depending on the $EXTV_{CC}$ pin voltage and connections to the DRVSET and DRVUV pins. Another LDO linear regulator supplies power at the $INTV_{CC}$ pin from the DRV_{CC} pin. The DRV_{CC} pin is the supply pin for the MOSFET gate drivers and the $INTV_{CC}$ LDO regulator whereas $INTV_{CC}$ pin is the supply pin for much of the LTC7899 internal circuitry. The V_{BIAS} LDO regulator and the $EXTV_{CC}$ LDO regulator regulate DRV_{CC} between 5V to 10V, depending on how the DRVSET pin is set. Each LDO regulator can supply a peak current of at least 100mA.

Bypass the DRV_{CC} pin to V_{IN}^- with a minimum of 4.7µF ceramic capacitor, and place it as close as possible to the pin. It is recommended to place an additional 1µF ceramic capacitor next to the DRV_{CC} pin and V_{IN}^- pin to supply the high frequency transient currents required by the MOSFET gate drivers. The $INTV_{CC}$ supply must be bypassed to V_{IN}^- with a 0.1µF ceramic capacitor.

The DRVSET pin programs the DRV_{CC} supply voltage, and the DRVUV pin selects different DRV_{CC} UVLO and $EXTV_{CC}$ switchover threshold voltages. *Table 6* summarizes the different DRVSET pin configurations along with the voltage settings that go with each configuration. *Table 7* summarizes the different DRVUV pin configurations and voltage settings. Tying the DRVSET pin to $INTV_{CC}$ programs DRV_{CC} to 9.7V. Tying the DRVSET pin to V_{IN}^- programs DRV_{CC} to 6V. Place a 50k to 100k resistor between DRVSET and V_{IN}^- to program the DRV_{CC} voltage between 5V to 10V, as shown in *Figure 42*.

Table 6. DRVSET Pin Configurations and Voltage Settings

DRVSET PIN	DRV_{CC} VOLTAGE (V)
$\lvert V_{IN}^- \rvert$	6
$INTV_{CC}$	9.7
Resistor to $\lvert V_{IN}^- \rvert$ 50k to 100k	5 to 10

Table 7. DRVUV Pin Configurations and Voltage Settings

DRVUV PIN	DRV_{CC} UVLO RISING and FALLING THRESHOLDS (V)	$EXTV_{CC}$ SWITCHOVER RISING and FALLING THRESHOLDS (V)
$\lvert V_{IN}^- \rvert$	4.0 and 3.8	4.7 and 4.45
FLOAT	5.5 and 5.2	6.0 and 5.75
$INTV_{CC}$	7.5 and 6.7	7.7 and 7.45

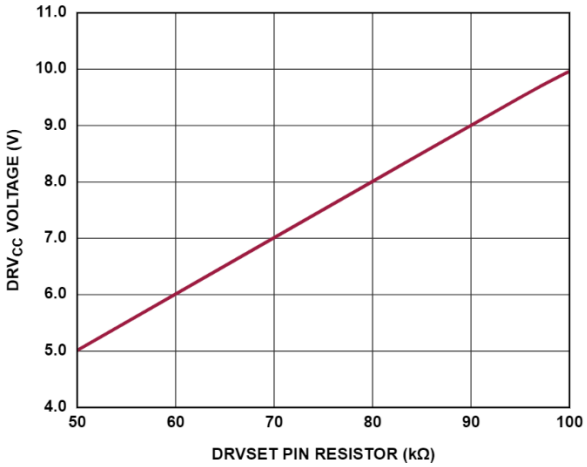


Figure 42. Relationship between DRV_{CC} Voltage and Resistor Value at DRVSET Pin

High input voltage applications in which large MOSFETs are driven at high frequencies can exceed the maximum junction temperature rating for the LTC7899. The DRV_{CC} current, which is dominated by the gate charge current, can be supplied by either the V_{BIAS} LDO regulator or the $EXTV_{CC}$ LDO regulator. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.45V, 5.75V, or 7.45V, as determined by the DRVUV pin), the V_{BIAS} LDO regulator is enabled. In this case, power dissipation for the IC is equal to $\lvert V_{IN}^- \rvert \times DRV_{CC}$ current (I_{DRVCC}). The gate charge current is dependent on the operating frequency, as discussed in the *Efficiency Considerations* section. To estimate the junction temperature, use the equation detailed in Note 2. For example, the LTC7899 DRV_{CC} current is limited to less than 35mA from a 36V supply when not using the $EXTV_{CC}$ supply at an ambient temperature of 95°C, as shown in Equation 19:

$$T_J = 95°C + (35mA)(36V)(43°C/W) = 150° \quad (19)$$

To prevent the junction temperature from exceeding the maximum rated as shown in *Table 2*, check the input supply current while operating in continuous conduction mode (MODE = $INTV_{CC}$) at maximum $\lvert V_{IN}^- \rvert$.

When the voltage applied to $EXTV_{CC}$ rises above its rising switchover threshold, the V_{BIAS} LDO regulator turns off and the $EXTV_{CC}$ LDO regulator enables. The $EXTV_{CC}$ LDO regulator remains on as long as the voltage applied to $EXTV_{CC}$ remains above its falling switchover threshold. The $EXTV_{CC}$ LDO attempts to regulate the DRV_{CC} voltage to the voltage as programmed by the DRVSET pin. Therefore, while $EXTV_{CC}$ is less than this voltage, the LDO regulator is in dropout and the DRV_{CC} voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than the programmed voltage (up to an absolute maximum of 30V), DRV_{CC} is regulated to the programmed voltage. Using the $EXTV_{CC}$ LDO regulator allows the MOSFET driver and control power to be derived from one of the switching regulator outputs of the LTC7899 during normal operation, and from the V_{BIAS} LDO when the output is out of regulation (e.g., start-up or short-circuit). If more current is required through the $EXTV_{CC}$ LDO than is specified, add an external Schottky diode between the $EXTV_{CC}$ and DRV_{CC} pins. In this case, do not apply more than 14V to the $EXTV_{CC}$ pin.

The following list summarizes the two possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ connected to $INTV_{CC}$. This connection causes V_{BIAS} LDO regulator to power DRV_{CC}, resulting in an efficiency penalty of up to 10% or more at high input voltages.
2. $EXTV_{CC}$ connected to an external supply. If an external supply is available, it can be used to power $EXTV_{CC}$, provided that it is compatible with the MOSFET gate drive requirements. This supply can be higher or lower than V_{IN}. However, a lower $EXTV_{CC}$ voltage results in higher efficiency.

Topside MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor, C_B, connected to the BOOST pin supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged through external diode D_B from DRV_{CC} when the SW pin is low, and the bottom MOSFET is turned on.

When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{OUT} and the BOOST pin follows. With the topside MOSFET on, the BOOST voltage is above the output voltage: $V_{BOOST} = V_{OUT} + V_{DRVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). For a typical application, a value of $C_B = 0.1\mu F$ is generally sufficient.

The external diode D_B can be a Schottky diode or silicon diode, but in either case it should have low leakage and fast recovery. The reverse breakdown of the diode must be greater than $(V_{OUT} + |V_{IN(MAX)}|)$. Pay close attention to the reverse leakage at high temperatures where it generally increases substantially.

A leaky diode not only increases the quiescent current of the converter, but it can also create a current path from the BOOST pin to DRV_{CC}. This will cause DRV_{CC} to rise if the diode leakage exceeds the current consumption on DRV_{CC}, which is primarily a concern in burst mode operation where the load on DRV_{CC} can be very small. There is an internal voltage clamp on DRV_{CC} that prevents the DRV_{CC} voltage from running away, but this clamp should be regarded as a failsafe only.

Minimum On-Time Considerations

The minimum on-time ($t_{ON(MIN)}$) is the smallest time duration that the LTC7899 is capable of turning on the bottom MOSFET. It is determined by internal timing delays and the gate charge required to turn on the MOSFET. Low duty cycle applications can approach this minimum on-time limit. Take care to ensure the results in Equation 20, as follows:

$$t_{ON(MIN)} < \frac{V_{OUT}}{(V_{OUT}+|V_{IN}^{-}|)\cdot f} \quad (20)$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller begins to skip cycles. The output voltage continues to be regulated, but the ripple voltage and current increases. The minimum on-time for the LTC7899 is approximately 120ns. However, as the peak sense voltage decreases, the minimum on-time gradually increases up to about 130ns. This change is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self-heating (such as a short from DRV_{CC} to V_{IN}^-), internal overtemperature shutdown circuitry shuts down the LTC7899. When the internal die temperature exceeds 180°C, the DRV_{CC} LDO regulator and gate drivers are disabled. When the die cools to 160°C, the LTC7899 enables the DRV_{CC} LDO regulator and resumes operation, beginning with a soft-start start-up. Avoid long-term overstress (T_J > 150°C) because it can degrade the performance or shorten the life of the device.

Phase-Locked Loop and Frequency Synchronization

The LTC7899 has an internal PLL that allows the turn-on of the bottom MOSFET to be synchronized to the rising edge of an external clock signal applied to the PLLIN/SPREAD pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

Rapid phase locking can be achieved by using the FREQ pin to set a free running frequency near the desired synchronization frequency. Before synchronization, the PLL is prebiased to the frequency set by the FREQ pin. Consequently, the PLL only needs to make minor adjustments to achieve phase lock and synchronization. Although it is not required, placing the free-running frequency near the external clock frequency prevents the oscillator from passing through a large range of frequencies as the PLL locks.

When synchronized to an external clock, the LTC7899 operates in pulse-skipping mode if it is selected by the MODE pin, or in forced continuous mode otherwise. The LTC7899 is guaranteed to synchronize to an external clock applied to the PLLIN/SPREAD pin that swings up to at least 2.2V and down to 0.5V or less. Note that the LTC7899 can only be synchronized to an external clock frequency within the range of 100kHz to 2.5MHz.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. Analyzing individual losses is useful for determining what is limiting the efficiency and which change produces the most improvement. The percent efficiency can be expressed by Equation 21, as follows:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...) \quad (21)$$

where L1, L2, L3, and so on, are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7899 circuits: IC V_{BIAS} current, DRV_{CC} regulator current, I^2R losses, and bottom MOSFET transition losses.

1. The V_{BIAS} current is the DC supply current given in *Table 1*, which excludes MOSFET driver and control currents. Other than at light loads in Burst Mode operation, V_{BIAS} current typically results in a small (<0.1%) loss.

2. DRV_{CC} current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge (dQ) moves from DRV_{CC} to V_{IN}^-. The resulting dQ/time duration (dt) is a current out of DRV_{CC} that is typically much larger than the control circuit current. In continuous mode,

gate charge current ($I_{GATECHG}$) = $f_{SW}(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the top and bottom MOSFETs and f_{SW} is the switching frequency.

3. I^2R losses are predicted from the DC resistances of the input fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode, the average input current flows through L and R_{SENSE}, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, the resistance of one MOSFET can be summed with the resistances of L, R_{SENSE}, and ESR to obtain the I^2R losses.

4. Transition losses apply only to the bottom MOSFETs and become significant only when operating at higher input voltages (typically 15V or greater) or at high frequency (MHz range). Transition losses can be estimated from the equation for the main switch power dissipation in the *Power MOSFET Selection* section.

Other hidden losses, such as copper trace and internal battery resistances, can account for an additional 5% to 10% efficiency degradation in portable systems. It is important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and low ESR at the switching frequency. A 25W supply typically requires a minimum of 20µF to 40µF of capacitance with a maximum of 20mΩ to 50mΩ of ESR. Other losses, including body diode conduction losses during dead time and inductor core losses, generally account for less than 2% total additional loss but can be significant when operating at high switching frequency.

Checking Transient Response

To check the regulator loop response, look at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} × ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for excessive overshoot or ringing, which indicates a stability problem.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time, and settling at this test point reflects the closed-loop response. Assuming a predominantly second order system, the phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the *Typical Application* circuits provide an adequate starting point for most applications.

The ITH series compensation resistor (R_C) to compensation capacitor (C_C) filter sets the dominant pole zero loop compensation. The values can be modified slightly (from 0.5 times to 2 times their initial values) to optimize transient response when the final PCB layout is done and the particular output capacitor type and value are determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of the full load current, with a rise time of 1µs to 10µs, produces output voltage and ITH pin waveforms that give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across from the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop. Therefore, this signal cannot be used to determine phase margin. For this reason, it is better to look at the ITH pin signal, which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop increases by increasing R_C, and the bandwidth of the loop increases by decreasing C_C. If R_C increases by the same factor that C_C

decreases, the zero frequency is kept the same, keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and demonstrates the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage, if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time must be controlled so that the load rise time is limited to approximately C_{LOAD} × 25µs/µF. Therefore, a 10µF capacitor requires a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume the nominal input voltage $V_{IN(NOMINAL)}$ = –48V with a range of –60V to –36V all with respect to ground, V_{OUT} = 12V with respect to ground, I_{OUT} = 8A, and f_{SW} = 200kHz.

Take the following steps to design an application circuit:

1. Set the operating frequency. The frequency is not one of the internal preset values. Therefore, a resistor from the FREQ pin to V_{IN}^- is required, with a value given by Equation 22, as follows:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{200\text{kHz}} = 185\text{k}\Omega \quad (22)$$

2. Determine the inductor value. Initially, select a value based on an inductor ripple current of 30%. The inductor value can then be calculated using Equation 23, as follows:

$$L = \frac{|V_{IN}-|}{f_{SW}\cdot(\Delta I_L)}\left(\frac{V_{OUT}}{|V_{IN}-|+V_{OUT}}\right) = 7.5\mu\text{H} \quad (23)$$

   The largest ripple happens when $|V_{IN}^-|$ = 36V, where the average maximum inductor current is $I_{L(MAX)} = I_{OUT(MAX)} \bullet (1 + V_{OUT}/|V_{IN}^-|)$ = 10.7A. A 10µH inductor will produce 30% ripple current. The peak inductor current will be the maximum DC value plus one-half the ripple current, or 12.3A.

3. Verify the minimum on-time of 120ns is not violated. The minimum on-time occurs at $V_{IN(MAX)}$, as shown in Equation 24, as follows:

$$t_{ON(MIN)} < \frac{V_{OUT}}{(|V_{IN(MAX)-}|+V_{OUT})\cdot f_{SW}} = \frac{12\text{V}}{60\text{V}\cdot 200\text{k}} = 1\mu\text{s} \quad (24)$$

4. This time is sufficient to satisfy the minimum on-time requirement. If the minimum on-time is violated, the LTC7899 skips pulses at high input voltage, resulting in lower frequency operation and higher inductor current ripple than desired. If undesirable, this behavior can be avoided by decreasing the frequency (with the inductor value accordingly adjusted) to avoid operation near the minimum on-time.

5. Select the R_{SENSE} resistor value. The peak inductor current is 10.7A • (1 + 0.30/2) = 12.3A in this case. The R_{SENSE} resistor value can then be calculated based on the minimum value for the maximum current sense threshold (45mV for ILIM = FLOAT), given by Equation 25, as follows:

$$R_{SENSE} \leq \frac{45\text{mV}}{13\text{A}} \cong 3\text{m}\Omega \quad (25)$$

6. To allow for additional margin, a lower value R_{SENSE} can be used (e.g., 2mΩ); however, be sure that the inductor saturation current has sufficient margin above $V_{SENSE(MAX)}/R_{SENSE}$, where the maximum value of 55mV is used for $V_{SENSE(MAX)}$.

7. Select the feedback resistors. If light load efficiency is required, high value feedback resistors can be used to minimize the current due to the feedback divider. Choosing 1% resistors: R_A = 20kΩ and R_B = 2kΩ yields an output voltage of 12.0V.
8. Select the MOSFETs. The best way to evaluate MOSFET performance in a particular application is to build and test the circuit on the bench, facilitated by an LTC7899 demo board. However, an educated guess about the application is helpful to initially select MOSFETs. I^2R losses will likely dominate over transition losses for the bottom MOSFET. Therefore, choose a MOSFET with lower $R_{DS(ON)}$ as opposed to lower gate charge to minimize the combined loss terms. The top MOSFET does not experience transition losses, and its power loss is generally dominated by I^2R losses. For this reason, the top MOSFET is typically chosen to be of lower $R_{DS(ON)}$ and subsequently higher gate charge than the bottom MOSFET. Also, choose MOSFETs with
   $B_{VDSS} > (V_{OUT} + |V_{IN(MAX)}^-|) = 72V$.
9. Select the input and output capacitors. C_{OUT} is chosen to filter the square current in the output. The maximum output current peak is given by Equation 26, as follows:

$$V_{ORIPPLE} = ESR \bullet \Delta I_L = 10m\Omega * 3.2A = 32mV_{P-P} \quad (26)$$

   On the 12V output, $32mV_{P-P}$ is equal to 0.26% of peak-to-peak voltage ripple.

10. Determine the bias supply components. Because the regulated output is greater than the $EXTV_{CC}$ switchover threshold, it can be used to bias $EXTV_{CC}$. For an 8ms soft-start, select a 0.1µF capacitor for the SS pin. As a first pass estimate for the bias components, select the DRV_{CC} capacitance C_{DRVCC} = 4.7µF, C_{INTVCC} = 0.1µF and C_B = 0.1µF.
11. Determine and set application specific parameters. Set the MODE pin based on the trade-off of light load efficiency and constant frequency operation. Set the PLLIN/SPREAD pin based on whether a fixed, spread spectrum, or phase-locked frequency is desired. The RUN pin can be used to control the minimum input voltage for regulator operation, or it can be tied to V_{BIAS} for always-on operation. Use ITH compensation components from the typical applications as a first guess, check the transient response for stability, and modify as necessary.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. *Figure 43* illustrates the current waveforms present in the various branches of the synchronous regulators operating in the continuous mode. Check the following in the layout:

1. Route the BGUP and BGDN traces together and connect them as close as possible to the bottom MOSFET gate. If using gate resistors, connect the resistor connections to the MOSFET gate as close as possible to the MOSFET. Connecting BGUP and BGDN further away from the bottom MOSFET gate can cause inaccuracies in the dead time control circuit of the LTC7899. Route the TGUP and TGDN traces together and connect them as close as possible to the top MOSFET gate.
2. Are the signal and power grounds kept separate? The combined IC V_{IN}^- pin and the V_{IN}^- return of C_{DRVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the top N-channel MOSFET and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the loop.
3. Does the LTC7899 V_{FBA} pin resistor (R_A) connect to the (+) terminal of C_{OUT}? Place the V_{FBA} and V_{FBB} resistors close to their respective V_{FB} pin to minimize noise coupling into the sensitive V_{FB} node. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
4. Route the $SENSE^-$ and $SENSE^+$ leads together with minimum PCB trace spacing. Route these traces away from the high frequency switching nodes on an inner layer, if possible. The filter capacitor between $SENSE^+$ and $SENSE^-$ must be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.
5. Connect the DRV_{CC} decoupling capacitor close to the IC, between the DRV_{CC} and the power V_{IN}^- pin. This capacitor carries the current peaks of the MOSFET drivers. Place an additional 1µF ceramic capacitor next to the DRV_{CC} and V_{IN}^- pins to help improve noise performance.
6. Keep the switching node (SW), top gate nodes (TGUP and TGDN), and boost node (BOOST) away from sensitive small signal nodes, especially from the voltage and current sensing feedback pins. All of these nodes have large and fast-moving signals. Therefore, keep the nodes on the output side of the LTC7899 and ensure they occupy the minimum PCB trace area.
7. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PCB as the input and output capacitors, with tie-ins for the bottom of the DRV_{CC} decoupling capacitor, the bottom of the voltage feedback resistive divider, and the GND pin of the IC.
8. Use separate traces and vias to connect the DRV_{CC} capacitor to the BOOST diode versus the connections to the controller, bias and pull-up connections.

PC Board Layout Debugging

Use a DC to 50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (the SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation is maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold, typically 25% of the maximum designed current level in burst mode operation.

The duty cycle percentage is maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame an improper PCB layout if regulator bandwidth optimization is not required.

Reduce $|V_{IN}^-|$ from its nominal level to verify operation of the regulator at maximum duty cycle. Check the operation of the undervoltage lockout circuit by further lowering $|V_{IN}^-|$ while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher $|V_{IN}^-|$ voltages. If problems coincide with high $|V_{IN}^-|$ and low output currents, look for capacitive coupling between the BOOST, SW, TGxx, and possibly BGxx connections and the sensitive voltage and current pins. Place the capacitor across the current sensing pins next to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower $|V_{IN}^-|$ voltages, look for inductive coupling between C_{IN}, the top MOSFET, and the bottom MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate the common GND path voltage pickup between these components and the $|V_{IN}^-|$ pin of the IC.

A problem that can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup is maintained, but the advantages of current mode control are not realized. Compensation of the voltage loop is more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor. The regulator maintains control of the output voltage.

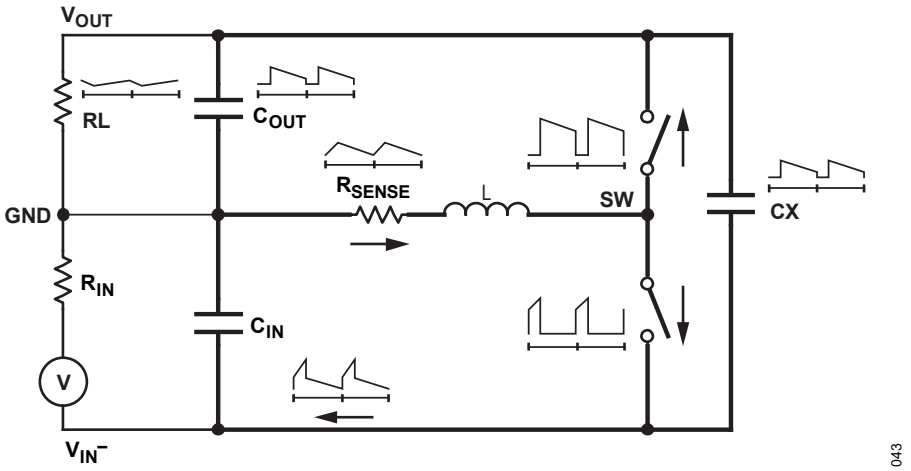


Figure 43. Branch Current Waveforms

TYPICAL APPLICATION

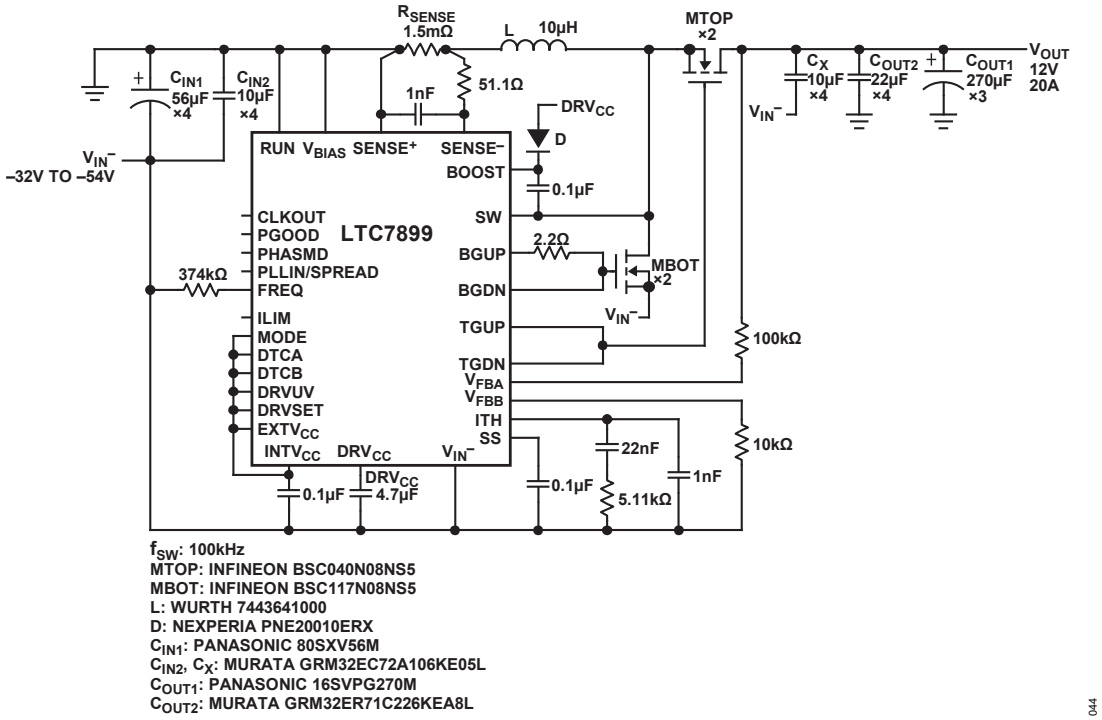


Figure 44. High Efficiency 100kHz 12V/20A Negative to Positive Converter

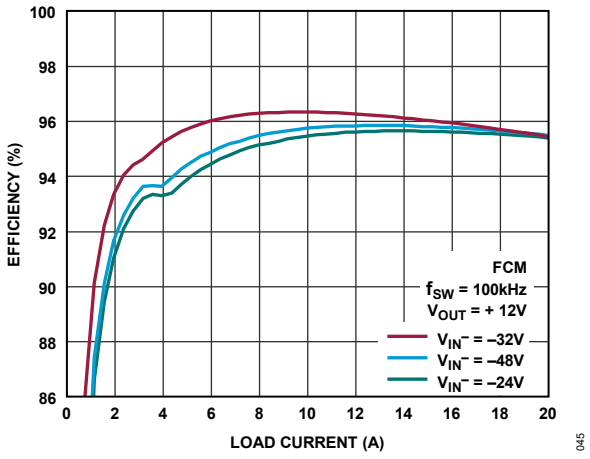


Figure 45. V_{OUT} Efficiency vs. Load Current for Figure 44

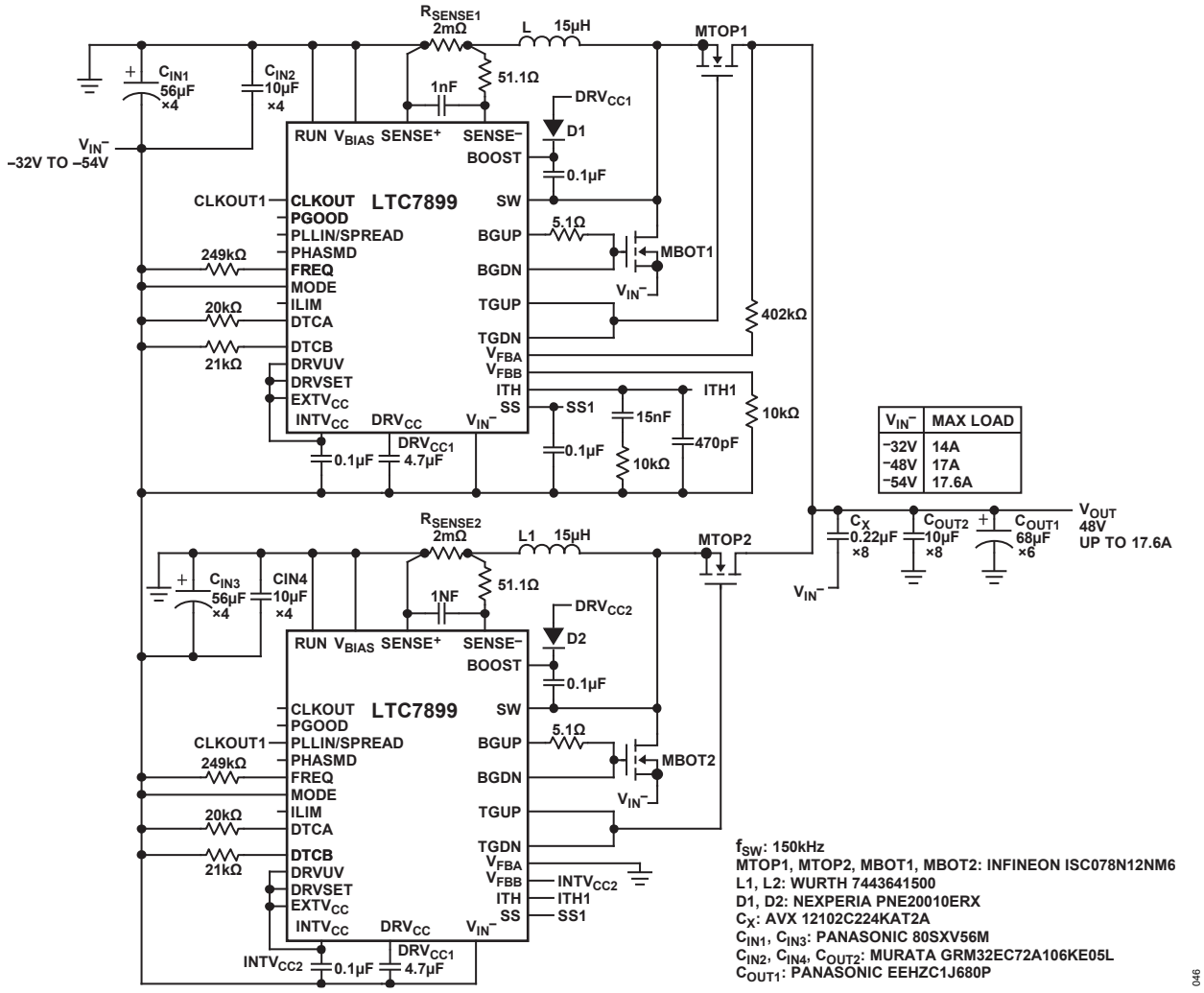


Figure 46. High Efficiency 2-Phase Single Output 48V Negative to Positive Converter

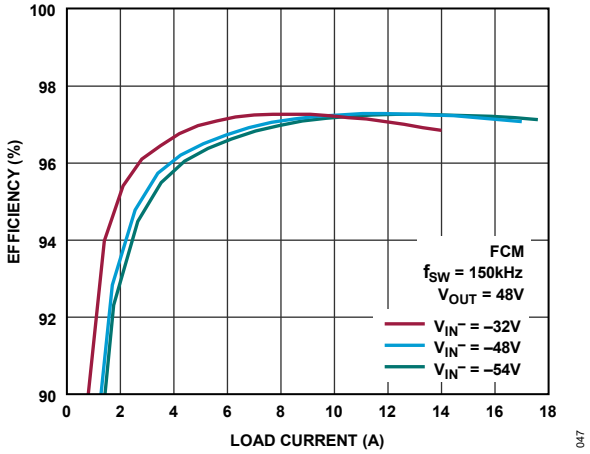


Figure 47. V_{OUT} Efficiency vs. Load Current for Figure 46

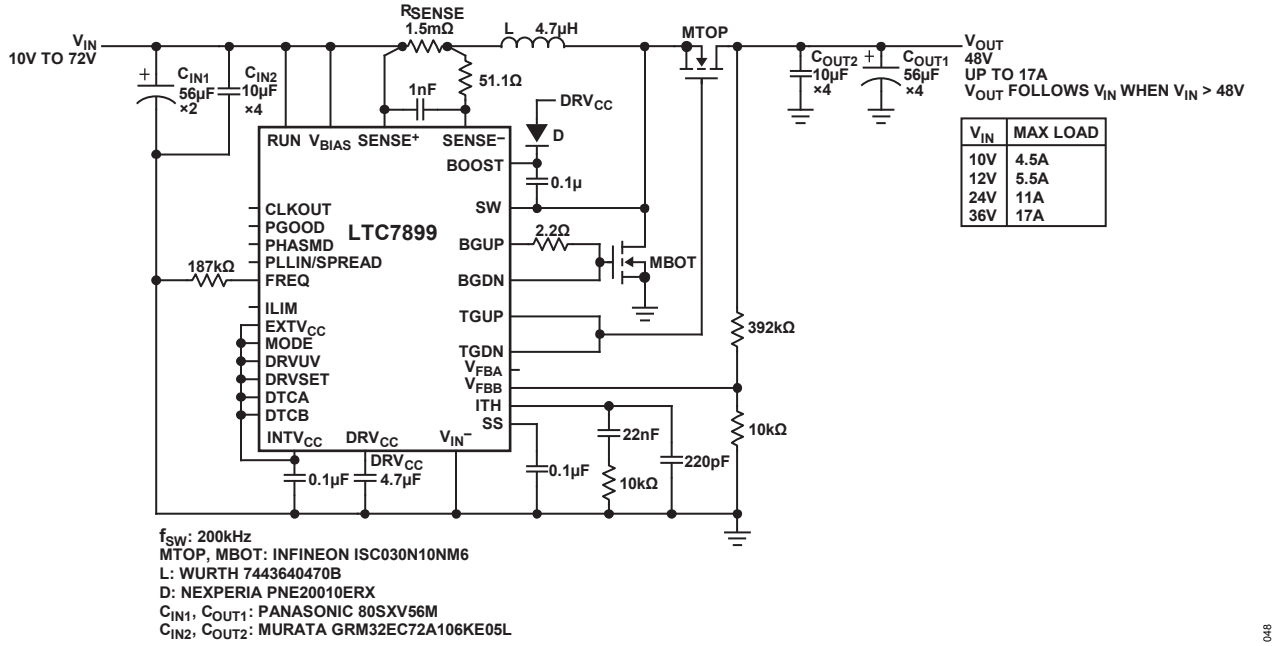
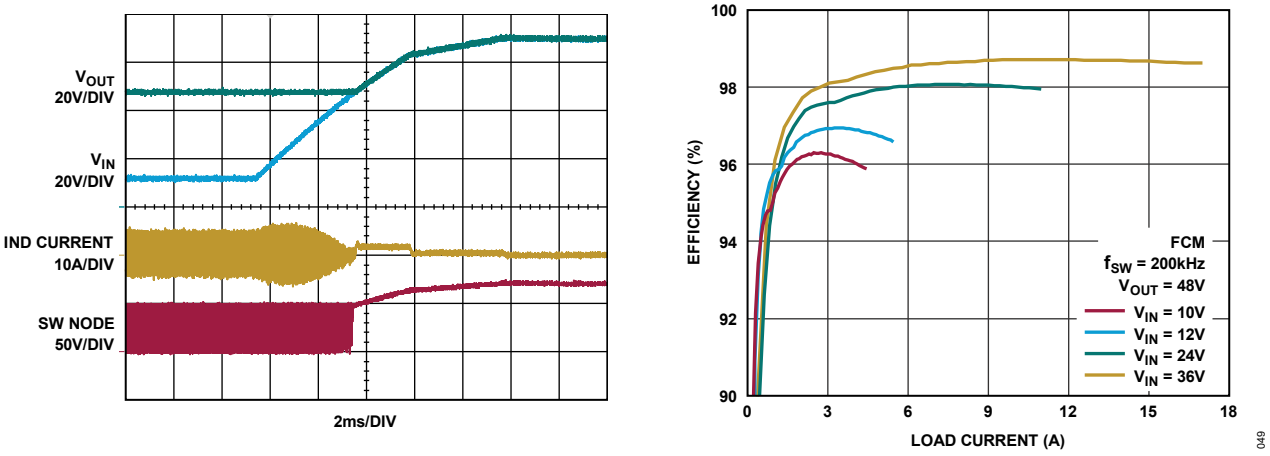


Figure 48. High Efficiency Wide Input Range 48V/17A Boost Converter with Pass-Through



(49a) V_{OUT} Start-Up

(49b) V_{OUT} Efficiency vs. Load Current

Figure 49. V_{OUT} Start-Up and Efficiency vs. Load Current for Figure 48

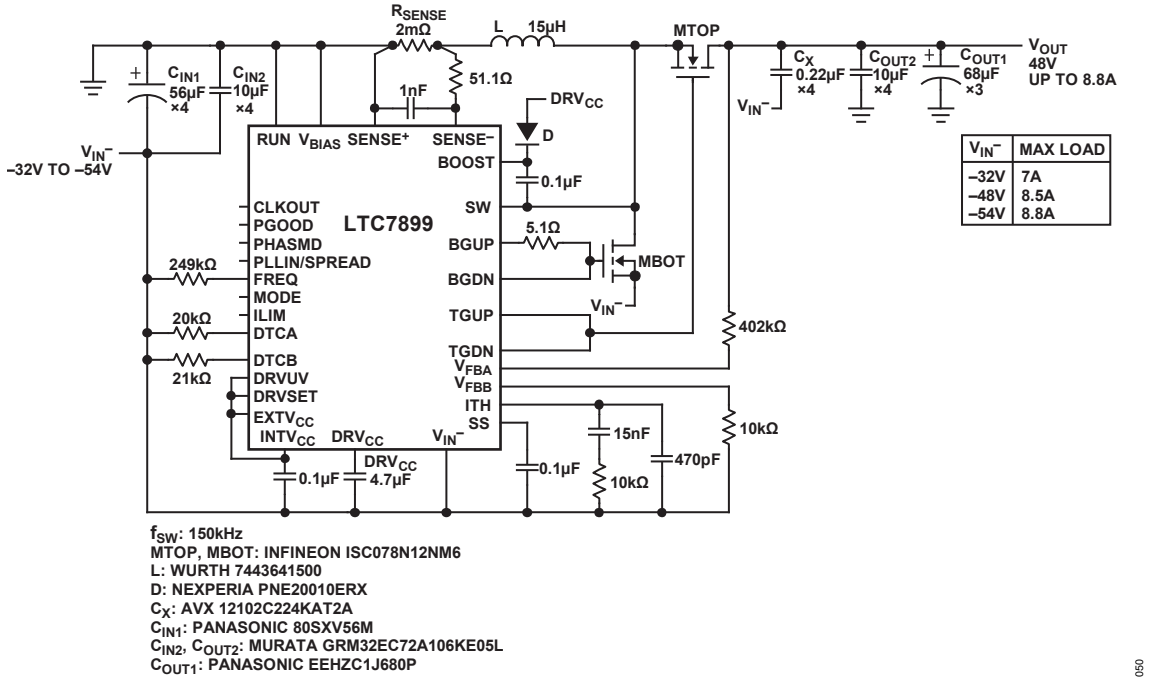


Figure 50. High Efficiency Wide Input 48V/8.8A Negative to Positive Converter

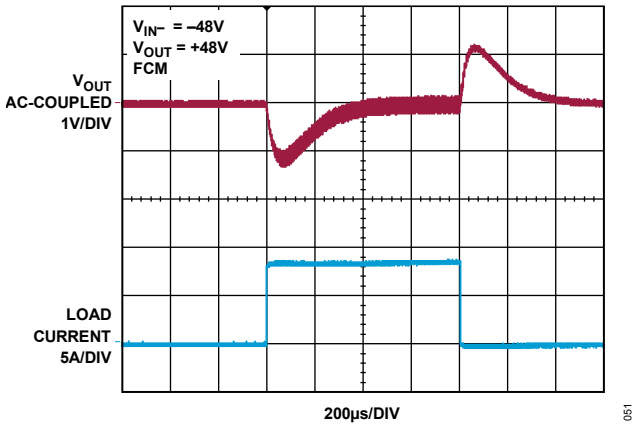


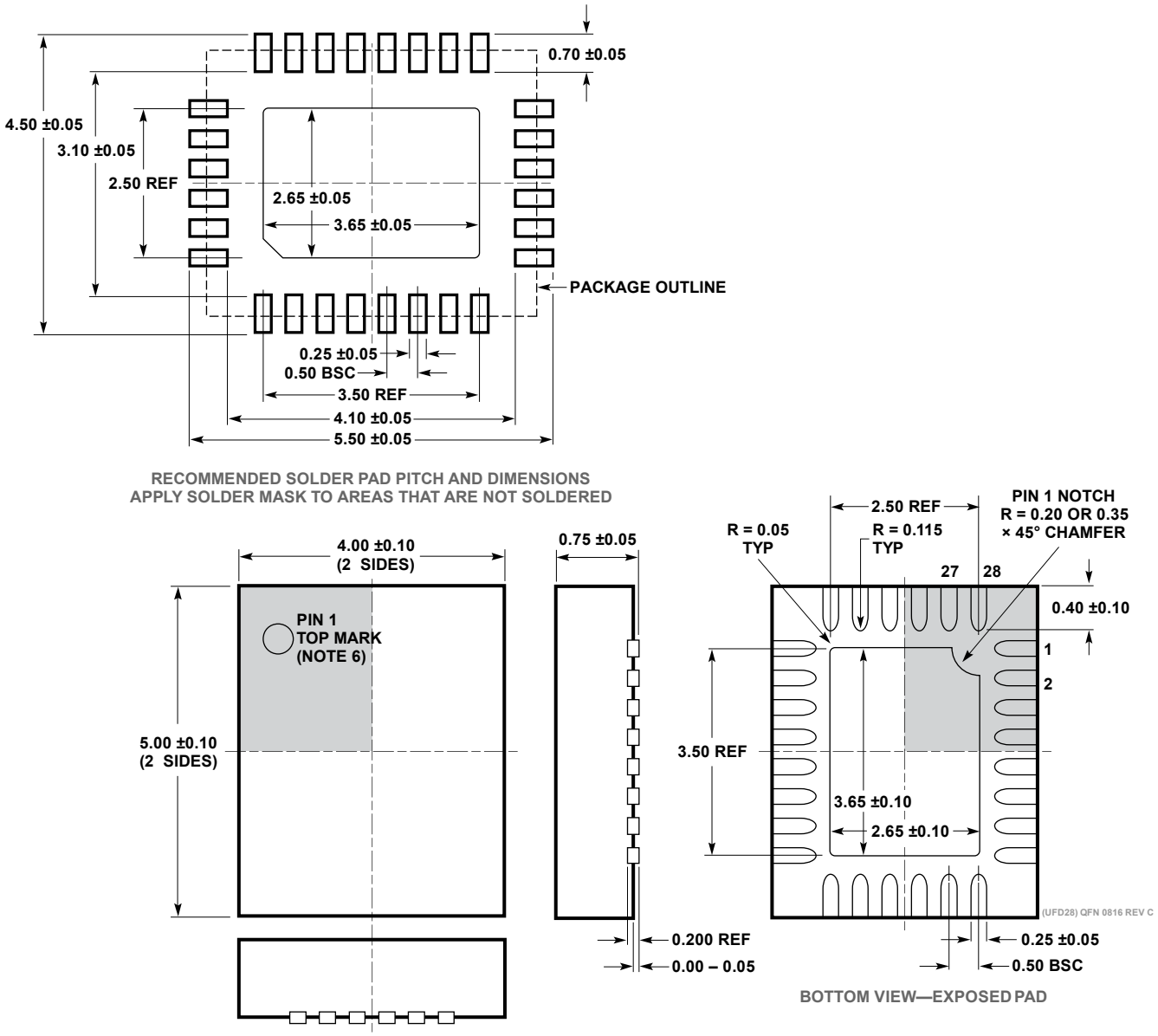
Figure 51. V_{OUT} Load Transient for Figure 50

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8709	Negative Input Synchronous Multi-Topology DC/DC Controller	V_{IN}: -4.5V to -80V, 100kHz to 750kHz Programmable Operating Frequency, Rail-to-Rail Output Current Monitor and Control, Power Good Pin, 20-Lead TSSOP Package
LTC3896	150V Low I_Q, Synchronous Inverting DC/DC Controller	V_{IN}: 4V to 140V, 50kHz to 900kHz Programmable Operating Frequency, Phase lockable frequency 75kHz to 850kHz, integrated Bootstrap Diode, Power Good Pin, 38-Lead TSSOP Package
LT3758	100V Boost, Flyback, SEPIC and Inverting Controller	V_{IN}: 5.5V to 100V, 100kHz to 1MHz Programmable Operating Frequency, 10-Lead DFN (3mm × 3mm) and MSOPE Packages, AEC-Q100 qualified
LT8710	80V Synchronous SEPIC/Inverting/Boost Controller with Output Current Control	V_{IN}: 4.5V to 80V, 100kHz to 750kHz Programmable Operating Frequency, Rail-to-Rail Output Current Monitor and Control, C/10 or Power Good Pin, 20-Lead TSSOP Package
LT8714	80V Bipolar Output Synchronous Controller with Seamless Four Quadrant Operation	V_{IN}: 4.5V to 80V, 100kHz to 750kHz Programmable Operating Frequency, Power Good Pin, 20-Lead TSSOP Exposed Package
LTC3863	65V Low I_Q Inverting DC/DC Controller	V_{IN}: 3.5 V to 60 V, 50kHz to 850kHz Programmable Operating Frequency, Phase lockable frequency 75kHz to 750kHz, 12-Lead Thermally Enhanced MSOP and 3mm × 4mm DFN Packages
LT3958	80V Flyback, SEPIC and Inverting Converter with 3.3A, 84V Switch	V_{IN}: 5V to 80V, 100kHz to 1MHz Programmable Operating Frequency, Thermally Enhanced QFN (5mm × 6mm) Package

OUTLINE DIMENSIONS

UFD Package
28-Lead Plastic QFN (4mm x 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 52. Package Description

ORDERING GUIDE

Table 8. Ordering Guide

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7899RUFD#PBF	LTC7899RUFD#TRPBF	LTC7899	28-Lead (4mm x 5mm) Plastic QFN	−40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.