30mΩ R_{ON} 12V Octal Electronic Circuit Breaker with SPI Interface

FEATURES

- **Eight Channels – 8× SPST**
- **Circuit Breaker Threshold Up to 1.5A Programmable in 50mA Increments**
- **20% Accurate Threshold**
- **30mΩ On Resistance**
- Operating Range: 0V to 13.2V
- SPI Interface with Daisy-Chain Mode
- Common Open-Drain FAULT Status Output
- 24-Lead 3mm × 5mm QFN

APPLICATIONS

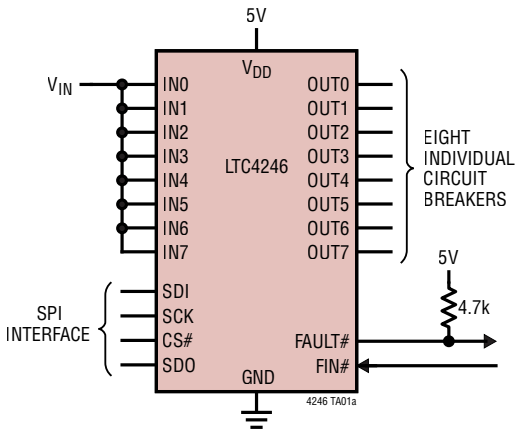
- ATE Wafer Probe Electronics
- Scope Probe Protection
- Industrial Control
- Relay Replacement

DESCRIPTION

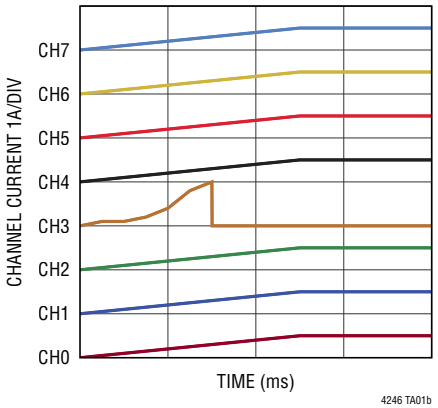
The LTC®4246 contains eight switches, each with an independent circuit breaker function. It is particularly well suited for extremely space constrained designs. Each switch can operate completely autonomously or be arbitrarily grouped with other switches that will respond together to the fault of any single device within its group. Optionally, channel grouping may be extended to multiple LTC4246 devices by selecting the FIN# (fault input) pin as part of a channel group. A required bias supply between 2.5V to 5V allows the switches to independently operate from 13.2V down to 0V. The LTC4246 provides an SPI serial interface to enable, disable and configure the timing and current thresholds of each channel as well as provide status to each channel's fault state.

A common open-drain FAULT status output indicates if any switch has opened due to a circuit breaker event.

TYPICAL APPLICATION



Startup with Fault on Channel 3

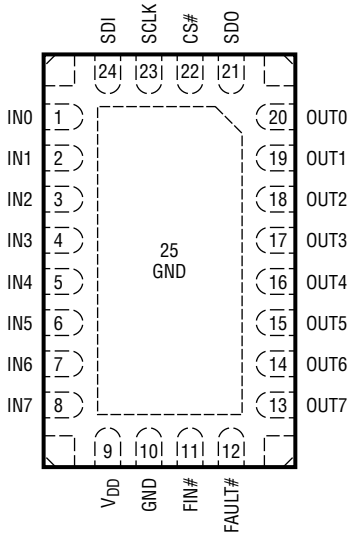


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{DD} .....–0.3V to 5.5V
SDI, SCLK, CS#, SDO.....–0.3V to 5.5V
IN0 - IN7 .....–0.3V to 16V
OUT0 - OUT7 .....–0.3V to 16V
FIN#.....–0.3V to V_{DD} + 0.3V
FAULT#.....–0.3V to V_{DD} + 0.3V
Average Output Current (OUT0 ~ OUT7).....1.8A
Average FAULT# Current 10mA
Operating Junction Temperature Range
I-Grades.....–40°C to 85°C
H-Grades .....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C
Maximum Reflow (Package Body)
Temperature.....260°C

PIN CONFIGURATION



LQFN PACKAGE
24-LEAD (3mm × 5mm × 0.95mm)
θ_{JA} = 37°C/W, MSL LEVEL 3
EXPOSED PAD (PIN 25) IS GND, SHOULD BE SOLDERED TO PCB

ORDER INFORMATION

TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4246IV#PBF	LHKW	24-Lead (3mm × 5mm × 0.95mm) LQFN Package	–40°C to 85°C
LTC4246HV#PBF	LHKW	24-Lead (3mm × 5mm × 0.95mm) LQFN Package	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	V_{DD} Operating Range		●	2.5		5.5	V
I_{DD}	V_{DD} Input Supply Current	CS# = V_{DD}, SCLK = 0V	●		2.5	5	mA
$PORb_{THLD}$	PORb Threshold	V_{DD} Rising	●	2.3		2.5	V
$PORb_{HYST}$	PORb Hysteresis	V_{DD} Falling			115		mV
V_{IN}	INn Operating Range		●	0		13.2	V
V_{OUT}	OUTn Operating Range	Note 5	●	0		V_{IN}	V
R_{ON}	Switch On Resistance	Threshold Set to 1.5A	●		30	50	mΩ
R_{ON} Matching	Switch On Resistance Matching CH 0-7	Threshold Set to 1.5A, Max - Min			2.5		mΩ
E_{AS}	Peak Avalanche Energy	L = 10µH, Note 6			5		mJ
dV_{OUT}/dt	Output Voltage Slew Rate	INn = 12V, R_{LOAD} = 10kΩ, C_{LOAD} = 10pF, Note 6			0.8		V/µs
$I_{ECB(ACCY)}$	Circuit Breaker Current Threshold Accuracy	All Ranges, Percent of Setting Ranges 150mA and 1500mA Ranges 50mA and 100mA	 ● ●			 ±20 ±30	 % %
$I_{ECB(RANGE)}$	Circuit Breaker Current Threshold Range				0.05 – 1.5		A
$I_{ECB(LSB)}$	Circuit Breaker Current LSB Step Size				50		mA
$INn_{LEAK,ON}$	ECB Leakage Current, Channel ON	50mA Range, INn = 13.2V, OUTn = Open 1.5A Range, INn = 13.2V, OUTn = Open 1.5A Range, INn = 13.2V, OUTn = Open	● ●		 600 90	500	nA nA nA
$INn_{LEAK,OFF}$	ECB Leakage Current, Channel OFF	50mA Range, INn = 13.2V, OUTn = 0V			2		nA
$IN_{LEAK,ADJ}$	Channel to Channel IN Leakage	INn = 0V, Other INn = 13.2V, Channel OFF INn = OUTn = 0V, Other INn = OUTn = 13.2V, Channels ON	● ●		| I | < 10 | I | < 10		nA nA
$OUT_{LEAK,ADJ}$	Channel to Channel OUT Leakage	OUTn = 0V, Other OUTn = 13.2V, Channel OFF	●		| I | < 10		nA
$t_{ECB(OFF)}$	Circuit Breaker Response Time	Current Step from 0A to 125% of Threshold CHn_OCP_TIMER = 00 CHn_OCP_TIMER = 01 CHn_OCP_TIMER = 10 CHn_OCP_TIMER = 11	 ● ● ● ●		 10 20 50 100	 12 24 60 120	 µs µs µs µs
$t_{ECB(OFF,FAST)}$	Fast Circuit Breaker Response Time	Current Step from 0A to 250% of Threshold	●			5	µs
$t_{ECB(ON)}$	Circuit Breaker Turn-on Time	R_{DS-ON} < 100mΩ, Threshold Set to 1.5A	●	20	100	120	µs
$t_{ECB(OFF)}$	Circuit Breaker Turn-off Time	From CS# Positive Edge	●		2	5	µs
Logic Inputs							
$V_{IN(TH)}$	FIN#, SDI, SCLK, CS# Input Level		●	$0.1V_{DD}$		$0.9V_{DD}$	$\%V_{DD}$
I_{INH} or I_{INL}	FIN#, SDI, SCLK, CS# Input Leakage Current		●			±1	µA
Logic Outputs							
$V_{FAULT\#(OL)}$	FAULT# Output Low Voltage	I = 3mA	●			150	mV
$I_{FAULT\#(LEAK)}$	FAULT# Output Leakage	V = 5V	●			1	µA
$V_{SDO(OL)}$	SDO Voltage Output Low	I = 1mA (CS# = 0V)	●			150	mV
$V_{SDO(OH)}$	SDO Voltage Output High	–1mA (CS# = 0V)	●	V_{DD} – 0.15			V
$I_{SDO(PU)}$	SDO Weak Pull-up	CS# = V_{DD}, SDO = 0V			2.5		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SPI Interface Timing (Note 4)							
$t_{SCLKH(MIN)}$	Clock High Time		●			20	ns
$t_{SCLKL(MIN)}$	Clock Low Time		●			20	ns
$t_{CS\#H(MIN)}$	CS# High Time		●			1.3	µs
$t_{SCLKCS\#H(MIN)}$	SCLK Low to CS# High Time		●			20	ns
$t_{CS\#SCLKH(MIN)}$	CS# Low to SCLK High Time		●			20	ns
$t_{SDIDS(MIN)}$	SDI Data Setup Time		●			20	ns
$t_{SDIHD(MIN)}$	SDI Data Hold Time		●	0		2	ns
$t_{HDSDO(MIN)}$	SDO Hold Time	C_{LOAD} = 10pF	●			20	ns
$t_{CS\#SDOV(MIN)}$	SDO Valid Time after Falling CS# Edge	C_{LOAD} = 10pF	●			30	ns
$t_{CS\#SDOZ(MIN)}$	SDO High-Z Time after Rising CS# Edge		●			100	ns
$f_{SCLK(MAX)}$	Maximum SCLK Frequency		●	25			MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

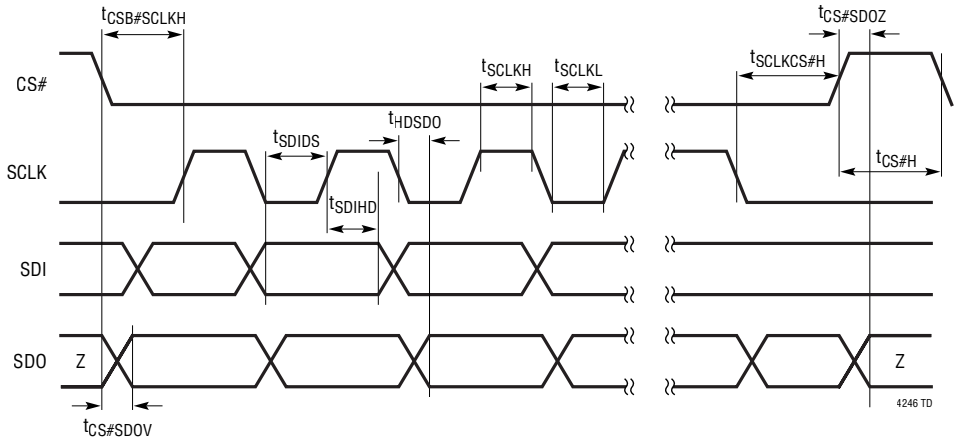
Note 3: The LTC4246 is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$ where θ_{JA} (in °C/W) is the package thermal impedance.

Note 4: Timing specifications are for the LTC4246 as a SPI slave device. See Block Diagram

Note 5: There is a parasitic diode from OUT (anode) to IN (cathode) that limits V_{OUT} to less than or equal to V_{IN}.

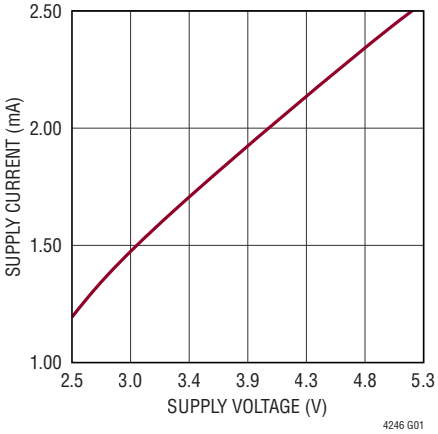
Note 6: The typical value is based on characterization and is not production tested.

TIMING DIAGRAM

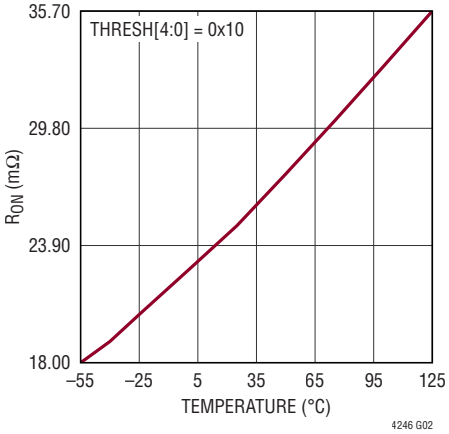


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{DD} = 5V unless otherwise noted.

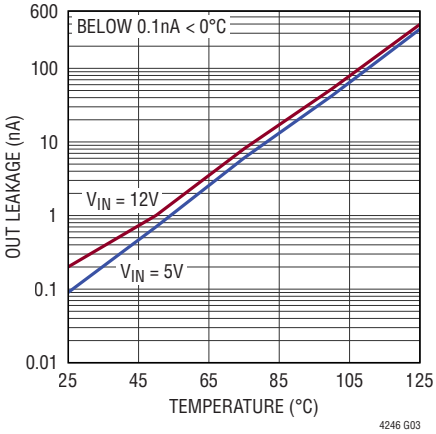
Supply Current



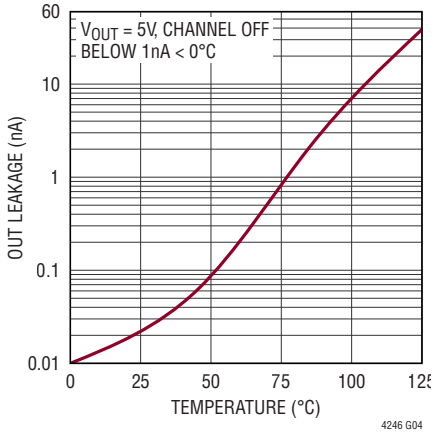
R_{ON} vs Temperature



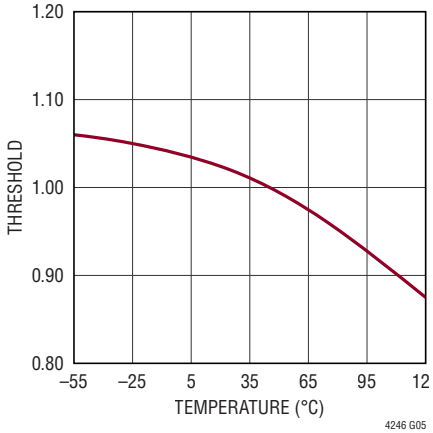
V_{IN} Leakage to V_{OUT} = 0V vs Temperature



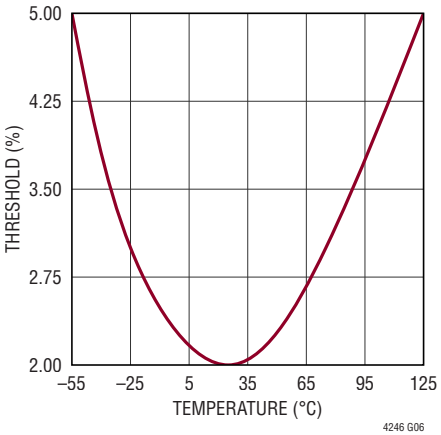
V_{OUT} Leakage vs Temperature



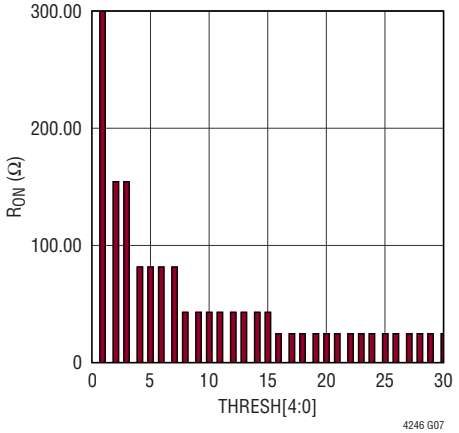
Circuit Breaker Threshold vs Temperature



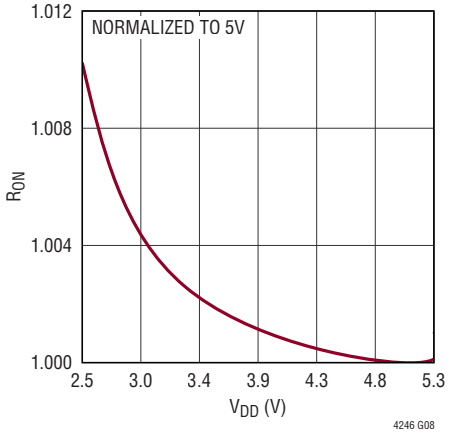
Circuit Breaker Threshold Matching



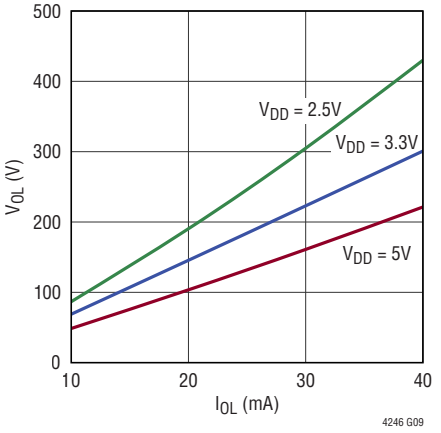
E_{CB} R_{ON} vs Threshold



E_{CB} R_{ON} vs V_{DD}



FAULT# Open Drain Output Impedance (V_{OL} vs I_{OL})



PIN FUNCTIONS

IN0 - IN7 (Pins 1 - 8): Individual Switch Inputs. Each switch is independent. However, each switch can have an affinity for any other switch or the FIN# input. Affinity allows all switches in a group to turn off if the overcurrent threshold of any one of them is exceeded. See Applications Information for more detail. If a channel is unused, tie the pin to GND.

V_{DD} (Pin 9): Bias Voltage Supply. V_{DD} is used to bias both internal analog and digital circuitry. Normal operation requires a voltage between 2.5V and 5.25V. V_{DD} is internally decoupled with 0.1µF – no additional bypass capacitor is required.

GND (Pin 10): Device Ground.

FIN# (Pin 11): Fault Input. FIN# provides an external option for channel affinity. If a channel is configured to have an affinity for the FIN# input, then the channel will become disabled if FIN# is driven low. This can be used as an asynchronous channel disable input or it can be driven by the FAULT# output of another LTC4246. If unused, tie to V_{DD}.

FAULT# (Pin 12): Fault Output. This open-drain output will pull low during a fault. The SPI serial bus can assign specific channels to drive the FAULT# output. Use a pullup resistor as necessary for this pin. If unused tie to GND.

OUT0 - OUT7 (Pins 13 - 20): Individual Switch Outputs. Each switch can be enabled and disabled individually, and each switch has an individual circuit breaker current threshold. If the switch current exceeds the circuit breaker threshold, the switch will turn off until it is reset via SPI. All switches default to off during power up. If a channel is unused, tie the pin to GND.

SDO (Pin 21): Serial Data Output. This pin can be used for daisy chaining many devices together or for reading back the data stored in a register for diagnostic purposes. The serial data is propagated on the falling edge of SCLK. Unlike many SPI interfaces, this product includes an internal 2.5µA pull-up on SDO that is active when CS# is high. When CS# is low, SDO is driven as a CMOS output. Note: this creates an upper bound on the maximum number of devices that can be used in non-daisy-chain configuration. When not used in a daisy-chain configuration, all SDO pins are tied together and any one SDO pin must be able to sink the combined pull-up currents.

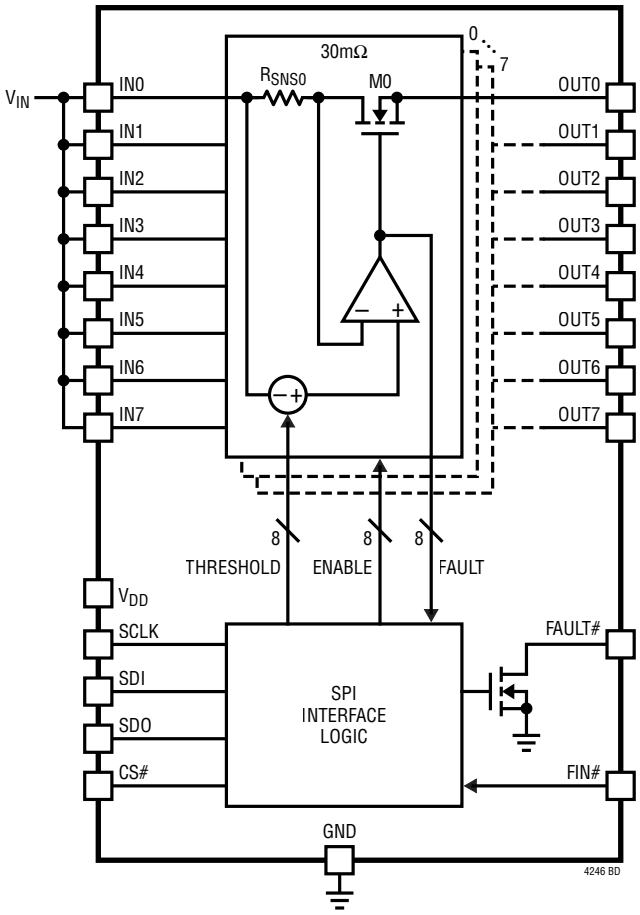
CS# (Pin 22): Active Low Chip Select Control Input. CS# selects the slave device with which the master intends to communicate. It also serves as the frame synchronization signal for the input data. When CS# is released high, the controller completes the current access and returns the controller to the ready state awaiting the next instruction. See the SPI Interface section for further details.

SCLK (Pin 23): Serial Clock Input. SCLK is the serial clock that synchronizes the slave device(s) to the master. SCLK is always driven by the master. Data is captured on the positive edge of SCLK. Data can be transferred at rates of up to 25MHz. For both master and slave devices, data will be valid before the rising edge of SCLK and meet the respective setup and hold times.

SDI (Pin 24): Serial Data Input. Data is captured on the positive edge of SCLK.

Exposed Pad (Pin 25): Ground. Must be connected to device ground.

BLOCK DIAGRAM



OPERATION

The LTC4246 provides fast electronic circuit breaker protection to loads connected to its eight output pins. The LTC4246 provides an SPI serial interface to enable, disable and configure the timing and current thresholds of each channel as well as provide status to each channels fault state. Low channel resistance minimizes the voltage drop across the device extending operation to low output voltage levels. The LTC4246 works for positive voltages in the range of 0V to 13.2V and provides programmable threshold currents of 0mA (commanded open) to 1500mA in 50mA steps. The LTC4246 SPI interface can be daisy-chain connected to extend the channel counts. Channels within a device can be grouped to trip if any of the single channels in a group trip. Additionally, the FIN# and FAULT# pins provide the capability to link multiple devices together such that channels in a device can respond to the fault state of another LTC4246. The LTC4246 contains internal V_{DD} decoupling capacitors and an SDO pullup resistor to eliminate the need for external components. The main functional circuits of the LTC4246 are illustrated in the Block Diagram.

The device powers up with all its channels disabled. Each channel's SPI registers must be configured to the desired threshold, affinity and timing setting. Channels can then be enabled simultaneously or individually through the ENABLE register. Once enabled, a switch takes <100µs to achieve the on state. During the first

OPERATION

100µs, the ECB function is disabled to eliminate the tripping due to inrush current of load capacitance. The input current is limited only by the LTC4246 switch on-resistance during the first 100µs. After the 100µs blanking period, the current in each channel is compared to the threshold value to determine the fault state. There are two measurements that occur each microsecond. The first is a gross short-circuit condition that occurs when the channel current is ~2× the set threshold for that channel. The 2× trip threshold can be disabled if desired in the respective channel's threshold register. The 2× overcurrent condition causes the channel to shut off in 1µs. The second condition that can trip the breaker for a channel is when the channel threshold current (1×) is met. In this case there are programmable response times of 10µs, 20µs, 50µs or 100µs. The programmable response times are intended to provide varying tolerance to transient peak currents to emulate the response behavior of a metallic fuse. This allows channel operation closer to the trip threshold without nuisance tripping of the ECB. Once a channel trips due to either the 1× or 2× threshold current, the channel is latched off and the respective fault status bit is set. If the channel is configured to drive the open-drain FAULT# pin, it will be driven low until the channel is reset. If the channel is given affinity to the FIN# pin, that channel will fault within 1µs of the FIN# going active low. The channel will turn off and its fault status will be reflected in the FAULT status register.

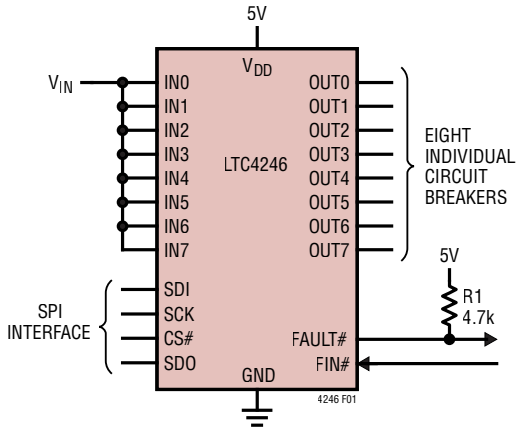


Figure 1. Typical Application

APPLICATIONS INFORMATION

RESET

The LTC4246 has three reset modes: Power-on Reset (POR), triggered when the V_{DD} voltage is below its POR threshold, and two soft reset modes, Soft Full Reset (Full) and Soft Quick Reset (Quick), controlled by the SPI interface. POR returns all registers to their default values. POR voltage thresholds for the V_{DD} pin are listed in the specification table. Both Full and Quick reset modes are invoked by writing a value to the RESET register (0x14) through the SPI interface. Full reset is invoked by writing the value 0x0D to the RESET register. This performs the same function as a power-on reset, including disabling all channels and resetting the value of the RESET register to 0x00. Quick reset is invoked by writing the value 0x50 to the RESET register. This value persists in the RESET register until changed, enabling the Quick reset mode. In Quick reset mode any channel fault can be cleared with a single write to the appropriate bits in the ENABLE register. When a fault occurs, the channel will turn off, the corresponding bit in the FAULT_REG register will assert, and the corresponding bit in the ENABLE register will go low. If configured, the FAULT# pin will go low for 500ns, then high again. Clear the fault and re-enable the channel by writing 1 to every enabled bit in the ENABLE register (0xFF to enable all channels). Exit Quick reset mode by writing 0x00 to the RESET register. Writing any value to the RESET register other than 0x50 or 0x0D has no effect, and the value remains in the register until changed.

APPLICATIONS INFORMATION

Table 1. Channel Current Threshold (mA) and R_{ON} (Ω) vs Threshold[4:0] Setting

CHANNEL 1× THRESHOLD CURRENT (mA)	CHANNEL 2× THRESHOLD CURRENT (mA)	THRESHOLD[4:0] SETTING	NOMINAL CHANNEL R_{ON} (Ω)	TYPICAL THRESHOLD CURRENT NOISE (mA-PP)
0	0	0x00	OPEN	
50	100	0x01	0.48	0.5
100	200	0x02	0.24	0.5
150	300	0x03	0.24	0.5
200	400	0x04	0.12	1
250	500	0x05	0.12	1
300	600	0x06	0.12	1
350	700	0x07	0.12	1
400	800	0x08	0.06	2.5
450	900	0x09	0.06	2.5
500	1000	0x0A	0.06	2.5
550	1100	0x0B	0.06	2.5
600	1200	0x0C	0.06	2.5
650	1300	0x0D	0.06	2.5
700	1400	0x0E	0.06	2.5
750	1500	0x0F	0.06	2.5
800	1600	0x10	0.03	5
850	1700	0x11	0.03	5
900	1800	0x12	0.03	5
950	1900	0x13	0.03	5
1000	2000	0x14	0.03	5
1050	2100	0x15	0.03	5
1100	2200	0x16	0.03	5
1150	2300	0x17	0.03	5
1200	2400	0x18	0.03	5
1250	2500	0x19	0.03	5
1300	2600	0x1A	0.03	5
1350	2700	0x1B	0.03	5
1400	2800	0x1C	0.03	5
1450	2900	0x1D	0.03	5
1500	3000	0x1E	0.03	5
No Limit	No Limit	0x1F	0.03	

AFFINITY

Each channel can respond to a fault on any other channel. This is called affinity, and a group of mutually responsive channels is an affinity group. Affinity supports applications such as paralleling multiple channels for higher circuit breaker currents, or grouping channels with related functions, such as force/sense connections as shown in Figure 5. When any channel within an affinity group, including the FIN# pin, if configured, enters a fault state all of the channels within that group will fault within 1µs and turn off. A channel with its THRESH[4:0] set to 0x1F (no current limit) will open if it has affinity with another channel that faults. Each channel has an affinity register, CHn_AFFINITY, that configures which other channels it will respond to. Each channel can also respond to the FIN# pin, allowing fault response between connected LTC4246 devices. Program one channel to listen to another by setting the bit for the other channel. For example, setting CH2_AFFINITY = 0x01 tells CH2 to respond to faults on CH0. Program a channel to listen to the FIN# pin by setting the FIN# bit in that channel's CHn_AFFINITY register. The FIN# bit is in the nth position in each CHn_AFFINITY register. Any or all of the bits can be set or cleared to define an affinity group. Affinity groups are mutual by default, meaning that setting one channel to listen to a second channel automatically sets the second channel to listen to the first. For example, setting bit 7 in CH0_AFFINITY (0x10; CH0 listens to CH7) will also automatically set bit 0 in CH7_AFFINITY (0x01; CH7 listens to CH0). It is possible, though not recommended, to unlink mutual affinity and create dependent affinity by subsequently clearing any bits that have been set automatically. When removing non-mutual behavior, it is recommended to first write all CHn_AFFINITY registers to 0x00 before making changes.

SPI Interface

The LTC4246 SPI serial interface provides access to sixteen 8-bit registers for configuration and status. The SPI interface pins are: Serial Data Input (SDI), Serial Data Output (SDO), Serial Clock (SCLK), and active low Chip Select (CS#). Each SPI command is one 16-bit word, consisting of an address byte and a data byte (Figure 1). Each SDI bit is defined on the rising of the SCLK pin, driven by the master. Each SDO bit changes on the falling edge of SCLK. A single command is framed between the falling and rising edges of the CS# pin. To initiate a

APPLICATIONS INFORMATION

transfer the SPI master lowers the CS# pin and sends a read/write bit followed by 7 bits of address and 8 bits of data on the SDI pin. The SPI master terminates the command by raising the CS# pin. A write transaction is a single word containing address and data (Figure 2a), during which the data returned on SDO is defined by the prior SPI command unrelated to the current one. A read command requires two transactions: one to request data, and a second transaction to retrieve the requested data (Figure 2b). After sending the 16-bit read command containing dummy (ignored) data, the SPI master initiates a second command during which the requested data comes out on the SDO pin. Because a read transaction uses two commands it may be interleaved by sending a second read or write command on SDI while the requested data is streaming out on SDO. A read command always returns 16 bits on SDO, of which the address portion is always 0x25. The rising CS# edge always latches a command, and any command not containing modulo 16 SCLK pulses (16, 32, ...) is ignored. 16-bit transactions are for parallel SPI operation. Longer blocks are used for daisy-chain operation.

Parallel Connected SPI

In the parallel connection mode, the CS# pin (driven low) is used to activate a single LTC4246 device which causes that devices SDO output driver to become active. If multiple LTC4246 devices are used, each has a unique CS# control line. When the CS# pin is high, the SDO output drive is limited to a weak 2.5µA pull-up current source to V_{DD}. This prevents an unselected parallel device from competing driving the common SDO data line. The SPI master (microcontroller, for example) drives the CS#, SCLK and SDI pins to shift a 16-bit command word (R/Wb, Address, Data) into the active device. When the CS# pin is driven high, the LTC4246 interprets the command. If the command is a write command (R/Wb bit low) the data word sent is loaded into the addressed register pointed to by the Address field of the command and the command is finished. If the command was a read command (R/Wb bit high), the LTC4246 loads its internal SPI shift register with the contents of the register pointed to by the address field of the command. The LTC4246 is now awaiting an additional CS# cycle to clock out the requested read reply word. The following CS# cycle clocks out the 16-bits read reply word, where the first 8 bits will always be 0x25 and the following 8-bits will be the data from the addressed register. After the 16-bits are clocked out, the CS# pin is returned high and the LTC4246 is ready for an additional command.

Daisy-Chain Connected SPI

Daisy chain connection is typically used for a large number of devices, as it only requires one CS# pin from the master and reduces board routing area for the SPI bus. The SPI master drives SCLK and CS# to all chips in the daisy chain, but it drives data only to SDI of the first LTC4246 in the chain and receives data only from SDO of the last LTC4246 in the chain. Each device in the chain drives the next one, SDO to SDI, just like a long shift register (Figure 3). Edges on the common CS# line frame transactions. When CS# is high each SDO pulls up with 2.5µA to V_{DD} to place a well defined logic 1 on its data line. In a daisy chain of length n devices, a single transaction is n • 16 bits long, containing n • 16 clocks between the falling and rising edges of CS#. Each device in the chain shifts data from SDI to SDO while CS# is low and latches the prior 16 bits when CS# rises. In this way a SPI master

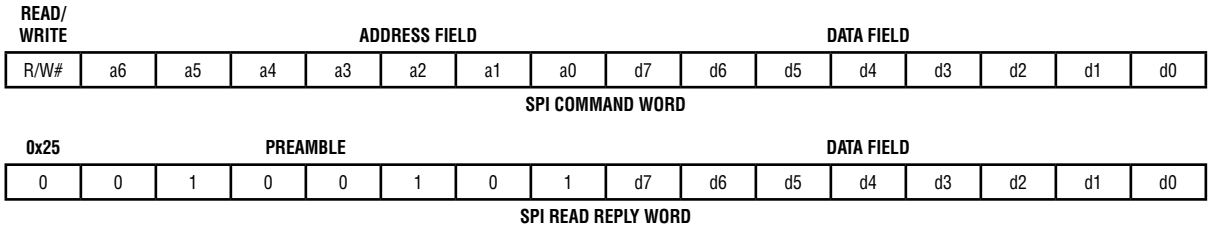


Figure 2. SPI Command Word and Read Reply Word

APPLICATIONS INFORMATION

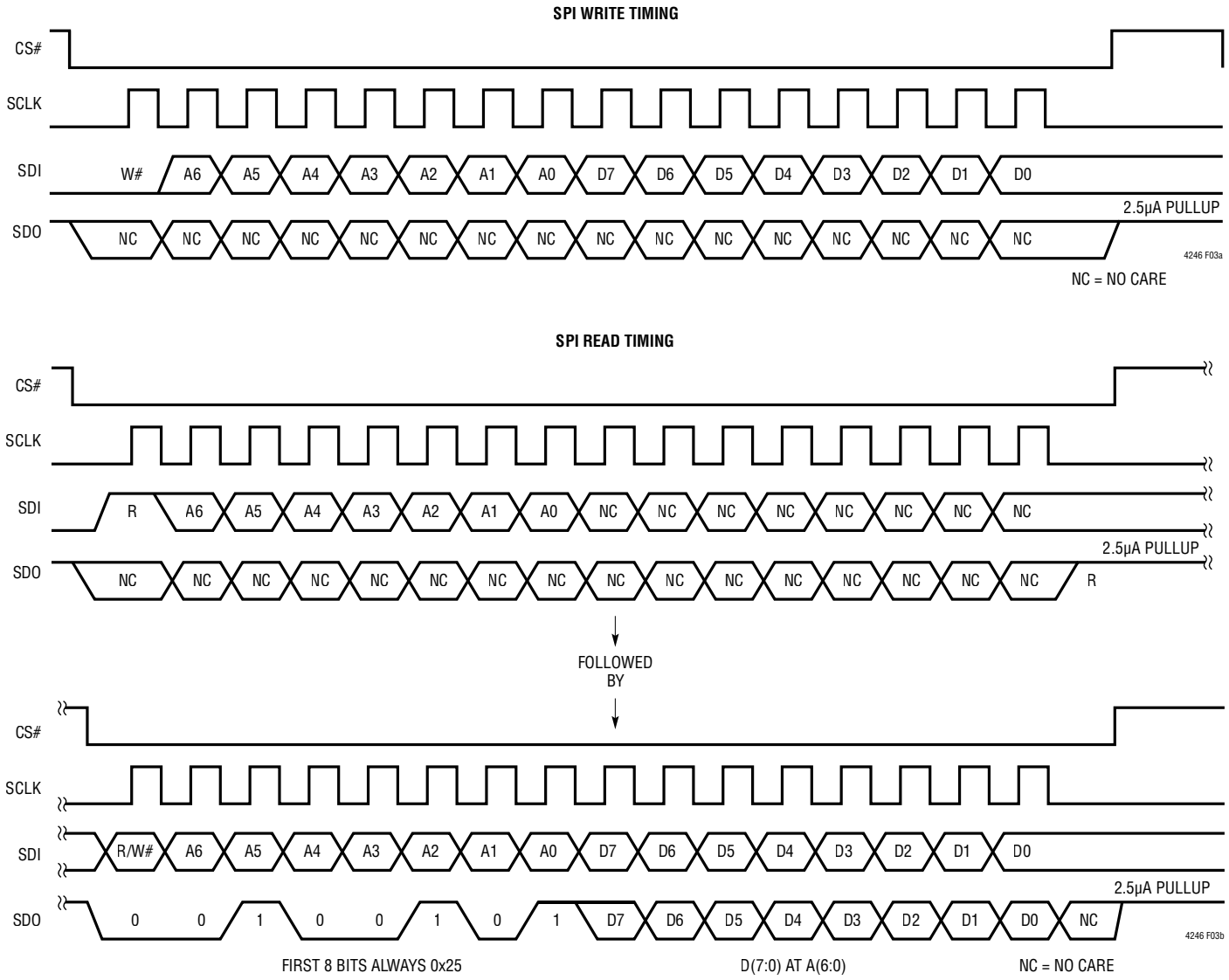
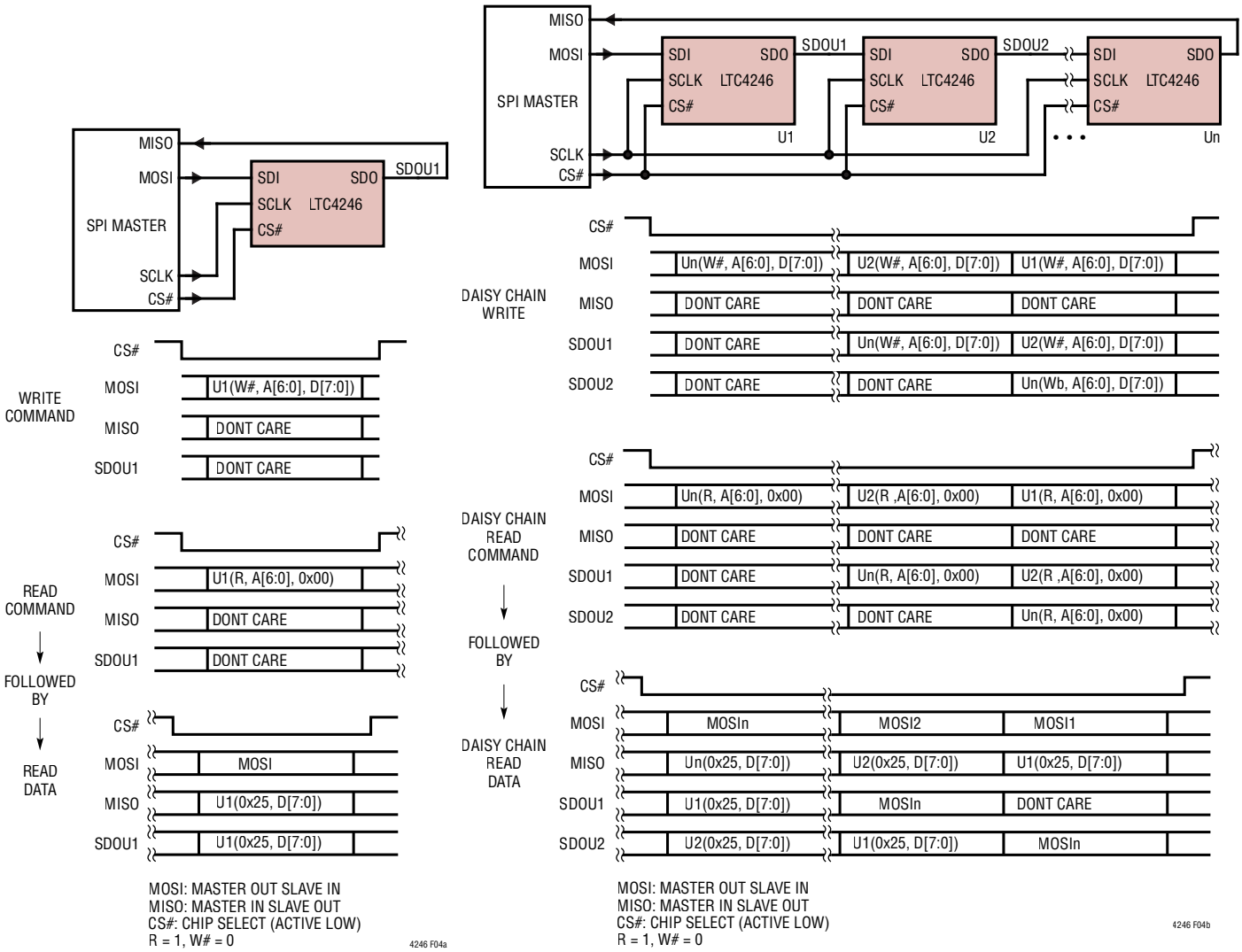


Figure 3. Register Write and Read Timing Diagram

can send and receive a long chain of words, one for each device in the daisy chain, while CS# is low (Figure 3). Only the master has awareness of the daisy chain length. Each LTC4246 in the chain behaves as it would in isolation or in parallel mode, shifting bits from SDI to SDO while CS# is low, and checking for modulo-16 byte transaction lengths when CS# rises. Write and Read behavior for each device is unchanged in a daisy-chain configuration. The NOOP command (address 0x00) is provided to simplify communication with a single device in the daisy chain. All other devices not participating may receive NOOP commands and will not respond.

APPLICATIONS INFORMATION



(a) SPI Mode **(b) SPI Daisy-Chain Mode**

Figure 4.

APPLICATIONS INFORMATION

Table 2. LTC4246 Register Address and Contents

REGISTER NAME	REGISTER ADDRESS	DESCRIPTION	READ/ WRITE	DATA LENGTH (BYTES)	DEFAULT VALUE
NO_OP	0x00	No Operation	R	1	0x00
ENABLE	0x01	Enable Channel Register	R/W	1	0x00
FAULT_PIN	0x02	Channels Fault Status Driving the FAULT# Pin	R/W	1	0xFF
FAULT_REG	0x03	Channels Fault State Status	R	1	0x00
CH0_THRESHOLD	0x04	Channel 0 Control Register	R/W	1	0x21
CH1_THRESHOLD	0x05	Channel 1 Control Register	R/W	1	0x21
CH2_THRESHOLD	0x06	Channel 2 Control Register	R/W	1	0x21
CH3_THRESHOLD	0x07	Channel 3 Control Register	R/W	1	0x21
CH4_THRESHOLD	0x08	Channel 4 Control Register	R/W	1	0x21
CH5_THRESHOLD	0x09	Channel 5 Control Register	R/W	1	0x21
CH6_THRESHOLD	0x0A	Channel 6 Control Register	R/W	1	0x21
CH7_THRESHOLD	0x0B	Channel 7 Control Register	R/W	1	0x21
CH0_AFFINITY	0x0C	Channel 0 Affinity Register	R/W	1	0x00
CH1_AFFINITY	0x0D	Channel 1 Affinity Register	R/W	1	0x00
CH2_AFFINITY	0x0E	Channel 2 Affinity Register	R/W	1	0x00
CH3_AFFINITY	0x0F	Channel 3 Affinity Register	R/W	1	0x00
CH4_AFFINITY	0x10	Channel 4 Affinity Register	R/W	1	0x00
CH5_AFFINITY	0x11	Channel 5 Affinity Register	R/W	1	0x00
CH6_AFFINITY	0x12	Channel 6 Affinity Register	R/W	1	0x00
CH7_AFFINITY	0x13	Channel 7 Affinity Register	R/W	1	0x00
RESET	0x14	Software Reset	R/W	1	0x00
REVID	0x15	Revision ID	R	1	0x13

REGISTER DETAILS: 8-CHANNEL ELECTRONIC CIRCUIT BREAKER

Table 3. NO_OP Register (0x00) – Read Only

BIT	NAME	DEFAULT	OPERATION
[7:0]	NO_OP	0x00	No operation, reads back 0x00.

Table 4. ENABLE Register (0x01) – Read Only

BIT	NAME	DEFAULT	OPERATION
7	EN_CH7	0	Enable bit for CH7. 1 = enable, 0 = disable.
6	EN_CH6	0	Enable bit for CH6. 1 = enable, 0 = disable.
5	EN_CH5	0	Enable bit for CH5. 1 = enable, 0 = disable.
4	EN_CH4	0	Enable bit for CH4. 1 = enable, 0 = disable.
3	EN_CH3	0	Enable bit for CH3. 1 = enable, 0 = disable.
2	EN_CH2	0	Enable bit for CH2. 1 = enable, 0 = disable.
1	EN_CH1	0	Enable bit for CH1. 1 = enable, 0 = disable.
0	EN_CH0	0	Enable bit for CH0. 1 = enable, 0 = disable.

Table 5. FAULT_PIN Register (0x02) – Read/Write

BIT	NAME	DEFAULT	OPERATION
7	FLT_CH7_EN	1	Channel 7 FAULT state drives FAULT#, 1 = enable, 0 = disable.
6	FLT_CH6_EN	1	Channel 6 FAULT state drives FAULT#, 1 = enable, 0 = disable.
5	FLT_CH5_EN	1	Channel 5 FAULT state drives FAULT#, 1 = enable, 0 = disable.
4	FLT_CH4_EN	1	Channel 4 FAULT state drives FAULT#, 1 = enable, 0 = disable.
3	FLT_CH3_EN	1	Channel 3 FAULT state drives FAULT#, 1 = enable, 0 = disable.
2	FLT_CH2_EN	1	Channel 2 FAULT state drives FAULT#, 1 = enable, 0 = disable.
1	FLT_CH1_EN	1	Channel 1 FAULT state drives FAULT#, 1 = enable, 0 = disable.
0	FLT_CH0_EN	1	Channel 0 FAULT state drives FAULT#, 1 = enable, 0 = disable.

Table 6. FAULT_REG (0x03) - Read/Write

BIT	NAME	DEFAULT	OPERATION
7	FLT_CH7_OUT	0	Channel 7 FAULT status, 1 = fault condition.
6	FLT_CH6_OUT	0	Channel 6 FAULT status, 1 = fault condition.
5	FLT_CH5_OUT	0	Channel 5 FAULT status, 1 = fault condition.
4	FLT_CH4_OUT	0	Channel 4 FAULT status, 1 = fault condition.
3	FLT_CH3_OUT	0	Channel 3 FAULT status, 1 = fault condition.
2	FLT_CH2_OUT	0	Channel 2 FAULT status, 1 = fault condition.
1	FLT_CH1_OUT	0	Channel 1 FAULT status, 1 = fault condition.
0	FLT_CH0_OUT	0	Channel 0 FAULT status, 1 = fault condition.

REGISTER DETAILS: 8-CHANNEL ELECTRONIC CIRCUIT BREAKER

Table 7. CHn_THRESHOLD Registers (0x04 through 0x0B) – Read/Write

BIT	NAME	DEFAULT	OPERATION
[7:6]	CHn_OCP_TIMER	00	ECB filter time. b00 = 10µs, b01 = 20µs, b10 = 50µs, b11 = 100µs
5	CHn_2X_OCP_EN	1	FAST 2x ECB. When enabled, a fault will be detected if the channel current exceeds twice the ECB threshold for 1µs.
[4:0]	THRESHOLD_CHn	00001	CHn ECB current threshold. The ECB current threshold can be set from 0mA (b00000) to 1500mA (b11110) in 50mA steps or the ECB can be disabled completely (b11111) yielding an always-on condition.

Table 8. CH0_AFFINITY Register (0x0C) – Read/Write

BIT	NAME	DEFAULT	OPERATION
7	ACH0_CH7	0	CH0 to CH7 affinity. If enabled, a fault on CH7 will disable CH0.
6	ACH0_CH6	0	CH0 to CH6 affinity. If enabled, a fault on CH6 will disable CH0.
5	ACH0_CH5	0	CH0 to CH5 affinity. If enabled, a fault on CH5 will disable CH0.
4	ACH0_CH4	0	CH0 to CH4 affinity. If enabled, a fault on CH4 will disable CH0.
3	ACH0_CH3	0	CH0 to CH3 affinity. If enabled, a fault on CH3 will disable CH0.
2	ACH0_CH2	0	CH0 to CH2 affinity. If enabled, a fault on CH2 will disable CH0.
1	ACH0_CH1	0	CH0 to CH1 affinity. If enabled, a fault on CH1 will disable CH0.
0	ACH0_FIN#	0	CH0 to FIN# affinity. If enabled, a FIN# falling edge will disable CH0.

Table 9. CH1_AFFINITY Register (0x0D) – Read/Write

BIT	NAME	DEFAULT	OPERATION
7	ACH1_CH7	0	CH1 to CH7 affinity. If enabled, a fault on CH7 will disable CH1.
6	ACH1_CH6	0	CH1 to CH6 affinity. If enabled, a fault on CH6 will disable CH1.
5	ACH1_CH5	0	CH1 to CH5 affinity. If enabled, a fault on CH5 will disable CH1.
4	ACH1_CH4	0	CH1 to CH4 affinity. If enabled, a fault on CH4 will disable CH1.
3	ACH1_CH3	0	CH1 to CH3 affinity. If enabled, a fault on CH3 will disable CH1.
2	ACH1_CH2	0	CH1 to CH2 affinity. If enabled, a fault on CH2 will disable CH1.
1	ACH1_FIN#	0	CH1 to FIN# affinity. If enabled, a FIN# falling edge will disable CH1.
0	ACH1_CH0	0	CH1 to CH0 affinity. If enabled, a fault on CH0 will disable CH1.

Table 10. CH2_AFFINITY Register (0x0E) – Read/Write

BIT	NAME	DEFAULT	OPERATION
7	ACH2_CH7	0	CH2 to CH7 affinity. If enabled, a fault on CH7 will disable CH2.
6	ACH2_CH6	0	CH2 to CH6 affinity. If enabled, a fault on CH6 will disable CH2.
5	ACH2_CH5	0	CH2 to CH5 affinity. If enabled, a fault on CH5 will disable CH2.
4	ACH2_CH4	0	CH2 to CH4 affinity. If enabled, a fault on CH4 will disable CH2.
3	ACH2_CH3	0	CH2 to CH3 affinity. If enabled, a fault on CH3 will disable CH2.
2	ACH2_FIN#	0	CH2 to FIN# affinity. If enabled, a FIN# falling edge will disable CH2.
1	ACH2_CH1	0	CH2 to CH1 affinity. If enabled, a fault on CH1 will disable CH2.
0	ACH2_CH0	0	CH2 to CH0 affinity. If enabled, a fault on CH0 will disable CH2.

REGISTER DETAILS: 8-CHANNEL ELECTRONIC CIRCUIT BREAKER

Table 11. CH3_AFFINITY Register (0x0F) – Read/Write

BIT	NAME	DEFAULT	OPERATION
7	ACH3_CH7	0	CH3 to CH7 affinity. If enabled, a fault on CH8 will disable CH3.
6	ACH3_CH6	0	CH3 to CH6 affinity. If enabled, a fault on CH7 will disable CH3.
5	ACH3_CH5	0	CH3 to CH5 affinity. If enabled, a fault on CH6 will disable CH3.
4	ACH3_CH4	0	CH3 to CH4 affinity. If enabled, a fault on CH5 will disable CH3.
3	ACH3_FIN#	0	CH3 to FIN# affinity. If enabled, a FIN# falling edge will disable CH3.
2	ACH3_CH2	0	CH3 to CH2 affinity. If enabled, a fault on CH2 will disable CH3.
1	ACH3_CH1	0	CH3 to CH1 affinity. If enabled, a fault on CH1 will disable CH3.
0	ACH3_CH0	0	CH3 to CH0 affinity. If enabled, a fault on CH0 will disable CH3.

Table 12. CH4_AFFINITY Register (0x10) – Read/Write

BIT	NAME	DEFAULT	OPERATION
7	ACH4_CH7	0	CH4 to CH7 affinity. If enabled, a fault on CH8 will disable CH4.
6	ACH4_CH6	0	CH4 to CH6 affinity. If enabled, a fault on CH7 will disable CH4.
5	ACH4_CH5	0	CH4 to CH5 affinity. If enabled, a fault on CH6 will disable CH4.
4	ACH4_FIN#	0	CH4 to FIN# affinity. If enabled, a FIN# falling edge will disable CH4.
3	ACH4_CH3	0	CH4 to CH3 affinity. If enabled, a fault on CH3 will disable CH4.
2	ACH4_CH2	0	CH4 to CH2 affinity. If enabled, a fault on CH2 will disable CH4.
1	ACH4_CH1	0	CH4 to CH1 affinity. If enabled, a fault on CH1 will disable CH4.
0	ACH4_CH0	0	CH4 to CH0 affinity. If enabled, a fault on CH0 will disable CH4.

Table 13. CH5_AFFINITY Register (0x11) – Read/Write

BIT	NAME	DEFAULT	OPERATION
7	ACH5_CH7	0	CH5 to CH7 affinity. If enabled, a fault on CH7 will disable CH5.
6	ACH5_CH6	0	CH5 to CH6 affinity. If enabled, a fault on CH6 will disable CH5.
5	ACH5_FIN#	0	CH5 to FIN# affinity. If enabled, a FIN# falling edge will disable CH5.
4	ACH5_CH4	0	CH5 to CH4 affinity. If enabled, a fault on CH4 will disable CH5.
3	ACH5_CH3	0	CH5 to CH3 affinity. If enabled, a fault on CH3 will disable CH5.
2	ACH5_CH2	0	CH5 to CH2 affinity. If enabled, a fault on CH2 will disable CH5.
1	ACH5_CH1	0	CH5 to CH1 affinity. If enabled, a fault on CH1 will disable CH5.
0	ACH5_CH0	0	CH5 to CH0 affinity. If enabled, a fault on CH0 will disable CH5.

REGISTER DETAILS: 8-CHANNEL ELECTRONIC CIRCUIT BREAKER

Table 14. CH6_AFFINITY Register (0x12) – Read/Write

BIT	NAME	DEFAULT	OPERATION
7	ACH6_CH7	0	CH6 to CH7 affinity. If enabled, a fault on CH7 will disable CH6.
6	ACH6_FIN#	0	CH6 to FIN# affinity. If enabled, a FIN# falling edge will disable CH6.
5	ACH6_CH5	0	CH6 to CH5 affinity. If enabled, a fault on CH5 will disable CH6.
4	ACH6_CH4	0	CH6 to CH4 affinity. If enabled, a fault on CH4 will disable CH6.
3	ACH6_CH3	0	CH6 to CH3 affinity. If enabled, a fault on CH3 will disable CH6.
2	ACH6_CH2	0	CH6 to CH2 affinity. If enabled, a fault on CH2 will disable CH6.
1	ACH6_CH1	0	CH6 to CH1 affinity. If enabled, a fault on CH1 will disable CH6.
0	ACH6_CH0	0	CH6 to CH0 affinity. If enabled, a fault on CH0 will disable CH6.

Table 15. CH7_AFFINITY Register (0x13) – Read/Write

BIT	NAME	DEFAULT	OPERATION
7	ACH7_FIN#	0	CH7 to FIN# affinity. If enabled, a FIN# falling edge will disable CH7.
6	ACH7_CH6	0	CH7 to CH6 affinity. If enabled, a fault on CH6 will disable CH7.
5	ACH7_CH5	0	CH7 to CH5 affinity. If enabled, a fault on CH5 will disable CH7.
4	ACH7_CH4	0	CH7 to CH4 affinity. If enabled, a fault on CH4 will disable CH7.
3	ACH7_CH3	0	CH7 to CH3 affinity. If enabled, a fault on CH3 will disable CH7.
2	ACH7_CH2	0	CH7 to CH2 affinity. If enabled, a fault on CH2 will disable CH7.
1	ACH7_CH1	0	CH7 to CH1 affinity. If enabled, a fault on CH1 will disable CH7.
0	ACH7_CH0	0	CH7 to CH0 affinity. If enabled, a fault on CH0 will disable CH7.

Table 16. RESET Register (0x14) – Read/Write

BIT	NAME	DEFAULT	OPERATION
[7:0]	RESET	0x00	Software Reset.
			Writing 0x0D will reset the LTC4246 to its default state. Self-clearing.
			Writing 0x50 will reset the LTC4246 Channel Fault Status register. Not self-clearing.

Table 17. (0x15) – Read Only

BIT	NAME	DEFAULT	OPERATION
[7:0]	REVID	0x13	Revision ID = 0x13.

DESIGN EXAMPLES

Electronic Circuit Breakers (ECB) are commonly used to protect a common power supply powering several loads in the event of a load failure. The ECB can provide feedback of the fault state back to the host processor which can attempt to resolve the condition or report and log the fault. The fast response time of the LTC4246 is valuable in protecting both the power supply and the downstream load from damage in the case that the fault condition is temporary or infrequent and can be valuable as a troubleshooting aid. A common application is where a system is comprised of several similar loads operating from a single power supply. If one of the loads is faulty, the system can still operate in a reduced state preventing the failed load from compromising the common power supply. The application in Figure 5 is an example of this case.

Figure 5 shows an automated test equipment application where the LTC4246 protects the wafer probe pins from excessive current if a tested device is shorted. In this application all eight channels of the device are sourced from the same power supply. It is possible to use several LTC4246 devices to increase channel count in this application. The FAULT# pin indicates to the controller if a fault occurs, and a SPI read indicates which channel. The fast response time of the LTC4246 can protect the probe needle in the case of a shorted load. The power supply can continue to power the remaining circuits in the presence of some shorts.

Figure 6 illustrates an application protecting a four wire power supply. In this application the LTC4246 is configured for channels 0 through 5 to have mutual affinity. If an overcurrent condition exists in the load, all six of the channels simultaneously open, disconnecting the source and Kelvin sense lines from the load. Channel pairs 0,1 and 4,5 share current to effectively double the trip threshold programmed in the registers. If unequal current sharing exists among the channel pairs, the channel with the lowest threshold determines the threshold for all channels in the application. R_{ON} matching is dominated by differences in the package resistance for the channels. Table 18 lists typical channel matching. Picking adjacent channels to share current is favorable due to R_{ON} matching. If power loss is not critical, some external resistive ballasting can be used to balance channel current sharing. R_{ON} increases for lower current threshold settings which offers better current sharing.

Table 18. Typical R_{ON} at 25°C for Channels 0 - 7

CHANNEL	R_{ON}, THRESH[4:0]≥0x10
0	27
1	27.6
2	26.2
3	25.5
4	25.2
5	25.9
6	27
7	27

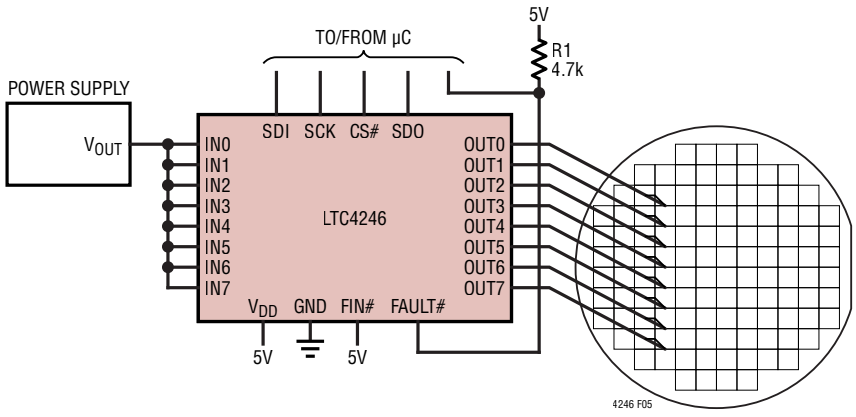


Figure 5. Automatic Test Equipment Probe Needle Protection

DESIGN EXAMPLES

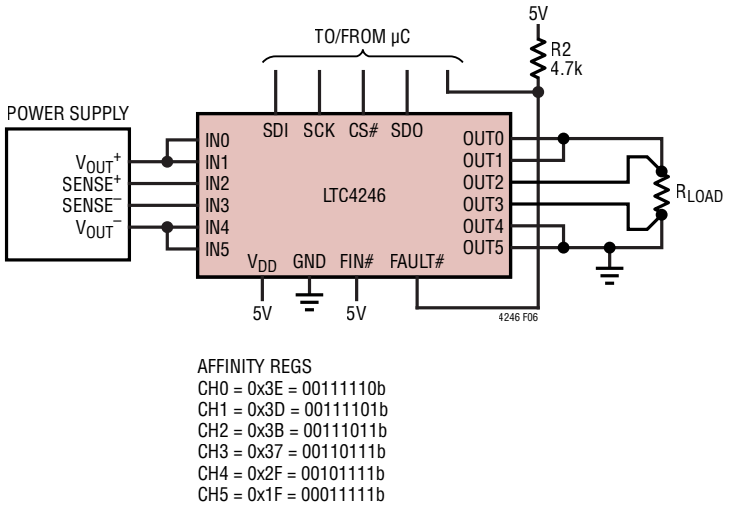


Figure 6. Using AFFINITY in a High Current Kelvin Sense Application

Figure 7 demonstrates an example use case for the FIN pin. In this application two four-wire power supplies are protected across two LTC4246 devices. The affinity of each channel includes the FIN pin so that if either power supply faults, all 12 channels will open isolating R_{LOAD1} and R_{LOAD2} from their respective power supplies. This application also demonstrates the wiring of a daisy-chain configuration where both devices share a common CS# line from the host processor. The FAULT# pin signals to the controller, which then sends a daisy-chain read command to both devices to determine the source of the fault, and a write command to re-enable both devices simultaneously.

Figure 8 illustrates a method using two channels to provide reverse isolation. The main switch of the LTC4246 has a parasitic diode with the cathode tied to INn and the anode tied to OUTn. If the INn voltage is always more positive than the OUTn terminal, then reverse isolation is not necessary. In the case where OUTn can exceed INn, using two channels in series can ensure one of the two series channels parasitic diodes is always reverse biased. The two series channels are enabled simultaneously and the two are linked with mutual affinity so that when one channel opens due to an overcurrent condition, both are turned off. The R_{ON} in this configuration is doubled from the series connection.

When changing from Power Supply 1 to Power Supply 2, the ENABLE register can be changed from 0x03 to 0x0C without an intermediate setting to 0x00 due to the break before make operation of the switches. The switches turn off within 5µs and require 25µs to enable so there is no simultaneous connection between the two supplies.

DESIGN EXAMPLES

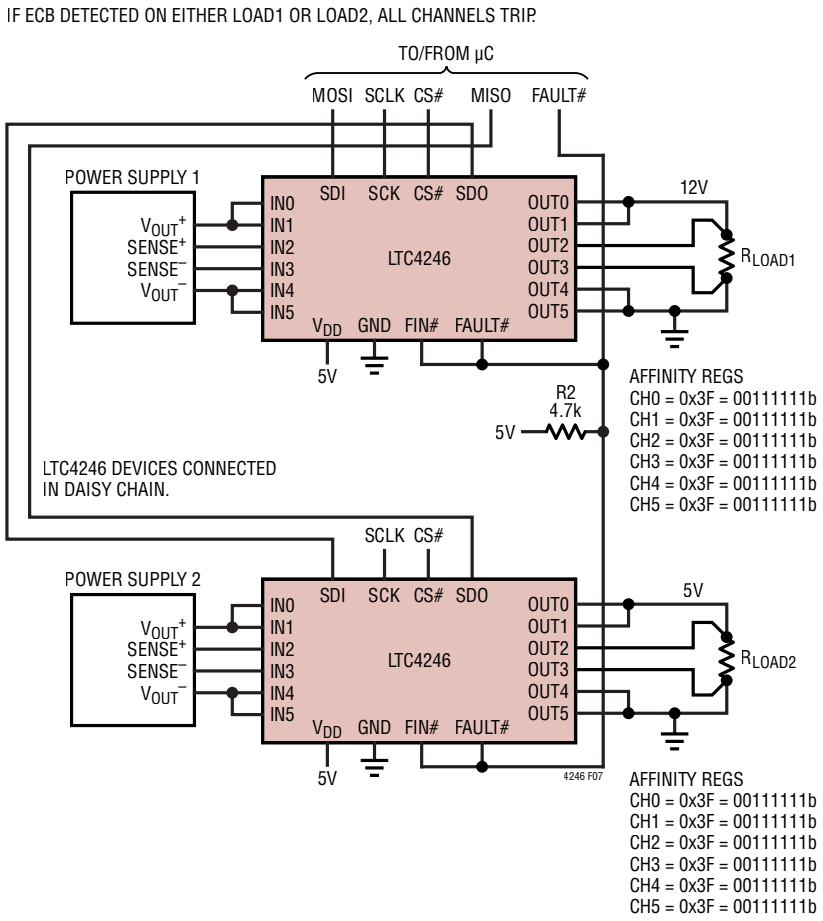


Figure 7. Using AFFINITY Across Multiple Devices Connected in Daisy Chain

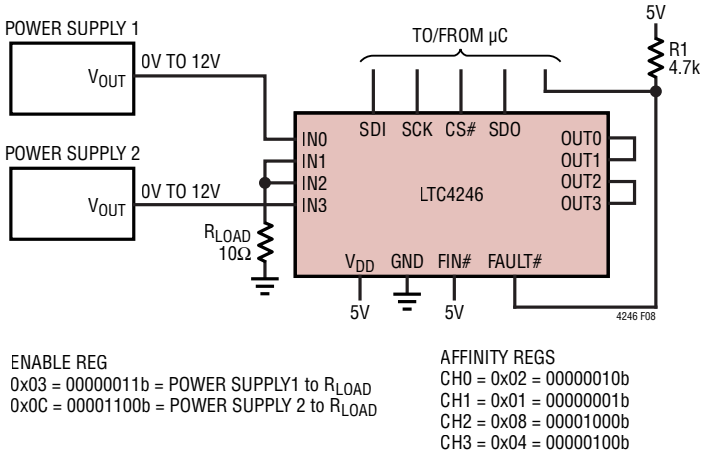
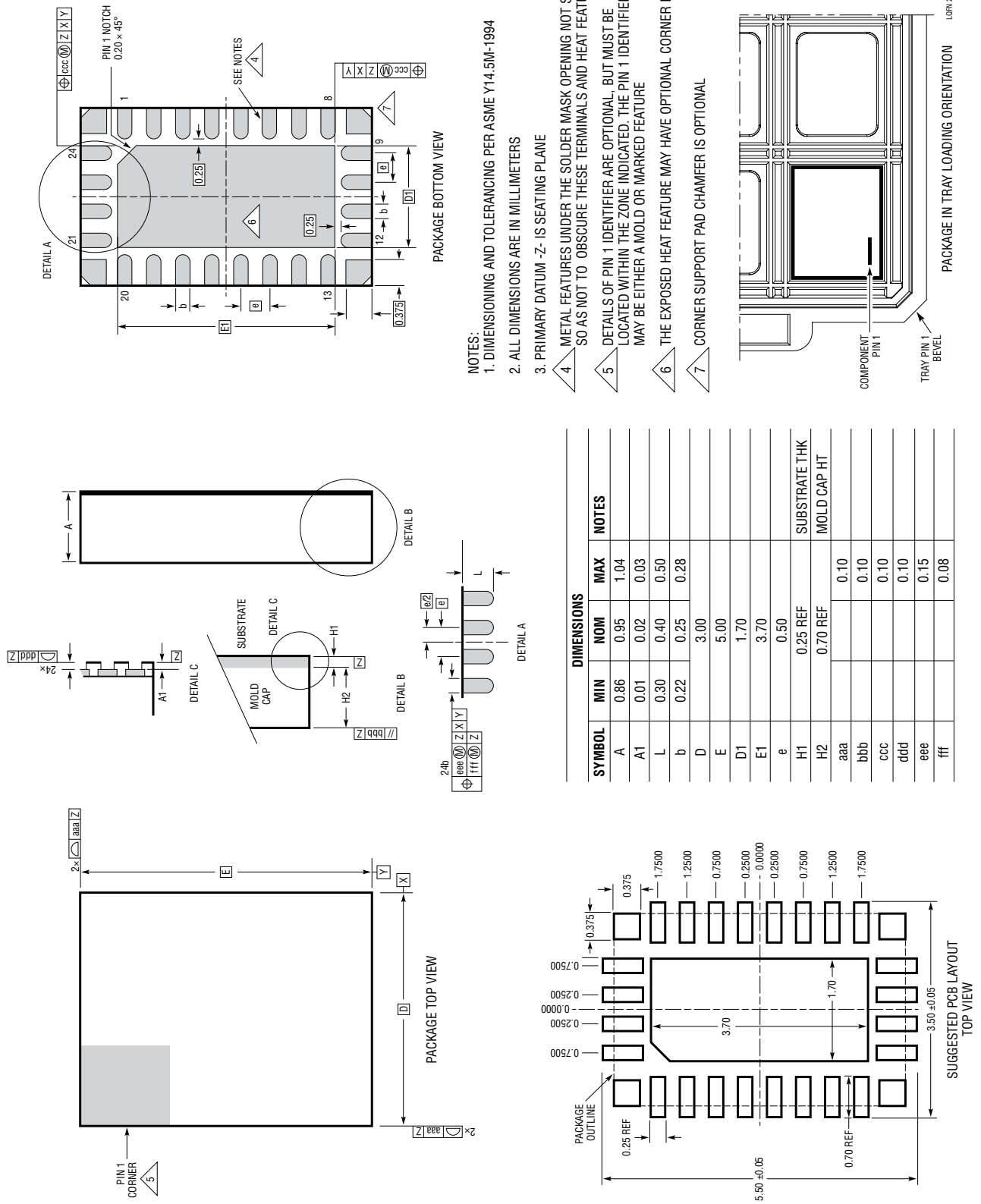


Figure 8. Implementing Reverse Isolation

PACKAGE DESCRIPTION

LQFN Package
24-Lead (3mm × 5mm × 0.95mm)
(Reference LTC DWG # 05-08-1687 Rev Ø)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.86	0.95	1.04	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		3.00		
E		5.00		
D1		1.70		
E1		3.70		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

TYPICAL APPLICATION

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4213	No R_{SENSE} Electronic Circuit Breaker	0V to 6V, 1µs Response Time, External NMOS Switch, 3mm × 2mm DFN Package
ADGS1412	SPI Interface, 1.5Ω R_{ON}, ±15V/+12V QUAD SPST Switch, MUX Configurable	V_{SS} to V_{DD} Analog Signal Range, 1.8V Logic Compatibility, 24-Lead LFCSP
ADGS1612	SPI Interface, 1Ω R_{ON}, ±5V, 12V, 5V, 3.3V, MUX Configurable, QUAD SPST Switch	V_{SS} to V_{DD} Analog Signal Range, 1.8V Logic Compatibility, 4mm × 4mm 24-Lead LFCSP Package
LTC4368	100V UVLO and Reverse Protection Controller with Bidirectional Circuit Breaker	+50mV Forward Sense Threshold, ±1.5% UV and OV Thresholds, 5µA Shutdown Current, 10-Pin MSOP and 3mm × 3mm DFN Packages
LTC7000	Fast 150V Protected High Side NMOS Static Switch Driver	3.5V to 135V, Adjustable Trip Threshold, Current Monitor Output, Auto Retry Timer, Adjustable Turn-On Slew Rate, 16-lead MSOP Package
LTC4224	Compact Dual Low Voltage Hot Swap Controller	1V to 6V, Adjustable Current limit, Limits Peak Fault Current in ≤1µs, 10-Lead MSOP and 3mm × 2mm DFN Packages
LTC4210	Hot Swap Controller in 6-Lead SOT-23 Package	Adjustable Current Limit with Circuit Breaker, 2.7V to 7V, Fast Response Limits Peak Fault Current, High Side Drive for External MOSFET Switch
ADP196	5V, 3A Logic Controlled High-Side Power Switch	Low R_{DSON} 10mΩ (WLCSP) or 27mΩ (LFCSP), 1.8V to 5.5V, 3A Continuous Operating Current to 70°C, 1mm × 1.5mm WLCSP, 2mm × 2mm LFCSP
ADP194/ ADP195/ADP198	Logic Controlled High-Side Power Switch	80mΩ R_{DSON} at 1.8V, Low Input Voltage Range 1.1V to 3.6V, Ultrasmall 0.8mm × 0.8mm × 0.5mm WLCSP