LTC2063/LTC2064/LTC2065

2µA Supply Current, Low IB, Zero-Drift Operational Amplifiers

Features

- Low Supply Current: 2µA Maximum (per Amplifier)
- Offset Voltage: 5µV Maximum
- Offset Voltage Drift: 0.02µV/°C Maximum
- Input Bias Current:
  - 3pA Typical
  - 30pA Maximum, –40°C to 85°C
  - 100pA Maximum, –40°C to 125°C
- Integrated EMI Filter (114dB Rejection at 1.8GHz)
- Shutdown Current: 170nA Maximum (per Amplifier)
- Rail-to-Rail Input and Output
- 1.7V to 5.25V Operating Supply Range
- A\text{VOL}: 140dB Typical
- Low-Charge Power-Up for Duty Cycled Applications
- Specified Temperature Ranges:
  - –40°C to 85°C
  - –40°C to 125°C
- SC70, TSOT23, MS8, DFN10, TSSOP14 and QFN16 Packages

Applications

- Signal Conditioning in Wireless Mesh Networks
- Portable Instrumentation Systems
- Low-Power Sensor Conditioning
- Gas Detection
- Temperature Measurement
- Medical Instrumentation
- Energy Harvesting Applications
- Low Power Current Sensing

Description

The LTC\textsuperscript{2063}/LTC2064/LTC2065 are single, dual, and quad low power, zero-drift, 20kHz amplifiers. The LTC2063/LTC2064/LTC2065 enable high resolution measurement at extremely low power levels.

Typical supply current is 1.4µA per amplifier with a maximum of 2µA. The available shutdown mode has been optimized to minimize power consumption in duty-cycled applications and features low charge loss during power-up, reducing total system power.

The LTC2063/LTC2064/LTC2065’s self-calibrating circuitry results in very low input offset (5µV max) and offset drift (0.02µV/°C). The maximum input bias current is only 20pA and does not exceed 100pA over the full specified temperature range. The extremely low input bias current of the LTC2063/LTC2064/LTC2065 allows the use of high value power-saving resistors in the feedback network.

With its ultralow quiescent current and outstanding precision, the LTC2063/LTC2064/LTC2065 can serve as a signal chain building block in portable, energy harvesting and wireless sensor applications.

The LTC2063 is available in 6-lead SC70 and 5-lead TSOT23 packages. The LTC2064 is available in 8-lead MSOP and 10-lead DFN packages. The LTC2065 is available in 14-lead TSSOP and 16-lead 3mm × 3mm QFN packages. These devices are fully specified over the –40°C to 85°C and –40°C to 125°C temperature ranges.

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Typical Application

Micropower Precision Oxygen Sensor

Duty Cycle Lowers System Power

[Diagram showing a circuit diagram and a graph illustrating the duty cycle effect on system power.]

For more information www.analog.com
### Absolute Maximum Ratings

(Note 1)

- Total Supply Voltage (\(V^+\) to \(V^-\)) .............. 5.5V
- Differential Input Current (+IN to –IN) (Note 2) .... ±10mA
- Differential Input Voltage (+IN to –IN) .............. 5.5V
- Input Voltage +IN, –IN, SHDN \((V^-) – 0.3V to (V^+) + 0.3V\)
- Input Current +IN, –IN, SHDN (Note 2) ............ ±10mA
- Output Short-Circuit Duration (Note 3) ..... Thermally Limited

Operating and Specified Temperature Range (Note 4)

- LTC2063/LTC2064/LTC2065 ............ –40°C to 85°C
- LTC2063H/LTC2064H/LTC2065H ...... –40°C to 125°C
- Maximum Junction Temperature ...................... 150°C
- Storage Temperature Range ...................... –65°C to 150°C

### Pin Configuration

#### LTC2063

- **TOP VIEW**
  - +IN 1
  - V^- 2
  - –IN 3
  - 6 V^+
  - 5 SHDN
  - 4 OUT

- **SC6 PACKAGE**
  - 6-Lead Plastic SC70
  - \(\theta_J = 265^\circ°C/W\) (Note 5)

- **S5 PACKAGE**
  - 5-Lead Plastic TSOT-23
  - \(\theta_J = 215°C/W\) (Note 5)

#### LTC2064

- **TOP VIEW**
  - OUTA 1
  - –INA 2
  - +INA 3
  - \(V^- 4\)
  - 16 OUTB
  - 15 +INB

- **MS8 PACKAGE**
  - 8-Lead Plastic MSOP
  - \(\theta_J = 183°C/W, \theta_C = 40°C/C\) (Note 5)

#### LTC2065

- **TOP VIEW**
  - OUTA
  - –INA
  - +INA
  - \(V^+\)
  - OUTB
  - –INB
  - +INB
  - \(V^-\)

- **QFN16 PACKAGE**
  - 16-Lead (3mm × 3mm) Plastic QFN
  - \(\theta_J = 68°C/W\) (Note 5)

- **TSSOP14 PACKAGE**
  - 14-Lead Plastic TSSOP
  - \(\theta_J = 100°C/W\) (Note 5)

### Order Information

<table>
<thead>
<tr>
<th>TAPE AND REEL (MINI)</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
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<tr>
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<td>LTC2063ISC6#TRPBF</td>
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### ORDER INFORMATION

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<td>14-Lead TSSOP</td>
<td>–40°C to 125°C</td>
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Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Parts ending with PBF are RoHS and WEEE compliant. Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

### ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25°C \). Unless otherwise noted, \( V_S = 1.8V \), \( V_{CM} = V_{OUT} = V_S/2 \), \( V_{SHDN} = 1.8V \), \( R_L \) to \( V_S/2 \).

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage (Note 6)</td>
<td>( V_S = 1.7V )</td>
<td>1</td>
<td>±5</td>
<td>±10</td>
<td>( \mu V )</td>
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<tr>
<td>( \Delta V_{OS}/\Delta T )</td>
<td>Input Offset Voltage Drift (Note 6)</td>
<td>( –40°C ) to ( 85°C )</td>
<td>●</td>
<td>±0.03</td>
<td>±0.06</td>
<td>( \mu V/°C )</td>
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<td>( I_B )</td>
<td>Input Bias Current (Note 7)</td>
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<td>0.5</td>
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<td>pA</td>
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<td>( I_{OS} )</td>
<td>Input Offset Current (Note 7)</td>
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<td>pA</td>
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<td>( I_n )</td>
<td>Input Noise Current Spectral Density</td>
<td>( f \leq 100Hz )</td>
<td>12</td>
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<td></td>
<td>fA/√Hz</td>
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<td>Input Noise Voltage Spectral Density</td>
<td>( f \leq 100Hz )</td>
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<td>( e_n )</td>
<td>Input Noise Voltage</td>
<td>DC to 10Hz</td>
<td>4.8</td>
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<td></td>
<td>( \mu V_{P-P} )</td>
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<td>( C_{IN} )</td>
<td>Input Capacitance</td>
<td>Differential Common Mode</td>
<td>3.3</td>
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<td></td>
<td>( \mu F )</td>
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<tr>
<td>( V_{CMR} )</td>
<td>Input Voltage Range</td>
<td>Guaranteed by CMRR</td>
<td>(( V^– )) – 0.1</td>
<td>(( V^+ )) + 0.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( CMRR )</td>
<td>Common Mode Rejection Ratio (Note 8)</td>
<td>( V_{CM} = (V^–) – 0.1V ) to ( (V^+) + 0.1V ) ( R_L = 499k )</td>
<td>103</td>
<td>130</td>
<td></td>
<td>dB</td>
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<tr>
<td>( PSRR )</td>
<td>Power Supply Rejection Ratio</td>
<td>( V_S = 1.7V ) to 5.25V ( R_L = 499k )</td>
<td>108</td>
<td>126</td>
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<td>dB</td>
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<tr>
<td>( A_{VOL} )</td>
<td>Open Loop Gain</td>
<td>( V_{OUT} = (V^–) + 0.1V ) to ( (V^+) – 0.1V ), ( R_L = 499k )</td>
<td>135</td>
<td></td>
<td></td>
<td>dB</td>
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<td>( V_{OL} )</td>
<td>Output Voltage Swing Low ( (V_{OUT} – V^–) )</td>
<td>( R_L = 499k )</td>
<td>0.05</td>
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<td>( R_L = 10k )</td>
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<td>( V_{OH} )</td>
<td>Output Voltage Swing High ( (V^– – V_{OUT}) )</td>
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<td></td>
<td>mV</td>
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<tr>
<td></td>
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<td>( R_L = 10k )</td>
<td>4.5</td>
<td>10</td>
<td>50</td>
<td>mV</td>
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<tr>
<td>( I_{SC} )</td>
<td>Output Short Circuit Current</td>
<td>Sourcing</td>
<td>5.8</td>
<td>5.6</td>
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<td>mA</td>
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<tr>
<td></td>
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<td>Sinking</td>
<td>10.4</td>
<td>5</td>
<td>13</td>
<td>mA</td>
</tr>
</tbody>
</table>

For more information: www.analog.com
**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ C \). Unless otherwise noted, \( V_S = 1.8V \), \( V_{CM} = V_{OUT} = V_S/2 \), \( V_{SHDN} = 1.8V \), \( R_L \) to \( V_S/2 \).

### SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS
--- | --- | --- | --- | --- | --- | ---
SR | Slew Rate | \( A_V = 1 \) | 3.5 & | | | V/ms
GBW | Gain Bandwidth Product | \( R_L = 499k \) | 20 & | | | kHz
IG | Power-Up Time | | 2 & | | | ms
FC | Internal Chopping Frequency | | 5 & | | | kHz
VS | Supply Voltage Range | Guaranteed by PSRR | ● & | 1.7 | 5.25 | V
IS | Supply Current per Amplifier | No Load \(-40^\circ C \) to \( 85^\circ C \) | | | | μA
| | | \(-40^\circ C \) to \( 125^\circ C \) | | | | μA
| | In Shutdown (\( SHDN = V^- \)) \(-40^\circ C \) to \( 85^\circ C \) | 90 & | | | nA
| | | \(-40^\circ C \) to \( 125^\circ C \) | | | | nA
VH | SHDN Pin Threshold, Logic High (Referred to \( V^- \)) | | ● & | 1.0 & | | V
VL | SHDN Pin Threshold, Logic Low (Referred to \( V^- \)) | | ● & | 0.65 & | | V
IH | SHDN Pin Current | \( V_{SHDN} = 0V \) | ● & | –150 | –20 | nA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ C \). Unless otherwise noted, \( V_S = 5V \), \( V_{CM} = V_{OUT} = V_S/2 \), \( V_{SHDN} = 5V \), \( R_L \) to \( V_S/2 \).

### SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS
--- | --- | --- | --- | --- | --- | ---
VOS | Input Offset Voltage (Note 6) | \( V_S = 5.25V \) | ● | 1 & | ±5 & | μV
\( \Delta VOS/\Delta T \) | Input Offset Voltage Drift (Note 6) | \(-40^\circ C \) to \( 85^\circ C \) | ● & | ±0.02 | | μV/°C
| | | \(-40^\circ C \) to \( 125^\circ C \) | ● | ±0.05 | | μV/°C
IB | Input Bias Current | \(-40^\circ C \) to \( 85^\circ C \) | ● & | –3 | | pA
| | | \(-40^\circ C \) to \( 125^\circ C \) | ● | ±30 | | pA
IO | Input Offset Current | \(-40^\circ C \) to \( 85^\circ C \) | ● & | 1.5 | | pA
| | | \(-40^\circ C \) to \( 125^\circ C \) | ● | ±100 | | pA
IN | Input Noise Current Spectral Density | \( f \leq 100Hz \) | 12 & | | | fA/√Hz
en | Input Noise Voltage Spectral Density | \( f \leq 100Hz \) | 220 & | | | nV/√Hz
enP–P | Input Noise Voltage | DC to 10Hz | 4.6 & | | | μV_{P–P}
CIN | Input Capacitance | Differential | 3.3 & | | | pF
| | | Common Mode | 3.5 & | | | pF
VCMR | Input Voltage Range | Guaranteed by CMRR | ● | (\( V^- \)) – 0.1 | (\( V^- \)) + 0.1 | V
CMRR | Common Mode Rejection Ratio | \( V_{CM} = (V^-) \) – 0.1V to (\( V^- \)) + 0.1V | 111 & | 130 | | dB
| | | \( R_L = 499k \) | 108 & | | | dB
PSRR | Power Supply Rejection Ratio | \( V_S = 1.7V \) to 5.25V | 108 & | 126 | | dB
| | | \( R_L = 499k \) | 106 & | | | dB
EMIRR | EMI Rejection Ratio | \( V_RF = 100mV_pk \) | 81 & | | | dB
| | | \( EMIRR = 20 \times \log(V_RF/\Delta V_OS) \) | 102 & | | | dB
| | | \( V_RF = 900mV_pk \) | 114 & | | | dB
| | | \( V_RF = 1800mHz \) | 100 & | | | dB
| | | \( V_RF = 2400mHz \) | | | | dB
AVOL | Open Loop Gain | \( V_{OUT} = (V^-) + 0.1V \) to (\( V^- \)) – 0.1V, \( R_L = 499k \) | ● | 112 | 140 | dB
### ELECTRICAL CHARACTERISTICS

The ⋄ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. Unless otherwise noted, $V_S = 5V$, $V_{CM} = V_{OUT} = V_S/2$, $V_{SHDN} = 5V$, $R_L$ to $V_S/2$.

<table>
<thead>
<tr>
<th>SYMBOL</th>
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<th>MIN</th>
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<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>$V_{OL}$</td>
<td>Output Voltage Swing Low ($V_{OUT} – V^-$)</td>
<td>$R_L = 499k$</td>
<td>0.1</td>
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<td></td>
<td>mV</td>
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<tr>
<td></td>
<td></td>
<td>$R_L = 10k$</td>
<td>⋄</td>
<td>5.5</td>
<td>15</td>
<td>mV</td>
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<td>$V_{OH}$</td>
<td>Output Voltage Swing High ($V^+ – V_{OUT}$)</td>
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<td>$V_S$</td>
<td>Supply Voltage Range</td>
<td>Guaranteed by PSRR</td>
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<td>$I_S$</td>
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<td>No Load</td>
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<td>$-40°C$ to $85°C$</td>
<td>⋄</td>
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<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40°C$ to $125°C$</td>
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<td>μA</td>
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<td>SHDN Pin Threshold, Logic High (Referred to $V^-$)</td>
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<td>V</td>
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<td>SHDN Pin Current</td>
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<td>⋄</td>
<td>−150</td>
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<td>nA</td>
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**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The inputs are protected by two series connected ESD protection diodes to each power supply. The input current should be limited to less than 10mA. The input voltage should not exceed 300mV beyond the power supply.

**Note 3:** A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

**Note 4:** The LTC2063/LTC2064/LTC2065 are guaranteed to meet specified performance from $-40°C$ to $85°C$. The LTC2063H/LTC2064H/LTC2065H are guaranteed to meet specified performance from $-40°C$ to $125°C$.

**Note 5:** Thermal resistance varies with the amount of PCB board metal connected to the package. The specified values are for short traces connected to the leads.

**Note 6:** These parameters are guaranteed by design. Thermocouple effects preclude measurements of these voltage levels during automated testing. $V_{OS}$ is measured to a limit determined by test equipment capability.

**Note 7:** Input bias current is only production tested at 5V. Input bias current at 1.8V is expected to meet or exceed 5V specifications.

**Note 8:** Minimum specifications for these parameters are limited by noise and the capabilities of the automated test system.
TYPICAL PERFORMANCE CHARACTERISTICS

Input Offset Voltage Distribution

Input Offset Voltage Distribution

Input Offset Voltage Drift Distribution

Input Offset Voltage Drift Distribution

Input Offset Voltage vs Input Common Mode Voltage

Input Offset Voltage vs Input Common Mode Voltage

Input Offset Voltage vs Supply Voltage

For more information www.analog.com
TYPICAL PERFORMANCE CHARACTERISTICS

Input Referred Voltage Noise Density

Input Referred Current Noise Density

EMI Rejection vs Frequency

Common Mode Rejection Ratio vs Frequency

Power Supply Rejection Ratio vs Frequency

Closed Loop Gain vs Frequency

Open Loop Gain and Phase vs Frequency

Open Loop Gain and Phase vs Frequency

For more information www.analog.com
TYPICAL PERFORMANCE CHARACTERISTICS

---

1. **Shutdown Transient with Sinusoidal Input**
   - For $V_S = 5V$ and $A_V = +1$

2. **Enable Transient with Sinusoidal Input**
   - For $V_S = 5V$ and $A_V = +1$

3. **Closed Loop Output Impedance vs Frequency**
   - $V_S = 5V$ and $A_V = +1$

4. **Output Impedance in Shutdown vs Frequency**
   - $V_S = 5V$ and $A_V = +1$

5. **LTC2064 Crosstalk vs Frequency**
   - $R_L = 10k$

---

For more information: [www.analog.com](http://www.analog.com)
TYPICAL PERFORMANCE CHARACTERISTICS

SHDN Pin Current vs Temperature

Shutdown Supply Current vs Supply Voltage

Shutdown Supply Current vs Temperature

Output Voltage Swing High vs Load Current

Output Voltage Swing Low vs Load Current

Output Voltage Swing Low vs Load Current

No Phase Reversal

Output Short Circuit Current vs Temperature

For more information www.analog.com
TYPICAL PERFORMANCE CHARACTERISTICS

Output Short Circuit Current vs Temperature

Large Signal Response

Large Signal Response

Small Signal Response

Small Signal Response

Small Signal Overshoot vs Load Capacitance

Positive Output Overload Recovery

Positive Output Overload Recovery
TYPICAL PERFORMANCE CHARACTERISTICS

Negative Output Overload Recovery

Positive Input Overload Recovery

Negative Input Overload Recovery

Negative Input Overload Recovery
PIN FUNCTIONS

**OUT**: Amplifier Output

**–IN**: Inverting Amplifier Input

**+IN**: Noninverting Amplifier Input

**V+**: Positive Power Supply. A bypass capacitor should be used between supply pins and ground.

**V–**: Negative Power Supply. A bypass capacitor should be used between supply pins and ground.

**SHDN**: Shutdown Control Pin. The SHDN pin threshold is referenced to V–. If tied to V+, the part is enabled. If tied to V–, the part is disabled and draws less than 170nA of supply current per amplifier. It is recommended to not float this pin.

BLOCK DIAGRAM

- Amplifier
- Shutdown Circuit
APPLICATIONS INFORMATION

Using the LTC2063/LTC2064/LTC2065

The LTC2063/LTC2064/LTC2065 are single, dual and quad zero-drift operational amplifiers with the open-loop voltage gain and bandwidth characteristics of a conventional operational amplifier. Advanced circuit techniques allow the LTC2063/LTC2064/LTC2065 to operate continuously through its entire bandwidth while self-calibrating unwanted errors.

Input Voltage Noise

Zero-drift amplifiers like the LTC2063/LTC2064/LTC2065 achieve low input offset voltage and 1/f noise by heterodyning DC and flicker noise to higher frequencies. In early zero-drift amplifiers, this process resulted in idle tones at the self-calibration frequency, often referred to as the chopping frequency. These artifacts made early zero-drift amplifiers difficult to use. The advanced circuit techniques used by the LTC2063/LTC2064/LTC2065 suppress these spurious artifacts, allowing for trouble-free use.

Input Current Noise

For applications with high source and feedback impedances, input current noise can be a significant contributor to total output noise. For this reason, it is important to consider noise current interaction with circuit elements placed at the amplifier’s inputs.

Figure 1. Input Current Noise Spectrum

The current noise spectrum of the LTC2063/LTC2064/LTC2065 is shown in Figure 1. Low input current noise is achieved through the use of MOSFET input devices and self-calibration techniques to eliminate 1/f current noise. As with all zero-drift amplifiers, there is an increase in current noise at the offset-nulling frequency. This phenomenon is discussed in the Input Bias Current and Clock Feedthrough section.

Input current noise also rises with frequency due to capacitive coupling of MOSFET channel thermal noise.

Input Bias Current and Clock Feedthrough

The input bias current of zero-drift amplifiers has different characteristics than that of a traditional operational amplifier. The specified input bias current is the DC average of transient currents which conduct due to the input stage's switching circuitry. In addition to this, junction leakages can contribute additional input bias current at elevated temperatures. Through careful design and the use of an innovative boot-strap circuit the input bias current of the LTC2063/LTC2064/LTC2065 does not exceed 20pA at room and 100pA over the full temperature range. This minimizes bias current induced errors even in high impedance circuits.

Transient switching currents at the input interact with source and feedback impedances producing error voltages which are indistinguishable from a valid input signal. The resulting error voltages are amplified by the amplifier’s closed-loop gain, which acts as a filter, attenuating frequency components above the circuit bandwidth. This phenomenon is known as clock feedthrough and is present in all zero-drift amplifiers. Understanding the cause and effect of clock feedthrough is important when using zero-drift amplifiers.

For zero-drift amplifiers, clock feedthrough is proportional to source and feedback impedances, as well as the magnitude of the transient currents. These transient currents have been minimized in the LTC2063/LTC2064/LTC2065.
APPLICATIONS INFORMATION

to allow use with high source and feedback impedances. Many circuit designs require high feedback impedances to minimize power consumption and/or require a sensor which is intrinsically high impedance. In these cases, a capacitor can be used, either at the input or across the feedback resistor, to limit the bandwidth of the closed-loop system. Doing so will effectively filter out the clock feedthrough signal.

Thermocouple Effects

In order to achieve accuracy on the microvolt level, thermocouple effects must be considered. Any connection of dissimilar metals forms a thermoelectric junction and generates a small temperature-dependent voltage. Also known as the Seebeck Effect, these thermal EMFs can be the dominant error source in low-drift circuits.

Connectors, switches, relay contacts, sockets, resistors, and solder are all candidates for significant thermal EMF generation. Even junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C, which significantly exceeds the maximum drift specification of the LTC2063/LTC2064/LTC2065. Figures 2 and 3 illustrate the potential magnitude of these voltages and their sensitivity to temperature.

In order to minimize thermocouple-induced errors, attention must be given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier’s input signal path and avoid connectors, sockets, switches, and relays whenever possible. If such components are required, they should be selected for low thermal EMF characteristics. Furthermore, the number, type, and layout of junctions should be matched for both inputs with respect to thermal gradients on the circuit board. Doing so may involve deliberately introducing dummy junctions to offset unavoidable junctions.

Air currents can also lead to thermal gradients and cause significant noise in measurement systems. It is important to prevent airflow across sensitive circuits. Doing so will often reduce thermocouple noise substantially. A summary of techniques can be found in Figure 4.

Leakage Effects

Leakage currents into high impedance signal nodes can easily degrade measurement accuracy of sub-nan AMP signals. High voltage and high temperature applications are especially susceptible to these issues. Quality insulation materials should be used, and insulating surfaces should be cleaned to remove fluxes and other residues. For humid environments, surface coating may be necessary to provide a moisture barrier.
* CUT SLOTS IN PCB FOR THERMAL ISOLATION.
** INTRODUCE DUMMY JUNCTIONS AND COMPONENTS TO OFFSET UNAVOIDABLE JUNCTIONS OR CANCEL THERMAL EMFS.
† ALIGN INPUTS SYMMETRICALLY WITH RESPECT TO THERMAL GRADIENTS.
‡ INTRODUCE DUMMY TRACES AND COMPONENTS FOR SYMMETRICAL THERMAL HEAT SINKING.
§ LOADS AND FEEDBACK CAN DISSIPATE POWER AND GENERATE THERMAL GRADIENTS. BE AWARE OF THEIR THERMAL EFFECTS.
# COVER CIRCUIT TO PREVENT AIR CURRENTS FROM CREATING THERMAL GRADIENTS.

Figure 4. Techniques for Minimizing Thermocouple-Induced Errors

 respects to the input pins and lead to thermocouple-induced error. Thermally isolate or align with inputs if resistor will cause heating.

† NO LEAKAGE CURRENT V,IN = V,IN
§ AVOID DISSIPATING SIGNIFICANT AMOUNTS OF POWER IN THIS RESISTOR.

Figure 5. Example Layout of Inverting Amplifier with Leakage Guard Ring

LEAKAGE CURRENT IS ABSORBED BY GROUND INSTEAD OF CAUSING A MEASUREMENT ERROR.
APPLICATIONS INFORMATION

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential very close to that of the inputs. The ring must be tied to a low impedance node. For inverting configurations, the guard ring should be tied to the potential of the positive input (+IN). For noninverting configurations, the guard ring should be tied to the potential of the negative input (−IN). In order for this technique to be effective, the guard ring must not be covered by solder mask. Ringing both sides of the printed circuit board may be required. See Figure 5 for an example of proper layout.

Shutdown Mode

The LTC2063 in the SC70 package, the LTC2064 in the DFN package and the LTC2065 in the QFN package, feature a shutdown mode for low-power applications. In the OFF state, each amplifier draws less than 170nA of supply current and the outputs present a high impedance to external circuitry.

Shutdown operation is accomplished by tying SHDN below VIL. If the shutdown feature is not required, it is recommended that SHDN be tied to V+. A current source pulls the SHDN pin high to automatically keep the amplifier in the ON state when the pin is floated, however this may not be reliable at elevated temperatures due to board leakage (see SHDN Circuit Block Diagram). For operation in noisy environments, a capacitor between SHDN and V+ is recommended to prevent noise from changing the shutdown state. When there is a danger of SHDN being pulled beyond the supply rails, resistance in series with the SHDN pin is recommended to limit the resulting current.

Start-Up Characteristics

Micropower op amps are often not micropower during start-up, which can cause problems when used on low current supplies. Large transient currents can conduct during power-up until the internal bias nodes settle to their final values. A large amount of current can be drawn from the supplies during this transient, which can sustain for several milliseconds in the case of a micropower part.

In the worst case, there may not be enough supply current available to take the system up to nominal voltages. In other cases, this transient power-up current will lead to added power loss in duty-cycled applications.

A way to quantify the transient current loss is to integrate the supply current during power-up to examine the total charge loss. If there were no additional transient current, the integrated supply current would appear as a smooth, straight line with a slope equal to the DC supply current of the part. Any deviation from a straight line indicates additional transient current that is drawn from the supply. The LTC2063/LTC2064/LTC2065 have been designed to minimize this charge loss during power-up so that power can be conserved in duty-cycled applications. Figure 6 shows the integrated supply current (i.e. charge) of the LTC2063 during power-up. Likewise, Figure 7 shows the charge loss due to enabling and disabling the part via the SHDN pin.
APPLICATIONS INFORMATION

There are benefits when the SHDN pin is used to disable and enable the part in duty-cycled applications, rather than powering down the external supply voltage (V+). Powering up and powering down the external supply will tend to waste charge due to charging and discharging the external decoupling capacitors. For these power-cycled applications, a relay or MOS device can be located after the decoupling capacitors to alleviate this, however there are drawbacks to this approach. The LTC2063 draws an initial charge of approximately 2nC when powered up. This recurring charge loss is unavoidable in power-cycled applications. Additionally, if the supply ramp rate exceeds 0.4V/µs, an internal transient ESD clamp will trigger, conducting additional current from V+ to V−. This will waste charge and can make insignificant any gain that may have been expected by power-cycling the supply. Figure 8 shows the charge loss at power-up.

The shutdown pin can be used to overcome these limitations in duty-cycled applications. The typical charge loss transitioning into and out of shutdown is only 1nC. Since the supply is not transitioned, the external decoupling capacitors do not draw charge from the supply.

Gas Sensor

This low power precision gas sensor circuit operates in an oxygen level range of 0% to 30%, with a nominal output of 1V in normal atmospheric oxygen concentrations (20.9%) when the gas sensor has been fully initialized. Total active power consumption is less than 2.1µA on a single rail supply.

Since this gas sensor produces 100µA in a normal oxygen environment and requires a 100Ω load resistor, the resulting input signal is typically around 10mV. The LTC2063’s rail-to-rail input means no additional DC level shifting is necessary, all the way down to very low oxygen concentrations.

Due to the extremely low input offset voltage of the LTC2063, which is 1µV typically and 5µV maximum, it is possible to gain up the mV-scale input signal substantially without introducing significant error. In the configuration shown in Figure 9, with a noninverting gain of 101V/V, the worst-case input offset results in a maximum of 0.5mV offset on the 1V output, or 0.05% error.

Although the 100kΩ resistor in series with the gas sensor does not strictly have the same precision requirement as the 10MΩ and 100kΩ resistors that set the gain, it is important to use a similar resistor at both input terminals. This helps to minimize additional offset voltage at the inputs due to thermocouple effects, hence the similar 0.1% precision requirement.

Figure 8. LTC2063 Power-Up Charge vs Supply Edge Rate

Figure 9. Micropower Precision Oxygen Sensor
APPLICATIONS INFORMATION

RTD Sensor

This low power platinum resistance temperature detector (RTD) sensor circuit draws only 35μA total supply current on a minimum 2.6V rail, and is accurate to within ±1°C at room temperature, including all error intrinsic to the Vishay PTS Class F0.3 Variant RTD. It covers the temperature range from −40°C to 85°C in 10mV/°C increments and produces an output of 1V at nominal room temperature of 25°C.

The LTC2063’s extremely low typical offset of 1μV and typical input bias current of 3pA allows for the use of a very low excitation current in the RTD. Thus, self-heating is negligible, improving accuracy.

The LT5400-3, B-grade, is used to provide a ±0.025% matched resistor network that is effectively a precision 131:1 voltage divider. This precision divider forms one half of a bridge circuit, with the 0.1% 110kΩ and RTD in the other branch. Note that the 110kΩ’s precision requirement is to ensure matching with the RTD. The 11kΩ R2 serves to provide a DC offset for the entire bridge so that the output is 1V at room temperature. Since bridge imbalances can lead to error, it is recommended to minimize the length of the leads connecting the RTD to reduce additional lead resistance.

The LT6656-2.048 reference helps create a known excitation current in the RTD at each temperature of operation, and also acts as a supply for the LTC2063, all while using less than 1μA itself. The LT6656 can accept input voltages anywhere between 2.6V and 18V, allowing for flexibility in selection of supply voltage while maintaining a fixed output range. The LT6656 reference can easily source the 35μA required to run the entire circuit, thanks to the LTC2063’s 2μA maximum supply current and ability to handle microvolt signals produced by the RTD under low excitation current.

Care should be taken to minimize thermocouple effects by preventing significant thermal gradients between the two op amp inputs. It is also important to choose feedback and series resistors that are low-tempco to minimize error due to drift over the entire temperature range.

2.6V ≤ VSupply ≤ 18V

VISHAY PTS SERIES
1kΩ PtRTD, CLASS F0.3
PTS12061B1K00P100
www.vishay.com

Figure 10. RTD Sensor

For more information www.analog.com
**APPLICATIONS INFORMATION**

**90V High Side Current Sense**

This micropower precision LTC2063 high side current sense circuit measures currents from 100μA to 250mA over a 4.5V to 90V input voltage range.

The output of this circuit is:

\[
\text{\textit{V}_\text{OUT}} = \frac{\text{\textit{R}_\text{OUT}} \cdot \text{\textit{R}_\text{SHUNT}}}{\text{\textit{R}_\text{IN}}} \cdot \text{\textit{I}_\text{SENSE}} = 500 \cdot \text{\textit{I}_\text{SENSE}}
\]

The LTC2063’s low typical input offset voltage of 1μV and low input bias current of 3pA contribute output errors that are much smaller than the error due to precision limitations of the resistors used. Thus, output accuracy is mainly set by the accuracy of the resistors \(\text{\textit{R}_\text{SENSE}}, \text{\textit{R}_\text{IN}},\) and \(\text{\textit{R}_\text{OUT}}\).

The LT1389-4.096V reference, along with the bootstrap circuit composed of M2, R3, and D1, establishes a very low power isolated 3V rail that protects the LTC2063 from reaching its absolute maximum voltage of 5.5V while allowing for much higher input voltages.

Since the LTC2063’s gain-bandwidth product is 20kHz, it is recommended to use this circuit to measure signals that are 2kHz or slower. Note that the output filter as drawn will limit the frequency to 1.5Hz, which optimizes for lowest noise. If this output filter bandwidth is too narrow, removing C2 leads to an output filter with 318Hz bandwidth, created by C3 and \(\text{\textit{R}_\text{OUT}}\).

**Figure 11. High Side Current Sense**

![Circuit Diagram for High Side Current Sense](image)

For more information www.analog.com
TYPICAL APPLICATIONS

Precision Micropower Low Side Current Sense

GAIN = 2.5V/10mV
V_{OUT} = 2.5V/1A \times I_{LOAD}

Micropower 16-Bit Data Acquisition
TYPICAL APPLICATIONS

Parallel LTC2064 Amplifiers to Reduce Noise by $\sqrt{2}$

$$V_{OUT} = \frac{V_{REF}}{2} \pm I_{LOAD} \times R_{SENSE} \times GAIN$$

$$GAIN = \frac{2M}{14k}$$

$I_{LOAD}$ CURRENT TO BE MEASURED (BI-DIRECTIONAL)

0.1% RESISTORS TO MAINTAIN OFFSET ACCURACY

For more information www.analog.com
TYPICAL APPLICATIONS

Micropower 16-Bit Data Acquisition with Single-to-Differential Input Driver

- +3.3V RAIL FOR WHOLE SYSTEM
- +2.7V OK IF ADC INTERFACE PERMITS

TOTAL ISUPPLY:
193.6µA CONVERSION
< 38.6µA SLEEP MODE

SINGLE-ENDED INPUT SIGNAL
1.25V OFFSET REQUIRED
MAX 250mVPP

DIFFERENTIAL ANALOG OUTPUT SIGNAL
1.25V OFFSET
FULL SCALE ±1.25V

GAIN = +10V/V, FILTER BW = 10Hz
GAIN = –10V/V, FILTER BW = 10Hz

For more information www.analog.com
SC6 Package
6-Lead Plastic SC70
(Reference LTC DWG # 05-08-1638 Rev B)

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. DETAILS OF THE PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE INDEX AREA
7. EIAJ PACKAGE REFERENCE IS EIAJ SC-70
8. JEDEC PACKAGE REFERENCE IS MO-203 VARIATION AB
**PACKAGE DESCRIPTION**

**S5 Package**
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)

**NOTE:**
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

[Diagrams and dimensions are shown here, but not transcribed due to the nature of the task.]
PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

For more information www.analog.com
PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE MOD-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT.
2. DRAWING NOT TO SCALE.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE.
5. EXPOSED PAD SHALL BE SOLDER PLATED.
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE.
PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1782 Rev Ø)

Exposed Pad Variation BB

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-4)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. NiPdAu PPF TERMINAL FINISH
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
F Package
14-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1650)

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE
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<td>A</td>
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<td>Added LTC2064, fixed typos</td>
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<td>B</td>
<td>4/20</td>
<td>Added LTC2065 to data sheet</td>
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TYPICAL APPLICATION

4CM CARBON MONOXIDE SENSOR
CITY TECHNOLOGY
70nA/ppm CO TYPICAL

4CM COUNTERT ELECTRODE (CE)
SELF-BIASES BELOW WE POTENTIAL
V_{WE} - V_{CE} = -0.3V TO -0.4V TYPICAL

RELATED PARTS

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<td>Micropower, Single/Dual, Zero-Drift Operational Amplifier</td>
<td>7μA I_S, 15μV V_{OS}, 11.8V to 5.5V V_S, 115kHz, RRIO</td>
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<td>Micropower, Low IB Single/Dual, Zero-Drift Op Amps</td>
<td>2μA I_S, 5μV V_{OS}, 1.7V to 5.25V V_S, 20kHz, RRIO</td>
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<td>Micropower, Single/Dual, Zero-Drift Operational Amplifier</td>
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<td>ADA4522-1/ADA4522-2/ ADA4522-4</td>
<td>55V, Low Noise Zero-Drift Operational Amplifier</td>
<td>900μA I_S, 5.8nV/√Hz, 5μV V_{OS}, 4.5V to 55V V_S, 3MHz, RR Output</td>
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<td>High Voltage-Low Noise Zero-Drift Operational Amplifier</td>
<td>4μV V_{OS}, 1.2mA I_S, 4.75V to 60V V_S, 1.5MHz, RR Output</td>
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<td>36V, Low Noise Zero-Drift Operational Amplifier</td>
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<td>1.5μA Max, Over-The-Top Precision Operational Amplifier</td>
<td>1.5μA I_S, 375μV V_{OS}, 2.2V to 36V V_S, 2.7kHz, RRIO</td>
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<td>1.6V, 1μA Precision Rail-to-Rail Input and Output Op Amps</td>
<td>1μA I_S, 500μV V_{OS}, 1.6V to 16V V_S, 2kHz, RRIO</td>
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