Micropower Synchronous Multitopology Controller with 42V Input Capability

FEATURES
- Easily Configurable as a Synchronous Buck, Boost, SEPIC, ZETA or Nonsynchronous Buck-Boost Converter
- Wide Input Range: 4.5V to 42V (Vin Can Operate to 0V, when EXTVCC > 4.5V)
- Automatic Low Noise Burst Mode® Operation
- Low IQ in Burst Mode Operation (15μA Operating)
- Input Voltage Regulation for High Impedance Source
- 100% Duty Cycle in Dropout (Buck Mode)
- 2A Gate Drivers (BG and TG)
- Adjustable Soft-Start with One Capacitor
- Frequency Programmable from 100kHz to 750kHz
- Can Be Synchronized to External Clock
- Available in 20-Lead TSSOP and 20-Lead 3mm × 4mm QFN Packages

APPLICATIONS
- General Purpose DC/DC Conversion
- Automotive Systems
- Industrial Supplies
- Solar Panel Power Converter

DESCRIPTION
The LT® 8711 is a multitopology current mode PWM controller that can easily be configured as a synchronous buck, boost, SEPIC, ZETA or as a nonsynchronous buck-boost converter. Its dual gate drive voltage inputs optimize gate driver efficiency.

The 15μA no-load quiescent current with the output voltage in regulation extends operating run time in battery powered systems. Low ripple Burst Mode operation enables high efficiency at very light loads while maintaining low output voltage ripple. The LT8711’s fixed switching frequency can be set from 100kHz to 750kHz or can be synchronized to an external clock.

The additional features include 100% duty cycle capability when in buck mode, a topology selection pin and adjustable soft-start. LT8711 is available in the 20-lead TSSOP and 20-lead 3mm × 4mm QFN packages.

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TYPICAL APPLICATION

400kHz 5V to 40V Input/12V Output Nonsynchronous Buck Boost

Efficiency vs Load Current

VIN = 5V
VIN = 12V
VIN = 24V
VIN = 36V
### Absolute Maximum Ratings

(Not 1)

- **VIN Voltage**: –0.3V to 42V
- **BIAS Voltage**: –0.3V to 42V
- **EXTVCC Voltage**: –0.3V to 42V
- **BG, TG Voltage**: Note 2
- **FB Voltage**: –0.3V to 5.5V
- **VC Voltage**: –0.3V to 2.5V
- **EN/FBIN Voltage**: –0.3V to MAX(VIN, EXTVCC)
- **SYNC Voltage**: –0.3V to 5.5V
- **OPMODE Voltage**: –0.3V to 5.5V
- **INTVEE Voltage**: Note 2
- **CSP Voltage**: –0.3V to 42V
- **CSN Voltage**: CSP – 0.3V to CSP + 0.3V
- **ISP Voltage**: ISN – 0.3V to ISN + 0.3V
- **ISN Voltage**: –0.3V to BIAS
- **INTVCC Voltage**: –0.3V to 5.5V
- **RT Voltage**: –0.3V to 5.5V
- **SS Voltage**: –0.3V to 5.5V

### Operating Junction Temperature Range

- **LT8711E**: –40°C to 125°C
- **LT8711I**: –40°C to 125°C

### Storage Temperature Range

- –65°C to 150°C

### Lead Temperature (Soldering, 10 sec)

- 300°C

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### Pin Configuration

**FE Package**

- 20-Lead Plastic TSSOP
- T_{JMAX} = 125°C, \( \theta_{JA} = 38°C/W, \ \theta_{JC} = 10°C/W \)
- EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

**UDC Package**

- 20-Lead (3mm × 4mm) Plastic QFN
- T_{JMAX} = 125°C, \( \theta_{JA} = 52°C/W, \ \theta_{JC} = 6.8°C/W \)
- EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

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### Order Information

- http://www.linear.com/product/LT8711#orderinfo

<table>
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<tr>
<th>Lead Free Finish</th>
<th>Tape and Reel</th>
<th>Part Marking*</th>
<th>Package Description</th>
<th>Temperature Range</th>
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<td>LT8711EFE#TRPBF</td>
<td>LT8711 FE</td>
<td>20-Lead TSSOP</td>
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</tr>
<tr>
<td>LT8711FE#PBF</td>
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<tr>
<td>LT8711EUDC#PBF</td>
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<td>LGQJ</td>
<td>20-Lead 3mm × 4mm QFN</td>
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<tr>
<td>LT8711IUDC#PBF</td>
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<td>LGQJ</td>
<td>20-Lead 3mm × 4mm QFN</td>
<td>–40°C to 125°C</td>
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</table>

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/). Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

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Rev A

For more information [www.analog.com](http://www.analog.com)
## ELECTRICAL CHARACTERISTICS

The ⋄ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_{IN} = 12V$, $V_{BIAS} = 12V$, unless otherwise noted (Note 3).

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<td>$V_{IN}$ Operating Voltage Range</td>
<td>$V_{EXTVCC} = 0V$</td>
<td>· 4.5</td>
<td>42</td>
<td>42</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{EXTVCC} = 4.5V$</td>
<td>· 0</td>
<td>0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>Quiescent Current in Normal Operation</td>
<td>$(V_{IN} + I_{EXTVCC} + I_{BIAS})$</td>
<td>· 2.0</td>
<td>2.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$V_{EN/FBIN} = 2.5V$, Not Switching</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Quiescent Current in Burst Mode Operation</td>
<td>$(V_{IN} + I_{EXTVCC} + I_{BIAS})$</td>
<td>15</td>
<td>25</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>$V_{FB} = V_{FB_REG} + 3mV$</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Quiescent Current in Shutdown</td>
<td>$(V_{IN} + I_{EXTVCC} + I_{BIAS})$</td>
<td>1</td>
<td>2</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>$V_{EN/FBIN} = 0V$</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>FB Output Regulation Voltage, $V_{FB_REG}$</td>
<td>$V_{EN/FBIN} = 4.5V$</td>
<td>784</td>
<td>800</td>
<td>816</td>
<td>mV</td>
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<td></td>
<td>$V_{EN/FBIN} = 0V$</td>
<td>795</td>
<td>800</td>
<td>805</td>
<td>mV</td>
</tr>
<tr>
<td>FB Line Regulation</td>
<td>$4.5V \leq V_{IN} \leq 42V$</td>
<td>0.01</td>
<td>0.05</td>
<td></td>
<td>%/V</td>
</tr>
<tr>
<td>FB Pin Input Bias Current</td>
<td>$V_{FB} = 0.8V$</td>
<td>· –50</td>
<td>0</td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td>Error Amp Transconductance</td>
<td>$\Delta I = \pm 5\mu A$</td>
<td>250</td>
<td></td>
<td></td>
<td>µmhos</td>
</tr>
<tr>
<td>Error Amp Voltage Gain</td>
<td>$R_T = 30.3k$</td>
<td>46</td>
<td>50</td>
<td>54</td>
<td>mV</td>
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<td>Maximum Current Sense Voltage, $V_{CGS} - V_{CSN}$</td>
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<td>mV</td>
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<tr>
<td>Switching Frequency, $f_{OSC}$</td>
<td>$R_T = 30.3k$</td>
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<td>750</td>
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<td>85</td>
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<td>750</td>
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<td>kHz</td>
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<tr>
<td>SYNC Input Voltage High</td>
<td>$V_{SYNC} = 0V$</td>
<td>1.3</td>
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<td></td>
<td>V</td>
</tr>
<tr>
<td>SYNC Input Voltage Low</td>
<td>$V_{SYNC} = 0V$</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SYNC Clock Pulse Duty Cycle</td>
<td>$V_{SYNC} = 0V$ to 2V, $f_{SYNC} = 500kHz$</td>
<td>20</td>
<td>80</td>
<td></td>
<td>%</td>
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<tr>
<td>Recommended SYNC Ratio $f_{SYNC}/f_{OSC}$</td>
<td>$V_{INTVCC} = 10mA$</td>
<td>0.8</td>
<td>1.2</td>
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<tr>
<td>$V_{INTVCC}$ Voltage</td>
<td>$V_{INTVCC} = 10mA$</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>$V_{INTVCC}$ Line Regulation</td>
<td>$V_{INTVCC} = 0mA$</td>
<td>–0.003</td>
<td>–0.03</td>
<td></td>
<td>%/V</td>
</tr>
<tr>
<td>$V_{INTVCC}$ Load Regulation</td>
<td>$V_{INTVCC} = 10mA$</td>
<td>–0.003</td>
<td>–0.03</td>
<td></td>
<td>%/V</td>
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<tr>
<td>$V_{INTVCC}$ Maximum External Load Current</td>
<td>$V_{INTVCC} = 0mA$</td>
<td>–1</td>
<td>–2</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$V_{INTVCC}$ Undervoltage Lockout</td>
<td>$V_{INTVCC} = 0mA$</td>
<td>3.9</td>
<td>4.1</td>
<td>4.3</td>
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</tr>
<tr>
<td></td>
<td>$V_{INTVCC} = 40mA$</td>
<td>3.45</td>
<td>3.6</td>
<td>3.75</td>
<td>V</td>
</tr>
<tr>
<td>$V_{INTVCC}$ Undervoltage Lockout Hysteresis</td>
<td>$V_{INTVCC} = 0mA$</td>
<td>500</td>
<td></td>
<td></td>
<td>mV</td>
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<tr>
<td>$V_{INTVCC}$ Voltage, $V_{BIAS} - V_{INTVEE}$</td>
<td>$V_{INTVEE} = 10mA$</td>
<td>4.85</td>
<td>5.15</td>
<td>5.4</td>
<td>V</td>
</tr>
<tr>
<td>$V_{INTVEE}$ Undervoltage Lockout, $V_{BIAS} - V_{INTVEE}$</td>
<td>$V_{BIAS} - V_{INTVEE} = 0mA$</td>
<td>3.6</td>
<td>3.85</td>
<td>4.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{BIAS} - V_{INTVEE} = 40mA$</td>
<td>3.4</td>
<td>3.6</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{INTVEE}$ Undervoltage Lockout Hysteresis, $V_{BIAS} - V_{INTVEE}$</td>
<td>$V_{INTVEE} = 250$</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
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<tr>
<td>BG Rise Time</td>
<td>$C_{BG} = 3.3nF$ (Note 4)</td>
<td>14</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>BG Fall Time</td>
<td>$C_{BG} = 3.3nF$ (Note 4)</td>
<td>12</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TG Rise Time</td>
<td>$C_{TG} = 3.3nF$ (Note 4)</td>
<td>11</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TG Fall Time</td>
<td>$C_{TG} = 3.3nF$ (Note 4)</td>
<td>14</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>BG and TG Non-Overlap Time</td>
<td>$C_{BG} = 3.3nF$ (Note 4)</td>
<td>70</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>BG and TG Non-Overlap Time</td>
<td>$C_{TG} = 3.3nF$ (Note 4)</td>
<td>70</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Minimum On-Time</td>
<td>$C_{BG} = C_{TG} = 3.3nF$</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
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</tbody>
</table>
**ELECTRICAL CHARACTERISTICS**  
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ C \). \( V_{IN} = 12V \), \( V_{BIAS} = 12V \), unless otherwise noted (Note 3).

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</thead>
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<td>SS Charge Current</td>
<td>( V_{SS} = 0V ), Current Flows Out of SS pin</td>
<td>●</td>
<td>6</td>
<td>10</td>
<td>15</td>
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<tr>
<td>SS Low Detection Voltage</td>
<td>Part Exiting Undervoltage Lockout</td>
<td>●</td>
<td>65</td>
<td>85</td>
<td>105</td>
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<tr>
<td>EN/FBIN Active Mode</td>
<td>EN/FBIN Rising</td>
<td>●</td>
<td>1.28</td>
<td>1.35</td>
<td>1.42</td>
</tr>
<tr>
<td>EN/FBIN Chip Enable</td>
<td>EN/FBIN Rising</td>
<td>●</td>
<td>0.97</td>
<td>1.03</td>
<td>1.11</td>
</tr>
<tr>
<td></td>
<td>EN/FBIN Falling</td>
<td>●</td>
<td>0.94</td>
<td>1</td>
<td>1.08</td>
</tr>
<tr>
<td>EN/FBIN Chip Enable Hysteresis</td>
<td></td>
<td></td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN/FBIN Input Voltage Low</td>
<td>Shutdown Mode</td>
<td>●</td>
<td>0.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN/FBIN Current Limit Adjustment Voltage</td>
<td>Full Current Limit</td>
<td>●</td>
<td>1.27</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Near Zero Current Limit</td>
<td>●</td>
<td>1.12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN/FBIN Pin Input Bias Current</td>
<td>( V_{EN/FBIN} = 12V )</td>
<td>●</td>
<td>–50</td>
<td>0</td>
<td>50</td>
</tr>
<tr>
<td>EN/FBIN Amp Transconductance</td>
<td>( V_{FB} = 0.6V )</td>
<td>●</td>
<td>40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN/FBIN Amp Voltage Gain</td>
<td>( V_{FB} = 0.6V )</td>
<td>●</td>
<td></td>
<td></td>
<td>100</td>
</tr>
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</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Do not apply a positive or negative voltage or current source to BG, TG and \( V_{EE} \) pins, otherwise permanent damage may occur.

**Note 3:** The LT8711E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT8711I is guaranteed over the full –40°C to 125°C operating junction temperature range.

**Note 4:** Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

**Note 5:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation over the specified maximum operating junction temperature may impair device reliability.
TYPICAL PERFORMANCE CHARACTERISTICS  \( T_A = 25^\circ C, \) unless otherwise noted.
TYPICAL PERFORMANCE CHARACTERISTICS  \( T_A = 25^\circ C \), unless otherwise noted.

**DCM Thresholds (ISP–ISN)**

**Oscillator Frequency vs Temperature**

**BG Transition Time vs Cap Load**

**TG Transition Time vs Cap Load**

**Minimum Operating Input Voltage**

**INTVCC vs Temperature**

**INTVCC UVLO vs Temperature**

**INTVCC Current Limit vs \( V_{IN} \) or EXTVCC**

**INTVCC Dropout from \( V_{IN} \) or EXTVCC**

For more information [www.analog.com](http://www.analog.com)
TYPICAL PERFORMANCE CHARACTERISTICS  \( T_A = 25^\circ C, \) unless otherwise noted.

- **INTVEE vs Temperature**
- **INTVEE UVLO vs Temperature**
- **INTVEE Current Limit vs BIAS**
- **INTVEE Dropout (BIAS = 6V)**
- **IQ_BURST vs VIN or EXTVCC**
- **IQ_BURST vs Temperature**

For more information [www.analog.com](http://www.analog.com)
**PIN FUNCTIONS** *(TSSOP/QFN)*

**EN/FBIN (Pin 1/Pin 19):** Enable and Input Voltage Regulation Pin. In conjunction with the UVLO (undervoltage lockout) circuit, this pin is used to enable/disable the chip and restart the soft-start sequence. The EN/FBIN pin is also used to limit the switching regulator current to avoid collapsing the input supply. Drive below 0.2V to disable the chip with very low quiescent current. Drive above 1.03V (typical) to activate the chip. The commanded input current will adjust when the EN/FBIN pin voltage is between 1.12V and 1.27V. Drive above 1.35V (typical) to activate switching with no reduction in input current and restart the soft-start sequence. See the Block Diagram and Applications section for more information. Do not float this pin.

**FB (Pin 2/Pin 20):** Feedback Input Pin. The LT8711 regulates the FB pin to 0.8V. Connect the feedback resistor divider tap to this pin.

**VC (Pin 3/Pin 1):** Error Amplifier Output Pin. Tie external compensation network to this pin.

**SS (Pin 4/Pin 2):** Soft Start Pin. Place a soft-start capacitor here. Upon start-up, the SS pin will be charged by a 410k resistor to about 4.3V. During an overtemperature or UVLO condition, the SS pin will be quickly discharged to reset the part. Once those conditions are clear, the part will attempt to restart.

**OPMODE (Pin 5/Pin 3):** Topology Selection Pin. Tie this pin to ground to select buck/ZETA mode. Tie to INTVCC to select SEPIC/boost mode. Tie to a 100pF capacitor to GND to select nonsynchronous buck-boost mode.

**ISP & ISN (Pins 6 & 7/ Pins 4 & 5):** Current Sense Positive and Negative Input Pins respectively. Kelvin connect ISP and ISN pins to a sense resistor.

**INTVCC (Pin 8/Pin 6):** 5V Dual Input LDO Regulator Pin. Must be locally bypassed with a minimum capacitance of 2.2µF to GND. Logic will choose to run INTVCC from the VIN or EXTVCC pins. A maximum 10mA external load can connect to the INTVCC pin. The undervoltage lockout on INTVCC is 3.6V (typical). The BG gate driver can begin switching when INTVCC exceeds 4.1V (typical).

**VIN (Pin 14/Pin 13):** Input Supply Pin. Must be locally bypassed. Can run down to 0V as long as EXTVCC > 4.5V.

**EXTVCC (Pin 15/Pin 14):** Alternate Input Supply Pin. Must be locally bypassed. Can run down to 0V as long as VIN > 4.5V.

**CSN & CSP (Pins 16 & 17/ Pins 15 & 16):** Current Sense Negative and Positive Input Pins Respectively. Kelvin connect CSN and CSP pins to a sense resistor.

**NC (Pin 18/Pin 11):** No Connection. Do not connect. Must be floated.

**SYNC (Pin 19/Pin 17):** To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock must exceed 1.3V, and the low level must be less than 0.4V. Drive this pin to less than 0.4V to revert to the internal free running clock. See the Applications Information section for more information.

**RT (Pin 20/Pin 18):** Timing Resistor Pin. Adjusts the LT8711’s switching frequency. Place a resistor from this pin to ground to set the frequency to a fixed free running level. Do not float this pin.

**GND (Pin 21/Pin 21):** Ground. Must be soldered directly to the local ground plane.

**TG (Pin 10/Pin 8):** PFET Gate Drive Pin. Low and high levels are INTVEE and BIAS respectively with a 2A drive capability.

**BG (Pin 11/Pin 10):** NFET Gate Drive Pin. Low and high levels are GND and INTVCC respectively with a 2A drive capability.

**NC (Pin 12/Pin 9):** No Connection. Do not connect. Must be floated.
**START-UP AND FAULT SEQUENCE**

**CHIP OFF**
- **ALL SWITCHES OFF**

**INITIALIZE**
- SS PULLED LOW
- INTVCC CHARGES UP

**ACTIVE MODE**
- SS CHARGES UP

**BEGIN SWITCHING**
- NFET BEGINS SWITCHING
- PFET BEGINS SWITCHING
- WHEN INTVEE REGULATOR IS OUT OF UVLO

**RESET DETECTED**
- SS DISCHARGES QUICKLY
- SWITCHER DISABLED

**RESET OVER**
- NO RESET CONDITIONS DETECTED

**RESET = UVLO ON VIN OR EXTVCC (<4.5V MAX)**
- UVLO ON INTVCC (<3.6V TYP)
- UVLO ON INTVEE (BUCK/BUCK-BOOST/ZETA) (<3.6V TYP)
- EN/FBIN < 1.35V (TYP) AT 1ST POWER-UP
- EN/FBIN < 1.00V (TYP) AFTER ACTIVE MODE SET
- STATUS CHANGE ON OPMODE PIN
- OVERTEMPERATURE (TJ > 165°C)

**Figure 1. State Diagram**
OPERATION

OPERATION—OVERVIEW

The LT8711 uses a constant frequency, current mode control scheme to provide excellent line and load regulation. The part’s undervoltage lockout (UVLO) function, together with soft-start, offers a controlled means of starting up. Output voltage and input voltage have control over the commanded peak current which allows a wide range of applications to be built using the LT8711. Synchronous switching makes high efficiency and high output current applications possible. When operating at light load condition, the LT8711 will enter burst mode to minimize switching loss. Refer to the Block Diagram and the State Diagram (Figure 1) for the following description of the part’s operation.

OPERATION—TOPOLOGY SELECTING

The 8711 can be configured as a synchronous buck, boost, SEPIC, ZETA or nonsynchronous buck-boost converter by configuration of the OPMODE pin.

When the OPMODE pin is connected to GND, the controller operates in buck/ZETA mode.

When the OPMODE pin is connected to the INTVCC pin, the controller operates in SEPIC/boost mode.

When the OPMODE pin is tied to a 100pF capacitor to GND, the controller operates in nonsynchronous buck-boost mode.

OPERATION—START-UP

Several functions are provided to enable a very clean start-up of the LT8711.

Precise Turn-On Voltages

The EN/FBIN pin has two voltage levels for activating the part: one that enables the part and allows internal rails to operate and a 2nd voltage threshold which activates a soft-start cycle and switching can begin. To enable the part, take the EN/FBIN pin above 1.03V (typical). This comparator has 50mV of hysteresis to protect against glitches and slow ramping. To activate a soft-start cycle and allow switching, take EN/FBIN above 1.35V (typical). When EN/FBIN exceeds 1.35V (typical), the logic state is latched so that if EN/FBIN drops between 1.03V to 1.35V (typical), the SS pin is not pulled low by the EN/FBIN pin. The EN/FBIN pin is also used for input voltage regulation which is at 1.200V (typical). Input voltage regulation is explained in more detail in the Operation—Regulation section. Taking the EN/FBIN pin below 0.2V shuts down the chip, resulting in extremely low quiescent current. See Figure 2 that illustrates the different EN/FBIN voltage thresholds.

Figure 2. EN/FBIN Modes of Operation

Undervoltage Lockout (UVLO)

The LT8711 has internal UVLO circuitry that disables the chip when the greater of VIN or EXTVCC < 3.6V (typical). The EN/FBIN pin can also be used to create a configurable UVLO.

Soft-Start of Switch Current

The soft-start circuitry provides for a gradual ramp-up of the switch current (refer to Max Current Limit vs SS in Typical Performance Characteristics). When the part is brought out of shutdown, the external SS capacitor is first discharged which resets the states of the logic circuits in the chip. Once the chip is in active mode, an integrated 410k resistor pulls the SS pin to ~4.3V at a ramp rate set by the external capacitor connected to the pin. Typical values for the soft-start capacitor range from 100nF to 1μF.
OPERATION

OPERATION—REGULATION

Use the Block Diagram when stepping through the following description of the LT8711 operating in regulation. The LT8711 has two modes of regulation:

1. Output Voltage (via FB pin)
2. Input Voltage (via EN/FBIN pin)

Both of these regulation loops control the peak commanded current. At the start of each oscillator cycle, the SR latch is set, which first turns off the external rectifier switch (NFET in Block Diagram), and then turns on the external main switch (PFET in Block Diagram). The PFET’s current flows through an external current sense resistor (RSENSE) generating a voltage proportional to the PFET switch current. This voltage is then amplified by A1 and added to a stabilizing ramp. The resulting sum is fed into the positive terminal of the PWM comparator. When the voltage on the positive input of the PWM comparator exceed the voltage on the negative input ($V_C$ pin), the SR latch is reset, turning off the PFET and then turning on the NFET. The voltage on the $V_C$ pin is controlled by one of the regulation loops, or a combination of regulation loops.

Slope compensation provides stability in constant frequency current mode control architectures by preventing subharmonic oscillations at high duty cycles. This is accomplished internally by adding a compensating ramp to the positive terminal of the PWM comparator.

Output Voltage Regulation

The error amplifier servos the $V_C$ node by comparing the voltage on the FB pin with an internal 0.800V reference. When the load current increases it causes a reduction in the feedback voltage relative to the reference causing the error amplifier to raise the $V_C$ voltage. In this manner, the FB error amplifier sets the correct peak current level to maintain output voltage regulation.

Input Voltage Regulation

A resistor divider from the converter’s input voltage to the EN/FBIN pin sets the input voltage regulation point. The EN/FBIN pin voltage connects to the positive input of amplifier EA2. The $V_C$ pin voltage is set by EA2, which is the amplified difference between the EN/FBIN pin voltage and an internal 1.200V reference voltage. In this manner, the EN/FBIN error amplifier sets the correct peak current level to maintain input voltage regulation.

OPERATION—RESET CONDITIONS

The LT8711 has three reset cases. When the part is in reset, the SS pin is pulled low and both power switches, NFET and PFET, are forced off. Once all of the reset conditions are gone, the part is allowed to begin a soft-start sequence and switching can commence. Each of the following events can cause the LT8711 to be in reset:

1. UVLO
   a. The greater of $V_{IN}$ and $EXTV_{CC}$ is < 4.5V (maximum)
   b. UVLO on $INTV_{CC}$, $INTV_{CC}$ < 3.6V (typical)
   c. UVLO on $INTV_{EE}$, $V_{BIAS}$ – $V_{INTVEE}$ < 3.6V (typical) unless BOOST/SEPIC topology is selected
   d. EN/FBIN < 1.35V (typical) at first power-up
   e. EN/FBIN < 1.00V (typical) after active mode set

2. OPMODE pin status changes

3. Die Temperature > 165°C

OPERATION—POWER SWITCH CONTROL

The external PFET and NFET switches are never on at the same time (except buck-boost mode), and there is a non-overlap time of about 100ns to prevent cross conduction.
OPERATION

Light Load Operation Modes
The SYNC pin can be used to tell the LT8711 to operate in FCM regardless of load current, or operate in DCM and Burst Mode at light loads.

  SYN = logic high: FCM
  SYN = logic low: DCM or Burst Mode operation

If a clock is applied to the SYNC pin the part will synchronize to an external clock frequency and operate in FCM mode.

OPERATION—AUTOMATIC LOW NOISE Burst Mode OPERATION
At no load or very light load condition, high FB voltage causes $V_C$ to decrease. When $V_C$ voltage is lower than a threshold voltage, the controller operates in Burst Mode to minimize switching loss. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the average input supply current to 15μA in a typical application. Low standby power and higher conversion efficiency is thus achieved. To optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.

OPERATION—LDO REGULATORS (INTVCC AND INTVEE)
The INTVCC LDO regulates at 5.0V (typical) and is used as the top rail for the BG gate driver. The INTVCC LDO can run from VIN or EXTVC and will intelligently select to run from the best rail to minimize power loss in the chip, but at the same time, select the proper input for maintaining INTVCC as close to 5.0V as possible. The INTVCC regulator also has safety features to limit the power dissipation in the internal pass device and also to prevent it from damage if the pin is shorted to ground. The UVLO threshold on INTVCC is 3.6V (typical), and the LT8711 will be in reset until the LDO comes out of UVLO.

The INTVEE regulator regulates to 5.15V (typical) below the BIAS pin voltage. The BIAS and INTVEE voltages are used for the top and bottom rails of the TG gate driver respectively. Just like the INTVCC regulator, the INTVEE regulator has a safety feature to limit the power dissipation in the internal pass device. The TG pin can begin switching only after the INTVEE regulator comes out of UVLO (3.85V typical across the BIAS and INTVEE pins). When the INTVEE regulator is in UVLO, for the boost and SEPIC topologies, the bottom switch is allowed to switch. The output current would flow through the body diode of the PFET. To protect the PFET from thermal damage under this condition, the maximum commanded current is folded back to 27mV (typical) across the CSP-CSN pins.

For more information www.analog.com
The LT8711 can be configured as a buck converter as in Figure 3.

For a desired output current and output voltage over a given input voltage range, Table 1 is a step-by-step set of equations to calculate component values for the LT8711 when operating as a buck converter. Refer to more detail in this section and the Appendix for further information on the design equations presented in Table 1.

**Variable Definitions:**

- $V_{IN(MIN)}$: Minimum Input Voltage
- $V_{IN(MAX)}$: Maximum Input Voltage
- $V_{OUT}$: Output Voltage
- $I_{OUT}$: Output Current of Converter
- $f$: Switching Frequency
- $D_{CMAX}$: Power Switch Duty Cycle at $V_{IN(MIN)}$
- $V_{CSPN}$: Current Limit Voltage at $D_{CMAX}$

**APPLICATIONS INFORMATION**

### Table 1. Buck Design Equations

<table>
<thead>
<tr>
<th>Parameters/Equations</th>
<th>Step 1: Inputs</th>
<th>Step 2: $D_{CMAX}$</th>
<th>Step 3: $V_{CSPN}$</th>
<th>Step 4: $R_{SENSE}$</th>
<th>Step 5: $L$</th>
<th>Step 6: $C_{OUT}$</th>
<th>Step 7: $C_{IN}$</th>
<th>Step 8: $R_{FB1}/R_{FB2}$</th>
<th>Step 9: $R_{T}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pick $V_{IN}$, $V_{OUT}$, $I_{OUT}$, and $f$ to calculate equations below.</td>
<td>$D_{CMAX} = \frac{V_{OUT}}{V_{IN(MIN)}}$</td>
<td>See Max Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find $V_{CSPN}$ at $D_{CMAX}$.</td>
<td>$R_{SENSE} \leq 0.75 \cdot \frac{V_{CSPN}}{I_{OUT}}$</td>
<td>$L_{TYP} = \frac{R_{SENSE} \cdot V_{IN(MIN)}}{12.5m \cdot f \cdot V_{OUT} \cdot \left(\frac{V_{IN(MIN)}}{V_{OUT}}\right)}$</td>
<td>$L_{MIN} = \frac{R_{SENSE} \cdot V_{IN(MIN)} \cdot 2V_{OUT} - V_{IN(MIN)}}{40m \cdot f \cdot V_{OUT}}$</td>
<td>$L_{MAX} = \frac{R_{SENSE} \cdot V_{IN(MIN)} - V_{OUT}}{2.5m \cdot f \cdot V_{OUT}}$</td>
<td>$C_{OUT} \geq \frac{1 - D_{CMIN}}{8 \cdot L \cdot f^2 \cdot 0.005}$</td>
<td>$C_{IN} \geq I_{OUT} \cdot \frac{D_{CMAX}}{f \cdot \Delta V_{IN}}$</td>
<td>$R_{FB1} = \frac{V_{OUT} - 1}{0.8V} \cdot R_{FB2}$</td>
</tr>
</tbody>
</table>

- Solve equations 1 to 4 for a range of $L$ values.
- The minimum value of the $L$ range is the higher of $L_{TYP}$ and $L_{MIN}$.
- $\Delta V_{IN}$ is acceptable maximum input ripple voltage.

**NOTE:** The final values for $C_{OUT}$ and $C_{IN}$ may deviate from the above equations in order to obtain desired load transient performance for a particular application. The $C_{OUT}$ and $C_{IN}$ equations assume zero ESR, so increase the capacitance accordingly based on the combined ESR.
BOOST CONVERTER COMPONENT SELECTION

The LT8711 can be configured as a boost converter as in Figure 4.

For a desired output current and output voltage over a given input voltage range, Table 2 is a step-by-step set of equations to calculate component values for the LT8711 when operating as a boost converter. Refer to more detail in this section and the Appendix for further information on the design equations presented in Table 2.

Variable Definitions:

- $V_{IN(MIN)}$ = Minimum Input Voltage
- $V_{IN(MAX)}$ = Maximum Input Voltage
- $V_{OUT}$ = Output Voltage
- $I_{OUT}$ = Output Current of Converter
- $f$ = Switching Frequency
- $D_{C MAX}$ = Power Switch Duty Cycle at $V_{IN(MIN)}$
- $V_{CSPN}$ = Current Limit Voltage at $D_{C MAX}$

Table 2. Boost Design Equations

<table>
<thead>
<tr>
<th>Step</th>
<th>Parameters/Equations</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Pick $V_{IN}$, $V_{OUT}$, $I_{OUT}$, and $f$ to calculate equations below.</td>
</tr>
<tr>
<td>2</td>
<td>$D_{C MAX} = 1 - \frac{V_{IN(MIN)}}{V_{OUT}}$</td>
</tr>
<tr>
<td>3</td>
<td>$V_{CSPN}$ See Max Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find $V_{CSPN}$ at $D_{C MAX}$.</td>
</tr>
<tr>
<td>4</td>
<td>$R_{SENSE} \leq 0.63 \times \frac{V_{CSPN}}{I_{OUT}} (1 - D_{C MAX})$</td>
</tr>
<tr>
<td>5</td>
<td>$L_{TYP} = R_{SENSE} \times \frac{V_{IN(MIN)}}{12.5m \times f} \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)$</td>
</tr>
<tr>
<td></td>
<td>$L_{MIN} = R_{SENSE} \times \frac{V_{OUT}}{40m \times f} \left(1 - \frac{V_{IN(MIN)}}{V_{OUT} - V_{IN(MIN)}}\right)$</td>
</tr>
<tr>
<td></td>
<td>$L_{MAX1} = R_{SENSE} \times \frac{V_{IN(MIN)}}{5m \times f} \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)$</td>
</tr>
<tr>
<td></td>
<td>$L_{MAX2} = R_{SENSE} \times \frac{V_{IN(MAX)}}{5m \times f} \left(1 - \frac{V_{IN(MAX)}}{V_{OUT}}\right)$</td>
</tr>
<tr>
<td></td>
<td>- Solve equations 1 to 4 for a range of $L$ values.</td>
</tr>
<tr>
<td></td>
<td>- The minimum value of the $L$ range is the higher of $L_{TYP}$ and $L_{MIN}$. The maximum of the $L$ value range is the lower of $L_{MAX}$.</td>
</tr>
<tr>
<td>6</td>
<td>$C_{OUT} \geq \frac{I_{OUT} \times D_{C MAX}}{f \times 0.005 \times V_{OUT}}$</td>
</tr>
<tr>
<td>7</td>
<td>$C_{IN} \geq \frac{D_{C MAX}}{8 \times L \times f^2 \times 0.005}$</td>
</tr>
<tr>
<td>8</td>
<td>$R_{FB1/RFB2} = \frac{1}{V_{OUT} - 0.8V} \times R_{FB2}$</td>
</tr>
<tr>
<td>9</td>
<td>$R_{T} = \frac{25000}{f} - 2$: $f$ is in kHz and $R_{T}$ is in kΩ</td>
</tr>
</tbody>
</table>

NOTE: The final values for $C_{OUT}$ and $C_{IN}$ may deviate from the above equations in order to obtain desired load transient performance for a particular application. The $C_{OUT}$ and $C_{IN}$ equations assume zero ESR, so increase the capacitance accordingly based on the combined ESR.
APPLICATIONS INFORMATION

SEPIC CONVERTER COMPONENT SELECTION

The LT8711 can be configured as a SEPIC converter as in Figure 5.

For a desired output current and output voltage over a given input voltage range, Table 3 is a step-by-step set of equations to calculate component values for the LT8711 when operating as a SEPIC converter. Refer to more detail in this section and the Appendix for further information on the design equations presented in Table 3.

Variable Definitions:

- $V_{IN\,(MIN)}$ = Minimum Input Voltage
- $V_{IN\,(MAX)}$ = Maximum Input Voltage
- $V_{OUT}$ = Output Voltage
- $I_{OUT}$ = Output Current of Converter
- $f$ = Switching Frequency
- $DC_{MAX}$ = Power Switch Duty Cycle at $V_{IN\,(MIN)}$
- $V_{CSPN}$ = Current Limit Voltage at $DC_{MAX}$

Table 3. SEPIC Design Equations

<table>
<thead>
<tr>
<th>Step 1: Inputs</th>
<th>Parameters/Equations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pick $V_{IN}$, $V_{OUT}$, $I_{OUT}$, and $f$ to calculate equations below.</td>
<td></td>
</tr>
</tbody>
</table>

| Step 2: $DC_{MAX}$ | $DC_{MAX} = \frac{V_{OUT}}{V_{IN\,(MIN)} + V_{OUT}}$ |

| Step 3: $V_{CSPN}$ | See Max Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find $V_{CSPN}$ at $DC_{MAX}$. |

| Step 4: $R_{SENSE}$ | $R_{SENSE} \leq 0.63 \cdot \frac{V_{CSPN}}{I_{OUT}} (1 - DC_{MAX})$ |
| $R_{SENSE1} = R_{SENSE2} = R_{SENSE}$ |

| Step 5: $L$ | $L_{TYP} = \frac{R_{SENSE} \cdot V_{OUT}}{12.5 \cdot f} \cdot \frac{V_{IN\,(MIN)}}{V_{IN\,(MIN)} + V_{OUT}}$ |
| $L_{MIN} = \frac{R_{SENSE} \cdot V_{OUT}}{40 \cdot f} \cdot \left(1 - \left(\frac{V_{IN\,(MIN)}}{V_{OUT}}\right)^2\right)$ |
| $L_{MAX} = \frac{R_{SENSE} \cdot V_{OUT}}{5 \cdot f} \cdot \frac{V_{IN\,(MIN)}}{V_{IN\,(MIN)} + V_{OUT}}$ |

- Solve equations 1 to 4 for a range of $L$ values.
- The minimum value of the $L$ range is the higher of $L_{TYP}$ and $L_{MIN}$. The maximum of the $L$ value range is the lower of $L_{MAX}$.
- $L = L1 = L2$ for coupled inductors.
- $L = L1 || L2$ for uncoupled inductors.

| Step 6: $C1$ | $C1 \geq 10\,\mu F$ (Typical); $V_{RATING} > V_{IN}$ |

| Step 7: $C_{OUT}$ | $C_{OUT} \geq \frac{I_{OUT} \cdot DC_{MAX}}{f} \cdot 0.005 \cdot V_{OUT}$ |

| Step 8: $C_{IN}$ | $C_{IN} \geq \frac{DC_{MAX}}{8 \cdot L \cdot f^2} \cdot 0.005$ |

| Step 9: $R_{FB1}/R_{FB2}$ | $R_{FB1} = \frac{V_{OUT}}{0.8\,V} - 1 \cdot R_{FB2}$ |

| Step 10: $R_T$ | $R_T = \frac{25000}{f}$ |

NOTE: The final values for $C_{OUT}$ and $C_{IN}$ may deviate from the above equations in order to obtain desired load transient performance for a particular application. The $C_{OUT}$ and $C_{IN}$ equations assume zero ESR, so increase the capacitance accordingly based on the combined ESR.

Figure 5. SEPIC Converter—The Component Values Given Are Typical Values for a 200kHz, 4.5V–40V to 12V/4A SEPIC

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APPLICATIONS INFORMATION

ZETA CONVERTER COMPONENT SELECTION

The LT8711 can be configured as a ZETA converter as in Figure 6.

For a desired output current and output voltage over a given input voltage range, Table 4 is a step-by-step set of equations to calculate component values for the LT8711 when operating as a ZETA converter. Refer to more detail in this section and the Appendix for further information on the design equations presented in Table 4.

Variable Definitions:

\( V_{\text{IN(MIN)}} \) = Minimum Input Voltage
\( V_{\text{IN(MAX)}} \) = Maximum Input Voltage
\( V_{\text{OUT}} \) = Output Voltage
\( I_{\text{OUT}} \) = Output Current of Converter
\( f \) = Switching Frequency
\( DC_{\text{MAX}} \) = Power Switch Duty Cycle at \( V_{\text{IN(MIN)}} \)
\( V_{\text{CSPN}} \) = Current Limit Voltage at \( DC_{\text{MAX}} \)

Table 4. ZETA Design Equations

<table>
<thead>
<tr>
<th>Step</th>
<th>Parameters/Equations</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td><strong>Inputs</strong></td>
</tr>
<tr>
<td></td>
<td>Pick ( V_{\text{IN}} ), ( V_{\text{OUT}} ), ( I_{\text{OUT}} ), and ( f ) to calculate equations below.</td>
</tr>
<tr>
<td>2</td>
<td><strong>( DC_{\text{MAX}} )</strong></td>
</tr>
<tr>
<td></td>
<td>( DC_{\text{MAX}} \approx \frac{V_{\text{OUT}}}{V_{\text{IN(MIN)}} + V_{\text{OUT}}} )</td>
</tr>
<tr>
<td>3</td>
<td><strong>( V_{\text{CSPN}} )</strong></td>
</tr>
<tr>
<td></td>
<td>See Max Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find ( V_{\text{CSPN}} ) at ( DC_{\text{MAX}} ).</td>
</tr>
<tr>
<td>4</td>
<td><strong>( R_{\text{SENSE}} )</strong></td>
</tr>
<tr>
<td></td>
<td>( R_{\text{SENSE}} \leq 0.63 \times \frac{V_{\text{CSPN}}}{I_{\text{OUT}}} \left(1 - DC_{\text{MAX}}\right) ) (</td>
</tr>
<tr>
<td>5</td>
<td><strong>( L )</strong></td>
</tr>
<tr>
<td></td>
<td>Solve equations 1 to 4 for a range of ( L ) values.</td>
</tr>
<tr>
<td></td>
<td>The minimum value of the ( L ) range is the higher of ( L_{\text{TYP}} ) and ( L_{\text{MIN}} ). The maximum of the ( L ) value range is the lower of ( L_{\text{MAX}} ).</td>
</tr>
<tr>
<td></td>
<td>( L = L_{1} = L_{2} ) for coupled inductors.</td>
</tr>
<tr>
<td></td>
<td>( L = L_{1}</td>
</tr>
<tr>
<td>6</td>
<td><strong>( C_{1} )</strong></td>
</tr>
<tr>
<td></td>
<td>( C_{1} \geq 10\mu F ) (Typical); ( V_{\text{RATING}} &gt; V_{\text{IN}} )</td>
</tr>
<tr>
<td>7</td>
<td><strong>( C_{\text{OUT}} )</strong></td>
</tr>
<tr>
<td></td>
<td>( C_{\text{OUT}} \geq \frac{I_{\text{OUT}} \times DC_{\text{MAX}}}{f \times 0.005 \times V_{\text{OUT}}} )</td>
</tr>
<tr>
<td>8</td>
<td><strong>( C_{\text{IN}} )</strong></td>
</tr>
<tr>
<td></td>
<td>( C_{\text{IN}} \geq \frac{DC_{\text{MAX}}}{8 \times L \times f^{2} \times 0.005} )</td>
</tr>
<tr>
<td>9</td>
<td><strong>( R_{\text{FB1}}/R_{\text{FB2}} )</strong></td>
</tr>
<tr>
<td></td>
<td>( R_{\text{FB1}} = \left(\frac{V_{\text{OUT}}}{0.8V} - 1\right) \times R_{\text{FB2}} )</td>
</tr>
<tr>
<td>10</td>
<td><strong>( R_{\text{T}} )</strong></td>
</tr>
<tr>
<td></td>
<td>( R_{\text{T}} = \frac{25000}{f} ), ( f ) is in kHz and ( R_{T} ) is in k( \Omega )</td>
</tr>
</tbody>
</table>

*NOTE:* The final values for \( C_{\text{OUT}} \) and \( C_{\text{IN}} \) may deviate from the above equations in order to obtain desired load transient performance for a particular application. The \( C_{\text{OUT}} \) and \( C_{\text{IN}} \) equations assume zero ESR, so increase the capacitance accordingly based on the combined ESR.

![Figure 6. ZETA Converter—The Component Values Given Are Typical Values for a 200kHz, 5V–40V to 12V/3.5A ZETA](image-url)
APPLICATIONS INFORMATION

BUCK-BOOST CONVERTER COMPONENT SELECTION

The LT8711 can be configured as a buck-boost converter as in Figure 7.

For a desired output current and output voltage over a given input voltage range, Table 5 is a step-by-step set of equations to calculate component values for the LT8711 when operating as a buck-boost converter. Refer to more detail in this section and the Appendix for further information on the design equations presented in Table 5.

Variable Definitions:

\[ V_{IN(MIN)} = \text{Minimum Input Voltage} \]
\[ V_{IN(MAX)} = \text{Maximum Input Voltage} \]
\[ V_{OUT} = \text{Output Voltage} \]
\[ I_{OUT} = \text{Output Current of Converter} \]
\[ f = \text{Switching Frequency} \]
\[ DC_{MAX} = \text{Power Switch Duty Cycle at } V_{IN(MIN)} \]

\[ V_{CSPN} = \text{Current Limit Voltage at } DC_{MAX} \]

Table 5. Buck-Boost Design Equations

<table>
<thead>
<tr>
<th>Step 1: Inputs</th>
<th>( V_{IN}, V_{OUT}, I_{OUT}, ) and ( f ) to calculate equations below.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step 2: DC(_{MAX})</td>
<td>( DC_{MAX} = \frac{V_{OUT}}{V_{IN(MIN)} + V_{OUT}} )</td>
</tr>
<tr>
<td>Step 3: V(_{CSPN})</td>
<td>See Max Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find ( V_{CSPN} ) at ( DC_{MAX} ).</td>
</tr>
<tr>
<td>Step 4: R(_{SENSE})</td>
<td>( R_{SENSE} \leq 0.63 \cdot \frac{V_{CSPN}}{I_{OUT}} (1 - DC_{MAX}) ) ( R_{SENSE1} = R_{SENSE2} = R_{SENSE} )</td>
</tr>
<tr>
<td>Step 5: L (_{TYP})</td>
<td>( L_{TYP} = \frac{R_{SENSE} \cdot V_{OUT}}{12.5 \cdot f \cdot V_{IN(MIN)}} )</td>
</tr>
<tr>
<td>( L_{MIN})</td>
<td>( L_{MIN} = \frac{R_{SENSE} \cdot V_{OUT}}{40m \cdot f \cdot (1 - \frac{V_{IN(MIN)}}{V_{OUT}})^2} )</td>
</tr>
<tr>
<td>( L_{MAX})</td>
<td>( L_{MAX} = \frac{R_{SENSE} \cdot V_{OUT}}{5m \cdot f \cdot V_{IN(MIN)} + V_{OUT}} )</td>
</tr>
</tbody>
</table>

- Solve equations 1 to 4 for a range of \( L \) values.
- The minimum value of the \( L \) range is the higher of \( L_{TYP} \) and \( L_{MIN} \). The maximum of the \( L \) value range is the lower of \( L_{MAX} \).

| Step 6: C\(_{OUT}\) | \( C_{OUT} \geq I_{OUT} \cdot DC_{MAX} / f \cdot 0.005 \cdot V_{OUT} \) |
| Step 7: C\(_{IN}\) | \( C_{IN} \geq \frac{DC_{MAX}}{8 \cdot L \cdot f^2} \cdot 0.005 \) |

| Step 8: \( R_{FB1}/R_{FB2}\) | \( R_{FB1} = \frac{V_{OUT} - 1}{0.8V} \cdot R_{FB2} \) |
| Step 9: \( R_{T}\) | \( R_{T} = \frac{25000}{f} \) \( f \) is in kHz and \( R_{T} \) is in kΩ |

NOTE: The final values for \( C_{OUT} \) and \( C_{IN} \) may deviate from the above equations in order to obtain desired load transient performance for a particular application. The \( C_{OUT} \) and \( C_{IN} \) equations assume zero ESR, so increase the capacitance accordingly based on the combined ESR.

Figure 7. Buck-Boost Converter—The Component Values Given Are Typical Values for a 400kHz, 5V–40V to 12V/2.5A Buck-Boost
APPLICATIONS INFORMATION

SETTING THE OUTPUT VOLTAGE REGULATION

The LT8711 output voltage is set by a resistor divider between VOUT, FB, and GND.

\[ V_{\text{OUT}} = 0.8V \times \left(1 + \frac{R_{\text{FB1}}}{R_{\text{FB2}}} \right) \]

where \( R_{\text{FB1}} \) and \( R_{\text{FB2}} \) are shown in the Block Diagram.

See the Electrical Characteristics for tolerances on the FB regulation voltage.

SETTING THE INPUT VOLTAGE REGULATION OR UNDervoltage LOCKOUT

By connecting a resistor divider between VIN, EN/FBIN, and GND, the EN/FBIN pin provides a means to regulate the input voltage or to create an undervoltage lockout function. Referring to error amplifier EA2 in the block diagram, when EN/FBIN is lower than the 1.2V reference, VC is pulled low. For example, if VIN is provided by a relatively high impedance source (e.g. a solar panel) and the current draw pulls VIN below a preset limit, VC will be reduced, thus reducing current draw from the input supply and limiting the input voltage drop.

To set the minimum or regulated input voltage use:

\[ V_{\text{IN(MIN-REG)}} = 1.2V \times \left(1 + \frac{R_{\text{IN1}}}{R_{\text{IN2}}} \right) \]

where \( R_{\text{IN1}} \) and \( R_{\text{IN2}} \) are shown in the Block Diagram.

Temperature Dependent Output Voltage Using NTC Resistor

It may be desirable to regulate the converter’s output based on the ambient temperature. The INTVCC LDO regulated voltage is 5.0V ± 4% (see Electrical Characteristics), and a negative temperature coefficient (NTC) resistor can be used to sum into the FB pin to create an output voltage that decreases with temperature. See Figure 8 for the necessary connections.

![Figure 8. Temperature Dependent Output Using an NTC Resistor Divider](image-url)
APPLICATIONS INFORMATION

where:

\[ R_{NTC(25)} = \text{Resistance of the NTC resistor at 25°C} \]
\[ \beta = \text{Material-specific constant of NTC resistor} \]

Specified at two temperatures such as \( \beta_{25/85} \). If more than two \( \beta \)s are specified, use the most appropriate for the application.

\[ T = \text{Absolute temperature in Kelvin} \]
\[ T_{25} = \text{Room temperature in Kelvin (298.15K)} \]

SWITCH CURRENT LIMIT (CSP-CSN CURRENT SENSING)

The external current sense resistor (\( R_{SENSE} \)) sets the maximum peak current. The maximum voltage across \( R_{SENSE} \) is 50mV (typical) at very low switch duty cycles, and then slope compensation decreases the current limit as the duty cycle increases (see the Max Current Limit vs Duty Cycle (CSP-CSN) plot in the Typical Performance Characteristics). The equation below gives the switch current limit for a given duty cycle and current sense resistor (find \( V_{CSPN} \) at the operating duty cycle in the plot mentioned).

\[
I_{SW \text{(LIMIT)}} = \frac{V_{CSPN}}{R_{SENSE}}
\]

To provide a desired load current for any given application, \( R_{SENSE} \) must be sized appropriately. The equation below calculates \( R_{SENSE} \) for a desired output current:

\[
R_{SENSE} \leq 0.74 \times \eta \times \frac{V_{CSPN}}{I_{OUT}} \times (1 - DC_{MAX}) \times \left(1 - \frac{i_{\text{RIPPLE}}}{2}\right)
\]

\[ \eta = \text{Converter efficiency (assume ~90%)} \]
\[ V_{CSPN} = \text{Max current limit voltage (see Max Current Limit vs Duty Cycle (CSP-CSN) plot in the Typical Performance Characteristics)} \]
\[ I_{OUT} = \text{Converter load current} \]
\[ DC_{MAX} = \text{Switching duty cycle at minimum } V_{IN} \text{ (see Power Switch Duty Cycle in Appendix)} \]
\[ i_{\text{RIPPLE}} = \text{Peak-to-peak inductor ripple current percentage at minimum } V_{IN} \text{ (recommended to use 25%)} \]

ISP-ISN CURRENT SENSING

CSP/CSN current sensing is used in switching regulator peak current control.

ISP/ISN current sensing monitors the current of the rectifier switch and helps protect the circuit from overload conditions.

The ISP-ISN circuitry delays switching if the rectifier switch current goes too high. This mechanism also protects the part during short-circuit and overload conditions by keeping the current through the inductor under control.

Let’s see a buck mode example.

A potential controllability problem could occur under short-circuit conditions without rectifier switch current sensing. If the power supply output is short circuited, the feedback amplifier (EA) responds to the low output voltage by raising the control voltage, \( V_C \), to its peak current limit value. Ideally, the top switch would be turned on, and then turned off as its current exceeded the value indicated by \( V_C \). However, there is finite response time involved in both the current comparator and turnoff of the top switch. These result in a minimum on time, \( t_{\text{ON(MIN)}} \). When combined with high \( V_{IN} \), the potential exists for a loss of control.
APPLICATIONS INFORMATION

Expressed mathematically the requirement to maintain control is:

\[ f \cdot t_{\text{ON}} \leq \frac{V_{R(\text{SENSE})_L} + V_{DS_{-}\text{NMOS}} + I \cdot R}{V_{\text{IN}}}, \]

where:
- \( f \) = switching frequency
- \( t_{\text{ON}} \) = switch minimum on time
- \( V_{R(\text{SENSE})_L} \) = voltage drop on high side sense resistor
- \( V_{DS_{-}\text{NMOS}} \) = voltage drop on high side PMOS switch
- \( V_{\text{IN}} \) = Input voltage
- \( I \cdot R \) = inductor \( I \cdot R \) voltage drop

If this condition is not observed, the current will not be limited at \( I_{PK} \), but will cycle-by-cycle ratchet up to some higher value. With rectifier switch current sensing, the current through the inductor would be controlled under the whole clock cycle. The switching will only resume once rectifier switch current has fallen below \( I_{PK} \).

ISP-ISN current sensing is also used in reverse current detecting for DCM operation.

CURRENT SENSE FILTERING

Certain applications may require filtering of the current sense signals due to excessive switching noise that can appear across \( R_{\text{SENSE}_1} \) and/or \( R_{\text{SENSE}_2} \). Higher operating voltages, higher inductor current, higher values of \( R_{\text{SENSE}} \), and more capacitive MOSFETs will all contribute additional noise across \( R_{\text{SENSE}} \) when MOSFETs transition. The CSP/CSN and/or the ISP/ISN sense signals can be filtered by adding one of the RC networks shown in Figure 10. The filter shown in Figure 10a filters out differential noise, whereas the filter in Figure 10b filters out the differential and common mode noise at the expense of an additional capacitor and approximately twice the capacitance value. It is recommended to Kelvin tie the ground connection directly to the paddle of the LT8711 if using the filter in Figure 10b. The filter network should be placed as close as possible to the LT8711. Resistors greater than 10Ω should be avoided as this can increase the offset voltages at the CSP/CSN and ISP/ISN pins.

<table>
<thead>
<tr>
<th>Table 6. CSP/CSN, ISP/ISN Bias Current:</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CM} = 0V )</td>
</tr>
<tr>
<td>( I_{\text{CSP \ (typ)}} )</td>
</tr>
<tr>
<td>( I_{\text{CSN \ (typ)}} )</td>
</tr>
<tr>
<td>( I_{\text{ISP \ (typ)}} )</td>
</tr>
<tr>
<td>( I_{\text{ISN \ (typ)}} )</td>
</tr>
</tbody>
</table>

When \( V_{CM} \) changes from 0V to 3V, bias current changes gradually from low side values to high side values as shown in Table 6.

CSN/ISN bias current at high side is proportional to temperature (see the CSN/ISN Bias Current vs Temperature plots in the Typical Performance Characteristics).

Positive bias currents flow into the pins. Negative bias currents flow out of the pins.

Bias current of 4µA ~ 25µA and –4µA ~ –25µA in the table changes according to the \( V_C \) voltage. 4µA (–4µA) corresponds to the minimum \( V_C \) voltage. 25µA (–25µA) corresponds to the maximum \( V_C \) voltage.

SWITCHING FREQUENCY

The LT8711 uses a constant frequency architecture whose frequency can be between 100kHz and 750kHz. The frequency can be set using the internal oscillator or can be synchronized to an external clock source. Selection of
APPLICATIONS INFORMATION

The switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. The switching frequency can be set by placing an appropriate resistor from the RT pin to ground and tying the SYNC pin low. The frequency can also be synchronized to an external clock source driven into the SYNC pin. The following sections provide more details.

Oscillator Timing Resistor (RT)
The operating frequency of the LT8711 can be set by the internal free-running oscillator. When the SYNC pin is driven low (< 0.4V), the frequency of operation is set by a resistor from the RT pin to ground. The oscillator frequency is calculated using the following formula:

\[ f = \frac{25000}{R_T + 2} \]

where \( f \) is in kHz and \( R_T \) is in kΩ. Conversely, \( R_T \) can be calculated from the desired frequency using:

\[ R_T = \frac{25000}{f} - 2 \]

Clock Synchronization
An external source can set the operating frequency of the LT8711 by providing a digital clock signal into the SYNC pin (RT resistor still required). The LT8711 will operate at the SYNC clock frequency. The LT8711 will revert to its internal free-running oscillator clock when the SYNC pin is driven below 0.4V for a few free-running clock periods. The LT8711 will operate in FCM mode with internal free-running oscillator clock if driving SYNC high for an extended period of time.

The duty cycle of the SYNC signal must be between 20% and 80% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

1. SYNC may not toggle outside the frequency range of 140kHz to 750kHz unless it is stopped below 0.4V to enable the free-running oscillator.

2. The SYNC frequency can always be higher than the free-running oscillator frequency (as set by the RT resistor), \( f_{OSC} \), but should not be less than 20% below \( f_{OSC} \).

LDO REGULATORS
The LT8711 has two linear regulators to run the BG and TG gate drivers. The INTVCC LDO regulates 5V (typical) above ground, and the INTVEE regulator regulates 5.15V (typical) below the BIAS pin.

INTVCC LDO Regulator
The INTVCC LDO is used as the top rail for the BG gate driver. An external capacitor greater than 2.2μF must be placed from the INTVCC pin to ground. The capacitor should have low ESR, such as a ceramic capacitor.

The INTVCC LDO can run off \( V_{IN} \) or EXTVCC and will intelligently select to run off the best rail for minimizing chip power loss, but at the same time, select the proper input for maintaining INTVCC as close to 5V as possible. For example, Figure 11 is a plot that shows how \( V_{IN} \) or EXTVCC is selected.

Overcurrent protection circuitry typically limits the maximum current draw from the LDO to ~50mA. If the selected input voltage is greater than 24V (typical), then the current limit of the LDO reduces linearly with input voltage to limit the maximum power in the INTVCC pass device. See the INTVCC Current Limit vs \( V_{IN} \) or EXTVCC plot in the Typical Performance Characteristics.

![Figure 11. INTVCC Input Voltage Selection](image)
APPLICATIONS INFORMATION

Power dissipated in the INTVCC LDO should be minimized to improve efficiency and prevent overheating of the LT8711. The current limit reduction with input voltage circuit helps prevent the part from overheating, but these guidelines should be followed. The maximum current drawn through the INTVCC LDO occurs under the following conditions:

1. Large (capacitive) MOSFETs being driven at high frequencies
2. The converter’s switch voltage (VIN for BUCK, VOUT for BOOST and BUCK-BOOST, VIN + VOUT for SEPIC converters) is high, thus requiring more charge to turn the MOSFET gates on and off.

In general, use appropriately sized MOSFETs and lower the switching frequency for higher voltage applications to keep the INTVCC current at a minimum.

INTVEE LDO Regulator

The BIAS and INTVEE voltages are used for the top and bottom rails of the TG gate driver respectively. An external capacitor greater than 2.2μF must be placed between the BIAS and INTVEE pins. The capacitor should have low ESR, such as ceramic capacitor.

Overcurrent protection circuitry typically limits the maximum current draw from the regulator to ~80mA. If the BIAS voltage is greater than 15V (typical), then the current limit of the regulator reduces linearly with input voltage to limit the maximum power in the INTVEE pass device. See the INTVEE Current Limit vs BIAS plot in the Typical Performance Characteristics.

The same thermal guidelines from the INTVCC LDO Regulator section apply to the INTVEE regulator as well.

NONSYNCHRONOUS CONVERTER

It may be desirable in some applications to replace the external PFET with a Schottky diode to make a nonsynchronous converter. One example would be a high output voltage application because the voltage drop across the rectifier has a small effect on the efficiency of the converter. In fact, for high output voltage applications, replacing the PFET with a Schottky may result in higher efficiency because the LT8711 doesn’t have to supply gate drive to the PFET. Figure 12 shows the recommended connections for using the LT8711 as a nonsynchronous boost converter, however the same concept can be used for any other converter topology.

Figure 12. Simplified Schematic of a Nonsynchronous Boost Converter

LAYOUT GUIDELINES FOR BUCK, BOOST, SEPIC, ZETA AND BUCK-BOOST TOPOLOGIES

General Layout Guidelines

- To optimize thermal performance, solder the exposed pad of the LT8711 to the ground plane with multiple vias around the pad connecting to additional ground planes.
- High speed switching path (see specific topology below for more information) must be kept as short as possible.
- The FB, VC and RT components should be placed as close to the LT8711 as possible, while being far away as practically possible from switching nodes. The ground for these components should be separated from the switch current path.
- Place bypass capacitors for the VIN and EXTVCC pins (1μF or greater) as close as possible to the LT8711.
- Place bypass capacitors for the INTVCC and INTVEE (between BIAS and INTVEE) pins (2.2μF or greater) as close as possible to the LT8711.
APPLICATIONS INFORMATION

- The load should connect directly to the positive and negative terminals of the output capacitor for best load regulation.

BUCK Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing MN, MP, C\text{IN}, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

![Figure 13. Suggested Component Placement for Buck Topology](image1)

Boost Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing MN, MP, C\text{OUT}, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

![Figure 14. Suggested Component Placement for Boost Topology](image2)

SEPIC Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing R\text{SENSE}1, MN, C1, MP, R\text{SENSE}2, C\text{OUT}, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

![Figure 15. Suggested Component Placement for SEPIC Topology](image3)

ZETA Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing R\text{SENSE}1, MN, C1, MP, R\text{SENSE}2, C\text{IN}, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

![Figure 16. Suggested Component Placement for ZETA Topology](image4)
APPLICATIONS INFORMATION

Buck-Boost Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing $R_{S\text{ENSE1}}$, $\text{DIO1}$, $\text{MP}$, $\text{C_IN}$, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

- Keep length of loop (high speed switching path) governing $R_{S\text{ENSE2}}$, $\text{MN}$, $\text{DIO2}$, $\text{C_OUT}$, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

Current Sense Resistor Layout Guidelines

- Route the CSP/CSN and ISP/ISN lines differentially (close together) from the chip to the current sense resistor as shown in Figure 17.

- Place the vias that connect the CSP/CSN and ISP/ISN lines directly at the terminals of the current sense resistor as shown in Figure 17.

THERMAL CONSIDERATIONS

Overview

The primary components on the board that consume the most power and produce the most heat are the power switches, MN and MP, the power inductor, the Schottky diodes in the nonsynchronous buck-boost converter and the LT8711 IC. It is imperative that a good thermal path be provided for these components to dissipate the heat generated within the packages. This can be accomplished by taking advantage of the thermal pads on the underside of the packages. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from each of these components and into a copper plane with as much area as possible. For the case of the power switches, the copper area of the drain connections shouldn’t be too big as to create a large EMI surface that can radiate noise around the board.

Power MOSFET Loss and Thermal Calculations

The LT8711 requires two external power MOSFETs, an NFET switch for the BG gate driver and a PFET switch for the TG gate driver. Important parameters for estimating the power dissipation in the MOSFETs are:

1. On-resistance ($R_{DS(\text{ON})}$)
2. Gate-to-drain charge ($Q_{GD}$)
3. PFET body diode forward voltage ($V_{BD}$)
4. $V_{DS}$ of the FETs during their Off-Time
5. Switch current ($I_{SW}$)
6. Switching frequency ($f$)

The power loss in each power switch has a DC and AC term. The DC term is when the power switch is fully on, and the AC term is when the power switch is transitioning from on-off or off-on.
The following applies for both the NFET and PFET power switches. Below are the equations for the power loss in MN and MP.

\[
\begin{align*}
P_{\text{MOSFET}} &= P_{\text{IR}} + P_{\text{SWITCHING}} \\
P_{\text{MN}} &= I_{\text{IN}}^2 \cdot R_{\text{DS(ON)}} + V_{\text{DS}} \cdot I_{\text{IN}} \cdot f \cdot t_{\text{RF}} + P_{\text{RR-N}} \\
P_{\text{MP}} &= I_{\text{IP}}^2 \cdot R_{\text{DS(ON)}} + V_{\text{BD}} \cdot \left( I_{\text{IPK}} + \frac{I_{\text{IVY}}}{1.6} \right) \cdot f \cdot 140 \cdot n_x + P_{\text{RR-P}} \\
I_{\text{PK}} &= I_{\text{SW}} + \frac{I_{\text{RIPPLE}}}{2}; I_{\text{IVY}} = I_{\text{SW}} - \frac{I_{\text{RIPPLE}}}{2} \\
P_{\text{RR-N}} &\approx \frac{V_{\text{DS}} \cdot I_{\text{RR}} \cdot t_{\text{RR}} \cdot f}{2} \\
P_{\text{RR-P}} &\approx \frac{V_{\text{DS}} \cdot I_{\text{RR}} \cdot t_{\text{RR}} \cdot f}{2}
\end{align*}
\]

where:

- \( f \) = Switching Frequency
- \( I_{\text{IN}} \) = NFET RMS Current
- \( I_{\text{IP}} \) = PFET RMS Current
- \( t_{\text{RF}} \) = Average of the rise and fall times of the NFET's drain voltage
- \( I_{\text{SW}} \) = Average switch current during its on-time
- \( I_{\text{PK}} \) = Peak inductor current
- \( I_{\text{IVY}} \) = Valley inductor current
- \( I_{\text{RIPPLE}} \) = Inductor ripple current
- \( DC \) = Switch duty cycle (see Power Switch Duty Cycle section in Appendix)
- \( V_{\text{BD}} \) = PFET body diode forward voltage at \( I_{\text{SW}} \)
- \( V_{\text{DS}} \) = Voltage across the FET when it's off.
- \( P_{\text{RR-N}} \) = PFET body diode reverse recovery power loss in the NFET
- \( P_{\text{RR-P}} \) = PFET body diode reverse recovery power loss in the PFET
- \( I_{\text{RR}} \) = Current needed to remove the PFET body diode charge
- \( t_{\text{RR}} \) = Reverse recovery time of PFET body diode

Typical values for \( t_{\text{RF}} \) are 10ns to 40ns depending on the MOSFET capacitance and drain voltage. In general, the lower the QGD of the MOSFET, the faster the rise and fall times of its drain voltage. For best calculations, measure the rise and fall times in the application.

PFET body diode reverse recovery power loss is dependent on many factors and can be difficult to quantify in an application. In general, this power loss increases with higher \( V_{\text{DS}} \) and/or higher switching frequency.

**Chip Power and Thermal Calculations**

Power dissipation in the LT8711 chip comes from three primary sources: INTVCC and INTVEE LDOs providing gate drive to the BG and TG pins and the chip quiescent current. The average current through each LDO is determined by the gate charge of the power switches, MN and MP, and the switching frequency. Below are the equations for calculating the chip power loss.

The INTVCC LDO primarily supplies voltage for the BG gate driver. The BIAS and INTVEE voltages supply the top and bottom rails of the TG gate driver respectively. The chip Q current comes from INTVCC. Below are the chip power equations:

\[
\begin{align*}
P_{\text{INTVCC BG}} &= Q_{\text{MN}} \cdot f \cdot V_{\text{SELECT}} \\
P_{\text{INTVCC Q}} &= 2 \text{mA} \cdot V_{\text{SELECT}} \\
P_{\text{INTVEE}} &= Q_{\text{MP}} \cdot f \cdot V_{\text{BIAS}}
\end{align*}
\]

where:

- \( f \) = Switching frequency
- \( Q_{\text{MN}} \) = Total gate charge of NFET power switch (MN)
- \( Q_{\text{MP}} \) = Total gate charge of PFET power switch (MP)
- \( V_{\text{SELECT}} \) = INTVCC LDO selected input voltage, \( V_{\text{IN}} \) or \( \text{EXTVCC} \) (see LDO Regulators section)

**Thermal Lockout**

If the die temperature reaches ~165°C, the part will go into shutdown, so the power switches turn off and the soft-start capacitor will be discharged. The LT8711 will come out of shutdown when the die temperature drops by ~5°C (typical).
APPENDIX

POWER SWITCH DUTY CYCLE

The external power main switch (PFET in the Block Diagram) cannot remain off for 100% of each clock cycle, and will turn on for a minimum on time (MinOnTime) when in regulation. This MinOnTime governs the minimum allowable duty cycle given by:

\[ DC_{\text{MIN}} = \left( \frac{\text{MinOnTime}}{T_P} \right) \times 100\% \]

where TP is the clock period and MinOnTime (found in the Electrical Characteristics) is 100ns (typ).

The application should be designed such that the operating duty cycle is higher than DC_{MIN}.

Duty cycle equations for different topologies are given below.

For the Buck topology (see Figure 3):

\[ DC_{\text{BUCK}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \]

For the Boost topology (see Figure 4):

\[ DC_{\text{BOOST}} = 1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}} \]

For the SEPIC topology (see Figures 6):

\[ DC_{\text{SEPIC}} = \frac{V_{\text{OUT}}}{V_{\text{IN}} + V_{\text{OUT}}} \]

For the ZETA topology (see Figures 7):

\[ DC_{\text{ZETA}} = \frac{V_{\text{OUT}}}{V_{\text{IN}} + V_{\text{OUT}}} \]

For the Buck-Boost topology (see Figures 8):

\[ DC_{\text{BUCK-BOOST}} = \frac{V_{\text{OUT}}}{V_{\text{IN}} + V_{\text{OUT}}} \]

INDUCTOR SELECTION

For high efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. Additionally, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper-wire resistance) to reduce \( I^2R \) losses, and must be able to handle the peak inductor current without saturating. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology where each inductor carries a fraction of the total switch current. Molded chokes or chip inductors do not have enough core area to support peak inductor currents in the 5A to 15A range. To minimize radiated noise, use a toroidal or shielded inductor. See Table 7 for a list of inductor manufacturers.

Table 7. Inductor Manufacturers

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Series</th>
<th>Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coilcraft</td>
<td>MSS1278, XAL1010, and MSD1278 Series</td>
<td><a href="http://www.coilcraft.com">www.coilcraft.com</a></td>
</tr>
<tr>
<td>Cooper Bussmann</td>
<td>DRQ127, DR127, and HCM1104 Series</td>
<td><a href="http://www.cooperbussmann.com">www.cooperbussmann.com</a></td>
</tr>
<tr>
<td>Vishay</td>
<td>IHLP Series</td>
<td><a href="http://www.vishay.com">www.vishay.com</a></td>
</tr>
<tr>
<td>Würth</td>
<td>WE-DCT Series</td>
<td><a href="http://www.we-online.com">www.we-online.com</a></td>
</tr>
</tbody>
</table>

Minimum Inductance

Although there can be a trade-off with efficiency, it is often desirable to minimize board space by choosing smaller inductors. When choosing an inductor, there are two conditions that limit the minimum inductance; (1) providing adequate load current, and (2) avoidance of subharmonic oscillation.

Adequate Load Current

Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be provided to the load.

Avoiding Subharmonic Oscillations

The LT8711’s internal slope compensation circuit will prevent subharmonic oscillations that can occur when the duty cycle is greater than 50%, provided that the inductance exceeds a minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

\[ L_{\text{MIN}} \geq \frac{V_{\text{IN}} \cdot R_{\text{SENSE}} \cdot (2 \cdot \text{DC} - 1)}{40m \cdot \text{DC} \cdot f}, \text{ Buck Topology} \]

\[ L_{\text{MIN}} \geq \frac{V_{\text{IN}} \cdot R_{\text{SENSE}} \cdot (2 \cdot \text{DC} - 1)}{40m \cdot \text{DC} \cdot f \cdot (1-\text{DC})}, \text{ Other Topologies} \]
where

\[ L_{\text{MIN}} = L_1 \text{ for buck, boost and buck-boost topologies} \]
\[ L_{\text{MIN}} = L_1 = L_2 \text{ for coupled dual inductor topologies} \]
\[ (\text{SEPIC and ZETA}) \]
\[ L_{\text{MIN}} = L_1 || L_2 \text{ for uncoupled dual inductor topologies} \]
\[ (\text{SEPIC and ZETA}) \]

**Inductor Current Rating**

The inductor(s) must have a rating greater than its (their) peak operating current to prevent inductor saturation, which would result in efficiency losses.

**POWER MOSFET SELECTION**

The LT8711 requires two external power MOSFETs, an NFET switch for the BG gate driver and a PFET switch for the TG gate driver. It is important to select MOSFETs for optimizing efficiency. For choosing an NFET and PFET, the important device parameters are:

1. Breakdown voltage (\(BV_{\text{DSS}}\))
2. Gate threshold voltage (\(V_{\text{GSTH}}\))
3. On-resistance (\(R_{\text{DS(ON)}}\))
4. Total gate charge (\(Q_{G}\))
5. Turn-off delay time (\(t_{\text{D(OFF)}}\))
6. Package has exposed paddle

If operating close to the \(BV_{\text{DSS}}\) rating of the MOSFET, check the leakage specifications on the MOSFET because leakage can decrease the efficiency of the converter.

The NFET and PFET gate-to-source drive is 5V typical. The BG gate driver can begin switching when the \(\text{INTV}_{\text{CC}}\) voltage exceeds ~4.1V, so ensure the selected NFET is in the linear mode of operation with 4.1V of gate-to-source drive to prevent possible damage to the NFET.

The TG gate driver can begin switching when the \(\text{BIAS-INTV}_{\text{EE}}\) voltage exceeds ~3.85V, so it is optimal that the PFET be in the linear mode of operation with 3.85V of gate-to-source drive. Try to choose a PFET with a low body diode reverse recovery time to minimize stored charge in the PFET. The stored charge in the PFET body diode gets removed when the NFET switch turns on and can lead to efficiency hits especially in applications where the \(V_{\text{DS}}\) of the PFET (during off-time) is high. For these applications, it may be beneficial to put a Schottky diode across the PFET to reduce the amount of charge in the PFET body diode.

Power MOSFET on-resistance and total gate charge go hand-in-hand and are typically inversely proportional to each other; the lower the on-resistance, the higher the total gate charge. Choose MOSFETs with an on-resistance to give a voltage drop to be less than 300mV at the peak current. At the same time, choose MOSFETs with a lower total gate charge to reduce LT8711 power dissipation and MOSFET switching losses.

The turn-off delay time (\(t_{\text{D(OFF)}}\)) of available NFETs is generally smaller than the LT8711’s non-overlap time. However, the turn-off time of the available PFETs should be looked at before deciding on a PFET for a given application. The turn-off time must be less than the non-overlap time of the LT8711 or else the NFET and PFET could be on at the same time and damage to external components may occur. If the PFET turn-off delay time as specified in the data sheet is less than the LT8711 non-overlap time, then the PFET is good to use. If the turn-off delay time is longer than the non-overlap time, it doesn’t necessarily mean it can’t be used. It may be unclear how the PFET manufacturer measures the turn-off delay time, so it is best to measure the PFET turn-off delay time with respect to the PFET gate voltage.

Finally, both the NFET and PFET power MOSFETs should be in a package with an exposed paddle for the drain connection to be able to dissipate heat. The on-resistance of MOSFETs is proportional to temperature, so it’s more efficient if the MOSFETs are running cool with the help of the exposed paddle. See Table 8 for a list of power MOSFET manufacturers.

**Table 8. Power MOSFET (NFET and PFET) Manufacturers**

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fairchild Semiconductor</td>
<td><a href="http://www.fairchildsemi.com">www.fairchildsemi.com</a></td>
</tr>
<tr>
<td>On-Semiconductor</td>
<td><a href="http://www.onsemi.com">www.onsemi.com</a></td>
</tr>
<tr>
<td>Vishay</td>
<td><a href="http://www.vishay.com">www.vishay.com</a></td>
</tr>
<tr>
<td>Diodes Inc.</td>
<td><a href="http://www.diodes.com">www.diodes.com</a></td>
</tr>
</tbody>
</table>
INPUT AND OUTPUT CAPACITOR SELECTION

Input and output capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out of the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low ESR (equivalent series resistance). Tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available.

Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching noise. A minimum 1μF ceramic capacitor should also be placed from \( V_{IN} \) to GND and from EXTVCC to GND as close to the LT8711 pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

COMPENSATION – ADJUSTMENT

To compensate the feedback loop of the LT8711, a series resistor capacitor network in parallel with an optional single capacitor should be connected from the \( V_C \) pin to GND. For most applications, choose a series capacitor in the range of 0.47nF to 10nF with 2.2nF being a good starting value. The optional parallel capacitor should range in value from 47pF to 220pF with 100pF being a good starting value. The compensation resistor, \( R_C \), is usually in the range of 10k to 100k. A good technique to compensate a new application is to use a 100k potentiometer in place of the series resistor \( R_C \). With the series and parallel capacitors at 2.2nF and 100pF respectively, adjust the potentiometer while observing the transient response and the optimum value for \( R_C \) can be found. The series capacitor can be reduced or increased from 2.2nF to speed up the converter or slow down the converter, respectively.
TYPICAL APPLICATIONS

400kHz, 5V–40V Input to 3.3V/6.5A Buck

Efficiency vs Load Current

Transient Response with 2A to 5.5A to 2A Output Load Step

LT8711

For more information www.analog.com
**TYPICAL APPLICATIONS**

400kHz, 12V Input to 24V/3A Boost Converter

![Circuit Diagram]

- **L1**: WÜRTH 8.2µH WE-HCI 7443550820
- **M1**: INFINEON BSC026N04
- **M2**: ST STL60P4LLF6
- **CIN**: 10µF, 50V, X7R
- **COUT**: 6.8µF, 50V, X7R

ADDITIONAL 47µF, 50V ELECTROLYTIC CAP ON VIN
ADDITIONAL 270µF, 50V ELECTROLYTIC CAP ON VOUT

**Efficiency vs Load Current**

![Graph]

**Transient Response with 1A to 2.5A to 1A Output Load Step (VIN = 12V)**

![Graph]

For more information [www.analog.com](http://www.analog.com)
200kHz, 4.5V–40V Input to 12V/4A SEPIC

V<sub>IN</sub> 4.5V TO 40V

L1: COILCRAFT 8.2µH XAL1510-822ME
L2: COILCRAFT 15µH XAL1510-153ME
M1: VISHAY SIR826ADP
M2: ST STL42P6LLF6

C<sub>IN</sub>: 10µF, 50V, X7R
ADDITIONAL 56µF, 50V ELECTROLYTIC CAP ON VIN
C<sub>OUT</sub>: 22µF, 25V, X7R
ADDITIONAL 270µF, 25V ELECTROLYTIC CAP ON VOUT

Transient Response with 2A to 4A to 2A Output Load Step (V<sub>IN</sub> = 12V)

Efficiency vs Load Current

For more information www.analog.com
TYPICAL APPLICATIONS

200kHz, 5V–40V Input to 12V/3.5A ZETA Converter

V_IN 5V TO 40V
C_IN 10µF, 6

EN/FBIN V_IN BIAS
EXTVCC
LT8711

INTVCC
TG
CSP
CSN

ISN
ISP

CSP
CSN

2.2µF
2.2µF

10µF ×3

1.1k
330nF

100pF
1nF

BG

R_T
118k

SYNC

1M

RT
330nF

100pF
1nF

GND

CIN
10µF ×6

VIN
5V TO 40V

L1B
10µH
L1A
10µH

R_FB1
69.8k

1M

COUT
22µF ×4

R_FB2
69.8k

R_FB
69.8k

VIN
5V TO 40V

L1: COILCRAFT 10µH MSD1583-103
M1: VISHAY SiR826ADP
M2: VISHAY Si7461DP
CIN: 10µF, 50V, X7R
ADDITIONAL 56µF 50V ELECTROLYTIC CAP ON VIN
COUT: 270µF 25V ELECTROLYTIC CAP ON VOUT

Efficiency vs Load Current

Efficiency (%)

LOAD CURRENT (A)

100
90
80
70
60
50
40
30
20
10
0

0.001
0.01
0.1
1
10

4

VIN = 6V
VIN = 12V
VIN = 24V

Transient Response with 1.5A to 3A to 1.5A
Output Load Step (VIN = 16V)

LOAD STEP
2A/DIV

VOUT
200mV/DIV

I_L1
2A/DIV

400µs/DIV

LOAD STEP
2A/DIV

VOUT
200mV/DIV

I_L1
2A/DIV

400µs/DIV
400kHz, 5V–40V Input to 12V/3.5A Buck-Boost Converter

TYPICAL APPLICATIONS

400kHz, 5V–40V Input to 12V/3.5A Buck-Boost Converter

Efficiency vs Load Current

Transient Response with 1.5A to 3A to 1.5A Output Load Step (VIN = 9V)

LT8711

For more information www.analog.com
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT8711#packaging for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation CB

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
   *DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

For more information www.analog.com
PACKAGE DESCRIPTION

Please refer to [http://www.linear.com/product/LT8711#packaging](http://www.linear.com/product/LT8711#packaging) for the most recent package drawings.

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-1742 Rev Ø)

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

For more information [www.analog.com](http://www.analog.com)
## REVISION HISTORY

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<th>REV</th>
<th>DATE</th>
<th>DESCRIPTION</th>
<th>PAGE NUMBER</th>
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<tbody>
<tr>
<td>A</td>
<td>04/18</td>
<td>Changed from 25mV to 27mV in last sentence.</td>
<td>13</td>
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**TYPICAL APPLICATION**

Boost Pre-Regulator for Automotive Stop-Start/Idle

**RELATED PARTS**

<table>
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<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
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<tr>
<td>LT3757A</td>
<td>Boost, Flyback, SEPIC and Inverting Controller</td>
<td>2.9V ≤ VIN ≤ 40V, 100kHz to 1MHz Programmable Operating Frequency, 3mm × 3mm DFN-10 and MSOP-10E</td>
</tr>
<tr>
<td>LT3758A</td>
<td>Boost, Flyback, SEPIC and Inverting Controller</td>
<td>5.5V ≤ VIN ≤ 100V, 100kHz to 1MHz Programmable Operating Frequency, 3mm × 3mm DFN-10 and MSOP-10E</td>
</tr>
<tr>
<td>LT3957A</td>
<td>Boost, Flyback, SEPIC and Inverting Converter with 5A, 40V Switch</td>
<td>3V ≤ VIN ≤ 40V, 100kHz to 1MHz Programmable Operating Frequency, 5mm × 6mm QFN</td>
</tr>
<tr>
<td>LT3958</td>
<td>Boost, Flyback, SEPIC and Inverting Converter with 3.3A, 84V Switch</td>
<td>5V ≤ VIN ≤ 80V, 100kHz to 1MHz Programmable Operating Frequency, 5mm × 6mm QFN</td>
</tr>
<tr>
<td>LT8705A</td>
<td>80V VIN and VOUT Synchronous 4-Switch Buck-Boost DC/DC Controller</td>
<td>2.8V ≤ VIN ≤ 80V, 100kHz to 400kHz Programmable Operating Frequency, 5mm × 7mm QFN-38 and TSSOP-38</td>
</tr>
<tr>
<td>LT8709</td>
<td>Negative Input Synchronous Multitopology DC/DC Control</td>
<td>–80V ≤ VIN ≤ –4.5V, Up to 400kHz Programmable Operating Frequency, TSSOP-20</td>
</tr>
<tr>
<td>LT8710</td>
<td>Synchronous SEPIC/Inverting/Boost Controller with Output Current Control</td>
<td>4.5V ≤ VIN ≤ 80V, 100kHz to 1MHz Programmable Operating Frequency, TSSOP-20</td>
</tr>
<tr>
<td>LT8714</td>
<td>Bipolar Output Synchronous Controller with Seamless Four Quadrant Operation</td>
<td>4.5V ≤ VIN ≤ 80V, Output Can Source or Sink Current for Any Output Voltage, Switching Frequency Up to 750kHz, 20-Lead TSSOP</td>
</tr>
</tbody>
</table>