18V/8A Step-Down Silent Switcher 3 with Ultralow Noise Reference

FEATURES

- **Silent Switcher®3 Architecture**
  - **Ultralow RMS Noise (10Hz to 100kHz): 4μV_{RMS}**
  - **Ultralow Spot Noise: 4nV/√Hz at 10kHz**
  - **Ultralow EMI Emissions on Any PCB**
  - **Internal Bypass Capacitors Reduce Radiated EMI**
- **High Efficiency at High Frequency**
- **Ultrafast Transient Response: 1μs**
- **Fast Minimum Switch On-Time: 15ns**
- **Input Voltage Range: 2.7V to 18V**
- **Output Voltage Range: 0V to (PV_{IN} - 0.5V)**
- **8A Maximum Continuous Output Current**
- **Precision Reference: ± 0.8% Over Temperature with Remote Sense**
- Supports Dynamic Output Voltage Control
- PolyPhase® Operation: Up to 12 Phases
- Forced Continuous Mode Capability
- Adjustable and Synchronizable: 300kHz to 4MHz
- Programmable Power Good
- Small 20-Lead 4mm × 3mm (LT8625SP) or 24-Lead 4mm × 4mm (LT8625SP-1) LQFN Exposed Back Package for Optional Heat Sink Mount

APPLICATIONS

- RF Power Suppliers: PLLs, VCOs, Mixers, LNAs, PAs
- High Speed/High Precision ADCs/DACs
- Low Noise Instrumentation

DESCRIPTION

The LT®8625SP/LT8625SP-1 synchronous step-down regulator features third-generation Silent Switcher technology which is uniquely designed to combine an ultralow noise reference with Silent Switcher architecture in order to achieve both high efficiency and excellent wideband noise performance.

The innovative ultralow noise architecture provides exceptional low frequency (0.1Hz to 100kHz) output noise performance in a switching regulator. The output voltage can be programmed with a single resistor, resulting in virtually constant output noise independent of output voltage.

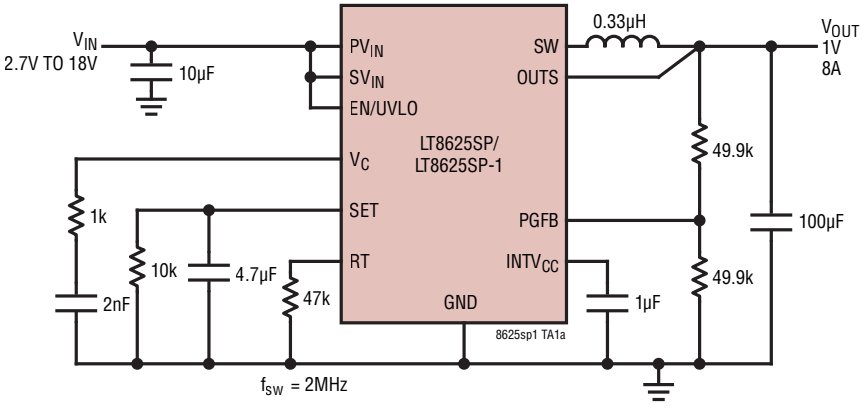
Silent Switcher architecture minimizes EMI emissions while delivering high efficiency at high switching frequencies. The top of the package features exposed die for optional heat sink attachment which can be used to significantly improve thermal performance.

The LT8625SP/LT8625SP-1 is ideal for high current, noise sensitive applications which benefit from the high efficiency of a synchronous switching regulator.

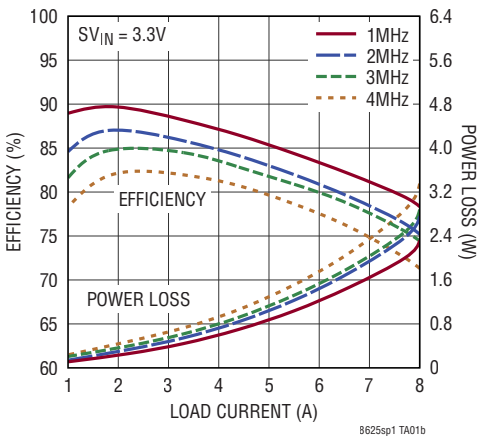
	PACKAGE SIZE	MAX TEMP	EXPOSED BACK	$INTV_{CC}$ CAPACITOR
LT8625S	4mm × 3mm	125°C	No	Internal
LT8625SP	4mm × 3mm	150°C	Yes	External
LT8625SP-1	4mm × 4mm	150°C	Yes	External

Note: The LT8625SP-1 (8A) is Pin-to-Pin Compatible with the LT8627SP (16A).

TYPICAL APPLICATION



$12V_{IN}$ to 1 V_{OUT} Efficiency



Rev. D

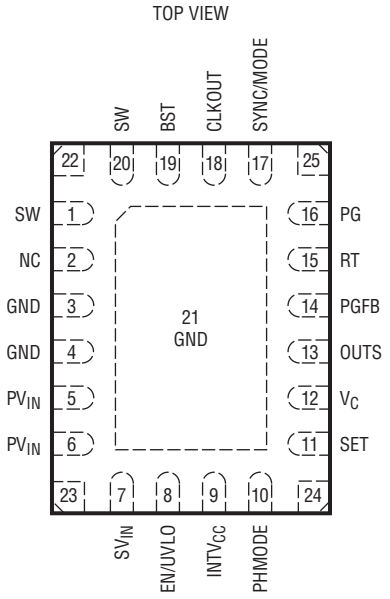
ABSOLUTE MAXIMUM RATINGS (Note 1)

PV_{IN}, SV_{IN}, EN/UVLO, PG ..... -0.3V to 18V
SYNC, OUTS, SET, PGFB..... -0.3V to 6V
PHMODE..... -0.3V to 4V

Operating Junction Temperature (Note 2)
LT8625SPJ ..... –40°C to 150°C
LT8625SPJ-1 ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Peak Package Body Temperature..... 260°C

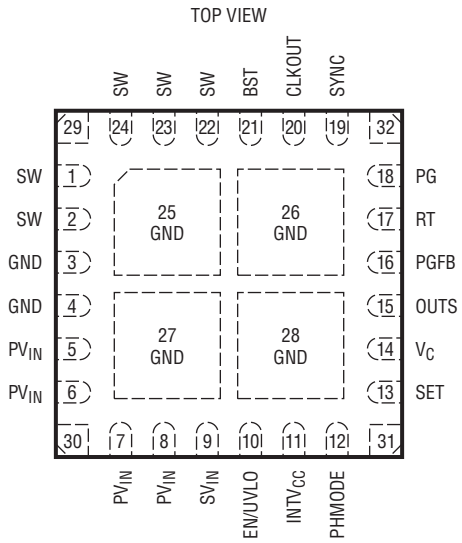
PIN CONFIGURATION

LT8625SP



LQFN PACKAGE
20-LEAD (4mm × 3mm × 0.95mm)
JEDEC BOARD θ_{JA} = 45°C/W, $\theta_{JC(top)}$ = 4.0°C/W, $\theta_{JC(pad)}$ = 12.1°C/W (NOTE 3),
DEMO BOARD: θ_{JA} = 29°C/W, Ψ_{JT} = 1.7°C/W
EXPOSED PAD (PIN 21) IS GND, SHOULD BE SOLDERED TO PCB.
EXPOSED PAD AT TOP OF PACKAGE CAN OPTIONALLY BE ATTACHED
TO HEAT SINK FOR IMPROVED THERMAL PERFORMANCE

LT8625SP-1



LQFN PACKAGE
24-LEAD (4mm × 4mm × 0.95mm)
JEDEC BOARD θ_{JA} = 41°C/W, $\theta_{JC(top)}$ = 4.1°C/W, $\theta_{JC(pad)}$ = 11.4°C/W (NOTE 3)
DEMO BOARD: θ_{JA} = 29°C/W, Ψ_{JT} = 1.7°C/W
EXPOSED PAD (PINS 25 – 28) ARE GND, SHOULD BE SOLDERED TO PCB.
EXPOSED PAD AT TOP OF PACKAGE CAN OPTIONALLY BE ATTACHED
TO HEAT SINK FOR IMPROVED THERMAL PERFORMANCE

ORDER INFORMATION

TAPE AND REEL (MINI)	TAPE AND REEL	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE**	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
			DEVICE	FINISH CODE			
LT8625SPJV#TRMPBF	LT8625SPJV#TRPBF	Au (RoHS)	HNX	e4	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 150°C
LT8625SPJV-1#TRMPBF	LT8625SPJV-1#TRPBF		HPC				

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- *The temperature grade is identified by a label on the shipping container.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

Parts ending with PBF are RoHS and WEEE compliant. **The LT8625SP package has the same dimensions as a standard 4mm × 3mm QFN package. The LT8625SP-1 package has the same dimensions as a standard 4mm × 4mm QFN package.

For more information on lead free part marking, go to: http://www.adi.com/leadfree/
For more information on tape and reel specifications, go to: http://www.adi.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum PV_{IN}	V_{SET} = 1V	●		2.5	2.7	V
Minimum SV_{IN} (Note 8)	V_{SET} = 1V	●		2.5	2.7	V
SET Pin Current (I_{SET})	V_{SET} = V_{OUTS} = 1V	 ●	99.7 99.2	100 100	100.3 100.8	µA µA
Fast Start-Up Set Pin Current	SV_{IN} = 12V, V_{SET} = 1V		2.2	2.7	3.2	mA
Start-Up Time (Notes 5, 11)	V_{OUT} = 1V, C_{SET} = 1µF, SV_{IN} = 12V, V_{PGFB} = 0.5 V_{OUT} = 1V, C_{SET} = 4.7µF, SV_{IN} = 12V, V_{PGFB} = 0.5 V_{OUT} = 1V, C_{SET} = 1µF, SV_{IN} = 12V, $R_{PGFB(TOP)}$ = 49.9k, $R_{PGFB(BOT)}$ = 49.9k V_{OUT} = 1V, C_{SET} = 4.7µF, SV_{IN} = 12V, $R_{PGFB(TOP)}$ = 49.9k, $R_{PGFB(BOT)}$ = 49.9k			25 120 1 2.5		ms ms ms ms
Output Noise Spectral Density (10kHz) (Notes 5, 6, 7)	SV_{IN} = 12V, V_{OUT} = 1V, C_{OUT} = 22µF ×3, L = 180nH, R_{SET} = 10kΩ, C_{SET} = 4.7µF f_{SW} = 4MHz, R_C = 4.99kΩ, C_C = 1nF			4		$nV/\sqrt{Hz}$
Output RMS Noise (10Hz – 100kHz) (Notes 5, 6, 7)	SV_{IN} = 12V, V_{OUT} = 1V, BW = 10Hz–100kHz, C_{OUT} = 22µF ×3, L = 180nH R_{SET} = 10kΩ, C_{SET} = 4.7µF f_{SW} = 4MHz, R_C = 4.99kΩ, C_C = 1nF			3.5		μV_{RMS}
SV_{IN} Quiescent Current	$V_{EN/UVLO}$ = 2V, Not Switching $V_{EN/UVLO}$ = 0.2V, Shutdown			2.8 50	3.3 105	mA µA
Oscillator Frequency	R_T = 392k R_T = 47k R_T = 18k	● ● ●	270 1.93 3.75	300 2 4	330 2.07 4.25	kHz MHz MHz
PGFB Upper Threshold	V_{PGFB} Rising	●	529	537.5	546	mV
PGFB Upper Threshold Hysteresis				5		mV
PGFB Lower Threshold	V_{PGFB} Falling	●	455	462.5	470	mV
PGFB Lower Threshold Hysteresis				5		mV
PGFB Pin Current	SV_{IN} = 6V, $V_{EN/UVLO}$ = 3V, V_{PGFB} = 0.5V			25		nA
PG Leakage	V_{PG} = 3.3V		–40		40	nA
PG Pull-Down Resistance	V_{PG} = 0.5V	●		380	1200	Ω
SYNC Threshold	SYNC DC and Clock Low Level Voltage SYNC DC and Clock High Level Voltage		0.7		 1.5	V V
OUTS Pin Output Current	V_{OUTS} = 1V		80	160	240	nA
Output Voltage Line Regulation (Note 10)	V_{SVIN} = 4V to 18V			0.001	0.01	%/V
Error Amp Offset (Notes 9, 10)	V_C = 1.2V, V_{SET} = 3V, SV_{IN} = 6V, PNP-Based Input Pair V_C = 1.2V, V_{SET} = 5V, SV_{IN} = 5.5V, NPN-Based Input Pair	● ●	–2 –2		2 2	mV mV
Error Amp Transconductance (Note 9)	V_C = 1.2V, V_{SET} = 1V, SV_{IN} = 6V, PNP-Based Input Pair V_C = 1.2V, V_{SET} = 5V, SV_{IN} = 5.5V, NPN-Based Input Pair		9.5 7.8	11.5 10	13.5 12.2	mS mS
Error Amp Gain	V_C = 1.2V, V_{SET} = 1V, SV_{IN} = 6V			2800		V/V
V_C Source Current (Note 9)	V_C = 1.2V, V_{SET} = 1V, V_{OUTS} = 0V, SV_{IN} = 6V, PNP-Based Input Pair V_C = 1.2V, V_{SET} = 5V, V_{OUTS} = 4.7V, SV_{IN} = 5.5V, NPN-Based Input Pair			330 330		µA µA
V_C Sink Current (Note 9)	V_C = 1.2V, V_{SET} = 1V, V_{OUTS} = 2V, SV_{IN} = 6V, PNP-Based Input Pair V_C = 1.2V, V_{SET} = 5V, V_{OUTS} = 5.3V, SV_{IN} = 5.5V, NPN-Based Input Pair			330 330		µA µA
V_C Pin to Switch Current Gain				11.5		A/V
V_C Clamp Voltage				2.2		V
SV_{IN} Current Consumption	R_T = 47k, f_{SW} =2MHz, SV_{IN} = 6V			11		mA
Minimum On-Time	I_{LOAD} = 2A	●		15	20	ns
Minimum Off-Time	I_{LOAD} = 2A			70	90	ns
Top Power N-Channel MOSFET Current Limit		●	13.5	16	17.5	A
Bottom Power N-Channel MOSFET Current Limit			9.25	11.5	13.75	A
SW Leakage Current	PV_{IN} = 18V, V_{SW} = 0V, 18V		–15		15	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power MOSFET On-Resistance Main Switch (Top) Synchronous Switch (Bottom)				 35 15		 mΩ mΩ
EN/UVLO Threshold	EN/UVLO Rising	●	1.27	1.32	1.37	V
EN/UVLO Hysteresis				50		mV
EN/UVLO Input Current	$V_{EN/UVLO}$ = 2V		–40		40	nA
EN Delay Time (Note 5, 12)	SV_{IN} = 12V, C_{VCC} = 0.1µF (internal) +1µF (external), R_C = 500Ω, C_C = 10nF, C_{SET} = 2.2µF			135		µs
PHMODE Thresholds	Between 180 and 120 Between 120 and 90		0.7 2.0		1.5 2.7	V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8625SPJ/LT8625SPJV-1 are guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: θ values determined per JEDEC 51-7, 51-12. See the Applications Information for information on improving the thermal resistance and for actual temperature measurements of a demo board in typical operating conditions.

Note 4: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

Note 5: Not subject to production test.

Note 6: OUTS ties directly to V_{OUT}.

Note 7: Adding a capacitor across the SET pin resistor decreases output voltage noise. Adding this capacitor bypasses the SET pin resistor's thermal noise as well as the reference current's noise. Use of a SET pin bypass capacitor also increases start-up time.

Note 8: Minimum SV_{IN} can increase with OUTS once OUTS is above a certain value. Refer to the Typical Characteristics curves for how this parameter changes with OUTS.

Note 9: The PNP-based input pair is active for the error amplifier as long as SV_{IN} is at least 1V above V_{SET}. As SV_{IN} drops to less than 1V above V_{SET}, the part gradually transitions to operating with the NPN-based input pair active.

Note 10: The LT8625SP/LT8625SP-1 is tested in a feedback loop that servos V_C to a specified voltage and measures the resultant V_{OUTS}.

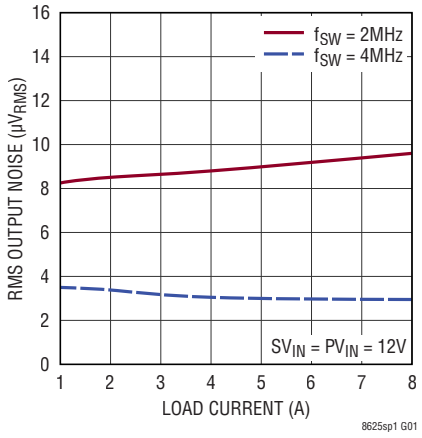
Note 11: The start-up time is defined as the time it takes from the EN/UVLO pin rising above the EN/UVLO threshold to when V_{OUT} has reached 90% of final value.

Note 12: EN Delay Time is the time from EN/UVLO high to first switching cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

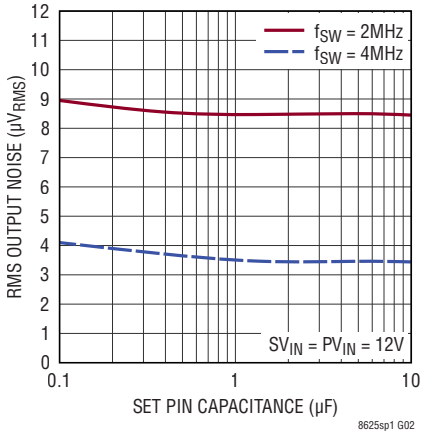
T_A = 25°C, unless otherwise noted.

Integrated RMS Output Noise vs Load (10Hz to 100kHz)



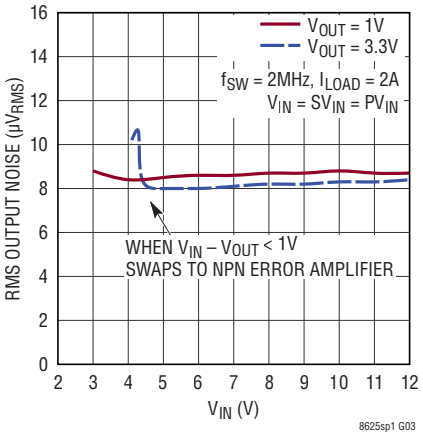
REFER TO TYPICAL APPLICATION CIRCUITS TA03 (2MHz) AND TA02 (4MHz)

Integrated RMS Output Noise vs C_{SET} (10Hz to 100kHz)



REFER TO TYPICAL APPLICATION CIRCUITS TA03 (2MHz) AND TA02 (4MHz)

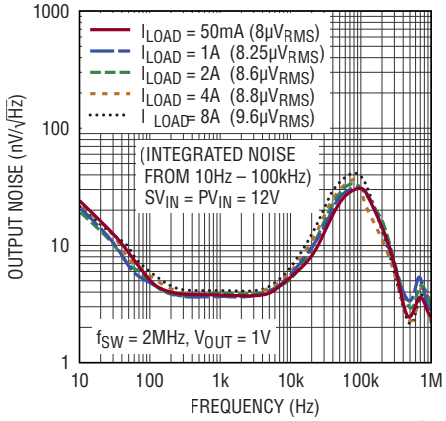
Integrated RMS Output Noise vs V_{IN} (10Hz to 100kHz)



REFER TO TYPICAL APPLICATION CIRCUITS TA03 (1V) AND TA07 (3.3V)

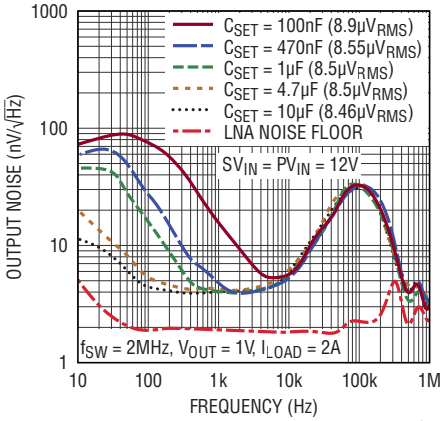
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Noise Spectral Density vs Load



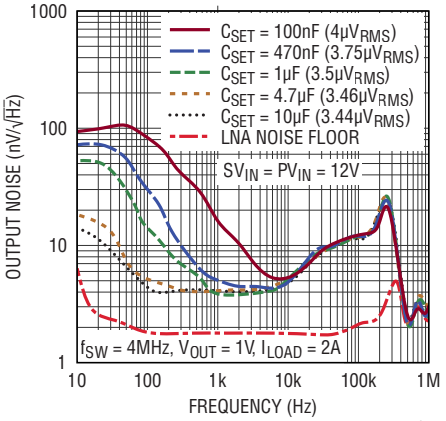
TYPICAL APPLICATION CIRCUIT TA03 (2MHz)

Noise Spectral Density vs C_{SET}



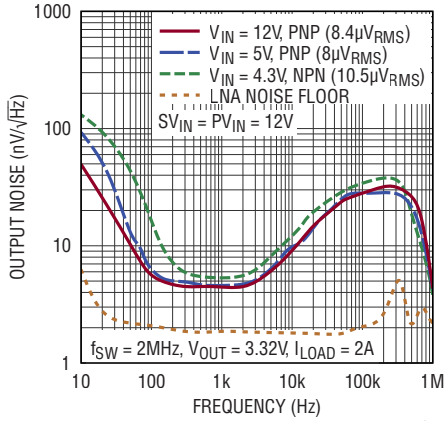
(INTEGRATED NOISE FROM 10Hz TO 100kHz)
TYPICAL APPLICATION CIRCUIT TA03 (2MHz)

Noise Spectral Density vs C_{SET}



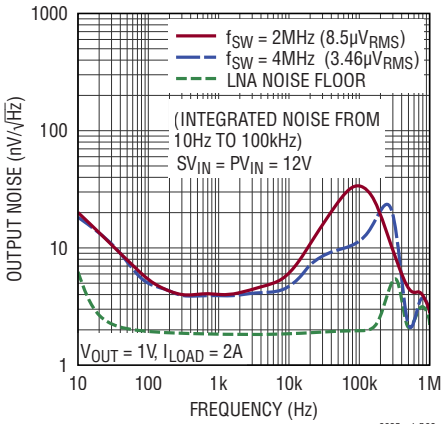
(INTEGRATED NOISE FROM 10Hz TO 100kHz)
TYPICAL APPLICATION CIRCUIT TA02 (4MHz)

Noise Spectral Density as a Function of Error Amplifier Input Pair



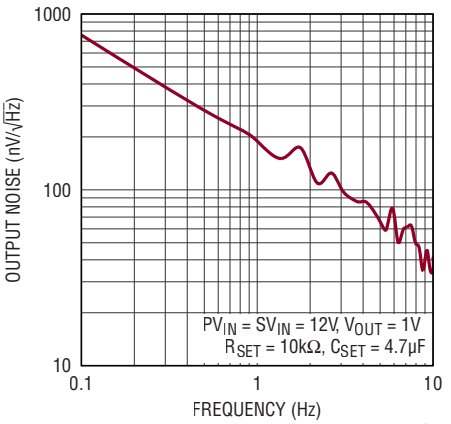
(INTEGRATED NOISE FROM 10Hz TO 100kHz)
TYPICAL APPLICATION CIRCUIT TA07 (3.3V)

Noise Spectral Density vs f_{SW}

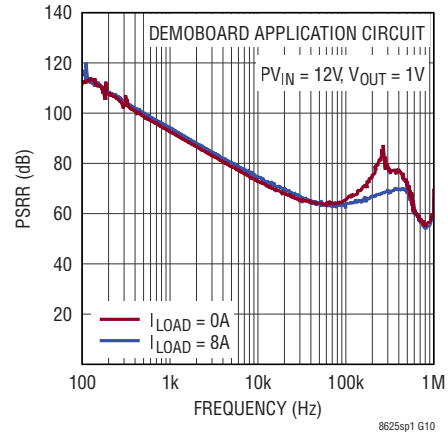


REFER TO TYPICAL APPLICATION CIRCUITS TA03 (2MHz) AND TA02 (4MHz)

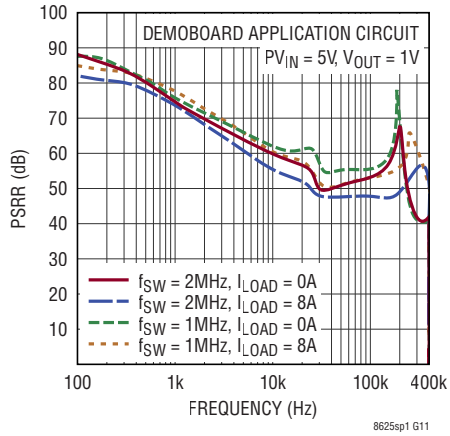
Noise Spectral Density (0.1Hz to 10Hz)



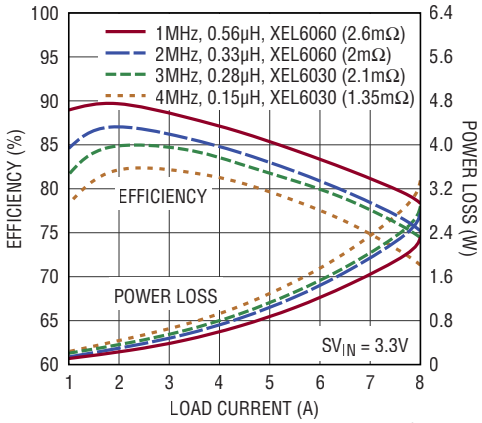
Power Supply Ripple Rejection



Power Supply Ripple Rejection

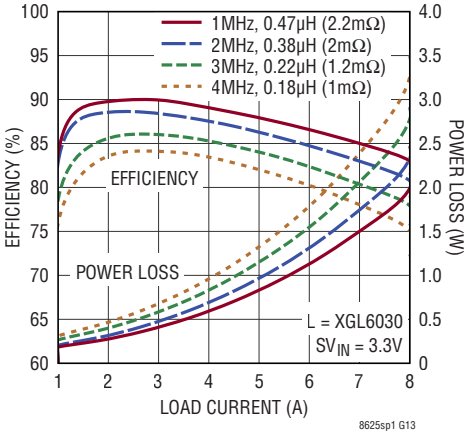


$12V_{IN}$ to $1V_{OUT}$ Efficiency

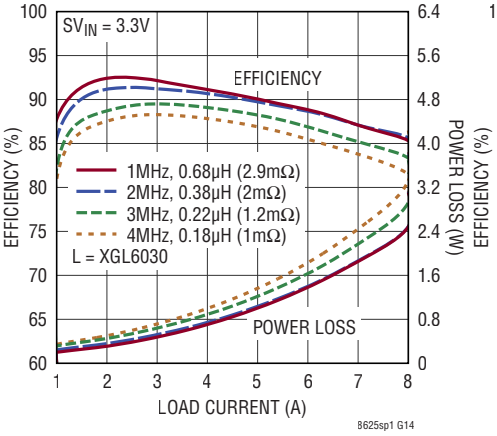


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

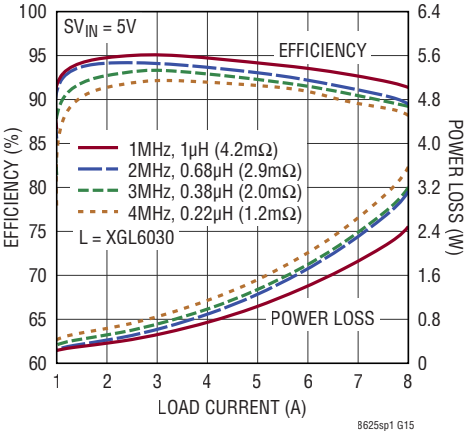
$12V_{IN}$ to $1.2V_{OUT}$ Efficiency



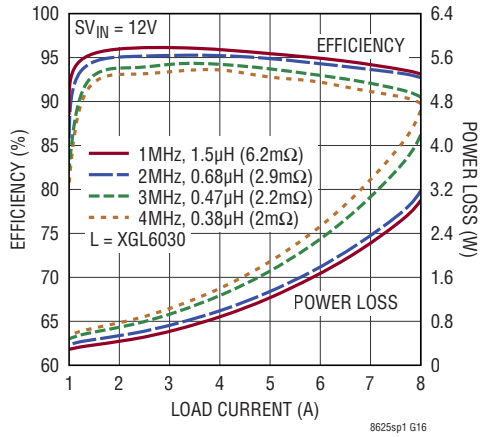
$12V_{IN}$ to $1.8V_{OUT}$ Efficiency



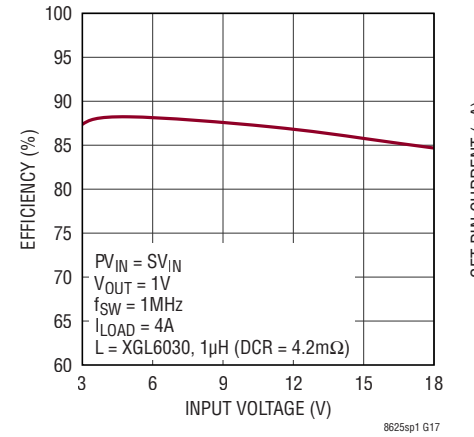
$12V_{IN}$ to $3.3V_{OUT}$ Efficiency



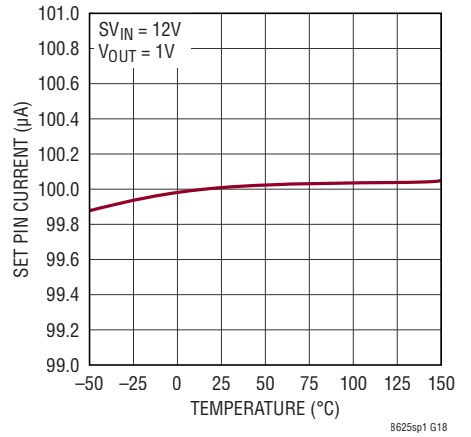
$12V_{IN}$ to $5V_{OUT}$ Efficiency



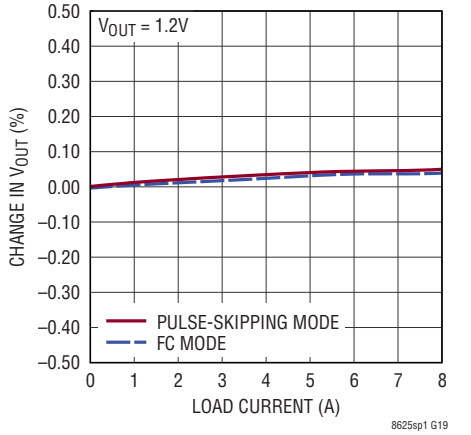
Efficiency vs V_{IN}



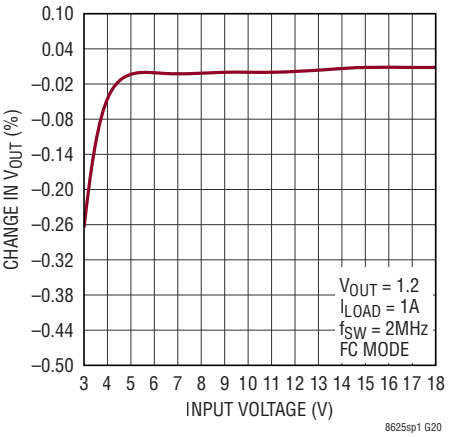
SET Pin Current



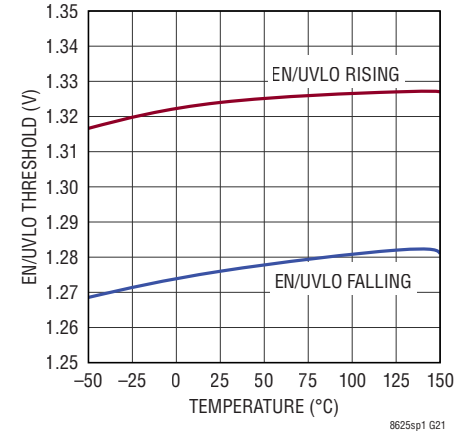
Load Regulation



Line Regulation

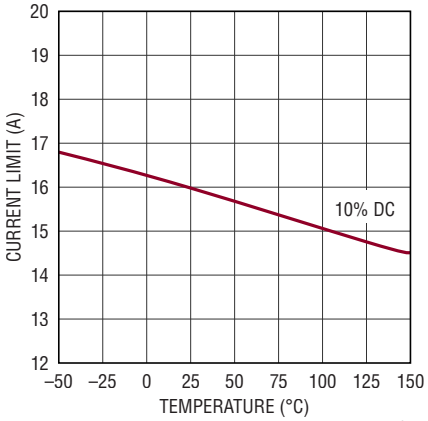


EN/UVLO Pin Thresholds

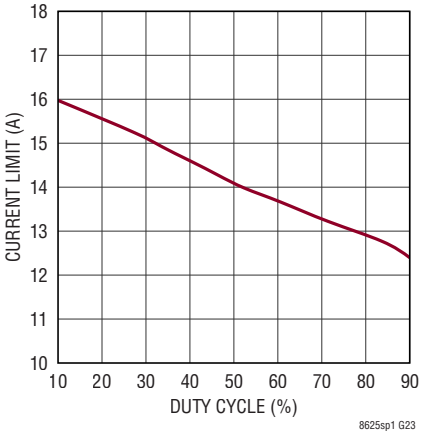


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

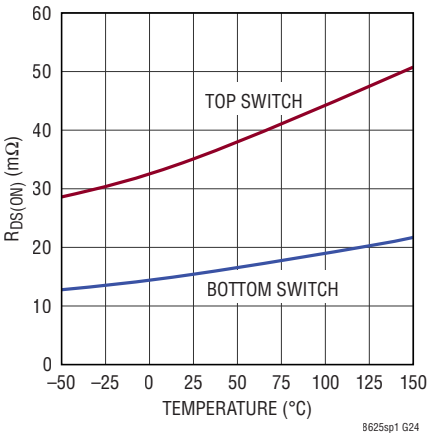
Top MOSFET Current Limit



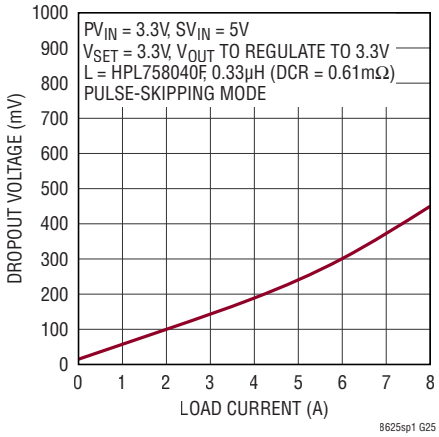
Top MOSFET Current Limit vs Duty Cycle



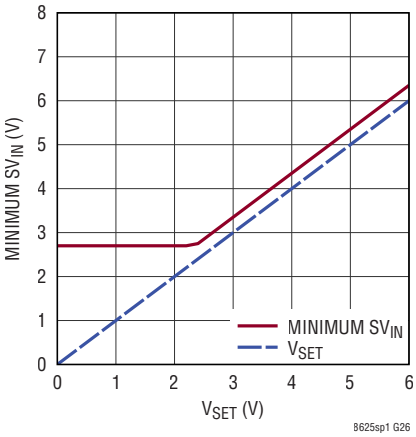
Switch $R_{DS(ON)}$ vs Temperature



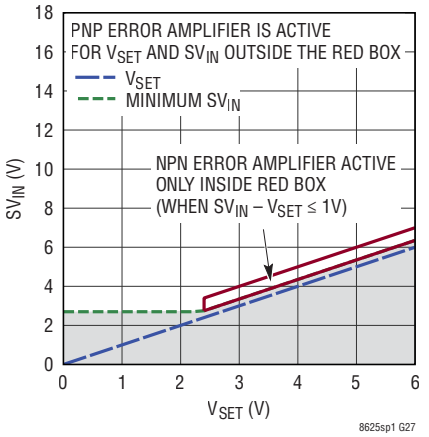
PV_{IN} Dropout Voltage



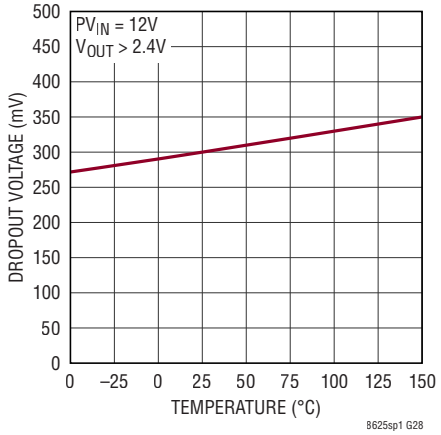
Minimum SV_{IN} as a Function of V_{SET}



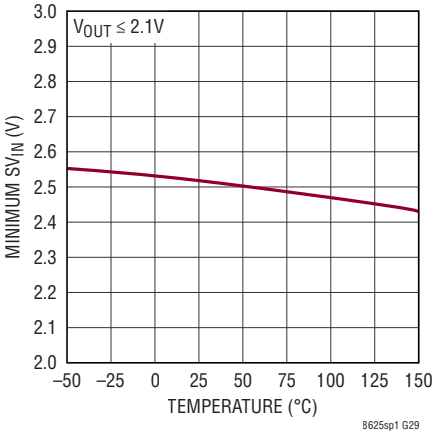
Minimum SV_{IN} as a Function of V_{SET}



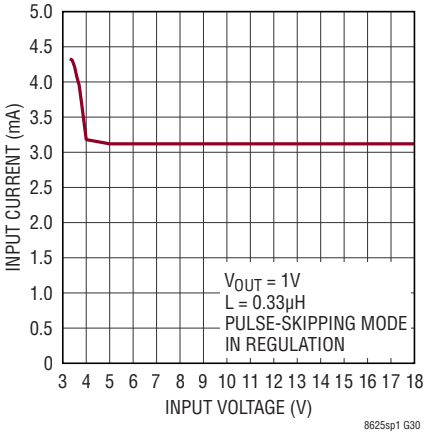
SV_{IN} Dropout Voltage



Minimum SV_{IN}

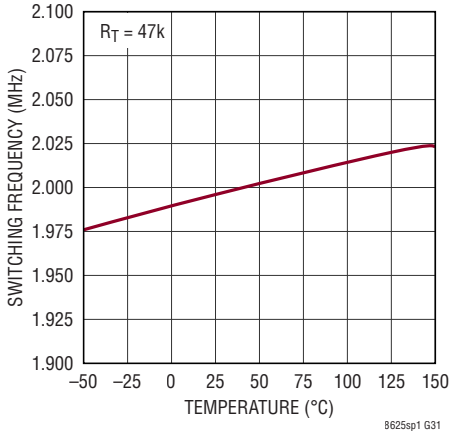


No-Load Supply Current

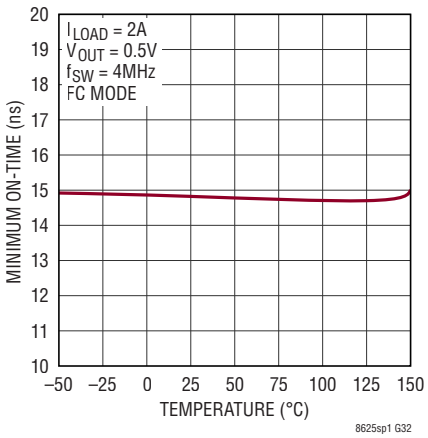


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

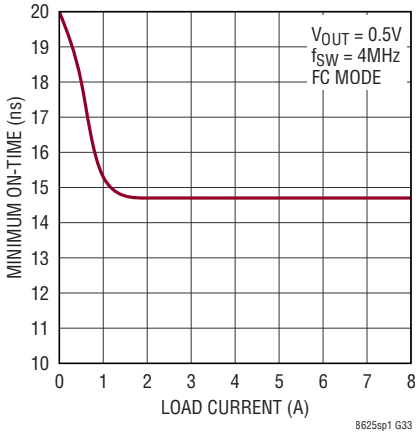
Switching Frequency



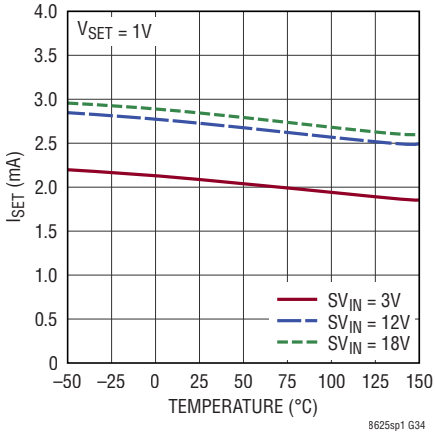
Minimum On-Time vs Temperature



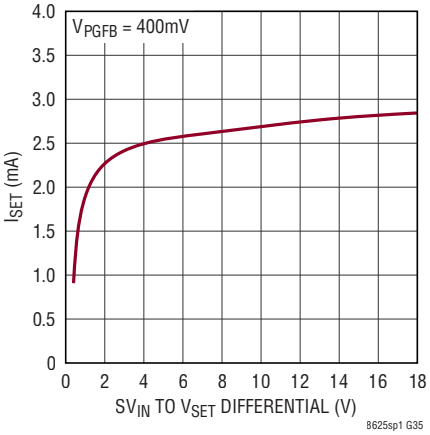
Minimum On-Time vs Load



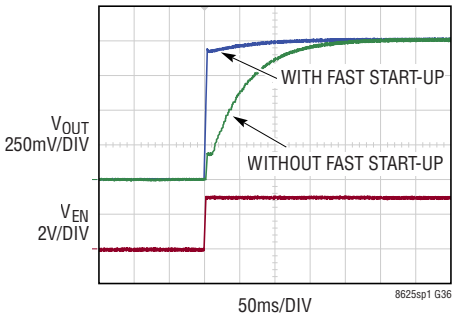
I_{SET} During Start-Up with Fast Start-Up Enabled



I_{SET} During Start-Up with Fast Start-Up Enabled

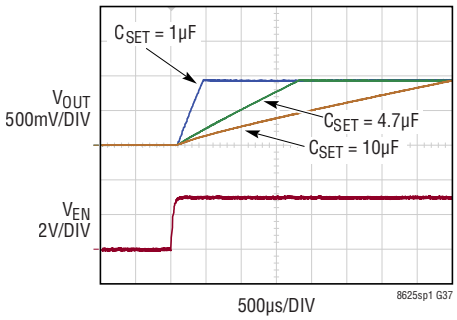


Start-Up Time with and without Fast Start-Up Circuitry for Large C_{SET}



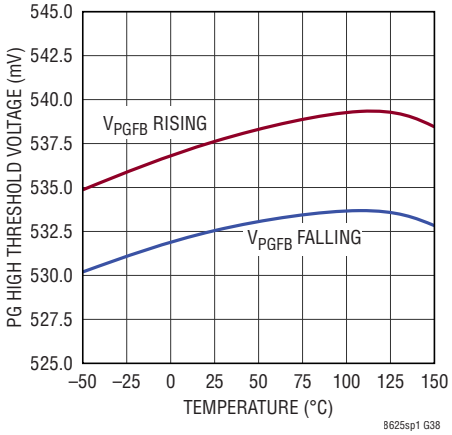
SV_{IN} = 5V
R_{SET} = 10kΩ, C_{SET} = 4.7µF
F_{SW} = 2MHz, L = 330nH, C_{OUT} = 5× 22µF
R_L = 1Ω

Soft-Start Waveforms

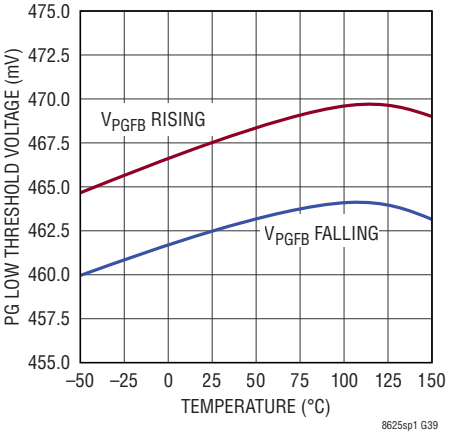


SV_{IN} = 5V
R_{SET} = 10kΩ, WITH FAST START-UP
F_{SW} = 2MHz, L = 330nH, C_{OUT} = 5× 22µF
R_L = 1Ω

PG High Thresholds

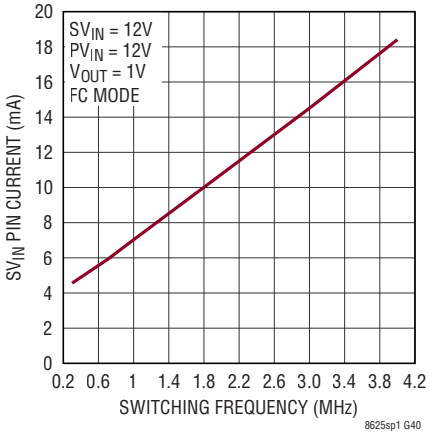


PG Low Thresholds

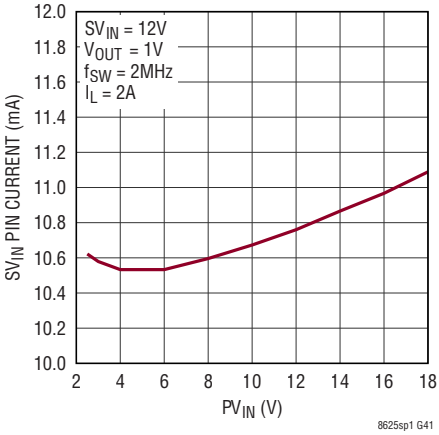


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

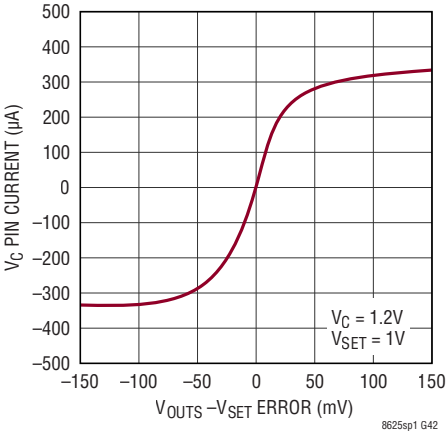
SV_{IN} Pin Current vs Frequency



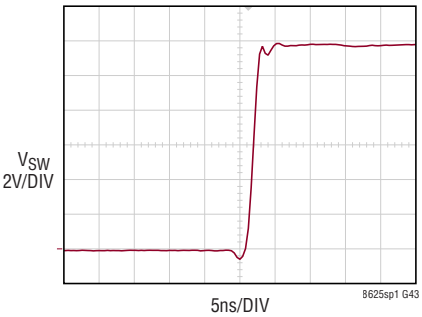
SV_{IN} Pin Current vs PV_{IN}



Error Amp Output Current

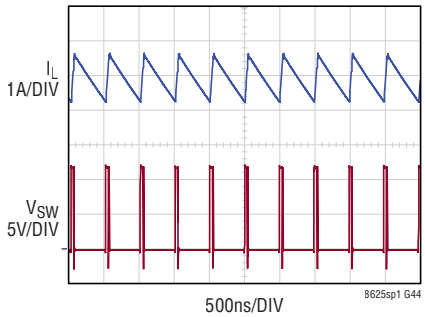


Switch Rising Edge



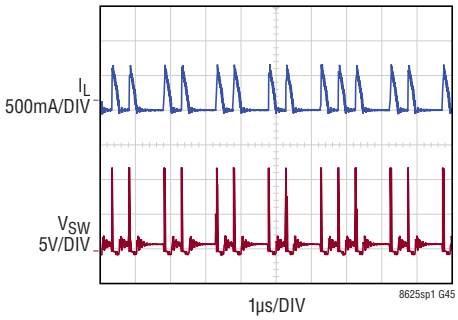
V_{IN} = 12V
I_{LOAD} = 6A

Switching Waveforms, Full Frequency Continuous Operation



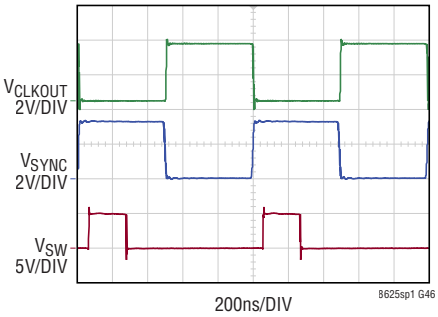
$12V_{IN}$ TO $1V_{OUT}$ AT 5A
f_{SW} = 2MHz

Switching Waveforms, Pulse-Skipping Operation



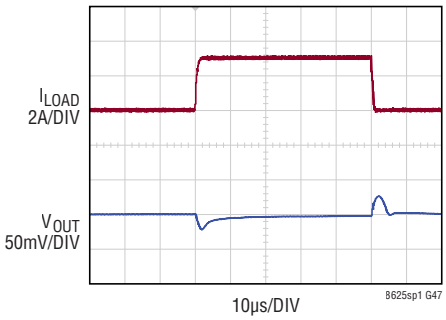
$12V_{IN}$ TO $1V_{OUT}$ AT 100mA
V_{SYNC} = 0V

CLKOUT Waveforms



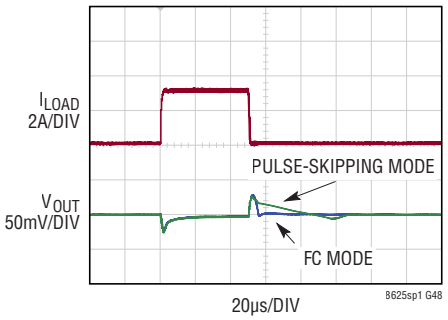
f_{SW} = 1MHz, PV_{IN} = 5V, V_{OUT} = 1V, I_{LOAD} = 3A
SYNCRHONIZATION MODE
V_{PHMODE} = 0V

Transient Response: Load Current Stepped from 2A to 5A



PV_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 2MHz
C_C = 2.2nF, R_C = 1k
C_{OUT} = 2× 100µF + 2× 22µF

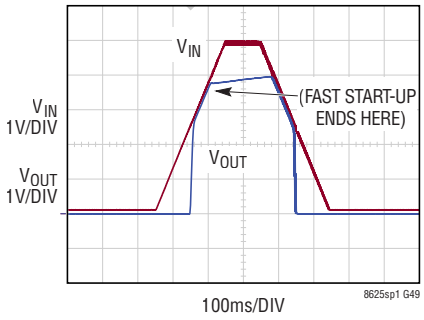
Transient Response: Load Current Stepped from 100mA to 3.1A



PV_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 2MHz
C_C = 2.2nF, R_C = 1k
C_{OUT} = 2× 100µF + 2× 22µF

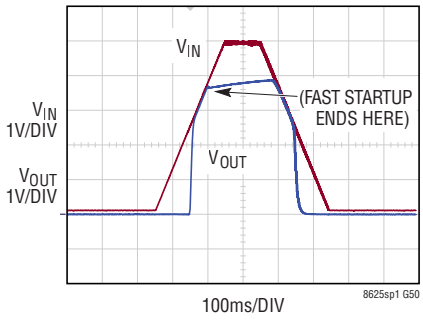
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Start-Up Dropout Performance



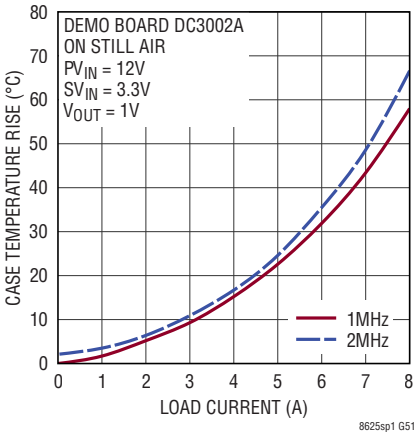
1Ω LOAD
(4A IN REGULATION)

Start-Up Dropout Performance

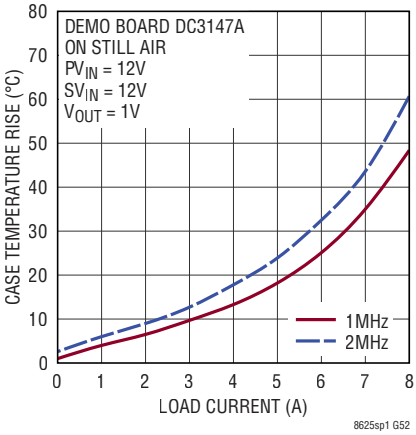


20Ω LOAD
(200mA IN REGULATION)

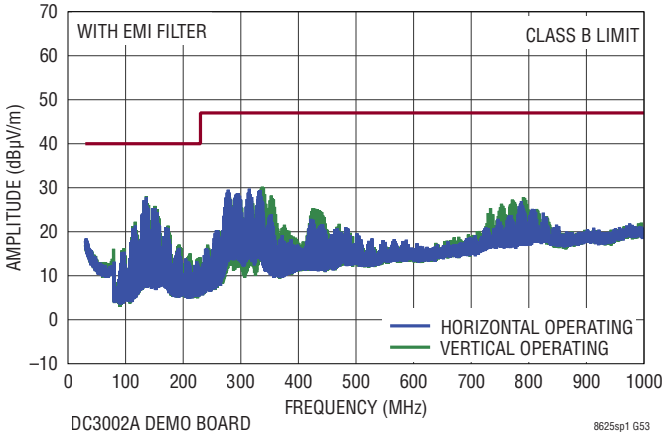
LT8625SP Case Temperature Rise (4mm × 3mm LQFN)



LT8625SP-1 Case Temperature Rise (4mm × 4mm LQFN)



Radiated EMI Performance (CISPR32 Radiated Emission Test with Class B Limits)



DC3002A DEMO BOARD
12V INPUT TO 1V OUTPUT AT 1A, f_{SW} = 2MHz

PIN FUNCTIONS (20 LQFN/24 LQFN)

SW (Pins 1, 20/Pins 1–2, 22–24): The SW Pins are the outputs of the internal power switches. Tie these pins together and connect them to the inductor. This node should be kept small on the PCB for good performance and low EMI.

NC (Pin 2): No Connect. This pin is not connected to internal circuitry and can be tied anywhere on the PCB, typically ground.

GND (Pins 3, 4, 21/Pins 3, 4, 25–28): Ground. Place the negative terminal of the input capacitor as close to the GND pins as possible. The exposed pads should be soldered to the PCB for good thermal performance. If necessary due to manufacturing limitations, the exposed pads may be left disconnected, however, thermal performance will be degraded.

PV_{IN} (Pins 5–6/Pins 5–8): Power V_{IN}. The PV_{IN} pins supply current to the LT8625SP/LT8625SP-1 internal circuitry and to the internal topside power switch. These pins must be tied together and be locally bypassed with a capacitor of 4.7µF or more. Be sure to place the positive terminal of the input capacitor as close as possible to the PV_{IN} pins, and the negative capacitor terminal as close as possible to the GND pins.

SV_{IN} (Pin 7/Pin 9): Signal V_{IN}. This pin supplies current to the LT8625SP/LT8625SP-1 internal circuitry and regulator. In order to provide sufficient headroom for the current reference, SV_{IN} must be at least 400mV higher than the desired setpoint that is programmed via the SET pin. For example, for a desired setpoint of 3.3V, SV_{IN} must be at least 3.3V + 400mV = 3.7V, or higher. See Typical Performance Characteristics for curves. If tied to a different supply than PV_{IN}, place a 1µF local bypass capacitor on this pin.

EN/UVLO (Pin 8/Pin 10): A voltage at this pin greater than 1.32V will enable switching, and a voltage less than 400mV is guaranteed to shut down the internal current bias and sub-regulators. The hysteretic threshold voltage is 1.32V going up and 1.28V going down. Tie to PV_{IN} if the shutdown feature is not used. An external resistor divider from PV_{IN} can be used to program a PV_{IN} threshold below which the LT8625SP/LT8625SP-1 will shut down.

$INTV_{CC}$ (Pin 9/Pin 11): Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. Do not load the $INTV_{CC}$ pin with external circuitry. $INTV_{CC}$ current will be supplied by SV_{IN}. Decouple this pin to ground with at least a 1µF low ESR ceramic capacitor.

PHMODE (Pin 10/Pin 12): The PHMODE pin sets the phase shift of the clock signal of the CLKOUT pin. Tie PHMODE to ground for 180° phase shift, float for 120° phase shift and tie high to $INTV_{CC}$ (~3.4V) or an external supply >3V for a 90° phase shift. See Block Diagram for internal pull-up and pull-down resistance.

SET (Pin 11/Pin 13): This pin is the noninverting input of the error amplifier and the regulation setpoint for the LT8625SP/LT8625SP-1. SET sources a precision 100µA current that flows through an external resistor connected between SET and GND. The LT8625SP/SP-1's output voltage is determined by $V_{SET} = I_{SET} \bullet R_{SET}$ when used in the default unity gain configuration. SET pin voltage range is from zero to 6V. Increasing the capacitor from SET to GND improves noise at the expense of increased start-up time. For optimum load regulation, Kelvin connect the ground side of the SET pin resistor directly to the load. This pin is pulled to ground with a 500Ω MOSFET during shutdown and fault conditions.

V_C (Pin 12/Pin 14): The V_C pin is the output of the internal error amplifier. The voltage on this pin controls the peak switch current. Tie an RC network from this pin to ground to compensate the control loop.

OUTS (Pin 13/Pin 15): Output Sense. This pin is the inverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connect OUTS directly to the output capacitor and the load. Also, tie the GND connections of the output capacitor and the SET pin capacitor directly together.

PGFB (Pin 14/Pin 16): Power Good Feedback. The PG pin pulls low if PGFB increases above 537.5mV or decreases below 462.5mV. Connecting an external resistor divider between V_{OUT}, PGFB and GND sets the programmable power good threshold with the following transfer function: $0.5V\ (\pm 7.5\%) \bullet (1 + R_{PGFB(TOP)}/R_{PGFB(BOT)})$. As discussed in the Applications Information section, PGFB also activates the fast start-up circuitry. PGFB must be tied to

PIN FUNCTIONS (20 LQFN/24 LQFN)

0.5V if power good and fast start-up functionalities are not needed.

RT (Pin 15/Pin 17): A resistor is tied between RT and ground to set the switching frequency.

PG (Pin 16/Pin 18): The PG pin is the open-drain output of an internal comparator. PG remains low until the PGFB pin is within ±7.5% of 0.5V, and there are no fault conditions. PG is also pulled low when EN/UVLO is below 1.32V, $INTV_{CC}$ has fallen too low, SV_{IN} is too low, or during thermal shutdown. PG is valid when SV_{IN} is above 2.7V.

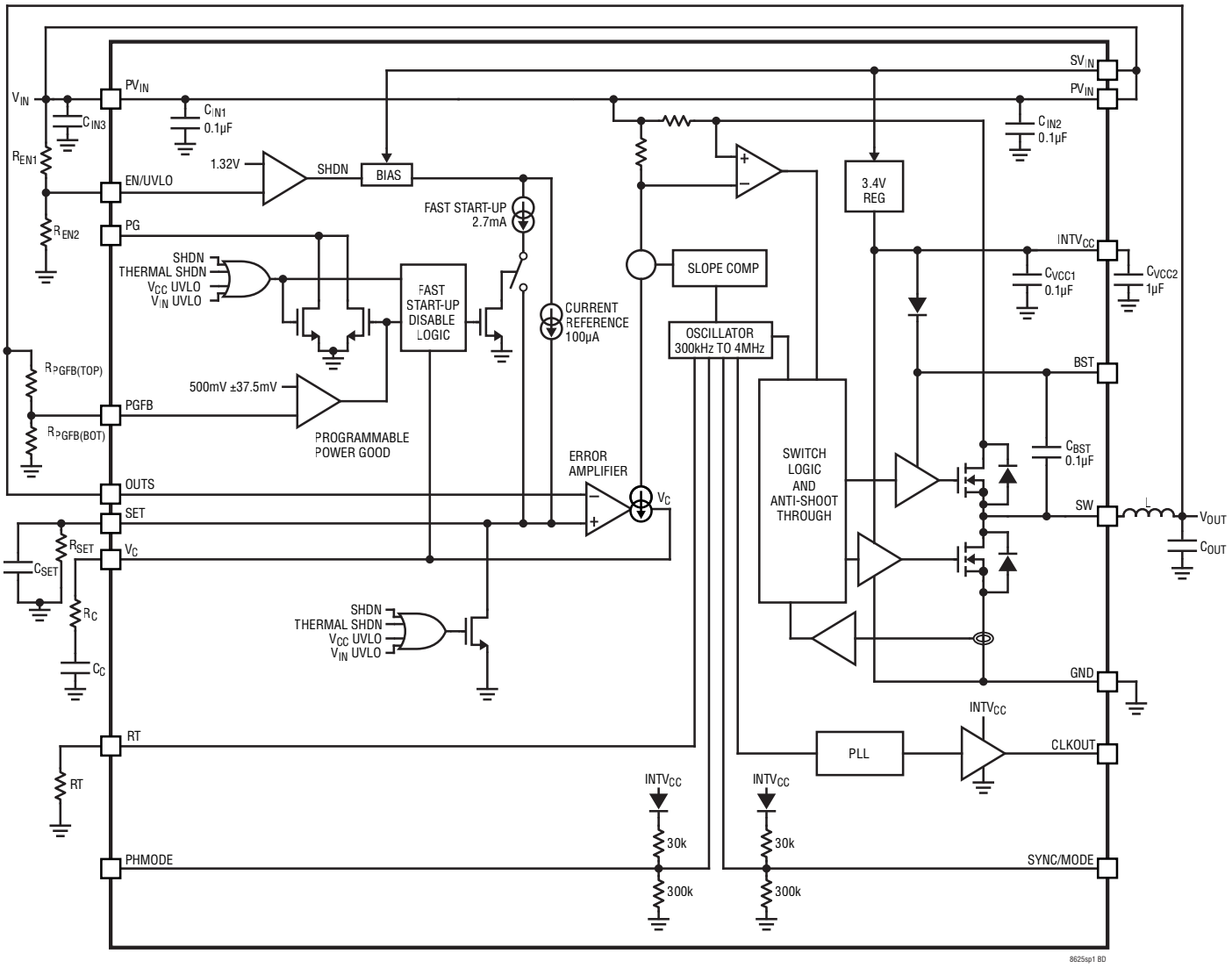
SYNC/MODE (Pin 17/Pin 19): For the LT8625SP/LT8625SP-1, this pin programs three different operating modes: 1) Pulse-skipping mode. Tie this pin to GND for pulse-skipping mode for improved efficiency at light loads. 2) Forced Continuous mode (FCM). This mode offers fast transient response and full frequency operation over a wide load range. Tie this pin high to $INTV_{CC}$ (~3.4V) or an external supply >1.5V for FCM. The part will also operate in this mode by default if this pin is left floating. 3) Synchronization mode. Drive this pin with a clock source to synchronize to an external frequency. During synchronization the part will operate in forced continuous mode.

CLKOUT (Pin 18/Pin 20): Output Clock Signal for PolyPhase Operation. The CLKOUT pin provides a 50% duty-cycle square wave of the switching frequency. The phase of CLKOUT with respect to the LT8625SP/LT8625SP-1's internal clock is determined by the state of the PHMODE pin. CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND. Float this pin if the CLKOUT function is not used.

BST (Pin 19/Pin 21): This pin is used to provide a drive voltage, higher than the input voltage, to the topside power switch. This pin should be floated.

Corner Pins (Pins 22-25/Pins 29-32): These pins are for mechanical support only and can be tied anywhere on the PCB. It is convenient to tie pin 22/pin 29 to SW and pin 23/pin 30 to PV_{IN}.

BLOCK DIAGRAM



OPERATION

The LT8625SP/LT8625SP-1 is a constant frequency, current mode, monolithic step-down regulator, operating using a current reference-based architecture to allow the employment of unity gain in order to minimize output noise across all output voltages. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the V_C pin. The error amplifier servos the V_C node by comparing the voltage on the OUTS pin to the reference voltage on the SET pin, which is set by the user with a resistor from the SET pin to ground. When the load current increases it causes a reduction in the OUTS voltage relative to the reference leading the error amplifier to raise the V_C voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or inductor current falls to zero (only in pulse-skipping mode). If overload conditions result in more than 11A flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

The “S” in LT8625SP/LT8625SP-1 refers to the second-generation Silent Switcher technology. This technology allows fast switching edges for high efficiency at high switching frequencies, while simultaneously achieving good EMI performance. This includes the integration of ceramic capacitors into the package for V_{IN}, $INTV_{CC}$, and boost (see Block Diagram). These capacitors keep all the fast AC current loops small, which improves EMI performance.

The “P” in LT8625SP/LT8625SP-1 refers to the fact that the package features exposed die for optional heat sink attach. This means heat sinks can be used to significantly improve thermal performance.

The LT8625SP/LT8625SP-1 features third-generation Silent Switcher technology, which combines an ultralow noise current reference with second generation Silent Switcher technology. The output voltage can be programmed with a single resistor, providing unity-gain operation over the output range, resulting in virtually constant ultralow output noise independent of output voltage.

If the EN/UVLO pin is below 0.4V, the LT8625SP/LT8625SP-1 is shut down and draws 50µA from the input. When the EN/UVLO pin rises above 1.32V, the switching regulator will become active.

To improve efficiency at light loads, the LT8625SP/LT8625SP-1 can operate in pulse-skipping mode in light load situations. The SYNC pin is tied low to use pulse-skipping operation and tied to $INTV_{CC}$ or to a voltage higher than 3V or floated, to use forced continuous mode (FCM). If a clock is applied to the SYNC pin, the part will synchronize to an external clock frequency and operate in FCM.

The LT8625SP/LT8625SP-1 can operate in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. When in FCM the oscillator operates continuously, and positive SW transitions are aligned to the clock. Negative inductor current is allowed. The LT8625SP/LT8625SP-1 can sink current from the output and return this charge to the input in this mode, improving load step transient response.

To improve efficiency across all loads, the SV_{IN} pin can be powered from an independent supply at a voltage lower than PV_{IN}.

The V_C pin allows the loop compensation of the switching regulator to be optimized based on the programmed switching frequency, allowing for a fast-transient response. The V_C and CLKOUT pins enable multiple LT8625SP/LT8625SP-1 regulators to run out-of-phase, reducing the amount of required input and output capacitors. The PHMODE pin selects the phasing of CLKOUT for different multiphase applications.

APPLICATIONS INFORMATION

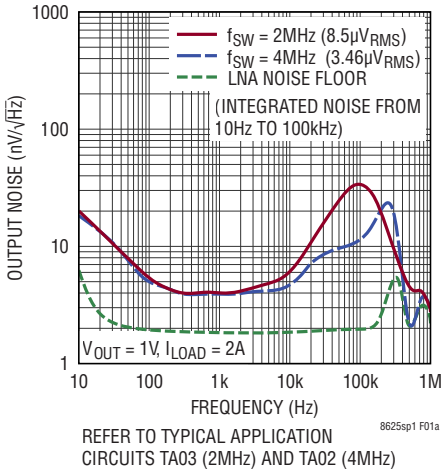
Low Frequency Output Noise

The LT8625SP/LT8625SP-1 offers many advantages with respect to noise performance in the low frequency range (<100kHz). Conventional step-down regulators have several sources of low frequency noise. The most critical noise sources for a conventional regulator are its reference, error amplifier, noise from the resistor divider network used for setting output voltage and the noise gain created by this resistor divider.

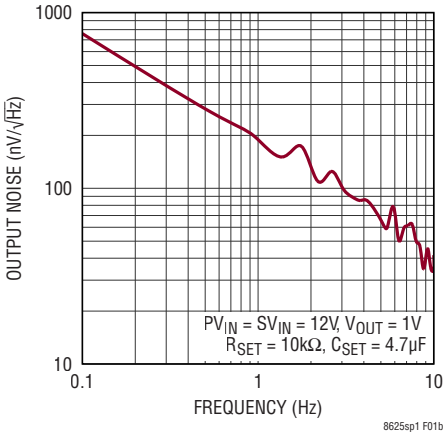
Unlike most step-down regulators, the LT8625SP/LT8625SP-1 does not use a voltage reference; instead, it uses a 100µA current reference. One problem that conventional step-down regulators face is that the resistor divider setting the output voltage gains up the reference noise. In contrast, the current reference architecture employed by the LT8625SP/LT8625SP-1 allows unity-gain operation to avoid gaining up noise from the reference to the output. Therefore, if a capacitor bypasses the SET pin resistor, then the output noise is independent of the programmed output voltage. The resultant output noise is typically 4nV/√Hz at 10kHz.

With the previously mentioned noise sources operating at such low noise levels, other noise sources become non-negligible contributors to the output noise. Choosing a compensation network that achieves good transient performance with a good phase margin will ensure optimal noise performance. The Applications Information section on Frequency Compensation provides guidelines on how to choose appropriate compensation.

See Figure 1 for noise spectral density from 10Hz to 100kHz and 0.1Hz to 10Hz. Refer to the Typical Performance Characteristics section for RMS integrated noise over various load currents and SET pin capacitances, as well as how the noise spectral density can vary over switching frequency, where each application is compensated for good transient response and phase margin.



(a)



(b)

Figure 1. Noise Spectral Density

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Filtering Switching Ripple and High Frequency Noise

The LT8625SP/LT8625SP-1 is a switching regulator and will also have the typical artifacts of a switching regulator at the output, namely a ripple at the fundamental switching frequency as well as high frequency spikes associated with the fast switching edges. While the output capacitor will absorb some of these spikes, the capacitor ESL will limit its ability to do so at high frequencies. Additional filtering at the output in the form of feedthrough capacitors, ferrite beads, or an additional LC filter stage are recommended to eliminate these high frequency spikes and significantly reduce switching ripple.

Feedthrough capacitors are recommended if additional switching ripple reduction is required while retaining fast transient response. Ensure sufficient feedthrough capacitors are paralleled to carry the required load current. Figure 2 shows an example where two 3A rated feedthrough capacitors are used for additional switching ripple suppression to deliver up to 6A at the output.

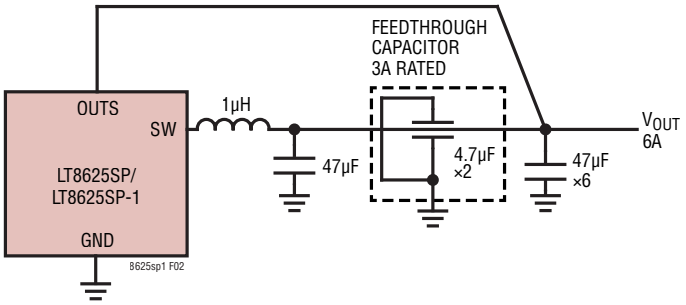

Figure 2. Additional Output Ripple Filtering Using Feedthrough Capacitors

If transient performance is not critical, other passive filter solutions can be realized using a ferrite bead, PCB trace, or physical inductor as a second L, and additional output capacitance for the second C, as shown in Figure 3.

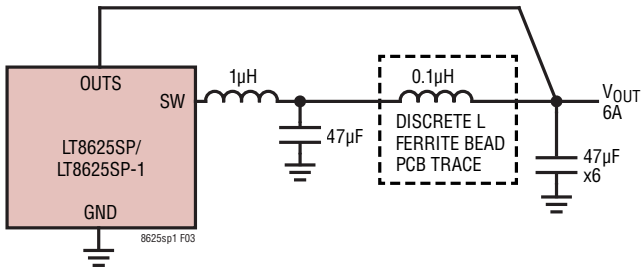

Figure 3. Additional Output Ripple Filtering Using a Second LC Filter

When designing an additional filter for further attenuation of the switching ripple, it is highly recommended to design with LTpowerCAD® to ensure the design is stable with good phase margin and provides sufficient attenuation at the switching frequency of interest.

The Silent Switcher 3 architecture makes it possible to achieve excellent noise performance from low to high frequencies at the output of the LT8625SP/LT8625SP-1 while utilizing only passive filtering.

PCB Layout Recommendations

The LT8625SP/LT8625SP-1 is specifically designed to minimize low frequency (10Hz-100kHz) noise, EMI emissions and maximize efficiency when switching at high frequencies. For optimal performance the LT8625SP/LT8625SP-1 can use multiple PV_{IN} bypass capacitors.

Two small capacitors can be placed as close as possible to the LT8625SP/LT8625SP-1 PV_{IN} pins, and a third capacitor with a larger value, 4.7µF or higher, should be placed near one of these two capacitors. See Figure 4 for a recommended PCB layout.

For more detail and PCB design files refer to the Demo Board guide for the LT8625SP/LT8625SP-1. Note that large, switched currents flow in the LT8625SP/LT8625SP-1 PV_{IN} and GND pins and the input capacitors. The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the PV_{IN} and GND pins. Capacitors with small case size such as 0402 or 0603 are optimal due to lowest parasitic inductance. Special care must be taken with the input capacitors to ensure they have a low impedance return path to the IC ground. This can be achieved by placing several ground vias on the GND side of the input capacitors such that the ground plane is utilized to full advantage. This should be an unbroken ground plane with a solid connection to the exposed pad of the IC, as shown in Figure 4b.

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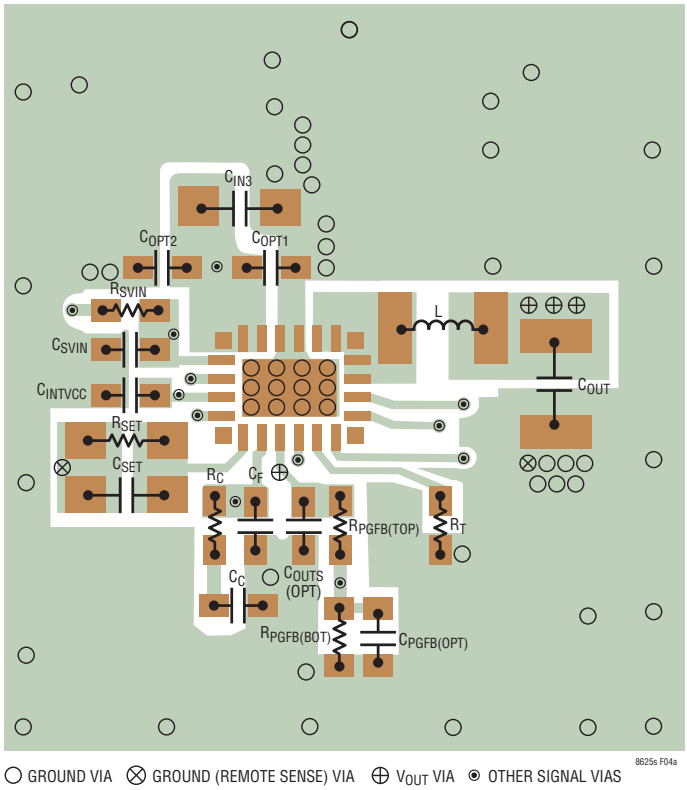
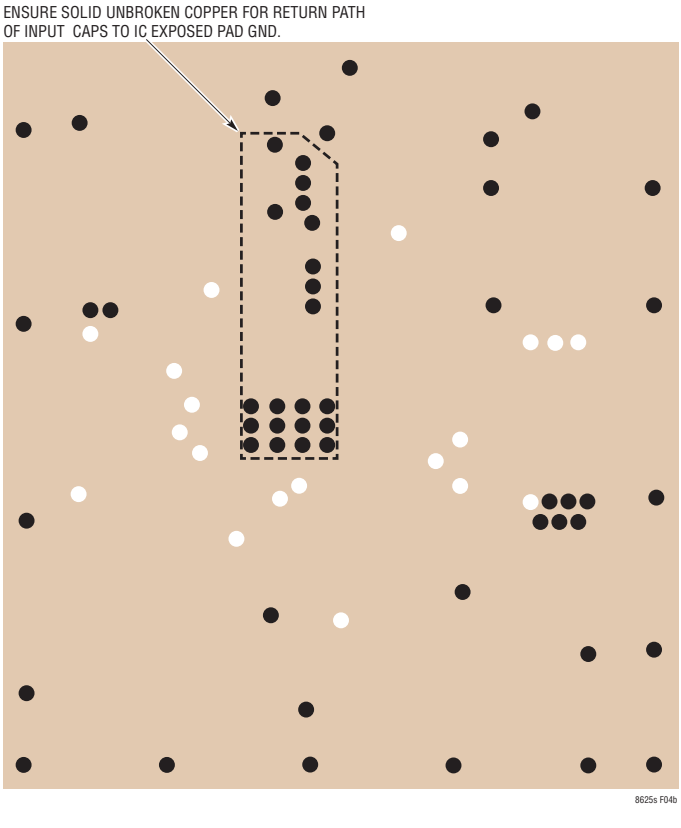


(a) Top Layer



(b) Ground Plane Layer

Figure 4. LT8625SP Suggested Layout (For LT8625SP-1 Suggested Layout Refer to LT8627SP Data Sheet)

The main inductor and output capacitors should be placed on the same side of the circuit board with the IC, and their connections should be made on that layer. The impedance of the output bulk capacitor's return path to IC ground should also be minimized through generous use of ground vias.

Care with ground layout prevents switching currents from the input capacitors coupling to the output through the ground which can introduce unintentional perturbations onto the OUTS pin. A small capacitor may also be placed locally to decouple the OUTS pin if needed.

An additional LC filter, if used, can be placed on the other side of the circuit board for optimal EMI performance, though this is not required.

Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible. Finally, keep the OUTS, PGFB and RT nodes small so that the ground traces will shield them from the SW and BOOST nodes. The OUTS, PGFB and RT traces should not pass underneath the main inductor and should also be kept away from inductor vias.

The exposed pad on the bottom of the package should be soldered to the PCB to reduce thermal resistance to ambient. To keep thermal resistance low, extend the ground plane from GND as much as possible, and add thermal vias to additional ground planes within the circuit board and on the bottom side.

The current reference architecture of the LT8625SP/LT8625SP-1 allows remote sense of the negative terminals of the load in addition to the positive terminal; note

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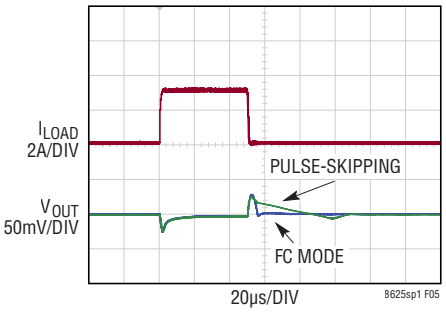
the via on the ground side of the R_{SET} and C_{SET} going to the ground side of C_{OUT} which can be configured for remote sense of the negative terminal of a load placed further away. Refer to the Output Sensing and Stability section for more information on implementing remote sense for LT8625SP/LT8625SP-1.

Forced Continuous Mode

The LT8625SP/LT8625SP-1 can operate in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. When in FCM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. Negative inductor current is allowed at light loads or under large transient conditions. The LT8625SP/LT8625SP-1 can sink current from the output and return this charge to the input in this mode, improving load step transient response (see Figure 5). At light loads, FCM operation is less efficient than pulse-skipping operation, but may be desirable in applications where it is necessary to keep switching harmonics out of the signal band. FCM must be used if the output is required to sink current. To enable FCM, tie the SYNC/MODE pin to $INTV_{CC}$ or > 1.5V, or float the pin.



PV_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 2MHz
C_C = 2.2nF, R_C = 1k
C_{OUT} = 2× 100µF + 2× 22µF

Figure 5. Load Step Transient Response with and without Forced Continuous Mode

FCM is disabled under PV_{IN} overvoltage conditions (PV_{IN} pin is held above 18V), if V_{OUT} is too high (the PGFB pin is held greater than 537.5mV) and is also disabled during start-up until the voltage on V_{OUT} has charged up to 92.5% of its final value (as indicated when the PGFB pin rises to above 462.5mV). For the latter two conditions, it is assumed the PGFB pin is tied to the output voltage through an appropriate resistor divider. When FCM is disabled in these ways, negative inductor current is not allowed and the LT8625SP/LT8625SP-1 operates in pulse-skipping mode.

Pulse-Skipping Mode

When not operating in forced continuous mode, the LT8625SP/LT8625SP-1 will operate in pulse-skipping mode. In this mode the oscillator operates continuously, and all switching cycles are aligned to the clock. Negative inductor current is not allowed in this mode; therefore, at light loads the LT8625SP/LT8625SP-1 may be operating in discontinuous mode. Additionally, in pulse-skipping mode the LT8625SP/LT8625SP-1 may also skip switching cycles at very light loads for improved efficiency, or at very high duty cycles in order to achieve better dropout. To enable pulse-skipping mode, tie the SYNC/MODE pin to GND.

Synchronization

To synchronize the LT8625SP/LT8625SP-1 oscillator to an external frequency, connect a square wave for the SYNC/MODE pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V (up to 6V), with a minimum on-time and off-time of 50ns.

While synchronized to an external clock, the part will run forced continuous mode to maintain regulation. The LT8625SP/LT8625SP-1 may be synchronized over a 300kHz to 4MHz range. The R_T resistor should be chosen to set the LT8625SP/LT8625SP-1 switching frequency to below the lowest synchronization input by approximately 20%. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 400kHz. The slope compensation is set by the R_T value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to

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avoid subharmonic oscillations at the frequency set by R_T, then the slope compensation will be sufficient for all synchronization frequencies.

Setting the Switching Frequency

The LT8625SP/LT8625SP-1 uses a constant frequency PWM architecture that can be programmed to switch from 300kHz to 4MHz by using a resistor tied from the RT pin to GND. Table 1 shows the necessary R_T value for a desired switching frequency.

Table 1. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.3	392
0.4	287
0.5	226
0.6	187
0.7	154
0.8	137
0.9	118
1.0	105
1.2	86.6
1.4	71.5
1.6	61.9
1.8	53.6
2	47.0
2.5	35.7
3	28.7
3.5	23.2
4	18.0

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range. The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated using Equation 1.

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}\left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)} \quad (1)$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.29V and ~0.13V, respectively at maximum load) and $t_{ON(MIN)}$ is the minimum top switch on-time (see the Electrical Characteristics table). This equation shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

For transient operation, V_{IN} may go as high as the absolute maximum rating of 18V regardless of the R_T value; however, the LT8625SP/LT8625SP-1 will reduce switching frequency as necessary to maintain control of inductor current to assure safe operation.

In pulse-skipping mode, the LT8625SP/LT8625SP-1 is capable of a maximum duty cycle of approximately 99%, and the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch (provided there is sufficient headroom (~0.4V) between SV_{IN} and SET for the current reference circuit to function correctly. In this mode the LT8625SP/LT8625SP-1 skips switch cycles, resulting in a lower switching frequency than programmed by R_T. The LT8625SP/LT8625SP-1 will switch as frequently as necessary to keep the boost capacitor refreshed, with a minimum switching frequency of approximately 80kHz. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

In FCM, the LT8625SP/LT8625SP-1 does not skip cycles, and so the maximum duty cycle is limited by the minimum off time and chosen switching frequency. For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios and thus must operate in FCM, use Equation 2 to set switching frequency.

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)} \quad (2)$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.29V and ~0.13V, respectively at maximum load), f_{SW} is the switching frequency (set by R_T), and $t_{OFF(MIN)}$ is the minimum switch off-time.

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Inductor Selection and Maximum Output Current

The LT8625SP/LT8625SP-1 is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions, the LT8625SP/LT8625SP-1 safely tolerates operation with a saturated inductor through the use of a high-speed peak-current mode architecture.

A good first choice for the inductor value is given by Equation 3.

$$L = \left(\frac{V_{OUT} + V_{SW(BOT)}}{f_{SW}} \right) \bullet 0.5 \quad (3)$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.13V) and L is the inductor value in µH.

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus ½ of inductor current. See Equation 4.

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2} \Delta I_L \quad (4)$$

where ΔI_L Is the inductor ripple current as calculated in Equation 6 and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 3A output should use an inductor with an RMS rating of greater than 3A and an I_{SAT} of greater than 4A. During long duration overload or short-circuit conditions, the inductor RMS rating requirement is greater to avoid overheating of the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 0.015Ω, and the core material should be intended for high frequency applications.

The LT8625SP/LT8625SP-1 limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is 16A at low duty cycles and decreases linearly to 13A at duty cycle = 80%. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current (see Equation 5).

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} \quad (5)$$

The peak-to-peak ripple current in the inductor can be calculated using Equation 6.

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right) \quad (6)$$

where f_{SW} is the switching frequency of the LT8625SP/LT8625SP-1, and L is the value of the inductor. Therefore, the maximum output current that the LT8625SP/LT8625SP-1 will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency and maximum input voltage used in the desired application.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower and the LT8625SP/LT8625SP-1 may operate with higher ripple current. This allows use of a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that low inductance may result in discontinuous operation, which further reduces maximum load current.

For more information about maximum output current and discontinuous operation, see Analog Device's Application Note 44.

For duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillation. See Application Note 19. Equation 7 calculates that minimum inductance.

$$L_{MIN} = \frac{PV_{IN}(2 \bullet DC - 1)}{4.4 \bullet f_{SW}} \quad (7)$$

where DC is the duty cycle ratio (V_{OUT}/V_{IN}) and f_{SW} is the switching frequency.

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Input Capacitors

The PV_{IN} of the LT8625SP/LT8625SP-1 should be bypassed with at least three ceramic capacitors for best performance. Two small ceramic capacitors can be placed close to the part (C_{OPT1}, C_{OPT2}). These capacitors should be 0402 or 0603 in size.

Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8625SP/LT8625SP-1 is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8625SP/LT8625SP-1's voltage rating. This situation is easily avoided (see Analog Device's Application Note 88). When SV_{IN} and PV_{IN} are powered from the same supply, a small RC filter (e.g., 10Ω and 1µF) from the supply to SV_{IN} can be added for particularly noise sensitive applications. If SV_{IN} and PV_{IN} are powered from independent supplies, SV_{IN} should also be bypassed with a single small ceramic capacitor of at least 1µF placed as close to the pin as possible.

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8625SP/LT8625SP-1 to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8625SP/LT8625SP-1's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Applications section.

Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost, but transient performance will suffer and may cause loop instability. See the Typical Applications in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

The LT8625SP/LT8625SP-1 will typically be operated at a switching frequency of 2MHz. Table 2 shows some examples of output capacitors with ideal frequency characteristics for when operating at switching frequencies around 2MHz. Figure 6 shows the frequency characteristics of these capacitors; it can be seen that a combination of these capacitors will minimize the impedance at the switching frequency on the output and keep the impedance low enough to suppress any higher frequency harmonics near the switching frequency, thus achieving the lowest output ripple.

Table 2. Examples of Output Capacitors with Desirable Frequency Characteristics for 2MHz Operation

PART DESCRIPTION	MANUFACTURER/PART NUMBER
22µF, X7R, 10V, 20% 1206	MURATA, GRM31CR71A226ME15
10µF, X7R, 25V, 10% 1206	MURATA, GRM31CR71E106KA12
4.7µF, X7S, 16V, 10% 0603	MURATA, GRM188C71C475KE21

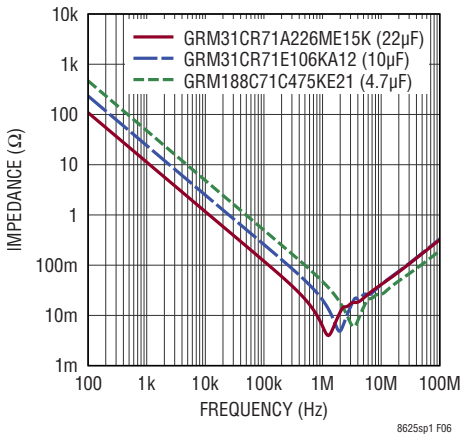

Figure 6. Frequency Characteristics of Example Output Capacitors for 2MHz operation

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Output Voltage

The LT8625SP/LT8625SP-1 incorporates a precision 100µA current source flowing out of the SET pin, which also ties to the error amplifier's non-inverting input. Figure 7 illustrates that connecting a resistor from SET to GND generates a reference voltage for the error amplifier. This reference voltage is simply the product of the SET pin current and the SET pin resistor. The error amplifier's unity-gain configuration produces a low impedance version of this voltage on its inverting input, the OUTS pin, which is externally tied to output voltage of the circuit.

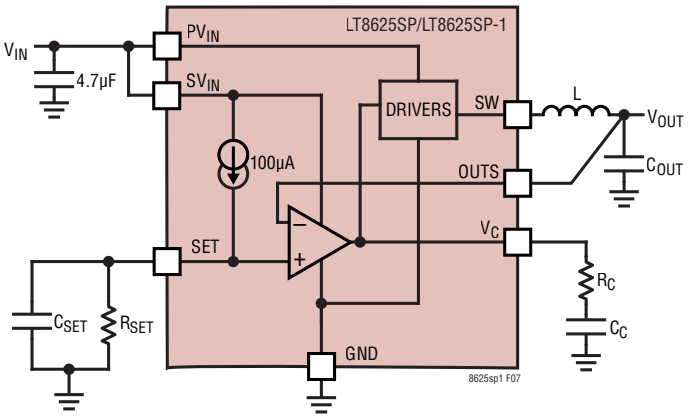

Figure 7. Adjustable Reference for Error Amplifier

The LT8625SP/LT8625SP-1's error amplifier and current reference allows for a wide output voltage range from 0V (using a 0Ω resistor) to 6V. A PNP-based input pair is active from V_{OUT} equals 0V up to V_{IN} minus 0.9V and an NPN-based input pair is active for output voltages where $V_{IN} – V_{OUT} < 0.5V$ or less, with a smooth transition between the two input pairs in between these ranges. The PNP-based input pair is designed to offer the best overall performance as it is active in the vast majority of applications; refer to the Electrical Characteristics table for details on offset voltage, SET pin current and output noise. Output noise variation with error amp input pair can be found in Typical Performance Characteristics section. Table 3 lists many common output voltages and their corresponding 1% R_{SET} resistors. Where the exact resistor value required for the output voltage is not available, two resistors can be paralleled to achieve the desired value. For example, for a 0.8V output voltage a resistor value of exactly 8kΩ is desired. The closest value with a single 1% resistor is 8.06k; with two resistors, 8.25k can be paralleled with 267k to achieve (almost) exactly 8k. 0.1% resistors may be used in order to achieve higher accuracy.

Table 3. 1% Resistor for Common Output Voltages

V_{OUT} (V)	R_{SET} (kΩ)
0.8	8.06
1	10
1.8	18
2.5	24.9
3.3	33.2
5	49.9

The benefit of using a current reference compared with a voltage reference as used in conventional regulators is that the regulator always operates in unity gain configuration, independent of the programmed output voltage. This allows the LT8625SP/LT8625SP-1 to have loop gain, frequency response, and bandwidth independent of the output voltage. Moreover, since none of the error amp gain is needed to amplify the SET pin voltage to a higher output voltage, output load regulation is more tightly specified.

Since the zero T_C current source is highly accurate, the SET pin resistor can become the limiting factor in achieving high accuracy. Hence, it should be a precision resistor. Additionally, any leakage paths to or from the SET pin create errors in the output voltage. If necessary, use high quality insulation (e.g., Teflon, Kel-F); moreover, cleaning of all insulating surfaces to remove fluxes and other residues may be required. High humidity environments may require a surface coating at the SET pin to provide a moisture barrier.

Since the SET pin is a high impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This is most noticeable when operating with a minimum output capacitor at heavy load currents. Bypassing the SET pin with a small capacitance to GND resolves this issue – 100nF is sufficient. This is the minimum recommended capacitance. In general a larger capacitance is typically preferred (see Set Pin (Bypass) Capacitance: Noise, Transient Response and Soft-Start section).

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For applications requiring higher accuracy or an adjustable output voltage, the SET pin may be actively driven by an external voltages source capable of sinking 100µA. Connecting a precision voltage reference to the SET pin eliminates any errors present in the output voltage due to the reference current and SET pin resistor tolerances.

Output Sensing and Stability

The LT8625SP/LT8625SP-1's OUTS pin provides a Kelvin sense connection to the output. The SET pin resistor's GND side provides a Kelvin sense connection to the load's GND side.

The LT8625SP/LT8625SP-1 internal error amplifier has a relatively high voltage gain of ~2800. Therefore, it is very important to avoid adding extra impedance (ESR and ESL) to the feedback loop and to minimize the noise coupling onto the OUTS pin, as a combination of excessive parasitics and noise injection can cause instability in the system. To that end, minimize the effects of PCB trace and solder inductance by tying the OUTS pin directly to C_{OUT} and the GND side of C_{SET} directly to the GND side of C_{OUT}. If this is not possible, for example, due to a design requiring remote sense, a small local OUTS capacitor of 150pF or less may be added for noise decoupling at the OUTS pin. Refer to the LT8625SP/LT8625SP-1 demo board manual for more information on the recommended layout that meets these requirements.

The LT8625SP/LT8625SP-1 is an externally compensated part, so even if the recommended layout is not followed (sometimes it is not possible due to application specific limitations), it is possible to choose a more conservative compensation with lower gain or bandwidth in order to retain stability during operation. However, this would be at the expense of transient response. A superior layout allows a better trade-off between transient response, phase margin, and output noise performance when selecting compensation values.

Frequency Compensation

Loop compensation determines the stability and transient performance and is provided by the components tied to the V_C pin. Generally, a capacitor (C_C) and a resistor (R_C) in series to ground are used. Designing the compensation network can be complicated and the best values depend on the application. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. LTpowerCAD simulation can help in this process. Stability should then be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load.

Figure 8 shows an equivalent circuit for the LT8625SP/LT8625SP-1 control loop. The error amplifier is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switches, and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C pin. Note that the output capacitor integrates this current, and that the capacitor on the V_C pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. A zero is required and comes from a resistor R_C in series with C_C. This simple model works as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. For more information about the compensation of switching mode power supplies, refer to Application Note 149: Modeling and Loop Compensation Design of Switching Mode Power Supplies.

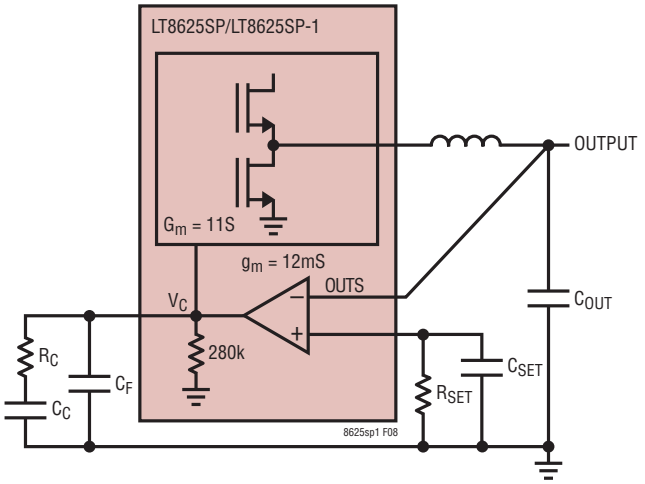

Figure 8. Model for Loop Response

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Enable Pin

The LT8625SP/LT8625SP-1 is in shutdown when the EN/UVLO pin is low and active when the pin is high. The rising threshold of the EN/UVLO comparator is 1.32V, with 50mV of hysteresis. The EN/UVLO pin can be tied to V_{IN} if the shutdown feature is not used or tied to a logic level if shutdown control is required.

When the enable pin drops below 1.32V, the part enters a shutdown state where the part stops switching, but internal circuitry will continue drawing current as the $INTV_{CC}$ regulator is still awake. Full shutdown is guaranteed when the enable pin drops below 400mV. In full shutdown the $INTV_{CC}$ regulator is disabled and the part will draw less than 100µA.

Adding a resistor divider from PV_{IN} to EN/UVLO programs the LT8625SP/LT8625SP-1 to regulate the output only when PV_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $PV_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $PV_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R_{EN1} and R_{EN2} such that they satisfy Equation 8.

$$PV_{IN(EN)} = \left(\frac{R_{EN1}}{R_{EN2}} + 1\right) \bullet 1.32V \quad (8)$$

where the LT8625SP/LT8625SP-1 will remain off until PV_{IN} is above $PV_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $PV_{IN(EN)}$.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from SV_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply enough current for the LT8625SP/LT8625SP-1's circuitry and must be bypassed to ground with a minimum 1µF capacitor. If SV_{IN} is connected to a different supply than PV_{IN}, be sure to bypass with a local ceramic capacitor. Do not connect an external load to the $INTV_{CC}$ pin.

Set Pin (Bypass) Capacitance: Noise, Transient Response and Soft-Start

In addition to reducing output noise, using a SET pin bypass capacitor will reduce sensitivity to any parasitic coupling of voltage spikes onto the SET pin. Note that any bypass capacitor leakage deteriorates the LT8625SP/LT8625SP-1's DC regulation. Capacitor leakage of even 100nA is a 0.1% DC error. Therefore, it is recommended to use a good quality, low leakage ceramic capacitor.

Ceramics are manufactured with various dielectrics, each with a different behavior across temperature and applied voltage. Care should be taken when selecting a ceramic to bypass the SET pin, as this is a critical component. An X7R (or better) ceramic capacitor is strongly recommended for its superior stability across temperature and DC voltage bias. Additionally, it is recommended to use larger case sizes for better DC bias characteristics as well as AC voltage characteristics.

As shown in Figure 9, capacitor DC bias characteristics tend to improve as component case size increases.

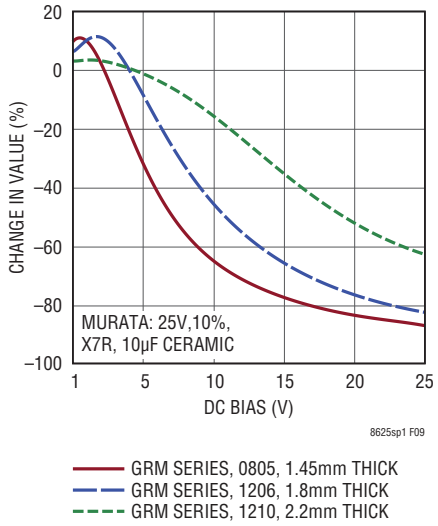


Figure 9. Capacitor Voltage Coefficient for Different Case Sizes

APPLICATIONS INFORMATION

Larger case sizes are also beneficial for improved AC voltage characteristics. Capacitor values are often rated at $1V_{RMS}$ of AC voltage, and can drop significantly when operating near $0V_{RMS}$, which is the operating condition of a bypass capacitor.

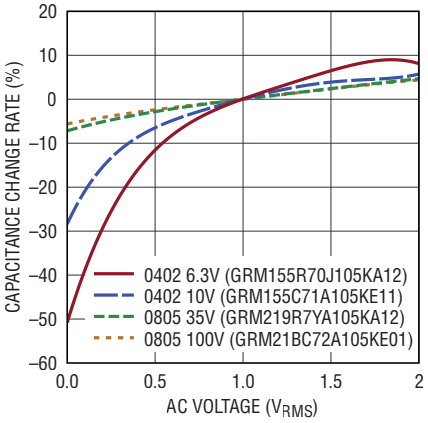
As shown in Figure 10a, Figure 10b, and Figure 10c, larger case sizes tend to experience a smaller capacitance drop when operating near $0V_{RMS}$. Therefore, an 0805 or larger ceramic capacitor should be used for the SET pin bypass capacitor for best performance. A larger desired capacitance value may require larger case sizes; for example, a 4.7µF value should use 1206 or larger. Table 4 shows some recommended SET pin capacitors.

Table 4. Suggested SET Capacitor Part Numbers

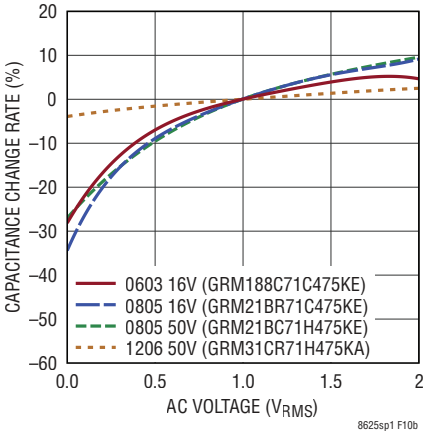
PART DESCRIPTION	MANUFACTURER/PART NUMBER
1µF, X7R, 35V, 0805	MURATA, GRM219R7YA105KA12
4.7µF, X7R, 50V, 1206	MURATA, GRM31CR71H475MA12
10µF, X7R, 100V, 1210	MURATA, GRM32EC72A106KE05

For high-vibration environments, non-piezoelectrically responsive capacitors should be used at the SET pin for optimal performance. A piezoelectric ceramic capacitor generates voltage, across its terminals due to mechanical stress upon it, induced by mechanical vibrations or thermal transients. Film capacitors are the preferred option. If a ceramic must be used, soft-termination ceramics are available, which reduce the sensitivity to the piezoelectric effect.

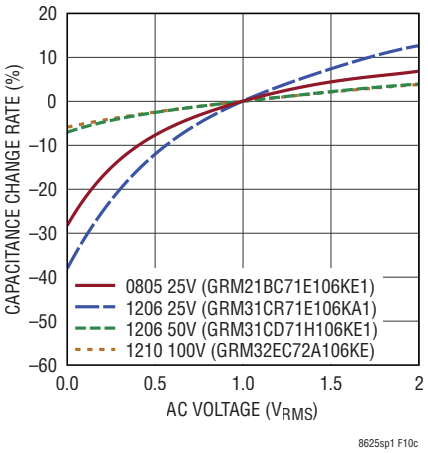
Using a SET pin bypass capacitor also soft-starts the output and limits inrush current. Soft-starting the output prevents a current surge on the input supply. The SET pin capacitor and resistor values set the ramp-up time of the reference voltage, and the output voltage will track this voltage. The SET pin resistor size is determined by the application's desired output voltage, however the capacitor size may be selected to achieve the desired ramp up time. It is important to keep in mind the size of the SET pin capacitor also plays a role in noise performance, which is typically the more important factor in determining the size of this capacitor.



(a) Rated Capacitance = 1µF



(b) Rated Capacitance = 4.7µF



(c) Rated Capacitance = 10µF

Figure 10. AC Voltage Characteristics for Different Capacitor Case Sizes

APPLICATIONS INFORMATION

Without fast start-up enabled, the R_C time constant, formed by the SET pin resistor and capacitor, controls soft-start time. Tie the PGFB pin to 0.5V to disable fast start-up. Ramp-up rate from 0% to 90% of nominal V_{OUT} is given by Equation 9.

$$t_{START\_NO\_FAST\_START-UP} = 2.3 \bullet R_{SET} \bullet C_{SET} \quad (9)$$

With fast-start-up enabled, the start-up time can be significantly reduced with the ramp-up time from 0% to 90% of nominal V_{OUT} is given by Equation 10.

$$t_{START\_FAST\_START-UP} = \frac{100\mu A \bullet R_{SET} \bullet C_{SET}}{2.7mA} \quad (10)$$

In most applications, fast start-up will be enabled, in which case a minimum SET capacitor size of 1µF is recommended for preventing reference voltage overcharge as well as ensuring good noise performance.

The SET pin is pulled to ground with a 500Ω MOSFET ($R_{SET-PULLDOWN}$) during shutdown, thermal shutdown, V_{CC} UVLO or V_{IN} UVLO. To ensure soft-start when the part exits any of the above conditions, there must have been sufficient time to allow the SET pin to be pulled to close to ground prior to start-up. This time will be a function of the chosen SET pin capacitance and $R_{SET-PULLDOWN}$.

Soft-Start and Power Sequencing

As discussed in the previous Set Pin (Bypass) Capacitance: Noise, Transient Response and Soft-Start section, soft-start is achieved through the controlled ramp up time of the SET pin voltage. Soft-start is guaranteed when PV_{IN} and SV_{IN} are tied together.

When PV_{IN} and SV_{IN} are powered by independent supplies, power sequencing must be considered to guarantee soft-start. The SET pin voltage should start at 0V when PV_{IN} is applied. To guarantee soft-start, do not power PV_{IN} last when sequencing PV_{IN}, SV_{IN} and EN/UVLO . An example of a specific case to avoid is having SV_{IN} and EN/UVLO powered up before PV_{IN}; in this instance, the SET pin voltage will have risen to some voltage greater than 0V when PV_{IN} is applied, and the LT8625SP/LT8625SP-1 will not soft-start correctly.

If connecting EN/UVLO to PV_{IN} instead of driving it with a digital signal, it is recommended to connect EN/UVLO to PV_{IN} through a resistor divider to set an appropriate UVLO threshold. This ensures correct startup and shutdown behavior in the event of rapid power cycling.

Fast Start-Up

For ultralow noise applications that require low 1/f noise (i.e., at frequencies below 100Hz), a larger value SET pin capacitor is required, up to 22µF. A larger value capacitor can be used but care should be taken regarding leakage. While normally larger capacitors would significantly increase the regulator's start-up time, the LT8625SP/LT8625SP-1 incorporates fast start-up circuitry that increases the SET pin current to about 2.7mA during start-up.

Upon start-up, the 2.7mA current source remains engaged while PGFB is below the Power Good threshold of 462.5mV, unless the regulator is in thermal shutdown, SV_{IN} is too low, or $INTV_{CC}$ has fallen too low.

The fast start-up circuit is disabled permanently once PGFB rises above the Power Good threshold, until either the part is powered down, or the part is placed into shutdown by pulling the EN/UVLO pin below 1.32V.

There is one more condition under which the 2.7mA current source is disabled during start-up. The purpose of this is to prevent overcharging V_{SET}. Since the part assumes that the PGFB pin is an accurate indication of the voltage on the SET pin, it assumes that V_{OUTS} follows V_{SET} closely. However, this may not always be the case – for example if the output capacitance is very large, or if for some reason the output is temporarily shorted to GND. Therefore, fast charge is also disabled whenever the V_C pin has railed to its maximum value (when V_{SET} has risen significantly about V_{OUTS}). This prevents incorrect behavior where the 2.7mA current sources stays on even when V_{SET} has risen above its intended value.

This means there is also a minimum SET capacitor requirement for using fast start-up without overcharging the reference voltage. This will depend on the compensation network, as the part is depending on the V_C pin voltage rising to its maximum value to inform the part to pause fast charge.

The recommended minimum required SET capacitance value to prevent overcharging the reference voltage is given in Equation 11.

APPLICATIONS INFORMATION

$$\text{Minimum } C_{SET} = 27 \bullet \frac{C_{COMP}}{V_{SET}} \quad (11)$$

If programmable power good and fast start-up capabilities are not required, the PGFB pin must be tied to 0.5V.

Programmable Power Good

As illustrated in the Block Diagram, power good threshold is user programmable using the ratio of two external resistors, $R_{PGFB(BOT)}$ and $R_{PGFB(TOP)}$ (see Equation 12).

$$V_{OUT(PG\_THRESHOLD)} = 0.5V \bullet \left(1 + \frac{R_{PGFB(TOP)}}{R_{PGFB(BOT)}}\right) + I_{PGFB} \bullet R_{PGFB(TOP)} \quad (12)$$

If the PGFB pin increases above 537.5mV or decreases below 462.5mV, the open-drain PG pin de-asserts and becomes high impedance. The power good comparator has 5mV hysteresis. The PGFB pin current (I_{PGFB}) from the Electrical Characteristics table must be considered when determining the resistor divider network. Please note that the programmable power good and fast start-up capabilities are disabled when PGFB is tied to 0.5V or when the device is in shutdown.

The PGFB pin current (I_{PGFB}) can be ignored if $R_{PGFB(BOT)}$ is less than 50k. Table 5 suggests some 1% PGFB resistor divider values for common V_{OUT} configurations.

Table 5. Suggested PGFB Resistor Divider Values

V_{OUT} (V)	$R_{PGFB(TOP)}$ (kΩ)	$R_{PGFB(BOT)}$ (kΩ)
0.8	29.4	48.7
0.9	39.2	48.7
1	49.9	49.9
1.2	69.8	49.9
1.8	130	49.9
3.3	280	49.9
5	453	49.9

Power Good at Start-Up

In some cases, certain ceramic capacitors on the SET pin may cause a small dip in the SET voltage during the transition from fast start-up current to 100µA. SET capacitors with better AC voltage characteristics (see Figure 10) may be less susceptible to this phenomenon. This SET voltage dip may cause a glitch on PG during start-up. If a PG glitch during start-up may cause an issue in the system, this can be handled simply by adding a small capacitor between the PGFB pin and GND (C_{PGFB}) as shown in Figure 11.

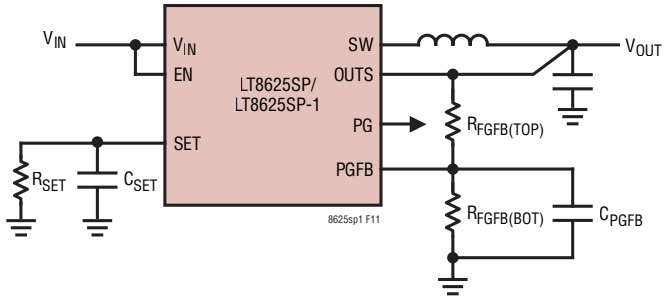


Figure 11. Schematic with C_{PGFB}

The addition of C_{PGFB} delays the time past the PG threshold at which fast start-up current turns off; this capacitor can be sized to compensate for the SET voltage dip. Table 6 shows suggested C_{PGFB} values for a given C_{SET} value, assuming $R_{PGFB(BOT)} \approx 50k\Omega$ (as shown in Table 5). For V_{OUT} = 0.5V, the OUTS pin should be tied to the PGFB pin with a 12.1k resistor, and a C_{PGFB} value chosen according to Table 6.

Table 6. Suggested C_{PGFB} Value for Given C_{SET}

C_{SET} (µF)	C_{PGFB} (PF)
0.47	220
1	470
2.2	1000
4.7	2200
10	4700

Multiphase Operation

For output loads that demand more current, multiple LT8625SP/LT8625SP-1 can be connected in parallel to the same output. To do this, the V_C, OUTS pins are connected together, and each LT8625SP/LT8625SP-1's SW node is connected to the common output through its own inductor. The CLKOUT signal can be connected to the SYNC/MODE pin of the following LT8625SP/LT8625SP-1 to line up both the frequency and the phase of the entire system.

Tying the PHMODE pin to GND, $INTV_{CC}$, or floating the pin generates a phase difference between the LT8625SP/LT8625SP-1's internal clock and CLKOUT of 180°, 90°, or 120° respectively, which corresponds to 2-phase, 4-phase, or 3-phase operation. A total of 12 phases can be paralleled to run simultaneously out-of-phase with respect to each other by programming the PHMODE pin of each LT8625SP/LT8625SP-1 to different voltage levels. During FCM and Synchronization modes all devices will operate at the same frequency. Figure 12 shows a 2-phase application where two LT8625SP/LT8625SP-1 are paralleled to get one output capable of up to 16A.

Due to the current reference architecture of the LT8625SP/LT8625SP-1, the SET pins can also be tied together, as shown in Figure 12 for better noise performance in the low frequency range, reduced component count, and superior current sharing between the phases due to the use of a common reference.

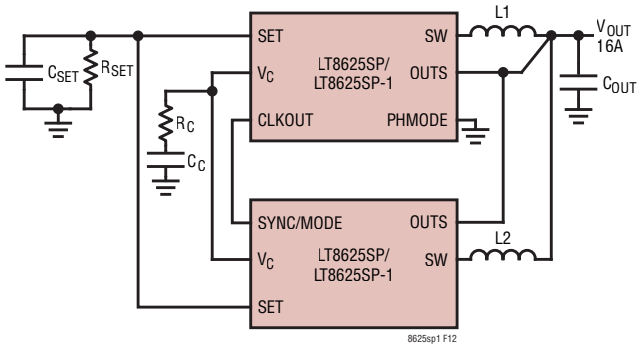


Figure 12. Paralleling Two LT8625SP/LT8625SP-1 Devices

If two SET pins are tied together as in Figure 12, the total current running through R_{SET} will be 200µA. The R_{SET} value should be sized accordingly; in this case, for $1V_{OUT}$, a R_{SET} value of 5kΩ will be required.

Output Voltages above 6V

The LT8625SP/LT8625SP-1 can be configured for output voltages above 6V, even though the SET pin voltage is limited to a maximum of 6V, by using a traditional resistor divider from V_{OUT} to OUTS, as shown in Figure 13. It is recommended to configure the SET pin voltage to be 5V, in which case the resistor values can be chosen according to Equation 14.

$$R1 = R2\left(\frac{V_{OUT} - 5V}{5V + R2 \bullet I_{OUTS}}\right) \quad (13)$$

The OUTS pin current must be taken into consideration in this configuration as an output divider is used. The OUTS pin current (I_{OUTS}) when $V_{SET} > 2V$ is 10µA ± 2.5µA, including variation over process and temperature. When $V_{SET} \leq 2V$, the OUTS pin current is 160nA ± 80nA per the Electrical Characteristics table. The divider values R1 and R2 can be chosen such that this OUTS pin current variation introduces < 0.1% error in output voltage regulation.

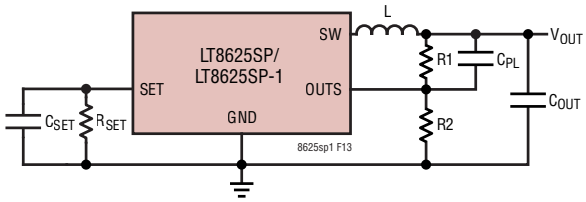


Figure 13. Configuring the LT8625SP/LT8625SP-1 for Output Voltages Above 6V

At output voltages above 6V, the low-frequency noise will have some dependency on the output voltage; the divider gains up the noise. By configuring the SET voltage to be 5V, this dependency is minimized; for example, the noise gain from a 5V reference to $9V_{OUT}$ will be ten times lower than the gain from a conventional 0.5V voltage reference to $9V_{OUT}$.

Shorted and Reversed Input Protection

The LT8625SP/LT8625SP-1 will tolerate a shorted output. The bottom switch current is monitored such that if inductor current is beyond safe levels, switching on of the top switch will be delayed until such time as the inductor current falls to safe levels.

There is another situation to consider in systems where the output will be held high when the input to the LT8625SP/LT8625SP-1 is absent. This may occur in battery charging applications or in battery-backup systems where a battery or some other supply is diode ORed with the LT8625SP/LT8625SP-1's output. If the PV_{IN} pin is allowed to float and the EN/UVLO pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT8625SP/LT8625SP-1's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate current draw in this state. If the

EN/UVLO pin is grounded the SW pin current will drop to ~50µA.

However, if the PV_{IN} pin is grounded while the output is held high, regardless of EN/UVLO, parasitic body diodes inside the LT8625SP/LT8625SP-1 can pull current from the output through the SW pin and the PV_{IN} pin. Figure 14 shows a connection of the PV_{IN} and EN/UVLO pins that will allow the LT8625SP/LT8625SP-1 to run only when the input voltage is present and that protects against a shorted or reversed input.

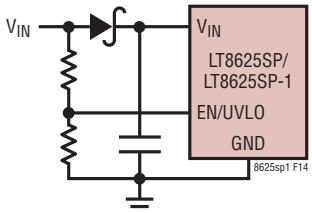


Figure 14. Reverse V_{IN} Protection

Thermal Considerations

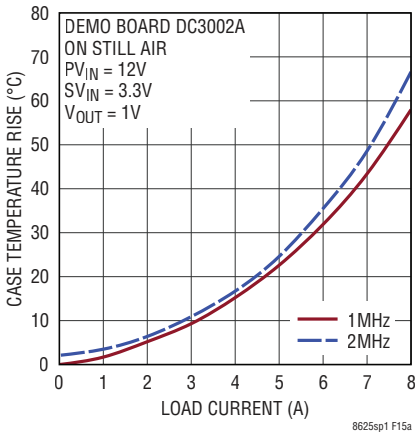
The LT8625SP/LT8625SP-1 offers exposed die back on the package top for heat sink mount. This option provides the capability improve thermal performance for the same load if an appropriately sized heat sink is mounted correctly on the package.

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8625SP/LT8625SP-1. The exposed pad on the bottom of the package should be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8625SP/LT8625SP-1. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8625SP/LT8625SP-1 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8625SP/LT8625SP-1 power dissipation by the thermal resistance from junction to ambient.

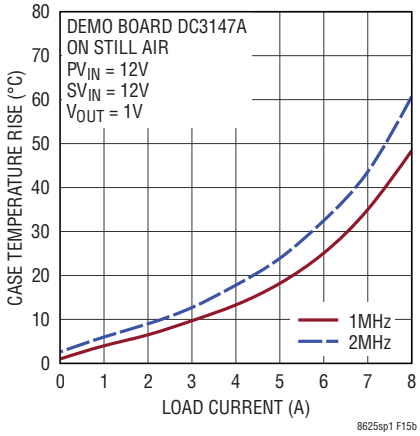
The internal overtemperature protection monitors the junction temperature of the LT8625SP/LT8625SP-1. If the junction temperature reaches approximately 165°C, the LT8625SP/LT8625SP-1 will stop switching and indicate a fault condition until the temperature drops about 5°C cooler.

Temperature rise of the LT8625SP/LT8625SP-1 is worst when operating at high load, high V_{IN} and high switching frequency. If the case temperature is too high for a given application, then either V_{IN}, switching frequency, or load current can be decreased to reduce the temperature to an appropriate level. Figure 15 shows examples of how case temperature rise can be managed by reducing switching frequency or load.

The LT8625SP/LT8625SP-1's top switch current limit decreases with higher duty cycle operation for slope compensation. This also limits the output current the LT8625SP/LT8625SP-1 can deliver for a given application. See curve in Typical Performance Characteristics.



(a) LT8625SP

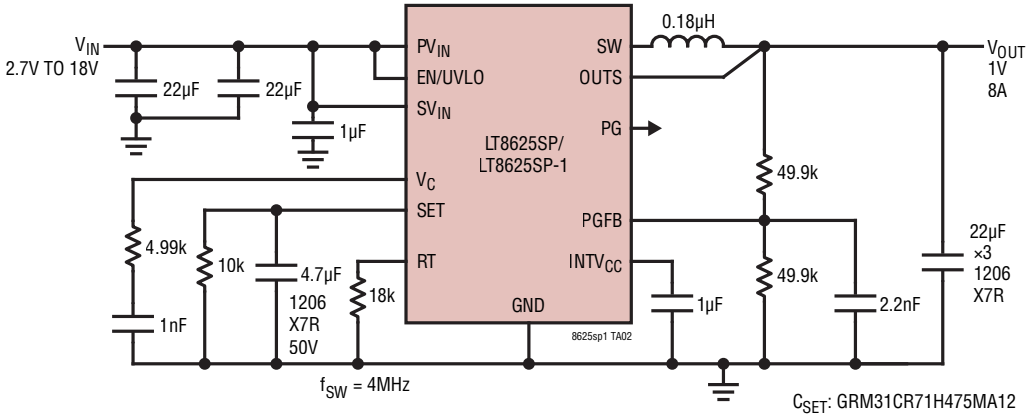


(b) LT8625SP-1

Figure 15. Case Temperature Rise

TYPICAL APPLICATIONS

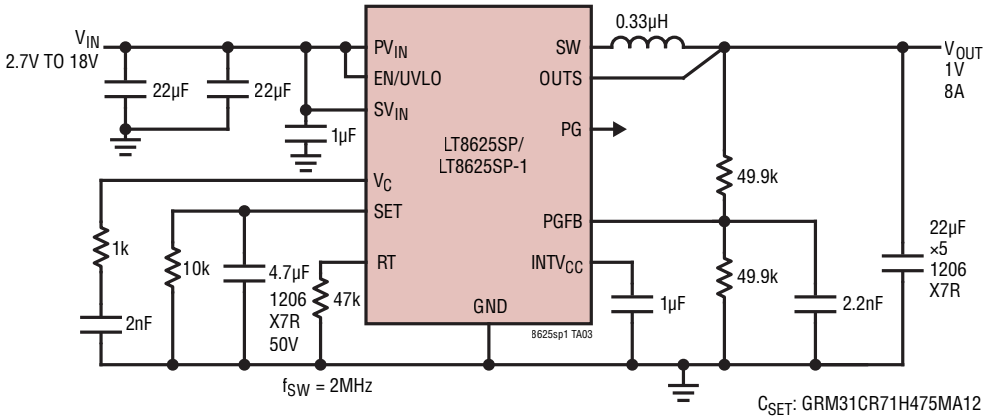
1V 8A 4MHz Step-Down Converter with Soft-Start, Fast Start-up and Power Good



PINS NOT USED IN THIS CIRCUIT:
BST, SYNC, PHMODE, CLKOUT

TYPICAL PERFORMANCE CHARACTERISTIC
4MHz, $1V_{OUT}$ NOISE DATA USES THIS CIRCUIT

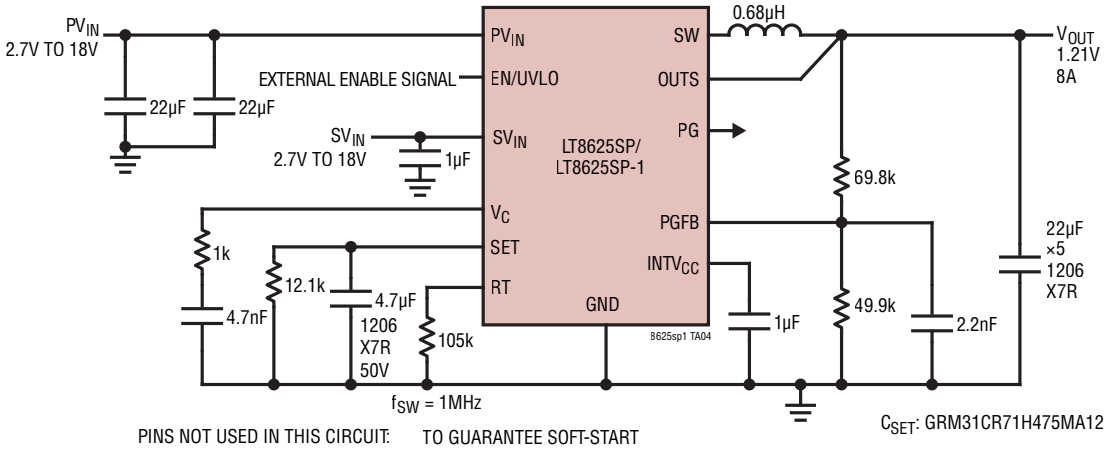
1V 8A 2MHz Step-Down Converter with Soft-Start, Fast Start-up and Power Good



PINS NOT USED IN THIS CIRCUIT:
BST, SYNC, PHMODE, CLKOUT

TYPICAL CHARACTERISTIC
2MHz, $1V_{OUT}$ NOISE DATA USES THIS CIRCUIT

1.2V 8A 1MHz Step-Down Converter with Soft-Start, Fast Start-up and Power Good

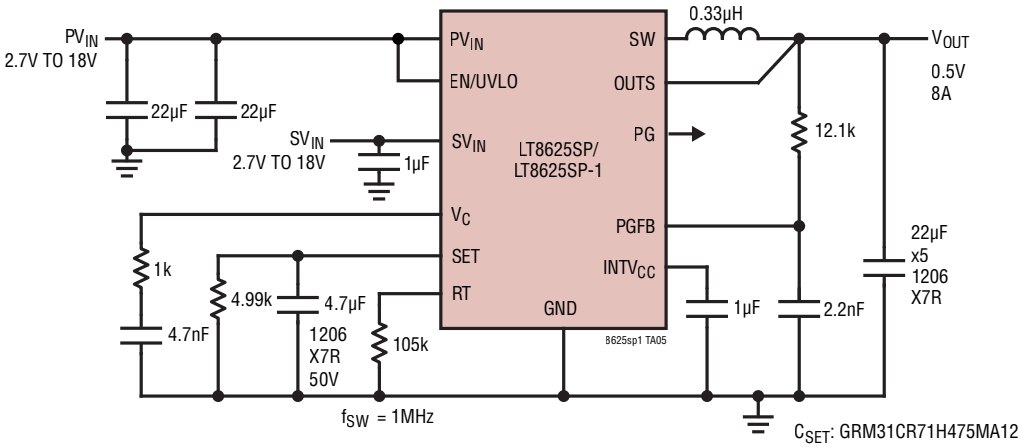


PINS NOT USED IN THIS CIRCUIT:
BST, SYNC, PHMODE, CLKOUT

TO GUARANTEE SOFT-START
DO NOT POWER PV_{IN} LAST WHEN SEQUENCING PV_{IN}, SV_{IN} AND EN/UVLO

TYPICAL APPLICATIONS

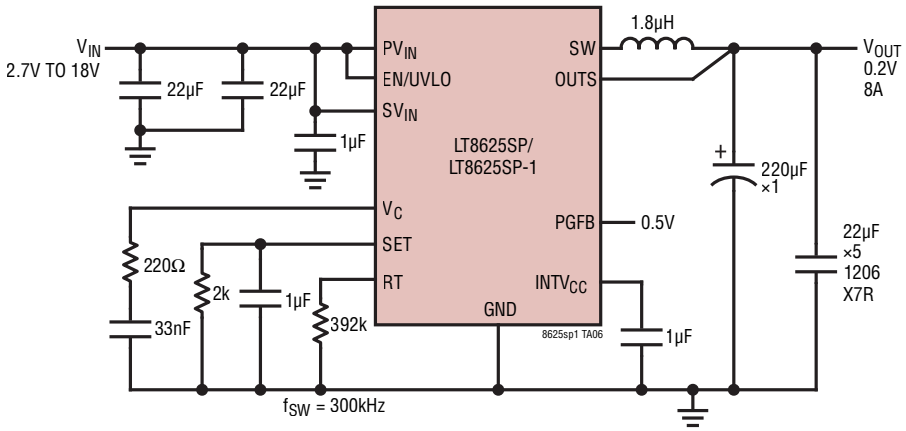
0.5V 8A 1MHz Step-Down Converter with Soft-Start, Fast Start-Up and Power Good



PINS NOT USED IN THIS CIRCUIT:
BST, SYNC, PHMODE, CLKOUT

TO GUARANTEE SOFT-START
DO NOT POWER PV_{IN} LAST WHEN SEQUENCING PV_{IN}, SV_{IN} AND EN/UVLO

0.2V 8A 300kHz Step-Down Converter with Soft-Start

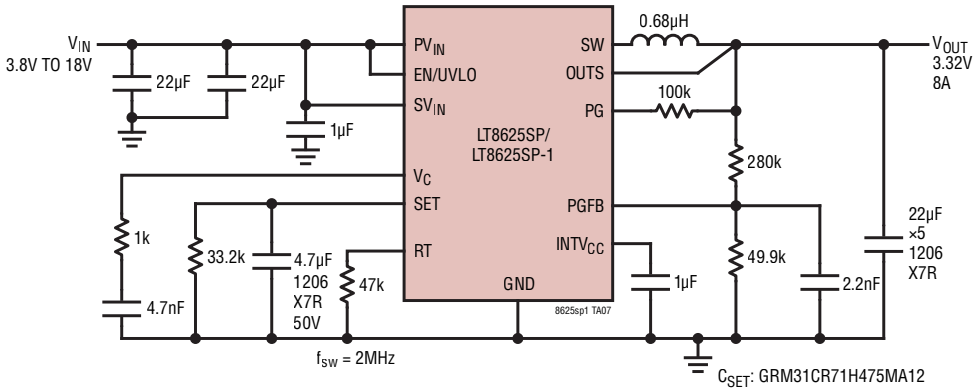


PINS NOT USED IN THIS CIRCUIT:
BST, SYNC, PHMODE, CLKOUT

**NOTE THAT APPLICATIONS WITH V_{OUT} BELOW 0.5V WILL NOT BE ABLE TO USE THE POWER GOOD AND FAST-STARTUP FUNCTIONALITIES.

TYPICAL APPLICATIONS

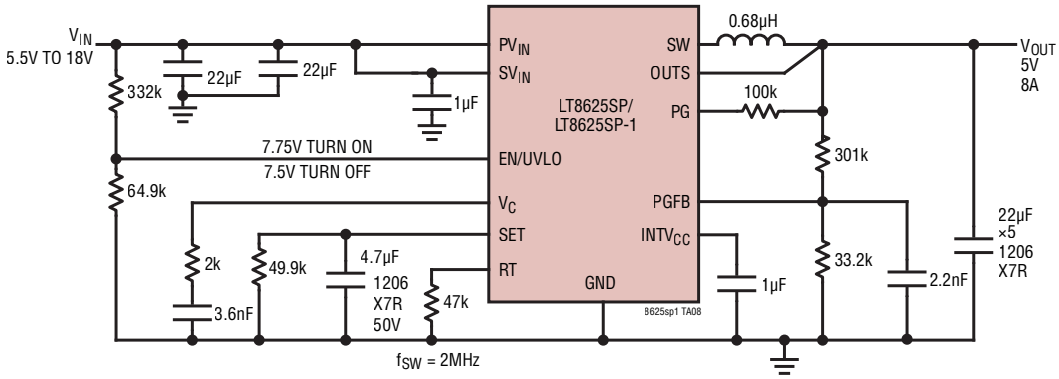
3.3V 8A 2MHz Step-Down Converter with Soft-Start, Fast Start-Up and Power Good



PINS NOT USED IN THIS CIRCUIT:
BST, SYNC, PHMODE, CLKOUT

TYPICAL CHARACTERISTIC
2MHz, 3.3V_{OUT} NOISE DATA USES THIS CIRCUIT

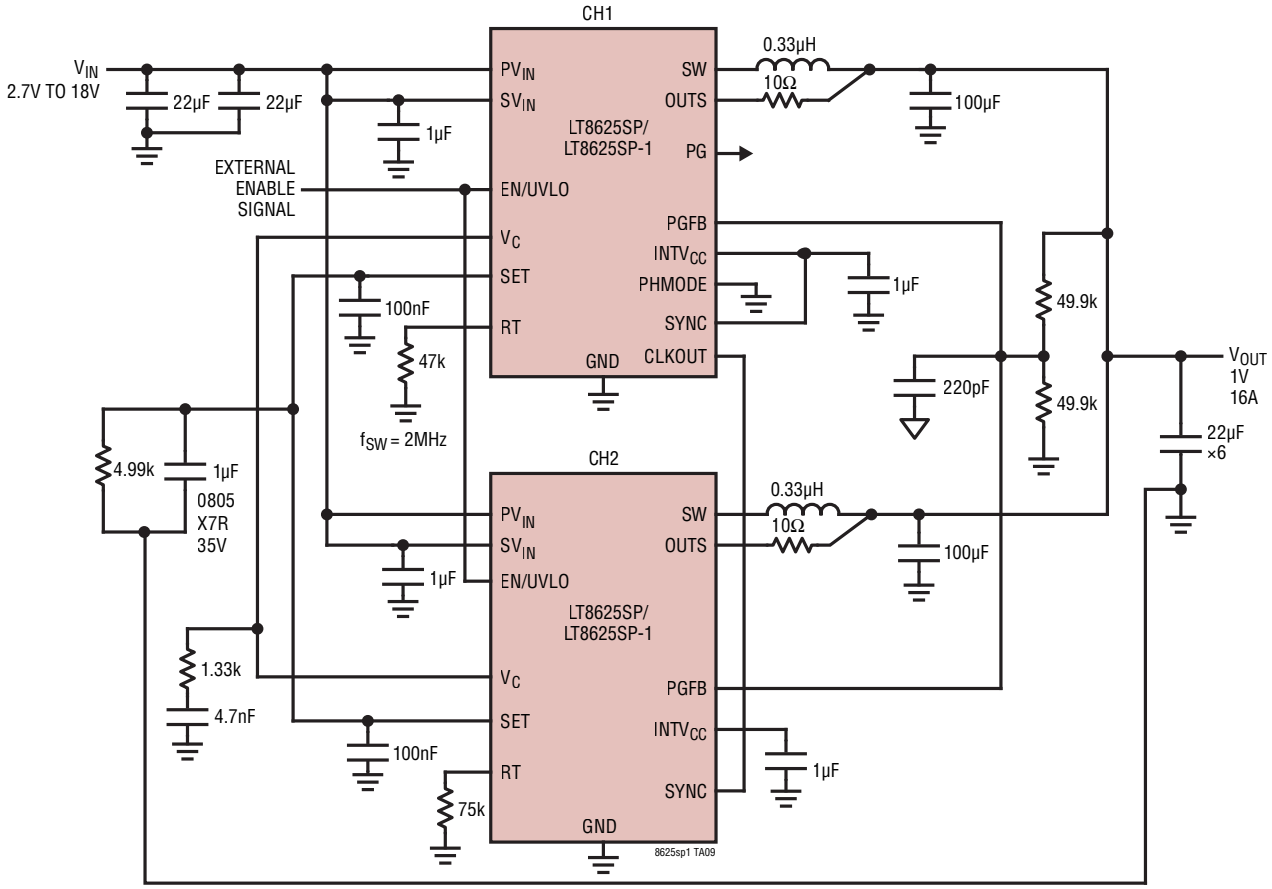
5V 8A 2MHz Step-Down Converter With Soft-Start, Fast Start-Up, Power Good and UVLO



PINS NOT USED IN THIS CIRCUIT:
BST, SYNC, PHMODE, CLKOUT

TYPICAL APPLICATIONS

1V 16A 2MHz 2-Phase Step-Down Converter With Soft-Start, Fast Start-Up, and Power Good



NOTE: CH2 IS SYNCHRONIZED TO 2MHz VIA SYNC PIN. RT RESISTOR VALUE MUST SET INTERNAL OSCILLATOR TO <1.6MHz (80% OF 2MHz)

V_C PINS TIED TOGETHER

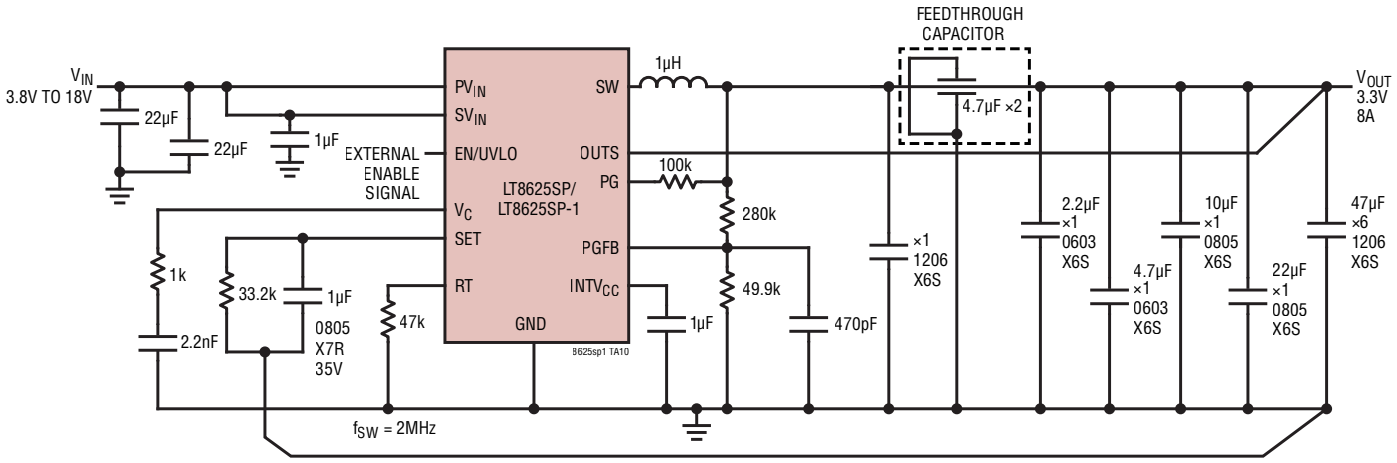
PHMODE TIED TO GND FOR 180 DEG. PHASE SHIFT AT CLKOUT

SET PINS CAN BE TIED TOGETHER FOR 200µA CURRENT REFERENCE. THIS PROVIDES LOWER 1/F NOISE AND BETTER CURRENT SHARING.

C_{SET}: GRM219R7YA105KA12

TYPICAL APPLICATIONS

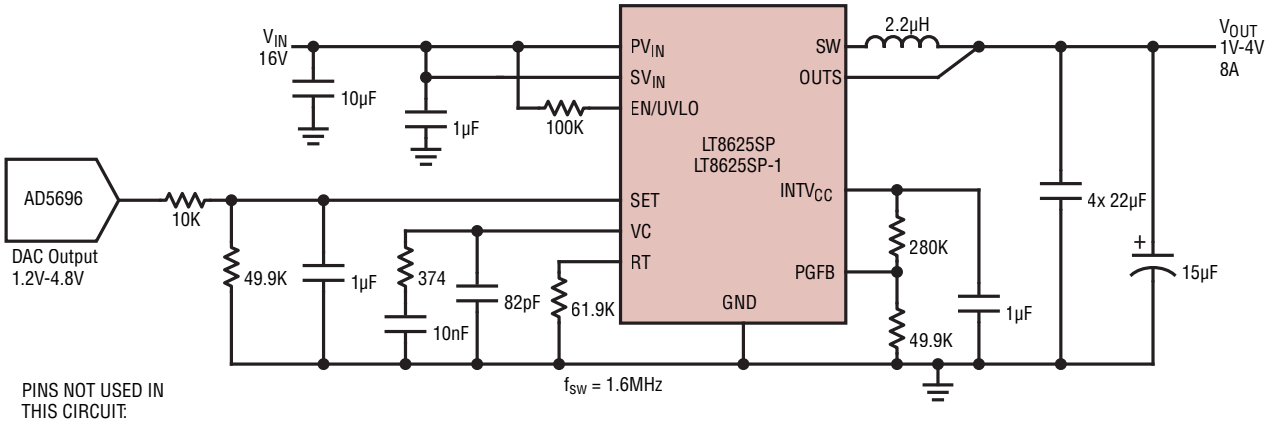
3.3V Step-Down Converter With Feedthrough Capacitors and Remote Sense



PINS NOT USED IN THIS CIRCUIT:
BST, SYNC, PHMODE, CLKOUT

C_{SET}: GRM219R7YA105KA12

Dynamic Voltage Control 1V-4V 1.6MHz Step-Down Converter with External DAC

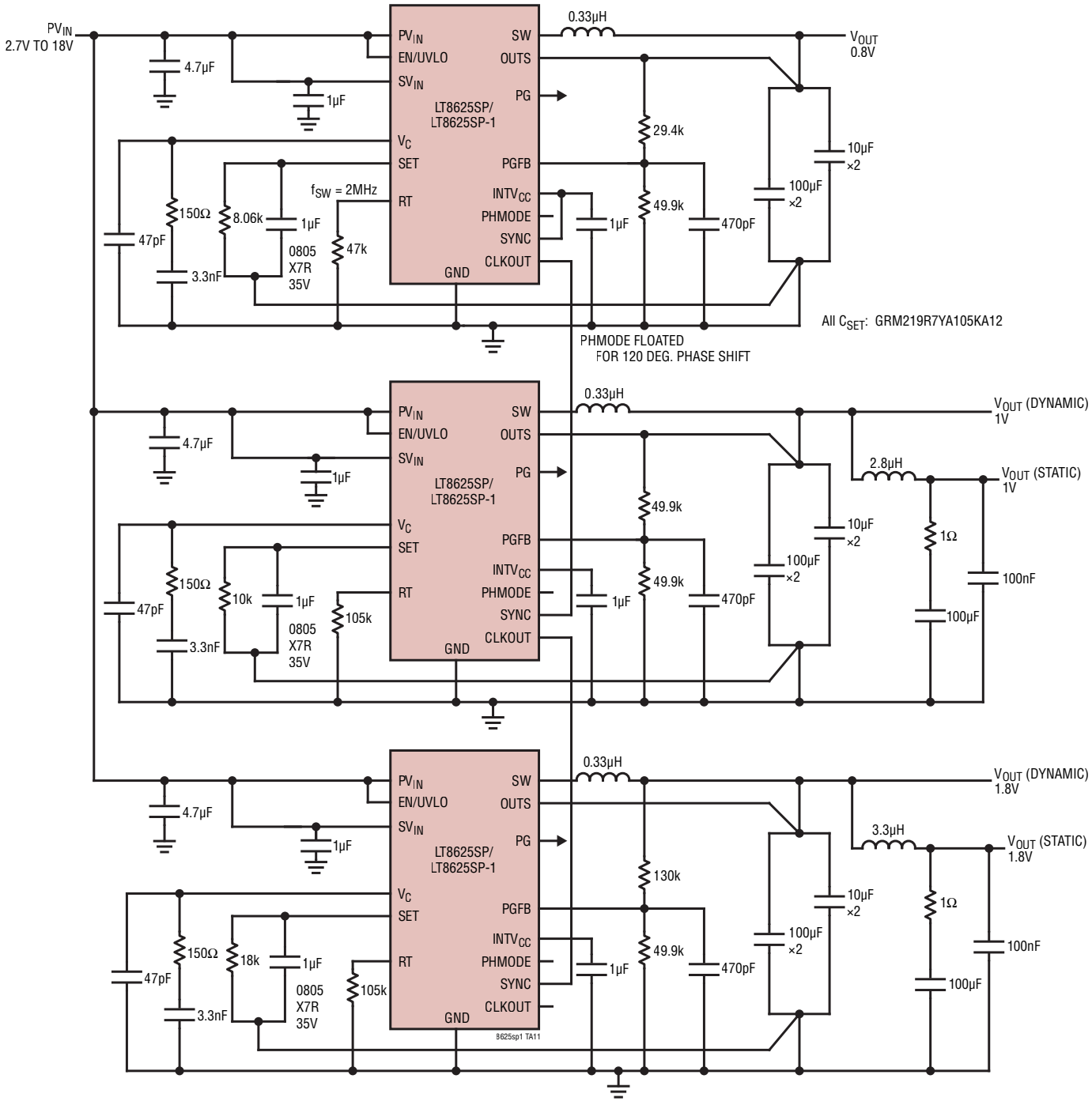


PINS NOT USED IN THIS CIRCUIT:
BST, SYNC, PHMODE, CLKOUT

C_{SET}: 1µF 16V X7R 0603 (GRM188R71C105MA12D)

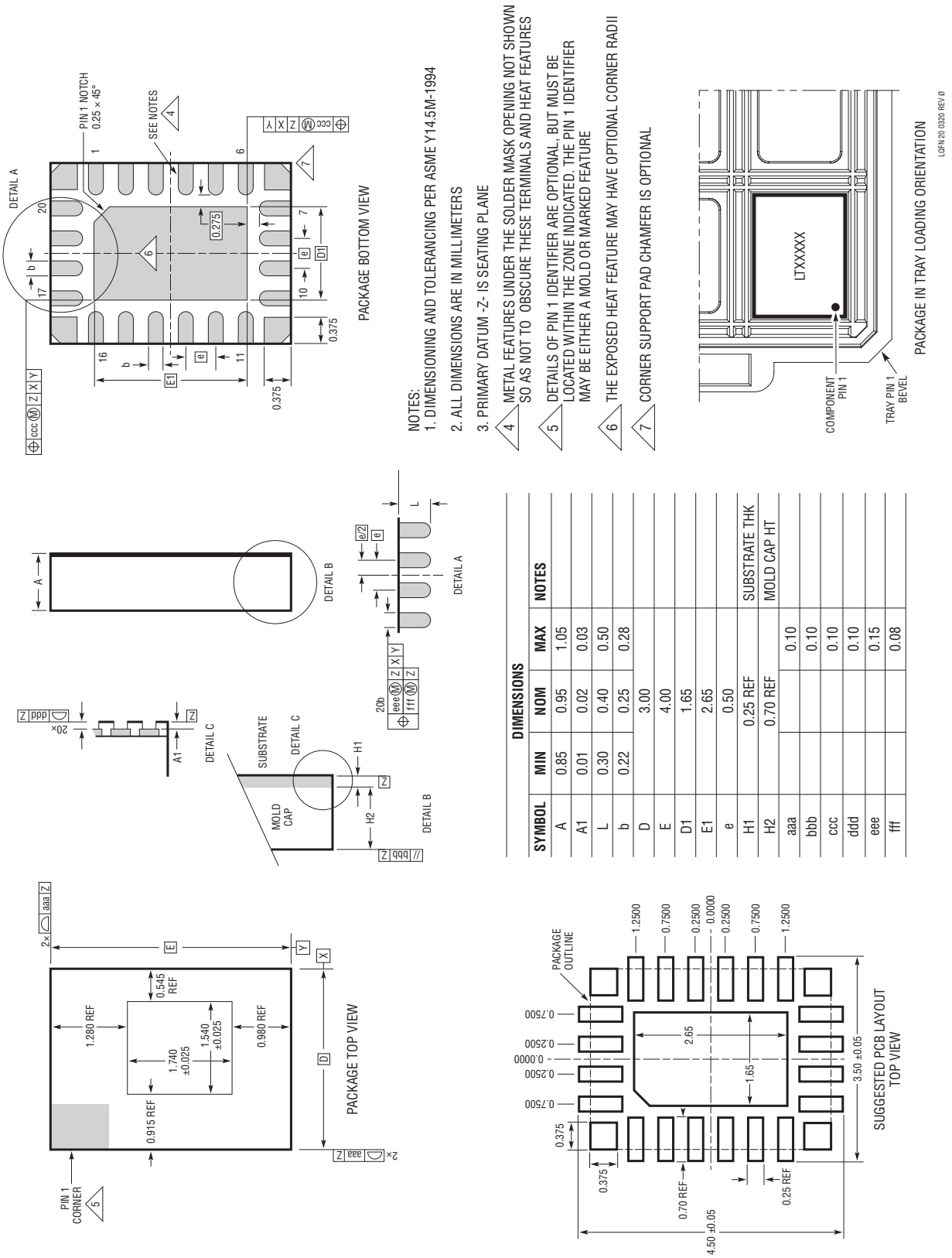
TYPICAL APPLICATIONS

Powering a Transceiver Using 3× LT8625SP/ LT8625SP-1



PACKAGE DESCRIPTION

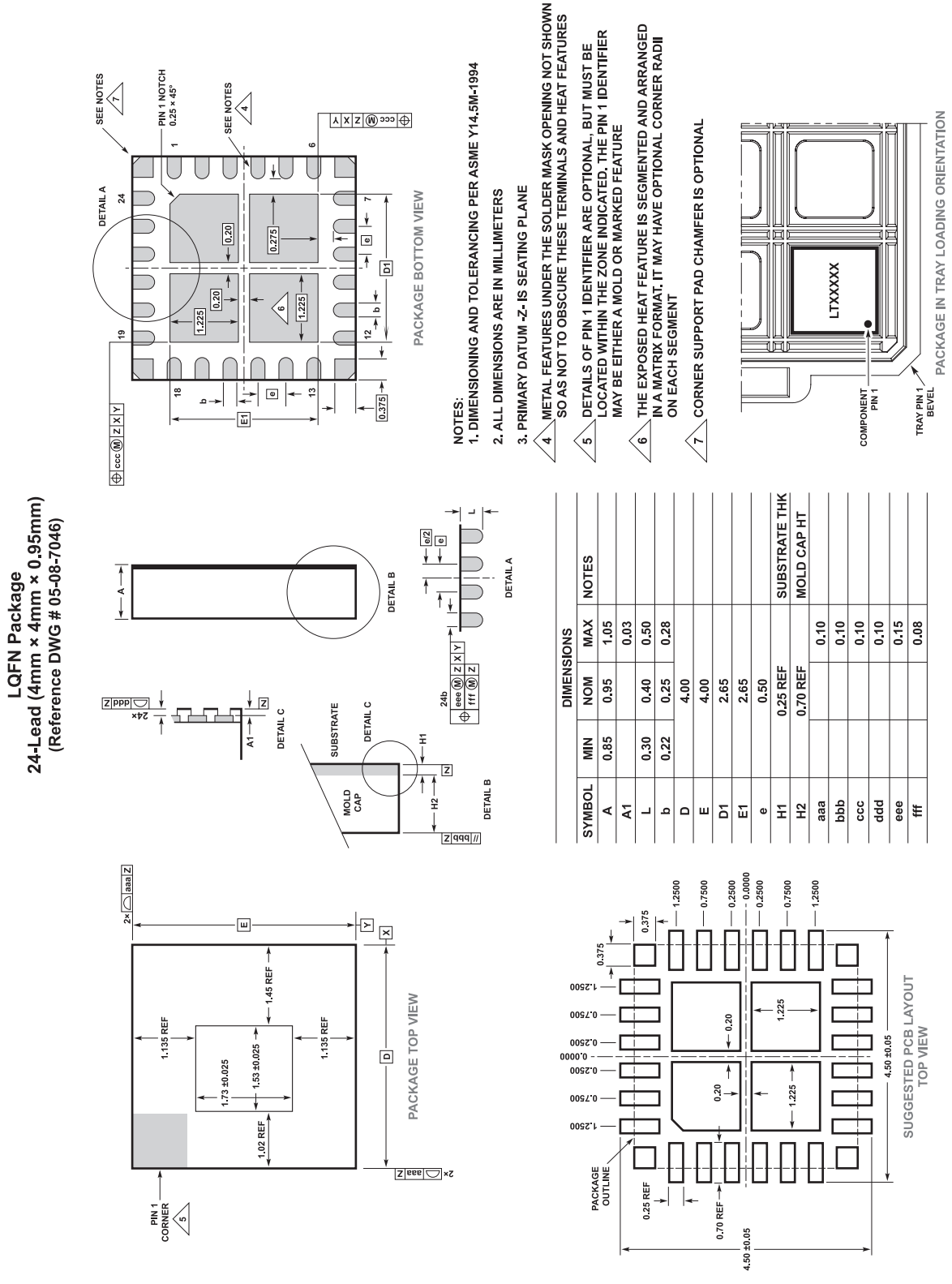
LQFN Package
20-Lead (3mm × 4mm × 0.95mm)
(Reference LTC DWG # 05-08-7038 Rev Ø)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.95	1.05	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		3.00		
E		4.00		
D1		1.65		
E1		2.65		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

PACKAGE DESCRIPTION



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A	0.85	0.95	1.05	
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e		0.50		
H1		0.25 REF		SUBSTRATE THK
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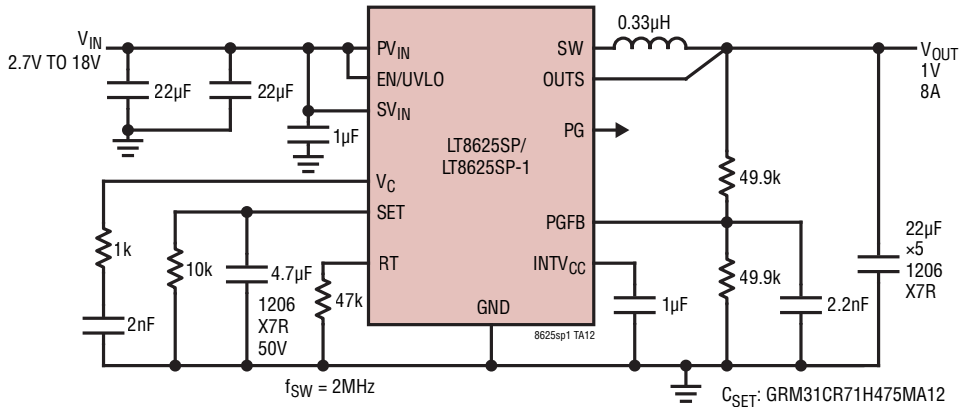
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/22	Updated Features	1
		Updated Package Height	2
		Updated Note 2	4
		Clarified Labels in Typical Performance Characteristics	5, 8
		Updated SET Pin Function description	11
		Updated Figure 4	17
		Updated Forced Continuous Mode information	18
		Updated Equation 2	19
		Clarified SET capacitor sizing information	24
		Updated Equation 12	25
		Updated Table 4	26
		Updated C_{SET} information	28-33, 36
		Updated PGFB Resistor values	33
		Updated Related Parts table	36
B	04/24	Updated Features and Description sections	1
		Updated Pin Configuration	2
		Updated Electrical Characteristics	3
		Updated Typical Performance Curves	5, 8
		Updated Pin Functions	11, 12
		Updated Block Diagram	13
		Updated text for Applications Information	15, 23, 24, 25
		Added Typical Application Circuit	32
		Updated Package Drawing	35
C	07/24	Updated Applications Information	24–29
		Updated Typical Application Circuits	30–35, 39
		Updated Related Parts	39
D	07/25	Updated Absolute Maximum Ratings	2

TYPICAL APPLICATION

1V 8A 2MHz Step-Down Converter with Soft-Start, Fast Start-up and Power Good



PINS NOT USED IN THIS CIRCUIT:
BST, SYNC, PHMODE, CLKOUT

TYPICAL CHARACTERISTIC
2MHz, 1V_{OUT} NOISE DATA USES THIS CIRCUIT

RELATED PARTS

PART	DESCRIPTION	COMMENTS
LT8625S	18V, 8A Synchronous Step-Down Silent Switcher 3 with Ultralow Noise Reference	4µV_{RMS} Noise, V_{IN} = 2.7V to 18V, $V_{OUT(MIN)}$ = 0V, I_Q = 2.8mA, 4mm × 3mm LQFN-20
LT8627SP	18V 16A Synchronous Step-Down Silent Switcher 3 Regulator with Ultralow Noise Reference	4µV_{RMS} Noise, V_{IN} = 2.8V to 18V, $V_{OUT(MIN)}$ = 0V, I_Q = 2.8mA, 4mm x 4mm LQFN-24
LT8642S	18V, 10A Synchronous Step-Down Silent Switcher 2 Regulator	96% Efficiency, V_{IN}: 2.8V to 18V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 240µA, I_{SD} < 1µA, 4mm × 4mm LQFN-24
LTC7151S	20V, 15A Synchronous Step-Down Silent Switcher 2 Regulator	92.5% Efficiency, V_{IN}: 3.1V to 20V, $V_{OUT(MIN)}$ = 0.5V, I_Q = 2mA, I_{SD} < 20µA, 4mm × 5mm LQFN-28
LTC7150S	20V, 20A Synchronous Step-Down Silent Switcher 2 Regulator	92% Efficiency, V_{IN}: 3.1V to 20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} ≤ 40µA, Differential Remote Sense, 6mm × 5mm BGA
LT3042	20V, 200mA, Ultralow Noise Ultrahigh PSRR Linear Regulator	0.8µV_{RMS} Noise and 79dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 350mV Dropout Voltage, Programmable Current Limit and Power Good, 3mm × 3mm DFN and MSOP Packages
LT3045	20V, 500mA, Ultralow Noise Ultrahigh PSRR Linear Regulator	0.8µV_{RMS} Noise and 75dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 260mV Dropout Voltage, 3mm × 3mm DFN and MSOP Packages
LT8650S	42V, Dual 4A, 95% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 6.2µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 6.2µA, I_{SD} < 1µA, 4mm × 6mm QFN-32 Package
LT8652S	18V, Dual 8.5A, 94% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 16µA	V_{IN} = 3V to 18V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 16µA, I_{SD} = 6µA, 4mm s× 7mm LQFN-36 Package
LTC3636	20V, Dual 6A Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 3.1V to 17V, $V_{OUT(MIN)}$ = 0.6V, I_Q < 8µA (Both Channels Enabled), ISD < 1µA, 3mm × 5mm QFN-24 Package
LT8640S/ LT8643S	42V, 6A Synchronous Step-Down Silent Switcher 2 with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 4mm × 4mm LQFN-24
LT8645S/ LT8646S	65V, 8A, Synchronous Step-Down Silent Switcher 2 with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 65V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 6mm × 4mm LQFN-32
LT8609/ LT8609A	42V, 2A, 94% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-10E