Data Sheet

LT8419

100V Half-Bridge GaN Driver with Single-Pin, Three-State PWM Input, Smart Integrated Bootstrap Switch, and Adjustable Dead Time

FEATURES

- Half-Bridge Gate Driver for GaN FETs
- 0.6Ω Driver Pull-Up Resistance
- 0.2Ω Driver Pull-Down Resistance
- 4A Peak Source, 8A Peak Sink Current Capability
- Smart Integrated Bootstrap Switch Prevents BST-SW Voltage Overcharging
- Split-Gate-Driver to Adjust Turn-On/Turn-Off Strength
- Default Low-State for All Driver Outputs
- Single Three-State, TTL Logic-Compatible PWM Input
- ~2ns, ~6ns, and ~10.5ns Programmable Dead Time
- Fast Propagation Delay: 13.5ns (typ)
- Balanced Driver Supply Voltage: $V_{BST} \approx V_{CC}$ = 3.85V - 5.5V
- Undervoltage and Overvoltage Lockout Protections
- Small, 12-Ball WLCSP Package

APPLICATIONS

- High-Frequency DC-DC Switching Power Converters
- Half-Bridge, Full-Bridge, Push-Pull Converters
- Data Center Power Supplies
- Motor Drivers, Class-D Audio Amplifiers
- Consumer, Industrial, and Automotive

GENERAL DESCRIPTION

The LT8419 is a 100V half-bridge GaN driver that integrates top and bottom driver stages, driver logic control, and protections. It can be configured into synchronous half-bridge or full-bridge topologies, as well as buck, boost, and buck-boost topologies. The LT8419 provides strong current sourcing/sinking capability with 0.6Ω pull-up and 0.2Ω pull-down resistances. It also integrates a smart integrated bootstrap switch to generate a balanced bootstrap voltage from V_{CC} with a minimum dropout voltage.

The LT8419 provides split gate drivers to adjust the turn-on and turn-off slew rates of GaN FETs to suppress ringing and optimize EMI performance. Driver PWM input defaults to three-state and driver outputs default to low-state to prevent GaN FETs from false turn-on. The PWM input of LT8419 is TTL logic-compatible and controls two complementary outputs with user adjustable dead time of ~2ns, ~6ns, and ~10.5ns. The LT8419 performs with a fast propagation delay of 13.5ns and maintains excellent delay matching of 1ns between the top and bottom channels, making it suitable for high-frequency DC-DC converters, motor drivers, and class-D audio amplifiers. In addition, the LT8419 employs the WLCSP package to minimize parasitic inductance, enabling its wide use in high-performance and high-power density applications.

TYPICAL APPLICATION

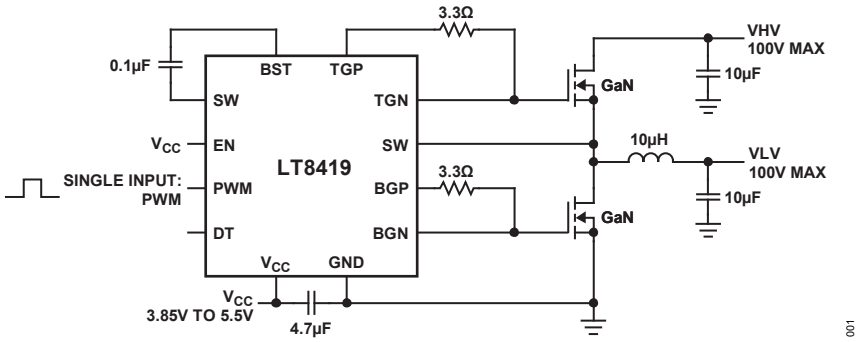


Figure 1. Highly Efficient GaN-Based Switching DC-DC Converter

TABLE OF CONTENTS

REVISION HISTORY

7/26 – Rev. 0

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C[1], V_{CC} = V_{BST} = 5V, V_{GND} = V_{SW} = 0V; TGP and TGN are connected with no load. BGP and BGN are connected with no load, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Supply Voltage and Current						
V_{CC} Operating Voltage Range	V_{CC}		3.85		5.5	V
V_{CC} Shutdown Current	I_{SHDN_VCC}	EN = 0V, PWM = float		45		µA
V_{CC} Quiescent Current	I_{Q_VCC}	EN = 5V, PWM = float		575		µA
V_{CC} Operating Current	I_{VCC}	f_{SW} = 400kHz		2.4		mA
BST Quiescent Current	I_{Q_BST}	EN = 5V, PWM = float		80		µA
BST Operating Current	I_{BST}	f_{SW} = 400kHz		1.0		mA
Undervoltage, Overvoltage Protections						
V_{CC} UVLO Threshold	V_{UVLO_VCC}	Falling	3.14	3.4	3.67	V
V_{CC} UVLO Hysteresis	$V_{UVLO\_HYST\_VCC}$			0.2		V
V_{CC} OVLO Threshold	V_{OVLO_VCC}	Rising	5.58	6.1	6.53	V
V_{CC} OVLO Hysteresis	$V_{OVLO\_HYST\_VCC}$			0.2		V
BST UVLO Threshold	V_{UVLO_BST}	Falling	2.9	3.1	3.35	V
BST UVLO Hysteresis	$V_{UVLO\_HYST\_BST}$			0.25		V
Input Pins (PWM, EN)						
TG Turn-On Input Threshold	$V_{IH(TG)}$	PWM rising	1.7	2.2	2.7	V
TG Turn-Off Input Threshold	$V_{IL(TG)}$	PWM falling	1.5	2.0	2.5	V
TG Turn-Off Hysteresis	V_{HYST_TG}			0.2		V
BG Turn-On Input Threshold	$V_{IH(BG)}$	PWM falling	0.5	1.0	1.5	V
BG Turn-Off Input Threshold	$V_{IL(BG)}$	PWM rising	0.7	1.2	1.7	V
BG Turn-Off Hysteresis	V_{HYST_BG}			0.2		V
PWM Input Three-State Float Voltage	V_{PWM_TRI}		1.36	1.56	1.76	V
TG Turn-Off to PWM Float Voltage	$V_{IL(TG)}$ - V_{PWM_TRI}		0.14			V
PWM Float Voltage to BG Turn-Off	V_{PWM_TRI} - $V_{IL(BG)}$		0.14			V
PWM Internal Pull-Up Resistor	R_{UP_PWM}			4		kΩ
PWM Internal Pull-Down Resistor	R_{DOWN_PWM}			14		kΩ
EN Turn-On Threshold	V_{ENR}	EN rising		2.2		V

(T_A = 25°C[1], V_{CC} = V_{BST} = 5V, V_{GND} = V_{SW} = 0V; TGP and TGN are connected with no load. BGP and BGN are connected with no load, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
EN Turn-Off Threshold	V_{ENF}	EN falling		2.0		V
EN Turn-Off Hysteresis	V_{HYST_EN}			0.2		V
EN Internal Pull-Down Resistor	R_{DOWN_EN}			200		kΩ
Bootstrap Switch						
BST Switch Forward Drop at Low Refresh Current	V_{F_BST}	$I_{VCC-BST}$ = 100µA		1	10	mV
BST Switch Forward Drop at High Refresh Current	V_{F_BST}	$I_{VCC-BST}$ = 100mA		0.4	1	V
BST Switch Dynamic On-Resistance	R_{BST}	$I_{VCC-BST}$ = 100mA		4		Ω
Gate Drivers						
TG Driver R_{ON} Gate Pull-Up Gate Pull-Down	 R_{TG_UP} R_{TG_DW}	$V_{(BST-SW)}$ = 5V		 0.6 0.2		 Ω Ω
BG Driver R_{ON} Gate Pull-Up Gate Pull-Down	 R_{BG_UP} R_{BG_DW}	V_{CC} = 5V		 0.6 0.2		 Ω Ω
TG Rise Time	t_{TGR}	C_L = 1nF, 10% to 90%		3		ns
TG Fall Time	t_{TGF}	C_L = 1nF, 90% to 10%		2		ns
BG Rise Time	t_{BGR}	C_L = 1nF, 10% to 90%		3		ns
BG Fall Time	t_{BGF}	C_L = 1nF, 90% to 10%		2		ns
Propagation Delay, Delay Matching, and Minimum Input Pulse[2]						
EN Turn-On Propagation Delay	$t_{PH(EN)}$	EN rising to BG rising (PWM = low)		250		us
EN Turn-Off Propagation Delay	$t_{PL(EN)}$	EN falling to BG falling (PWM = low)		350		ns
TG Turn-On Propagation Delay	t_{RPD_TG}	PWM rise to TG rise (DT = GND) (TGP = TGN = TG)		13.5	20	ns
TG Turn-Off Propagation Delay	t_{FPD_TG}	PWM fall to TG fall (for all DT)		11	17	ns
BG Turn-On Propagation Delay	t_{RPD_BG}	PWM fall to BG rise (DT = GND) (BGP = BGN = BG)		13.5	20	ns
BG Turn-Off Propagation Delay	t_{FPD_BG}	PWM rise to BG fall (for all DT)		12	18	ns
TG, BG Minimum Input Pulse Width	t_{TGW}, t_{BGW}			14		ns

(T_A = 25°C[1], V_{CC} = V_{BST} = 5V, V_{GND} = V_{SW} = 0V; TGP and TGN are connected with no load. BGP and BGN are connected with no load, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Dead Time (DT)						
BG/TG Low to TG/BG High Propagation Delay (Dead Time)	$t_{PLH(BG)}$	DT = GND, BG off to TG on		1.5		ns
	$t_{PLH(TG)}$	DT = GND, TG off to BG on		2.5		
	$t_{PLH(BG)}$	DT = Float, BG off to TG on		10		
	$t_{PLH(TG)}$	DT = Float, TG off to BG on		11		
	$t_{PLH(BG)}$	DT = V_{CC}, BG off to TG on		5.5		
	$t_{PLH(TG)}$	DT = V_{CC}, TG off to BG on		6.5		
Dead-Time Float Voltage	V_{DT_FLOAT}			2.5		V

1 The LT8419 is tested under pulsed load conditions such that $T_J \approx T_A$. The LT8419 is guaranteed to meet specifications from -40°C to 125°C junction temperature. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \times J_A)$, where θ_{JA} (in °C/W) is the package thermal impedance.

2 The definition of propagation delay for the top or bottom side gate driver and delay matching is illustrated in the following timing diagram.

Timing Diagrams

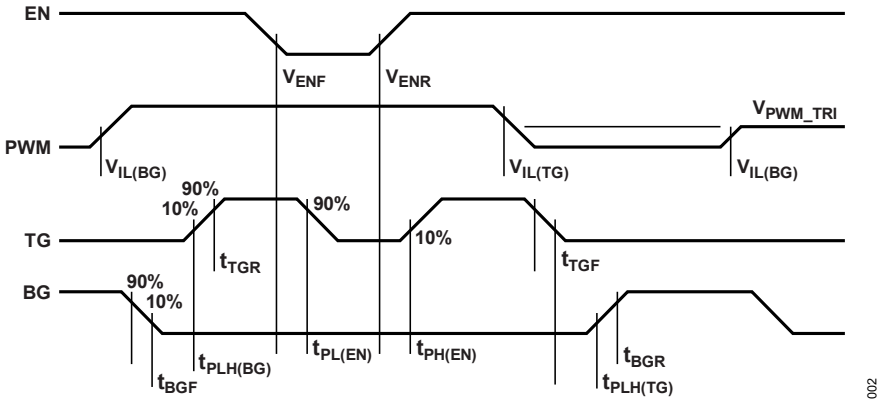


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings[1]

PARAMETER	RATING
EN, PWM	-0.3V to +6V
V_{CC}, (BST – SW), DT	-0.3V to +6V
BGP, BGN	-0.3V to V_{CC} + 0.3V
TGP, TGN	SW - 0.3V to BST + 0.3V
BST	-0.3V to +106V
BST (at 100ms Transient)	-0.3V to +116V
SW	-5V to +100V
SW (at 100ms Transient)	-5V to +110V
Operating Junction Temperature Range[2] [3]	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C

1 Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect device reliability and lifetime.

2 The LT8419 is tested under pulsed load conditions such that $T_J \approx T_A$. The LT8419 is guaranteed to meet specifications from –40°C to 125°C junction temperature. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \bullet J_A)$, where θ_{JA} (in °C/W) is the package thermal impedance.

3 The LT8419 includes overtemperature protection intended to protect the device during momentary overload conditions. The maximum rated junction temperature is exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

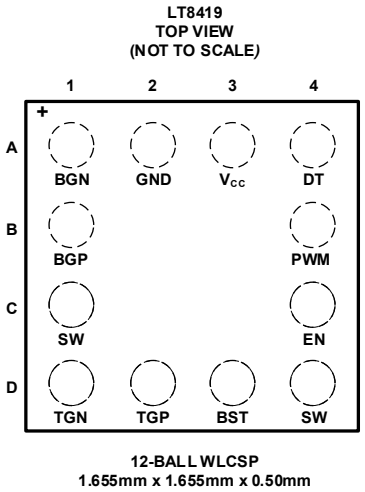
Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Table 3. 12-Ball WLCSP Package Thermal Resistance

Thermal Resistance	
Junction-to-Ambient Θ_{JA}	73 °C/W
Junction-to-Case $\Theta_{JC\ (TOP)}$	0.6 °C/W
Junction-to-Board $\Theta_{JB\ (BOTTOM)}$	12 °C/W

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Package Size: 1.655mm x 1.655mm, Ball Diameter: 0.26mm, Ball Pitch Size: 0.4mm

Figure 3. Pin Diagram

Pin Descriptions

Table 4. Pin Descriptions

PIN	NAME	DESCRIPTION
A1	BGN	Bottom-Side Split Gate Driver Output Pull-Down Branch. Adding a resistor from BGN to the GaN FET's gate can program the turn-off strength of the bottom-side GaN FET.
A2	GND	Ground. Connect this pin to the source of the bottom-side GaN FET with low inductance and resistance.
A3	V_{CC}	Internal Control Circuitry and Gate Driver Power Supply. Locally bypass this pin to ground with a minimum 4.7µF ceramic capacitor.
A4	DT	Dead-Time Programming. Connect this pin to GND, V_{CC}, or leave unconnected. See the Theory of Operation section for details.
B1	BGP	Bottom-Side Split Gate Driver Output Pull-Up Branch. Adding a resistor from BGP to the GaN FET's

PIN	NAME	DESCRIPTION
		gate can program the turn-on strength of the bottom side GaN FET.
B4	PWM	Three-State Gate Driver Input Signal. PWM is TTL input logic compatible. The TG/BG state is determined by the voltage on this pin. If this pin is floating, an internal resistor divider triggers the high-impedance mode in which both BG and TG are turned off. Minimize trace capacitance on this pin as much as possible.
C1, D4[1]	SW	Switch Node. Connect SW to the source of the top synchronous GaN FET and the bottom terminal of the bootstrap capacitor with low inductance and resistance.
C4	EN	Enable. A voltage on this pin above 2.2V enables the gate drivers. The TG and BG pins are both in the low state if this pin is logic-low.
D1	TGN	Top-Side Split Gate Driver Output Pull-Down Branch. Adding a resistor from TGN to the GaN FET's gate can program the turn-off strength of the top-side GaN FET.
D2	TGP	Top-Side Split Gate Driver Output Pull-Up Branch. Adding a resistor from TGP to the GaN FET's gate can program the turn-on strength of the top-side GaN FET.
D3	BST	Bootstrap Floating Driver Supply. The BST pin has an on-die bootstrap switch from V_{CC}. An external bootstrap capacitor on the SW pin can be used to provide a stable and well-balanced bootstrap voltage for the top-side gate driver. Locally bypass this pin to SW with a minimum 100nF ceramic capacitor.

[1] C1 and D4 are internally connected.

BLOCK DIAGRAM

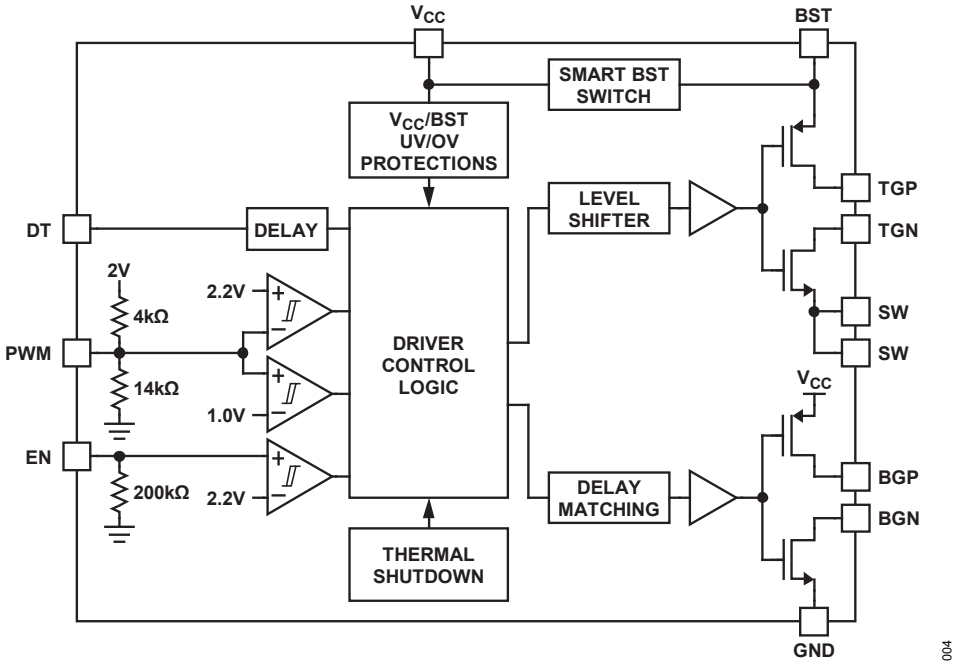


Figure 4. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5. Peak Source Current vs. Driver Output Voltage

Figure 6. Peak Sink Current vs. Driver Output Voltage

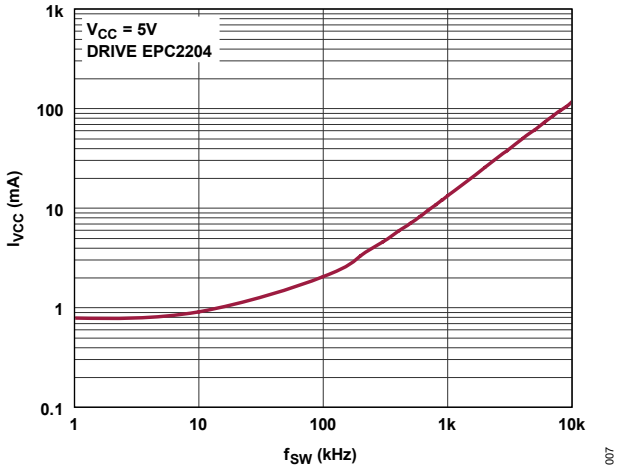


Figure 7. V_{CC} Operating Current vs. Switching Frequency

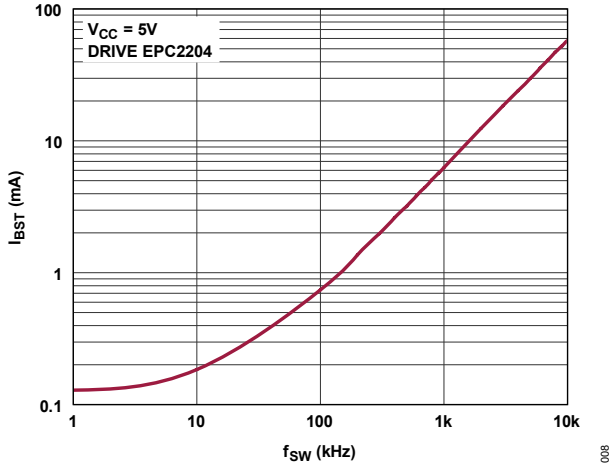


Figure 8. BST Operating Current vs. Switching Frequency

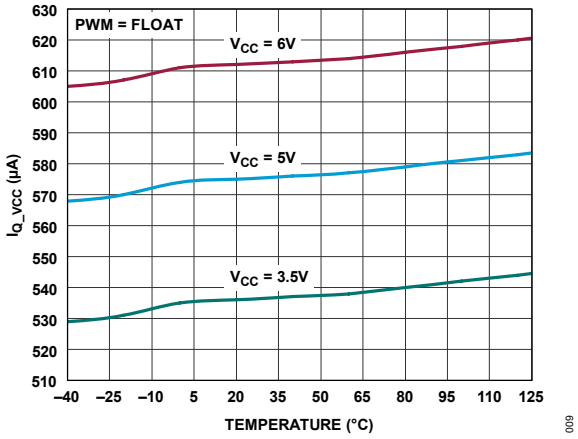


Figure 9. V_{CC} Quiescent Current vs. Temperature

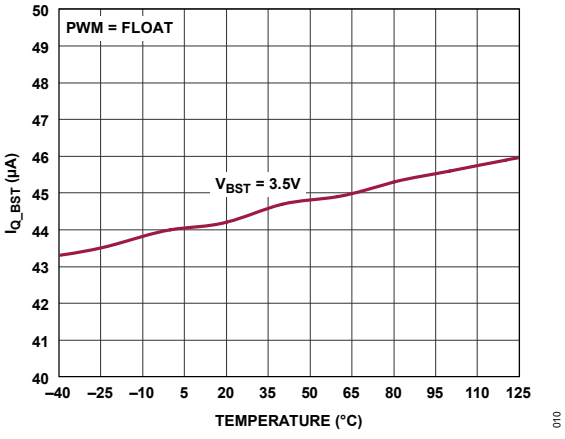


Figure 10. BST Quiescent Current vs. Temperature

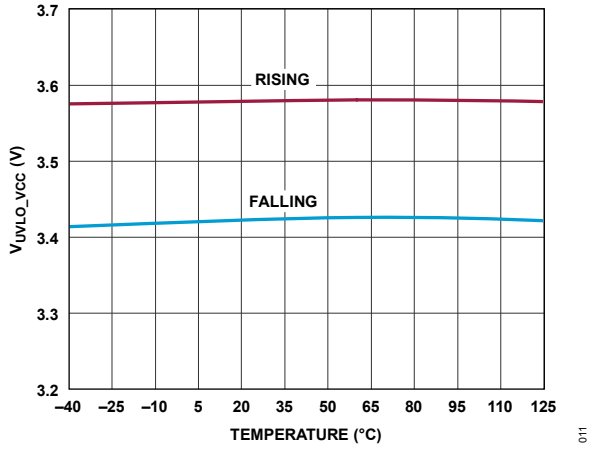


Figure 11. V_{CC} UVLO Threshold vs. Temperature

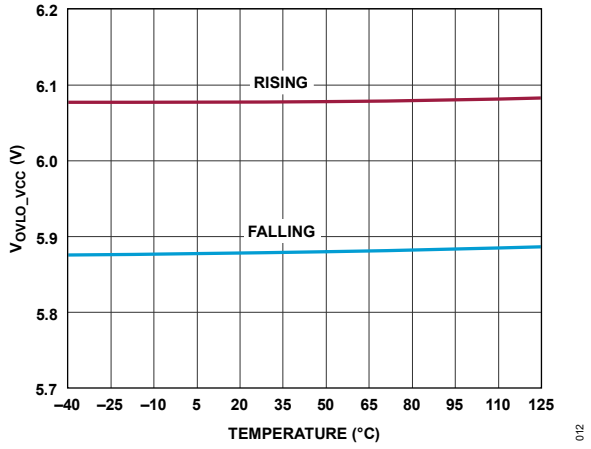


Figure 12. V_{CC} OVLO Threshold vs. Temperature

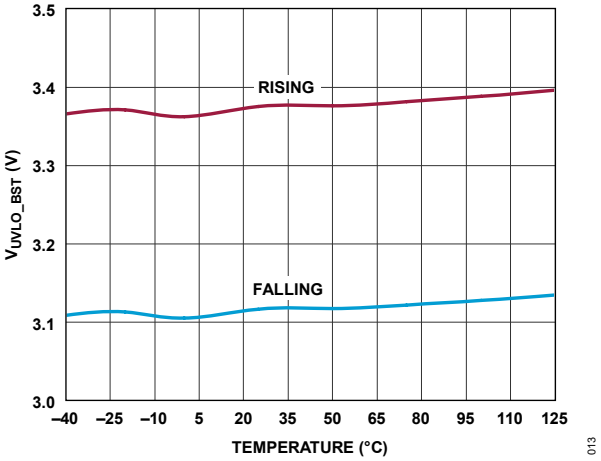


Figure 13. BST UVLO Threshold vs. Temperature

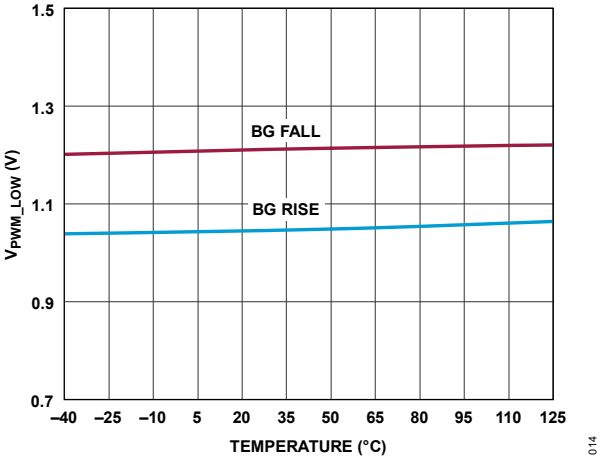


Figure 14. PWM LOW Threshold vs. Temperature

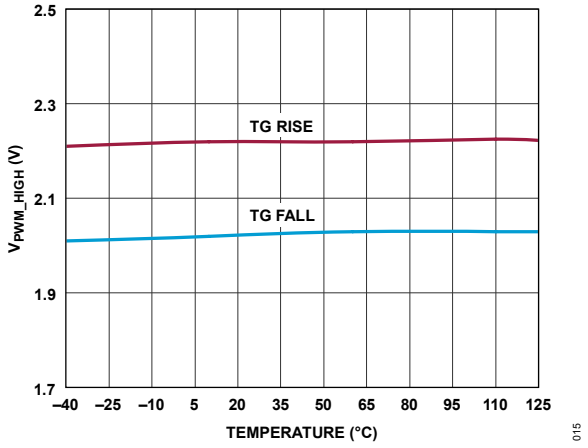


Figure 15. PWM HIGH Threshold vs. Temperature

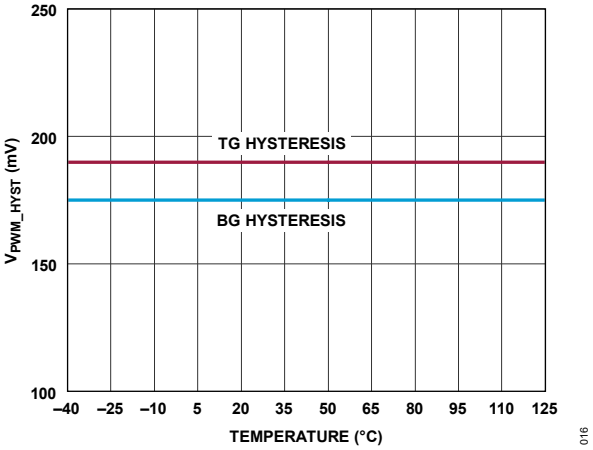


Figure 16. Input Threshold Hysteresis vs. Temperature

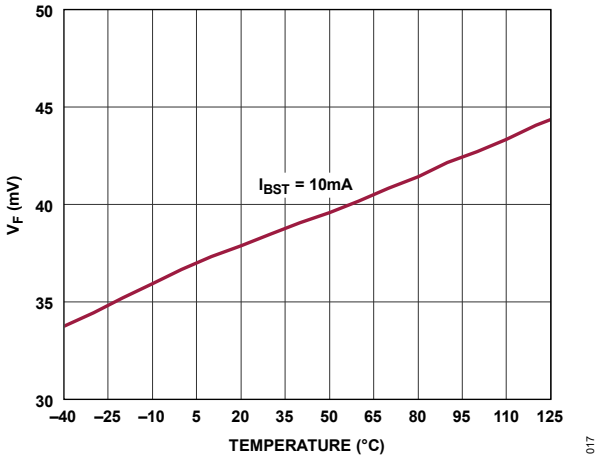


Figure 17. Bootstrap Switch Voltage vs. Temperature

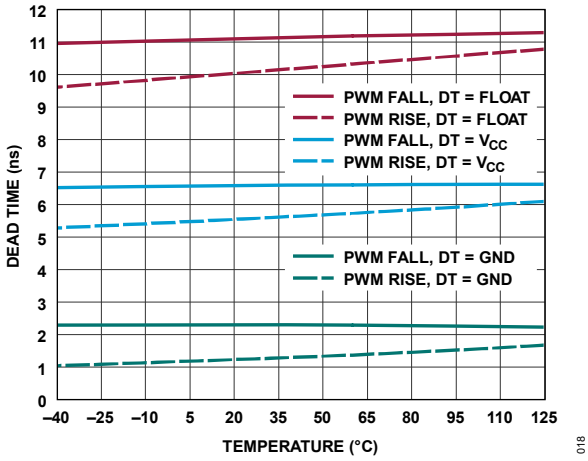


Figure 18. Dead Time vs. Temperature

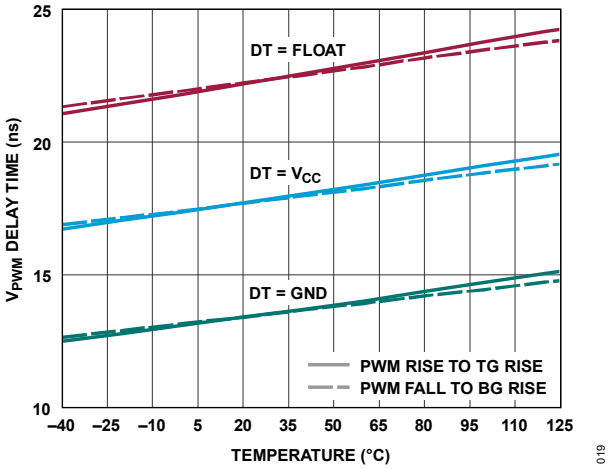


Figure 19. BG/TG Rising Propagation Delay vs. Temperature

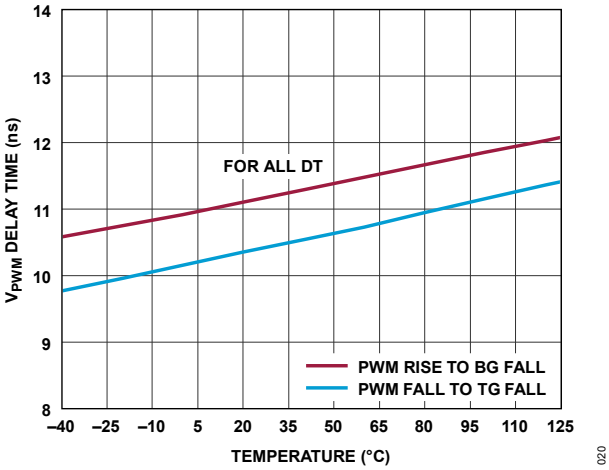


Figure 20. BG/TG Falling Propagation Delay vs. Temperature

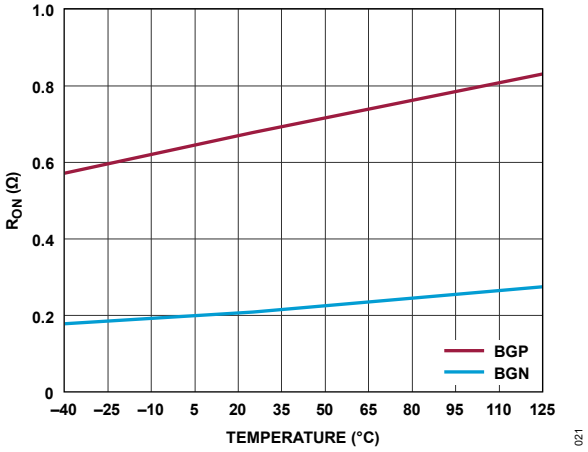


Figure 21. BG On-Resistance vs. Temperature

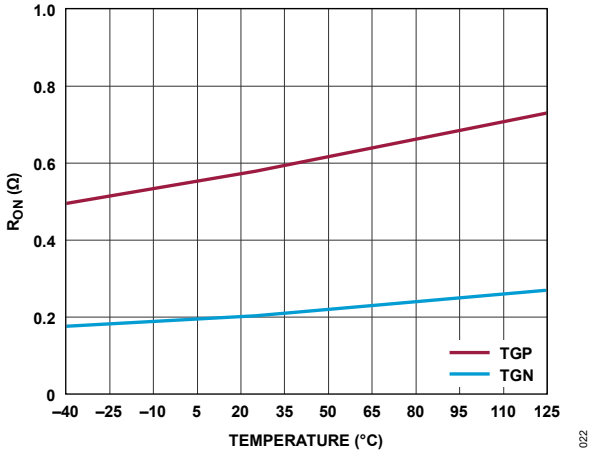


Figure 22. TG On-Resistance vs. Temperature

THEORY OF OPERATION

The LT8419 is a 100V half-bridge GaN driver that integrates top, bottom gate drivers, V_{CC}, BST, UV, and OV protection control logic. It can be used in half bridges and full bridges. It supports multiple topologies including buck, boost, buck-boost, and a variety of applications, including data center power, class-D audio amplifiers, and motor drivers. In addition, the LT8419 employs a small-footprint WLCSP package, which can be used in different applications requiring high-power density, high-frequency operation, small form factor, and low cost.

Chip Startup, V_{CC} UVLO/OVLO Protections

The LT8419 has an undervoltage lockout (UVLO) in the V_{CC} drive power rail. When the V_{CC} voltage falls below the threshold voltage of 3.4V, both the TG and BG pins are turned off to prevent the GaN FETs from being falsely turned on. When the V_{CC} voltage rises above its UVLO threshold of 3.6V (with 200mV hysteresis voltage) and EN is also above 2.2V (with 200mV hysteresis voltage), the LT8419 is activated after a wakeup time. After that, the LT8419 senses PWM, and DT signals and controls TG and BG outputs. Due to the charging time of the BST rail, TG is prohibited from turning on until the BST UV threshold of 3.35V is reached. In addition, to protect the GaN FETs from overdrive voltage and gate damage, V_{CC} OVLO (overvoltage lockout) feature is integrated into the LT8419. When the V_{CC} voltage rises above 6.1V, V_{CC} OV is triggered, which turns off both TG and BG. When the V_{CC} voltage falls below 5.9V, V_{CC} OV is recovered, and TG/BG starts to switch again following the EN, PWM, and DT control signals.

Input Interface PWM, EN

The LT8419 employs a three-state PWM input with fixed transition thresholds. The relationship between the transition thresholds and three input states of the LT8419 is illustrated in *Figure 23*. The PWM input pin of the LT8419 is compatible with TTL logic and can withstand voltages up to 6V. The LT8419 provides a fast propagation delay of 13.5ns and maintains an excellent delay matching of 1ns between top and bottom channels, making it suitable for high-frequency switching operations. When the voltage on PWM is greater than the threshold ($V_{IH(TG)}$), TG is pulled up to BST, which turns on the high-side GaN FET. This GaN FET stays on until the PWM falls below $V_{IL(TG)}$. Similarly, when PWM is less than $V_{IH(BG)}$, BG is pulled up to V_{CC}, which turns on the low-side GaN FET. BG stays high until PWM increases above the threshold $V_{IL(BG)}$. The hysteresis between the corresponding V_{IH} and V_{IL} voltage levels eliminates false triggering due to the noise during switch transitions. However, take care to keep noise from coupling into the PWM pin, particularly in high-frequency, high-voltage applications. The thresholds are positioned to allow for a region in which both BG and TG are low. An internal resistor divider sets the PWM pin voltage into this region if the signal driving the PWM pin goes into a high-impedance state. The EN pin can also be used to keep both BG and TG low if the high-impedance state is not available from the PWM driving signal. Driving the EN pin low keeps both TG and BG off, and driving the EN pin high enables TG and BG switching based on the PWM input. There is an internal 200kΩ pull-down resistor from the EN pin to GND to keep the EN default state low if its input is not driven.

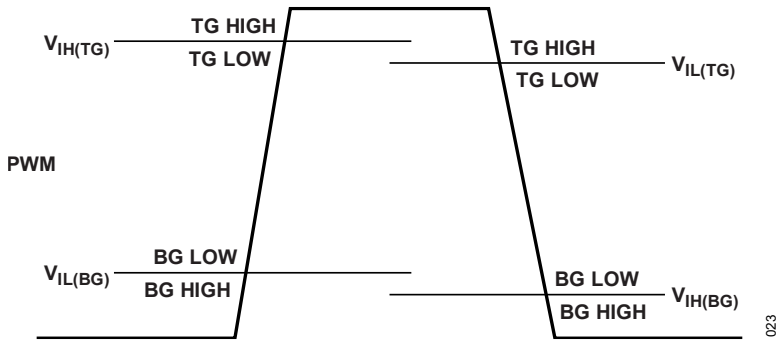


Figure 23. Three-State PWM Operation

Programmable Dead Time

The LT8419 offers three programmable dead-time settings during BG/TG low to TG/BG high transition (dead time). Dead-time settings are latched with V_{CC} high and EN high. With DT = GND, the minimum dead-time setting is ~2ns. With DT = V_{CC}, the dead-time setting is nominally ~6ns. The maximum dead-time setting is ~10.5ns, with DT = FLOAT. The dead-time float voltage is 2.5V. Dead time is reset at V_{CC} power-up or by toggling the EN pin. Not all dead-time settings are appropriate with all loads.

Smart Bootstrap (BST) Switch and BST UVLO

During the dead-time interval between TG turn-off to BG turn-on, or between BG turn-off to TG turn-on, the GaN power switch demonstrates a high reverse conduction voltage of 2V ~ 3V from source to drain (even higher at high conduction current), which can bring SW node down to -2V ~ -3V and leads to the overcharge of the BST rail and permanent gate damage of the GaN power switch. In the LT8419, the smart BST switch comprises power switches that are controllable for BST charging or blocking. When the bottom switch is turned on and the switching node voltage is close to ground level, the BST switch is turned on to start charging the BST capacitor. In this way, the LT8419 can generate a well-balanced bootstrap voltage from V_{CC} with a minimum dropout voltage, which prevents GaN FETs from overcharge and gate damage. The LT8419 provides a bootstrap UVLO protection to prevent GaN FETs from turning on at an insufficient gate drive voltage. When the BST-SW rail falls below 3.1V, TG stops to turn on until the BST capacitor is replenished and the BST rail rises above 3.35V (250mV hysteresis), and TG starts to switch again.

Split Gate Driver

The LT8419 also provides split gate drivers for both top and bottom power switches. Thus, turn-on and turn-off slew rates of the top and bottom gate drivers are adjustable independently by connecting different values of gate resistors at the TGP, TGN, BGP, and BGN pins. Additionally, the LT8419 integrates strong gate drivers with 0.6Ω pull-up resistance, 0.2Ω pull-down resistance, a strong 4A current sourcing, and 8A current sinking capability, which can drive a variety of GaN FETs with different Q_G or $R_{DS(ON)}$ values. Driver outputs TGP and TGN have a default 500kΩ pull-down resistance to the SW node; BGP and BGN have a default 500kΩ pull-down resistance to ground to prevent top and bottom GaN FETs from false turn-on.

APPLICATIONS INFORMATION

Figure 1 shows a typical LT8419 application circuit. The following sections serve as guidelines for selecting external components for typical applications.

Selecting the V_{CC} and BST Capacitor

The LT8419 supports a wide range of switching frequencies. Thus, the V_{CC} and BST capacitors must be selected properly based on the system switching frequency and the Q_G of GaN FETs.

The bypass capacitor, C_{VCC}, provides the gate charge for the top-side and bottom-side GaN FETs. The charge to turn on the external GaN FET is referred as gate charge, Q_G, and is typically specified in the external GaN FET data sheet. Gate charge depends on the gate drive level and external GaN FET, which ranges from 1nC to tens of nC. The required bypass capacitance can be approximated as:

$$C_{VCC} > \frac{Q_{GT} + Q_{GB}}{\Delta V} \quad (1)$$

where:

Q_{GT} and Q_{GB} are the gate charge of the top-side and bottom-side GaN FETs, respectively.

ΔV is the maximum allowable voltage drop across C_{VCC}.

An external boost capacitor, C_{BST}, connected between BST and SW, supplies the gate driver voltage for the TG top driver. To turn on the external GaN FET, the driver places the CBST voltage across the gate and source of the GaN FET. The C_{BST} capacitance must have at least ten times the gate capacitance to fully turn on the external GaN FET. For most applications, a capacitor value of 0.1µF for C_{BST} is sufficient. However, if multiple GaN FETs are paralleled and driven by the LT8419, the C_{BST} capacitance must be increased correspondingly and maintained in the following relationship:

$$C_{BST} > \frac{10Q_{GT,TOTAL}}{1V} \quad (2)$$

A smart BST switch is integrated into the LT8419 to keep charging the C_{BST} to eliminate the requirement of the external V_{CC}-to-BST Schottky diode. An additional diode from V_{CC} to BST may overcharge the BST rail and damage the high-side GaN FET gate. When the BG/TG is low, the total current from V_{CC} is typically 575µA; when the BG/TG is switching at 400kHz with no load at driver outputs, the total current from V_{CC} is typically 2.4mA.

Selecting the Gate Resistance

The LT8419 provides split gate drivers for top and bottom GaN power switches. A gate resistor up to 10Ω can be added to TGP/TGN and BGP/BGN pins to adjust the turn-on/turn-off rate of two GaN FETs for electromagnetic interference (EMI) and efficiency optimization.

Power Dissipation

The major power dissipation on the LT8419 is the sum of the power loss on the gate driver and the BST switch. The gate driver loss is caused by charging and discharging the gate capacitance of the GaN FETs. Because the gate loss occurs once per cycle, it is proportional to the switching frequency. Unlike a pure capacitive load, a power GaN FET's gate capacitance seen by the driver output varies with its V_{GS} voltage level (V_{CC} in this case) during switching. For simplicity, the gate power dissipation can be calculated using its gate charge Q_G. For identical GaN FETs on BG and TG, the gate loss is:

$$P_{gate} = 2Q_G \times V_{CC} \times f_{sw} \quad (3)$$

The reverse recovery loss and forward bias power loss on the traditional bootstrap diode are avoided by using the integrated BST switch. The BST switch loss is dominated by the conduction loss on its $R_{DS(ON)}$ while charging the capacitor. Larger GaN FET gate capacitance requires more current to charge the BST capacitor, resulting in more loss:

$$P_{BST} \approx (Q_{TG} \times f_{SW})^2 \times R_{DS(ON),BST}/D_{BG} \quad (4)$$

where:

$R_{DS(ON),BST}$ is the on-resistance of the BST switch, and D_{BG} is the duty cycle of bottom gate.

PCB Bypass and Grounding Guideline

The LT8419 requires proper bypassing on the V_{CC} and BST-SW supplies due to its high-speed switching (nanoseconds) and large AC currents. Careless component placement and PCB routing may cause excessive ringing and undershoots/overshoots.

To obtain optimum performance from the LT8419:

- Mount the capacitors as close as possible between the V_{CC} and GND pins as well as the BST and SW pins. Shorten the traces as much as possible to reduce lead inductance.
- Use a low-inductance, low-impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LT8419 can sink up to 8A peak currents, and any significant ground drop degrades signal integrity.
- Plan the power/ground routing carefully. Know where the large load switching current is originating and going. Maintain separate ground return paths for the input pin and output power stage.
- Kelvin connect the TG pin to the top GaN FET gate and SW pin to the top GaN FET source. Kelvin connect the BG pin to the bottom GaN FET gate and the driver ground to the bottom GaN FET source. Keep the copper trace between the driver output pin and load short and wide.
- Refer to the EVAL-LT8419-AZ PCB layout as an example.

Soldering Guideline

Precondition the solder pad with flux for better solder flow. Because of the small solder balls, type 4 solder paste (20 microns to 38 microns grain size) or finer solder paste is recommended to apply on the pad. After placing the IC manually, use a telescope to ensure a good alignment. For better accuracy, it is recommended to use automated fine-pitch placement machines with vision alignment. Melt the solder paste using a hot plate instead of a heat gun to prevent the IC from being blown away. To verify good connections, vision and X-ray inspections are recommended. Failure to make good electrical or thermal contact between the balls and the copper board causes driver or system malfunction or higher thermal resistance.

PACKAGE OUTLINE DIMENSIONS

12-Ball Wafer Level Chip Scale Package (WLCSP)
(CB-12-17, Unit: millimeter)

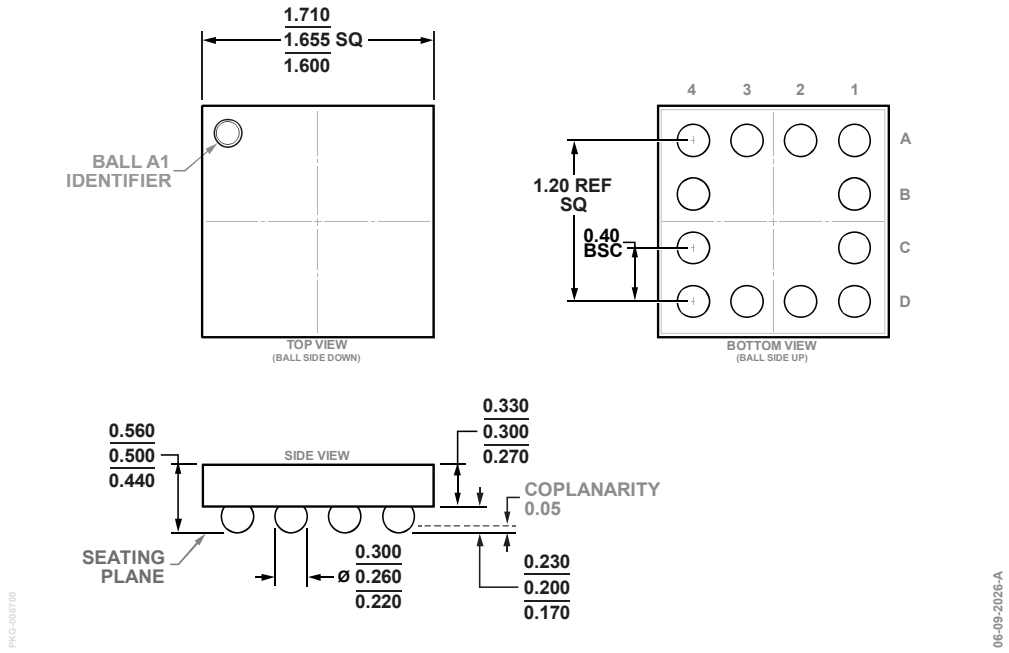


Figure 24. Package Drawing

BUMP DIAMETER (mm)	PAD DIAMETER (mm)	MASK DIAMETER (mm)
0.260 ± 0.04	0.200 ± 0.015	0.300 ± 0.015

Table 5. Recommended Pad Dimensions (from AN-617)

TYPICAL APPLICATIONS

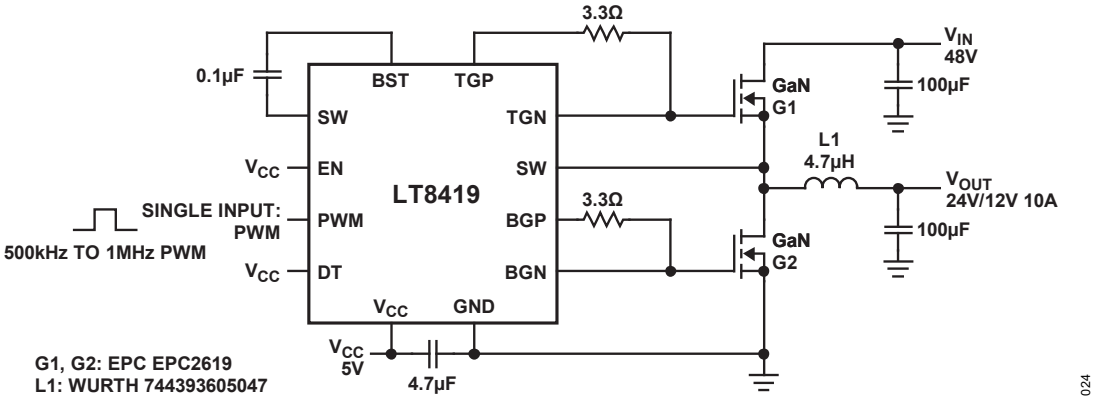


Figure 25. 48V Input, 24V/12V and 10A Output, 500kHz to 1MHz Buck Converter

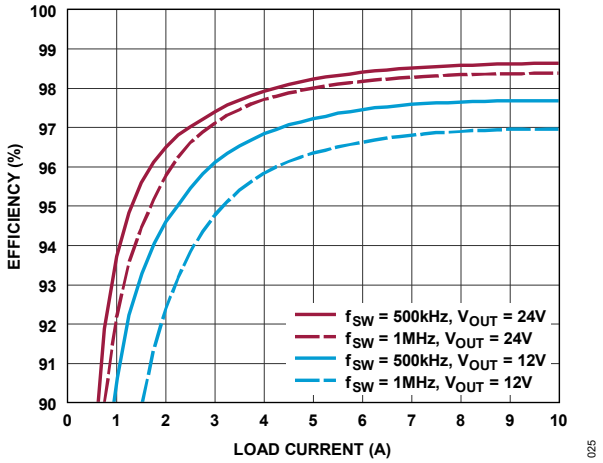


Figure 26. Efficiency vs. Load Current (with Forced Air)

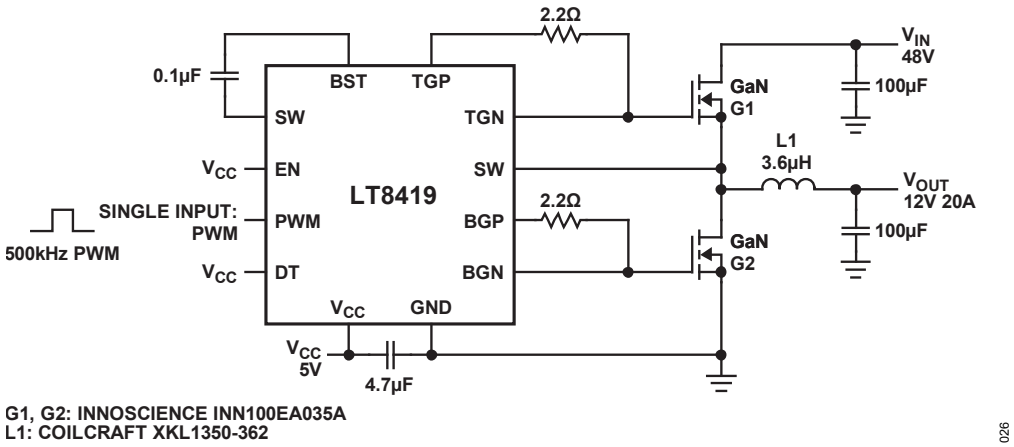


Figure 27. 48V Input, 12V 20A Output, 500kHz Buck Converter

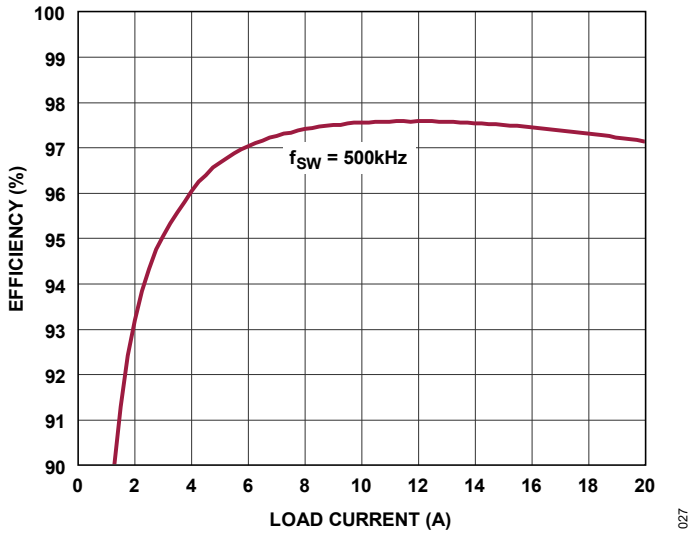


Figure 28. Efficiency vs. Load Current (with Forced Air)

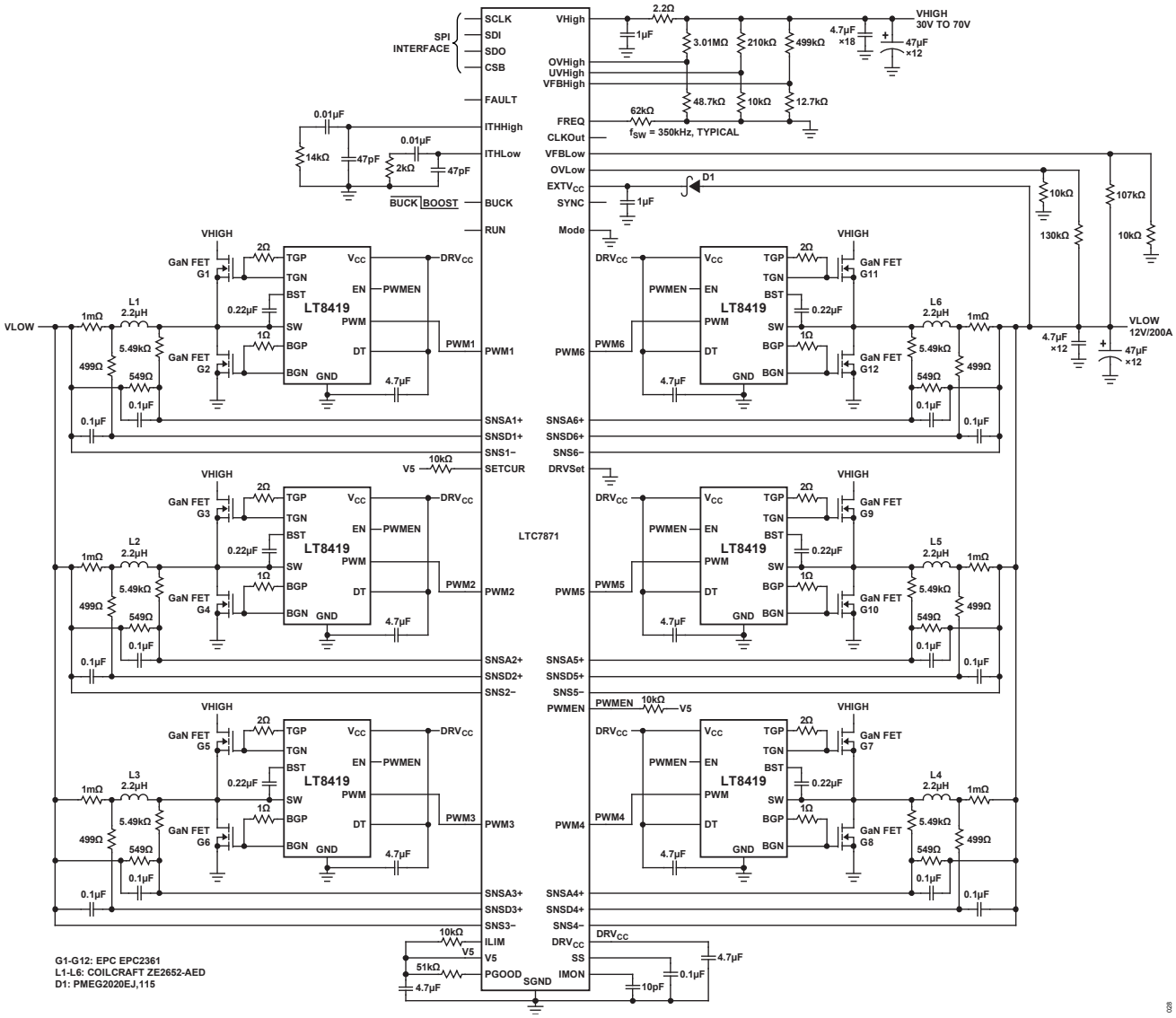


Figure 29. High Efficiency 6-Phase, 12V 200A Bidirectional Supply

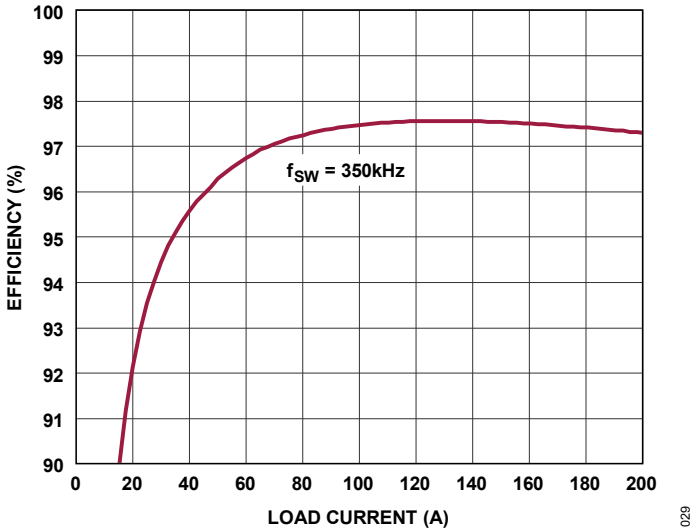


Figure 30. Efficiency vs. Load Current (with Forced Air)

ORDERING GUIDE

Table 6. Ordering Guide

TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8419ACBZ-R7	8419	12-Ball WLCSP	-40°C to 125°C

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8418	100V Half-Bridge GaN Driver with Smart Integrated Bootstrap Switch	Up to 100V supply voltage, 3.85V ≤ V_{CC} ≤ 5.5V.
LTC7060	100V Half-Bridge Driver with Floating Grounds and Adjustable Dead Time	Up to 100V supply rail, 6V ≤ V_{CC} ≤ 14V, programmable dead-time control, three-state PWM input with enable pin.
LTC4449	High-Speed Synchronous N-Channel MOSFET Driver	Up to 38V supply voltage, 4V ≤ V_{CC} ≤ 6.5V, 3.2A peak pull-up, 4.5A peak pull-down.
LTC4446	High Voltage Synchronous N-Channel MOSFET Driver without Shoot-Through Protection	Up to 100V supply voltage, 7.2V ≤ V_{CC} ≤ 13.5V, 2.5A/3A peak pull-up, 1.2Ω/0.55Ω peak pull-down.
LTC4444	High Voltage Synchronous N-Channel MOSFET Driver with Shoot-Through Protection	Up to 100V supply voltage, 7.2V ≤ V_{CC} ≤ 13.5V, 2.5A/3A peak pull-up, 1.2Ω/0.55Ω peak pull-down.