Fully Integrated 17V/8A Switched Capacitor 2:1 Converter Configurable as a Voltage Divider, Doubler, or Inverter

FEATURES

- **Wide VHIGH/VLOW Voltage Range from 0V/0V to 17V/8.5V with a Startup Voltage of 3.45V**
- **Maximum Output Current 8A as a Voltage Divider**
- **Low Quiescent Current of 4µA at Shutdown**
- **Over 97% Peak Efficiency**
- **Standalone Voltage Divider (2:1), Doubler (1:2), Inverter (1:-1) Conversion**
- **Soft Startup into Steady-State Operation**
- Inrush Current Limit and Overcurrent Protection
- Parallel Operation for Higher Output Power
- Integrated Bootstrap Diodes
- Available in a 3mm x 3mm LFCSP Package

APPLICATIONS

- Battery System Applications
- Portable Consumer Electronics
- Industrial Applications

GENERAL DESCRIPTION

The **LT®7826** is a fully integrated monolithic DC-to-DC converter. It achieves very high efficiency with a switched capacitor architecture in applications with an input-to-output voltage ratio of 2:1 (divider), 1:2 (doubler), or 1:1 (inverter). The LT7826 can handle a maximum voltage of 17V and provide a maximum output current of 8A, with fault protection. It features integrated bootstrap diodes and provides a compact and cost-effective solution for battery applications requiring current limit protection. The LT7826 operates at a fixed 500kHz switching frequency, while synchronization is available through the MODE pin for frequency tuning and interleave operation. The part is available in a 3mm x 3mm LFCSP package.

TYPICAL APPLICATION

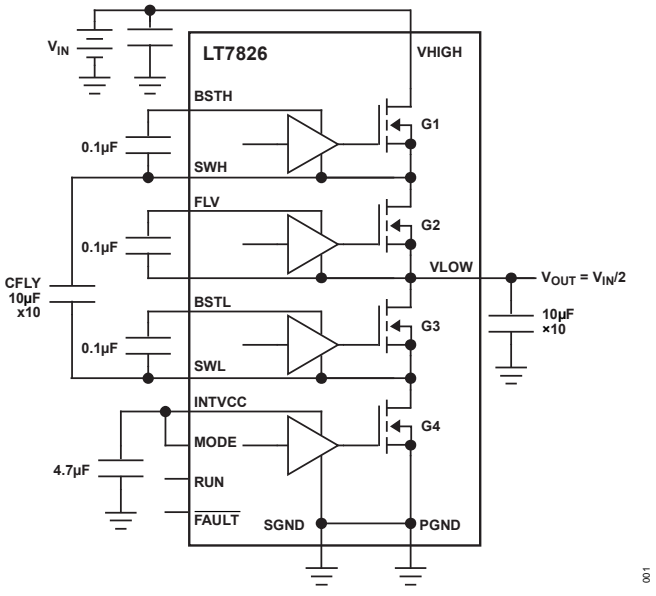

Figure 1. High-Efficiency 2:1 Voltage Divider

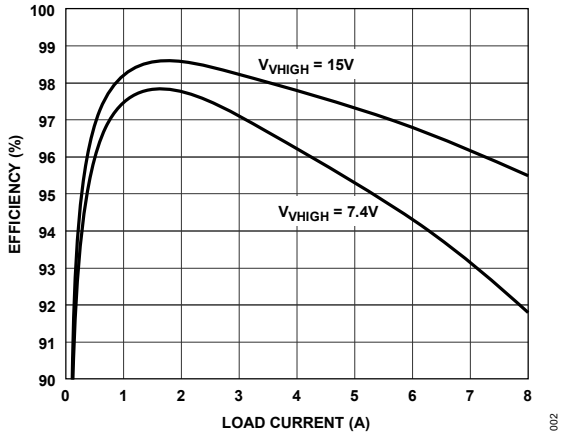

Figure 2. Efficiency vs. Load Current 2:1 Voltage Divider

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	6/25	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C, V_{VHIGH} = 8V, V_{RUN} = 4V, V_{MODE} = 4V, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
VHIGH Voltage Range	V_{VHIGH}			0		17	V
VLOW Voltage Range	V_{VLOW}			0		8.5	V
VHIGH Supply Current	I_Q	V_{RUN} = 0V			4		µA
Undervoltage Lockout Threshold	V_{UVLO}	V_{INTVCC} Falling V_{INTVCC} Rising			3.15 3.45		V
On-Resistance from VHIGH to SWH	R_{ON1}				15		mΩ
On-Resistance from SWH to VLOW, and from VLOW to SWL	$R_{ON2,3}$				10		mΩ
On-Resistance from SWL to PGND	R_{ON4}				12		mΩ
RUN Pin ON Threshold	V_{RUN}	V_{RUN} rising	-40°C ≤ T_J ≤ 125°C	1.1	1.2	1.35	V
RUN Pin ON Hysteresis	V_{RUN_hys}				45		mV
RUN Pin Pull-Up Current	I_{RUN}	V_{RUN} = 0V			0.55		µA
V_{CC} LDO Voltage No Load	V_{INTVCC}				4		V
Standby Mode Threshold	V_{MODE}	V_{MODE} Falling V_{MODE} Rising			1 1.2		V
PWM Frequency for Synchronization	f_{SYNC}			100			kHz
PWM Amplitude for Synchronization	V_{SYNC}			2.6			V
MODE Pin Pull-low Impedance	R_{MODE}	V_{MODE} = 2.6V			1.6		MΩ
MODE Pin Max Pull-Low current	I_{MODE_MAX}	V_{MODE} = 4V			1.86		µA
Switching frequency in Full-Power Switching Mode	f_S				500		kHz
$\overline{FAULT}$ Open-Drain Pull-Down Resistance	$R_{\overline{FAULT}}$				330		Ω

(T_A = 25°C, V_{VHIGH} = 8V, V_{RUN} = 4V, V_{MODE} = 4V, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
$\overline{FAULT}$ Leakage Current	$I_{\overline{FAULT}\_LEAK}$	V_{RUN} = 0V $V_{\overline{FAULT}} = 17V$				1	µA
VLOW Fault Threshold, Upper	$V_{VLOW\_FAULT\_UP}$	V_{MODE} = 4V V_{VLOW} Rising			$\frac{V_{VHIGH}}{2}$ + 0.32		V
VLOW Fault Threshold, Lower	$V_{VLOW\_FAULT\_LOW}$	V_{MODE} = 4V V_{VLOW} Falling			$\frac{V_{VHIGH}}{2}$ - 0.32		V

1 Junction temperature (T_J) is calculated from the Ambient temperature (T_A) and Power dissipation (PD) according to the following formula: $T_J = T_A + (P_D \times \theta_{JA})$

2 All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
VHIGH, VLOW	-0.3V to 18V
(BSTH-SWH), (BSTL-SWL)	-0.3V to 5V
(FLV, VLOW)	-0.3V to 5V
INTVCC, RUN	-0.3V to 5V
MODE	-0.3V to 12V
$\overline{\text{FAULT}}$	-0.3V to 18V
Operating Junction Temperature Range	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C

[1] All voltages are referenced to SGND unless otherwise specified.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to Printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Electrostatic Discharge (ESD)

ESD Caution

Electrostatic discharge (ESD) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

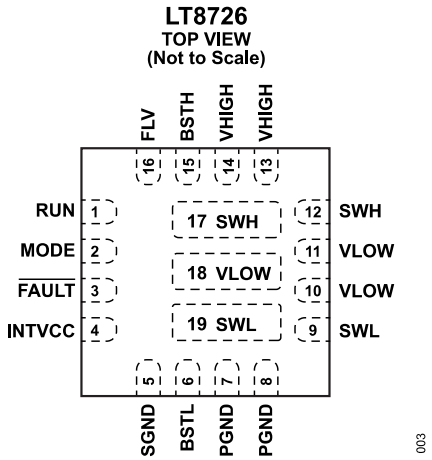


Figure 3. Pin Configuration

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	RUN	Digital control input with internal 0.55µA pull-up current. Forcing the RUN pin voltage below 1.155V shuts down the circuit. When the RUN pin voltage exceeds 1.2V, internal circuitry starts up, including a low-dropout regulator for INTVCC.
2	MODE	Logic input signal with internal 1.6MΩ pull-low resistance. MODE pin voltage higher than 1.2V enables the switched capacitor operation. MODE voltage lower than 1V activates standby mode, which is similar to shutdown mode but with INTVCC voltage ready at 4V. The MODE pin can also be utilized for synchronization. Applying an external clock signal with a frequency higher than 100kHz and an amplitude larger than 2.6V would cause the switching frequency to synchronize to this clock with inverted phase, i.e., the SWL waveform would be antiphase to the clock at the MODE pin.
3	$\overline{\text{FAULT}}$	Open drain output for fault indication. $\overline{\text{FAULT}}$ is pulled to SGND when the VLOW voltage is out of the window of ± 320mV, around half of VHIGH voltage, or during other fault conditions, including UVLO and over temperature.
4	INTVCC	Output of the internal linear low dropout regulator. The internal control and driver circuits are powered by this voltage source. Must be decoupled to power ground with a minimum of 1µF ceramic or other low Equivalent series resistance (ESR) capacitor. Do not use the INTVCC pin to supply power to any other IC.
5	SGND	Signal Ground. All small-signal components should connect to this ground. Connect this pin with PGND pins on the PCB.
6, 15	BSTL, BSTH	Bootstrapped Supplies to the floating drivers. Bootstrapped capacitors are connected from BSTL to SWL, and from BSTH to SWH.
7, 8	PGND	Power Ground.
9	SWL	Low-side switching node. Connected to one terminal of flying capacitors.

10, 11	VLOW	Switched capacitor converter low-side voltage pin. Connect low-side capacitors from VLOW to PGND.
12	SWH	High-side switching node. Connected to the other terminal of flying capacitors.
13, 14	VHIGH	Switched capacitor converter high-side voltage pin. Connect high-side capacitors from VHIGH to PGND.
16	FLV	Floating bias voltage for the internal driver circuit. A 0.1µF~1µF ceramic capacitor or other low ESR capacitor is required from this pin to the VLOW pin.
17	SWH	Exposed pad is internally connected to SWH (Pin 12).
18	VLOW	Exposed pad is internally connected to VLOW (Pins 10, 11).
19	SWL	Exposed pad is internally connected to SWL (Pin 9).

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4. Shutdown Current vs. Input Voltage

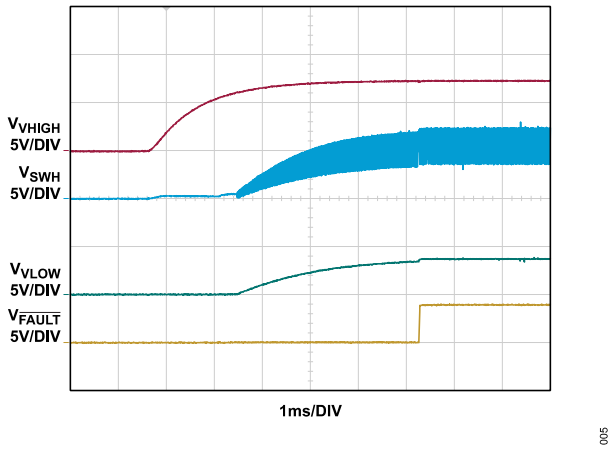


Figure 5. Soft Start-up for 7.4V to 3.7V Voltage Divider (See Typical Application)

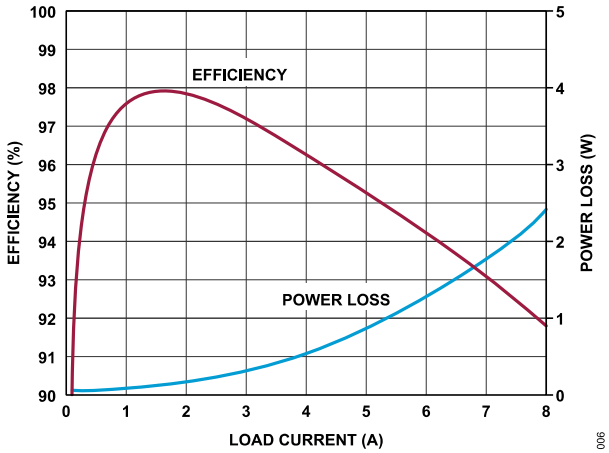


Figure 6. Efficiency and Power Loss vs. Load Current for 7.4V to 3.7V Voltage Divider (See Typical Application)

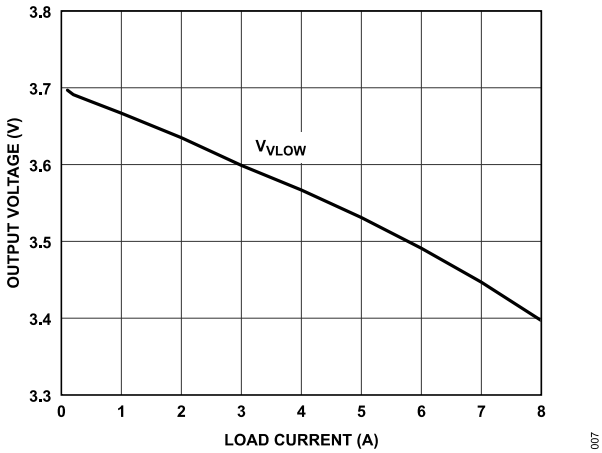


Figure 7. Output Voltage Load Regulation for 7.4V to 3.7V Voltage Divider (See Typical Application)

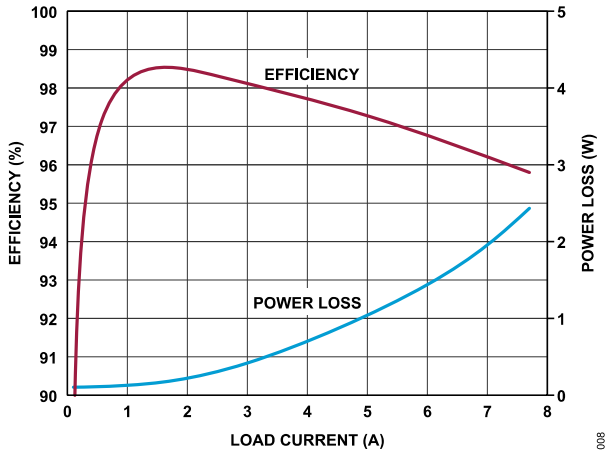


Figure 8. Efficiency and Power Loss vs. Load Current for 15V to 7.5V Voltage Divider (See Typical Application)

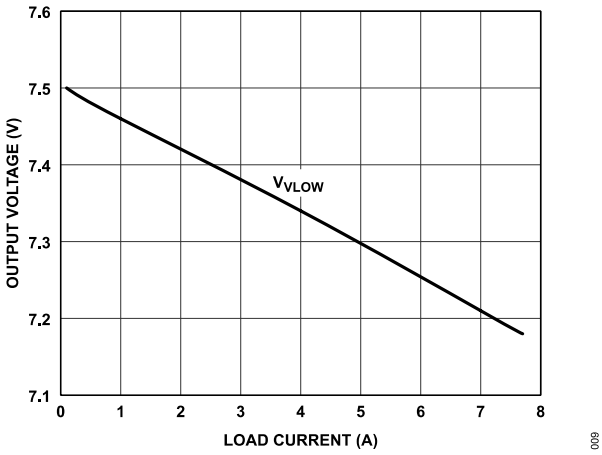


Figure 9. Output Voltage Load Regulation for 15V to 7.5V Voltage Divider (See Typical Application)

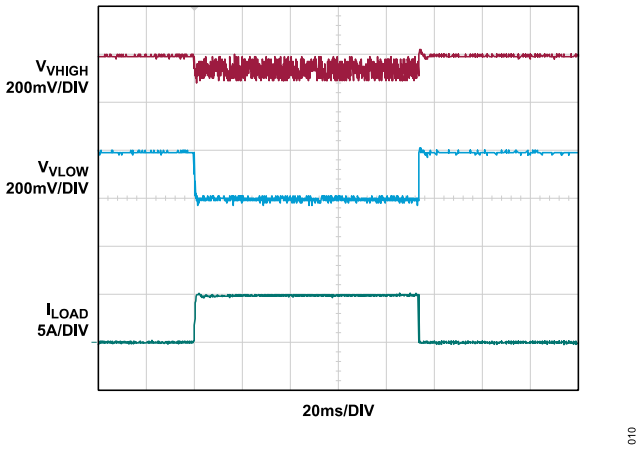


Figure 10. Load Transient 0A~5A~0A for 7.4V to 3.7V Voltage Divider (See Typical Application)

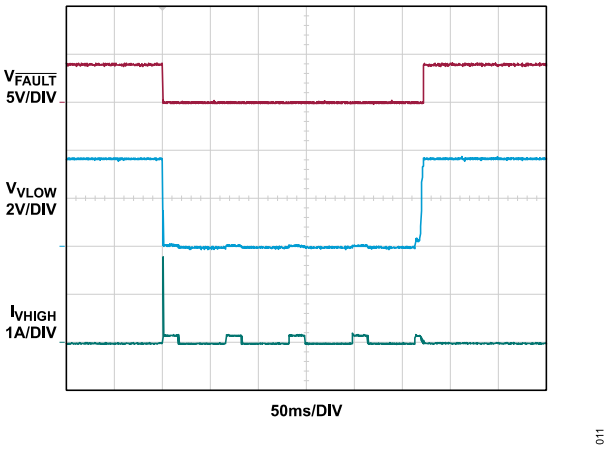


Figure 11. Output Short Circuit and Recovery for 7.4V to 3.7V Voltage Divider (See Typical Application)

BLOCK DIAGRAM

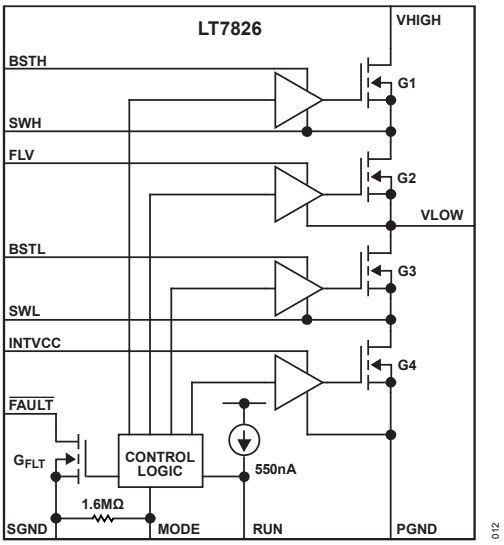


Figure 12. LT7826 Block Diagram

THEORY OF OPERATION

The LT7826 is a constant-frequency, open-loop switched capacitor/charge pump converter for high-power and high-voltage applications. In steady-state operation, the internal switches are turned on and off to force the flying capacitor between SWH and SWL, either parallel or serial, with the capacitor at VLOW. When the flying capacitor and VLOW capacitor are paralleled, the voltages on these capacitors are the same. When the flying capacitor and VLOW capacitor are serial to VHIGH, the voltage on the flying capacitor plus the voltage on the VLOW capacitor equals the voltage on VHIGH. With this switched cap operation, the VLOW pin voltage remains close to half of the VHIGH voltage in the steady state, and it is not sensitive to variable loads due to very low output impedance at a high switching frequency. The LT7826 does not regulate the output voltage with a closed-loop feedback system. However, it stops switching when fault conditions occur, such as a VLOW pin shorted to GND, an overcurrent event, and overtemperature protection.

Start-Up and Shutdown (RUN)

The LT7826 is in shutdown mode when the RUN pin is pulled down. In shutdown mode, most internal circuits are turned off, including the INTVCC regulator, and the entire LT7826 consumes less than 4µA current. Releasing the RUN pin allows an internal 0.55µA current to pull up this pin and enable the INTVCC regulator when the RUN pin voltage exceeds 1.2V. Alternately, the RUN pin can be externally pulled up or driven directly by a logic. Do not exceed the absolute maximum rating of 6V on this pin.

INTVCC Power and UVLO

INTVCC is generated by an internal low dropout (LDO) and regulated to 4V for internal and gate-drive circuitry. It is powered from VLOW when V_{VLOW} is higher than 3.8V; otherwise, it is powered from VHIGH. When V_{INTVCC} rises above its UVLO threshold of 3.45V, LT7826 is ready for switching operation. When V_{INTVCC} decreases below 3.15V, LT7826 stops switching. A ceramic or other low-ESR capacitor with a capacitance of 1µF or up should be connected between INTVCC and the ground, and placed close to these pins.

MODE Pin and Standby Mode

With RUN pin voltage above 1.2V and INTVCC voltage above its UVLO threshold, LT7826 is ready for switching. However, switching will not start until the MODE pin voltage is higher than 1.2V. The MODE pin is pulled low with an internal 1.6MΩ resistor, which makes LT7826 default to not switching (standby) after power up. Connect the MODE pin to INTVCC or VHIGH to enable the LT7826 switching operation after power-up. The MODE pin can handle a maximum voltage of 12V.

The MODE pin can also be used for synchronization. It responds to a clock signal with a frequency between 100kHz and 1MHz and an amplitude higher than 2.6V, which will be adopted as the switching frequency for full power operation. Phase inverting is also included in the design, causing SWL to run antiphase to the clock at the MODE pin. With this synchronization and phase inversion, interleave operation can be achieved when multiple LT7826s are connected in parallel.

Pre-balance

With RUN pin voltage above 1.2V, INTVCC voltage above its UVLO threshold, and MODE pin voltage above 1.2V, the LT7826 starts up and monitors the VHIGH and VLOW voltage continuously. To avoid surge current through the circuit, LT7826 enters a pre-balance mode if V_{VLOW} is lower than $V_{VHIGH}/2$ – 265mV or higher than $V_{VHIGH}/2$ + 265mV. In pre-balance mode, the maximum internal power FET current is 485mA, and the switching frequency is 250kHz. When V_{VLOW} is within the window of $V_{VHIGH}/2$ ± 265mV, LT7826 exits pre-balance mode and starts full power switching.

A function of enable/disable cycling over switching is included in the pre-balance mode operation in LT7826. With this function, the pre-balance switching continues for 16.4ms to charge up the flying and output capacitors. If V_{VLOW} is still not close enough to $V_{VHIGH}/2$ to activate full-power switching, LT7826 pauses switching for 49.1ms until its next switching enabled interval. This enables/disables cycling to continue as long as needed, averting over temperature if the flying or output capacitors are large, or if power pins are shorted to ground.

Over Current Protection

During steady-state operation, VLOW voltage drops linearly as load current increases. The overcurrent protection is implemented by monitoring the voltage difference between V_{VLOW} and $V_{VHIGH}/2$. When the difference exceeds 320mV, the LT7826 exits full power switching and reduces the maximum power Field-effect transistor (FET) current to 485mA. When overcurrent condition is removed and V_{VLOW} returns to within the window of V_{VHIGH} ± 265mV, LT7826 enters full power switching again. The function of enable/disable cycling over switching is also applied during overcurrent condition, as shown by the waveforms in *Figure 11*.

$\overline{\text{FAULT}}$ Pin and Fault Response

The $\overline{\text{FAULT}}$ pin is used for fault indication in LT7826, and is implemented with an open-drain structure. When LT7826 enters full power switching, the $\overline{\text{FAULT}}$ pin is released and may be pulled up externally to indicate the readiness of output. The $\overline{\text{FAULT}}$ pin would be pulled low in other situations, such as pre-balance mode, overcurrent, or overtemperature conditions. The overtemperature threshold in LT7826 is 175°C, above which all the switching stops. The die temperature must be lower than 165°C to re-start switching in LT7826.

APPLICATIONS INFORMATION

The *Typical Application* is an LT7826 voltage divider circuit. The converter can convert VHIGH voltage to VLOW voltage with a 2:1 step-down ratio and supply 8A load current in the steady state operation. In pre-balance or overcurrent conditions, the converter automatically limits the maximum power switch current to 485mA for thermal protection.

Pre-balance Mode with Reduced Loading Capacity

To avoid surge current through the circuit, after power up, LT7826 would enter a pre-balance mode if V_{VLOW} is lower than $V_{VHIGH}/2$ - 0.265V or higher than $V_{VHIGH}/2$ + 0.265V. In pre-balance mode, the maximum current through the internal power switch is limited to 485mA, and LT7826 would switch at a frequency of 250kHz, or half of the default frequency of full-power switching. The flying capacitor and output capacitor would be gradually charged up by pre-balance mode operation. As V_{VLOW} gets close to $V_{VHIGH}/2$, the charging current would further reduce due to the lower overdrive voltage over the power switch inside LT7826. When V_{VLOW} is within the window of $V_{VHIGH}/2 \pm 265mV$, LT7826 would exist in pre-balance mode and start full-power switching.

Because of the reduced current capability during pre-balance mode, the loading current should be less than 30mA in pre-balance mode to ensure that V_{VLOW} can get close enough to $V_{VHIGH}/2$ to activate full-power switching.

Effective Open-Loop Output Resistance And Load Regulation

LT7826 does not regulate the output voltage through feedback closed loop system. The VLOW voltage is very close to half the VHIGH voltage in steady-state operation. As the load current increases, the output voltage decreases. The output resistance is very low, depending on the switching frequency and the capacitance of CFLY and CLOW. In many applications, multi-layer ceramic capacitors (MLCC) are selected as flying capacitors. The voltage coefficients of MLCC capacitors strongly depend on the type and size of capacitors. Normally, larger-size X7R MLCC capacitors are better than X5R in terms of voltage coefficient. The MLCCs still drop 20% to 30% capacitance with high DC bias voltage. Capacitance derating needs to be considered when estimating the output resistance of the switched capacitor circuits.

Input/Output Capacitor and Flying Capacitor Selection

In switched capacitor applications, large AC currents flow through the flying capacitors and input/output capacitors. Low ESR ceramic capacitors are highly recommended for these applications. Ensure the maximum RMS capacitor current is within the spec, or higher-rated capacitors are preferred. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose capacitors rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. The LTspice® simulation tool can be used to quantify the root mean square (RMS) current.

Generally, the higher the capacitance of the flying capacitor, the lower the flying capacitor voltage ripple, and the higher power efficiency the switched capacitor converter can achieve. In a voltage divider application, flying capacitor voltage ripple can be estimated with the following equation:

$$V_{CFLY\_RIPPLE} = \frac{I_{OUT}}{2 \times f_{SW} \times C_{FLY}}$$

Selecting the flying capacitor so that the ripple voltage is around 100mV at the full load condition is a good start.

The input capacitor's RMS current is approximately half of the load current. The input capacitor must be selected to accommodate the maximum load conditions.

The output capacitor would largely impact the output voltage ripple at the switching frequency. The higher the capacitance at the output port, the smaller voltage ripples the output would contain.

Voltage Doubler Applications

The LT7826 may be used as a voltage doubler, with VLOW as the input and VHIGH as the output. After power up LT7826 doubler would enter pre-balance mode to gradually charge up the flying capacitor and output capacitor. When V_{VHIGH} is higher than $2V_{VLOW}$ - 530mV, the circuit would exist pre-balance mode and start full-power switching. Over current protection would be triggered when V_{VHIGH} is lower than $2V_{VLOW}$ - 640mV, and the power switch current would be limited to 485mA or less. The maximum output current a single LT7826 doubler can provide is 4A.

Voltage Inverter Applications

The LT7826 may be used as a voltage inverter, with the input source V_{IN} connected between VHIGH and VLOW, and PGND as the system output referred to VLOW as system ground. After power up LT7826 inverter would enter pre-balance mode to gradually charge up the flying capacitor and output capacitor. When system output is within the window of $-V_{IN} \pm 265mV$, the circuit would exist pre-balance mode and start full-power switching. Overcurrent protection would be triggered when system output is out of the window of $-V_{IN} \pm 320mV$, and the power switch current would be limited to 485mA or less. The maximum output current a single LT7826 inverter can provide is 4A.

Interleave Operation in Parallel Applications

Multiple LT7826 converters can be connected in parallel in high-power applications. The synchronization function with the MODE pin can be utilized to achieve interleave operation, as shown in *Figure 13*. The parallel connection of LT7826s with interleave operation can also be implemented in doubler or inverter applications.

PCB Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC:

1. Is the exposed pad SWH/VLOW/SWL solidly connected to the corresponding pins on the PCB?
2. Are all the capacitors CFLY/CHIGH/CLOW close to the IC? The PCB trace to those capacitors should be wide enough to handle large load currents.
3. Is the INTVCC bypassing capacitor connected close to the IC, between the INTVCC and the ground plane?
4. Are the bootstrap capacitors connected close to the IC, between the BSTH and SWH, and the BSTL and SWL?
5. Are the PCB traces to VHIGH/VLOW/PGND wide enough to handle large load currents?
6. In the cases of a multilayer board, are there enough thermal vias on the VHIGH/VLOW/PGND plane?

For more information, refer to the **Evaluation board design** for the PCB layout examples.

TYPICAL APPLICATIONS

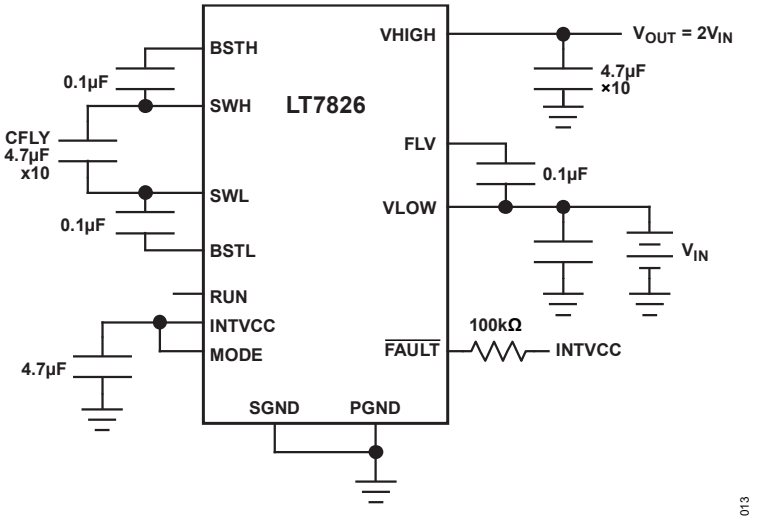


Figure 13. High-Efficiency 3.5V (V_{IN}) to 7V (V_{OUT}), 4A Voltage Doubler

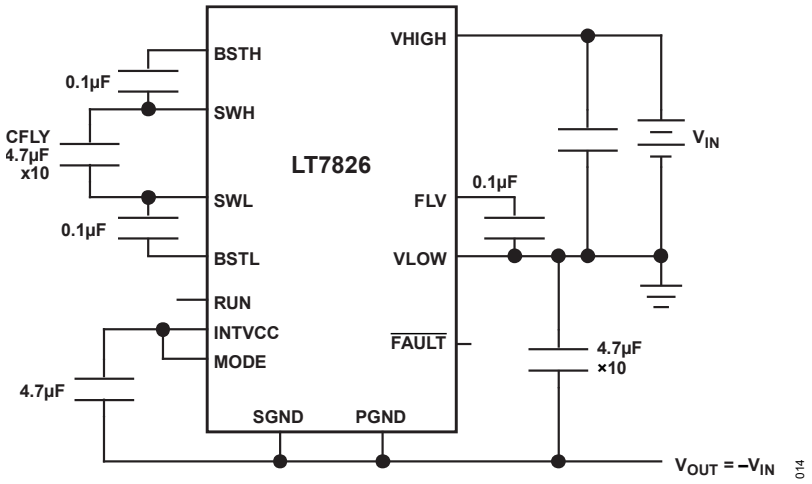


Figure 14. High-Efficiency 4V (V_{IN}) to -4V (V_{OUT}), 4A Voltage Inverter

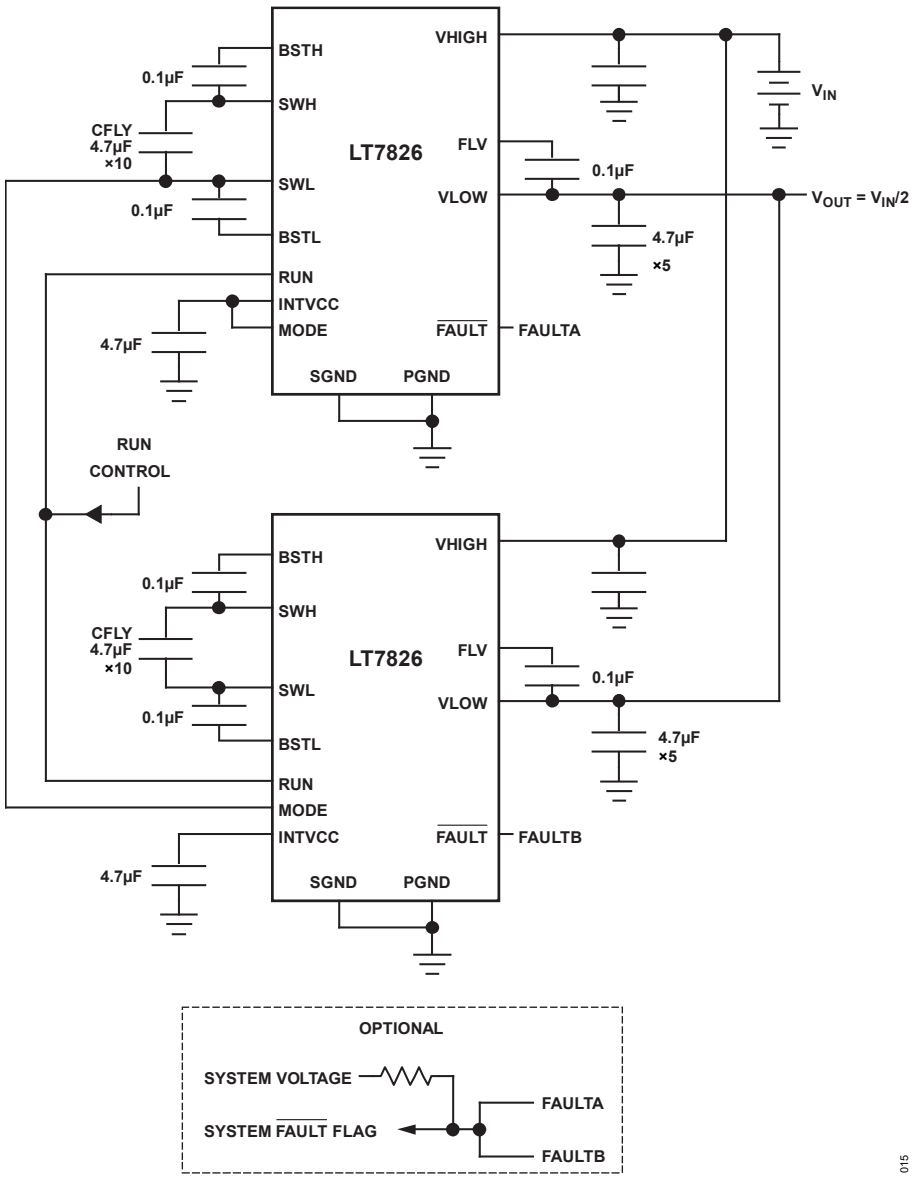
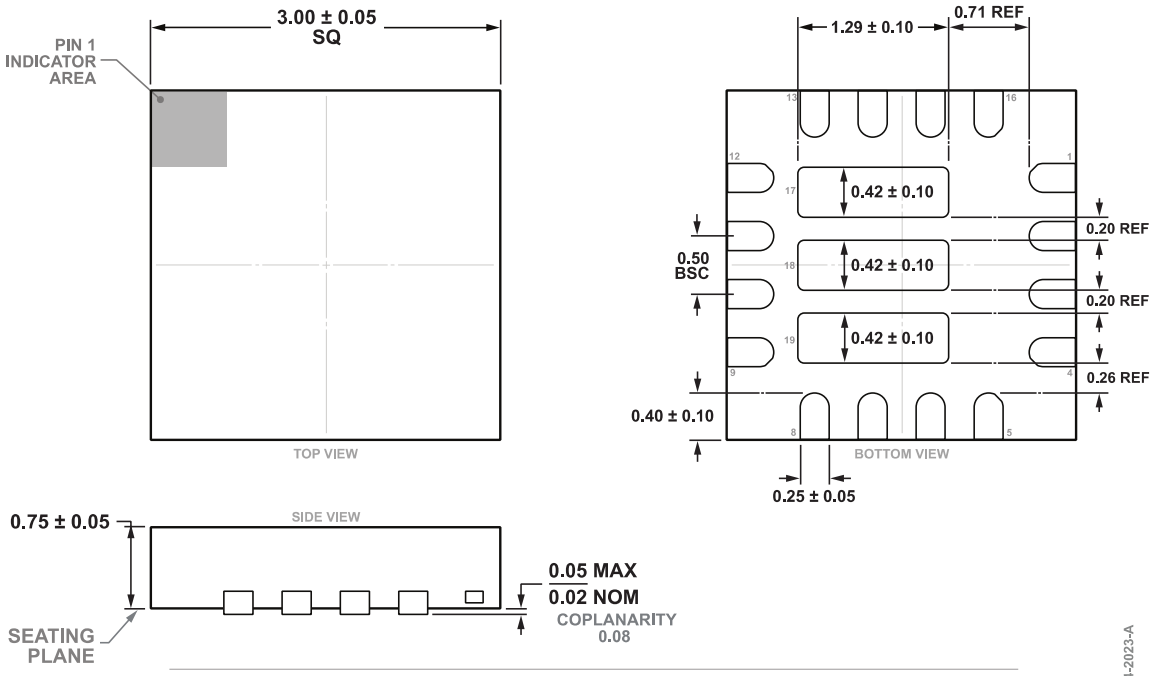


Figure 15. High-Efficiency 7.4V (V_{IN}) to 3.7V (V_{OUT}), 16A Voltage Divider with Interleave Operation

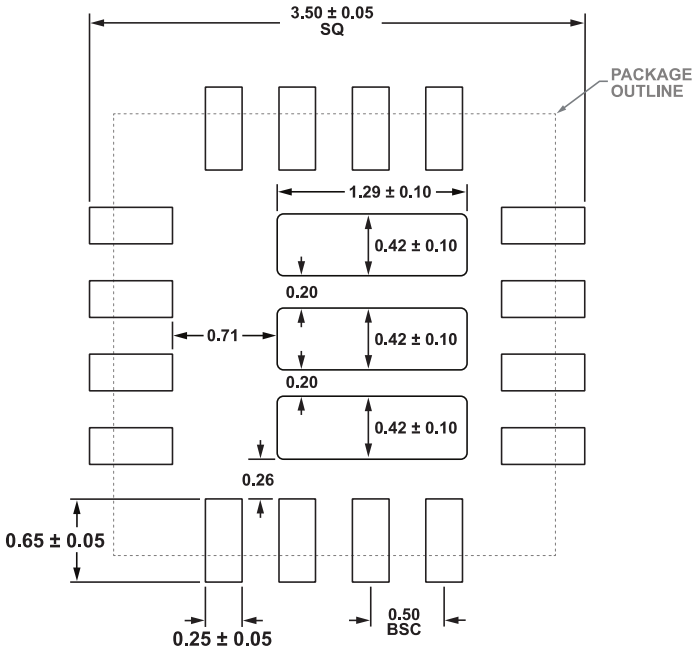
OUTLINE DIMENSIONS

ANALOG DEVICES

19 (16)-Lead Lead Frame Chip Scale Package [LFCSP]
3 x 3mm Body and 0.75mm Package Height
(CP-19-1)
Dimensions shown in millimeters



RECOMMENDED SOLDER PAD LAYOUT
(TOP VIEW)



ORDERING GUIDE

Table 4. Ordering Guide

LEAD FREE FINISH	TAPE AND REEL	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PART MARKING
LT7826ACPZ	LT7826ACPZ-RL	-40°C to 125°C	16-Lead LFCSP (3 x 3mm)	LHWP

Note: Some packages are available in 500-unit reels through designated sales channels with the part number LT7826ACPZ-R7.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7820	Fixed Ratio High Power Inductor less (Charge Pump)	6V < V_{IN} ≤ 72V, Fixed 50% Duty Cycle, 100kHz to 1MHz Switching Frequency (4mm × 5mm) UFD Package
LTC7821	80V, Hybrid Step-Down Synchronous Controller	10V < V_{IN} ≤ 72V, 0.8V < V_{OUT} ≤ V_{IN}/2, 50kHz to 1.7MHz Switching Frequency (5mm × 5mm) UH Package
LTC7825	Fully Integrated 24V/12A Switched Capacitor DC/DC Converter with Overvoltage and Overcurrent Protections	0V < V_{IN} ≤ 24V, 0V < V_{IN} ≤ V_{IN}/2, 100kHz to 1.4MHz Switching Frequency (4mm × 5mm) LGA (LQFN) Package