# 135V Synchronous Buck Controller with Symmetrical Sink/Source Capability and Dynamically Adjustable Output Voltage Programming

## FEATURES

- Wide Input Voltage ($V_{IN}$ - $V_{SS}$) Range: 8.0V to 135V (140V ABS MAX)
- Wide Output Voltage Range: 0.8V ≤ $V_{OUT}$ ≤ 135V (140V ABS MAX)
- Dynamically Adjustable $V_{OUT}$ Programming
- Symmetrical Sink and Source Current Capability for Fast $V_{OUT}$ Slewing Up or Down
- Split-Output Gate Drivers for Adjustable Turn-On and Turn-Off Driver Strengths and Small Dead-Times (35ns)
- Floating I/O Control Pins Referenced to System GND
- 100% Duty Cycle Operation
- Programmable or Synchronizable Frequency (100kHz to 2.5MHz)
- 32-Pin (5mm x 5mm) QFN Package

## APPLICATIONS

- Industrial Power Systems
- Telecommunications Power Systems
- Test Equipment

## GENERAL DESCRIPTION

The **LT7809** is a high-performance, step-down, DC/DC switching regulator controller that drives a N-channel synchronous silicon metal oxide semiconductor field-effect transistor (MOSFET) stage and can operate voltages up to 135V. Its constant frequency current mode architecture allows a phase-lockable switching frequency of up to 2.5MHz.

The gate drive voltage for the LT7809 is 10V to drive standard-threshold MOSFETs to maximize efficiency. An internal charge pump allows for 100% duty cycle operation.

OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The LT7809 features a precision 0.8V reference, enabling the output voltage to be statically programmed from 0.8V to 135V. An output voltage adjustment pin, combined with the LT7809's symmetrical sink and source current capability, allows the output voltage to be dynamically slewed up or down.

## TYPICAL APPLICATION

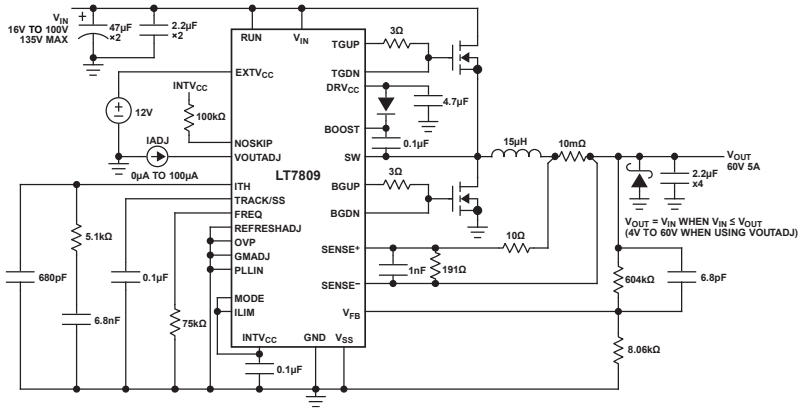


*Figure 1. Dynamic Output Step-Down Converter*

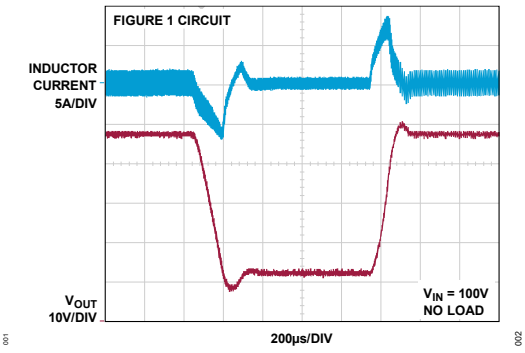


*Figure 2. $V_{OUT}$ Step Waveform for Figure 1*


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## REVISION HISTORY

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| Sp0 | 12/25 | Initial release | — |
| A | 5/26 | Release from limited to open market<br>Updated Table 2 | 7 |

# SPECIFICATIONS

**Table 1. Electrical Characteristics**

(Specifications are for $T_J$ = -40°C to +150°C for the minimum and maximum values, $T_A$ = 25°C for the typical values, all voltages with respect to $V_{SS}$, unless otherwise noted. $V_{IN}$ = 12V, GND = $V_{SS}$, (RUN - GND) = 12V, $EXTV_{CC}$ = $INTV_{CC}$, TGUP = TGDN = TGxx, BGUP = BGDN = BGxx, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Input Supply ($V_{IN}$)** | | | | | | |
| Input Supply Operating Range | $V_{IN}$ | | 8.0 | | 135 | V |
| **Controller Operation** | | | | | | |
| Regulated Output Voltage Set Point | $V_{OUT}$ | | 0.8 | | 135 | V |
| Regulated Feedback Voltage[1] | $V_{FB}$ | $V_{IN}$ = 8V to 135V,<br>ITH voltage = 1.6V to 2.2V<br>$T_A$ = 25°C | <br>0.788<br>0.792 | <br>0.8<br>0.8 | <br>0.812<br>0.808 | <br>V<br>V |
| Feedback Current | | $V_{FB}$ = 0.8V | -75 | 0 | 75 | nA |
| Maximum Current Sense Threshold | $V_{SENSE(MAX)}$ | $V_{FB}$ = 0.7V, $SENSE^-$ = 3.3V<br>ILIM = 0V<br>ILIM = floating<br>ILIM = $INTV_{CC}$ | <br>21<br>45<br>67 | <br>25<br>50<br>75 | <br>29<br>55<br>83 | <br>mV<br>mV<br>mV |
| Minimum Current Sense Threshold | $V_{SENSE(MIN)}$ | $V_{FB}$ = 0.9V, $SENSE^-$ = 3.3V<br>ILIM = 0V<br>ILIM = floating<br>ILIM = $INTV_{CC}$ | <br>-32<br>-53<br>-77 | <br>-22<br>-43<br>-66 | <br>-11<br>-31<br>-52 | <br>mV<br>mV<br>mV |
| $SENSE^+$ Pin Current | $I_{SENSE^+}$ | $SENSE^+$ = 3.3V, $T_A$ = 25°C | -1 | 0 | 1 | µA |
| $SENSE^-$ Pin Current | $I_{SENSE^-}$ | $SENSE^-$ < $INTV_{CC}$ – 0.5V<br>$SENSE^-$ > $INTV_{CC}$ + 0.5V | | 0.85<br>610 | | µA<br>µA |
| Soft-Start Charge Current | | TRACK/SS = 0V | 7 | 9 | 11 | µA |
| RUN Pin ON Threshold<br>RUN Pin Hysteresis | | RUN Rising with respect to GND | 1.10 | 1.25<br>120 | 1.40 | V<br>mV |
| **DC Supply Current** | | | | | | |
| $V_{IN}$ Shutdown Current | | RUN = GND | | 17 | | µA |
| **Gate Drivers** | | | | | | |
| TGxx or BGxx On-Resistance | | Pull-up<br>Pull-down | | 2.5<br>1.5 | | Ω<br>Ω |

(Specifications are for $T_J$ = -40°C to +150°C for the minimum and maximum values, $T_A$ = 25°C for the typical values, all voltages with respect to $V_{SS}$, unless otherwise noted. $V_{IN}$ = 12V, GND = $V_{SS}$, (RUN - GND) = 12V, $EXTV_{CC}$ = $INTV_{CC}$, TGUP = TGDN = TGxx, BGUP = BGDN = BGxx, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| TGxx or BGxx Transition Time[3]<br>Rise Time<br>Fall Time | | | | <br>25<br>15 | | <br>ns<br>ns |
| TGxx Off to BGxx On Delay[3] | | | | 35 | | ns |
| BGxx Off to TGxx On Delay[3] | | | | 35 | | ns |
| TG Minimum On-Time[4] | $t_{ON(MIN)}$ | | | 60 | | ns |
| Maximum Duty Cycle | | Output in Dropout | 100 | | | % |
| **Charge Pump for BST-SW Supply** | | | | | | |
| Charge Pump Output Current<br>$V_{SW}$ = 0V<br>$V_{SW}$ = 12V | | $V_{BST-SW}$ = 7V, | | <br>−110<br>−75 | | <br>µA<br>µA |
| Charge Pump Output Voltage | $V_{BST-SW}$ | BST = −1µA, SW = 0V or 12V | 10 | 11 | 12 | V |
| **Low Dropout (LDO) Linear Regulators** | | | | | | |
| $DRV_{CC}$ Voltage for $V_{IN}$ and $EXTV_{CC}$ LDOs | | $EXTV_{CC}$ = $INTV_{CC}$ for $V_{IN}$ LDO, $EXTV_{CC}$ = 12V for $EXTV_{CC}$ LDO | 9.1 | 9.6 | 10.1 | V |
| $DRV_{CC}$ Load Regulation | | $DRV_{CC}$ load current = 0mA to 100mA, $T_A$ = 25°C | | 1 | 3 | % |
| Undervoltage Lockout | UVLO | $DRV_{CC}$ Rising<br>$DRV_{CC}$ Falling | 7.1<br>6.3 | 7.3<br>6.6 | 7.5<br>6.8 | V<br>V |
| $EXTV_{CC}$ LDO Switchover Voltage | | $EXTV_{CC}$ Rising<br>Hysteresis | 7.4 | 7.6<br>250 | 7.8 | V<br>mV |
| $INTV_{CC}$ Regulation Point | | | | 4.5 | | V |
| **Oscillator and Phase-Locked Loop** | | | | | | |
| Fixed Frequency | $f_{OSC}$ | PLLIN = 0V<br>FREQ = 0V, $T_A$ = 25°C<br>FREQ = $INTV_{CC}$<br>FREQ = 374kΩ<br>FREQ = 75kΩ, $T_A$ = 25°C<br>FREQ = 14.7kΩ | <br>320<br>2.0<br><br>450<br> | <br>370<br>2.25<br>100<br>500<br>2.5 | <br>420<br>2.5<br><br>550<br> | <br>kHz<br>MHz<br>kHz<br>kHz<br>MHz |
| Synchronizable Frequency Range | $f_{SYNC}$ | PLLIN = External Clock | 0.1 | | 2.5 | MHz |

(Specifications are for $T_J$ = -40°C to +150°C for the minimum and maximum values, $T_A$ = 25°C for the typical values, all voltages with respect to $V_{SS}$, unless otherwise noted. $V_{IN}$ = 12V, GND = $V_{SS}$, (RUN - GND) = 12V, $EXTV_{CC}$ = $INTV_{CC}$, TGUP = TGDN = TGxx, BGUP = BGDN = BGxx, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| PLL Lock Time | | PLLIN 100kHz to 1MHz Step | | 100 | | µs |
| PLLIN Input High Level<br>PLLIN Input Low Level | | Voltages with respect to GND | 2.2 | | <br>0.5 | V<br>V |
| **NOSKIP Output** | | | | | | |
| NOSKIP Voltage Low | | $I_{NOSKIP}$ = 2mA<br>Voltage with respect to GND | | 0.2 | 0.4 | V |
| NOSKIP Leakage Current | | $V_{NOSKIP}$ = 5V, $T_A$ = 25°C<br>with respect to GND | -1 | 0 | 1 | µA |
| **VOUTADJ Input** | | | | | | |
| VOUTADJ Current Error | | $(I_{VFB} - I_{VOUTADJ})/I_{VOUTADJ}$, $V_{FB}$ = 0.8V<br>$I_{VOUTADJ}$ = 10µA<br>$I_{VOUTADJ}$ = 100µA | <br>-3<br>-2 | <br>0<br>0 | <br>3<br>2 | <br>%<br>% |
| VOUTADJ Voltage | | $I_{VOUTADJ}$ = 100µA | | | 3.5 | V |
| **GMADJ Setting** | | | | | | |
| Transconductance Amplifier | $g_m$ | ITH = 1.2V, Sink/Source = 5µA<br>GMADJ = float<br>GMADJ = $INTV_{CC}$<br>PLLIN ≥ 1MHz<br>PLLIN = 200kHz<br>GMADJ = 0V<br>PLLIN ≥ 1MHz<br>PLLIN = 200kHz | | <br>3.2<br>3.2<br>3.2<br>2.3<br><br>3.2<br>1.0 | | <br>mS<br>mS<br>mS<br>mS<br><br>mS<br>mS |
| **BOOST Refresh Setting** | | | | | | |
| Boost Refresh Pulse Width | | REFRESHADJ = $INTV_{CC}$<br>REFRESHADJ = float<br>REFRESHADJ = 0V | | 170<br>130<br>95 | | ns<br>ns<br>ns |

1 The LT7809 is tested in a feedback loop that servos $V_{ITH}$ to a specified voltage and measures the resultant $V_{FB}$.

2 Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the *Applications Information* section.

3 Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

4 The minimum on-time condition is specified for an inductor peak-to-peak ripple current >40% of $I_{MAX}$ (See the *Minimum On-Time Considerations* in the Applications Information section).

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise specified. All pins with respect to $V_{SS}$, unless otherwise noted.

**Table 2. Absolute Maximum Ratings**

| PARAMETER | RATING |
|---|---|
| Input Supply ($V_{IN}$) | -0.3V to 140V |
| BOOST | -0.3V to 150V |
| SW | -5V to 150V |
| BOOST to SW | -0.3V to 15V |
| GND | -0.3V to 140V |
| $V_{IN}$ to GND | -0.3V to 140V |
| TGUP, TGDN, BGUP, BGDN[1] | Not applicable |
| $EXTV_{CC}$ | -0.3V to 30V |
| $DRV_{CC}$ | -0.3V to 14V |
| $EXTV_{CC}$ to $DRV_{CC}$ | -6V to 30V |
| $INTV_{CC}$ | -0.3V to 6V |
| RUN | -0.3V to 140V |
| RUN to GND | -0.3V to 140V |
| VOUTADJ to GND | -0.3V to 6V |
| VOUTADJ pin current | 0µA to 200µA |
| PLLIN to GND | -0.3V to 6V |
| NOSKIP to GND | -0.3V to 6V |
| $V_{FB}$, ITH, TRACK/SS, OVP | -0.3V to 6V |
| ILIM, FREQ, MODE | -0.3V to 6V |
| GMADJ, REFRESHADJ | -0.3V to 6V |
| $SENSE^+$, $SENSE^-$ | -0.3V to 140V |
| $SENSE^+$ to $SENSE^-$ | -6V to 0.3V |
| Operating Junction Temperature Range[2] | -40°C to 150°C |
| Storage Temperature Range | -65°C to 150°C |

1 Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only. Otherwise, permanent damage can occur.

2 The LT7809 is specified over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with the board layout, rated package thermal impedance, and other environmental factors. The junction temperature ($T_J$, in °C) is calculated from the ambient temperature ($T_A$, in °C) and power dissipation ($P_D$, in Watts) according to the following formula: $T_J = T_A + (P_D \times \theta_{JA})$, where $\theta_{JA}$ is the package thermal impedance and equals 44°C/W for the 32-lead (5mm × 5mm), quad flat no lead (QFN) package.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

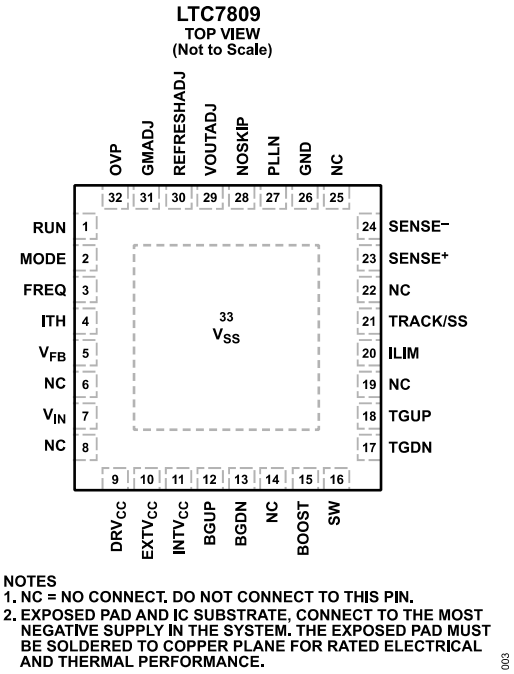



***Figure 3. Pin Configuration***

**Table 3. Pin Descriptions**

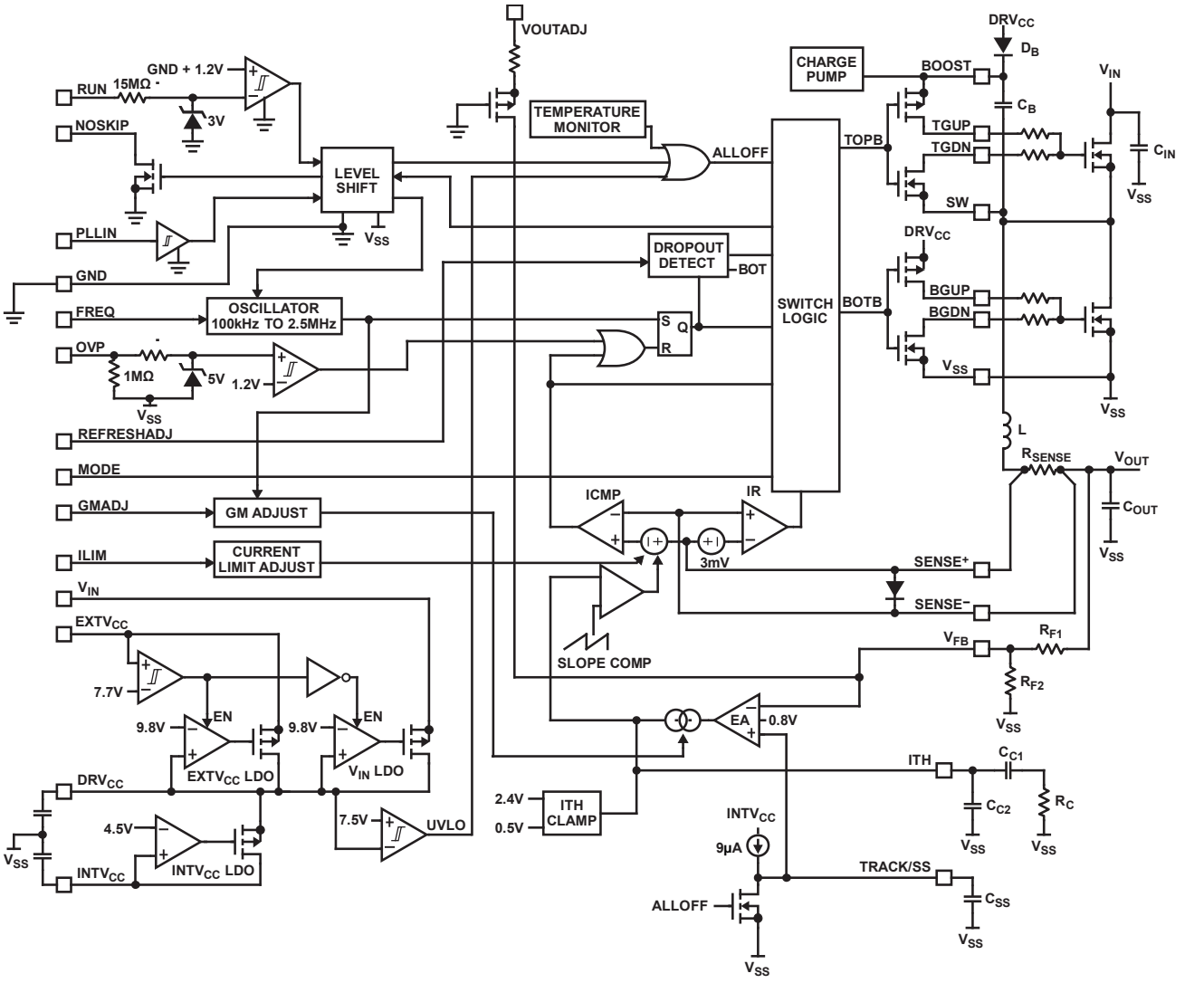
| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | RUN | Run Control Input for the Controller. Forcing RUN pin below 1.2V (with respect to GND) disables switching of the controller. Forcing RUN pin below 0.7V shuts down the entire LT7809, reducing quiescent current to approximately 17µA. The RUN pin is referenced to the GND pin, allowing the LT7809 to be used with a true ground-referenced external signal or logic with no level shifters needed. The RUN pin can be tied to $V_{IN}$ for always-on operation. Do not float this pin. |
| 2 | MODE | Mode Select Input. This input determines how the LT7809 operates at light loads. Connect MODE to $INTV_{CC}$ to force continuous inductor current operation. Tying MODE to $INTV_{CC}$ through a 100kΩ resistor or connecting MODE to $V_{SS}$ selects pulse skipping operation. |
| 3 | FREQ | Frequency Control Pin for the Internal Voltage Controlled Oscillator (VCO). Connect FREQ to $V_{SS}$ for a fixed frequency of 370kHz. Connect FREQ to $INTV_{CC}$ for a fixed frequency of 2.25MHz. Program frequencies between 100kHz and 2.5MHz by using a resistor between FREQ and $V_{SS}$. Minimize the capacitance on FREQ. |
| 4 | ITH | Error Amplifier Output and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage. |

| | | |
|---|---|---|
| 5 | $V_{FB}$ | Error Amplifier Feedback Input. The $V_{FB}$ pin receives the remotely sensed feedback voltage from an external resistive divider across the output. |
| 6 | NC | No Connect. Leave pin 6 floating. |
| 7 | $V_{IN}$ | Main Supply Pin. A bypass capacitor must be tied between $V_{IN}$ and $V_{SS}$. |
| 8 | NC | No Connect. Leave pin 8 floating. |
| 9 | $DRV_{CC}$ | Gate Driver Output of the internal LDO regulator from $V_{IN}$ or $EXTV_{CC}$. The gate drivers and the $INTV_{CC}$ internal LDO are powered from $DRV_{CC}$. A low ESR 4.7µF ceramic bypass capacitor should be connected between $DRV_{CC}$ and $V_{SS}$, as close as possible to the IC. |
| 10 | $EXTV_{CC}$ | External Power Input to an Internal LDO Regulator Connected to $DRV_{CC}$. This LDO regulator supplies $DRV_{CC}$ power, bypassing the internal $V_{IN}$ LDO regulator whenever $EXTV_{CC}$ is higher than the $EXTV_{CC}$ switchover voltage. See the $EXTV_{CC}$ connection in the *Power and Bias Supplies (VIN, EXTVCC, DRVCC, and INTVCC)* section. Do not exceed 30V on $EXTV_{CC}$ with respect to $V_{SS}$. Connect $EXTV_{CC}$ to $INTV_{CC}$ if the $EXTV_{CC}$ LDO regulator is not used. |
| 11 | $INTV_{CC}$ | Output of the Internal 4.5V Low Dropout Regulator from $DRV_{CC}$. The internal analog and digital circuits are powered from this pin. A low ESR 0.1µF ceramic bypass capacitor should be connected between $INTV_{CC}$ and $V_{SS}$, as close as possible to the IC. |
| 12 | BGUP | High Current Gate Driver Pull-Up for Bottom MOSFET. BGUP pulls up to $DRV_{CC}$. Tie BGUP directly to the bottom MOSFET gate for maximum gate drive transition speed on the gate rising edge. Tie a resistor between BGUP and the bottom MOSFET gate to adjust the gate rising slew rate. BGUP also serves as the Kelvin sense of the bottom MOSFET gate during turn-off. |
| 13 | BGDN | High Current Gate Driver Pull-Down for Bottom MOSFET. BGDN pulls down to $V_{IN}$. Tie BGDN directly to the bottom MOSFET gate for maximum gate drive transition speed on the gate falling edge. Tie a resistor between BGDN and the bottom MOSFET gate to adjust the gate falling slew rate. BGDN also serves as the Kelvin sense of the bottom MOSFET gate during turn-on. |
| 14 | NC | No Connect. Leave pin 14 floating. |
| 15 | BOOST | Bootstrapped Supply to the Top Side Floating Driver. Connect a capacitor between the BOOST and SW pins. Also connect a Schottky diode between the BOOST and $DRV_{CC}$ pins. The voltage swing at the BOOST pin is from $DRV_{CC}$ to ($V_{IN}$ + $DRV_{CC}$). |
| 16 | SW | Switch Node Connection to Inductor. |
| 17 | TGDN | High Current Gate Driver Pull-Down for Top MOSFET. TGDN pulls down to SW. Tie TGDN directly to the top MOSFET gate for maximum gate drive transition speed on the gate falling edge. Tie a resistor between TGDN and the top MOSFET gate to adjust the gate falling slew rate. |
| 18 | TGUP | High Current Gate Driver Pull-Up for Top MOSFET. TGUP pulls up to BOOST. Tie TGUP directly to the top MOSFET gate for maximum gate drive transition speed on the gate rising edge. Tie a resistor between TGUP and the top MOSFET gate to adjust the gate rising slew rate. |
| 19 | NC | No Connect. Leave pin 19 floating. |

| | | |
|---|---|---|
| 20 | ILIM | Current Comparator Sense Voltage Range Input. Tying ILIM to $V_{SS}$ or $INTV_{CC}$ or floating ILIM sets the maximum current sense threshold to one of three different levels (25mV, 75mV, and 50mV, respectively). |
| 21 | TRACK/SS | External Tracking/Soft Start Input. TRACK/SS regulates the $V_{FB}$ voltage to the lesser of 0.8V or the voltage on the TRACK/SS pin. An internal 9µA pull-up current source is connected to TRACK/SS. A capacitor to $V_{SS}$ at TRACK/SS sets the ramp time to the final regulated output voltage. The ramp time is equal to 1ms for every 11.25nF of capacitance. Alternatively, a resistor divider on another voltage supply connected to TRACK/SS allows the output to track the other supply during startup. |
| 22 | NC | No Connect. Leave pin 22 floating. |
| 23 | $SENSE^+$ | The Positive Input to the Differential Current Comparator. The ITH pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins in conjunction with the current sense resistor ($R_{SENSE}$) set the current trip threshold. |
| 24 | $SENSE^-$ | The Negative Input to the Differential Current Comparator. The $SENSE^-$ pin supplies current to the current comparator when $SENSE^-$ is greater than $INTV_{CC}$. |
| 25 | NC | No Connect. Leave pin 25 floating. |
| 26 | GND | Ground. This pin should be externally tied to system ground. The RUN, PLLIN, NOSKIP, and VOUTADJ pins are reference to this GND pin. |
| 27 | PLLIN | External Synchronization Input to Phase Detector. When an external clock is applied to PLLIN with respect to GND, the phase-locked loop forces the rising TGxx signal to synchronize with the rising edge of the external clock. When not synchronizing to an external clock, tie PLLIN to GND. |
| 28 | NOSKIP | No Skip Pulse Open-Drain Logic Output. This pin is high impedance when the controller is switching at full frequency and pulled to GND when the controller skips pulses (when the top gate does not turn on at the start of each switching cycle or when the bottom gate stays on at the start of each switching cycle). |
| 29 | VOUTADJ | $V_{OUT}$ Adjust Current Input. The current injected into this pin becomes the pull-up current on the VFB node. The amount of current into the VOUTADJ pin should not exceed 100µA. This pin is referenced to the GND pin. When not used, VOUTADJ needs to be floating. |
| 30 | REFRESHADJ | Boost Refresh Adjust Program Pin. This pin programs the minimum BG pulse width under dropout conditions. Tying this pin to $V_{SS}$ or floating or $INTV_{CC}$ sets the minimum BG pulse width to one of three different settings (95ns, 130ns, and 170ns, respectively). |
| 31 | GMADJ | Error Amplifier (EA) GM Adjust Program Pin. This pin programs how the error amplifier's transconductance ($g_m$) scales with frequencies below 1MHz. Tying this pin to $V_{SS}$ or $INTV_{CC}$ allows the $g_m$ of EA to scale down with frequencies below 1MHz. The $V_{SS}$ setting reduces $g_m$ with frequency at a steeper rate ($g_m$ = 1.0 mS at 200kHz) compared to the $INTV_{CC}$ setting ($g_m$ = 2.3 mS at 200kHz). Floating this pin maintains a fixed EA $g_m$ ($g_m$ = 3.2 mS) under all operating frequencies. See *GMADJ Pin* in the Applications Information section for more information. |
| 32 | OVP | Tie to $V_{SS}$. |

| | | |
|---|---|---|
| 33 | $V_{SS}$ (EPAD) | Exposed Pad and IC substrate, connect to the most negative supply in the system. The exposed pad must be soldered to copper plane for rated electrical and thermal performance. |

## BLOCK DIAGRAM




*ALL VOLTAGES WITH RESPECT TO $V_{SS}$ UNLESS OTHERWISE NOTED

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***Figure 4. Block Diagram***

## TYPICAL PERFORMANCE CHARACTERISTICS

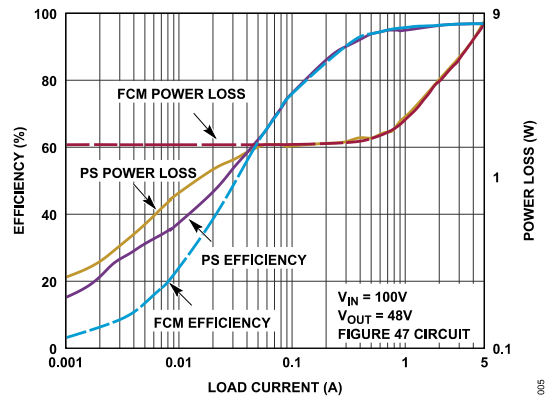



*Figure 5. Efficiency and Power Loss vs Load Current*

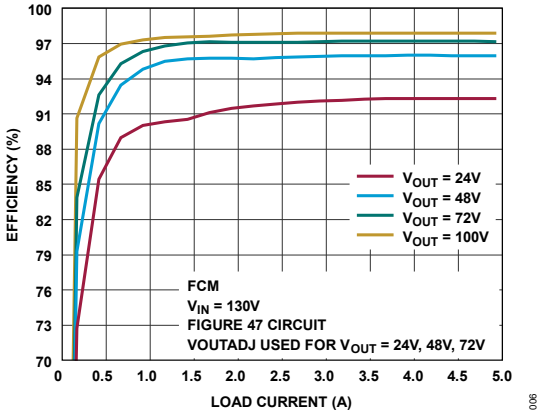



*Figure 6. Efficiency vs Load Current*

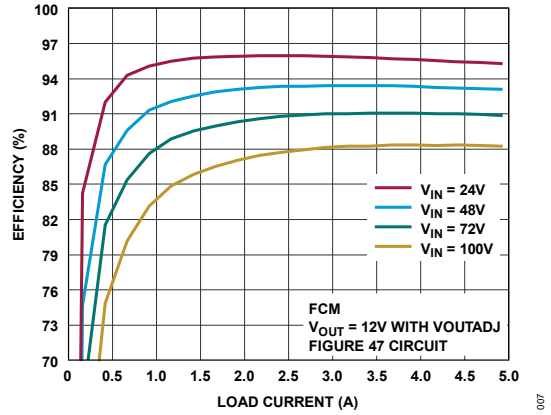



*Figure 7. Efficiency vs Load Current*

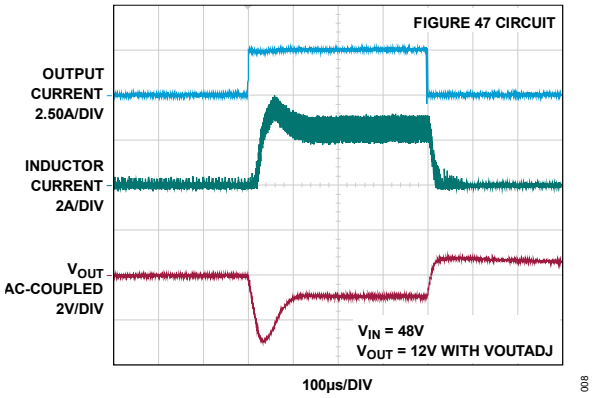



*Figure 8. Load Step Pulse-Skipping Mode*

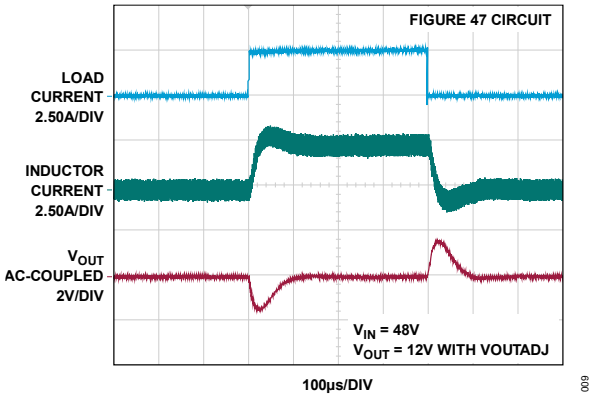



*Figure 9. Load Step Forced Continuous Mode*

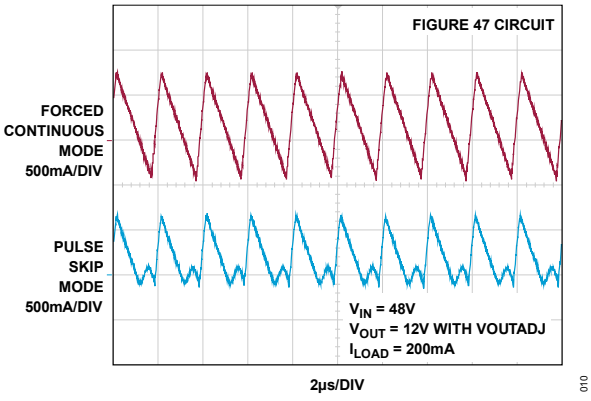



*Figure 10. Inductor Current at Light Load*

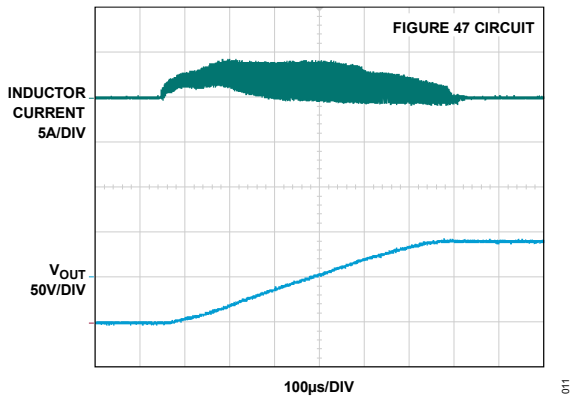



*Figure 11. $V_{OUT}$ Step Pulse-Skipping Mode*

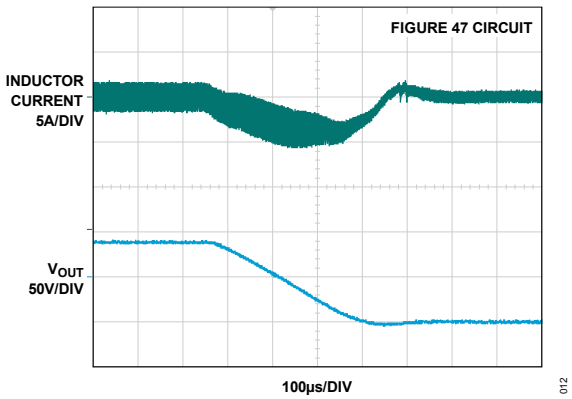



*Figure 12. $V_{OUT}$ Step Forced Continuous Mode*

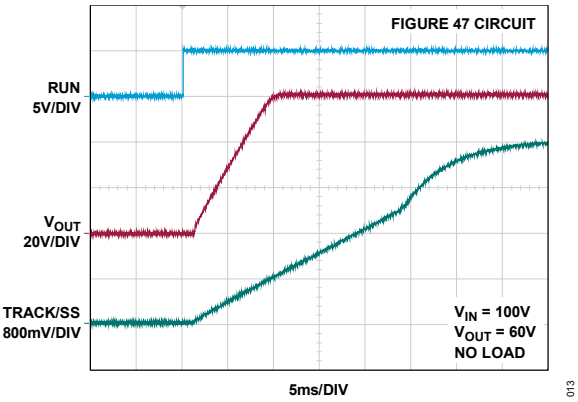



*Figure 13. Soft Start-Up*

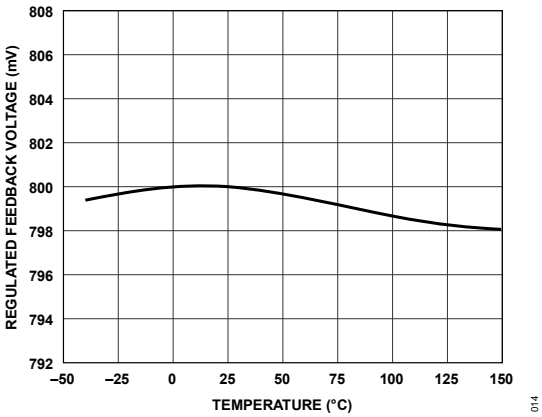



*Figure 14. Regulated Feedback Voltage vs Temperature*

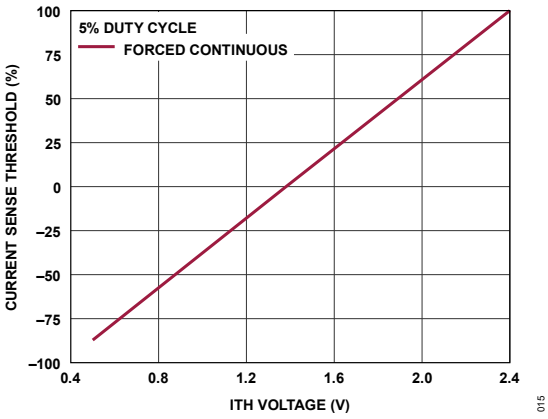



*Figure 15. Maximum Current Sense Threshold vs $V_{ITH}$ in Forced Continuous Mode*

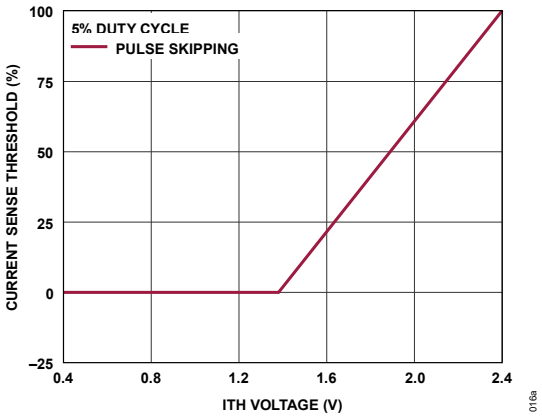



*Figure 16. Maximum Current Sense Threshold vs $V_{ITH}$ in Pulse-Skipping Mode*

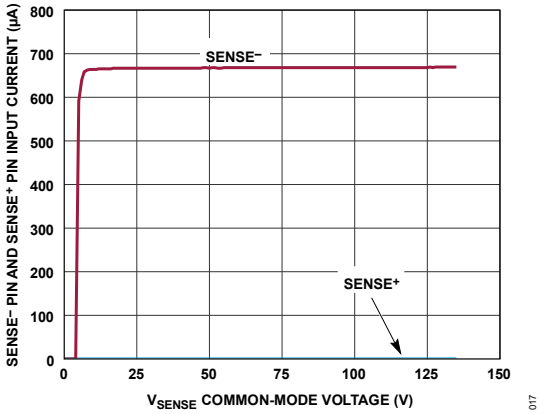



*Figure 17. SENSE Input Current vs $V_{SENSE}$ Voltage*

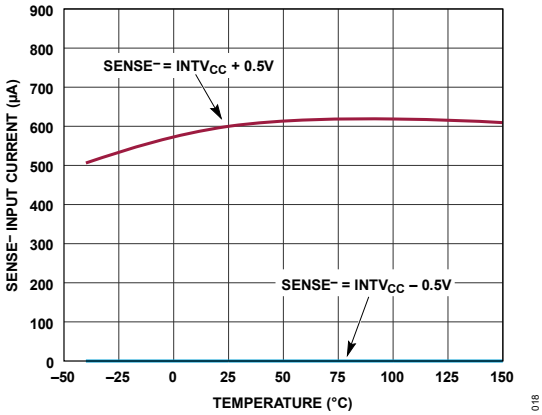



*Figure 18. SENSE⁻ Input Current vs Temperature*

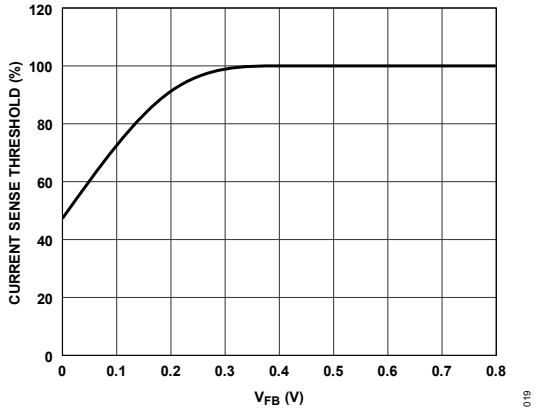



*Figure 19. Foldback Current Limit*

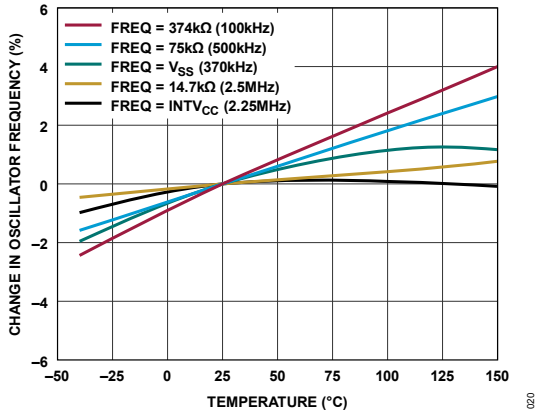



*Figure 20. Oscillator Frequency vs Temperature*

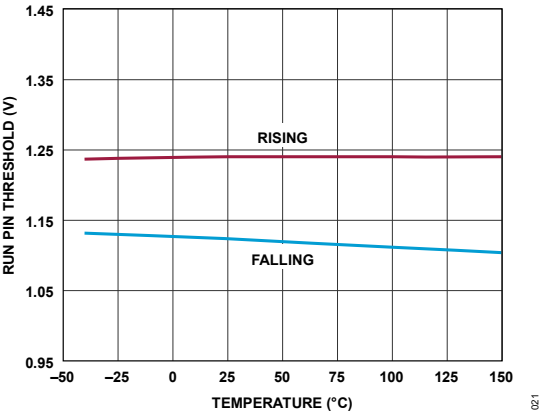



*Figure 21. RUN Pin Threshold vs Temperature*

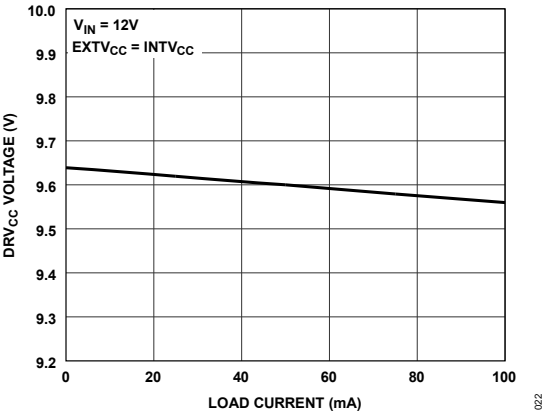



*Figure 22. $DRV_{CC}$ Load Regulation*

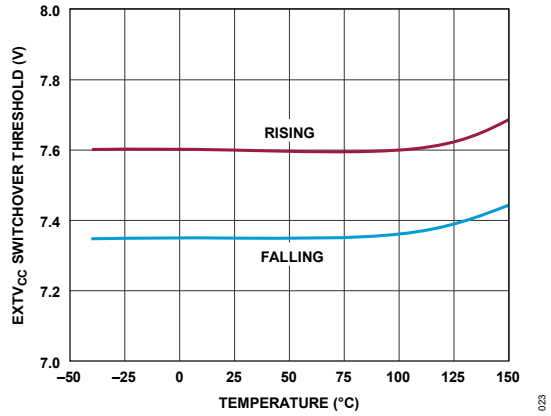



*Figure 23. $EXTV_{CC}$ Switchover Voltage vs Temperature*

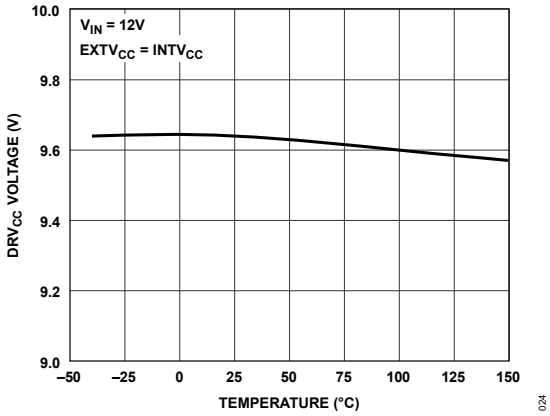



*Figure 24. $DRV_{CC}$ Voltage vs Temperature*

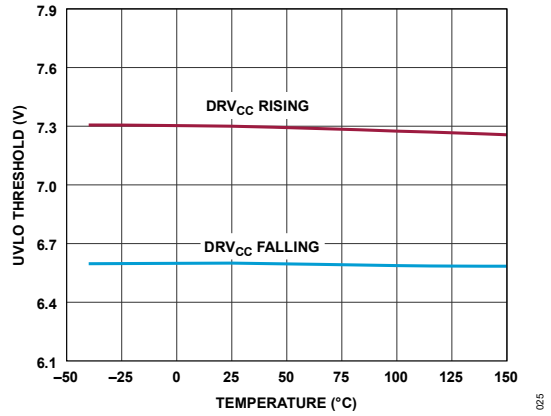



*Figure 25. $DRV_{CC}$ Undervoltage Lockout Threshold vs Temperature*

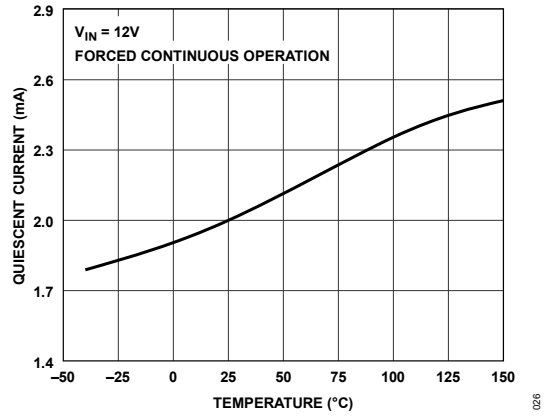



*Figure 26. Quiescent Current vs Temperature*

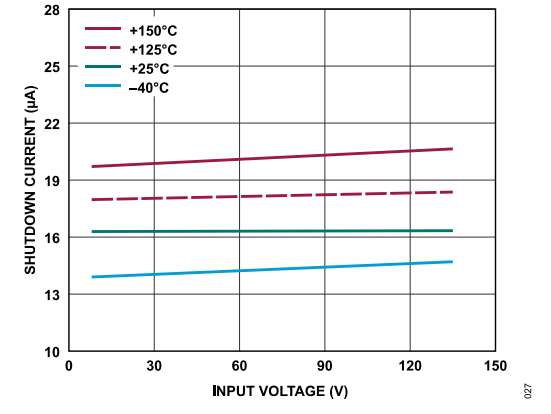



*Figure 27. Shutdown Current vs $V_{IN}$ Voltage*

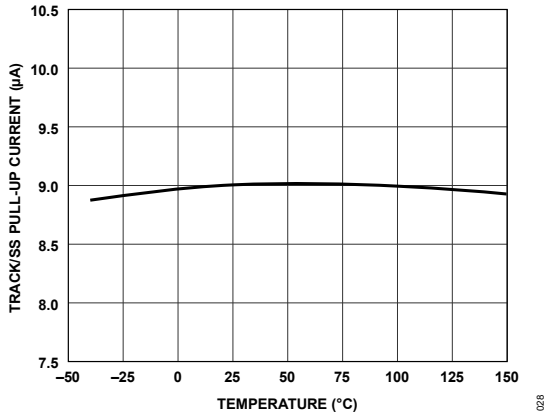



*Figure 28. TRACK/SS Pull-up Current vs Temperature*

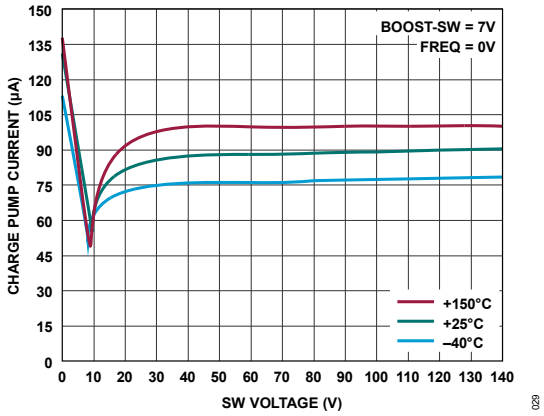



*Figure 29. Boost Charge Pump Output Current vs SW Voltage*

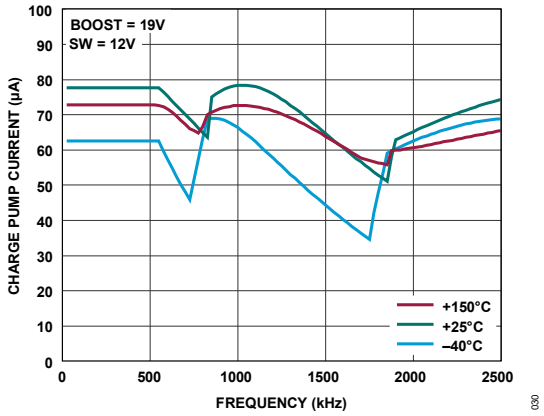



*Figure 30. Boost Charge Pump Output Current vs Frequency*

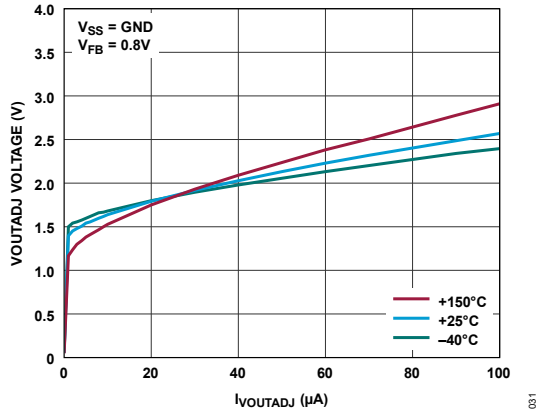



*Figure 31. VOUTADJ Voltage vs $I_{VOUTADJ}$*

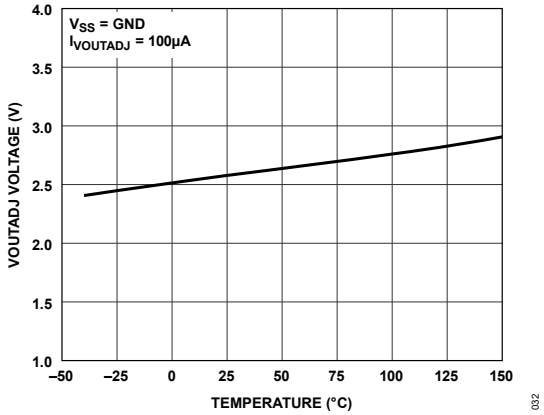



*Figure 32. VOUTADJ Voltage vs Temperature*

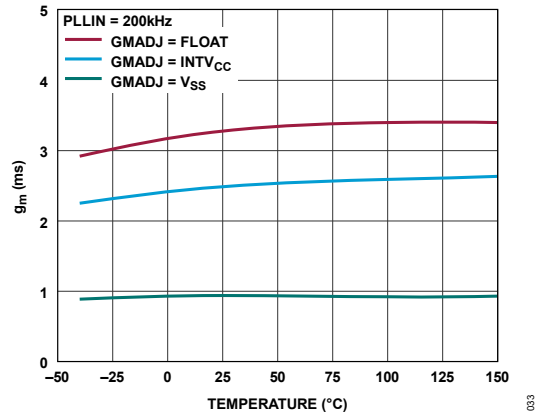



*Figure 33. $g_m$ vs Temperature*

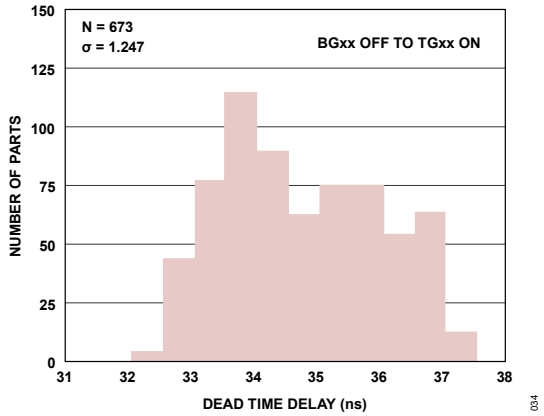



*Figure 34. BGxx Off to TGxx On Delay Histogram*

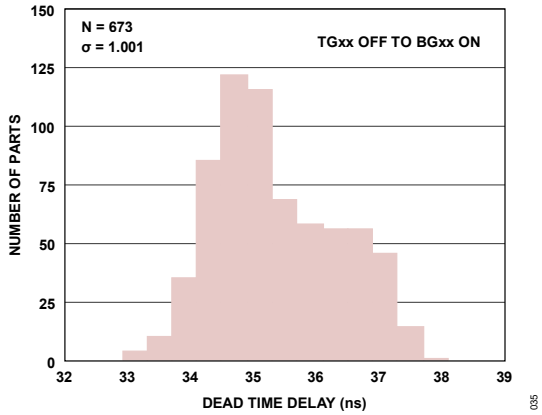



*Figure 35. TGxx Off to BGxx On Delay Histogram*

# THEORY OF OPERATION

## Main Control Loop

The LT7809 is a synchronous controller using a constant frequency, peak-current mode architecture. During normal operation, the external top MOSFET turns on when the clock sets the set/reset (SR) latch, causing the inductor current to increase. The main switch turns off when the main current comparator, ICMP, resets the SR latch. After the top MOSFET is turned off each cycle, the bottom MOSFET turns on, which causes the inductor current to decrease until either the inductor current starts to reverse, as indicated by the current comparator (IR), or the beginning of the next clock cycle.

The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier (EA). The error amplifier compares the output voltage feedback signal at the $V_{FB}$ pin (which is generated with an external resistor divider connected across the output voltage, $V_{OUT}$, to $V_{SS}$ and a current injected into the VOUTADJ pin) to the internal 0.8V reference voltage. When the load current increases, it causes a slight decrease in $V_{FB}$ relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

## Power and Bias Supplies ($V_{IN}$, $EXTV_{CC}$, $DRV_{CC}$, and $INTV_{CC}$)

The $DRV_{CC}$ pin supplies power for the top and bottom MOSFET drivers. LDO linear regulators are available from both the $V_{IN}$ pin and the $EXTV_{CC}$ pin to provide power to $DRV_{CC}$. When the $EXTV_{CC}$ pin is tied to a voltage below its switchover voltage, the $V_{IN}$ LDO regulator supplies power to $DRV_{CC}$. If $EXTV_{CC}$ is taken above its switchover voltage, the $V_{IN}$ LDO regulator turns off and the $EXTV_{CC}$ LDO regulator turns on. When enabled, the $EXTV_{CC}$ LDO regulator supplies power to $DRV_{CC}$. Using the $EXTV_{CC}$ pin allows the $DRV_{CC}$ power to be derived from a high efficiency external source, such as the LT7809 switching regulator output.

The $INTV_{CC}$ pin supplies power for most of the internal circuits in the LT7809. The $INTV_{CC}$ supply is derived from an LDO linear regulator from $DRV_{CC}$ and is regulated to 4.5V.

## High-Side Bootstrap Capacitor (REFRESHADJ Pin)

The top MOSFET driver is biased from the floating bootstrap capacitor, $C_B$, which normally recharges during each cycle through an external diode when the SW voltage goes low. As the input and output voltages get closer together and the loop causes the duty cycle to increase, the turn-on time for the bottom MOSFET decreases. A minimum turn-on time for the bottom MOSFET provides time for the bootstrap capacitor to refresh its voltage. This refresh time can be programmed to one of three settings (95ns, 130ns, or 170ns) based on the configuration of the REFRESHADJ pin.

The LT7809 also has an internal charge pump that keeps the required bias on BOOST when the loop enters dropout and turns on the top FET continuously, resulting in 100% duty cycle. The internal charge pump can nominally supply a charging current of 80µA.

## Startup and Shutdown (RUN and TRACK/SS Pins)

The LT7809 can be shut down using the RUN pin. Pulling the RUN pin below 1.08V with respect to GND shuts down the main control loop. Pulling the RUN pin below 0.7V with respect to GND disables the controller and most internal circuits, including the $DRV_{CC}$ and $INTV_{CC}$ LDO regulators. In this shutdown state, the LT7809 draws only 17µA of quiescent current.

The RUN pin needs to be externally pulled up or driven directly by logic. The RUN pin can tolerate up to 140V (absolute maximum) with respect to $V_{SS}$ and 140V with respect to GND. Therefore, the pin can be tied to $V_{IN}$ in always-on applications where the controller is enabled continuously and never shuts down. Additionally, a resistor divider

from $V_{IN}$ to the RUN pin can be used to set a precise input undervoltage lockout so that the power supply does not operate below a user-adjustable level.

The startup of $V_{OUT}$ is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 0.8V internal reference voltage (with respect to $V_{SS}$), the LT7809 regulates the $V_{FB}$ voltage to the TRACK/SS pin voltage instead of the 0.8V reference voltage. This method allows the TRACK/SS pin to be used as a soft-start, which smoothly ramps the output voltage on startup, limiting the input supply inrush current. An external capacitor from the TRACK/SS pin to $V_{SS}$ is charged by an internal 9µA pull-up current, creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 0.8V (and beyond), $V_{OUT}$ rises smoothly from zero to its final value.

Alternatively, the TRACK/SS pin can be used to make the startup of $V_{OUT}$ track that of another supply. Typically, this requires connecting to the TRACK/SS pin through an external resistor divider from the other supply to $V_{SS}$ (see the *RUN Pin* section and *Soft-Start and Tracking (TRACK/SS Pin)* section).

## Frequency Selection and Phase-Locked Loop (FREQ and PLLIN Pins)

The free running switching frequency of the LT7809 controller is selected using the FREQ pin. Tying FREQ to $V_{SS}$ selects 370kHz, whereas tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and $V_{SS}$ allows the frequency to be programmed between 100kHz and 2.5MHz.

A phase-locked loop (PLL) is available on the LT7809 to synchronize the internal oscillator to an external clock source connected to the PLLIN pin with respect to GND. The PLL of the LT7809 aligns the turn-on of the external top MOSFET to the rising edge of the synchronizing signal.

The PLL frequency is prebiased to the free running frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL only needs to make slight changes to synchronize the rising edge of the external clock to the rising edge of TGxx. For more rapid lock to the external clock, use the FREQ pin to set the internal oscillator to approximately the frequency of the external clock. The PLL of the LT7809 is guaranteed to lock to an external clock source whose frequency is between 100kHz and 2.5MHz.

The PLLIN pin is transistor-transistor logic (TTL)-compatible with thresholds of 1.6V (rising) and 1.1V (falling) with respect to GND and is guaranteed to operate with a clock signal swing of 0.5V to 2.2V.

## Foldback Current

If the voltage on the $V_{FB}$ pin falls to less than 300mV continuously for 180µs, foldback current limiting gets activated and progressively lowers the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the $V_{FB}$ voltage is keeping up with the TRACK/SS voltage).

## Full Frequency Operation Indicator (NOSKIP Pin)

The NOSKIP pin indicates whether the controller is switching at full frequency or skipping pulses. NOSKIP is connected to an open drain of an internal N-channel MOSFET with its source connected to the GND pin. When the MOSFET is off, the NOSKIP pin is allowed to be pulled up by an external resistor to a source no greater than 6V (with respect to the GND pin). The internal MOSFET is turned off (NOSKIP becomes high impedance) whenever the controller is switching at full frequency. The MOSFET is turned on (NOSKIP gets pulled to GND) whenever the controller skips a switching cycle, which occurs when either the top gate remains off at the start of the next switching cycle (very low duty cycles) or when the top gate remains on at the start of the next switching cycle (very high duty cycles). The MOSFET is turned off again once the top gate turns on at the start of the next switching cycle.

### Dynamically Adjustable Output Voltage Programming (VOUTADJ Pin)

$V_{OUT}$ can be dynamically adjusted through control of the VOUTADJ pin. Current injected into the VOUTADJ pin becomes an internal pull-up current on the $V_{FB}$ pin, such that $V_{OUT}$ can be slewed up or down depending on the amount of current sourced into the VOUTADJ pin.

## APPLICATIONS INFORMATION

*Figure 1* is a basic LT7809 application circuit. External component selection is largely driven by the load requirement and begins with the selection of the inductor, current sense components, operating frequency, and light load operating mode. The remaining power stage components, consisting of the input and output capacitors and power FETs, can then be chosen. Next, feedback resistors are selected to set the desired output voltage. Then, the remaining external components are selected, such as for soft-start, biasing, and loop compensation.

### Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this trade-off, the effect of the inductor value on the ripple current and low current operation must also be considered. The inductor value has a direct effect on the ripple current.

The maximum average inductor current ($I_{L(MAX)}$) is equal to the maximum output current. The peak current is equal to the average inductor current plus half of the inductor ripple current ($\Delta I_L$), which decreases with higher inductance (L) or higher frequency (f) and increases with higher $V_{IN}$, as shown in Equation 1, as follows:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

Accepting larger values of $\Delta I_L$ allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \times I_{L(MAX)}$. The maximum $\Delta I_L$ occurs at the maximum input voltage.

### Inductor Core Selection

When the value for L is known, select the type of inductor. High efficiency regulators generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. The actual core loss is independent of the core size for a fixed inductor value, but it is dependent on the inductance value selected. As inductance increases, core losses decrease. However, because increased inductance requires more turns of wire, copper losses increase.

Ferrite designs have low core loss and are preferred for high switching frequencies. Therefore, design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This collapse results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

### Current Sense Selection

The LT7809 can be configured to use either inductor DC resistance (DCR) sensing or low value resistor sensing. The choice between the two current sensing schemes is a design trade-off between cost, power consumption, and accuracy. DCR sensing is popular because it saves expensive current sensing resistors and is more power efficient, particularly in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. The selection of other external components is driven by the load requirement and begins with the selection of $R_{SENSE}$ (if $R_{SENSE}$ is used) and the inductor value.

The SENSE+ and SENSE– pins are the inputs to the current comparator. The common mode voltage range on these pins is 0V to 140V (the absolute maximum), enabling the LT7809 to regulate output voltages up to a maximum of 135V. The SENSE+ pin is high impedance, drawing less than ≈1µA. This high impedance allows the current comparator to be used in inductor DCR sensing. The impedance of the SENSE– pin changes depending on the common mode voltage. When less than $INTV_{CC}$ – 0.5V, the SENSE– pin is relatively high impedance, drawing ≈1µA. When the SENSE– pin is above $INTV_{CC}$ + 0.5V, a higher current (≈700µA) flows into the pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current. The SENSE– pin has an additional ≈70µA current when its voltage is above 3.2V to bias internal circuitry from $V_{OUT}$ instead of $V_{IN}$, which reduces the input referred supply current.

Filter components mutual to the sense lines must be placed close to the LT7809, and the sense lines must run close together to a Kelvin connection underneath the current sense element (shown in *Figure 36*). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (*Figure 38*), the R1 resistor must be placed close to the switching node to prevent noise from coupling into sensitive small signal nodes.

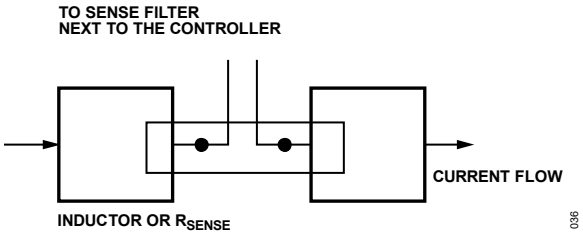



***Figure 36. Sense Lines Placement with Inductor or Sense Resistor***

## Low Value Resistor Current Sensing

*Figure 37* shows a typical sensing circuit using a discrete resistor. $R_{SENSE}$ is chosen based on the required output current. The current comparator of the controller has a $V_{SENSE(MAX)}$ of 50mV, 25mV, or 75mV, as determined by the state of the ILIM pin. The current comparator threshold voltage sets the peak inductor current.

Using the maximum inductor current ($I_{L(MAX)}$) and ripple current ($\Delta I_L$) (as described in the *Inductor Value Calculation* section), the target sense resistor value is given by Equation 2, as follows:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (2)$$

To ensure that the application delivers full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the *Table 1*.

The parasitic inductance (ESL) of the sense resistor introduces significant error in the current sense signal for lower inductor value (3µH) or higher current (5A) applications. This error is proportional to the input voltage and can degrade line regulation or cause loop instability. Placing an RC filter ($R_F$) into the sense pins, as shown in *Figure 37*, can be used to compensate for this error. For optimal cancellation of the ESL, set the RC filter time constant to $R_F \times C_F = ESL/R_{SENSE}$ ($C_F$ is the filter capacitor). In general, select $C_F$ to be in the range of 1nF to 10nF and calculate the corresponding $R_F$. Surface-mount sense resistors in low ESL, wide footprint geometries are recommended to minimize this error. If not specified in the data sheet of the manufacturer, the ESL can be approximated as 0.4nH for a resistor with a 1206 footprint, and 0.2nH for a resistor with a 1225 footprint.

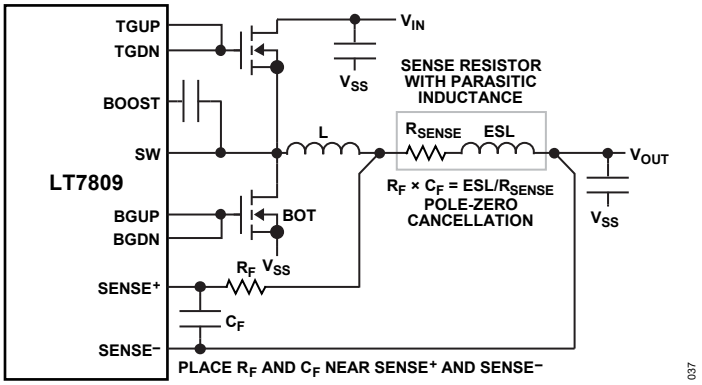



*Figure 37. Current Sensing Methods-Using a Resistor to Sense Current*

## Inductor DCR Current Sensing

For applications requiring the highest possible efficiency at high load currents, the LT7809 is capable of sensing the voltage drop across the inductor DCR, as shown in *Figure 38*. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor costs several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2) × C1 time constant is chosen to be equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. The DCR can be measured using an inductance, capacitance, and resistance (LCR) meter. However, the DCR tolerance is not always the same and varies with temperature. Consult the data sheet of the manufacturer for detailed information.

Using $I_{L(MAX)}$ and $\Delta I_L$ (as described in the *Inductor Value Calculation* section), the target sense resistor value is given by Equation 3, as follows:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (3)$$

To ensure that the application delivers full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in *Table 1*.

Next, determine the DCR of the inductor. When provided, use the maximum value noted by the manufacturer, typically given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for the maximum inductor temperature ($T_{L(MAX)}$) is 100°C. To scale the maximum inductor DCR ($DCR_{MAX}$) to the desired sense resistor ($R_D$) value, use the divider ratio given by Equation 4, as follows:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}} \quad (4)$$

C1 is typically selected to be in the range of 0.1µF to 0.47µF. This range forces the equivalent resistance (R1||R2) to around 2kΩ, reducing the error that can result from the ≈1µA current of the SENSE+ pin.

R1||R2 is scaled to the room temperature inductance and the maximum DCR given by Equation 5, as follows:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \cdot C1} \quad (5)$$

The sense resistor values are given by Equation 6 and Equation 7, as follows:

$$R1 = \frac{R1||R2}{R_D} \tag{6}$$

$$R2 = \frac{R1 \cdot R_D}{1 - R_D} \tag{7}$$

The maximum power loss ($P_{LOSS}$) in R1 is related to the duty cycle and occurs in continuous mode at the maximum input voltage ($V_{IN(MAX)}$) given by Equation 8, as follows:

$$P_{LOSS} \text{ in } R1 = \frac{(V_{IN(MAX)} - V_{OUT}) \cdot V_{OUT}}{R1} \tag{8}$$

Ensure that R1 has a power rating higher than $P_{LOSS}$ in R1. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses, and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

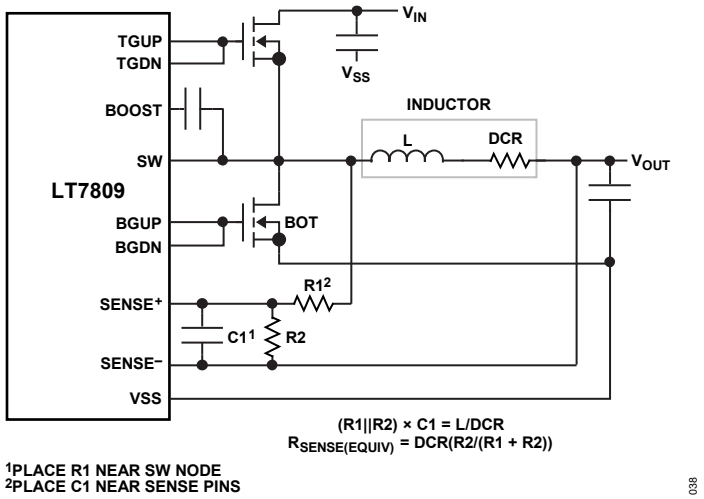



***Figure 38. Current Sensing Methods-Using the Inductor DCR to Sense Current***

## Setting the Operating Frequency

Selecting the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing gate charge and transition losses, but requires larger inductance values and/or more output capacitance to maintain low output ripple voltage.

In higher voltage applications, transition losses contribute more significantly to power loss, and a proper balance between size and efficiency is achieved with a switching frequency between 300kHz and 900kHz. Lower voltage applications benefit from lower switching losses, and can operate at switching frequencies up to 2.5MHz, if desired. The switching frequency is set using the FREQ and PLLIN pins, as shown in *Table 4*.

**Table 4. Setting the Switching Frequency**

| FREQ PIN | PLLIN PIN | FREQUENCY |
|---|---|---|
| $V_{SS}$ | GND | 370kHz |
| $INTV_{CC}$ | GND | 2.25MHz |
| Resistor to $V_{SS}$ | GND | 100kHz to 2.5MHz |
| Any of the Above | External clock 100kHz to 2.5kHz referenced to the GND pin | Phase-Locked to External Clock |

Tying the FREQ pin to $V_{SS}$ selects 370kHz, whereas tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and $V_{SS}$ allows the frequency to be programmed anywhere between 100kHz and 2.5MHz. Choose a FREQ pin resistor ($R_{FREQ}$) from *Figure 39* or Equation 9, as follows:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{f_{OSC}} \quad (9)$$

A PLL is also available on the LT7809 to synchronize the internal oscillator to an external clock source connected to the PLLIN pin with respect to GND. After the PLL locks, TGxx is synchronized to the rising edge of the external clock signal. See the *Phase-Locked Loop and Frequency Synchronization* section for details.

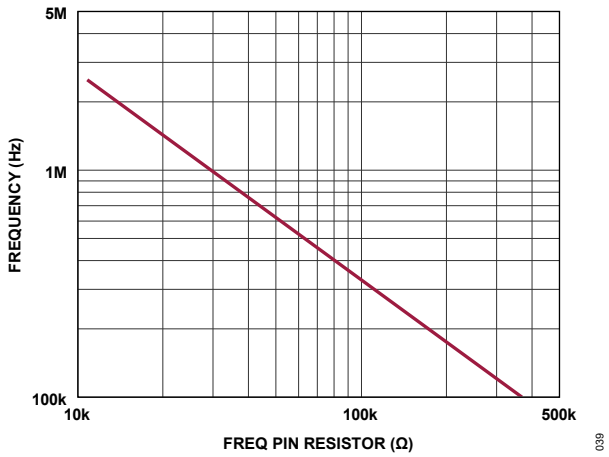



***Figure 39. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin***

## Selecting Light-Load Operating Mode

The LT7809 can be set to enter constant frequency pulse-skipping mode or forced continuous conduction mode at light load currents. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to $INTV_{CC}$ through a 100kΩ resistor or tie the MODE pin to $V_{SS}$. When synchronized to an external clock through the PLLIN pin, the LT7809 operates in pulse-skipping mode if it is selected. Otherwise, the LT7809 operates in forced continuous mode.

The requirements of each application dictate the appropriate choice for light-load operating mode. In forced continuous mode, the inductor current is allowed to reverse at light loads and switches at the same frequency regardless of the load. In this mode, the efficiency at light loads is considerably lower. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of the load current.

In pulse-skipping mode, constant frequency operation is maintained down to approximately 1% of the designed maximum output current. At very light loads, the PWM comparator can remain tripped for several cycles and force

the top MOSFET to remain off for the same number of cycles (that is, skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). Pulse-skipping mode provides higher light load efficiency than forced continuous mode. Consequently, pulse-skipping mode represents a compromise between light load efficiency, output ripple, and EMI.

## Power MOSFET Selection

Note that for this section $V_{IN}$ represents ($V_{IN}$ - $V_{SS}$) and $V_{OUT}$ represents ($V_{OUT}$ – $V_{SS}$).

Two external power FETs must be selected for the LT7809: one N-channel MOSFET for the top (main) switch and one N-channel MOSFET for the bottom (synchronous) switch. The peak-to-peak drive levels are set by the $DRV_{CC}$ regulation point (10V). Therefore, both logic-level and standard-level threshold MOSFETs can be used in most applications. Pay close attention to the breakdown voltage ($BVD_{SS}$) specification for the MOSFETs as well.

Selection criteria for the power MOSFETs include the on resistance ($R_{DS(ON)}$), miller capacitance ($C_{MILLER}$), input voltage, and maximum output current. $C_{MILLER}$ can be approximated from the gate charge curve typically provided in the data sheet of the MOSFET manufacturer. $C_{MILLER}$ is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat, divided by the specified change in the voltage difference between the drain and source terminals of the MOSFET ($V_{DS}$). This result is then multiplied by the ratio of the application applied $V_{DS}$ to the gate charge curve specified $V_{DS}$. When the IC is operating in continuous mode, the duty cycles for the top and bottom FETs are given by Equation 10 and Equation 11, as follows:

$$\text{MAIN SWITCH DUTY CYCLE} = \frac{V_{OUT}}{V_{IN}} \tag{10}$$

$$\text{SYNCHRONOUS SWITCH DUTY CYCLE} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \tag{11}$$

The MOSFET power dissipations at maximum output current are given by Equation 12 and Equation 13, as follows:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \delta)\, R_{DS(ON)} + (V_{IN})^2 \left(\frac{I_{MAX}}{2}\right) (R_{DR}) (C_{MILLER}) \cdot \left[\frac{1}{V_{DRVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right] (f) \tag{12}$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \delta) R_{DS(ON)} \tag{13}$$

Where:

$P_{MAIN}$ is the power dissipation from the main switch.
$V_{DRVCC}$ is the $DRV_{CC}$ voltage.
$P_{SYNC}$ is the power dissipation from the synchronous switch.
δ is the temperature dependency of $R_{DS(ON)}$ (δ ≈ 0.005/°C).
$R_{DR}$ is the effective driver resistance at the miller threshold voltage of the MOSFET ($R_{DR}$ ≈ 2Ω).
$V_{THMIN}$ is the typical MOSFET minimum threshold voltage.

Both MOSFETs have $I^2R$ losses ($I^2R$ is the power loss equation of the MOSFETs), whereas the main N-channel equations include an additional term for transition losses, which are highest at high input voltages. For $V_{IN}$ < 20 V, the high current efficiency generally improves with larger FETs. However, for $V_{IN}$ > 20V, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower $C_{MILLER}$ provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short circuit when the synchronous switch is on close to 100% of the period.

## $C_{IN}$ and $C_{OUT}$ Selection

Note that for this section $V_{IN}$ represents ($V_{IN}$ - $V_{SS}$) and $V_{OUT}$ represents ($V_{OUT}$ – $V_{SS}$).

The selection of the input capacitance ($C_{IN}$) is usually based on the worst-case RMS current drawn through the input network (battery, fuse, or capacitor). The highest $V_{OUT} \times I_{OUT}$ product needs to be used in Equation 14 to determine the maximum RMS capacitor current requirement.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $V_{OUT}/V_{IN}$. To prevent large voltage transients, use a low effective series resistance (ESR) capacitor sized for the maximum RMS current ($I_{RMS}$). At $I_{MAX}$, the maximum RMS capacitor current is given by Equation 14, as follows:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}[(V_{OUT})(V_{IN} - V_{OUT})]^{\frac{1}{2}} \quad (14)$$

Equation 16 has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$ ($I_{OUT}$ is the output current). This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the ripple current ratings of capacitor manufacturers are often based on only 2000 hours of life. This basis makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors can be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LT7809, ceramic capacitors can also be used for $C_{IN}$. Consult the manufacturer if there is any question.

Placing a small (0.1µF to 1µF) bypass capacitor between the chip $V_{IN}$ pin and $V_{SS}$ close to the LT7809 is also suggested. An optional 1Ω to 10Ω resistor placed between $C_{IN}$ and the $V_{IN}$ pin provides further isolation from a noisy input supply.

The selection of the output capacitance ($C_{OUT}$) is driven by the ESR. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple ($\Delta V_{OUT}$) is approximated to Equation 15, as follows:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 \cdot f \cdot C_{OUT}}\right) \quad (15)$$

Where:

$f$ is the operating frequency.
$\Delta I_L$ is the ripple current in the inductor.

The output ripple is highest at maximum input voltage since $\Delta I_L$ increases with input voltage.

## Setting the Output Voltage and VOUTADJ Pin

The LT7809 output voltage is set by an external feedback resistor divider carefully placed across the output and $V_{SS}$ and the current injected into the VOUTADJ pin as shown in *Figure 40*.

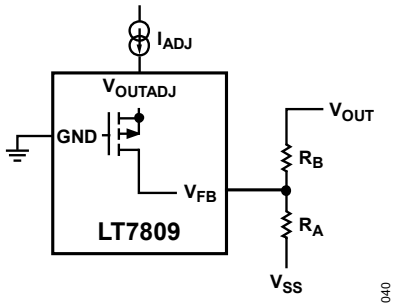



***Figure 40. Setting the Output Voltage***

The regulated output voltage is determined by Equation 16, as follows:

$$V_{OUT} = 0.8V \left(1 + \frac{R_B}{R_A}\right) + V_{SS} - I_{ADJ} \times R_B \quad (16)$$

Where:
$I_{ADJ}$ is the current sourced into the VOUTADJ pin.

The selection of $R_A$ and $R_B$ depend on the required values for $V_{OUT}$ for the $I_{ADJ}$ settings. $I_{ADJ}$ has a current range of 0µA to 100µA. $R_B$ should be calculated first based on the required $V_{OUT}$ range ($V_{OUTMAX}$ – $V_{OUTMIN}$) divided by the $I_{ADJ}$ range. $R_A$ can then be calculated using $R_B$, $V_{SS}$, and the maximum $V_{OUT}$ ($V_{OUTMAX}$). For example:

$V_{IN}$ = 100V, $V_{SS}$ = -15V, $V_{OUTMAX}$ = 80V, $V_{OUTMIN}$ = 0V

1) Calculate $R_B$ = ($V_{OUTMAX}$ – $V_{OUTMIN}$) / 100µA = 800kΩ
2) Calculate $R_A$ = 0.8V x $R_B$ / ($V_{OUTMAX}$ – $V_{SS}$ – 0.8V) = 6.79kΩ

Where;
$V_{OUTMAX}$ = $V_{OUT}$ with $I_{ADJ}$ = 0µA
$V_{OUTMIN}$ = $V_{OUT}$ with $I_{ADJ}$ = 100µA

The VOUTADJ pin can withstand voltages up to 6V (ABS MAX) with respect to GND which allows $V_{OUT}$ to be controlled with respect to $V_{SS}$ from a GND referenced source with no level shifters required.

## RUN Pin

The LT7809 is enabled using the RUN pin. The RUN pin is referenced to the GND pin, allowing the LT7809 to be used with a true ground-referenced external signal or logic with no level shifters required. The RUN pin has a rising threshold of 1.2V (with respect to the GND pin) with 120mV of hysteresis. Pulling the RUN pin below 1.08V shuts down the main control loop and resets the soft-start. Pulling the RUN pin below 0.7V disables the controller and most internal circuits, including the $DRV_{CC}$ and $INTV_{CC}$ LDO regulators. In this state, the LT7809 draws only ≈17µA of quiescent current.

The RUN pin is high impedance and must be externally pulled up, pulled down or driven directly by logic. The RUN pin can tolerate up to 140V with respect to $V_{SS}$ or the GND pin (the absolute maximum). Therefore, the pin can be conveniently tied to $V_{IN}$ in always-on applications where the controller is enabled continuously and never shuts down. Do not float the RUN pin.

The RUN pin can alternatively be configured as an undervoltage lockout on the $V_{IN}$ supply with a resistor divider from $V_{IN}$ to GND. A simple resistor divider can be used as shown in *Figure 41* to meet specific $V_{IN}$ voltage requirements.

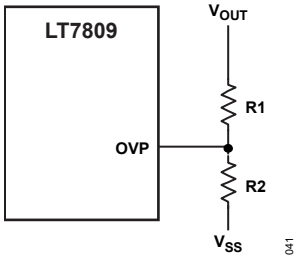



***Figure 41. Using the RUN Pin as an Undervoltage Lockout***

The $V_{IN}$ rising UVLO threshold can be calculated from Equation 17, as follows:

$$V_{IN}\ \text{UVLO Rising} = 1.2V\left(1 + \frac{R1}{R2}\right) \quad (17)$$

## Soft-Start and Tracking (TRACK/SS Pin)

The start-up of $V_{OUT}$ is controlled by the voltage on the TRACK/SS pin with respect to the $V_{SS}$ pin. When the voltage on the TRACK/SS pin is less than the internal 0.8V reference, the LT7809 regulates the $V_{FB}$ pin voltage to the voltage on the TRACK/SS pin instead of the internal reference. The TRACK/SS pin can be used to program an external soft-start function, or to allow $V_{OUT}$ to track another supply during start-up.

Soft-start is enabled by connecting a capacitor from the TRACK/SS pin to $V_{SS}$. An internal 9µA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The LT7809 regulates its feedback voltage (and hence $V_{OUT}$) according to the voltage on the TRACK/SS pin, allowing $V_{OUT}$ to rise smoothly from 0V to its final regulated value. For a desired soft-start time ($t_{SS}$), select a soft-start capacitor ($C_{SS}$) = $t_{SS}$ × 11.25nF/ms.

Alternatively, the TRACK/SS pin can be used to track another supply during start-up, as shown qualitatively in *Figure 42* and *Figure 43*. To track another supply, connect a resistor divider from the leader supply ($V_X$) to the TRACK/SS pin of the follower supply ($V_{OUT}$), as shown in *Figure 44*. During start-up, $V_{OUT}$ tracks $V_X$, according to the ratio set by the resistor divider in Equation 18, as follows:

$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \cdot \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B} \quad (18)$$

Set $R_{TRACKA} = R_A$ and $R_{TRACKB} = R_B$ for coincident tracking ($V_{OUT} = V_X$ during start-up).

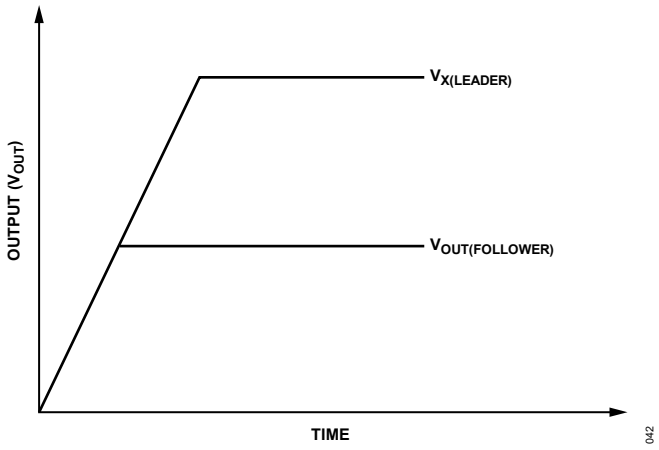



***Figure 42. Coincident Tracking***

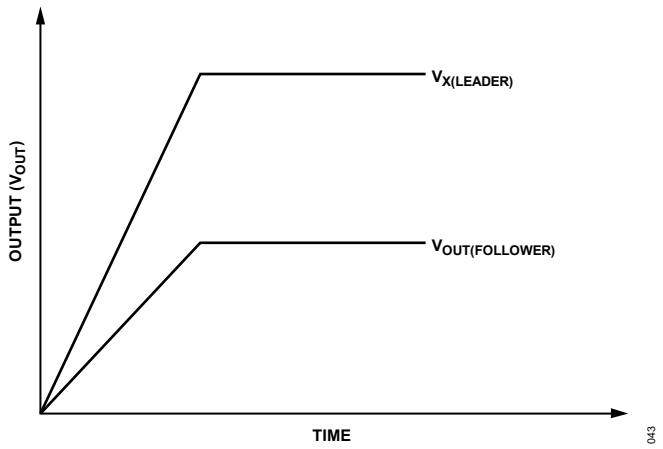



*Figure 43. Ratiometric Tracking*

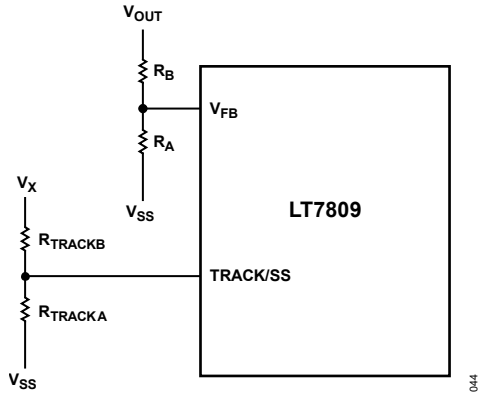



*Figure 44. Using the TRACK/SS Pin for Tracking*

## $DRV_{CC}$ and $INTV_{CC}$ Regulators

The LT7809 features two separate internal LDO linear regulators that supply power at the $DRV_{CC}$ pin from either the $V_{IN}$ pin or the $EXTV_{CC}$ pin, depending on the $EXTV_{CC}$ pin voltage. Another LDO linear regulator supplies power at the $INTV_{CC}$ pin from the $DRV_{CC}$ pin. The $DRV_{CC}$ pin is the supply pin for the MOSFET gate drivers and the $INTV_{CC}$ LDO regulator, whereas $INTV_{CC}$ pin is the supply pin for much of the LT7809 internal circuitry. The $V_{IN}$ LDO regulator and the $EXTV_{CC}$ LDO regulator regulate $DRV_{CC}$ to 9.8V (typical) with respect to $V_{SS}$. Each LDO regulator can supply a peak current of at least 100mA.

Bypass the $DRV_{CC}$ pin to $V_{SS}$ with a minimum of 4.7µF ceramic capacitor, and place it as close as possible to the $DRV_{CC}$ pin. It is recommended to place an additional 1µF ceramic capacitor next to the $DRV_{CC}$ pin and $V_{SS}$ pin to supply the high frequency transient currents required by the MOSFET gate drivers. The $INTV_{CC}$ supply must be bypassed with a 0.1µF ceramic capacitor to $V_{SS}$.

High input voltage applications in which large MOSFETs are driven at high frequencies can exceed the maximum junction temperature rating for the LT7809. The $DRV_{CC}$ current, which is dominated by the gate charge current, can be supplied by either the $V_{IN}$ LDO regulator or the $EXTV_{CC}$ LDO regulator. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (7.7V typical), the $V_{IN}$ LDO regulator is enabled. In this case, power dissipation for the IC is equal to ($V_{IN}$ – $V_{SS}$) - ($V_{DRVCC}$) × $DRV_{CC}$ current ($I_{DRVCC}$). The gate charge current is dependent on the operating

frequency, as discussed in the *Efficiency Considerations* section. To estimate the junction temperature, use the equation detailed in Note 2. For example, the LT7809 $DRV_{CC}$ current is limited to less than 20.1mA from a 100V supply ($V_{SS}$ = 0V) when not using the $EXTV_{CC}$ supply at an ambient temperature of 70°C, as shown in Equation 19 as follows:

$$T_J = 70°C + (20.1mA) \times (100V - 9.6V) \times (44°C/W) = 150°C \quad (19)$$

When the voltage applied to $EXTV_{CC}$ rises above its rising switchover threshold, the $V_{IN}$ LDO regulator turns off and the $EXTV_{CC}$ LDO regulator enables. The $EXTV_{CC}$ LDO regulator remains on as long as the voltage applied to $EXTV_{CC}$ remains above its falling switchover threshold (7.6V typical). The $EXTV_{CC}$ LDO attempts to regulate the $DRV_{CC}$ voltage to the voltage to 9.8V with respect to $V_{SS}$. Therefore, while $EXTV_{CC}$ is less than this voltage, the LDO regulator is in dropout, and the $DRV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. Using the $EXTV_{CC}$ LDO regulator allows the MOSFET driver and control power to be derived from the switching regulator output of the LT7809 during normal operation, and from the $V_{IN}$ LDO when the output is out of regulation (for example, start up or short circuit). If more current is required through the $EXTV_{CC}$ LDO than is specified, add an external Schottky diode between the $EXTV_{CC}$ and $DRV_{CC}$ pins. In this case, do not apply more than 14V to the $EXTV_{CC}$ pin with respect to $V_{SS}$.

Significant efficiency and thermal gains can be realized by powering $DRV_{CC}$ from an output because the $V_{IN}$ current resulting from the driver and control currents is scaled by a factor of $V_{OUT}/((V_{IN}) \times$ Efficiency). For 8V to 30V regulator outputs, connect the $EXTV_{CC}$ pin to $V_{OUT}$. Tying the $EXTV_{CC}$ pin to a 12V supply reduces the junction temperature in Equation 19 from 150°C to the results given by Equation 20, as follows:

$$T_J = 70°C + (20.1mA) \times (12V - 9.6V) \times (44°C/W) = 72°C \quad (20)$$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive $DRV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ connected to $INTV_{CC}$. This connection causes the $V_{IN}$ LDO regulator to power $DRV_{CC}$, resulting in an efficiency penalty of up to 10% or more at high input voltages.
2. $EXTV_{CC}$ connected directly to the regulator output. This connection is the normal connection for an application with an output range of 8V to 30V and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available, it can be used to power $EXTV_{CC}$, provided that it is compatible with the MOSFET gate drive requirements. This supply can be higher or lower than $V_{IN}$. However, a lower $EXTV_{CC}$ voltage results in higher efficiency.
4. $EXTV_{CC}$ connected to an output derived boost or charge pump. For regulators where outputs are below 8V, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output derived voltage that is boosted to greater than the $EXTV_{CC}$ switchover threshold.

## Topside MOSFET Driver Supply ($C_B$, $D_B$)

An external bootstrap capacitor, $C_B$, connected to the BOOST pin supplies the gate drive voltage for the top MOSFET. Capacitor $C_B$ in *Figure 4* is charged through an external diode $D_B$ from $DRV_{CC}$ when the bottom MOSFET is on, and SW is low.

When the top MOSFET turns on, the driver places the $C_B$ voltage across the gate source of the top MOSFET, which enhances the top MOSFET and turns on the topside switch. The switch node voltage, SW, rises to $V_{IN}$, and the BOOST pin follows. With the top MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = (V_{IN} + V_{DRVCC})$. The value of the boost capacitor, $C_B$, needs to be 100 times that of the total input capacitance of the top MOSFET. For a typical application, a value of $C_B$ = 0.1µF is sufficient. The reverse breakdown of the external diode $D_B$ must be greater than the maximum of ($V_{IN} - V_{SS}$).

## Minimum On-Time Considerations

The minimum on-time ($t_{ON(MIN)}$) is the smallest time duration that the LT7809 is capable of turning on the top MOSFET. $t_{ON(MIN)}$ is determined by internal timing delays and the gate charge required to turn on the MOSFET. Low duty cycle applications can approach this minimum on-time limit. Take care to ensure the results in Equation 21, as follows:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \cdot f} \quad (21)$$

If the duty cycle falls below what can be accommodated by the minimum on time, the controller begins to skip cycles. The output voltage continues to be regulated, but the ripple voltage and current increase. The minimum on-time for the LT7809 is approximately 60ns. However, as the peak sense voltage decreases, the minimum on time gradually increases up to about 80ns. This change is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

### NOSKIP Pin

The NOSKIP pin is an open-drain logic output that indicates if the controller is skipping cycles. This pin is high impedance when the controller is switching at full frequency and pulled to GND when the controller skips pulses (when the top gate does not turn on at the start of each switching cycle or when the bottom gate stays on at the start of each switching cycle).

The NOSKIP pin is referenced to the GND pin, allowing the LT7809 to be used with a true ground-referenced external signal or logic with no level shifters needed.

### GMADJ Pin

The GMADJ pin provides an optional feature where the $g_m$ of the EA is adjusted to track the switching frequency below 1MHz. This feature can help optimize the performance of systems that have dynamically adjusted outputs and potentially will have the clocking frequency adjusted.

Float the GMADJ pin to have a constant $g_m$ at all switching frequencies. Tie GMADJ to $V_{SS}$ to have a $g_m$ that scales from 3.2mS at 1MHz to 1.0mS at 200kHz. Tie GMADJ to $INTV_{CC}$ to have a $g_m$ that scales from 3.2mS at 1MHz to 2.3mS at 200kHz. The typical values of $g_m$ vs switching frequency are shown in *Figure 45*.

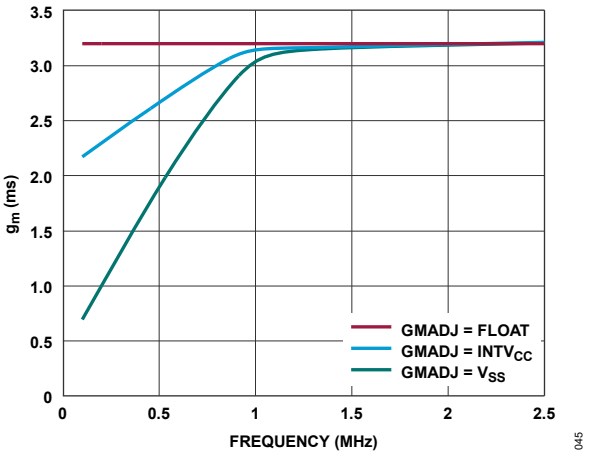



***Figure 45. Error Amplifier Transconductance versus Switching Frequency***

### REFRESHADJ Pin

As the part approaches dropout TG stays high for longer periods of time and BG pulses decrease to the minimum BG pulse width. The minimum BG pulse width is referred to as a boost refresh, as during a BG cycle the boost capacitor will recharge.

The REFRESHADJ pin can increase the minimum BG pulse width to allow more time for larger boost capacitors to recharge. Tie REFRESHADJ to $V_{SS}$ or floating or $INTV_{CC}$ to set the minimum BG pulse width to one of three different settings (95ns, 130ns or 170ns, respectively).

## Protection Features

### Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self-heating (such as a short from $DRV_{CC}$ to GND), internal overtemperature shutdown circuitry shuts down the LT7809. When the internal die temperature exceeds 180°C, the gate drivers are disabled. When the die cools to 160°C, the LT7809 resumes operation, beginning with a soft-start start-up. Avoid long-term overstress ($T_J$ > 150°C) because it can degrade the performance or shorten the life of the device.

### Current Limit and Foldback

The LT7809 includes current foldback to reduce the load current when the output is shorted to $V_{SS}$. If the output voltage falls below 40% of its regulation point, the maximum sense voltage is progressively lowered from 100% to 40% of its maximum value. Under short-circuit conditions with low duty cycles, the LT7809 begins cycle skipping to limit the short-circuit current. In this situation, the bottom MOSFET dissipates most of the power, but less than in normal operation. The short-circuit ripple current ($\Delta I_{L(SC)}$) is determined by $t_{ON(MIN)}$ ≈ 60ns, the input voltage, and the inductor value given by Equation 23, as follows:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \cdot V_{IN}/L \quad (23)$$

The resulting average short-circuit current ($I_{SC}$) is given by Equation 24, as follows:

$$I_{SC} = 40\% \cdot I_{LIM(MAX)} - \frac{\Delta I_{L(SC)}}{2} \quad (24)$$

where $I_{LIM(MAX)}$ is the maximum peak inductor current.

## Phase-Locked Loop and Frequency Synchronization

The LT7809 has an internal PLL that allows the turn on of the top MOSFET to be synchronized to the rising edge of an external clock signal applied to the PLLIN pin. The LT7809 is guaranteed to synchronize to an external clock applied to the PLLIN pin that swings up to at least 2.2V and down to 0.5V or less with respect to GND. Note that the LT7809 can only be synchronized to an external clock frequency within the range of 100kHz to 2.5MHz.

The lock time of the LT7809 PLL can be characterized by the amount of time the PLL takes to lock to a step input change in frequency of the signal applied to the PLLIN pin. The typical lock time of the LT7809 PLL to a 200kHz to a 1MHz step in synchronization frequency is 100µsec.

More rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. Before synchronization, the PLL is prebiased to the frequency set by the FREQ pin. Consequently, the PLL only needs to make minor adjustments to achieve phase lock and synchronization. Although it is not required, placing the free-running frequency near the external clock frequency prevents the oscillator from passing through a large range of frequencies as the PLL locks.

## Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. Analyzing individual losses is useful for determining what is limiting the efficiency and which change produces the most improvement. The percent efficiency can be expressed by Equation 24, as follows:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...) \quad (24)$$

where L1, L2, L3, and so on are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LT7809 circuits: IC $V_{IN}$ current, $DRV_{CC}$ regulator current, $I^2R$ losses, and top MOSFET transition losses.

1. The $V_{IN}$ current is the DC supply current given in *Table 1*, which excludes MOSFET driver and control currents. $V_{IN}$ current typically results in a small (<0.1%) loss.
2. $DRV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power FETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge ($d_Q$) moves from $DRV_{CC}$ to $V_{SS}$. The resulting $d_Q$/time duration (dt) is a current out of $DRV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, gate charge current ($I_{GATECHG}$) = SW frequency ($f_{SW}$) × ($Q_T$ + $Q_B$), where $Q_T$ and $Q_B$ are the gate charges of the top and bottom MOSFETs.

   Supplying $DRV_{CC}$ from an output derived source through $EXTV_{CC}$ scales the $V_{IN}$ current required for the driver and control circuits by a factor of $V_{OUT}/(V_{IN}$ × efficiency). For example, in a 20V to 5V application, 10mA of $DRV_{CC}$ current results in approximately 2.5mA of $V_{IN}$ current. This result reduces the mid-current loss from 10% or more (if the driver was powered directly from $V_{IN}$) to only a few percent.
3. $I^2R$ losses are predicted from the DC resistances of the input fuse (if used), MOSFET, inductor (L), current sense resistor, and input and output capacitor ESR. In continuous mode, the average output current flows through L and $R_{SENSE}$ but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, the resistance of one MOSFET can be summed with the resistances of L, $R_{SENSE}$, and capacitor ESR to obtain the $I^2R$ losses.

   For example, if each $R_{DS(ON)}$ = 30mΩ, $R_L$ = 50mΩ, $R_{SENSE}$ = 10mΩ and ESR = 40mΩ (the sum of both input and output capacitance losses), the total resistance is 130mΩ. The resulting losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of $V_{OUT}$ for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems are not doubling but quadrupling the importance of loss terms in the switching regulator system.
4. Transition losses apply only to the top MOSFETs and become significant only when operating at higher input voltages (typically 15V or greater). Transition losses can be estimated using Equation 26, as follows:

$$\text{Transition Loss} = 1.7 \times (V_{IN} - V_{ss})^2 \times I_{L(MAX)} \times C_{RSS} \times f_{SW} \quad (26)$$

Where $C_{RSS}$ is the reverse transfer capacitance.

Other hidden losses, such as copper trace and internal battery resistances, can account for an additional 5% to 10% efficiency degradation in portable systems. It is important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that $C_{IN}$ has adequate charge storage and low ESR at the switching frequency. A 25W supply typically requires a minimum of 20µF to 40µF of capacitance with a maximum of 20mΩ to 50mΩ of ESR. Other losses, including inductor core losses, generally account for less than 2% of the total additional loss.

## Checking Transient Response

To check the regulator loop response, look at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, $V_{OUT}$ shifts by an amount equal to $\Delta I_{LOAD}$ × ESR, where ESR is the effective series resistance of $C_{OUT}$. $\Delta I_{LOAD}$ also begins to charge or discharge $C_{OUT}$, generating the feedback error signal that forces the regulator to adapt to the current change and return $V_{OUT}$ to its steady-state value. During this recovery time, $V_{OUT}$ can be monitored for excessive overshoot or ringing, which indicates a stability problem.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time, and settling at this test point reflect the closed-loop response. Assuming a predominantly second order system, the phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in *Figure 47* and *Figure 49* provide an adequate starting point for most applications.

The ITH series compensation resistor ($R_C$) to compensation capacitor ($C_C$) filter sets the dominant pole zero loop compensation. The values can be modified slightly (from 0.5 times to 2 times their initial values) to optimize transient response when the final PCB layout is done and the particular output capacitor type and value are determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of the full load current, with a rise time of 1µs to 10µs, produces output voltage and ITH pin waveforms that give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across from the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop. Therefore, this signal cannot be used to determine phase margin. For this reason, it is better to look at the ITH pin signal, which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop increases by increasing $R_C$, and the bandwidth of the loop increases by decreasing $C_C$. If $R_C$ increases by the same factor that $C_C$ decreases, the zero frequency is kept the same, keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and demonstrates the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with $C_{OUT}$, causing a rapid drop in $V_{OUT}$. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage, if the load switch resistance is low and it is driven quickly. If the ratio of $C_{LOAD}$ to $C_{OUT}$ is greater than 1:50, the switch rise time must be controlled so that the load rise time is limited to approximately $C_{LOAD}$ × 25µs/µF. Therefore, a 10µF capacitor requires a 250µs rise time, limiting the charging current to about 200mA.

## Design Example

As a design example, assume the nominal input voltage $V_{IN(NOMINAL)}$ = 48V, $V_{IN(MAX)}$ = 100V, $V_{OUT}$ = 12V, $I_{OUT}$ = 4A, and $f_{SW}$ = 1MHz.

Take the following steps to design an application circuit:

1. Set the operating frequency. The frequency is not one of the internal preset values. Therefore, a resistor from the FREQ pin to GND is required, with a value given by Equation 27, as follows:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{1\text{MHz}} = 37\text{k}\Omega \quad (27)$$

2. Determine the inductor value. Initially, select a value based on an inductor ripple current of 30%. The inductor value can then be calculated using Equation 28, as follows:

$$L = \frac{V_{OUT}}{f_{SW}(\Delta I_L)}\left(1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right) = 7.5\mu H \quad (28)$$

The highest value of ripple current occurs at the maximum input voltage. In this case the ripple at $V_{IN}$ = 100V is 35%.

3. Verify the minimum on-time of 60ns is not violated. The minimum on-time occurs at $V_{IN(MAX)}$, as shown in Equation 29, as follows:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f_{SW})} = 120ns \quad (29)$$

4. This time is sufficient to satisfy the minimum on-time requirement. If the minimum on-time is violated, the LT7809 skips pulses at high input voltage, resulting in lower frequency operation and higher inductor current ripple than desired. If undesirable, this behavior can be avoided by decreasing the frequency (with the inductor value accordingly adjusted) to avoid operation near the minimum on-time.
5. Select the $R_{SENSE}$ resistor value. The peak inductor current is the maximum DC output current plus half of the inductor ripple current, or 4A + (1.2A/2) = 4.6A in this case. The $R_{SENSE}$ resistor value can then be calculated based on the minimum value for the maximum current sense threshold (45mV for ILIM = FLOAT), given by Equation 30, as follows:

$$R_{SENSE} \leq \frac{45mV}{4.6A} \cong 10m\Omega \quad (30)$$

6. To allow for additional margin, a lower value $R_{SENSE}$ can be used (for example, 8mΩ); however, be sure that the inductor saturation current has sufficient margin above $V_{SENSE(MAX)}/R_{SENSE}$, where the maximum value of 55mV is used for $V_{SENSE(MAX)}$.
7. Select the feedback resistors. If light load efficiency is required, high value feedback resistors can be used to minimize the current due to the feedback divider. However, in most applications, a feedback divider current in the range of 10µA to 100µA or more is acceptable. For a 50µA feedback divider current, $R_A$ = 0.8V/50µA = 16kΩ. $R_B$ can then be calculated as $R_B = R_A(12V/0.8V - 1)$ = 226kΩ.
8. Select the MOSFETs. The best way to evaluate MOSFET performance in a particular application is to build and test the circuit on the bench, facilitated by an LT7809 evaluation board. However, an educated guess about the application is helpful to initially select MOSFETs. Because this is a high voltage, low current application, transition losses likely dominate over $I^2R$ losses for the top MOSFET. Therefore, choose a MOSFET with lower gate charge as opposed to a lower $R_{DS(ON)}$ to minimize the combined loss terms. The bottom MOSFET does not experience transition losses, and its power loss is generally dominated by $I^2R$ losses. For this reason, the bottom MOSFET is typically chosen to be of lower $R_{DS(ON)}$ and higher gate charge than the top MOSFET.
9. Select the input and output capacitors. $C_{IN}$ is chosen for an RMS current rating of at least 2A ($I_{OUT}$/2, with margin) at temperature. $C_{OUT}$ is chosen with an ESR of 10mΩ for low output ripple. Multiple capacitors connected in parallel may be required to reduce the ESR to this level. The output ripple in continuous mode is highest at the maximum input voltage. The output voltage ripple due to ESR is approximately given by Equation 31, as follows:

$$V_{ORIPPLE} = ESR \bullet \Delta I_L = 10m\Omega^{*}1.2A = 12mV_{P-P} \quad (31)$$

On the 12V output, $12mV_{P-P}$ is equal to 0.10% of peak-to-peak voltage ripple.

10. Determine the bias supply components. Because the regulated output is greater than the $EXTV_{CC}$ switchover threshold, it can be used to bias $EXTV_{CC}$. For an 8ms soft-start, select a 0.1µF capacitor for the TRACK/SS pin. As a first pass estimate for the bias components, select the $DRV_{CC}$ capacitance $C_{DRVCC}$ = 4.7µF, $C_{INTVCC}$ = 0.1µF and $C_B$ = 0.1µF.
11. Determine and set application-specific parameters. Set the MODE pin based on the trade-off of light load efficiency and constant frequency operation. Set the PLLIN pin based on whether a fixed or phase-locked frequency is desired. The RUN pin can be used to control the minimum input voltage for regulator operation, or it can be tied to $V_{IN}$ for always-on operation. Use ITH compensation components from the typical applications as a first guess, check the transient response for stability, and modify as necessary.

## PC Board Layout Checklist

*Figure 46* shows the current waveforms present in the various branches of the synchronous regulators operating in the continuous mode.

When laying out the PCB, use the following checklist to ensure proper operation of the IC.

1. Route the BGUP and BGDN traces together and connect them as close as possible to the bottom MOSFET gate. If using gate resistors, connect the resistor connections to the MOSFET gate as close as possible to the MOSFET. Connecting BGUP and BGDN further away from the bottom MOSFET gate can cause inaccuracies in the dead time control circuit of the LT7809. Route the TGUP and TGDN traces together and connect them as close as possible to the top MOSFET gate.
2. The combined IC $V_{SS}$ pin and the $V_{SS}$ return of $C_{DRVCC}$ must return to the combined $C_{OUT}$ negative terminals. The path formed by the top N-channel MOSFET and the $C_{IN}$ capacitor must have short leads and PCB trace lengths. Connect the output capacitor's negative terminals as close as possible to the negative terminals of the input capacitor by placing the capacitors next to each other and away from the loop.
3. Connect the LT7809 $V_{FB}$ pin resistive dividers to the positive terminals of $C_{OUT}$ and the signal $V_{SS}$. Place the divider close to the $V_{FB}$ pin to minimize noise coupling into the sensitive $V_{FB}$ node. The feedback resistor connections must not be along the high current input feeds from the input capacitors.
4. Route the $SENSE^-$ and $SENSE^+$ leads together with minimum PCB trace spacing. Route these traces away from the high frequency switching nodes on an inner layer, if possible. The filter capacitor between $SENSE^+$ and $SENSE^-$ must be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.
5. Connect the $DRV_{CC}$ decoupling capacitor close to the IC, between the $DRV_{CC}$ and the power $V_{SS}$ pin. This capacitor carries the current peaks of the MOSFET drivers. Place an additional 1µF ceramic capacitor next to the $DRV_{CC}$ and $V_{SS}$ pins to help improve noise performance.
6. Keep the switching node (SW), top gate nodes (TGUP and TGDN), and boost node (BOOST) away from sensitive small signal nodes, especially from the voltage and current sensing feedback pins. All of these have large and fast-moving signals. Therefore, keep the nodes on the output side of the LT7809 and ensure they occupy the minimum PCB trace area.
7. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PCB as the input and output capacitors, with tie-ins for the bottom of the $DRV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider, and the $V_{SS}$ pin of the IC.

## PC Board Layout Debugging

Use a DC to 50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (the SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application.

The duty cycle percentage is maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame an improper PCB layout if regulator bandwidth optimization is not required.

Reduce $V_{IN}$ from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering $V_{IN}$ while monitoring the outputs to verify operation. Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TGxx, and possibly BGxx connections and the sensitive voltage and current pins. Place the capacitor across the current sensing pins next to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between $C_{IN}$, the top MOSFET, and the bottom MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate the common $V_{SS}$ path voltage pickup between these components and the $V_{SS}$ pin of the IC.

A problem that can be missed in an otherwise properly working switching regulator results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup is maintained, but the advantages of current mode control are not realized. Compensation of the voltage loop is more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor. The regulator maintains control of the output voltage.

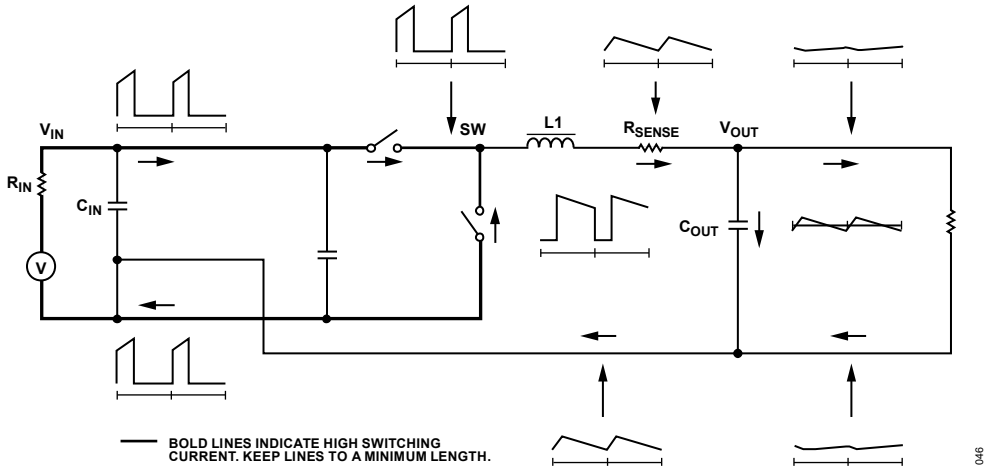



*Figure 46. Branch Current Waveforms*

## TYPICAL APPLICATIONS

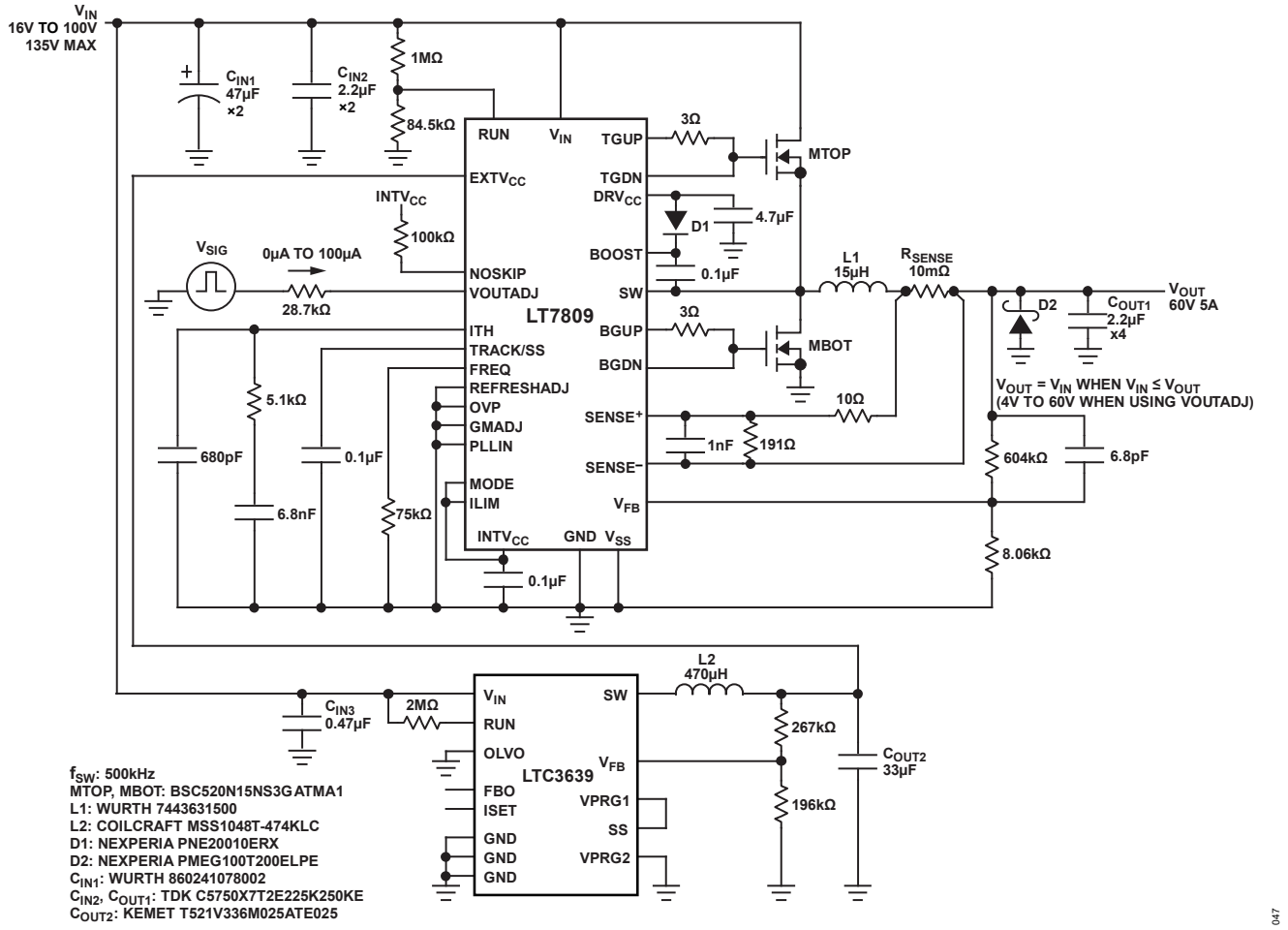



*Figure 47. Single Supply Configuration. Positive $V_{OUT}$*

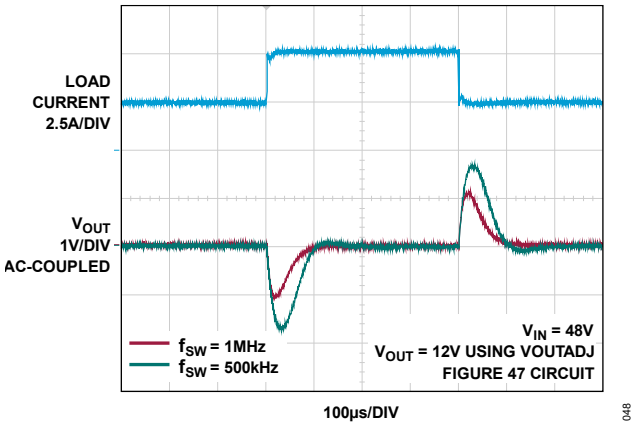



*Figure 48. Load Step Response at Different Switching Frequency*

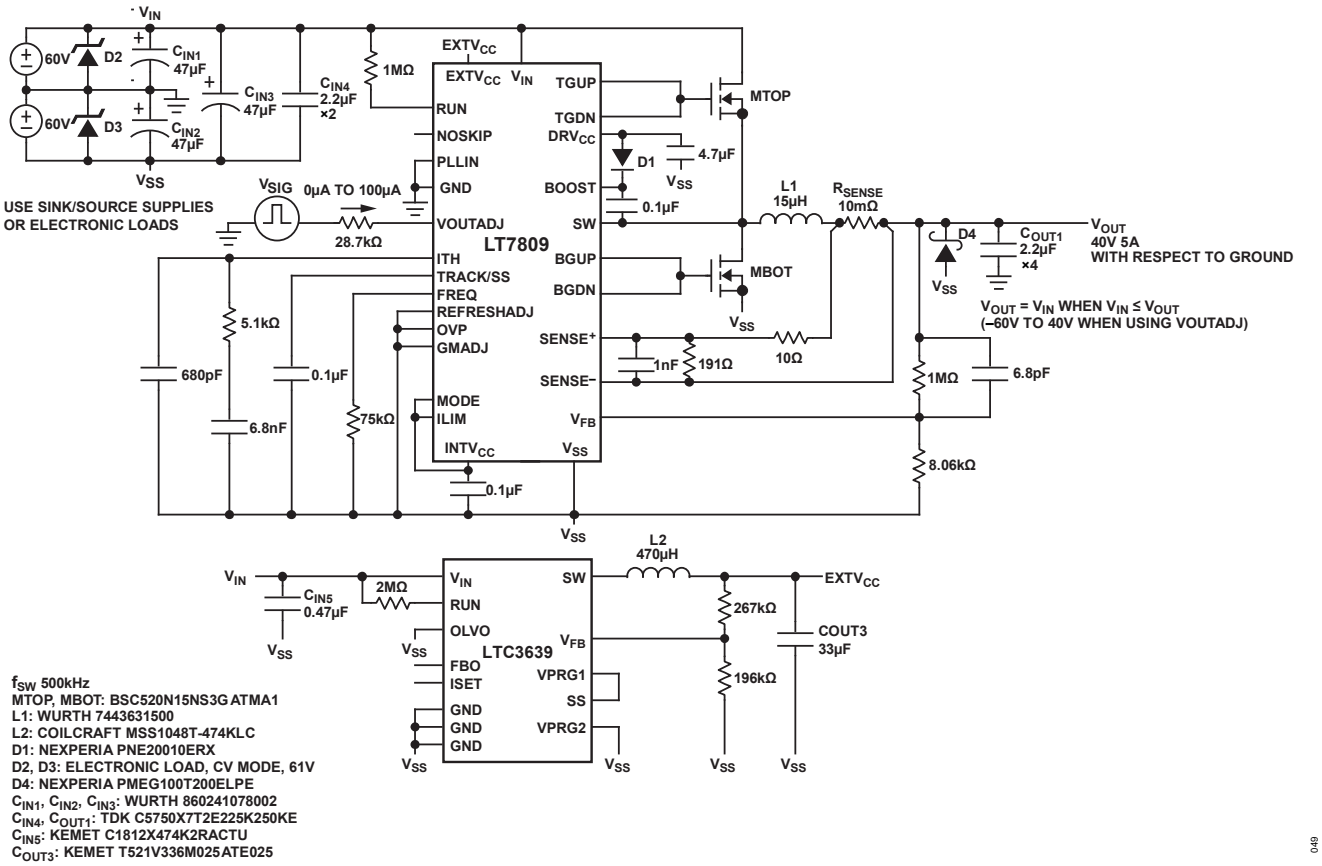



*Figure 49. Dual Supply Configuration. Negative or Positive $V_{OUT}$*

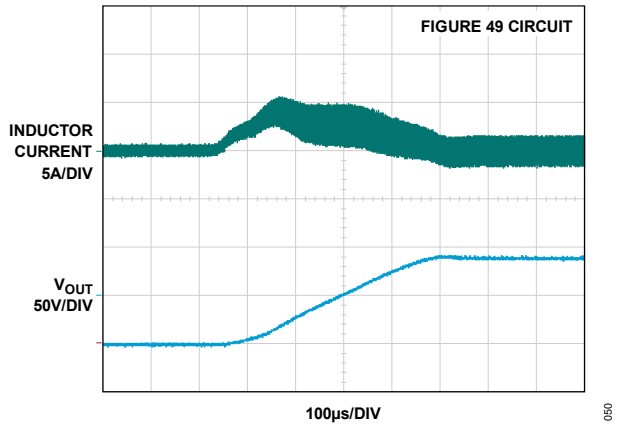


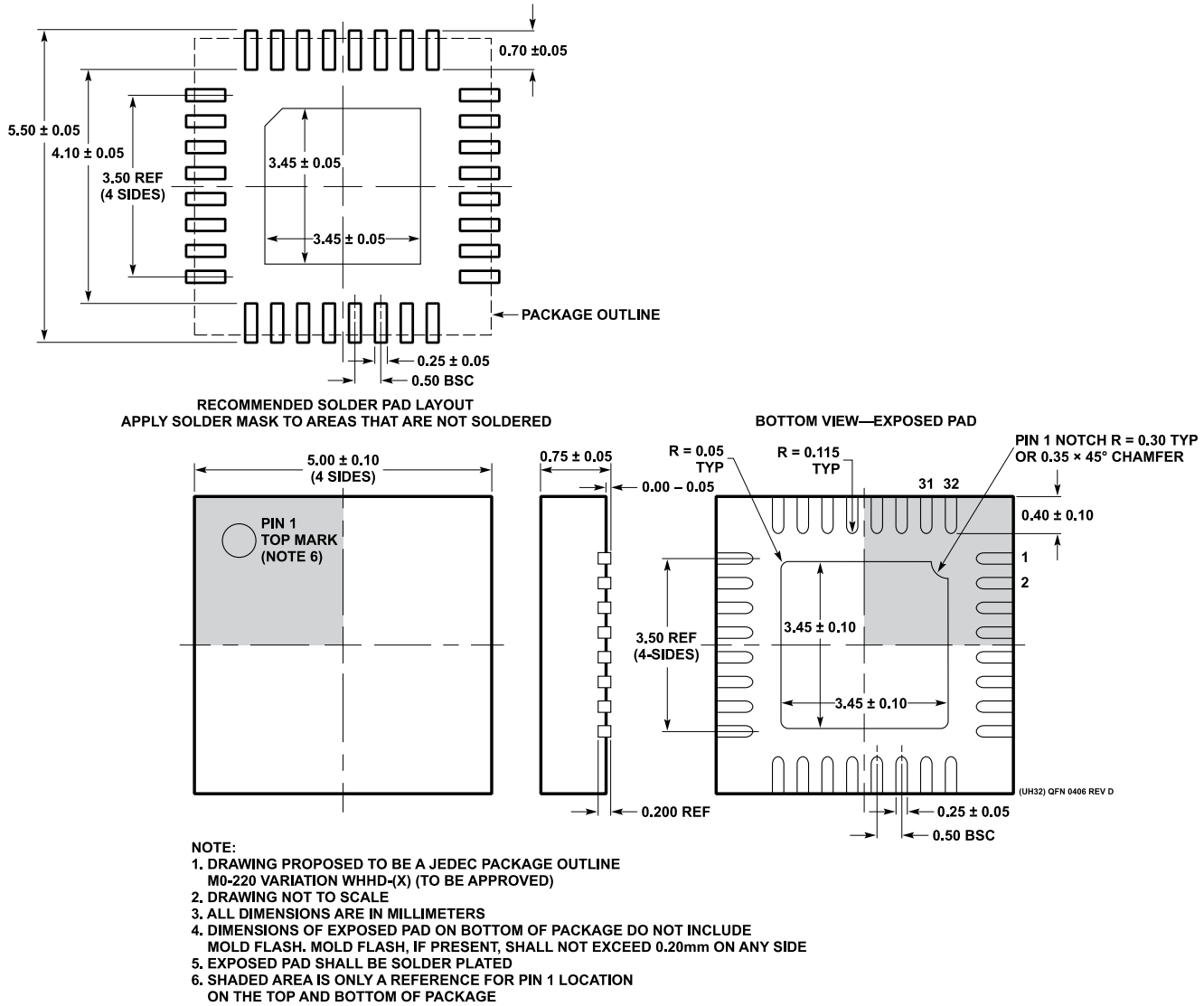

*Figure 50. $V_{OUT}$ Step from -50V to +40V using VOUTADJ*

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC3896 | 150V, Low $I_Q$, Synchronous Inverting DC/DC Controller with Ground-Referenced Control/Interface Pins | $4V \le V_{IN} \le 140V$, 150V Absolute Maximum, PLL Fixed Frequency 50kHz to 900kHz, $-0.8V \le V_{OUT} \le -60V$, Adjustable 5V to 10V Gate Drive, $I_Q = 40\mu A$ |
| LTC7810 | 150V, Low $I_Q$, Dual, 2-Phase Synchronous Step-Down DC/DC Controller with 100% Duty Cycle, 10V Gate Drive | $4.5V \le V_{IN} \le 140V$, $1V \le V_{OUT} \le 60V$, $I_Q = 110\mu A$, PLL Fixed Frequency 50kHz to 750kHz, 48-Lead, 7mm × 7mm, eLQFP Package |
| LTC7897 | 140V, Low $I_Q$, Synchronous Buck Controller with Programmable 5V to 10V Gate Drive | $4V \le V_{IN} \le 135V$, $0.8V \le V_{OUT} \le 135V$, $I_Q$: 5µA, Programmable Frequency (100kHz to 2.5MHz), 28-Pin (4mm x 5mm) QFN Package |
| LTC7899 | 140V, Low $I_Q$, Negative to Positive Synchronous Boost Controller with 10V Gate Drive | $\lvert V_{IN}\rvert + V_{OUT}$ Range = 4V to 135V Absolute Maximum, Programmable Frequency (100kHz to 2.5MHz), 28-Pin (4mm x 5mm) QFN Package |

# OUTLINE DIMENSIONS

**UH Package**
**32-Lead Plastic QFN (5mm x 5mm)**
(Reference LTC DWG # 05-08-1693 Rev D)




NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

***Figure 51. Package Description***

## ORDERING GUIDE

**Table 5. Ordering Guide**

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LT7809RUH#PBF | LT7809RUH#TRPBF | 7809 | 32-Lead (5mm x 5mm) Plastic QFN | -40°C to 150°C |

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.