**HMC905LP3E**

**6 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)**

**Typical Applications**
The HMC905LP3E is ideal for:
- LO Generation with Low Noise Floor
- Software Defined Radios
- Clock Generators
- Fast Switching Synthesizers
- Military Applications
- Test Equipment
- Sensors

**Features**
- Low Noise Floor:
  - -164 dBc/Hz at 10 MHz Offset for N = 4
- Programmable Frequency Divider, N = 1, 2, 3 or 4
- 400 MHz to 6 GHz Input Frequency Range
- Up to +6 dBm Output Power
- Sleep Mode: Consumes <1 µA
- 16 Lead 3X3 mm SMT Package: 9mm²

**General Description**
The HMC905LP3E is a SiGe BiCMOS low noise programmable frequency divider in a 3x3 mm leadless surface mount package. The circuit can be programmed to divide from N = 1 to N = 4 in the 400 MHz to 6 GHz input frequency range. The high level output power (up to 6 dBm single ended) with a very low SSB phase noise and 50% duty cycle makes this device ideal for low noise clock generation, LO generation and LO drive applications. Configurable bias and output power controls allow current consumption and output power control. The device incorporates a power down feature, good input to output isolation and fast start up time. The HMC905LP3E can be included into fast switching "ping-pong" applications.

**Functional Diagram**

**Electrical Specifications, \( T_A = +25^\circ C, Vcc = +3.3V, Z_o = 50\Omega \)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Input Characteristics</td>
<td>RF Input Frequency</td>
<td>Single-ended input</td>
<td>400</td>
<td>6000(^{[1]})</td>
<td>MHz</td>
</tr>
<tr>
<td>RF Input Power</td>
<td>Single-ended input</td>
<td>0</td>
<td>6</td>
<td>10</td>
<td>dBm</td>
</tr>
<tr>
<td>Divider Output Characteristics</td>
<td>Output Power (Single-ended Out)</td>
<td>Typically, 50 ohms load resistors connected to Vcc - 1 bit programmable (CTRL digital signal) (^{[2]})</td>
<td>-2</td>
<td>3</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>SSB Phase Noise @ 10 kHz Offset</td>
<td>+6 dBm Input Power, 6 GHz input, Single-Ended Input and Output, Divide-by-4 (^{[3]})</td>
<td>-150</td>
<td>dBc/Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SSB Phase Noise @ 100 kHz Offset</td>
<td>EN bit from OFF to ON State (0V to Vcc)</td>
<td>-158</td>
<td>dBc/Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SSB Phase Noise @ 1 MHz Offset</td>
<td>EN bit from ON to OFF State (Vcc to 0V)</td>
<td>-164</td>
<td>dBc/Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Start Up Time</td>
<td>Delay from divide ratio change to output frequency change</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power Down Time</td>
<td>Setting Time at Division Ratio Change</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

\(^{[1]}\) Maximum 5500 MHz in Divide by 2.

\(^{[2]}\) See typical supply currents vs. BIAS0, BIAS1, CTRL bits table

\(^{[3]}\) See Residual Phase Noise plot

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HMC905LP3E

6 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)

Electrical Specifications, \( T_A = +25^\circ\text{C}, Vcc = +3.3\text{V}, Z_0 = 50\Omega \) (Continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation SE Input to SE Output</td>
<td>EN bit OFF</td>
<td>-80</td>
<td>-30</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td>Duty Cycle for Differential Mode</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>

Logic Inputs

<table>
<thead>
<tr>
<th>Logic Inputs</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL Input Low Voltage</td>
<td></td>
<td>0</td>
<td>0.8</td>
<td>500</td>
<td>V</td>
</tr>
<tr>
<td>VIH Input High Voltage</td>
<td></td>
<td>1.5</td>
<td>3.3</td>
<td>7.0</td>
<td>V</td>
</tr>
</tbody>
</table>

Power Supplies

<table>
<thead>
<tr>
<th>Power Supplies</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc Analog Supply</td>
<td>Low Noise LDO for good phase noise - HMC860LP3E</td>
<td>3.15</td>
<td>3.3</td>
<td>3.45</td>
<td>V</td>
</tr>
<tr>
<td>Current Consumption</td>
<td>Total current vs. BIAS and CTRL bits [1]</td>
<td>82</td>
<td>100</td>
<td>125</td>
<td>mA</td>
</tr>
<tr>
<td>Sleep Current</td>
<td>EN = 0V</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>µA</td>
</tr>
</tbody>
</table>

[1] The bias bits combination BIAS1 BIAS0 = 1 1 is not recommended

All data plots taken on Evaluation Board (schematic on page 10) single-ended with the unused output port 50 ohms terminated, Vcc = +3.3V, Ta=+25 °C, except stated otherwise

Input Sensitivity Window

![Input Sensitivity Window Graph](image)

Residual Phase Noise Divide by 1, 2, 3 & 4 [2]

![Residual Phase Noise Graph](image)

Phase Noise for 3 Cascaded HMC905LP3E from 6 GHz VCO

![Phase Noise Graph](image)

Output Phase Noise vs. Input Power Divide-by-4

![Output Phase Noise Graph](image)

[2] Fin = 6 GHz, Pin = 6 dBm, CTRL = 1, BIAS1 BIAS0 = 01

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6 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)

Pout vs. Division Ratio

Output Power vs. Temperature Divide-by-4

Output Power vs. Input Power Level Divide-by-4

Pout Divide-by-4 vs. CTRL & BIAS

Output Power vs. Voltage Supply Divide-by-4

[1] CTRL = 0, BIAS1, BIAS0 = 00, Pin = 6 dBm

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H2, H3, H4, H5 Harmonics, Divide-by-1

H2, H3, H4, H5 Harmonics, Divide-by-2

H2, H3, H4, H5 Harmonics, Divide-by-3

H2, H3, H4, H5 Harmonics, Divide-by-4

Input to Output Isolation

[1] CTRL = 0, BIAS1 BIAS0 = 00, Pin = 6 dBm

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6 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)

**Absolute Maximum Ratings**

- **RF Input Power**: 12 dBm
- **Supply Voltage (Vcc)**: 3.6V
- **Control Inputs (B0, B1, CTRL, Bias0, EN)**: 3.6V
- **Junction Temperature**: 125 °C
- **Continuous Pdiss (T = 85 °C)**: 1.3 W
- **Thermal Resistance (Junction to ground paddle)**: 30 °C/W
- **Storage Temperature**: -65 to +125 °C
- **Operating Temperature**: -40 to +85 °C
- **ESD Sensitivity (HBM)**: Class 1A

**Programming Truth Table for Frequency Division Ratios**

<table>
<thead>
<tr>
<th>State</th>
<th>B0, B1, CTRL, Bias1, Bias0, EN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>0 to 0.8V</td>
</tr>
<tr>
<td>High</td>
<td>1.5V to 3.3V</td>
</tr>
</tbody>
</table>

**Digital Control Input Voltages**

<table>
<thead>
<tr>
<th>State</th>
<th>B0, B1, CTRL, Bias1, Bias0, EN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>0 to 0.8V</td>
</tr>
<tr>
<td>High</td>
<td>1.5V to 3.3V</td>
</tr>
</tbody>
</table>

**Typical Supply Current vs. EN, BIAS0, BIAS1 & CTRL Bits**

<table>
<thead>
<tr>
<th>EN</th>
<th>CTRL</th>
<th>BIAS1</th>
<th>BIAS0</th>
<th>3.3V Supply Typ. Current (mA)</th>
<th>Pout Typ. (dBm)</th>
<th>Noise Floor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>84</td>
<td>1.5</td>
<td>Low</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>105</td>
<td>4.8</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>98</td>
<td>3.9</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>100</td>
<td>2.4</td>
<td>Better</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>120</td>
<td>6.3</td>
<td>Best</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>113</td>
<td>5.3</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0.001</td>
<td>-55</td>
<td></td>
</tr>
</tbody>
</table>

Note: Currents for the divide-by-4 option, 2 GHz and 6 dBm input and 3.3V; for Vcc voltage supply from 3.15V to 3.45V, the HMC905LP3E total current is varying with a maximum of ~8% around typical values. With temperature, the total current is changing from +25°C to -40°C/+85°C with about ±3%.
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6 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)

Outline Drawing

Package Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package Body Material</th>
<th>Lead Finish</th>
<th>MSL Rating</th>
<th>Package Marking [1]</th>
</tr>
</thead>
<tbody>
<tr>
<td>HMC905LP3E</td>
<td>RoHS-compliant Low Stress Injection Molded Plastic</td>
<td>100% matte Sn</td>
<td>MSL1 [2]</td>
<td>905 XXX</td>
</tr>
</tbody>
</table>

NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
   PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

[1] 4-Digit lot number XXXX
# HMC905LP3E

## 6 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)

### Pin Description

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Function</th>
<th>Description</th>
<th>Interface Schematic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Vcc</td>
<td>+3.3V Voltage Supply</td>
<td>![Pin 1 Vcc Diagram]</td>
</tr>
<tr>
<td>2</td>
<td>RFINP</td>
<td>RF Positive Input. Input is DC coupled, external DC blocks required.</td>
<td>![Pin 2 RFINP Diagram]</td>
</tr>
<tr>
<td>3</td>
<td>RFINN</td>
<td>RF Negative Input. Input is DC coupled, external DC blocks required.</td>
<td>![Pin 3 RFINN Diagram]</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>This pin must be connected to RF/DC ground.</td>
<td>![Pin 4 GND Diagram]</td>
</tr>
<tr>
<td>5</td>
<td>B0</td>
<td>Division ratio (LSB) See programming truth table.</td>
<td>![Pin 5 B0 Diagram]</td>
</tr>
<tr>
<td>6</td>
<td>B1</td>
<td>Division ratio (MSB) See programming truth table.</td>
<td>![Pin 6 B1 Diagram]</td>
</tr>
<tr>
<td>7</td>
<td>CTRL</td>
<td>Divider Output Buffer Power Control</td>
<td>![Pin 7 CTRL Diagram]</td>
</tr>
<tr>
<td>13</td>
<td>BIAS1</td>
<td>Divider Core Bias Control</td>
<td>![Pin 13 BIAS1 Diagram]</td>
</tr>
<tr>
<td>14</td>
<td>BIAS0</td>
<td>Divider Core Bias Control</td>
<td>![Pin 14 BIAS0 Diagram]</td>
</tr>
<tr>
<td>15</td>
<td>EN</td>
<td>Chip Enable</td>
<td>![Pin 15 EN Diagram]</td>
</tr>
<tr>
<td>8, 9, 12, 16</td>
<td>N/C</td>
<td>No connection required. This pin may be connected to ground, without affecting performance.</td>
<td>![Pin 8-16 N/C Diagram]</td>
</tr>
</tbody>
</table>
**Pin Description (Continued)**

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Function</th>
<th>Description</th>
<th>Interface Schematic</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>IOUTN</td>
<td>Divider Negative Output, Open Drain. Typically 50 Ohms connected to Vcc.</td>
<td><img src="image" alt="Divider Circuit" /></td>
</tr>
<tr>
<td>11</td>
<td>IOUTP</td>
<td>Divider Positive Output, Open Drain. Typically 50 Ohms connected to Vcc.</td>
<td><img src="image" alt="Divider Circuit" /></td>
</tr>
</tbody>
</table>

**Application Note:**

The HMC905LP3E is a high performance RF divider. Such dividers are high gain devices with internal feedback. The device will oscillate if used with AC coupled RF inputs and if no RF input is applied. Normally, if the RF input signal is removed the device should be disabled, or it should be placed in divide by 1 mode. The device is stable in divide by one mode with no RF input. The device will oscillate in divide 2, 3, or 4 modes with no RF input. In general, very small RF input levels will stop all oscillations. At the minimum rated RF input sensitivity level or higher, no oscillations or spurious signals exist and excellent low noise performance is achieved. For input frequency lower than 400 MHz, square wave input signal is recommended.

For single ended applications, apply the signal on the positive input RFinp and terminate the unused output with 50 ohms.
**Evaluation PCB**

- The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes.
- The evaluation circuit board shown is available from Hittite upon request.

### List of Materials for Evaluation PCB 126830

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J3</td>
<td>DC Connector</td>
</tr>
<tr>
<td>J1, J4, J7, J8</td>
<td>SMA SRI Connector</td>
</tr>
<tr>
<td>C1, C2, C10 - C12, C18</td>
<td>1nF Capacitor, 0402 Pkg</td>
</tr>
<tr>
<td>C3, C6, C9</td>
<td>100nF Capacitor, 0402 Pkg</td>
</tr>
<tr>
<td>C5</td>
<td>10μF Capacitor, 1206 Pkg</td>
</tr>
<tr>
<td>C8</td>
<td>10pF Capacitor, 0402 Pkg</td>
</tr>
<tr>
<td>R1, R7</td>
<td>51 Ohms, Resistor, 0402 Pkg</td>
</tr>
<tr>
<td>R2 - R6, R9</td>
<td>100 kOhms, Resistor, 0402 Pkg</td>
</tr>
<tr>
<td>TP1, TP3, TP4</td>
<td>PC Compact SMT</td>
</tr>
<tr>
<td>U1</td>
<td>HMC905LP3E Programmable Divider</td>
</tr>
<tr>
<td>PCB</td>
<td>126828 Eval Board</td>
</tr>
</tbody>
</table>

[1] Reference this number when ordering complete evaluation PCB

Evaluation PCB Schematic

Input Voltage Range
3.15V min, 3.3V nom, 3.45 V max
Current 80mA to 125mA

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Application Support: Phone: 978-250-3343  or  apps@hittite.com