HMC705LP4 / HMC705LP4E

6.5 GHz PROGRAMMABLE DIVIDER (N = 1 - 17)

Typical Applications
The HMC705LP4(E) is ideal for:
• Satellite Communication Systems
• Point-to-Point Radios
• Military Applications
• Sonet Clock Generation
• Test Equipment

Features
Ultra Low SSB Phase Noise Floor:
-153 dBc/Hz @ 100 kHz
Programmable Divider (N = 1 - 17) Operating up to 6.5 GHz
24 Lead 4X4mm SMT Package: 16mm²

General Description
The HMC705LP4(E) is a low noise GaAs HBT programmable divider in a 4x4 mm leadless surface mount package. The divider can be programmed to divide by any number from N = 1 to N = 17 up to 6.5 GHz. The HMC705LP4E’s high frequency operation along with low phase noise floor is very useful in high performance fast settling synthesizer architectures. The HMC705LP4E may be combined with Hittite’s Phase Frequency Detectors, VCOs and PLL ICs to create low noise, fast settling phase locked loops.

Functional Diagram

Electrical Specifications, $T_A = +25°$ C, $Vcc = Vcc1 = Vcc2 = +5V$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Input Frequency</td>
<td>Sine Wave or Square Wave Input</td>
<td>6.5</td>
<td></td>
<td></td>
<td>GHz</td>
</tr>
<tr>
<td>Minimum Input Frequency</td>
<td>Sine Wave or Square Wave Input</td>
<td></td>
<td>0.1</td>
<td></td>
<td>GHz</td>
</tr>
<tr>
<td>Input Power Range</td>
<td>Fin = 0.1 to 6.5 GHz*</td>
<td>-15</td>
<td>0</td>
<td>10</td>
<td>dBm</td>
</tr>
<tr>
<td>Output Power</td>
<td>Divide-by-2</td>
<td>0</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>SSB Phase Noise</td>
<td>Fin = 6 GHz, N = 17</td>
<td>-153</td>
<td></td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>Total Supply Current</td>
<td></td>
<td>190</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

* For sine wave inputs less than 400 MHz input power must be greater than or equal to -5 dBm
**HMC705LP4 / HMC705LP4E**

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**Input Sensitivity Window, All States**

![Graph showing input sensitivity window for all states.]

**Input Sensitivity Window vs. Temperature, N = 17, T = -40°C to +85°C**

![Graph showing input sensitivity window vs. temperature for N = 17.]

**Output Power, Divide Ratio**

**States 1 through 5**

![Graph showing output power for divide ratio (N = 1 to 5).]

**States 6 through 17**

![Graph showing output power for divide ratio (N = 6 to 17).]

**Fundamental Feedthru Power, Pin = 0 dBm**

![Graph showing fundamental feedthru power level for different divide ratios.]

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**SSB Phase Noise Performance**  
*Fin = 6 GHz, N = 2; T = -40°C, +25°C, +85°C*  
![Graph showing SSB Phase Noise Performance for N = 2 at different temperatures.](image)

**SSB Phase Noise Performance**  
*Fin = 6 GHz, N = 17; T = -40°C, +25°C, +85°C*  
![Graph showing SSB Phase Noise Performance for N = 17 at different temperatures.](image)

**SSB Phase Noise Performance**  
*Fin = 6 GHz, N = 2; Vcc = 4.75V, 5V, 5.25V*  
![Graph showing SSB Phase Noise Performance for N = 2 at different Vcc values.](image)

**SSB Phase Noise Performance**  
*Fin = 6 GHz, N = 17; Vcc = 4.75V, 5V, 5.25V*  
![Graph showing SSB Phase Noise Performance for N = 17 at different Vcc values.](image)

**2nd Harmonic, N = 1 through 5**  
![Graph showing 2nd Harmonic output power for N = 1 through 5.](image)

**2nd Harmonic, N = 6 through 17**  
![Graph showing 2nd Harmonic output power for N = 6 through 17.](image)
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6.5 GHz PROGRAMMABLE DIVIDER (N = 1 - 17)

3rd Harmonic, N = 1 through 5

4th Harmonic, N = 1 through 5

5th Harmonic, N = 1 through 5

3rd Harmonic, N = 6 through 17

4th Harmonic, N = 6 through 17

5th Harmonic, N = 6 through 17
Output Voltage Waveform, $F_{in} = 500$ MHz, $N = 2$, $P_{in} = 0$ dBm, $T = 25$ °C

![Graph](image1)

Output Voltage Waveform, $F_{in} = 750$ MHz, $N = 3$, $P_{in} = 0$ dBm, $T = 25$ °C

![Graph](image2)

Output Voltage Waveform, $F_{in} = 2500$ MHz, $N = 10$, $P_{in} = 0$ dBm, $T = 25$ °C

![Graph](image3)

Output Voltage Waveform, $F_{in} = 4250$ MHz, $N = 17$, $P_{in} = 0$ dBm, $T = 25$ °C

![Graph](image4)

<table>
<thead>
<tr>
<th>$N$</th>
<th>Output Duty Cycle (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Input</td>
</tr>
<tr>
<td>2</td>
<td>50</td>
</tr>
<tr>
<td>3 - 17</td>
<td>$(1 - (2/N)) \times 100$</td>
</tr>
</tbody>
</table>

Note:

[1] Peak to peak amplitude does not change relative to $N$.
[2] Pulse duty cycle changes relative to $N$. 

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### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Input (Vcc = +5V)</td>
<td>+13 dBm</td>
</tr>
<tr>
<td>Supply Voltage (Vcc)</td>
<td>+5.5V</td>
</tr>
<tr>
<td>Logic Inputs</td>
<td>-0.5V to (0.5V + Vcc)</td>
</tr>
<tr>
<td>Junction Temperature (Tj)</td>
<td>135 °C</td>
</tr>
<tr>
<td>Continuous Pdiss (T = 85 °C)</td>
<td>2.4 W</td>
</tr>
<tr>
<td>(derate 49 mW/°C above 85 °C)</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance (Junction to ground paddle)</td>
<td>20.5 °C/W</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65 to +150 °C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40 to +85 °C</td>
</tr>
</tbody>
</table>

### Typical Supply Current vs. Vcc

<table>
<thead>
<tr>
<th>Vcc (V)</th>
<th>Icc (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.75</td>
<td>180</td>
</tr>
<tr>
<td>5.00</td>
<td>190</td>
</tr>
<tr>
<td>5.25</td>
<td>210</td>
</tr>
</tbody>
</table>

Note: HMC705LP4E will work over full voltage range above.

### Outline Drawing

**Bottom View**

**Package Information**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package Body Material</th>
<th>Lead Finish</th>
<th>MSL Rating</th>
<th>Package Marking [3]</th>
</tr>
</thead>
<tbody>
<tr>
<td>HMC705LP4</td>
<td>Low Stress Injection Molded Plastic</td>
<td>Sn/Pb Solder</td>
<td>MSL1 [1]</td>
<td>H705 XXXX</td>
</tr>
<tr>
<td>HMC705LP4E</td>
<td>RoHS-compliant Low Stress Injection Molded Plastic</td>
<td>100% matte Sn</td>
<td>MSL1 [2]</td>
<td>H705 XXXX</td>
</tr>
</tbody>
</table>

[1] Max peak reflow temperature of 235 °C
[3] 4-Digit lot number XXXX

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For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 Phone: 781-329-4700 • Order online at www.analog.com Application Support: Phone: 1-800-ANALOG-D
## Pin Description

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Function</th>
<th>Description</th>
<th>Interface Schematic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 - 6, 8, 18</td>
<td>N/C</td>
<td>The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.</td>
<td>![Interface Schematic 1]</td>
</tr>
<tr>
<td>7, 20 - 24</td>
<td>DIV1, S0 NO - N2 BYP</td>
<td>CMOS compatible input control bit Logic “LOW” = NORMAL Logic “HIGH” = INVERT</td>
<td>![Interface Schematic 2]</td>
</tr>
<tr>
<td>9, 19</td>
<td>Vcc1, Vcc2</td>
<td>Supply Voltage</td>
<td>![Interface Schematic 3]</td>
</tr>
<tr>
<td>10, 13, 14, 17</td>
<td>GND</td>
<td>These pins and package bottom must be connected to RF DC ground.</td>
<td>![Interface Schematic 4]</td>
</tr>
<tr>
<td>11</td>
<td>NFIN</td>
<td>(These pins are AC coupled and must be DC Blocked externally.)</td>
<td>![Interface Schematic 5]</td>
</tr>
<tr>
<td>12</td>
<td>FIN</td>
<td>Frequency Input Frequency Input Complement</td>
<td>![Interface Schematic 6]</td>
</tr>
<tr>
<td>15</td>
<td>NOut</td>
<td>Frequency, output complement</td>
<td>![Interface Schematic 7]</td>
</tr>
<tr>
<td>16</td>
<td>Fout</td>
<td>Frequency output</td>
<td>![Interface Schematic 8]</td>
</tr>
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</table>
### HMC705LP4(E) Programming Truth Table

<table>
<thead>
<tr>
<th>Division Ratio N</th>
<th>S0</th>
<th>N0</th>
<th>N1</th>
<th>N2</th>
<th>DIV 1</th>
<th>BYP</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
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<tr>
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<tr>
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<tr>
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<td>1</td>
<td>0</td>
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<tr>
<td>14</td>
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<td>1</td>
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<td>0</td>
<td>1</td>
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<tr>
<td>15</td>
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<td>1</td>
<td>1</td>
<td>0</td>
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<tr>
<td>16</td>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<tr>
<td>17</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

0 = Logic Low  
1 = Logic High
Evaluation PCB Circuit

- **+5V**
- **R1 10KΩ**
- **C8 1000pF**
- **C1 1000pF**
- **C2 1000pF**
- **C3 100pF**
- **C4 100pF**
- **C5 100pF**
- **C6 1000pF**
- **C7 1000pF**
- **C9 4.7uF**
- **J1**
- **J2**
- **J3**
- **J4**
- **J5**
- **J6**
- **N**
- **MUX**
- ** PACKAGE BASE **
- **GND**
- **FOUT**
- **NFOUT**
- **FIN**
- **NFFIN**

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**6.5 GHz PROGRAMMABLE DIVIDER (N = 1 - 17)**

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Evaluation PCB

List of Materials for Evaluation PCB 116993 [1]

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1 - J4</td>
<td>PCB Mount SMA Connector</td>
</tr>
<tr>
<td>J5</td>
<td>14 Position Header</td>
</tr>
<tr>
<td>J6</td>
<td>4 Position Header</td>
</tr>
<tr>
<td>R1</td>
<td>10K Ohm Resistor Network, Bissel SMD</td>
</tr>
<tr>
<td>C1, C2</td>
<td>1000 pF Capacitor, 0402 Pkg.</td>
</tr>
<tr>
<td>C3 - C5</td>
<td>100 pF Capacitor, 0402 Pkg.</td>
</tr>
<tr>
<td>C6 - C8</td>
<td>1000 pF Capacitor, 0603 Pkg.</td>
</tr>
<tr>
<td>C9</td>
<td>4.7 μF Tantalum Capacitor, Case A</td>
</tr>
<tr>
<td>U1</td>
<td>HMC705LP4(E) Programmable Divider</td>
</tr>
<tr>
<td>PCB [2]</td>
<td>116991 Eval Board</td>
</tr>
</tbody>
</table>

[1] Reference this number when ordering complete evaluation PCB


The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.
Typical Application Showing Spurious Performance

CMOS/TTL Input Characteristics

Maximum Input Logic “0” Voltage ($V_{IL\,MAXIMUM}$) = 1.1V @ 1 µA.
Minimum Input Logic “1” Voltage ($V_{IH\,MINIMUM}$) = 1.8V @ 50 µA.

Input IV characteristics for the logic inputs (S0, N0 - N2, DIVI, BYP) are shown below: