HMC311AST89

Gain Block MMIC Amplifier, DC to 6GHz

FEATURES

- P1dB output power: 15.5dBm
- Output IP3: 31.5dBm
- Gain: 16dB
- 50Ω inputs and outputs
- Industry standard, 3-lead SOT-89 package
- Included in the HMC-DK001 designer's kit

APPLICATIONS

- Cellular/PCS/3G
- Fixed wireless and WLAN
- CATV and cable modems
- Microwave radios

FUNCTIONAL BLOCK DIAGRAM

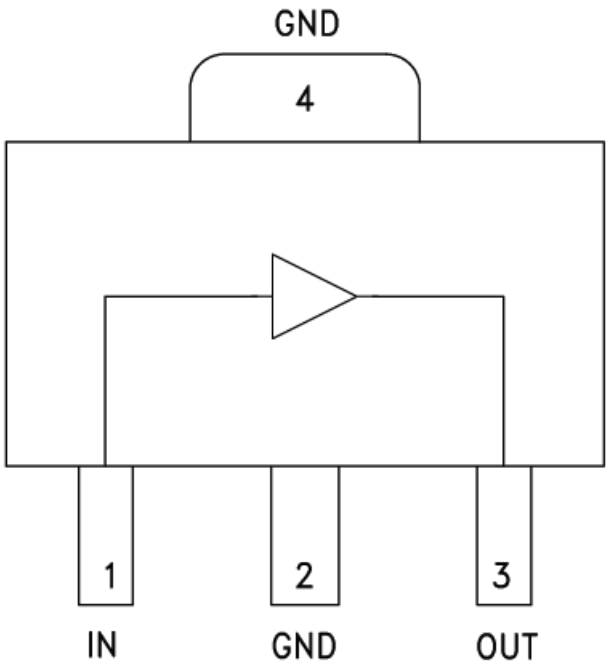

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The HMC311AST89 is a monolithic microwave IC (MMIC), surface-mounted technology (SMT), DC to 6GHz amplifier. Packaged in an industry standard SOT89E, the amplifier can be used as either a cascadable 50Ω gain stage or to drive the LO of Analog Devices, Inc., mixers with up to a 16.5dBm output power. The HMC311AST89 offers 16dB of gain and an output IP3 of 31.5dBm while requiring only 54mA from a 5V supply. The Darlington feedback pair used results in reduced sensitivity to normal process variations and yields excellent gain stability over temperature while requiring a minimal number of external bias components.

One Analog Way, Wilmington, MA 01887-2356, U.S.A.

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_S = 5V, R_{BIAS} = 22Ω, T_A = 25°C, unless otherwise noted.

Data taken with broadband bias tee on device output.

Table 1. Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN	DC to 1.0GHz	14.0	16.0		dB
	1.0GHz to 4.0GHz	13.0	15.0		dB
	4.0GHz to 6.0GHz	12.5	14.5		dB
GAIN VARIATION OVER TEMPERATURE	DC to 2.0GHz		0.004	0.007	dB/°C
	2.0GHz to 4.0GHz		0.007	0.012	dB/°C
	4.0GHz to 6.0GHz		0.012	0.016	dB/°C
RETURN LOSS INPUT AND OUTPUT	DC to 2.0GHz		8		dB
	2.0GHz to 5.0GHz		7		dB
	5.0GHz to 6.0GHz		8		dB
REVERSE ISOLATION	DC to 6GHz		20		dB
OUTPUT POWER FOR 1dB COMPRESSION (P1dB)	DC to 2.0GHz	13.5	15.5		dBm
	2.0GHz to 4.0GHz	12.0	15.0		dBm
	4.0GHz to 6.0GHz	10.0	13.0		dBm
OUTPUT THIRD-ORDER INTERCEPT (IP3)	DC to 1.0GHz		31.5		dBm
	1.0GHz to 2.0GHz		30		dBm
	2.0GHz to 4.0GHz		27		dBm
	4.0GHz to 6.0GHz		24		dBm
NOISE FIGURE	DC to 4GHz		4.5		dB
	4.0GHz to 6.0GHz		5		dB
SUPPLY CURRENT (I_{CQ})			55	74	mA

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

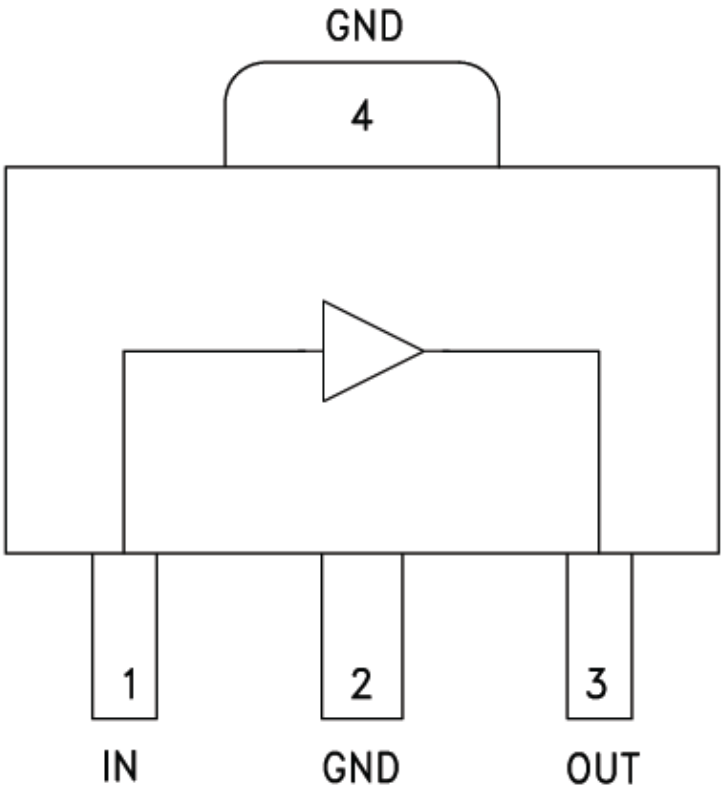

Figure 2. Pin Configuration

Table 2. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	RFIN	RF Input. The RFIN pin is DC-coupled. An off-chip DC blocking capacitor is required.
2, 4	GND	Ground. The GND pins and package bottom must be connected to RF and DC ground.
3	RFOUT	RF Output and DC Bias for the Output Stage.

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
RK-3	SOT-89	3-Lead Small Outline Transistor Package

For the latest package outline information and land patterns (footprints), go to Package Index.