

Isolated ADC with Sigma-Delta Modulated Bit Stream Output

FEATURES

- ▶ 5MHz to 50MHz main clock input frequency
- ▶ 16 bits, no missing codes
- ▶ Full-scale analog input voltage range: $\pm 320\text{mV}$
- ▶ SNR: 88dB typical
- ▶ High isolation common-mode transient immunity: $200\text{kV}/\mu\text{s}$ minimum
- ▶ Offset drift vs. temperature: $\pm 0.60\mu\text{V}/^\circ\text{C}$ maximum
- ▶ Gain error drift vs. temperature: $\pm 28\text{ppm}/^\circ\text{C}$ maximum
- ▶ Integrated digital isolator
- ▶ Operating temperature range: -40°C to $+125^\circ\text{C}$
- ▶ Wide-body SOIC
 - ▶ 8-lead SOIC_IC
- ▶ Safety and regulatory approvals
 - ▶ UL 1577 (pending)
 - ▶ $V_{\text{ISO}} = 5700\text{V}$ rms for 1minute
 - ▶ IEC/EN/CSA 62368-1 (pending)
 - ▶ IEC/CSA 61010-1 (pending)
- ▶ DIN EN IEC 60747-17 (VDE 0884-17) (pending)
 - ▶ $V_{\text{IORM}} = 2121\text{V}$ peak

APPLICATIONS

- ▶ Shunt current monitoring
- ▶ AC motor controls
- ▶ Power and solar inverters
- ▶ Wind turbine inverters
- ▶ Analog-to-digital and opto-isolator replacement

GENERAL DESCRIPTION

The ADuM7811 is a high-performance isolated analog-to-digital converter (ADC) with a second-order Σ - Δ modulator that converts an analog input signal into a high speed, single-bit data stream, with on-chip digital isolation based on Analog Devices, Inc., *iCoupler*® technology. The device operates from a 4.0V to 5.5V power supply range (high-side supply voltage, V_{DD1}) and accepts a pseudodifferential input signal of $\pm 250\text{mV}$ ($\pm 320\text{mV}$ full-scale). The pseudodifferential input is ideally suited for shunt-resistor current monitoring in high voltage applications where galvanic isolation is required.

The analog input is continuously sampled by a high-performance analog modulator and converted to a pulse density modulation digital output stream with a data rate of up to 51MHz. The analog input can be reconstructed with an appropriate sinc3 digital filter to achieve an 88dB signal-to-noise ratio (SNR) at 195.3kSPS with a 256 decimation rate and a 50MHz input clock. The serial input and output operates from a 3V to a 5.5V supply (controller-side supply voltage, V_{DD2}).

The serial interface is digitally isolated. High speed complementary metal-oxide semiconductor (CMOS) technology, combined with monolithic transformer technology, results in the on-chip isolation providing outstanding performance characteristics, superior to alternatives such as optocoupler devices.

The ADuM7811 device is available in a 8-lead SOIC_IC and has an operating temperature range of -40°C to $+125^\circ\text{C}$.

FUNCTIONAL BLOCK DIAGRAM

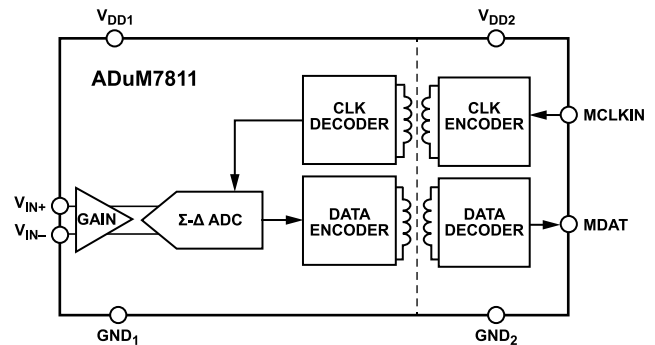


Figure 1. ADuM7811 Functional Block Diagram

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REVISION HISTORY**4/2026—Revision 0: Initial Version**

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD1} = 4.0V to 5.5V, V_{DD2} = 3.0V to 5.5V, V_{IN+} = -250mV to +250mV, V_{IN-} = 0V, T_A = -40°C to +125°C, maximum MCLKIN frequency (f_{MCLKIN}) = 40MHz, tested with a sinc3 filter, and a 256 decimation rate, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE¹						
Resolution		16			Bits	Filter output truncated to 16 bits
Integral Nonlinearity	INL		±2	±3	LSB	
Differential Nonlinearity ²	DNL			±0.99	LSB	No missed codes to 16 bits
Offset Error ²			±50	±110	µV	Initial at T_A = 25°C
Offset Error Drift vs. Temperature ²			±50	±110	µV	
Offset Error Drift vs. Temperature ²			±0.30	±0.60	µV/°C	
Gain Error ²			±0.02	±0.20	% FSR	Initial at T_A = 25°C
Gain Error Drift vs. Temperature ²			±12.5	±28	ppm/°C	
ANALOG INPUT						
Input Voltage Range		-320		+320	mV	Full-scale range
Input Common-Mode Voltage Range		-250		+250	mV	For specified performance
Input Common-Mode Voltage Range			-0.2 to +0.8		V	
Dynamic Input Current			±0.15	±0.5	µA	V_{IN+} = ±250mV, V_{IN-} = 0V
Input Capacitance ²	C_{IN}		90		pF	
DYNAMIC SPECIFICATIONS¹						
Signal-to-Noise and Distortion Ratio	SINAD	82	88		dB	F_{IN} = 1kHz
Signal-to-Noise Ratio	SNR	83	88		dB	
Total Harmonic Distortion	THD		-109	-95	dB	
Peak Harmonic or Spurious-Free Dynamic Range Noise	SFDR		-99		dB	
Effective Number of Bits	ENOB	13.3	14.3		Bits	For more details, see the Digital Filter section
ISOLATION COMMON-MODE TRANSIENT IMMUNITY¹						
	CMTI	200			kV/µs	Common-mode voltage ($ V_{CM} $) = 1kV
LOGIC INPUTS (MCLK)						
Input High Voltage	V_{IH}	$0.7 \times V_{DD2}$			V	CMOS with Schmitt trigger
Input Low Voltage	V_{IL}			$0.3 \times V_{DD2}$	V	
Input Current	I_{IN}			±0.6	µA	
Input Capacitance ²	C_{IN}		5		pF	
LOGIC OUTPUTS (MDAT)						
Output High Voltage	V_{OH}	$V_{DD2} - 0.4$	$V_{DD2} - 0.2$		V	Output current (I_{OUT}) = -4mA
Output Low Voltage	V_{OL}		0.2	0.4	V	I_{OUT} = 4mA
POWER REQUIREMENTS						
High-Side Supply Voltage ²	V_{DD1}	4.0		5.5	V	
Controller-Side Supply Voltage ²	V_{DD2}	3.0		5.5	V	
High-Side Supply Current	I_{DD1}		17.4	21	mA	F_{MCLK} = 50MHz
Controller-Side Supply Current	I_{DD2}		6.3	8	mA	V_{DD2} = 4.5V to 5.5V, C_{Load} = 25pF
			4.9	6	mA	V_{DD2} = 3.0V to 3.6V, C_{Load} = 25pF
Power Dissipation (Controller-Side + High-Side)			130	160	mW	V_{DD2} = 4.5V to 5.5V, C_{Load} = 25pF
			113	140	mW	V_{DD2} = 3.0V to 3.6V, C_{Load} = 25pF

¹ See the [Terminology](#) section.

² These specifications are guaranteed by design and characterization.

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TIMING SPECIFICATIONS

$V_{DD1} = 4.0V$ to $5.5V$, $V_{DD2} = 3.0V$ to $5.5V$, and $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Sample tested during initial release to ensure compliance. It is recommended to read MDAT on the MCLKIN rising edge.

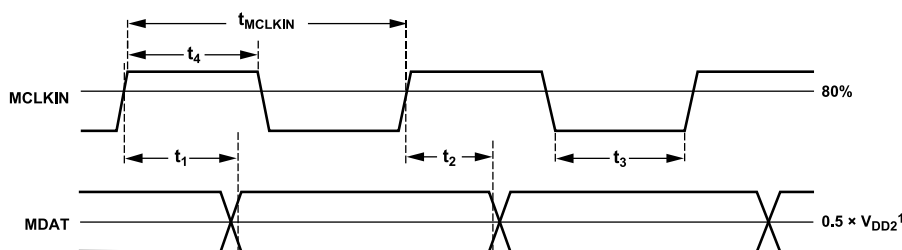
Table 2. Timing Characteristics

Parameter	Limit at T_{MIN} , T_{MAX}			Unit	Description
	Min	Typ	Max		
f_{MCLKIN}	5	40	51	MHz	Main clock input frequency
t_{MCLKIN}	19.6	25	200	ns	Main clock input period
t_1^1			10	ns	Data access time after MCLKIN rising edge
t_2^1	3			ns	Data hold time after MCLKIN rising edge
t_3	$0.4 \times t_{MCLKIN}$		$0.6 \times t_{MCLKIN}$	ns	Main clock low time
t_4	$0.4 \times t_{MCLKIN}$		$0.6 \times t_{MCLKIN}$	ns	Main clock high time
Data Latency ²			36	MCLKIN cycles	Internal Data Latency

¹ Defined as the time required from an 70% MCLKIN rising input level to when the MDAT output crosses $0.3 \times V_{DD2}$ or $0.7 \times V_{DD2}$ transitioning to the next value, as shown in Figure 2. Measured with a 25pF load capacitance.

² This specification is guaranteed by design and characterization.

Timing Diagram



¹SEE NOTE 1 OF TABLE 2 FOR FURTHER DETAILS.

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Figure 2. Data Timing Diagram

INSULATION SPECIFICATIONS

The ADuM7811 is suitable for safe electrical insulation only within the safety limiting ratings. Compliance with the safety limiting ratings shall be ensured by means of suitable protective circuits.

Table 3. ADuM7811, 8-Lead Standard Small Outline Package [SOIC_IC] (RI-8-1) Insulation Characteristics

Parameter	Symbol	Value	Unit	Test Conditions/Comments
GENERAL				
Minimum External Clearance Distance	CLR	8.3	mm	Measured from input terminals to output terminals, shortest distance through air per IEC 60664-1
Minimum External Creepage Distance	CRP	8.3	mm	Measured from input terminals to output terminals, shortest distance along body per IEC 60664-1
Distance Through Insulation	DTI	34	μm	Minimum internal
Comparative Tracking Index	CTI	>600	V	Per IEC 60112
Material Group	I			Per IEC 60664-1
Overtoltage Category per IEC 60664-1	I to IV			Rated mains voltage $\leq 600V$ rms
	I to III			Rated mains voltage $\leq 1000V$ rms
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T_S	150	$^{\circ}C$	Maximum ambient temperature for isolation barrier safety

SPECIFICATIONS

Table 3. ADuM7811, 8-Lead Standard Small Outline Package [SOIC_IC] (RI-8-1) Insulation Characteristics (Continued)

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Maximum Junction Temperature, Safety	$T_{JMAX,S}$	150	°C	Maximum junction temperature for isolation barrier safety
Maximum Total Power Dissipation	P_{TOT}	1.38	W	$T_A \leq 25^\circ\text{C}$, $P_{TOT} = P_{SI} = P_{SO}$
Derating Above Ambient (T_A)		11.0	mW/°C	$T_A > 25^\circ\text{C}$, see Figure 3
Junction-to-Air Thermal Impedance	θ_{JA}	90.6	°C/W	For more details, see the Thermal Characteristics section
IEC 60747-17 (REINFORCED INSULATION)				
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	2121	V peak	AC voltage, end of life test, $f = 60\text{Hz}$
Maximum Isolation Working Voltage	V_{IOWM}	1500	V rms	
		2121	V peak	DC voltage
Maximum Transient Isolation Voltage	V_{IOTM}	8000	V peak	$V_{TEST} \geq 1.2 \times V_{IOTM}$, $t = 1\text{s}$ (100% production)
Maximum Impulse Voltage	V_{IMP}	8000	V peak	Surge voltage in air, waveform per IEC 61000-4-5
Maximum Surge Isolation Voltage	V_{IOSM}	12800	V peak	$V_{TEST} \geq 1.3 \times V_{IMP}$ minimum 10kV (type test), tested in oil, waveform per IEC 61000-4-5
Apparent Charge	q_{pd}	≤ 5	pC	Method a (sample test), $V_{ini} = V_{IOTM}$, $t_{ini} = 60\text{s}$, $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_m = 10\text{s}$
				Method b1 (100% production), $V_{ini} \geq 1.2 \times V_{IOTM}$, $t_{ini} = 1\text{s}$, $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_m = 1\text{s}$
Resistance (Input to Output) ¹	R_{IO}	$>10^{12}$	Ω	$T_A = 25^\circ\text{C}$, $V_{TEST} = 500\text{V DC}$, $t = 60\text{s}$
	$R_{IO,S}$	$>10^9$	Ω	$T_A = T_S$, $V_{TEST} = 500\text{V DC}$, $t = 60\text{s}$
Capacitance (Input to Output) ¹	C_{IO}	1.0	pF	$f_{TEST} = 1\text{MHz}$
Climatic Category		40/125/21		
Pollution Degree		2		Per IEC 60664-1
UL 1577				
Maximum Withstanding Isolation Voltage	V_{ISO}	5700	V rms	$V_{TEST} = 1.2 \times V_{ISO}$, $t = 1\text{s}$ (100% production)

¹ Device measured as a 2-terminal device with Pin 1 to Pin 4 connected and Pin 5 to Pin 8 connected.

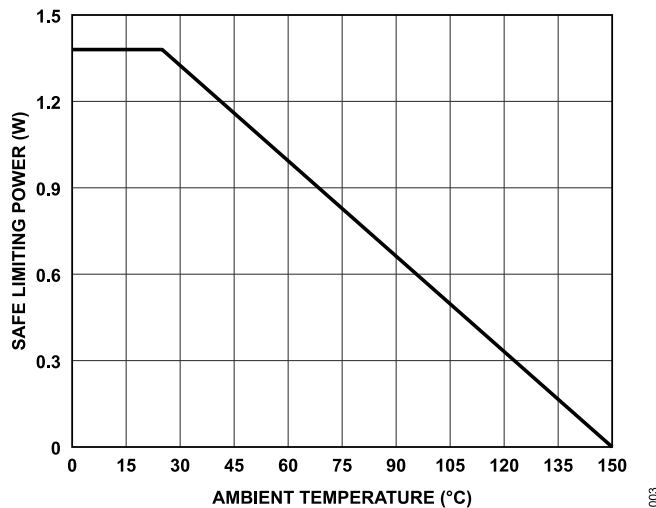


Figure 3. Thermal Derating Curve for 8-Lead Standard Small Outline Package [SOIC_IC] (RI-8-1), Dependence of Safety Limiting Power with Ambient Temperature per IEC 60747-17

SPECIFICATIONS

REGULATORY INFORMATION

The ADuM7811 RI-8-1 has been approved by the organizations listed in [Table 4](#). Copies of the relevant certificates are available at [Safety and Regulatory Certifications for Digital Isolation](#).

Table 4. ADuM7811, 8-Lead Standard Small Outline Package [SOIC_IC] (RI-8-1) Package Certifications

Regulatory Agency	Safety Standard/Rating	Certificate Number
UL	UL 1577 component recognition program: Single protection, 5700V rms isolation voltage	E214100
CSA ¹	CSA/EN/IEC 62368-1: Basic insulation ² at 1000V rms Reinforced insulation at 600V rms	Pending
	CSA/IEC 61010-1: Basic insulation at 1000V rms Reinforced insulation at 600V rms	Pending
VDE	IEC 60747-17: Reinforced insulation at 2121V peak	Pending

¹ Working voltages are quoted for Pollution Degree 2, Material Group I and Overvoltage Category II except where otherwise specified. ADuM7811 case material has been evaluated by CSA as Material Group I.

² Working voltages are quoted for Pollution Degree 2, Material Group I, and Overvoltage Category III.

RECOMMENDED OPERATING CONDITIONS

Table 5. Recommended Operating Conditions

Parameter	Rating
Ambient Operating Temperature (T_A)	-40°C to +125°C
Supply Voltages	
V_{DD1} to GND ₁	4.0V to 5.5V
V_{DD2} to GND ₂	3.0V to 5.5V
Input/Output Signal Voltage	
V_{IN+} , V_{IN-} to GND ₁	-320mV to +320mV
V_{IN+} to V_{IN-}	-320mV to +320mV
MCLKIN to GND ₂	0V to V_{DD2}
MDAT to GND ₂	0V to V_{DD2}

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted. All voltages are relative to their respective GND_x .

Table 6. Absolute Maximum Ratings

Parameter	Rating
Supply Voltages	
V_{DD1} to GND_1	-0.3V to +6V
V_{DD2} to GND_2	-0.3V to +6V
Input/Output Voltage	
Analog Input Voltage to GND_1	-1V to +1.9V
Digital Input Voltage to GND_2 (MCLK)	-0.3V to $V_{DD2} + 0.3\text{V}$
Digital Output Voltage to GND_2 (MDAT)	-0.3V to $V_{DD2} + 0.3\text{V}$
Input Current to Any Pin Except Supplies ¹	$\pm 10\text{mA}$
Average Output Current from Any Pin Except Supplies	$\pm 10\text{mA}$
Temperature	
Ambient Operating (T_A)	-40°C to $+125^\circ\text{C}$
Storage Range (T_{ST})	-65°C to $+150^\circ\text{C}$
Junction (T_J Maximum)	150°C
Pb-Free, Soldering	
Reflow	260°C

¹ Transient currents of up to 100mA do not cause silicon controlled rectifier (SCR) to latch up.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to the PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JB} is the junction-to-board thermal resistance.

Thermal resistance and characterization parameter values specified in Table 7 are defined and calculated based on the JEDEC JESD51 standards. For more details on their definition and usage, see JEDEC JESD51-12 and the [Thermal Analysis](#) section.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	Ψ_{JB}	Ψ_{JT}	Unit
RI-8-1 ¹	90.6	89	58	6.1	$^\circ\text{C}/\text{W}$

¹ Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no vias and still air.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field-induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADuM7811

Table 8. ADuM7811, 8-Lead SOIC_IC (RI-8-1)

ESD Model	Withstand Threshold (V)	Class
HBM	± 4000	3A
FICDM	± 1250	IV

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

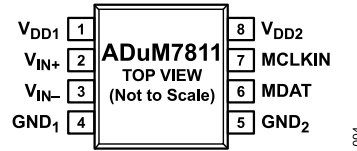


Figure 4. ADuM7811, Pin Configuration

Table 9. ADuM7811, Pin Function Descriptions

Pin Number	Mnemonic	Description
1	V _{DD1}	High-Side Supply Voltage, 4V to 5.5V. This pin is the supply voltage for the high-side of the ADuM7811 and is relative to GND ₁ . For device operation, connect the supply voltage to Pin 1. Decouple the supply pin to GND ₁ with a 10µF capacitor in parallel with a 100nF capacitor.
2	V _{IN+}	Positive Analog Input channel.
3	V _{IN-}	Negative Analog Input channel.
4	GND ₁	Ground 1. This pin is the ground reference point for all circuitry on the high side.
5	GND ₂	Ground 2. This pin is the ground reference point for all circuitry on the controller side.
6	MDAT	Serial Data Output. The single-bit modulator output is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the MCLKIN input and are valid on the following MCLKIN rising edge.
7	MCLKIN	Main Clock Logic Input. 5MHz to 50MHz frequency range. The bit stream from the modulator is propagated on the rising edge of the MCLKIN.
8	V _{DD2}	Controller-Side Supply Voltage, 3V to 5.5V. This pin is the supply voltage for the controller side and is relative to GND ₂ . Decouple this supply to GND ₂ with a 10µF capacitor in parallel with a 100nF capacitor as close to the pin as possible.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{V}$, $V_{DD2} = 5\text{V}$, $V_{IN+} = -250\text{mV}$ to $+250\text{mV}$, $V_{IN-} = 0\text{V}$, and $f_{MCLKIN} = 40\text{MHz}$, using a sinc3 filter with a 256 oversampling ratio (OSR), unless otherwise noted.

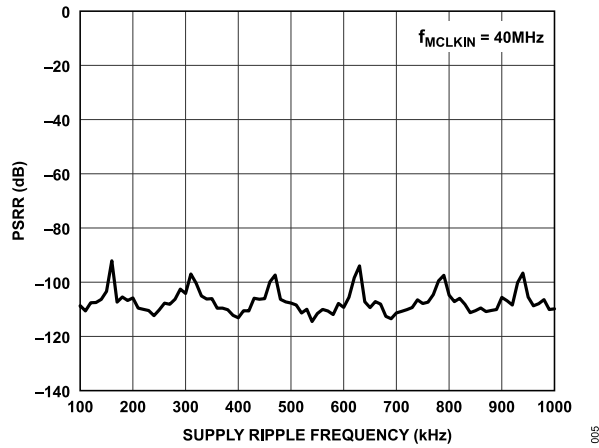


Figure 5. Power-Supply Rejection Ratio (PSRR) vs. Supply Ripple Frequency

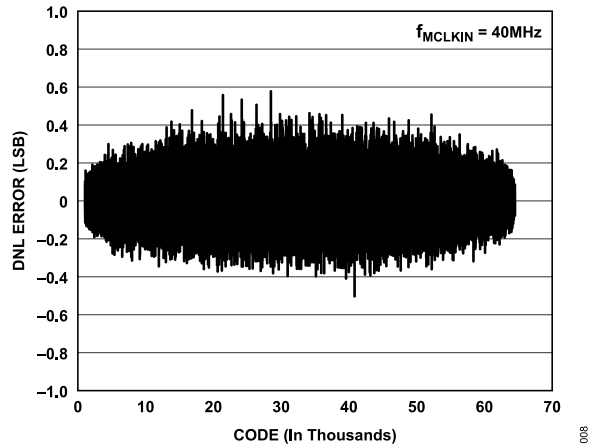


Figure 8. Typical DNL Error

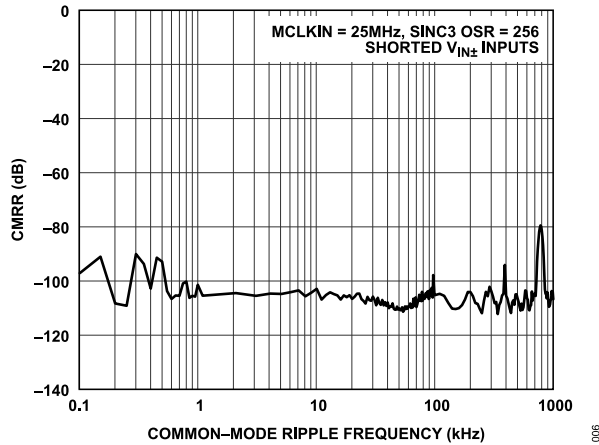


Figure 6. Common-Mode Rejection Ratio (CMRR) vs. Common-Mode Ripple Frequency

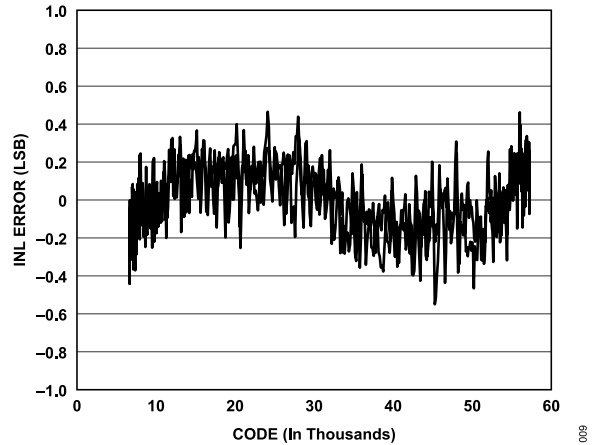


Figure 9. Typical INL Error

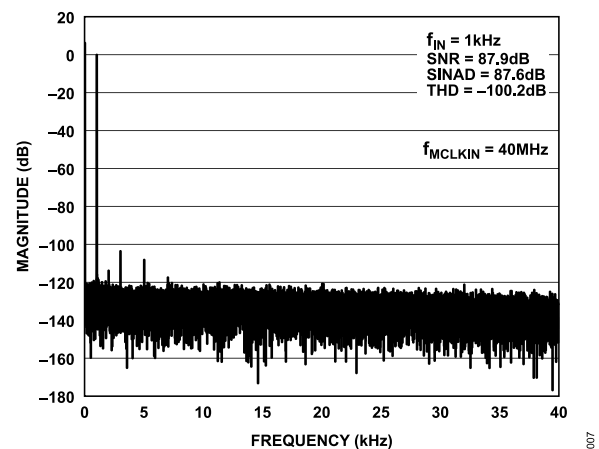


Figure 7. Typical Fast Fourier Transform (FFT)

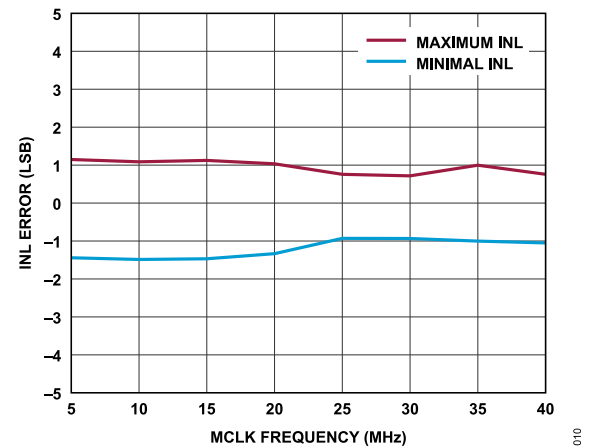


Figure 10. INL Error vs. MCLK Input Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

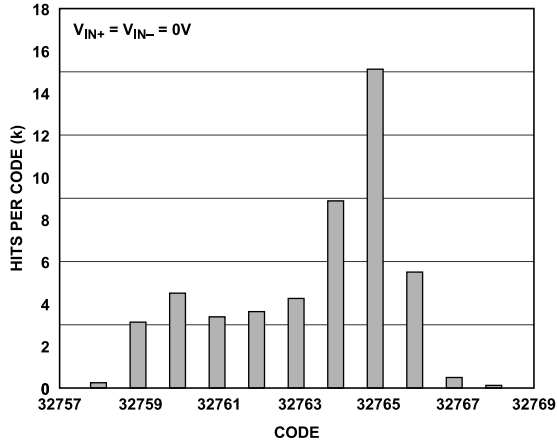


Figure 11. Histogram of Codes at the Code Center

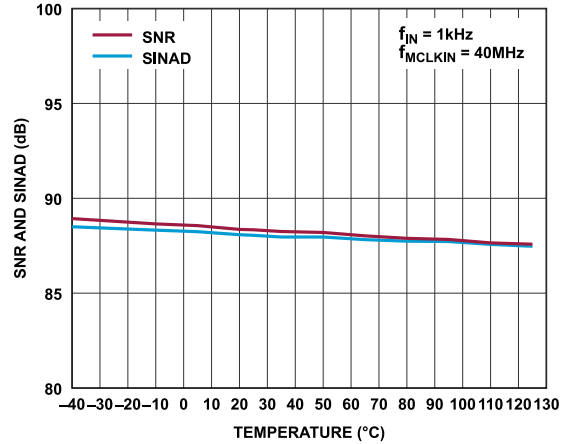


Figure 14. SNR and SINAD vs. Temperature

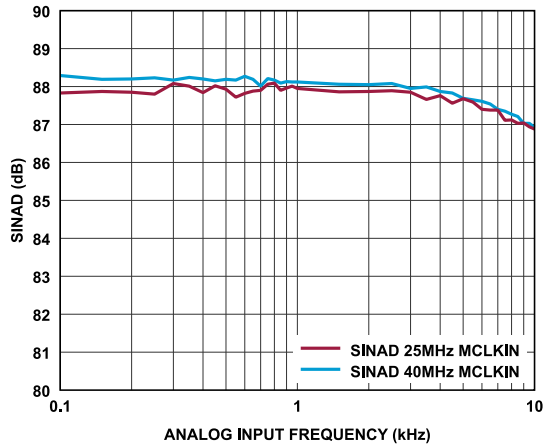


Figure 12. SINAD vs. Analog Input Frequency

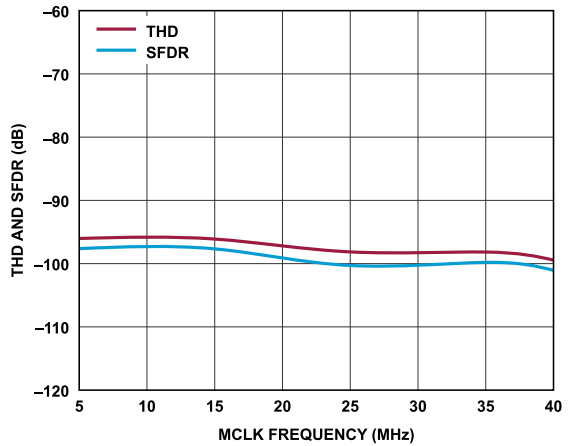


Figure 15. THD and SFDR vs. MCLK Input Frequency

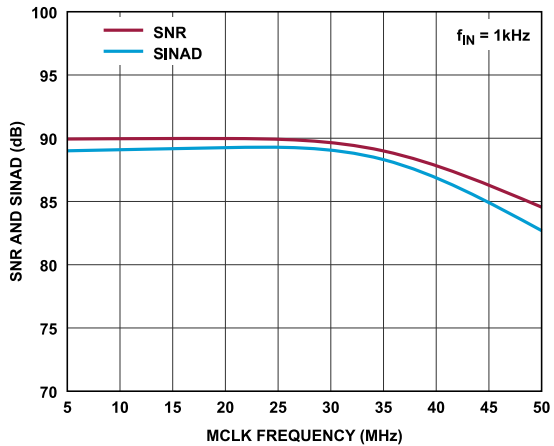


Figure 13. SNR and SINAD vs. MCLK Input Frequency

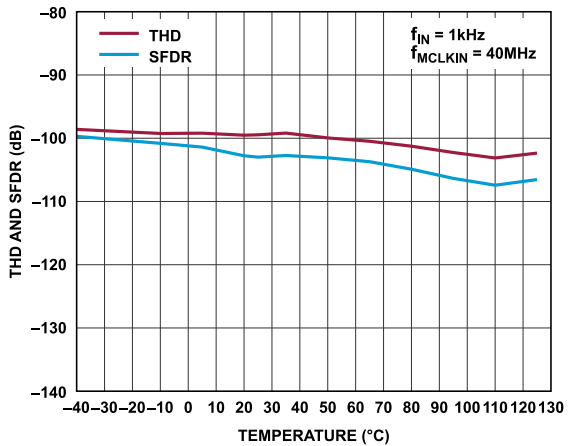


Figure 16. THD and SFDR vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

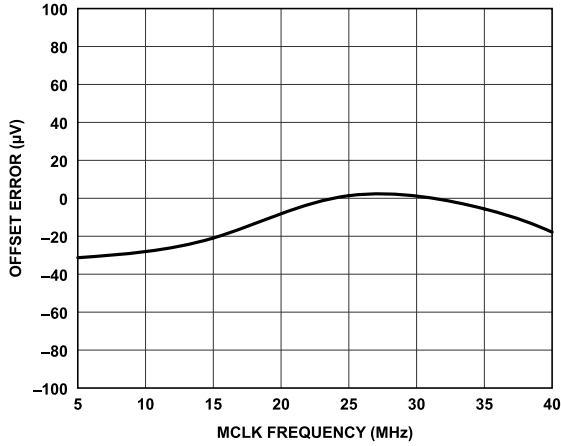


Figure 17. Offset Error vs. MCLK Input Frequency

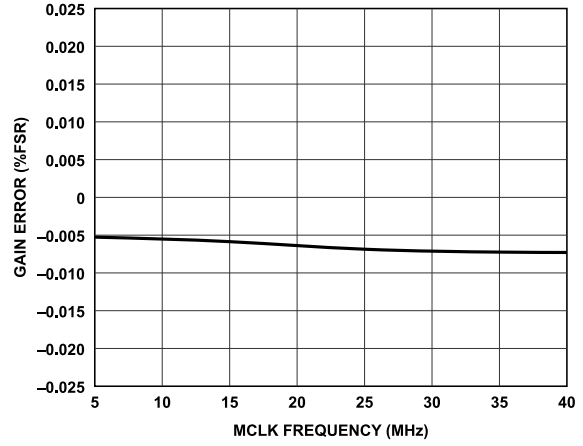


Figure 20. Gain Error vs. MCLK Input Frequency

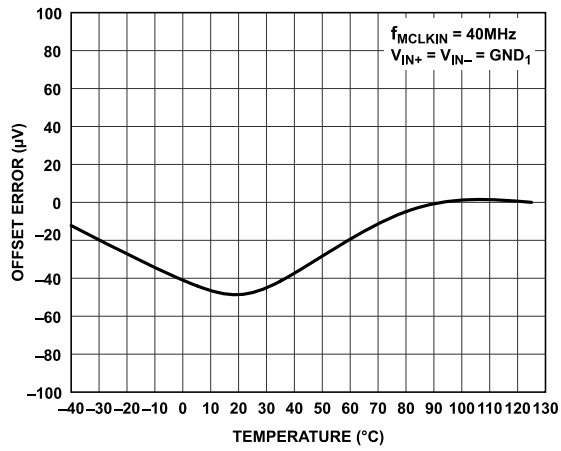


Figure 18. Offset Error vs. Temperature

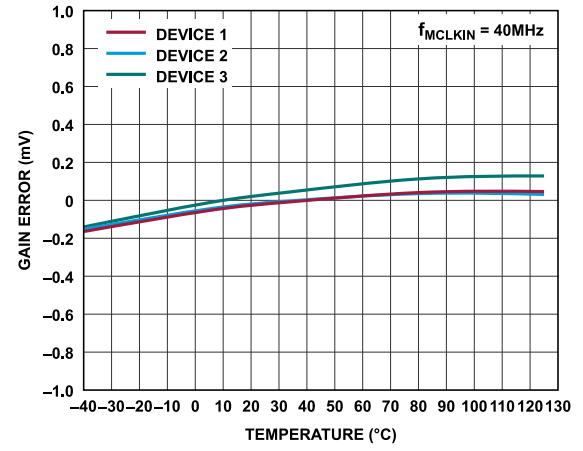


Figure 21. Gain Error vs. Temperature

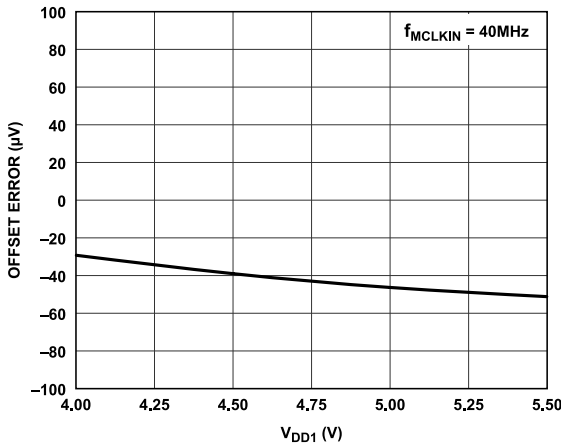


Figure 19. Offset Error vs. V_{DD1}

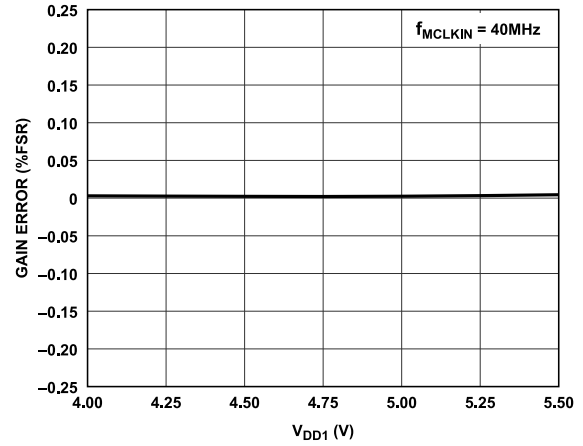


Figure 22. Gain Error vs. V_{DD1}

TYPICAL PERFORMANCE CHARACTERISTICS

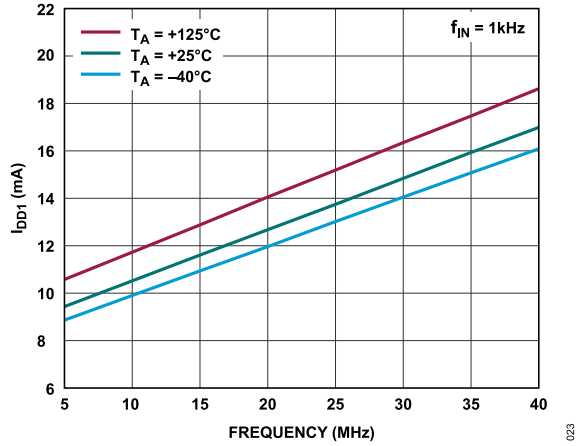


Figure 23. I_{DD1} vs. MCLK Input Frequency at Various Temperatures

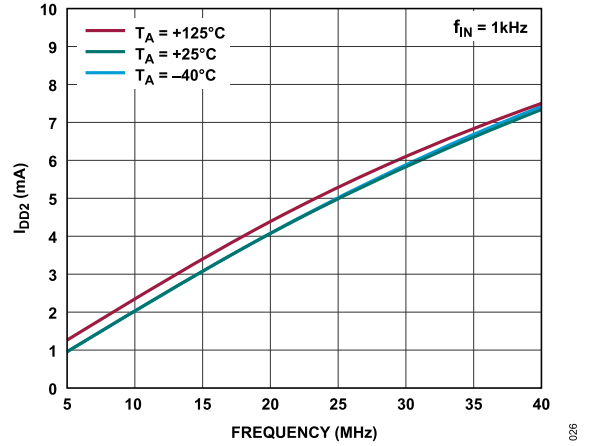


Figure 26. I_{DD2} vs. MCLK Input Frequency at Various Temperatures

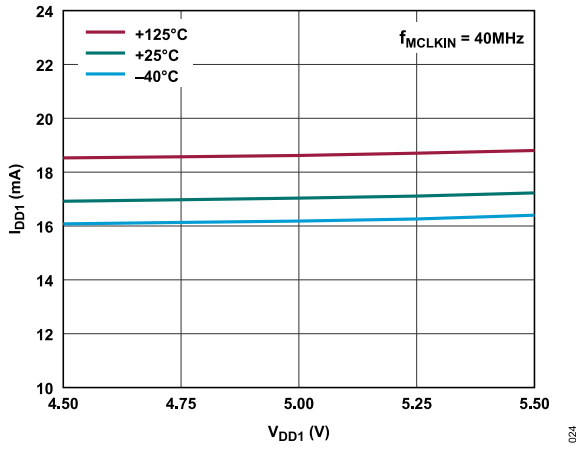


Figure 24. I_{DD1} vs. V_{DD1} at Various Temperatures

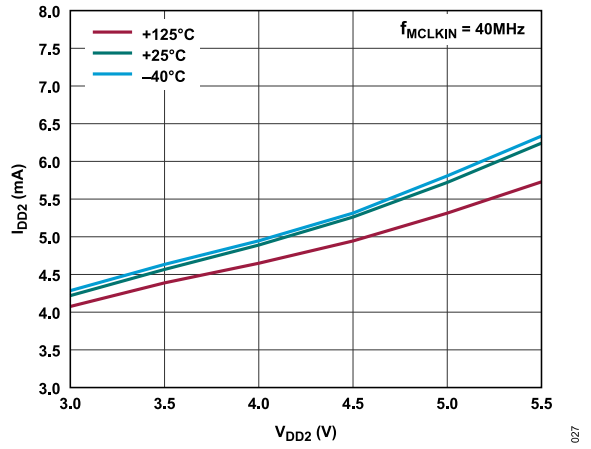


Figure 27. I_{DD2} vs. V_{DD2} at Various Temperatures

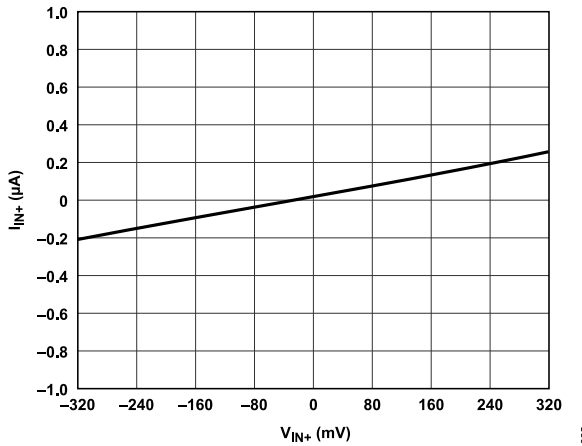


Figure 25. V_{IN+} Current (I_{IN+}) vs. V_{IN+} DC Input

TERMINOLOGY

Differential Nonlinearity (DNL)

DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)

INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are specified negative full scale, -250mV ($V_{\text{IN}+} - V_{\text{IN}-}$), Code 7168 for the 16-bit level, and specified positive full scale, $+250\text{mV}$ ($V_{\text{IN}+} - V_{\text{IN}-}$), Code 58,368 for the 16-bit level.

Offset Error

Offset error is the deviation of the midscale code (32,768 for the 16-bit level) from the ideal $V_{\text{IN}+} - V_{\text{IN}-}$ (that is, 0V).

Offset Drift vs. Temperature

The offset drift is calculated using the box method, as shown in Equation 1:

$$\text{Offset Drift} = ((\text{Voltage}_{\text{MAX}} - \text{Voltage}_{\text{MIN}})/T_{\Delta}) \quad (1)$$

where:

$\text{Voltage}_{\text{MAX}}$ is the maximum offset error point recorded.

$\text{Voltage}_{\text{MIN}}$ is the minimum offset error point recorded.

T_{Δ} is the difference in temperature between the maximum and minimum operating range.

Gain Error

The gain error includes both positive full-scale gain error and negative full-scale gain error. Positive full-scale gain error is the deviation of the specified positive full-scale code (58,368 for the 16-bit level) from the ideal $V_{\text{IN}+} - V_{\text{IN}-}$ (250mV) after the offset error is adjusted out. Negative full-scale gain error is the deviation of the specified negative full-scale code (7168 for the 16-bit level) from the ideal $V_{\text{IN}+} - V_{\text{IN}-}$ (-250mV) after the offset error is adjusted out.

Gain Error Drift vs. Temperature

The gain error drift (GED) is calculated using the box method, as shown in Equation 2:

$$\text{GED (ppm)} = ((\text{Voltage}_{\text{MAX}} - \text{Voltage}_{\text{MIN}})/(\text{Voltage}_{\text{FS}} \times T_{\Delta})) \times 10^6 \quad (2)$$

where:

$\text{Voltage}_{\text{MAX}}$ is the maximum gain error point recorded.

$\text{Voltage}_{\text{MIN}}$ is the minimum gain error point recorded.

$\text{Voltage}_{\text{FS}}$ is the analog input range full scale.

T_{Δ} is the difference in temperature between the maximum and minimum operating range.

Signal-to-Noise-and-Distortion Ratio (SINAD)

SINAD is the measured ratio of signal-to-noise and distortion at the output of the ADC. The signal is the rms value of the sine wave, and noise is the rms sum of all nonfundamental signals up to half

the sampling frequency ($f_{\text{S}}/2$), including harmonics, but excluding DC.

Signal-to-Noise Ratio (SNR)

SNR is the measured ratio of signal-to-noise at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_{\text{S}}/2$), excluding DC.

The ratio is dependent on the number of quantization levels in the digitization process, that is, the greater the number of levels, the smaller the quantization noise. The theoretical SNR for an ideal N-bit converter with a sine wave input is given by the Equation 3:

$$\text{SNR} = (6.02N + 1.76)\text{dB} \quad (3)$$

Therefore, for a 12-bit converter, the SNR is 74dB.

Isolation Common-Mode Transient Immunity (CMTI)

The isolation CMTI specifies the rate of the rise and fall of a transient pulse applied across the isolation boundary, beyond which clock or data is corrupted. Both the rate of change and the absolute common-mode voltage of the pulse are recorded. The ADuM7811 is tested under both static and dynamic CMTI conditions. CMTI is tested for static and dynamic inputs while monitoring the filtered data output for variations in response to a randomized application of the CMTI pulse.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the harmonics to the fundamental. It is defined, as shown in Equation 4:

$$\text{THD (dB)} = 20\log\sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}{V_1^2}} \quad (4)$$

where:

V_1 is the rms amplitude of the fundamental.

$V_2, V_3, V_4, V_5,$ and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious-Free Dynamic Range (SFDR) Noise

Peak harmonic or SFDR noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_{\text{S}}/2$, excluding DC) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is defined by Equation 5:

$$\text{ENOB} = (\text{SINAD} - 1.76)/6.02 \text{ bits} \quad (5)$$

TERMINOLOGY**Common-Mode Rejection Ratio (CMRR)**

CMRR is the ratio of the power in the ADC output at $\pm 250\text{mV}$ frequency, f , to the power of a $+250\text{mV}$ p-p sine wave applied to the common-mode voltage of $V_{\text{IN}+}$ and $V_{\text{IN}-}$ of frequency, f_{S} , as shown in [Equation 6](#):

$$\text{CMRR (dB)} = 10 \log(P_f/P_{f_S}) \quad (6)$$

where:

P_f is the power at frequency, f , in the ADC output.

P_{f_S} is the power at frequency, f_{S} , in the ADC output.

Power-Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the specified full-scale ($\pm 250\text{mV}$) transition point due to a change in power supply voltage from the nominal value.

THEORY OF OPERATION

CIRCUIT INFORMATION

The ADuM7811 isolated ADC with Σ - Δ modulator converts an analog input signal to a high speed single-bit data stream. The time average single-bit data from the modulator is directly proportional to the input signal. Figure 28 shows a typical application circuit where the ADuM7811 is used to provide isolation between the analog input, a current sensing resistor or shunt, and the digital output, which is then processed by a digital filter to provide an N-bit word.

ANALOG INPUT

The pseudodifferential analog input of the ADuM7811 is implemented with a sampled switched capacitor circuit. The analog input is processed through a high bandwidth SAR ADC on the sensing side, which preserves linearity and signal-to-noise robustness. The SAR information is taken at a lower sampling frequency than the Σ - Δ modulator output but contains more bandwidth information with less samples. Through an ADI proprietary method, the SAR information is encoded into a second-order modulator stage that digitizes the processed input signal into a single-bit output stream available on the controller side of the IC. The sample clock (MCLKIN) provides the clock signal for the conversion process as well as the output data framing clock. Due to the fact that the exact time of sampling occurs less frequently than the Σ - Δ clock frequency, the exact moment of sampling can vary within the window of samples that are processed by the decimation filter into an output result. The effect on the sampled data shows up as a time shift in the output, and the effect decreases as the decimation rate of the Σ - Δ output increases. This clock source is externally supplied to the ADuM7811. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream that accurately represents the analog input over time appears at the output of the converter (see Figure 29).

A differential signal of 0V ideally results in a stream of alternating 1s and 0s at the MDAT output pin that is high 50% of the time and low 50% of the time. A differential input of 250mV produces a stream of 1s and 0s that are high 89.06% of the time. A differential input of -250mV produces a stream of 1s and 0s that are high 10.94% of the time.

A differential input of 320mV ideally results in a stream of all 1s interrupted with a 0 every 128 MCLKIN cycles. A differential input of -320mV ideally results in a stream of all 0s interrupted with a 1 every 128 MCLKIN cycles. The ADuM7811 absolute full-scale range is ± 320 mV, and the specified full-scale performance range is ± 250 mV, as shown in Table 10.

Table 10. Analog Input Range

Analog Input	Voltage Input (mV)
Positive Full-Scale (+FS) Value	+320
Positive Specified Performance	+250
Zero	0
Negative Specified Performance	-250
Negative Full-Scale (-FS) Value	-320

To reconstruct the original information, this output must be digitally filtered and decimated. A sinc3 filter is recommended because this filter is one order higher than that of the ADuM7811 modulator, which is a second-order modulator. When a 256 decimation rate is used, the resulting 16-bit word rate is 156.25kSPS, assuming a 50MHz external clock frequency. For more details on the sinc filter implementation, see the Digital Filter section. Figure 30 shows the transfer function of the ADuM7811 relative to the 16-bit output.

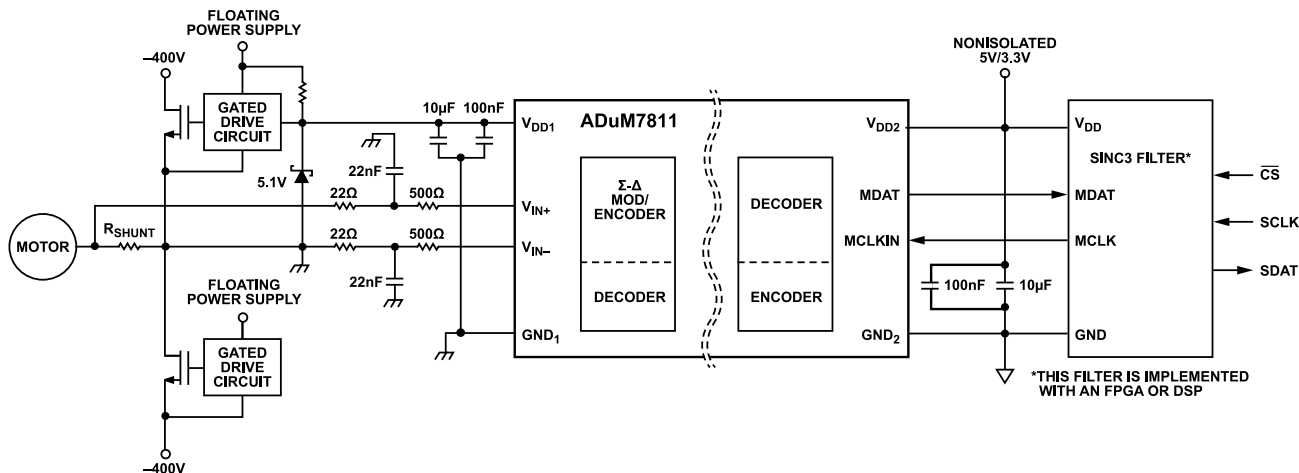


Figure 28. Typical Application Circuit

THEORY OF OPERATION

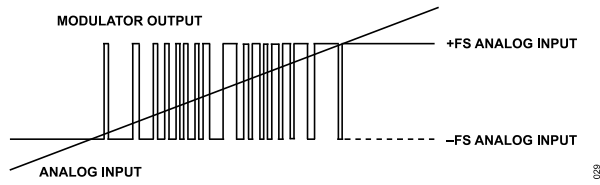


Figure 29. Analog Input vs. Modulator Output

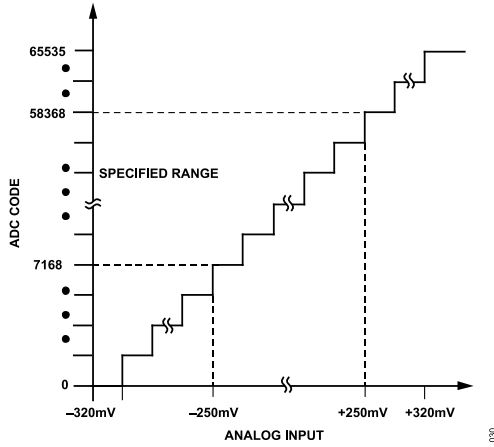


Figure 30. Filtered and Decimated 16-Bit Transfer Function

OVERRANGE RESPONSE

Under the condition the differential voltage on the inputs V_{IN+} to V_{IN-} exceeds $\pm(127/128)$ of the maximum input range $\pm 320\text{mV}$, the MDAT output generates a fault response. The MDAT fault response pattern density is $(127/128)$ for a $+317.5\text{mV}$ input, as shown in Figure 31, or $(1/128)$ for a -317.5mV input.

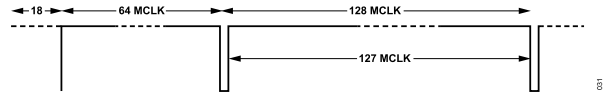


Figure 31. Overrange Response MDAT Pattern

APPLICATIONS INFORMATION

CURRENT SENSING APPLICATIONS

The ADuM7811 is ideally suited for current sensing applications where the voltage across a shunt resistor (R_{SHUNT}) is monitored. The load current flowing through an external shunt resistor produces a voltage at the input terminals of the ADuM7811. The ADuM7811 provides isolation between the analog input from the current sensing resistor and the digital outputs. By selecting the appropriate shunt resistor value, a variety of current ranges can be monitored.

Choosing R_{SHUNT}

The shunt resistor (R_{SHUNT}) values used in conjunction with the ADuM7811 are determined by the specific application requirements in terms of voltage, current, and power. Small resistors minimize power dissipation, whereas low inductance resistors prevent any induced voltage spikes, and high tolerance devices reduce current variations. The final values chosen are a compromise between low power dissipation and accuracy. Higher value resistors use the full performance input range of the ADC, thus achieving maximum SNR performance. Low value resistors dissipate less power but do not use the full performance input range. The ADuM7811, however, delivers excellent performance, even with lower input signal levels, which allows low value shunt resistors to be used while maintaining system performance.

To choose a suitable shunt resistor, first determine the current through the shunt. Calculated the shunt current for a 3-phase induction motor as:

$$I_{RMS} = PW / (1.73 \times V \times EF \times PF) \quad (7)$$

where:

I_{RMS} is the motor phase current (A rms).
 PW is the motor power (W).
 V is the motor supply voltage (V AC).
 EF is the motor efficiency (%).
 PF is the power efficiency (%).

To determine the shunt peak sense current (I_{SENSE}), consider the motor phase current and any overload that may be possible in the system. When the peak sense current is known, divide the voltage range of the ADuM7811 ($\pm 250\text{mV}$) by the peak sense current to yield a maximum shunt value.

If the power dissipation in the shunt resistor is too large, the shunt resistor can be reduced, and less of the ADC input range can be used. Figure 32 shows the SINAD performance characteristics and the ENOB of resolution for the ADuM7811 for different input signal amplitudes. The performance of the ADuM7811 at lower input signal ranges allows smaller shunt values to be used while still maintaining a high level of performance and overall system efficiency.

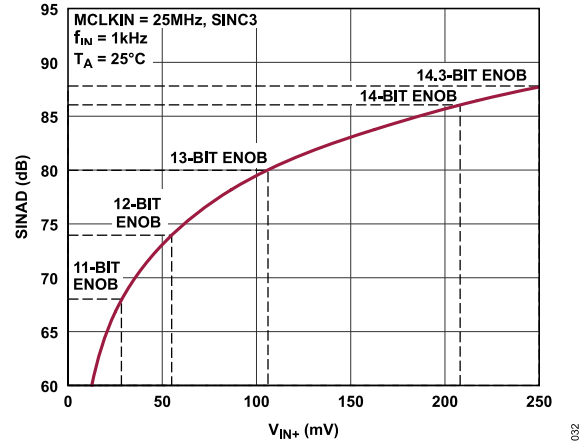


Figure 32. SINAD vs. V_{IN+} AC Input Signal Amplitude

R_{SHUNT} must dissipate the $\text{current}^2 \times \text{resistance}$ (I^2R) power losses. If the power dissipation rating of the resistor is exceeded, the value may drift, or the resistor may be damaged, resulting in an open circuit. This open circuit may result in a differential voltage across the terminals of the ADuM7811, in excess of the absolute maximum ratings. If I_{SENSE} has a large high frequency component, choose a resistor with low inductance.

VOLTAGE SENSING APPLICATIONS

The ADuM7811 can also be used for isolated voltage monitoring. For example, in motor control applications, the device can be used to sense the bus voltage. In applications where the voltage being monitored exceeds the specified analog input range of the ADuM7811, a voltage divider network can be used to reduce the voltage being monitored to the required range.

INPUT FILTER

In a typical use case for directly measuring the voltage across a shunt resistor, the ADuM7811 can be connected directly across the shunt resistor with a simple RC low-pass filter on each input.

The recommended circuit configuration for driving the differential inputs to achieve best performance is shown in Figure 33. An RC low-pass filter is placed on both the analog input pins. Recommended values for the resistors and capacitors are 22Ω and 22nF , respectively. If possible, equalize the source impedance on each analog input to minimize offset. Downstream of the RC filter, to optimize performance, the use of $R2$ series resistors is suggested. Recommended value for the resistors $R2$ are 500Ω .

APPLICATIONS INFORMATION

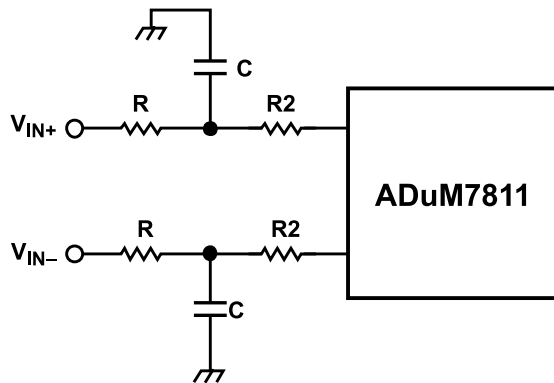


Figure 33. RC Low-Pass Filter Input Network

DIGITAL FILTER

The output of the ADuM7811 is a continuous digital bit stream. To reconstruct the original input signal information, this output bit stream must be digitally filtered and decimated. A sinc filter is recommended due to simplicity of the filter. A sinc3 filter is recommended because the filter is one order higher than that of the ADuM7811 modulator, which is a second-order modulator. The type of filter selected, the decimation rate, and the modulator clock used determines the overall system resolution and throughput rate. The higher the decimation rate, the greater the system accuracy. However, there is a trade-off between accuracy and throughput rate and, therefore, higher decimation rates result in lower throughput solutions. Note that for a given bandwidth requirement, a higher MCLKIN frequency can allow higher decimation rates to be used, resulting in higher SNR performance.

A sinc3 filter is recommended for the ADuM7811. This filter can be implemented on a field programmable gate array (FPGA) or a digital signal processor (DSP). Equation 8 describes the transfer function of a sinc filter:

$$H(Z) = \left(\frac{1}{DR} \frac{(1 - Z^{-DR})}{(1 - Z^{-1})} \right)^N \quad (8)$$

where:

Z is the sample.

DR is the decimation rate.

N is the sinc filter order.

The throughput rate of the sinc filter is determined by the modulator clock and the decimation rate selected.

$$\text{Throughput} = \text{MCLK}/DR \quad (9)$$

where MCLK is the modulator clock frequency.

As the decimation rate increases, the data output size from the sinc filter increases. The output data size is expressed in Equation 10. The 16 most significant bits are used to return a 16-bit result.

$$\text{Data Size} = N \times \log_2 DR \quad (10)$$

For a sinc³ filter, the -3dB filter response point can be derived from the filter transfer function, Equation 8, and is 0.262 times the throughput rate.

Another widespread parameter used to compare the accuracy of ADCs and Σ - Δ modulators is the ENOB. Figure 34 shows the ENOB of the ADuM7811 with different decimation rate. In this document, this number is calculated from the SINAD by using Equation 11:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76\text{dB}}{6.02\text{dB}} \quad (11)$$

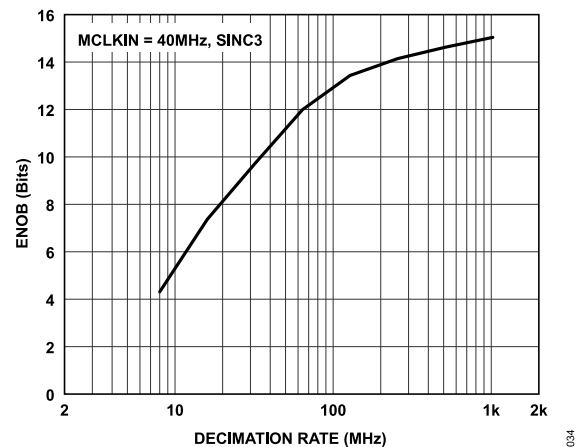


Figure 34. ENOB vs. Decimation Rate of Sinc3 Filter Order

GROUNDING AND LAYOUT

It is recommended to decouple the V_{DD1} supply with a 10 μ F (C2) capacitor in parallel with a 100nF (C1) capacitor to GND₁. Decouple the V_{DD2} supply with a 10 μ F capacitor in parallel with a 100nF capacitor to GND₂. In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout so that any coupling that occurs equally affects all pins on a given component side. Failure to ensure equal coupling can cause voltage differentials between pins to exceed the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage. Place any decoupling used as close to the supply pins as possible.

If possible, equalize the source impedance on each analog input to minimize offset. Check for mismatch and thermocouple effects on the analog input PCB tracks to reduce offset drift.

For best performance, a recommended layout showing an optimized placement and connection of the decoupling capacitors C1 and C2 for a 4-layer board is shown in Figure 35. The connection between the V_{DD1} and GND₁ pins to the decoupling caps C1 and C2 is made via the inner layer 1 (in gray). Via in pads are suggested in V_{DD1} and GND₁ pin connections when possible.

APPLICATIONS INFORMATION

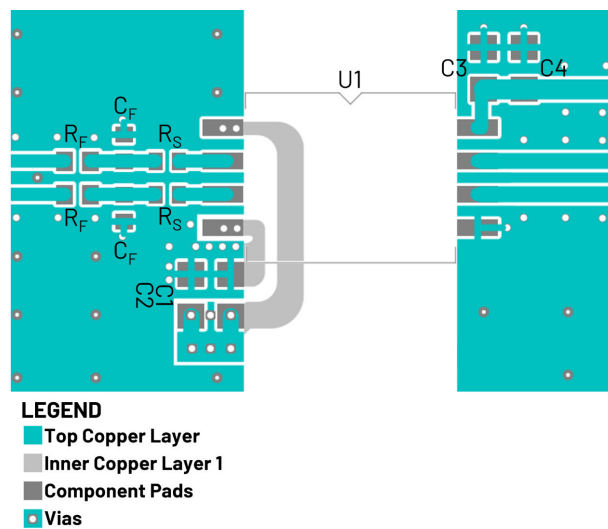


Figure 35. Recommended Layout of the ADuM7811

THERMAL ANALYSIS

The ADuM7811 consists of three internal die attached to a split lead frame with two die attach pads. For the purposes of thermal analysis, the die are treated as a thermal unit, with the highest junction temperature reflected in the thermal parameter values from [Table 7](#). The thermal parameter values are based on thermal simulations with the devices mounted on a JEDEC standard, 4-layer board with fine width traces on outer layers, planes on inner layers, no thermal vias and still air. Under normal operating conditions, the ADuM7811 can operate at full load across the full temperature range without derating the output current.

θ_{JA} and θ_{JB} are mainly used to compare the thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. θ_{JA} and θ_{JB} can be used for first order approximation of the junction temperature in the system environment.

If an accurate thermal measurement of the board temperature near the device under test or directly on the package top surface operating in the system environment is available along with the corresponding device power dissipation, then using Ψ_{JB} or Ψ_{JT} is a more appropriate way to estimate the worst-case junction temperature in the system environment. Use Ψ_{JB} when the temperature measurement point is on the board or Ψ_{JT} when it is on the package top. The junction temperature is estimated using the [Equation 12](#):

$$T_J = \psi_{Jx} \times P_d + T_x \quad (12)$$

where:

P_d is the dissipated power.

T_x is the measured temperature at location x and x is either B for the PCB or T for the package top.

The temperature measurement point for θ_{JB} and Ψ_{JB} is on the PCB Pin 2 on the outer edge of the pin footprint. The temperature measurement point for Ψ_{JT} is at the center of the package's top side.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RI-8-1	SOIC_IC	8-Lead Standard Small Outline Package, with Increased Creepage Wide Body

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

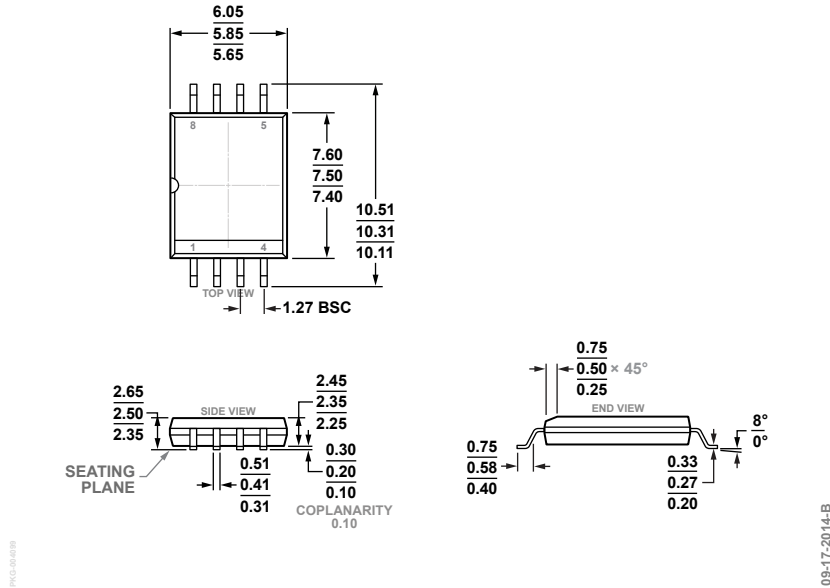


Figure 36. 8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC] Wide Body (RI-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Packing Quantity	Package Option
ADuM7811-8BRIZ	-40°C to +125°C	8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	Tube, 80	RI-8-1
ADuM7811-8BRIZ-RL	-40°C to +125°C	8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	Reel, 1500	RI-8-1

¹ Z = RoHS Compliant Part.

EVALUATION BOARDS

Model ¹	Package Description
EV-ADuM7811-8FMCZ	ADuM7811 8-Lead SOIC_IC Evaluation Board

¹ Z = RoHS Compliant Part.

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