Data Sheet

ADuM362N

3.0 kV rms 6-Channel Digital Isolator

FEATURES

- High common-mode transient immunity: 180 kV/µs typical
- High robustness to radiated and conducted noise
- Low propagation delay
  - 6.2 ns typical (10 ns maximum) for 5 V operation
- Low dynamic power consumption, <1.65 mA/ch at 1 Mbps
- 2.25 V to 5.5 V level translation
- 150 Mbps maximum guaranteed data rate for 5 V operation
- High temperature operation: 125°C
- Safety and regulatory approvals
- RQ-16 [QSOP] package
  - UL 1577 (pending)
    - V_{ISO} = 3000 V_{RMS} for 1 minute
  - EN IEC 60747-17 (pending)
    - V_{IORM} = 636 V_{PEAK}
    - V_{IOSM} = 10,000 V_{PEAK} (reinforced)
  - IEC/EN/CSA 62368-1 (pending)
  - IEC/CSA 60601-1 (pending)
  - IEC/CSA 61010-1 (pending)
  - CQC GB 4943.1 (pending)
- ±8 kV IEC 61000-4-2 ESD protection across isolation barrier
- ±4 kV HBM ESD protection on input/output pins
- Fail-safe high (N1) or low (N0) options
- 16-lead, RoHS compliant, QSOP package

APPLICATIONS

- Serial-peripheral interface (SPI) data converter isolation
- RS-485 and controller area network with flexible data rate (CAN FD) industrial field bus isolation
- PWM controller signal isolation
- General-purpose multichannel isolation

GENERAL DESCRIPTION

The ADuM362N[1] is a 6-channel digital isolator based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed, complementary metal-oxide semiconductor (CMOS) and back-to-back monolithic air core transformer technology, these isolation components provide outstanding performance characteristics and meet CISPR 32/EN 55032 Class B limits at 5 Mbps. The maximum propagation delay is 10 ns with a pulse-width distortion of less than 3 ns at 5 V operation. Channel matching is tight at 3.0 ns maximum.

The ADuM362N data channels are independent and are available in a variety of configurations with a withstand voltage rating of 3 kV rms (see Figure 17). The devices operate with the supply voltage on either side ranging from 2.25 V to 5.5 V, which provides compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

Two different fail-safe options are available, by which the outputs transition to a predetermined state when the input power supply is not applied.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

Rev. 0

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REVISION HISTORY

9/2024—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

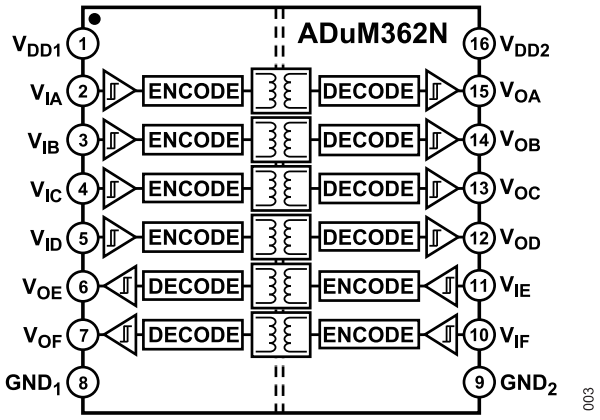

Figure 1. ADuM362N Functional Block Diagram

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty-cycle signals.

Table 1. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within pulse-width distortion (PWD) limit
Data Rate		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		6.2	10	ns	50% input to 50% output
Pulse-Width Distortion	PWD		0.3	3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.1	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.3	3.0	ns	
Opposing Direction	t_{PSKOD}		0.3	3.0	ns	
Jitter[1]						For more details, see the Jitter Measurement section
Random Jitter, RMS (1σ)[2]	$t_{JIT(RJ)}$		5.4		ps	1 MHz clock input, all channels switching
Deterministic Jitter, Peak-to-Peak[3, 4]	$t_{JIT(DJ)}$		104		ps	100 Mbps, 2^{15} − 1 PRBS input
Total Jitter, Peak-to-Peak, at Bit Error Rate (BER) 1 × 10^{-12}	$t_{JIT(TJ)}$					100 Mbps, 2^{15} − 1 PRBS input[5]
Without Crosstalk			198		ps	Single channel switching
With Crosstalk			260		ps	All channels switching
DC SPECIFICATIONS						
Input Threshold Voltage						V_{Ix}
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{HYS}		0.85		V	$V_{IH} - V_{IL}$
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[6] = −20 μA, V_{Ix} = V_{IxH}[7]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[6] = −4 mA, V_{Ix} = V_{IxH}[7]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[6] = 20 μA, V_{Ix} = V_{IxL}[8]
			0.2	0.4	V	I_{Ox}[6] = 4 mA, V_{Ix} = V_{IxL}[8]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM362N						
	$I_{DD1 (Q)}$		1.4	2.1	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD2 (Q)}$		1.8	2.9	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD1 (Q)}$		9.3	12.6	mA	V_I[9] = 1 (N0), 0 (N1)[10]
	$I_{DD2 (Q)}$		7.1	9.7	mA	V_I[9] = 1 (N0), 0 (N1)[10]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.052		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.067		mA/Mbps	Inputs switching, 50% duty cycle, C_L = 0 nF
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{UVLO+}		2.0	2.2	V	Rising supply voltage enable threshold
Negative V_{DDx} Threshold	V_{UVLO-}	1.7	1.8		V	Falling supply voltage lockout threshold
V_{DDx} Hysteresis	V_{UVLO_HYS}		0.2		V	UVLO hysteresis
UVLO Release Time	t_{UVLO}		60		μs	UVLO release delay after V_{UVLO+} threshold

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[11, 12]	$\lvert CM_H \rvert$	100	180		kV/µs	$V_{Ix} = V_{DDx}$, $V_{CM} \geq 1000$ V, $T_A = 125°C$
	$\lvert CM_L \rvert$	100	180		kV/µs	$V_{Ix} = 0$ V, $V_{CM} \geq 1000$ V, $T_A = 125°C$

[1] Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter.

[2] This specification is measured over a population of ~100,000 edges.

[3] Peak-to-peak jitter specifications include jitter due to PWD.

[4] This specification is measured over a population of ~300,000 edges.

[5] Using the following formula: $t_{JIT(TJ)} = 14 \times t_{JIT(RJ)} + t_{JIT(DJ)}$.

[6] I_{Ox} is the Channel x output current, where x = A, B, C, D, E, or F.

[7] V_{IxH} is the input-side logic high.

[8] V_{IxL} is the input-side logic low.

[9] V_I is the voltage input.

[10] N0 refers to the ADuM362N0 models, and N1 refers to the ADuM362N1 models. For more details, see the Ordering Guide section.

[11] Guaranteed by design and not subject to production test.

[12] $\lvert CM_H \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $\lvert CM_L \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 2. Total Supply Current vs. Data Throughput

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
ADuM362N						
1 Mbps						
Supply Current Side 1	I_{DD1}		5.3	7.5	mA	$C_L = 0$ nF
Supply Current Side 2	I_{DD2}		4.5	6.4	mA	$C_L = 0$ nF
25 Mbps						
Supply Current Side 1	I_{DD1}		6.4	8.7	mA	$C_L = 0$ nF
Supply Current Side 2	I_{DD2}		6.2	8.5	mA	$C_L = 0$ nF
100 Mbps						
Supply Current Side 1	I_{DD1}		10.4	13.9	mA	$C_L = 0$ nF
Supply Current Side 2	I_{DD2}		11.5	16.8	mA	$C_L = 0$ nF

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ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty-cycle signals.

Table 3. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within PWD limit
Data Rate		100			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		6.6	10	ns	50% input to 50% output
Pulse-Width Distortion	PWD		0.5	3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.5	3.0	ns	
Opposing Direction	t_{PSKOD}		0.5	3.0	ns	
Jitter[1]						For more details, see the Jitter Measurement section, all channels switching
Random Jitter, RMS (1σ)[2]	$t_{JIT(RJ)}$		7.1		ps	1 MHz clock input
Deterministic Jitter, Peak-to-Peak[3, 4]	$t_{JIT(DJ)}$		124		ps	100 Mbps, 2^{15} − 1 PRBS input
Total Jitter, Peak-to-Peak, at Bit Error Rate (BER) 1 × 10^{-12}	$t_{JIT(TJ)}$					100 Mbps, 2^{15} − 1 PRBS input[5]
Without Crosstalk			232		ps	Single channel switching
With Crosstalk			257		ps	All channels switching
DC SPECIFICATIONS						
Input Threshold Voltage						V_{Ix}
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{HYS}		0.7		V	$V_{IH} - V_{IL}$
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[6] = −20 μA, V_{Ix} = V_{IxH}[7]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[6] = −2 mA, V_{Ix} = V_{IxH}[7]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[6] = 20 μA, V_{Ix} = V_{IxL}[8]
			0.2	0.4	V	I_{Ox}[6] = 2 mA, V_{Ix} = V_{IxL}[8]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM362N						
	$I_{DD1 (Q)}$		1.3	2.2	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD2 (Q)}$		1.8	2.8	mA	V_I[9] = 1 (N0), 0 (N1)[10]
	$I_{DD1 (Q)}$		8.7	12.2	mA	V_I[9] = 1 (N0), 0 (N1)[10]
	$I_{DD2 (Q)}$		6.8	9.5	mA	V_I[9] = 1 (N0), 0 (N1)[10]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.036		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.044		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{UVLO+}		2.0	2.2	V	Rising supply voltage enable threshold
Negative V_{DDx} Threshold	V_{UVLO-}	1.7	1.8		V	Falling supply voltage lockout threshold
V_{DDx} Hysteresis	V_{UVLO_HYS}		0.2		V	UVLO hysteresis
UVLO Release Time	t_{UVLO}		60		μs	UVLO release delay after V_{UVLO+} threshold

SPECIFICATIONS

Table 3. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[11, 12]	$\lvert CM_H \rvert$	100	180		kV/µs	$V_{Ix} = V_{DDx}$, $V_{CM} \geq 1000$ V, $T_A = 125°C$
	$\lvert CM_L \rvert$	100	180		kV/µs	$V_{Ix} = 0$ V, $V_{CM} \geq 1000$ V, $T_A = 125°C$

[1] Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter.

[2] This specification is measured over a population of ~100,000 edges.

[3] Peak-to-peak jitter specifications include jitter due to PWD.

[4] This specification is measured over a population of ~300,000 edges.

[5] Using the following formula: $t_{JIT(TJ)} = 14 \times t_{JIT(RJ)} + t_{JIT(DJ)}$.

[6] I_{Ox} is the Channel x output current, where x = A, B, C, D, E, or F.

[7] V_{IxH} is the input-side logic high.

[8] V_{IxL} is the input-side logic low.

[9] V_I is the voltage input.

[10] N0 refers to ADuM362N0 models, and N1 refers to ADuM362N1 models. For more details, see the Ordering Guide section.

[11] Guaranteed by design and not subject to production test.

[12] $\lvert CM_H \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $\lvert CM_L \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 4. Total Supply Current vs. Data Throughput

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
ADuM362N						
1 Mbps						
Supply Current Side 1	I_{DD1}		5.3	7.2	mA	$C_L = 0$ nF
Supply Current Side 2	I_{DD2}		4.5	6.2	mA	$C_L = 0$ nF
25 Mbps						
Supply Current Side 1	I_{DD1}		6.2	8.1	mA	$C_L = 0$ nF
Supply Current Side 2	I_{DD2}		5.7	7.4	mA	$C_L = 0$ nF
100 Mbps						
Supply Current Side 1	I_{DD1}		9.1	11.5	mA	$C_L = 0$ nF
Supply Current Side 2	I_{DD2}		9.4	12.7	mA	$C_L = 0$ nF

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operation range: 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty-cycle signals.

Table 5. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within PWD limit
Data Rate		100			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		7.2	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.3	4.5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			8.9	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.4	5.0	ns	
Opposing Direction	t_{PSKOD}		0.4	5.0	ns	
Jitter[1]						For more details, see the Jitter Measurement section
Random Jitter, RMS (1σ)[2]	$t_{JIT(RJ)}$		8.7		ps	1 MHz clock input, all channels switching
Deterministic Jitter, Peak to Peak[3, 4]	$t_{JIT(DJ)}$		172		ps	100 Mbps, 2^{15} − 1 PRBS
Total Jitter, Peak to Peak, at Bit Error Rate (BER) 1 × 10^{-12}	$t_{JIT(TJ)}$					100 Mbps, 2^{15} − 1 PRBS[5]
Without Crosstalk			309		ps	Single channel switching
With Crosstalk			424		ps	All channels switching
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{HYS}		0.65		V	$V_{IH} - V_{IL}$
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[6] = −20 μA, V_{Ix} = V_{IxH}[7]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[6] = −2 mA, V_{Ix} = V_{IxH}[7]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[6] = 20 μA, V_{Ix} = V_{IxL}[8]
			0.2	0.4	V	I_{Ox}[6] = 2 mA, V_{Ix} = V_{IxL}[8]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM362N						
	$I_{DD1 (Q)}$		1.4	2.2	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD2 (Q)}$		1.8	2.8	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD1 (Q)}$		8.7	12.2	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD2 (Q)}$		6.8	9.8	mA	V_I[9] = 0 (N0), 1 (N1)[10]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.032		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.038		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{UVLO+}		2.0	2.2	V	Rising supply voltage enable threshold
Negative V_{DDx} Threshold	V_{UVLO-}	1.7	1.8		V	Falling supply voltage lockout threshold
V_{DDx} Hysteresis	V_{UVLO_HYS}		0.2		V	UVLO hysteresis
UVLO Release Time	t_{UVLO}		60		μs	UVLO release delay after V_{UVLO+} threshold

SPECIFICATIONS

Table 5. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[11, 12]	$\lvert CM_H \rvert$	100	180		kV/µs	$V_{Ix} = V_{DDx}$, $V_{CM} \geq 1000$ V, $T_A = 125°C$
	$\lvert CM_L \rvert$	100	180		kV/µs	$V_{Ix} = 0$ V, $V_{CM} \geq 1000$ V, $T_A = 125°C$

[1] Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter.

[2] This specification is measured over a population of ~100,000 edges.

[3] Peak-to-peak jitter specifications include jitter due to PWD.

[4] This specification is measured over a population of ~300,000 edges.

[5] Using the following formula: $t_{JIT(TJ)} = 14 \times t_{JIT(RJ)} + t_{JIT(DJ)}$.

[6] I_{Ox} is the Channel x output current, where x = A, B, C, D, E, or F.

[7] V_{IxH} is the input-side logic high.

[8] V_{IxL} is the input-side logic low.

[9] V_I is the voltage input.

[10] N0 refers to ADuM362N0 models, and N1 refers to ADuM362N1 models. For more details, see the Ordering Guide section.

[11] Guaranteed by design and not subject to production test.

[12] $\lvert CM_H \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $\lvert CM_L \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 6. Total Supply Current vs. Data Throughput

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
ADuM362N						
1 Mbps						
Supply Current Side 1	I_{DD1}		5.1	7.2	mA	$C_L = 0$ nF
Supply Current Side 2	I_{DD2}		4.5	6.1	mA	$C_L = 0$ nF
25 Mbps						
Supply Current Side 1	I_{DD1}		5.7	7.9	mA	$C_L = 0$ nF
Supply Current Side 2	I_{DD2}		5.3	7.1	mA	$C_L = 0$ nF
100 Mbps						
Supply Current Side 1	I_{DD1}		8.4	10.4	mA	$C_L = 0$ nF
Supply Current Side 2	I_{DD2}		8.2	10.2	mA	$C_L = 0$ nF

SPECIFICATIONS

INSULATION CHARACTERISTICS

The ADuM362N is suitable for reinforced electrical insulation only within the safety ratings, as shown in Figure 2. Maintenance of the safety ratings is ensured by protective circuits.

Table 7. RQ-16 Isolation Characteristics

Parameter	Symbol	Conditions	Value RQ-16	Unit
CLASSIFICATIONS				
Overvoltage Category per IEC60664-1	–	For rated mains voltage ≤ 150 V_{RMS}	I to III	–
		For rated mains voltage ≤ 300 V_{RMS}	I to III	–
Climatic Classification	–		40/125/21	–
Pollution Degree	–	Per DIN VDE V 0110 (refer to Table 1 of the DIN VDE standard)	2	–
VOLTAGE				
Maximum Working-Isolation Voltage[1]	V_{IOWM}	Continuous RMS voltage	450	V_{RMS}
Maximum Repetitive-Isolation Voltage[1]	V_{IORM}	Continuous PEAK voltage	636	V_{PEAK}
Maximum Transient-Isolation Voltage[1]	V_{IOTM}	t = 1 s	4242	V_{PEAK}
Maximum Withstanding-Isolation Voltage[1]	V_{ISO}	f_{TEST} = 60 Hz, duration = 60 s	3000	V_{RMS}
Maximum Surge-Isolation Voltage[1]	V_{IOSM}	Test method per IEC 60065, $V_{IOSM} \geq 1.3 \times V_{IMP}$[2]	10000	V_{PEAK}
Maximum Impulse Voltage[1]	V_{IMP}	Tested in air, 1.2 µs/50 µs waveform per IEC 62368-1	4000	V_{PEAK}
Input-to-Output Test Voltage	V_{PR}		1192	V_{PEAK}
Apparent Charge	q_{PD}	Method b1, V_{PR} = 1.875 x VIORM, t = 1 s	5	pC
PACKAGE CHARACTERISTICS				
External Creepage[3]	CPG	Measured from input terminals to output terminals, shortest distance path along body	≥3.5	mm
External Clearance[3]	CLR	Measured from input terminals to output terminals, shortest distance through air[4]	≥3.5	mm
Internal Clearance	DTI	Minimum internal clearance	34	µm
Comparative Tracking Index	CTI		>600	V
Material Group		Material Group (IEC 60112)	I	–
Resistance (Input to Output)[5]	R_{IO}	V_{IO} = 500 V, T_A = 25°C	10^{13}	Ω
		V_{IO} = 500 V, T_A = T_S	10^{9}	Ω
Capacitance (Input-to-Output)[5]	C_{IO}	f = 1 MHz	4	pF
IC Junction-to-Ambient Thermal Resistance	θ_{JA}	Simulated per JEDEC JESD-51	88.28	°C/W
SAFETY LIMITING VALUES				
Maximum Ambient-Safety Temperature	T_S		150	°C
Maximum Input-Power Dissipation	P_S	Total Power Dissipation at 25°C	1.40	°C/W

1 V_{ISO}, V_{IOTM}, V_{IOWM}, V_{IORM}, V_{IMP}, and V_{IOSM} are defined by the IEC 60747-17 standard.

2 Devices are immersed in oil during surge characterization.

3 In accordance with IEC 62368-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

4 Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

5 Device is measured as a 2-terminal device with Pin 1 through Pin 4 connected and Pin 5 through Pin 8 connected.

SPECIFICATIONS

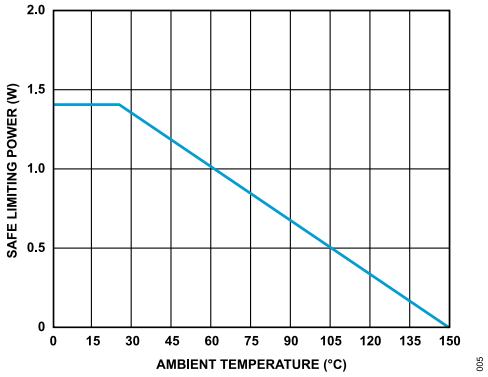

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values, per IEC 60747-17

REGULATORY INFORMATION

For details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels, see Table 11. Certifications available at Safety and Regulatory Certification for Digital Isolation.

Table 8. RQ-16 [QSOP] Package

Regulatory Agency	Standard Certification/Approval	File
UL (pending)	UL1577	Pending
	Single protection, 3000 V_{RMS} isolation voltage[1]	
TÜV Süd (pending)	EN IEC 60747-17	Pending
	Reinforced insulation, 636 V_{PEAK}[2]	
CSA (pending)	IEC EN/CSA 62368-1	Pending
	Basic insulation at 350 V_{RMS}	
	Reinforced insulation at 175 V_{RMS}	
	IEC/CSA 60601-1	
	Basic insulation (1 MOPP), 187 V_{RMS}	
	IEC/CSA 61010-1	
	Basic insulation at 300 V_{RMS}	
	Reinforced insulation at 150 V_{RMS}	
TÜV Süd (pending)	EN IEC 62368-1	Pending
	Basic insulation at 350 V_{RMS}	
	Reinforced insulation at 175 V_{RMS}	
CQC (pending)	CQC GB 4943.1	Pending
	Basic insulation at 350 V_{RMS}	
	Reinforced insulation at 175 V_{RMS}	

[1] In accordance with UL 1577, each product is proof tested by applying an insulation test voltage ≥3600 V_{RMS} for 1 sec.

[2] In accordance with IEC 60747-17, each product is proof tested by applying an insulation test voltage ≥1192 V_{PEAK} for 1 sec (partial-discharge detection limit = 5 pC).

RECOMMENDED OPERATING CONDITIONS

Table 9. Recommended Operating Conditions

Parameter	Symbol	Rating
Operating Temperature	T_A	−40°C to +125°C
Supply Voltages		
V_{DD1}		2.25 V to 5.5 V
V_{DD2}		2.25 V to 5.5 V
Input Signal Rise and Fall Times		1.0 ms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 10. Absolute Maximum Ratings

Parameter	Rating
Supply Voltages	
V_{DD1} to GND_1	−0.5 V to +7.0 V
V_{DD2} to GND_2	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{IE}, V_{IF})[1]	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB}, V_{OC}, V_{OD}, V_{OE}, V_{OF})[2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[4]	−300 kV/µs to +300 kV/µs
Temperature	
Storage Range (T_{ST})	−65°C to +150°C
Ambient Operating Range (T_A)	−40°C to +125°C
Moisture Sensitivity Level	MSL3

[1] V_{DDI} is the input-side supply voltage.

[2] V_{DDO} is the output-side supply voltage.

[3] For the maximum rated current values for various ambient temperatures, see Figure 2.

[4] Refer to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latchup or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 11. Maximum Continuous Working Voltage, RQ-16 [QSOP] Package

Parameter	Rating[1]	Constraint
AC VOLTAGE		
Bipolar Waveform		
Basic Insulation	450 V rms	Rating limited by VIOWM[2] (reinforced) rating per IEC60747-17
Reinforced Insulation	347 V rms	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment
DC VOLTAGE		
Basic Insulation	636 V DC	Rating limited by VIORM[3] (reinforced) rating per IEC60747-17
Reinforced Insulation	347 V DC	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier in a Pollution Degree 2 environment. For more details, see the Insulation Lifetime section.

[2] VIOWM is the RMS or equivalent DC voltage characterizing the specified long-term withstand capability of its isolation.

[3] VIORM is the maximum repetitive peak-isolation voltage.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

International electrotechnical commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

ESD Ratings for ADuM362N

Table 12. ADuM362N, 16-Lead [QSOP]

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±4000	3A
CDM[1]	±1250	C3
IEC[2]	±8000	Level 4

[1] With respect to local V_{DDx} and GND_x pins.

[2] Across the isolation barrier between GND_1 and GND_2.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

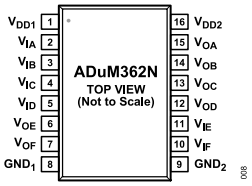

Figure 3. ADuM362N Pin Configuration

Table 13. ADuM362N Pin Function Descriptions

Pin Number	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1. This pin requires a 0.1 µF bypass capacitor.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	V_{IC}	Logic Input C.
5	V_{ID}	Logic Input D.
6	V_{OE}	Logic Output E.
7	V_{OF}	Logic Output F.
8	GND_1	Ground Reference for Isolator Side 1.
9	GND_2	Ground Reference for Isolator Side 2.
10	V_{IF}	Logic Input F.
11	V_{IE}	Logic Input E.
12	V_{OD}	Logic Output D.
13	V_{OC}	Logic Output C.
14	V_{OB}	Logic Output B.
15	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2. This pin requires a 0.1 µF bypass capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

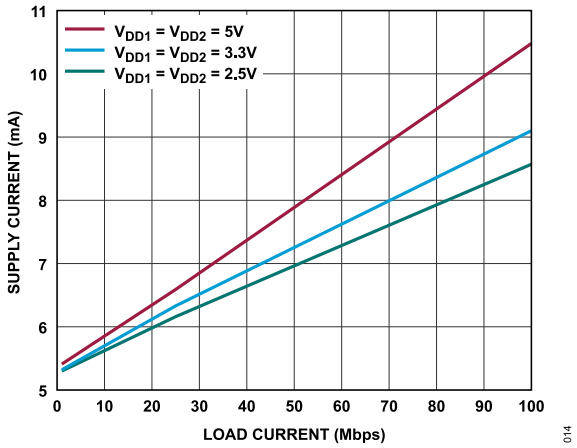

Figure 4. ADuM362N I_{DD1} Supply Current vs. Data Rate at Various Voltages

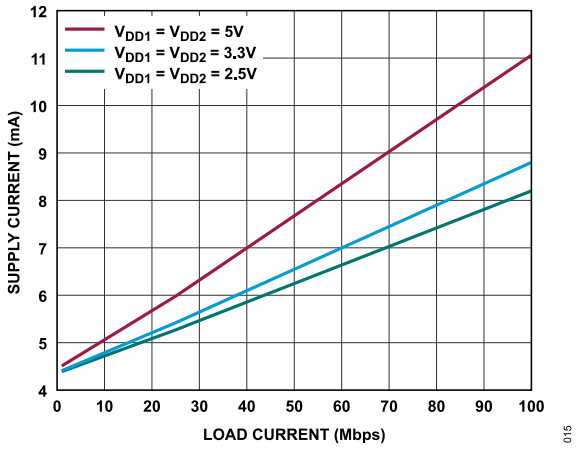

Figure 5. ADuM362N I_{DD2} Supply Current vs. Data Rate at Various Voltages

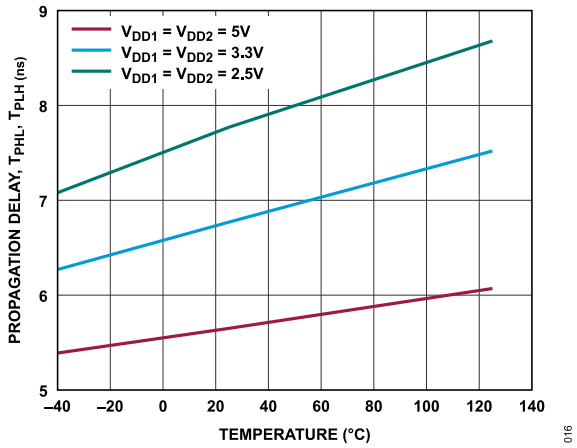

Figure 6. Propagation Delay, t_{PLH}, t_{PHL} vs. Temperature at Various Voltages

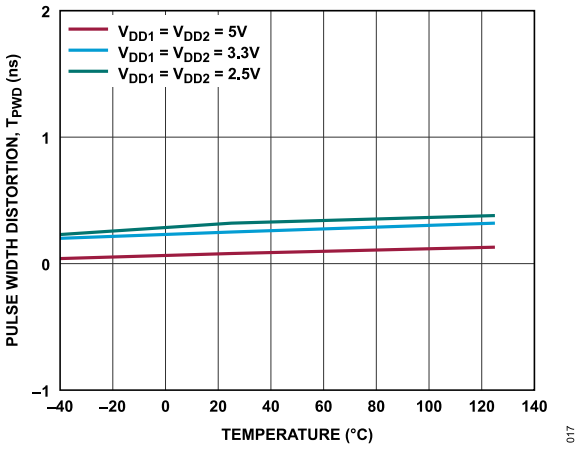

Figure 7. Pulse-Width Distortion, t_{PWD} vs. Temperature at Various Voltages

THEORY OF OPERATION

The ADuM362N utilizes a high frequency carrier to transmit data across the isolation barrier by *i*Coupler chip-scale transformer coils separated by layers of polyimide isolation. Using an on/off keying (OOK) technique and the differential architecture, as shown in Figure 8 and Figure 9, the ADuM362N has very-low propagation delay and supports high speed operation.

There is no interdependency between the V_{DD1} and V_{DD2} supplies. The device can simultaneously operate at any voltage within the specified operating ranges and can sequence in any order. This feature enables the isolator to perform voltage translation of 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient (CMTI) immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

Figure 8 shows the waveforms for the ADuM362N when the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the low fail-safe output state ADuM362N0 sets the output to low. For the ADuM362N that have a high fail-safe output state, Figure 9 shows the conditions where the carrier waveform is off when the input state is high. When the input side is off or not operating, the high fail-safe output state ADuM362N1 sets the output to high. For the model numbers that have the fail-safe output state of low or the fail-safe output state of high, see Figure 17.

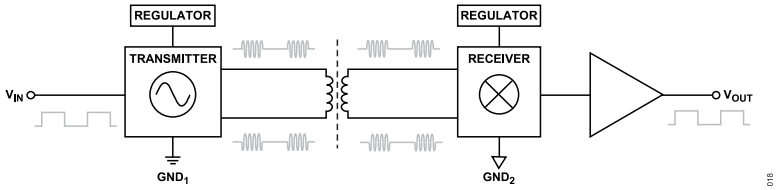

Figure 8. Operational Block Diagram of a Single-Channel with a Low Fail-Safe Output State

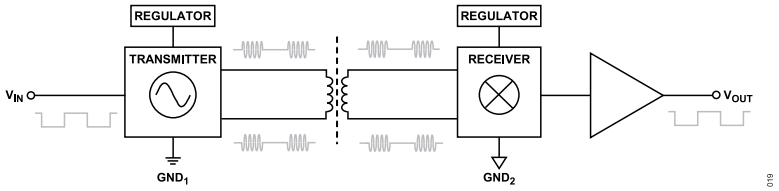

Figure 9. Operational Block Diagram of a Single-Channel with a High Fail-Safe Output State

THEORY OF OPERATION

TRUTH TABLE

Table 14. ADuM362N Truth Table (Positive Logic)

V_{Ix} Input[1, 2]	V_{DDI} State[2]	V_{DDO} State[2]	Default Low (N0), V_{Ox} Output[1, 2, 3]	Default High (N1), V_{Ox} Output[1, 2, 3]	Test Conditions/ Comments
L	Powered	Powered	L	L	Normal operation
H	Powered	Powered	H	H	Normal operation
L	Undervoltage	Powered	L	H	Fail-safe output
X[4]	Powered	Undervoltage	Indeterminate	Indeterminate	

[1] L means low, H means high, X means don't care, NC means not connected, and Z means high impedance within one diode drop of GND_x.

[2] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, D, E, or F). V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

[3] N0 refers to ADuM362N0 models, and N1 refers to ADuM362N1 models. For more details, see the Ordering Guide section.

[4] Input pins (V_{Ix} on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry).

I/O Schematics

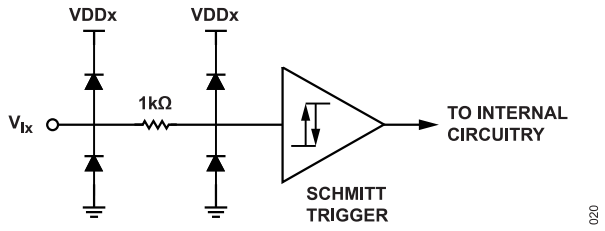

Figure 10. V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{IE}, V_{IF} Input Schematics

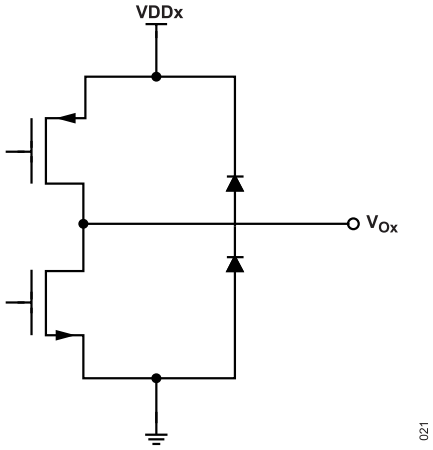

Figure 11. V_{OA}, V_{OB}, V_{OC}, V_{OD}, V_{OE}, V_{OF} Output Schematics

APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM362N digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 12). Connect the bypass capacitors in between Pin 1 and Pin 8 for V_{DD1} and between Pin 9 and Pin 16 for V_{DD2}. The required bypass capacitor value is between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm. Low ESR capacitors are important for direct power injection (DPI) and CMTI performance.

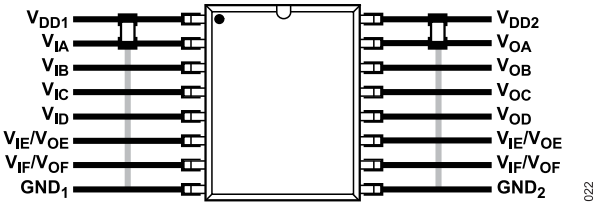

Figure 12. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this design can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latchup or permanent damage (see Table 10).

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time required for a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

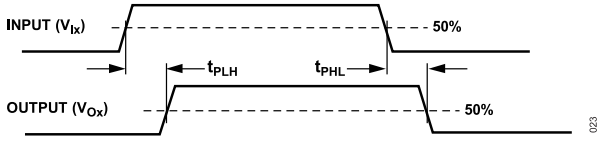

Figure 13. Propagation Delay Parameters

PWD is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel matching is the maximum amount the propagation delay differs between channels within a single ADuM362N component.

Propagation delay skew is the maximum amount the propagation delay differs between multiple ADuM362N components operating under the same conditions.

JITTER MEASUREMENT

Figure 14 shows the resulting eye diagram for the ADuM362N. The measurement is taken by using a Keysight 81160A pulse pattern generator at 100 Mbps with a pseudorandom bit sequence (PRBS15) input. Jitter is measured using the Tektronix 6 Series B mixed-signal oscilloscope, with a TAP1500 probe and using the Tektronix jitter and analysis software. The 10% to 90% rise and fall times of the input signal from the generator approximately equals 1.2 ns. The result shows a typical output eye diagram measured on the ADuM362N. Figure 14 shows the random and deterministic jitter characteristics for a PRBS input.

Total Jitter is evaluated at a BER of 1×10^{-12} and calculated for a PRBS input with and without the effects of crosstalk. The total jitter measurement without crosstalk consists of examining one channels input, while the adjacent channels inputs are grounded. The jitter measurement with crosstalk consists of all channels switching simultaneously at the same rate.

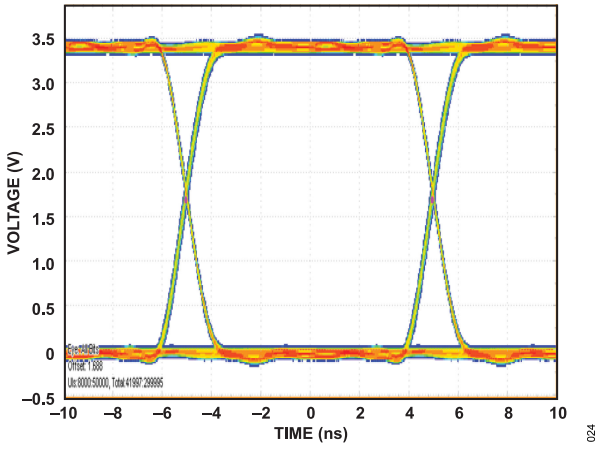

Figure 14. ADuM362N Output-Channel Eye Diagram (V_{DD1} = V_{DD2} = 3.3 V, 100 Mbps, T_A = 25°C, C_L = 15 pF, PRBS15 Input)

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking, and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

APPLICATIONS INFORMATION

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total RMS voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADuM362N isolator are shown in Table 7.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as DC stress, which causes very little wear out because there is no displacement current, and an AC component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz AC and DC across the barrier as shown in Equation 1. Because only the AC portion of the stress causes wear out, the equation can be rearranged to solve for the AC RMS voltage, as is shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the AC RMS voltage determines the product lifetime.

$$V_{RMS} = \sqrt{{V_{AC\,RMS}}^2 + {V_{DC}}^2} \quad (1)$$

or

$$V_{AC\,RMS} = \sqrt{{V_{RMS}}^2 - {V_{DC}}^2} \quad (2)$$

where:
V_{RMS} is the total RMS working voltage.
$V_{AC\,RMS}$ is the time varying portion of the working voltage.
V_{DC} is the DC offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power-conversion applications. Assume that the line voltage on one side of the isolation is 240 V AC rms and a 400 V DC bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 15 and the following equations.

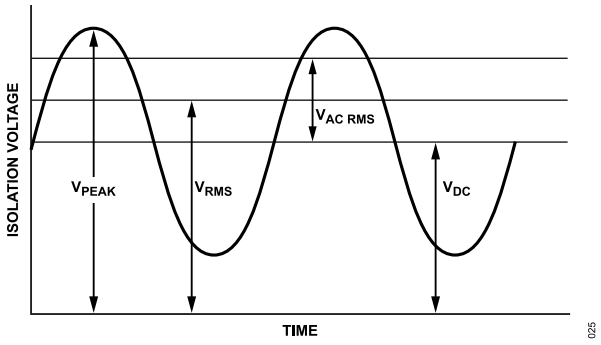

Figure 15. Critical Voltage Example

The working voltage across the barrier from Equation 1 is:

$$V_{RMS} = \sqrt{{V_{AC\,RMS}}^2 + {V_{DC}}^2}$$
$$V_{RMS} = \sqrt{240^2 + 400^2} \quad (3)$$
$$V_{RMS} = 466 \text{ V}$$

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the AC RMS voltage, use Equation 2:

$$V_{AC\,RMS} = \sqrt{{V_{RMS}}^2 - {V_{DC}}^2}$$
$$V_{AC\,RMS} = \sqrt{466^2 - 400^2} \quad (4)$$
$$V_{AC\,RMS} = 240 \text{ V rms}$$

In this case, the AC RMS voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 11 for the expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the DC working voltage limit in Table 11 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

OUTLINE DIMENSIONS

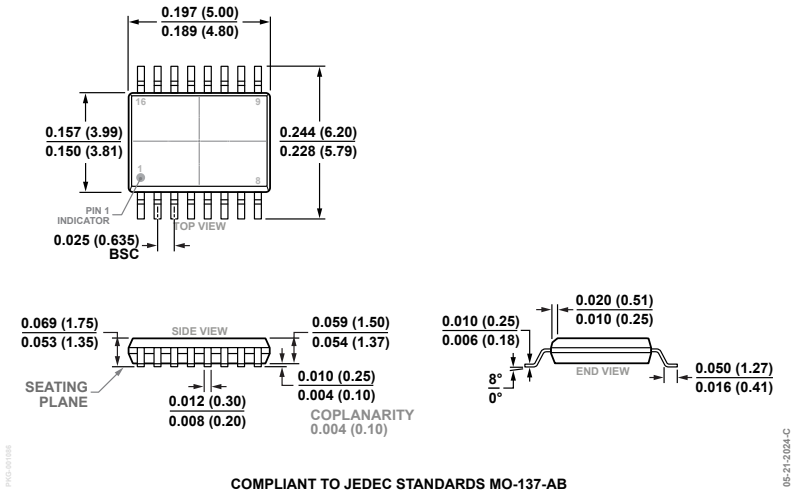

Figure 16. 16-Lead Shrink Small-Outline Package [QSOP]
(RQ-16)
Dimensions Shown in inches and (millimeters)

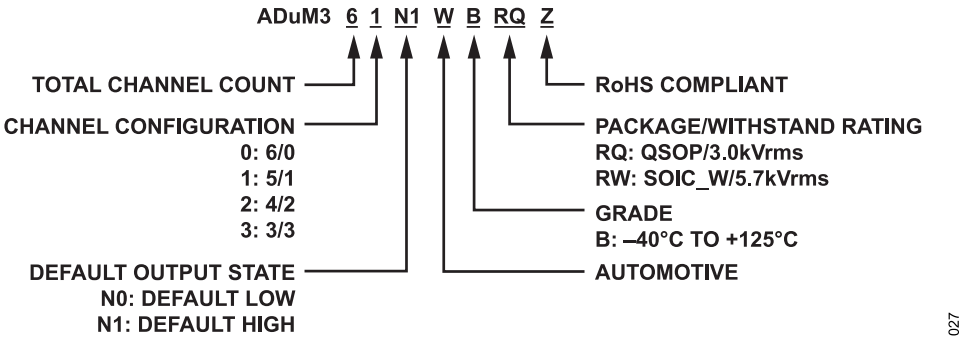

Figure 17. Product Selector Guide

OUTLINE DIMENSIONS

Updated: September 17, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADuM362N0BRQZ	−40°C to +125°C	16-Lead [QSOP]	Tube, 98	RQ-16
ADuM362N0BRQZ-RL7	−40°C to +125°C	16-Lead [QSOP]	Reel, 1000	RQ-16
ADuM362N1BRQZ	−40°C to +125°C	16-Lead [QSOP]	Tube, 98	RQ-16
ADuM362N1BRQZ-RL7	−40°C to +125°C	16-Lead [QSOP]	Reel, 1000	RQ-16

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADuM36xNEBZ	Evaluation Board for the ADuM362N

[1] Z = RoHS-Compliant Part.

AUTOMOTIVE PRODUCTS

The ADuM362N0W/ADuM362N1W models will be available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers must review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact the local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.