Isolated, Half-Bridge Gate Driver with Adjustable Dead Time, 10A Output

FEATURES

- 10A peak current (< 1.1Ω R_{DSON_x})
- Precise timing characteristics
  - 41ns max propagation delay over specified temperature range
  - 6.3ns maximum channel-to-channel matching
- High common-mode transient immunity (CMTI): >210kV/µs
- 4.5V to 28V driver side supply voltage
- Multiple UVLO options for driver side supplies:
  - Grade A: 4.5V maximum
  - Grade B: 7.6V maximum
- UVLO V_{DD1} positive going threshold: 2.25V maximum
- Adjustable dead time control
- CMOS input logic levels
- High junction temperature operation: 150°C
- Safety and regulatory approvals
  - UL1577
    - V_{ISO} = 3000V_{RMS} for 1 minute
  - EN/IEC 62368-1
  - EN/IEC 61010-1
  - IEC 60747-17 (VDE 0884-17) (pending)
    - VIORM = 1200Vpeak
  - GB4943.1
- 16-lead, RoHS compliant, SOIC_N package (4.0mm creepage)

APPLICATIONS

- IGBT, SiC, GaN applications
- AC-DC and DC-DC power supplies
- Uninterruptable power supplies (UPS)
- Industrial motor drives
- Industrial inverters

GENERAL DESCRIPTION

The ADuM3250 is a 10A isolated, dual channel/half bridge gate driver that employs Analog Devices, Inc., *i*Coupler® technology to provide a precision timing across the isolation barrier.

Thanks to its strong gate driver capability and precise timing performance, the ADuM3250 is ideal for applications using insulated-gate bipolar transistors (IGBTs) and metal-oxide semiconductor field effect transistors (MOSFETs), as well as wide-bandgap devices such as silicon carbide (SiC) and gallium nitride (GaN) switches, with a maximum recommended switching frequency of up to 1MHz. ADuM3250 provides 1200V_{PK} isolation and comes with small outline integrated circuit (SOIC)-16 package with 4.0mm creepage.

The ADuM3250 secondary side supplies (V_{DDA}, V_{DDB}) support up to 28V. To ensure compatibility and optimal performance across different power switches technologies, ADuM3250 is available in two different undervoltage lock-out (UVLO) options on V_{DDA} and V_{DDB}.

Additional features include a DISABLE pin, which can force the output to a low state, and a dead-time control pin (DT) that prevents simultaneous activation of both channels, thereby avoiding shoot-through conditions.

FUNCTIONAL BLOCK DIAGRAM

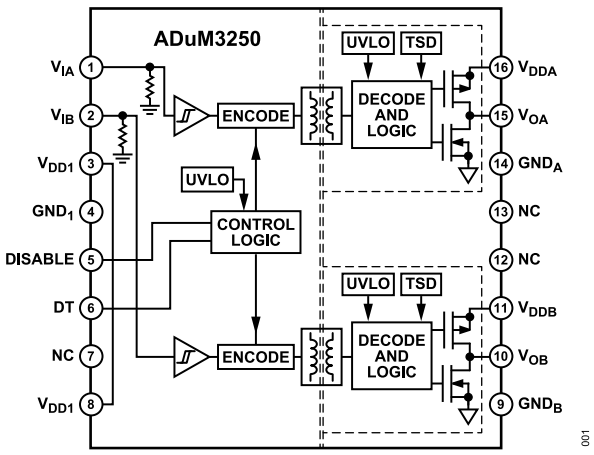


Figure 1. ADuM3250 Functional Block Diagram

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REVISION HISTORY

10/2026—Rev. 0 to Rev. A

Change to Features ... 1
Change to General Description ... 1
Changes to Electrical Characteristics ... 3
Changes to PCB Layout ... 16
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10/2026—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD1} referenced to GND_1, V_{DDA}, V_{DDB} referenced respectively to GND_A and GND_B, 2.25V ≤ V_{DD1} ≤ 5.5V, 4.5V ≤ V_{DDA},V_{DDB} ≤ 28V, and T_J = −40°C to +150°C, unless otherwise noted. All minimum and maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_J = 25°C, V_{DD1} = 5.0V, and V_{DDA} = V_{DDB} = 15V.

Table 1. ADuM3250 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic Input Voltage	V_{DD1}	2.25		5.5	V	
Output Supply Voltage	V_{DDA}, V_{DDB}	4.5		28	V	
Undervoltage Lock-Out (UVLO)						
V_{DD1} Positive Going Threshold	$V_{VDD1UV+}$		2.0	2.2	V	
V_{DD1} Negative Going Threshold	$V_{VDD1UV-}$	1.65	1.8		V	
V_{DD1} Hysteresis	$V_{VDD1UVH}$		0.2		V	
V_{DDA} and V_{DDB}Positive Going Threshold	$V_{VDDAUV+}$, $V_{VDDBUV+}$		4.3	4.5	V	Grade A
			7.2	7.6	V	Grade B
V_{DDA} and V_{DDB} Negative Going Threshold	$V_{VDDAUV-}$, $V_{VDDBUV-}$	3.9	4.1		V	Grade A
		6.7	7.0		V	Grade B
V_{DDA} and V_{DDB} Hysteresis	$V_{VDDAUVH}$, $V_{VDDBUVH}$		0.2		V	Grade A
			0.2		V	Grade B
Input Supply Current, Quiescent	$I_{DD1 (Q)}$					
V_{IA} High or V_{IB} High			2.25	3.2	mA	
Both Inputs Low			0.43	1	mA	DT = V_{DD1} (dead time disabled)
Both Inputs High			3.68	6	mA	DT = V_{DD1} (dead time disabled)
Input Currents	I_{IA}, I_{IB}			14	µA	V_{IA} = V_{IB} = V_{DD1}
Input Voltage						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DD1}			V	
Logic Low	V_{IL}			0.3 × V_{DD1}	V	
DT Disable Threshold						
Logic High		0.8 × V_{DD1}			V	
Hysteresis			0.14 × V_{DD1}		V	
Output Supply Current, Per Channel, Quiescent	$I_{DD2 (Q)}$					
Output Channel						
High			1.7	2.5	mA	V_{IA} = V_{IB} = V_{DD1}
Low			1.5	2.5	mA	V_{IA} = V_{IB} = GND_1
Thermal Shutdown (TSD)						
Positive Edge	T_{TSD_POS}		165		°C	
Hysteresis	T_{TSD_HYST}		20		°C	
Drive Strength						
Pull-Down On Resistance	R_{DSON_N}			0.7	Ω	Tested at 250mA, V_{DDx} = 15V
				0.7	Ω	Tested at 1A, V_{DDx} = 15V
Pull-Up On Resistance	R_{DSON_P}			1.1	Ω	Tested at 250mA, V_{DDx} = 15V
				1.1	Ω	Tested at 1A, V_{DDx} = 15V
Peak Current	I_{PEAK}		10		A	V_{DDA}, V_{DDB} = 15V, 0.1Ω gate resistance
SWITCHING SPECIFICATIONS						
Pulse Width[1]	t_{PW_MIN}	10	15		ns	Load capacitance (C_L) = 2.2nF, V_{DD1} = 5V, V_{DDA} and V_{DDB} = 15V, external gate resistor (R_G) = 1Ω

SPECIFICATIONS

Table 1. ADuM3250 Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Propagation Delay[2]						
Rising Edge	t_{DLH}	20	25	41	ns	
Falling Edge	t_{DHL}	20	23	41	ns	
Time to Disable	t_{DIS}	20	26	41	ns	
Time to Enable	t_{EN}	20	26	41	ns	
Delay Skew[3]	t_{PSK}			6.5	ns	C_L = 2.2nF, R_G = 5.1Ω
Pulse Width Distortion	t_{PWD}			6	ns	C_L = 2.2nF, R_G = 5.1Ω
Channel-to-Channel Matching[4]	t_{PSKCD}			6.3	ns	C_L = 2.2nF, R_G = 5.1Ω
Output Rise and Fall Time (10% to 90%)	t_R/t_F		25	32	ns	C_L = 2.2nF, V_{DD1} = 5V, V_{DDA} and V_{DDB} = 15V, R_G = 5.1Ω, see Figure 19
Adjustable Dead Time	DT					C_L = 2.2nF, V_{DD1} = 5V, V_{DDA} and V_{DDB} = 15V, R_G = 5.1Ω
		2200	2320	2960	ns	Dead-time resistor (R_{DT}) = 500kΩ
		58	62	90	ns	R_{DT} = 10kΩ
Common-Mode Transient Immunity	CMTI					
Static		−210		+210	kV/µs	Guaranteed by characterization; not production tested
Dynamic		−210		+210	kV/µs	Guaranteed by characterization; not production tested

[1] t_{PW_MIN} refers to the shortest duration of a signal on V_{Ix} that allows the output to change state. Input signals with duration lower than t_{PW_MIN} do not produce any change on V_{Ox} outputs.

[2] t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% level of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the VOx signal. See Figure 19 for the waveforms of the propagation delay parameters.

[3] t_{PSK} is the magnitude of the worst case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 19 for the waveforms of the propagation delay parameters.

[4] Channel-to-channel matching is the absolute value of the difference in propagation delays between two channels on a single device.

INSULATION CHARACTERISTICS

The ADuM3250 is suitable for reinforced electrical insulation only within the safety ratings, as shown in Figure 2. Maintenance of the safety ratings is ensured by protective circuits.

Table 2. ADuM3250, 16-Lead Narrow-Body SOIC [SOIC_N] (R-16) Insulation Characteristics

Parameter	Symbol	Value	Unit	Conditions
General				
Minimum external clearance distance	CLR	4.0	mm	Pin to pin air distance across package
Minimum external creepage distance	CRP	4.0	mm	Pin to pin surface distance across package
Distance through insulation	DTI	42.0	µm	Minimum internal
Comparative tracking index	CTI	>600	V	Per IEC 60112
Material Group		I		Per IEC 60664-1
Overvoltage category per IEC 60664-1		I-IV		Rated mains voltage ≤ 150V_{RMS}
		I-III		Rated mains voltage ≤ 300V_{RMS}
		I-II		Rated mains voltage ≤ 600V_{RMS}
Safety Limiting Values				
Maximum ambient safety temperature	T_S	150	°C	
Maximum total power dissipation	P_{TOT}	1.49	W	T_A = 25°C, P_{TOT} = P_{SI} = P_{SO}
Derating above ambient	T_A	11.9	mW/°C	TA > 25°C see Figure 2
Junction to air thermal impedance	θ_{JA}	84.04	°C/W	See Table 6
IEC 60747-17 (Reinforced Insulation)				

SPECIFICATIONS

Table 2. ADuM3250, 16-Lead Narrow-Body SOIC [SOIC_N] (R-16) Insulation Characteristics (Continued)

Parameter	Symbol	Value	Unit	Conditions
Maximum repetitive peak isolation voltage	V_{IORM}	1200	V_{PK}	
Maximum isolation working voltage	V_{IOWM}	848	V_{RMS}	AC voltage, end of life test, f = 60Hz
		1200	V_{DC}	DC voltage
Maximum transient isolation voltage	V_{IOTM}	4242	V_{PK}	V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production)
Maximum impulse voltage	V_{IMP}	4242	V_{PK}	Surge voltage in air; waveform per IEC 61000-4-5
Maximum surge isolation voltage	V_{IOSM}	12800	V_{PK}	V_{TEST} ≥ 1.3 × V_{IMP} (sample test), tested in oil, waveform per IEC 61000-4-5
Apparent charge	q_{PD}	≤5	pC	Method A (type test), V_{INI} = V_{IOTM}, t_{INI} = 60s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10s
				Method B1 (100% production), V_{INI} = 1.2 × V_{IOTM}, t_{INI} = 1s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1s
Isolation capacitance	C_{IO}	1.00	pF	f = 1MHz
Isolation resistance	R_{IO}	$>10^{11}$	Ω	V_{TEST} = 500V_{DC}, T_S = 25°C, t = 60s
	R_{IO_S}	$>10^{9}$	Ω	V_{TEST} = 500V_{DC}, T_S = 150°C, t = 60s
Climatic category		40/150/21		
Pollution degree		2		
UL 1577				
Maximum withstand isolation voltage	V_{ISO}	3000	V_{RMS}	V_{TEST} = 1.2 x V_{ISO}, t = 1s (100% production)

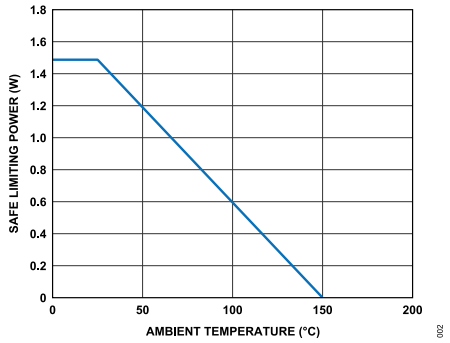


Figure 2. Thermal Derating Curve for 16-Lead Narrow-Body SOIC [SOIC_N] (R-16), Dependance of Safety Limiting Values with Ambient Temperature per IEC 60747-17

SPECIFICATIONS

REGULATORY INFORMATION

The ADuM3250 has been approved by the organizations listed in Table 3. Copies of the relevant certificates are available at Safety and Regulatory Certification for Digital Isolation.

Table 3. ADuM3250, 16-Lead Narrow-Body SOIC [SOIC_N] R-16 Package Certifications

Regulatory Agency	Standard Certification/Rating	Certificate Number
UL	UL1577 Single/basic protection, 3000V_{RMS} isolation voltage[1]	E214100
VDE	IEC 60747-17 Reinforced insulation, 1200V_{PEAK}	Pending
TÜV Süd[2]	EN/IEC 62368-1 Basic insulation at 600V_{RMS} Reinforced insulation at 300V_{RMS} EN/IEC 61010-1 Basic insulation at 600V_{RMS} from mains Reinforced insulation at 300V_{RMS} from mains	B 056232 0045
CQC	GB4943.1 Basic insulation at 300V_{RMS} Reinforced insulation at 150V_{RMS}	CQC26001520134

[1] In accordance with UL1577, each product is proof tested by applying an insulation test voltage ≥3600V_{RMS} for 1 sec.

[2] Basic and reinforced values for Pollution Degree 2, altitude ≤ 2000m, Material Group I, and Overvoltage Category II, unless otherwise noted.

RECOMMENDED OPERATING CONDITIONS

Table 4. Recommended Operating Conditions

Parameter	Rating
Operating Temperature	−40°C to +125°C
Supply Voltages	
V_{DD1}	2.25V to 5.5V
V_{DDA} and V_{DDB}	4.5V to 28V
Common-Mode Transient Immunity	
Static	±210kV/µs
Dynamic	±210kV/µs
Dead-Time Resistor Range	0Ω to 500kΩ

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5. Absolute Maximum Ratings

Parameter	Rating
Supply Voltages	
V_{DD1} to GND_1	−0.5V to +7.0V
V_{DDA} to GND_A and V_{DDB} to GND_B	−0.3V to +30V
Input[1] (V_{IA}, V_{IB}, DT, and DISABLE)	−0.5V to V_{DD1} + 0.5V
Output[2]	
V_{OA}	−0.3V to V_{DDA} + 0.3V
V_{OB}	−0.3V to V_{DDA} + 0.3V
V_{OA} transient for 200ns[3]	−2V to V_{DDA} + 0.3V
V_{OB} transient for 200ns[3]	−2V to V_{DDA} + 0.3V
Temperature Range	
Storage (T_{ST})	−55°C to +150°C
T_J	−40°C to +150°C
Common-Mode Transients[4] (CMT_H, CMT_L)	−210kV/µs to +210kV/µs

1 Rating assumes V_{DD1} is above 2.5V. V_{IA} and V_{IB} are rated up to 5.5V when V_{DD1} is unpowered.

2 Referenced to GND_A or GND_B, maximum of 30.3V.

3 Not tested in production.

4 Refers to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latchup, momentary data corruption, or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to the printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance, and Ψ_{JT} is the junction to top characterization parameter.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JT}	Unit
R-16	84.04	30.39	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

International electrotechnical commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

ESD Ratings for the ADuM3250

Table 7. ESD Ratings, R-16 [SOIC_N]

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±3500	2
CDM[1]	±1250	C3
IEC[2]	±8000	Level 4

1 With respect to local V_{DDx} and GND_x pins.

2 Across the isolation barrier between GND_1 and GND_2.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

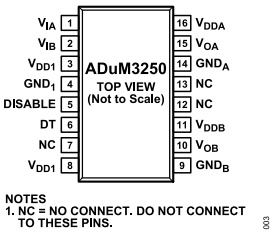


Figure 3. ADuM3250 Pin Configuration

Table 8. ADuM3250 Pin Function Descriptions

Pin Number	Mnemonic	Description
1	V_{IA}	Logic Input for Channel A.
2	V_{IB}	Logic Input for Channel B.
3, 8	V_{DD1}	Input Supply Voltage. Refer to the PCB Layout section for decoupling recommendations.
4	GND_1	Ground Reference for Input Logic Signals.
5	DISABLE	Input Disable. The DISABLE pin disables the isolator inputs and refresh circuits.
6	DT	Dead-Time Control Input. The resistor connected from the DT pin to ground sets the dead time between the output transitions. Connect the DT pin directly to V_{DD1} to disable dead-time function and allow overlap of the output signals. Do not connect external capacitance on the pin, and keep the DT to resistor routing short.
7, 12, 13	NC	No Connect. Do not connect to these pins.
9	GND_B	Ground Reference for Output B.
10	V_{OB}	Output B.
11	V_{DDB}	Output B Supply Voltage. For the correct decoupling recommendation, see the PCB Layout section.
14	GND_A	Ground Reference for Output A.
15	V_{OA}	Output A.
16	V_{DDA}	Output A Supply Voltage. For the correct decoupling recommendation, see the PCB Layout section.

ADUM3250 TRUTH TABLE

Table 9. ADuM3250 Truth Table

DISABLE	V_{IA}	V_{IB}	DT Status	V_{DD1} Status	V_{DDA}, V_{DDB} Status	V_{OA}	V_{OB}	Notes
Low	Low	Low	Enabled	Powered	Powered	Low	Low	Output transition begins after dead time expires
Low	Low	High	Enabled	Powered	Powered	Low	High	Output transition begins after dead time expires
Low	High	Low	Enabled	Powered	Powered	High	Low	Output transition begins after dead time expires
Low	High	High	Enabled	Powered	Powered	Low	Low	Output transition begins after dead time expires
Low	Low	Low	Disabled	Powered	Powered	Low	Low	The channels operate independently
Low	Low	High	Disabled	Powered	Powered	Low	High	The channels operate independently
Low	High	Low	Disabled	Powered	Powered	High	Low	The channels operate independently

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 9. ADuM3250 Truth Table (Continued)

DISABLE	V_{IA}	V_{IB}	DT Status	V_{DD1} Status	V_{DDA}, V_{DDB} Status	V_{OA}	V_{OB}	Notes
Low	High	High	Disabled	Powered	Powered	High	High	The channels operate independently
High	X[1]	X	X	Powered	Powered	Low	Low	Device is disabled
X	X	X	X	Unpowered	Powered	Low	Low	Output returns to input state after V_{DD1} power restoration
X	X	X	X	Powered	Unpowered	Low	Low	Output remains low

[1] X means "don't care".

TYPICAL PERFORMANCE CHARACTERISTICS

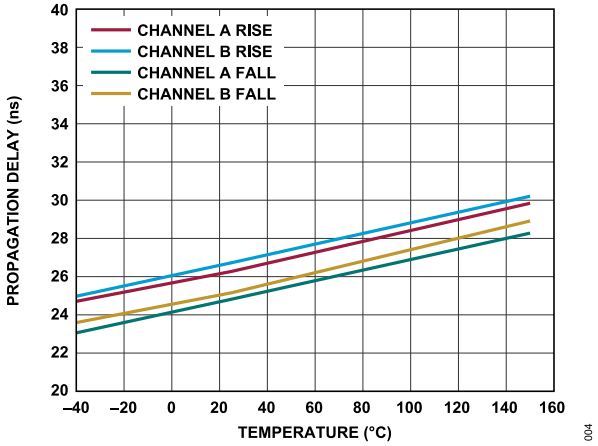


Figure 4. Propagation Delay vs. Temperature, V_{DD1} = 5V, V_{DD2} = 15V (V_{DD2} Refers to V_{DDA} or V_{DDB})

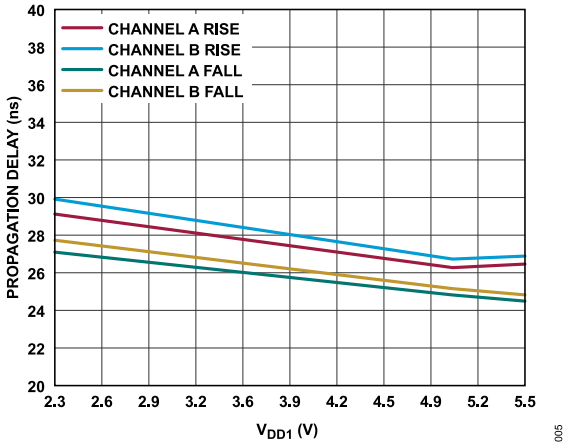


Figure 5. Propagation Delay vs. V_{DD1} Supply Voltage, Rising and Falling, V_{DD2} = 15V (V_{DD2} refers to V_{DDA} or V_{DDB})

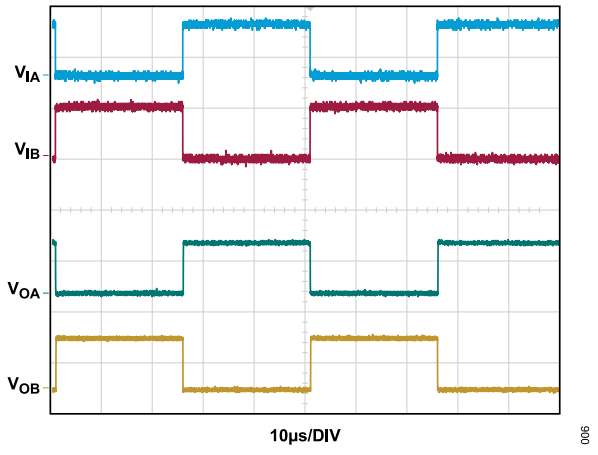


Figure 6. Input and Output Operation with Dead Time, 10kΩ Dead-Time Resistor

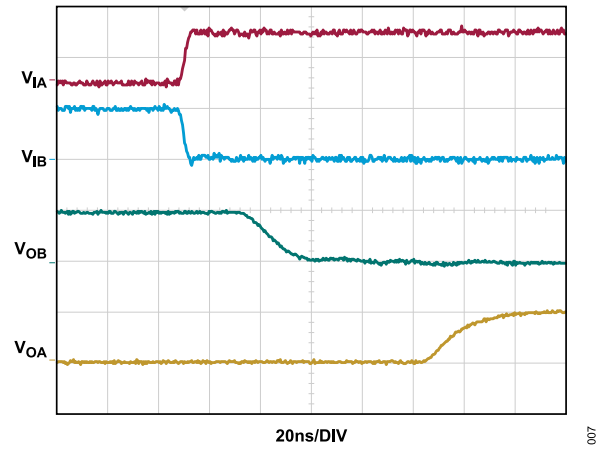


Figure 7. Input and Output Operation with Dead Time, 10kΩ Dead-Time Resistor (Detail), R_{GATE} = 5.1Ω, C_L = 2.2nF

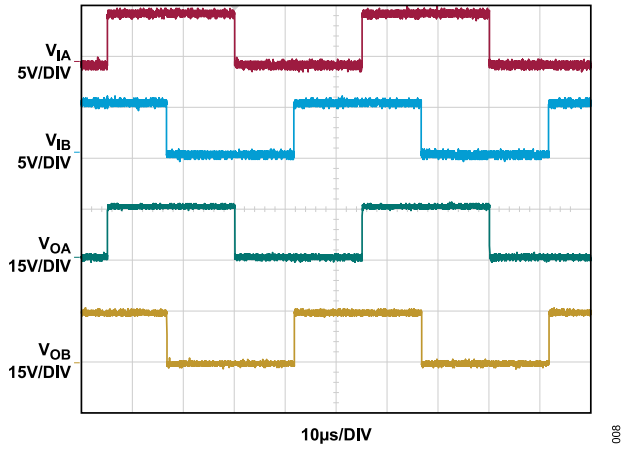


Figure 8. Input and Output Operation Without Overlap Protection

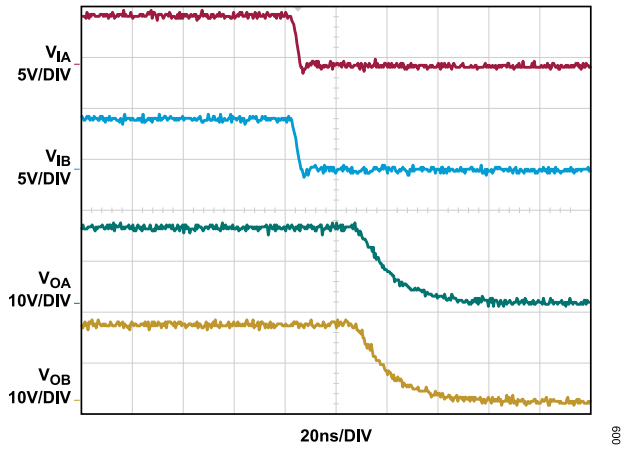


Figure 9. Input and Output Operation Without Overlap Protection (Detail), R_{GATE} = 5.1Ω, C_L = 2.2nF

TYPICAL PERFORMANCE CHARACTERISTICS

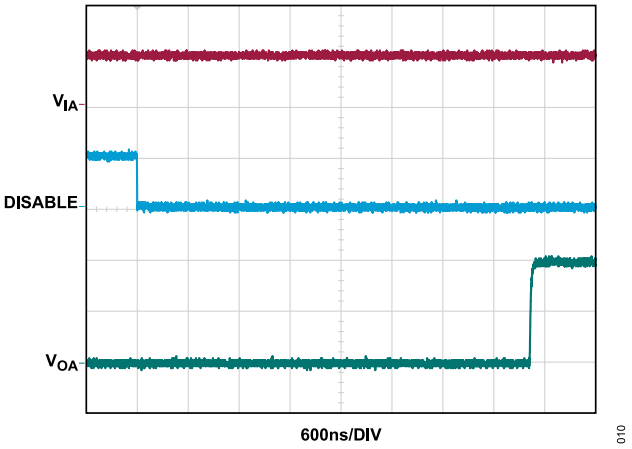


Figure 10. Typical DISABLE Delay to Output Waveform, V_{DDA} = 20V

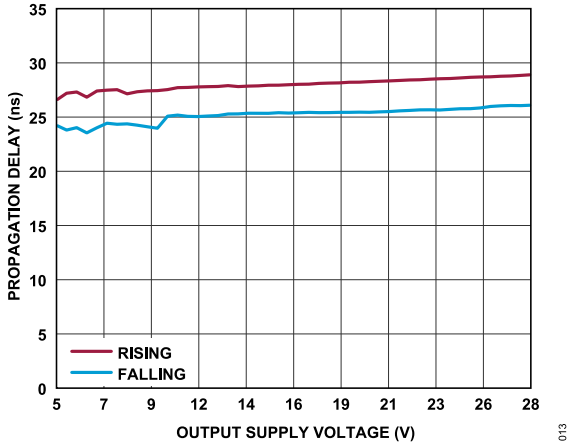


Figure 13. Propagation Delay vs. Output Supply Voltage, Rising and Falling, V_{DD1} = 5V

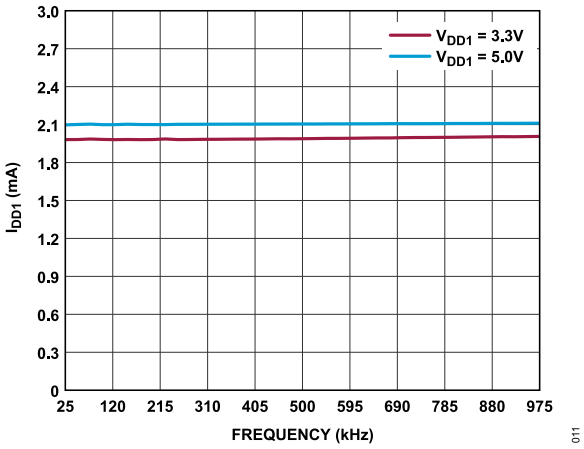


Figure 11. V_{DD1} Current (I_{DD1}) vs. Frequency for V_{DD1} = 3.3V and V_{DD1} = 5V, 50% Duty Cycle

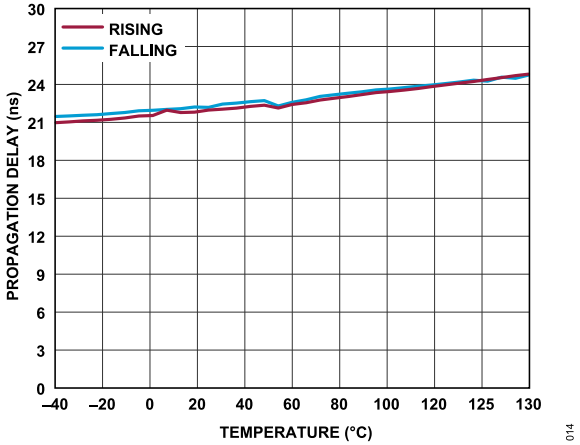


Figure 14. Propagation Delay vs. Temperature

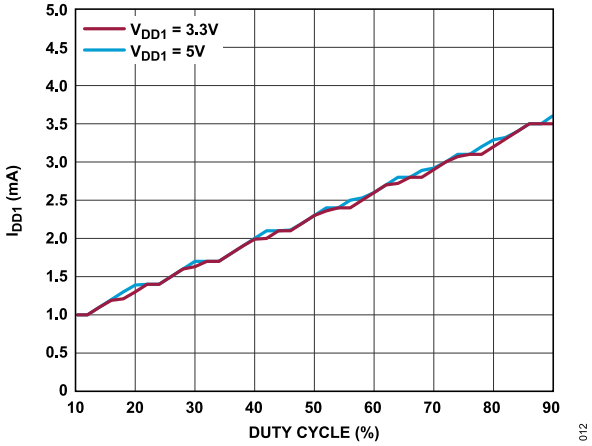


Figure 12. I_{DD1} vs. Duty Cycle for V_{DD1} = 3.3V and V_{DD1} = 5V, 20KHz

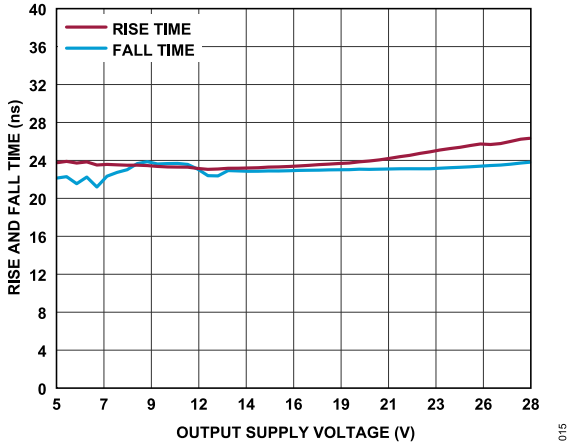


Figure 15. Rise and Fall Time vs. Output Supply Voltage, with R_G = 5.1Ω and C_L = 2.2nF

TYPICAL PERFORMANCE CHARACTERISTICS

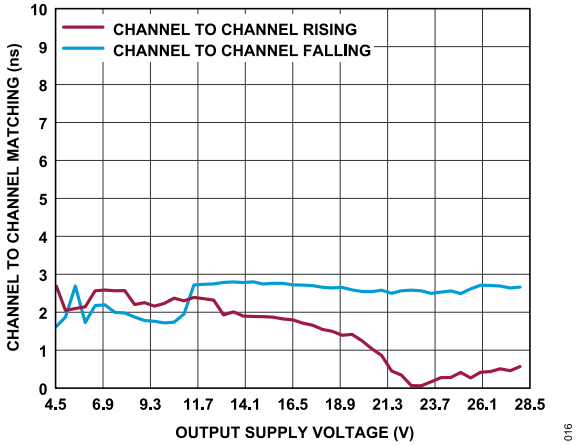


Figure 16. Channel-To-Channel Matching vs. Output Supply Voltage, Rising and Falling

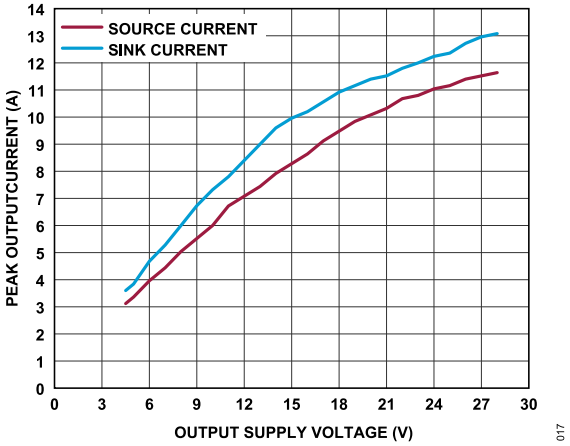


Figure 17. Peak Output Current vs. Output Supply Voltage with a 1.0Ω Series Gate Resistor

THEORY OF OPERATION

ISOLATED GATE DRIVER OPERATIONS

Gate drivers are required where fast rise times of switching device gates are desired. The gate signal for most enhancement type power devices is referred to a source or emitter node. The gate driver must have the ability to follow this source or emitter node, necessitating isolation between the controlling signal and the output of the gate driver in topologies where the source or emitter nodes swing, such as a half bridge. Gate switching times are a function of the drive strength of the gate driver. Buffer stages before a CMOS output reduce the total delay time and increase the final drive strength of the driver.

COMMUNICATION ACROSS ISOLATION BARRIER

The ADuM3250 achieves isolation between the control side and output side of the gate driver by means of a high-frequency carrier that transmits data across the isolation barrier using *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. The encoding scheme used by the ADuM3250 is a positive logic on/off keying (OOK), a high signal transmitted by the presence of the carrier frequency across the *i*Coupler chip scale transformer coils. Positive logic encoding ensures that a low signal is seen on the output when the input side of the gate driver is unpowered. A low state is the most common safe state in enhancement mode power devices, driving in situations where shoot-through conditions can exist. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques such as differential coil layout. Figure 18 illustrates the OOK encoding used by the ADuM3250.

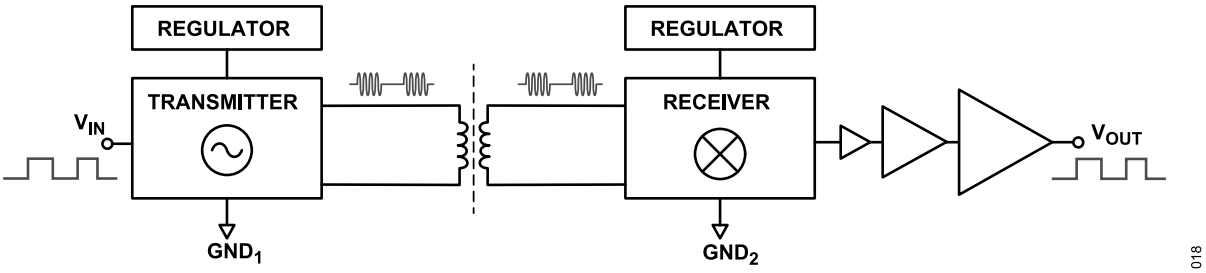


Figure 18. Operational Block Diagram of OOK Encoding (V_{IN} Is the Input Voltage, GND_2 is GND_A or GND_B, and V_{OUT} Is the Output Voltage)

THEORY OF OPERATION

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay parameter describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic-low output can differ from the propagation delay to a logic-high output. Table 1 specifies the rising edge propagation delay (t_{DLH}) as the time between the rising input high logic threshold (V_{IH}) to the output rising (t_R) 10% threshold (see Figure 19). Likewise, the falling edge propagation delay (t_{DHL}) is the time between the input falling logic-low threshold (V_{IL}) and the output falling (t_F) 90% threshold. The rise and fall times are dependent on the load conditions and are not included in the propagation delay, which is the industry standard for gate drivers.

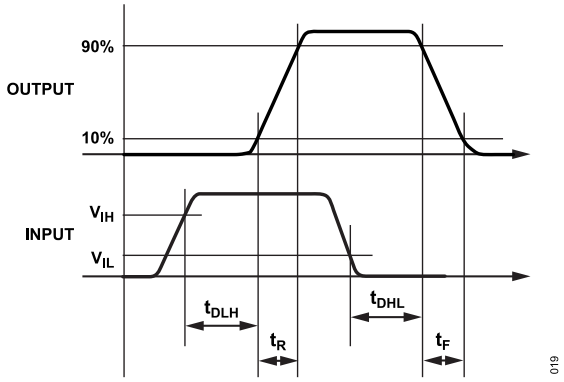


Figure 19. Propagation Delay Parameters

Channel-to-channel matching is the maximum amount that the propagation delay differs between channels within a single component.

Propagation delay skew is the maximum amount that the propagation delay differs between multiple components operating under the same conditions.

ADJUSTABLE DEAD TIME CONTROL

The ADuM3250 DT pin is used to implement an overlap protection that prevents the gate driver outputs (V_{OA} and V_{OB}) to go high at the same even if both inputs are high. It is possible to enable this function and set a fixed delay between the output high-side and low-side transitions by using a single resistor between the DT pin and ground. The relationship between R_{DT} and the obtained dead time is shown in Figure 20 and is represented by the following equation:

$$DT(ns) \approx 5 \times R_{DT}(k\Omega) \quad (1)$$

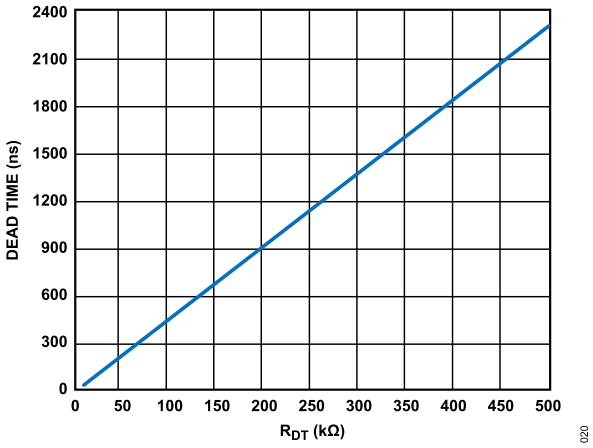


Figure 20. Dead Time vs. Dead-Time Resistor

The DT pin controls the edge transitions between V_{OA} and V_{OB} and affects only the rising edge transition of the gate drive signal. Keeping both inputs high with DT function enabled forces both outputs to low. It is possible to disable the dead time and overlap protection by connecting DT to V_{DD1}. Figure 21 shows an example of gate driver switching operation with dead time.

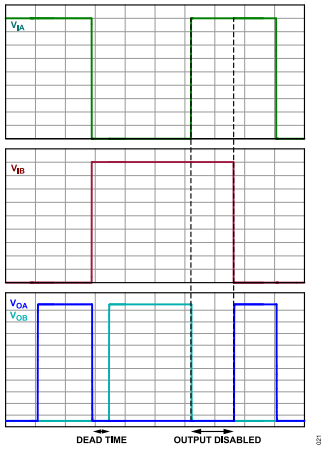


Figure 21. Dead Time Operation

PROTECTION FEATURES

Thermal Shutdown (TSD)

If the internal temperature of the ADuM3250 exceeds 165°C (typical), the device enters in thermal shutdown (TSD). During the TSD time, the gate drive is disabled and the outputs, V_{OA} and V_{OB}, are driven low. When thermal shutdown occurs, the device does not leave TSD state until the internal temperature drops below 145°C (typical), at which time, the devices exit shutdown and normal operation is restored.

Undervoltage Lock-Out (UVLO)

The ADuM3250 includes undervoltage lock-out (UVLO) protection on both the primary and secondary sides of the device. If either the primary-side or secondary-side supply voltage falls below its

THEORY OF OPERATION

respective UVLO falling-edge threshold, the gate driver outputs (V_{OA} and V_{OB}) are forced low, preventing the driven switch to be turned on during insufficient supply conditions.

Once the affected supply voltage rises above the corresponding UVLO rising-edge threshold, normal operation resumes and the outputs follow the logic state present at the input pins.

To prevent false triggering due to supply ripple or noise, hysteresis is built into the UVLO thresholds. This hysteresis ensures stable operation during slow supply ramps or in the presence of small voltage variations. The primary-side UVLO threshold levels are common across all ADuM3250 models.

POWER DISSIPATION

When driving the gate of a power switch (for example, an IGBT, SiC MOSFET, or GaN device), the gate driver dissipates power associated with charging and discharging the gate capacitance. This power dissipation can be significant and, if not properly managed, can cause the device to enter thermal shutdown (TSD).

The gate of a power transistor can be approximated as a capacitive load. Due to Miller capacitance and other nonlinear effects, a common conservative approach is to multiply the specified input capacitance of the device (C_{ISS}) by a factor of 3 to 5 to estimate the effective capacitive load. Using this approximation, the total power dissipated due to switching can be estimated by the following equation:

$$P_{DISS} = C_{EST} \times (V_{DD2} - GND_2)^2 \times f_{SW} \quad (2)$$

where:

$C_{EST} = C_{ISS} \times 5$.
V_{DD2} is V_{DDA} or V_{DDB}.
GND_2 is GND_A or GND_B.
f_{SW} is the switching frequency of the driven switch.

Alternatively, the power dissipation can be estimated using the total gate charge with the following equation:

$$P_{DISS} = Q_G \times (V_{DD2} - GND_2) \times f_{SW} \quad (3)$$

where Q_G is the total gate charge of the driven device.

The total switching power dissipation is shared between the internal on resistances of the gate driver output stages and the external gate resistors (R_{GON} and R_{GOFF}). The fraction of the total dissipation that occurs inside the device can be estimated from the ratio of the internal driver resistances to the total series resistance.

The internal power dissipation for each ADuM3250 channel can be estimated as follows:

$$P_{DISS_ADuM3250} = P_{DISS} \times \left(0.5\frac{R_{DSON_P}}{R_{GON} + R_{DSON_P}} + 0.5\frac{R_{DSON_N}}{R_{GOFF} + R_{DSON_N}}\right) \quad (4)$$

Because ADuM3250 contains two output channels, the resulting junction temperature can be estimated with the following:

$$T_{ADuM3250} = \theta_{JA} \times 2 \times P_{DISS_ADuM3250} + T_A \quad (5)$$

where:

θ_{JA} is the junction-to-ambient thermal resistance.
T_A is the ambient temperature.

For the devices to remain within specification, $T_{ADuM3250}$ must not exceed 165°C. If $T_{ADuM3250}$ exceeds the thermal shutdown positive-going threshold, the device enters the TSD state. Normal operation resumes only after the junction temperature falls below the TSD negative-going threshold.

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM3250 requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins.

Use a small ceramic capacitor with a value between 0.01µF and 0.1µF to provide a good high frequency bypass. On the output power supply pin, V_{DDA} or V_{DDB}, it is also recommended to add a 10µF capacitor to provide the charge required to drive the gate capacitance at the ADuM3250 outputs. On the output supply pin, avoid the use of vias with a bypass capacitor or use multiple vias to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin must be as short as possible. Do not connect external capacitors on DT pin.

If the dead-time control feature is used, connect a resistor between DT and GND_1, minimizing the trace length. If the dead-time control is not used, connect the DT pin to V_{DD1}.

Figure 22 and Figure 23 show two possible PCB layouts that optimize the decoupling strategy.

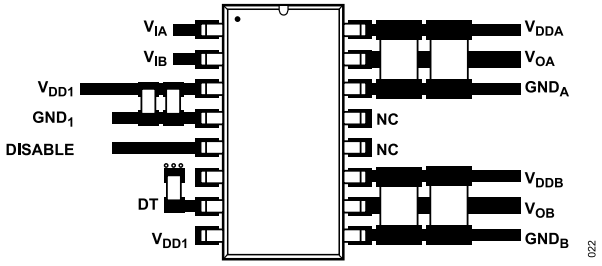


Figure 22. Layout with Output Traces Underneath Decoupling Capacitors

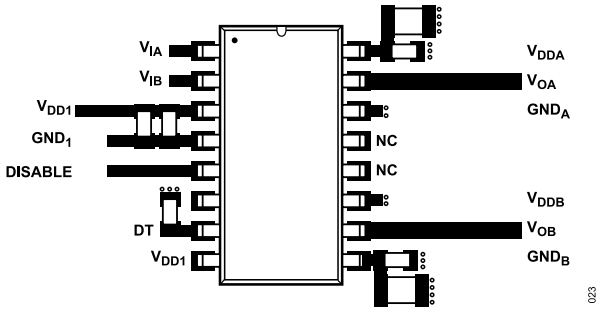


Figure 23. Layout Without Output Traces Underneath Decoupling Capacitors

OUTPUT LOAD CHARACTERISTICS

The output signals depend on the characteristics of the output load, which is typically a normally-off transistor. The driver output response to a normally-off transistor load with a gate voltage (V_{GATE}) can be modeled with a switch output resistance (R_{SW}), an inductance due to the PCB trace (L_{TRACE}), a series gate resistor (R_{GATE}), and a gate-to-source capacitance (C_{GS}), as shown in Figure 24.

R_{SW} is the switch resistance of the ADuM3250 internal driver output. R_{GATE} is the intrinsic gate resistance of the MOSFET and any external series resistance. A MOSFET that requires a 4A gate driver has a typical intrinsic gate resistance of approximately 1Ω and a C_{GS} of between 2nF and 10nF. L_{TRACE} is the inductance of the PCB trace, typically a value of 5nH or less for a well-designed layout with a short and wide connection from the ADuM3250 output to the gate of the MOSFET. The following equation defines the Q factor of the RLC circuit, which indicates how the output responds to a step change. For a well damped output, Q is less than 1.

$$Q = \frac{1}{R_{SW} + R_{GATE}} \times \sqrt{\frac{L_{TRACE}}{C_{GS}}} \quad (6)$$

Output ringing is reduced by adding a series gate resistance to dampen the response.

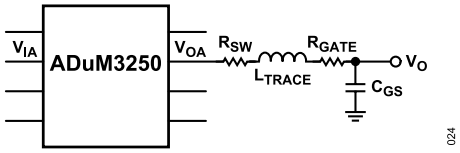


Figure 24. Resistor, Inductor, and Capacitor (RLC) Model of the Gate of an N Channel MOSFET

BOOTSTRAP AND HALF BRIDGE OPERATION

The ADuM3250 is well suited for operating two output gate signals referenced to separate grounds, as in the case for a half bridge configuration. Because isolated auxiliary supplies are often expensive, it is beneficial to reduce the amount of supplies. One method to reduce power supplies is to use a bootstrapped configuration for the high-side supply of the ADuM3250 (see Figure 25). In this topology, the decoupling capacitor (C_A) acts as the energy storage for the high-side supply and is filled whenever the low-side switch is closed, bringing GND_A to GND_B. During the C_A charging time, control the dV/dt of the V_{DDA} voltage to reduce the possibility of glitches on the output. To control the dV/dt of the V_{DDA} voltage, introduce a series resistance (R_{BOOT}) into the C_A charging path. Note that in Figure 25, D_{BOOT} is the bootstrapped diode, C_{DD1} is the decoupling capacitor on the input side, and C_B is the decoupling capacitor for the driver low-side supply.

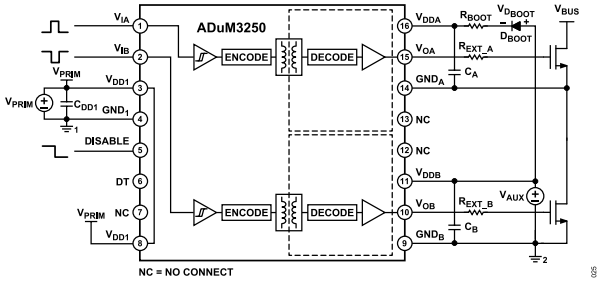


Figure 25. Circuit of Bootstrapped Half-Bridge Operation

APPLICATIONS INFORMATION

PEAK CURRENT RATING AND GATE RESISTOR SELECTION

The ADuM3250 provides two independent output channels. Each output is connected to the gate of the external power device through a series gate resistor. The internal output driver MOSFETs can source and sink peak currents greater than 10A per output (V_{OA} and V_{OB}).

In practical applications, an external series gate resistor is recommended to control the effective drive strength. The resistor limits peak gate current, reduces gate voltage overshoot, and shifts a portion of the gate-drive power dissipation away from the gate driver IC. A standard implementation using a single series gate resistor R_G is shown in Figure 26.

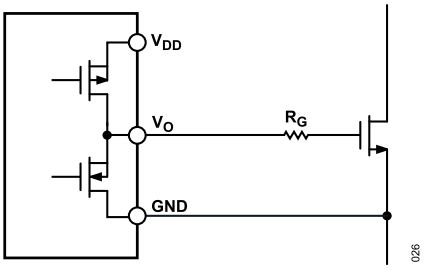


Figure 26. Single Gate Resistor Configuration

In some applications, different turn-on and turn-off switching speeds are required. This can be achieved by adding a diode in series with the gate resistor to create separate current paths for turn-on and turn-off transitions.

In the configuration shown in Figure 27, the diodes enforce unidirectional current flow. During turn-on, the gate current flows through R_{G_ON}, whereas during turn-off, the current flows through R_{G_OFF}, allowing independent optimization of the turn-on and turn-off gate resistances.

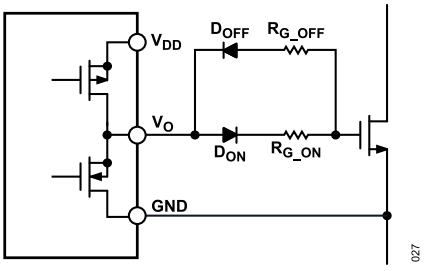


Figure 27. Two Different Turn-On and Turn-Off Current Paths Implemented Adding a Diode in Series with the Gate Resistors

Figure 28 shows an alternative implementation using a single diode. During turn-on, the gate current flows only through R1, resulting in an effective turn-on resistance of R_{ON} = R1. During turn-off, the diode becomes forward-biased and the current flows through both R_{G1} and R_{G2}, producing an effective turn-off resistance of R_{OFF} = R1 // R2.

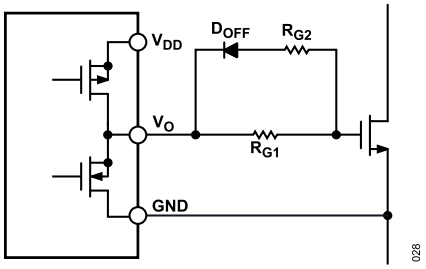


Figure 28. Two Different Turn-On and Turn-Off Current Paths Implemented Adding a Diode in Series with One Resistor

When diodes are used to force separate current paths, the gate off voltage is shifted upward by the diode forward voltage (V_F). For this reason, a low-V_F diode is recommended to provide a high voltage margin minimizing the risk of unintended turn-on of the power device.

Because part of the energy used to charge and discharge the gate capacitance is dissipated in the external gate resistor, an appropriately rated resistor must be selected. If a single resistor does not provide sufficient power dissipation capability, multiple resistors can be placed in parallel to distribute the power. Refer to Power Dissipation section for additional considerations.

APPLICATIONS INFORMATION

THERMAL ANALYSIS

The ADuM3250 consist of three internal dies attached to a split lead frame with three die attached pads. For the purposes of thermal analysis, the dies are treated as a single thermal unit, with the highest junction temperature reflected in the thermal parameter values in Table 6. The thermal parameter values are based on thermal simulations with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM3250 can operate at full load across the full temperature range without derating the output current.

θ_{JA} and θ_{JB} are mainly used to compare the thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. θ_{JA} and θ_{JB} can be used for first order approximation of the junction temperature in the system environment.

If an accurate thermal measurement of the board temperature near the device under test or directly on the package top surface operating in the system environment is available along with the corresponding device power dissipation, then using Ψ_{JB} or Ψ_{JT} is a more appropriate way to estimate the junction temperature in the system environment. Use Ψ_{JB} when the temperature measurement point is on the board or Ψ_{JT} when it is on the package top. The junction temperature is estimated using the following equation:

$$T_J + \psi_{Jx} \times P_d + T_X$$

where:

Pd is the dissipated power.
Tx is the measured temperature at location x.
x is either B for the PCB or T for the package top.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
R-16	SOIC_N	16- Lead Standard Small-Outline Package Narrow Body

For the latest package outline information and land patterns (footprints), go to Package Index.

Updated: October 16, 2026

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADUM3250ARZ	-40°C to +125°C	16-Lead SOIC	TUBE, 48	R-16
ADUM3250ARZ-RL7	-40°C to +125°C	16-Lead SOIC	REEL, 1000	R-16
ADUM3250BRZ	-40°C to +125°C	16-Lead SOIC	TUBE, 48	R-16
ADUM3250BRZ-RL7	-40°C to +125°C	16-Lead SOIC	REEL, 1000	R-16
ADUM3250CRZ	-40°C to +125°C	16-Lead SOIC	TUBE, 48	R-16
ADUM3250CRZ-RL7	-40°C to +125°C	16-Lead SOIC	REEL, 1000	R-16

[1] Z = RoHS Compliant Part.

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